



# BUK625R0-40C

N-channel TrenchMOS intermediate level FET

Rev. 1 — 17 September 2010

Product data sheet

## 1. Product profile

### 1.1 General description

Intermediate level gate drive N-channel enhancement mode Field-Effect Transistor (FET) in a plastic package using advanced TrenchMOS technology. This product has been designed and qualified to the appropriate AEC Q101 standard for use in high performance automotive applications.

### 1.2 Features and benefits

- AEC Q101 compliant
- Suitable for standard and logic level gate drive sources
- Suitable for thermally demanding environments due to 175 °C rating

### 1.3 Applications

- 12 V Automotive systems
- Electric and electro-hydraulic power steering
- Motors, lamps and solenoid control
- Start-Stop micro-hybrid applications
- Transmission control
- Ultra high performance power switching

### 1.4 Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{DS}$	drain-source voltage	$T_j \geq 25\text{ °C}$ ; $T_j \leq 175\text{ °C}$	-	-	40	V
$I_D$	drain current	$V_{GS} = 10\text{ V}$ ; $T_{mb} = 25\text{ °C}$ ; see <a href="#">Figure 1</a>	-	-	90	A
$P_{tot}$	total power dissipation	$T_{mb} = 25\text{ °C}$ ; see <a href="#">Figure 2</a>	-	-	158	W
<b>Static characteristics</b>						
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = 10\text{ V}$ ; $I_D = 25\text{ A}$ ; $T_j = 25\text{ °C}$ ; see <a href="#">Figure 11</a>	-	4.1	5	mΩ

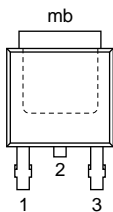
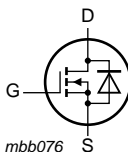
Table 1. Quick reference data ...continued

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>Avalanche ruggedness</b>						
$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	$I_D = 90\text{ A}$ ; $V_{sup} \leq 40\text{ V}$ ; $R_{GS} = 50\ \Omega$ ; $V_{GS} = 10\text{ V}$ ; $T_{j(\text{init})} = 25\text{ }^\circ\text{C}$ ; unclamped	-	-	200	mJ
<b>Dynamic characteristics</b>						
$Q_{GD}$	gate-drain charge	$I_D = 25\text{ A}$ ; $V_{DS} = 32\text{ V}$ ; $V_{GS} = 10\text{ V}$ ; see <a href="#">Figure 13</a> ; see <a href="#">Figure 14</a>	-	25.9	-	nC

[1] Continuous current is limited by package.

## 2. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	G	gate		
2	D	Drain		
3	S	source		
mb	D	mounting base; connected to drain		

**SOT428 (DPAK)**

## 3. Ordering information

Table 3. Ordering information

Type number	Package		Version
	Name	Description	
BUK625R0-40C	DPAK	plastic single-ended surface-mounted package (DPAK); 3 leads (one lead cropped)	SOT428

## 4. Limiting values

**Table 4. Limiting values**

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit	
$V_{DS}$	drain-source voltage	$T_j \geq 25\text{ °C}; T_j \leq 175\text{ °C}$	-	40	V	
$V_{GS}$	gate-source voltage	DC	[1]	-16	16	V
		Pulsed	[2]	-20	20	V
$I_D$	drain current	$T_{mb} = 25\text{ °C}; V_{GS} = 10\text{ V};$ see <a href="#">Figure 1</a>	[3]	-	90	A
		$T_{mb} = 100\text{ °C}; V_{GS} = 10\text{ V};$ see <a href="#">Figure 1</a>		-	87	A
$I_{DM}$	peak drain current	$T_{mb} = 25\text{ °C}; t_p \leq 10\text{ }\mu\text{s};$ pulsed; see <a href="#">Figure 3</a>		-	490	A
$P_{tot}$	total power dissipation	$T_{mb} = 25\text{ °C};$ see <a href="#">Figure 2</a>		-	158	W
$T_{stg}$	storage temperature		-55	175	°C	
$T_j$	junction temperature		-55	175	°C	
<b>Source-drain diode</b>						
$I_S$	source current	$T_{mb} = 25\text{ °C}$	[3]	-	90	A
$I_{SM}$	peak source current	$t_p \leq 10\text{ }\mu\text{s};$ pulsed; $T_{mb} = 25\text{ °C}$		-	490	A
<b>Avalanche ruggedness</b>						
$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	$I_D = 90\text{ A}; V_{sup} \leq 40\text{ V}; R_{GS} = 50\text{ }\Omega;$ $V_{GS} = 10\text{ V}; T_{j(init)} = 25\text{ °C};$ unclamped		-	200	mJ
$E_{DS(AL)R}$	repetitive drain-source avalanche energy		[4][5][6]	-	-	J

[1] -16V accumulated duration not to exceed 168 hrs.

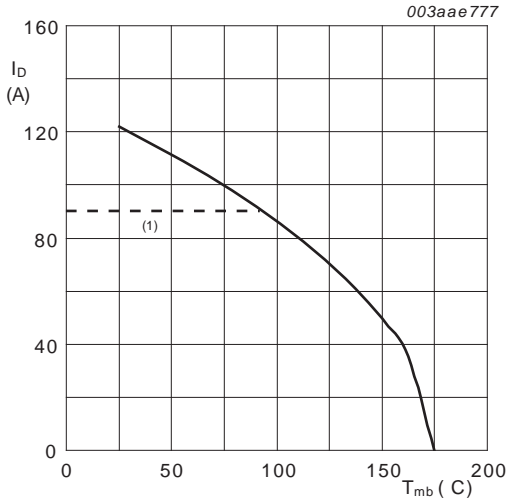
[2] Accumulated pulse duration not to exceed 5mins.

[3] Continuous current is limited by package.

[4] Single-pulse avalanche rating limited by maximum junction temperature of 175 °C.

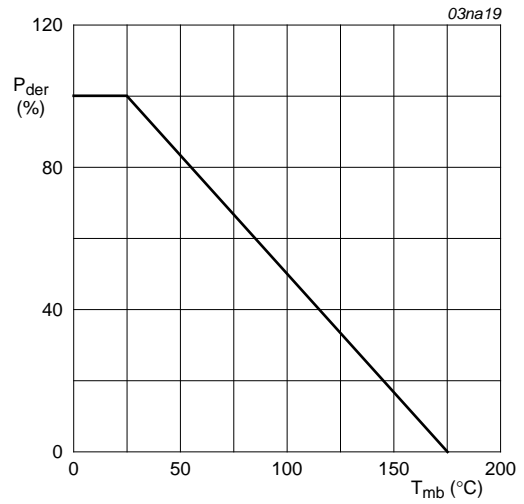
[5] Repetitive avalanche rating limited by an average junction temperature of 170 °C.

[6] Refer to application note AN10273 for further information.



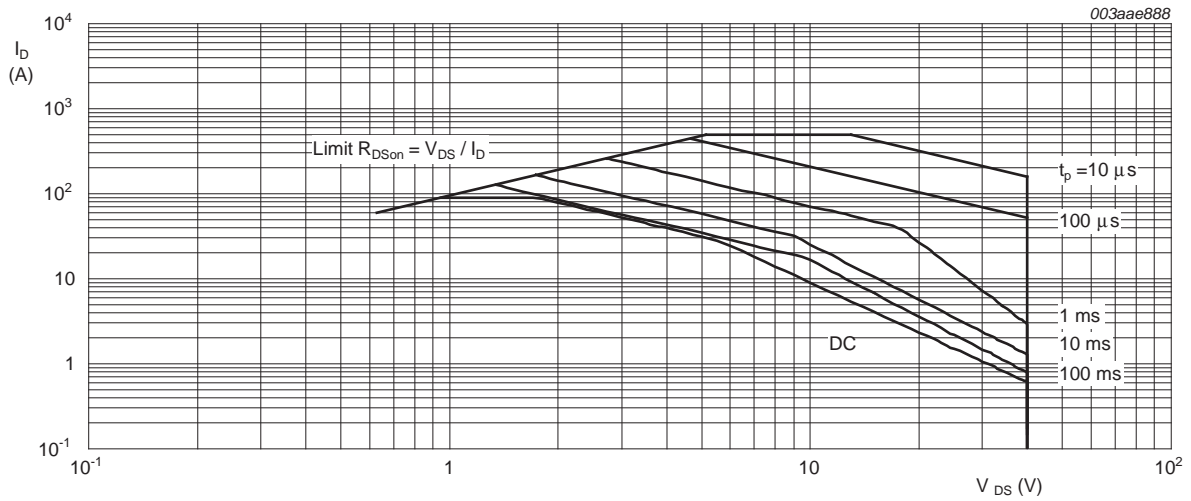
$V_{GS} \geq 10V$   
 (1) Capped at 90 A due to package.

**Fig 1. Continuous drain current as a function of mounting base temperature**



$$P_{der} = \frac{P_{tot}}{P_{tot(25^\circ C)}} \times 100\%$$

**Fig 2. Normalized total power dissipation as a function of mounting base temperature**



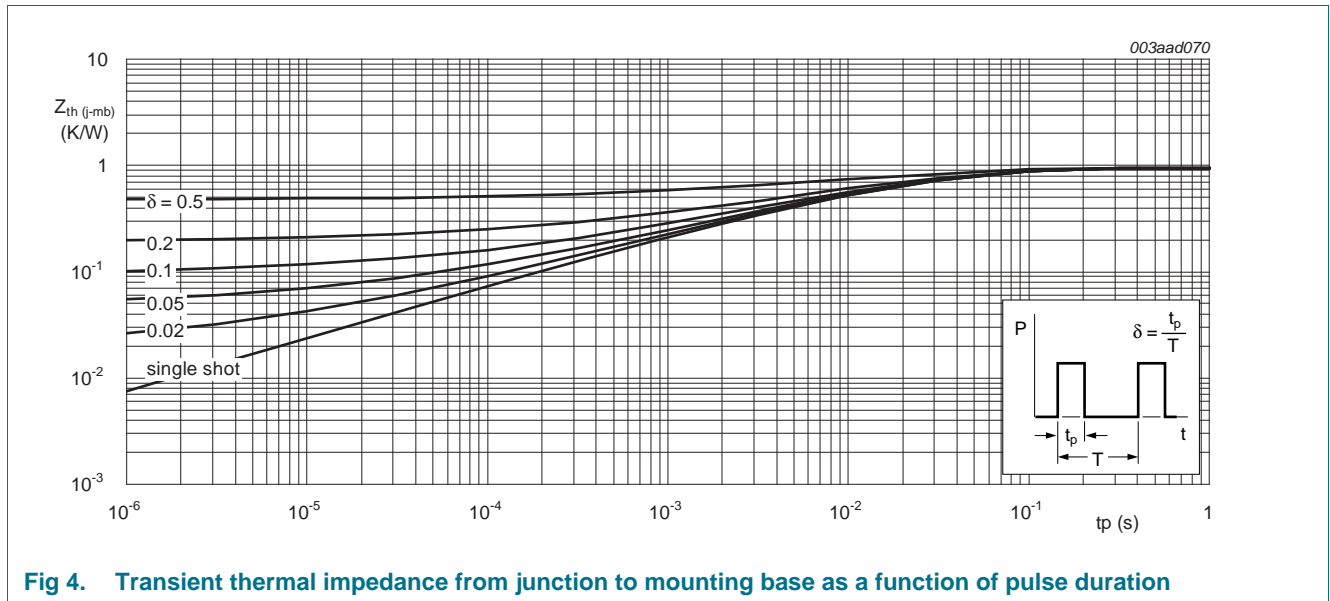
$T_{mb} = 25^\circ C; I_{DM}$  is a single pulse

**Fig 3. Safe operating area; continuous and peak drain currents as a function of drain-source voltage**

## 5. Thermal characteristics

**Table 5. Thermal characteristics**

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	see <a href="#">Figure 4</a>	-	-	0.95	K/W



**Fig 4. Transient thermal impedance from junction to mounting base as a function of pulse duration**

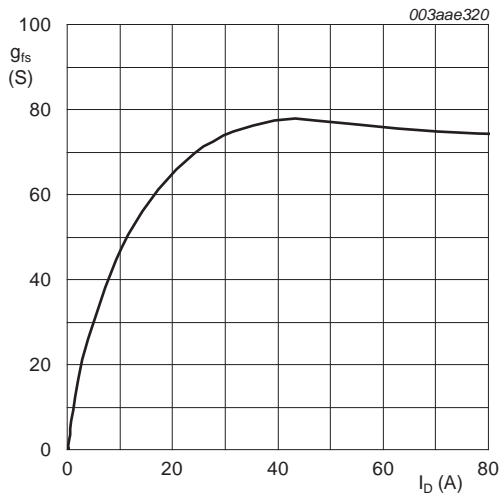
## 6. Characteristics

Table 6. Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>Static characteristics</b>						
$V_{(BR)DSS}$	drain-source breakdown voltage	$I_D = 250 \mu A$ ; $V_{GS} = 0 V$ ; $T_j = 25 \text{ }^\circ\text{C}$	40	-	-	V
		$I_D = 250 \mu A$ ; $V_{GS} = 0 V$ ; $T_j = -55 \text{ }^\circ\text{C}$	36	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	$I_D = 1 \text{ mA}$ ; $V_{DS} = V_{GS}$ ; $T_j = 25 \text{ }^\circ\text{C}$ ; see <a href="#">Figure 9</a> ; see <a href="#">Figure 10</a>	1.8	2.3	2.8	V
		$I_D = 1 \text{ mA}$ ; $V_{DS} = V_{GS}$ ; $T_j = -55 \text{ }^\circ\text{C}$ ; see <a href="#">Figure 9</a>	-	-	3.3	V
		$I_D = 1 \text{ mA}$ ; $V_{DS} = V_{GS}$ ; $T_j = 175 \text{ }^\circ\text{C}$ ; see <a href="#">Figure 9</a>	0.8	-	-	V
$I_{DSS}$	drain leakage current	$V_{DS} = 40 V$ ; $V_{GS} = 0 V$ ; $T_j = 25 \text{ }^\circ\text{C}$	-	0.02	1	$\mu A$
		$V_{DS} = 40 V$ ; $V_{GS} = 0 V$ ; $T_j = 175 \text{ }^\circ\text{C}$	-	-	500	$\mu A$
$I_{GSS}$	gate leakage current	$V_{DS} = 0 V$ ; $V_{GS} = 20 V$ ; $T_j = 25 \text{ }^\circ\text{C}$	-	2	100	nA
		$V_{DS} = 0 V$ ; $V_{GS} = -20 V$ ; $T_j = 25 \text{ }^\circ\text{C}$	-	2	100	nA
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = 10 V$ ; $I_D = 25 A$ ; $T_j = 25 \text{ }^\circ\text{C}$ ; see <a href="#">Figure 11</a>	-	4.1	5	m $\Omega$
		$V_{GS} = 5 V$ ; $I_D = 25 A$ ; $T_j = 25 \text{ }^\circ\text{C}$ ; see <a href="#">Figure 11</a>	-	5.5	6.9	m $\Omega$
		$V_{GS} = 4.5 V$ ; $I_D = 25 A$ ; $T_j = 25 \text{ }^\circ\text{C}$ ; see <a href="#">Figure 11</a>	-	6.2	8.3	m $\Omega$
		$V_{GS} = 10 V$ ; $I_D = 25 A$ ; $T_j = 175 \text{ }^\circ\text{C}$ ; see <a href="#">Figure 12</a> ; see <a href="#">Figure 11</a>	-	-	10.1	m $\Omega$
<b>Dynamic characteristics</b>						
$Q_{G(tot)}$	total gate charge	$I_D = 25 A$ ; $V_{DS} = 32 V$ ; $V_{GS} = 10 V$ ; see <a href="#">Figure 13</a> ; see <a href="#">Figure 14</a>	-	88	-	nC
		$I_D = 25 A$ ; $V_{DS} = 32 V$ ; $V_{GS} = 5 V$ ; see <a href="#">Figure 13</a> ; see <a href="#">Figure 14</a>	-	50.5	-	nC
$Q_{GS}$	gate-source charge	$I_D = 25 A$ ; $V_{DS} = 32 V$ ; $V_{GS} = 10 V$ ; see <a href="#">Figure 13</a> ; see <a href="#">Figure 14</a>	-	14.6	-	nC
$Q_{GD}$	gate-drain charge	$I_D = 25 A$ ; $V_{DS} = 32 V$ ; $V_{GS} = 10 V$ ; see <a href="#">Figure 13</a> ; see <a href="#">Figure 14</a>	-	25.9	-	nC
$C_{iss}$	input capacitance	$V_{GS} = 0 V$ ; $V_{DS} = 25 V$ ; $f = 1 \text{ MHz}$ ; $T_j = 25 \text{ }^\circ\text{C}$ ; see <a href="#">Figure 15</a>	-	3900	5200	pF
$C_{oss}$	output capacitance	$T_j = 25 \text{ }^\circ\text{C}$ ; see <a href="#">Figure 15</a>	-	512	614	pF
$C_{rss}$	reverse transfer capacitance		-	350	480	pF
$t_{d(on)}$	turn-on delay time	$V_{DS} = 30 V$ ; $R_L = 1.2 \text{ } \Omega$ ; $V_{GS} = 10 V$ ; $R_{G(ext)} = 10 \text{ } \Omega$	-	23	-	ns
$t_r$	rise time		-	52	-	ns
$t_{d(off)}$	turn-off delay time		-	164	-	ns
$t_f$	fall time		-	77	-	ns
$L_D$	internal drain inductance	from upper edge of drain mounting base to centre of die ; $T_j = 25 \text{ }^\circ\text{C}$	-	3.5	-	nH
$L_S$	internal source inductance	from source lead to source bond pad ; $T_j = 25 \text{ }^\circ\text{C}$	-	7.5	-	nH

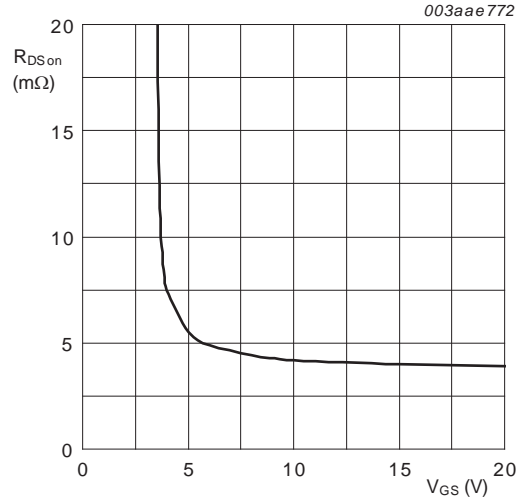
**Table 6. Characteristics ...continued**

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>Source-drain diode</b>						
$V_{SD}$	source-drain voltage	$I_S = 25\text{ A}$ ; $V_{GS} = 0\text{ V}$ ; $T_j = 25\text{ °C}$ ; see <a href="#">Figure 16</a>	-	0.85	1.2	V
$t_{rr}$	reverse recovery time	$I_S = 20\text{ A}$ ; $di_S/dt = -100\text{ A}/\mu\text{s}$ ; $V_{GS} = 0\text{ V}$ ;	-	42	-	ns
$Q_r$	recovered charge	$V_{DS} = 25\text{ V}$	-	65	-	nC



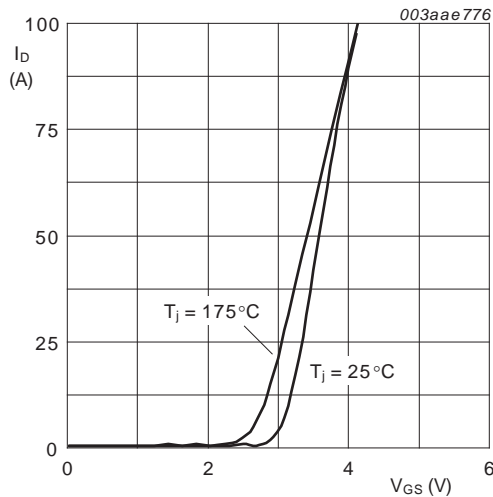
$T_j = 25\text{ °C}$ ;  $V_{DS} = 25\text{ V}$

**Fig 5. Forward transconductance as a function of drain current; typical values**



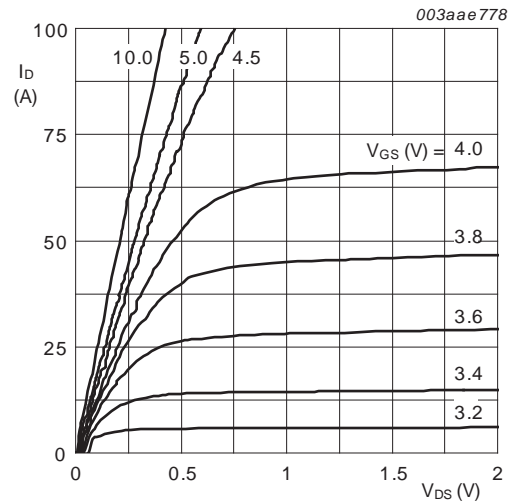
$T_j = 25\text{ °C}$ ;  $I_D = 25\text{ A}$

**Fig 6. Drain-source on-state resistance as a function of gate-source voltage; typical values**



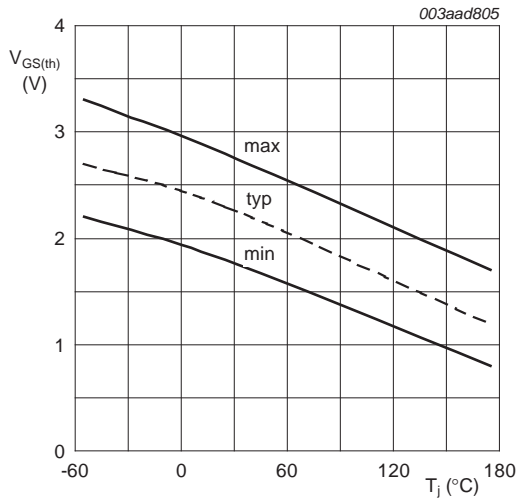
$V_{DS} > I_D \times R_{DSon}$

**Fig 7. Transfer characteristics: drain current as a function of gate-source voltage; typical values**



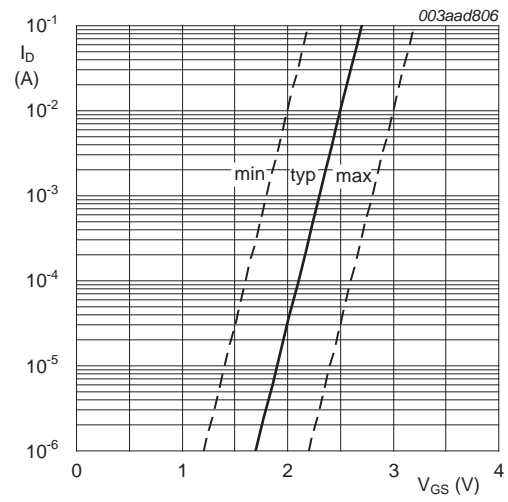
$T_j = 25\text{ °C}$

**Fig 8. Output characteristics: drain current as a function of drain-source voltage; typical values**



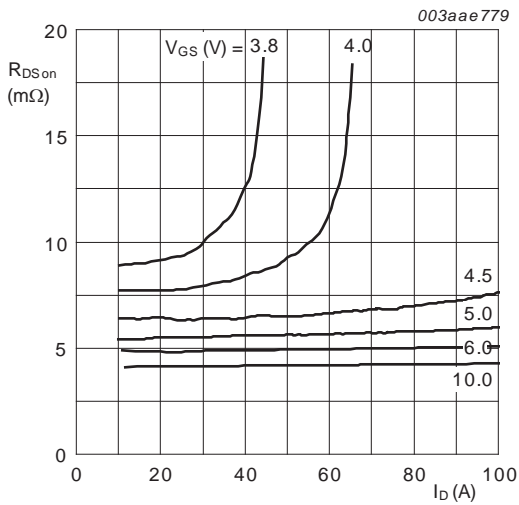
$$I_D = 1\text{mA}; V_{DS} = V_{GS}$$

**Fig 9. Gate-source threshold voltage as a function of junction temperature**



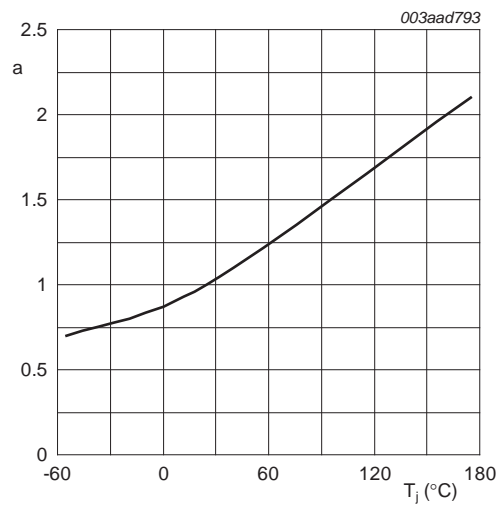
$$T_j = 25\text{ }^\circ\text{C}; V_{DS} = 5\text{V}$$

**Fig 10. Sub-threshold drain current as a function of gate-source voltage**



$$T_j = 25\text{ }^\circ\text{C}$$

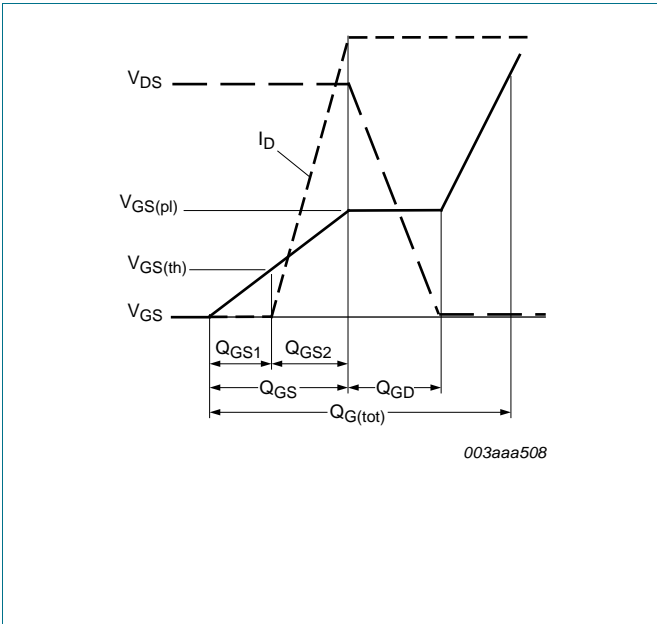
**Fig 11. Drain-source on-state resistance as a function of drain current; typical values**



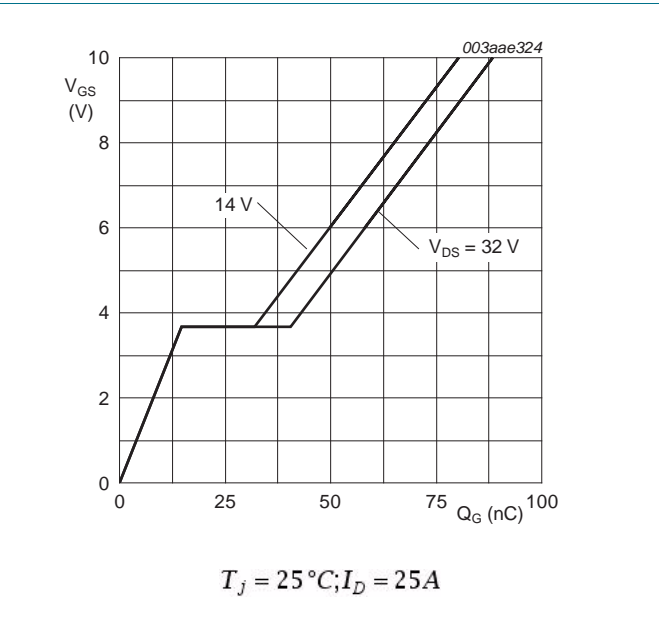
$$a = \frac{R_{DS(on)}}{R_{DS(on)25\text{ }^\circ\text{C}}}$$

**Fig 12. Normalized drain-source on-state resistance factor as a function of junction temperature**

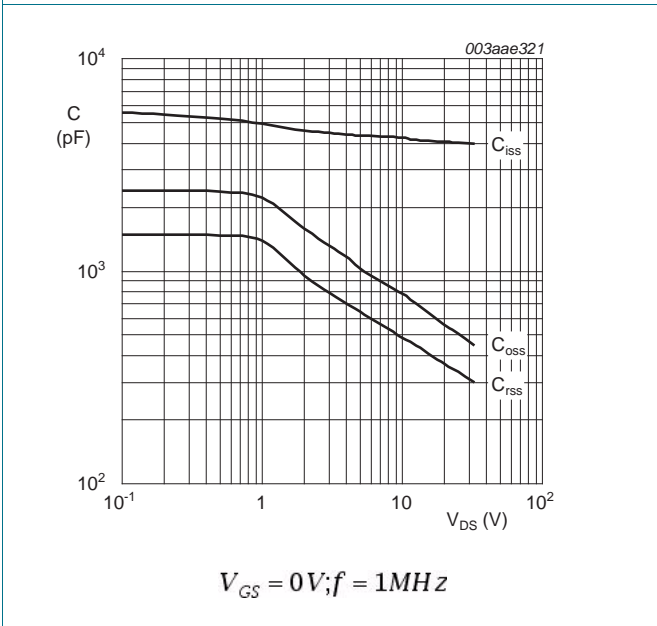




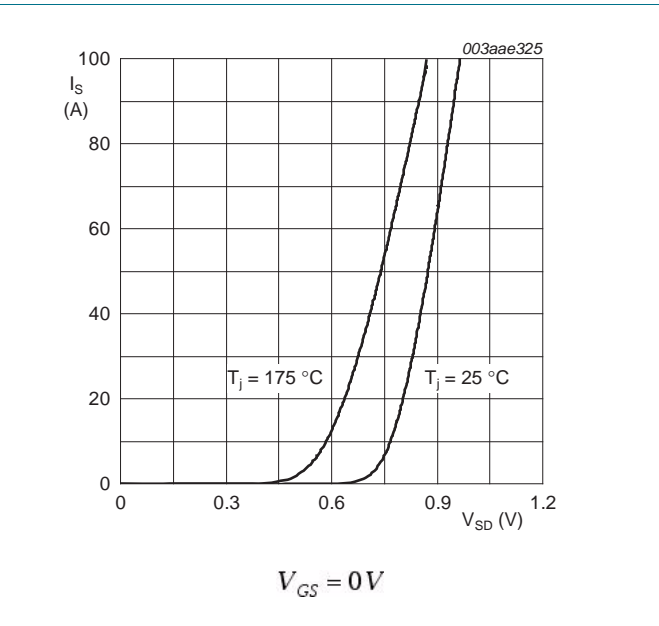
**Fig 13. Gate charge waveform definitions**



**Fig 14. Gate-source voltage as a function of gate charge; typical values**



**Fig 15. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values**



**Fig 16. Source current as a function of source-drain voltage; typical values**

**7. Package outline**

Plastic single-ended surface-mounted package (DPAK); 3 leads (one lead cropped)

SOT428

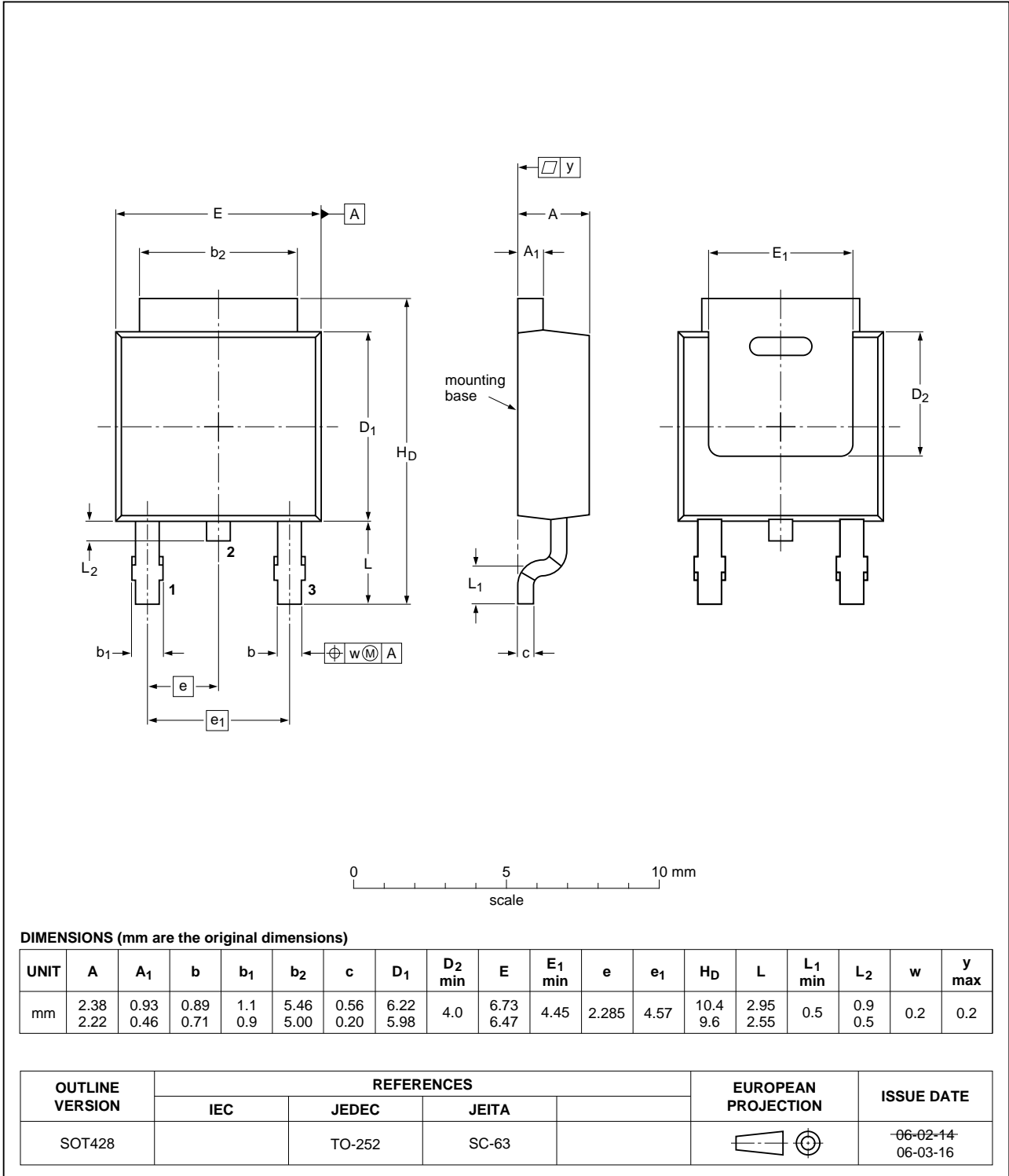


Fig 17. Package outline SOT428 (DPAK)

## 8. Revision history

Table 7. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
BUK625R0-40C v.1	20100917	Product data sheet	-	-

## 9. Legal information

### 9.1 Data sheet status

Document status <sup>[1][2]</sup>	Product status <sup>[3]</sup>	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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[IPS70R2K0CEAKMA1](#) [RJK60S3DPP-E0#T2](#) [RJK60S5DPK-M0#T0](#) [APT5010JVFR](#) [APT12031JFLL](#) [APT12040JVR](#) [DMN3404LQ-7](#)  
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