BLF6G15L-500H; BLF6G15LS-500H

Power LDMOS transistor

Rev. 3 — 12 July 2013 Product data sheet

1. Product profile

1.1 General description

A 500 W LDMOS RF power transistor for transmitter applications and industrial applications. The transistor is optimized for digital applications and can deliver 65 W average DVB-T at 1.5 GHz. The excellent ruggedness of this device makes it ideal for digital transmitter applications.

Table 1. Test information

RF performance at V_{DS} = 50 V; I_{Dq} = 1.3 A.

Mode of operation	f (MHz)	$P_{L(AV)}$ (W)	G_p (dB)	η_D (%)	IMD3 (dBc)	IMD_{shldr} (dBc)	PAR (dB)
2-tone, class-AB	1452 to 1492	250	15	34	–24	-	-
DVB-T (8k OFDM)	1452 to 1492	65	16	19	-	–32 [1]	9 [2]

[1] Measured [dBc] with delta marker at 4.3 MHz from center frequency.

[2] PAR (of output signal) at 0.01 % probability on CCDF; PAR of input signal = 9.5 dB at 0.01 % probability on CCDF.

1.2 Features and benefits

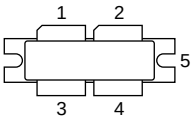
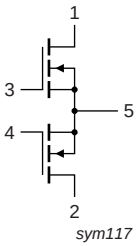
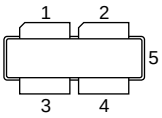
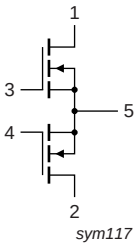
- Easy power control
- Integrated ESD protection
- Excellent ruggedness
- High efficiency
- Excellent thermal stability
- Internally matched for ease of use
- Compliant to Directive 2002/95/EC, regarding Restriction of Hazardous Substances (RoHS)

1.3 Applications

- Digital transmitter applications DVB at 1.5 GHz
- Industrial applications at 1.5 GHz

2. Pinning information

Table 2. Pinning

Pin	Description		Simplified outline	Graphic symbol
BLF6G15L-500H (SOT539A)				
1	drain1			
2	drain2			
3	gate1			
4	gate2			
5	source	[1]		
BLF6G15LS-500H (SOT539B)				
1	drain1			
2	drain2			
3	gate1			
4	gate2			
5	source	[1]		

[1] Connected to flange.

3. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
BLF6G15L-500H	-	flanged balanced LDMOST ceramic package; 2 mounting holes; 4 leads	SOT539A
BLF6G15LS-500H	-	earless flanged balanced LDMOST ceramic package; 4 leads	SOT539B

4. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DS}	drain-source voltage		-	100	V
V_{GS}	gate-source voltage		–0.5	+13	V
I_D	drain current		-	45	A
T_{stg}	storage temperature		–65	+150	°C
T_j	junction temperature		-	200	°C

5. Thermal characteristics

Table 5. Thermal characteristics

Symbol	Parameter	Conditions	Typ	Unit
$R_{th(j\text{-}case)}$	thermal resistance from junction to case	T_{case} = 85 °C; P_L = 65 W	0.18	K/W

6. Characteristics

Table 6. DC characteristics

T_j = 25 °C; per section unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{(BR)DSS}$	drain-source breakdown voltage	V_{GS} = 0 V; I_D = 2.7 mA	100	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	V_{DS} = 10 V; I_D = 270 mA	1.4	1.8	2.4	V
I_{DSS}	drain leakage current	V_{GS} = 0 V; V_{DS} = 50 V	-	-	2.8	μA
I_{DSX}	drain cut-off current	V_{GS} = $V_{GS(th)}$ + 3.75 V; V_{DS} = 10 V	38	42	-	A
I_{GSS}	gate leakage current	V_{GS} = 11 V; V_{DS} = 0 V	-	-	280	nA
g_{fs}	forward transconductance	V_{DS} = 10 V; I_D = 270 mA	1.33	2.3	-	S
$R_{DS(on)}$	drain-source on-state resistance	V_{GS} = $V_{GS(th)}$ + 3.75 V; I_D = 9.5 A	-	100	193	mΩ

Table 7. RF characteristics

RF characteristics in NXP class-AB production circuit, in frequency range 1452 MHz to 1492 MHz; T_{case} = 25 °C.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
DVB-T (8k OFDM), class-AB						
V_{DS}	drain-source voltage		-	50	-	V
I_{Dq}	quiescent drain current		-	1.3	-	A
$P_{L(AV)}$	average output power		-	65	-	W
G_p	power gain		14.5	16	-	dB
η_D	drain efficiency		16	19	-	%
IMD_{shldr}	intermodulation distortion shoulder	[1]	-	–32	–30	dBc
PAR	peak-to-average ratio	[2]	8.5	9	-	dB

[1] Measured [dBc] with delta marker at 4.3 MHz from center frequency.

[2] PAR (of output signal) at 0.01 % probability on CCDF; PAR of input signal = 9.5 dB at 0.01 % probability on CCDF.

6.1 Ruggedness in class-AB operation

The BLF6G15L-500H and BLF6G15LS-500H are capable of withstanding a load mismatch corresponding to VSWR = 10 : 1 through all phases under the following conditions: V_{DS} = 50 V; I_{Dq} = 1.3 A at rated power.

7. Application information

7.1 Impedance information

Table 8. Typical impedance

Typical values per section unless otherwise specified.

f	Z_S	Z_L
MHz	Ω	Ω
1452	1.226 – j2.663	2.137 – j2.750
1472	1.375 – j2.757	1.869 – j2.378
1492	1.15 – j2.735	1.817 – j2.684

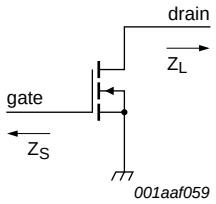
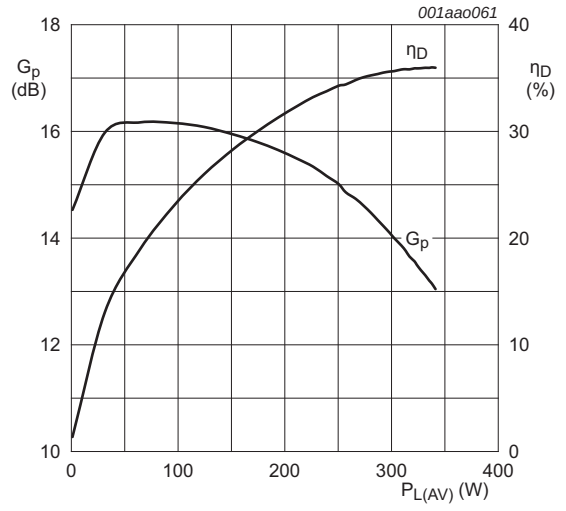


Fig 1. Definition of transistor impedance

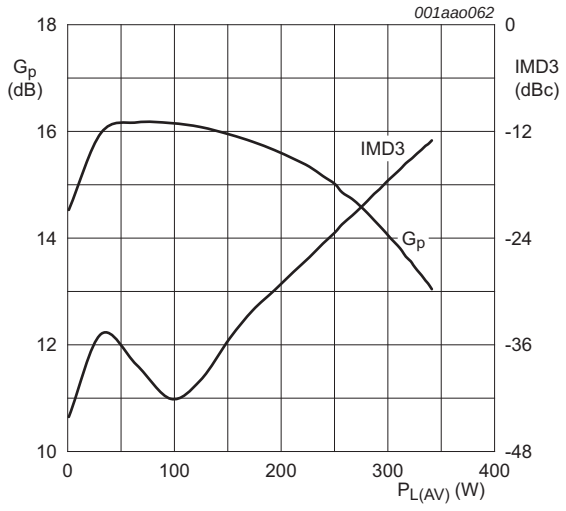
7.2 Graphs

7.2.1 2-Tone



V_{DS} = 50 V; I_{Dq} = 1.3 A; f = 1490 MHz.

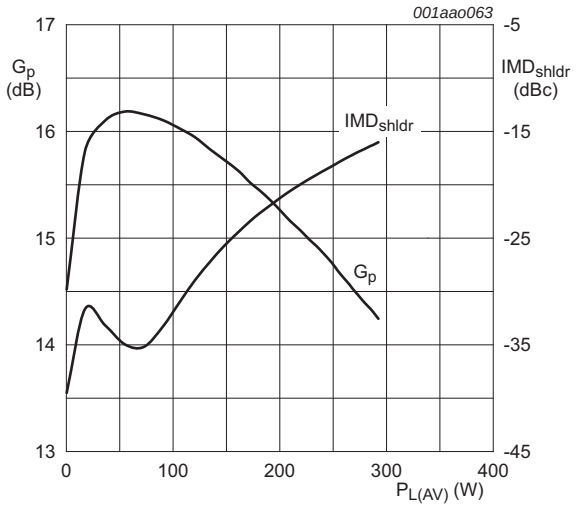
Fig 2. 2-Tone power gain and drain efficiency as function of average load power; typical values



V_{DS} = 50 V; I_{Dq} = 1.3 A; f = 1490 MHz.

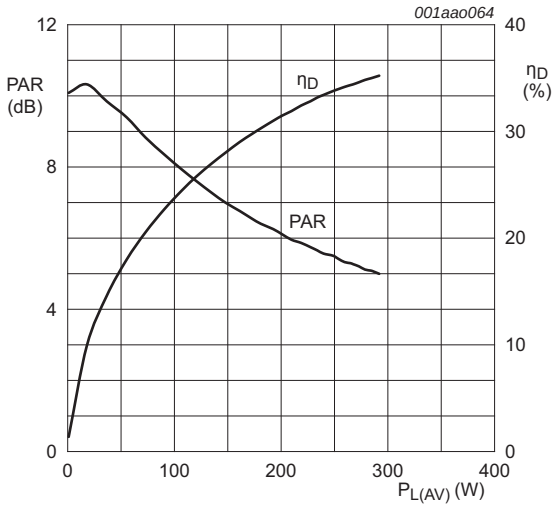
Fig 3. 2-Tone power gain and third order intermodulation distortion as function of average load power; typical values

7.2.2 DVB-T



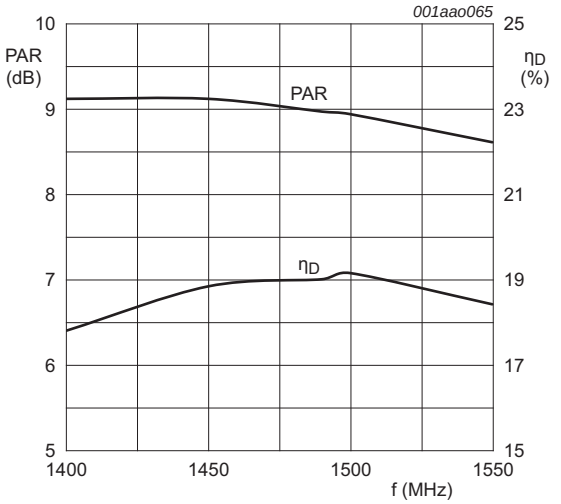
V_{DS} = 50 V; I_{Dq} = 1.3 A; f = 1490 MHz.

Fig 4. DVB-T power gain and intermodulation distortion shoulder as function of average load power; typical values



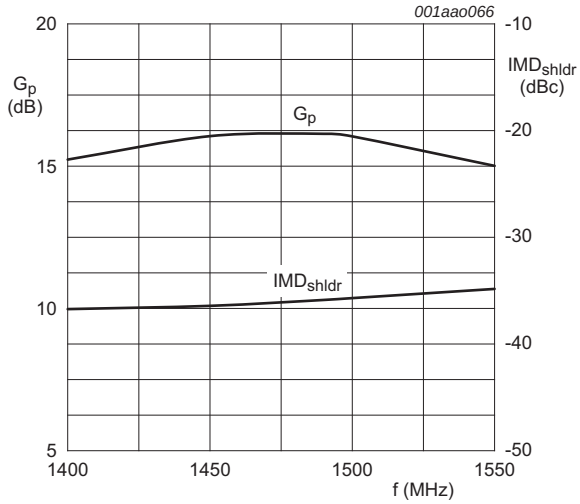
V_{DS} = 50 V; I_{Dq} = 1.3 A; f = 1490 MHz.

Fig 5. DVB-T peak-to-average ratio and drain efficiency as function of average load power; typical values



V_{DS} = 50 V; I_{Dq} = 1.3 A; $P_{L(AV)}$ = 65 W.

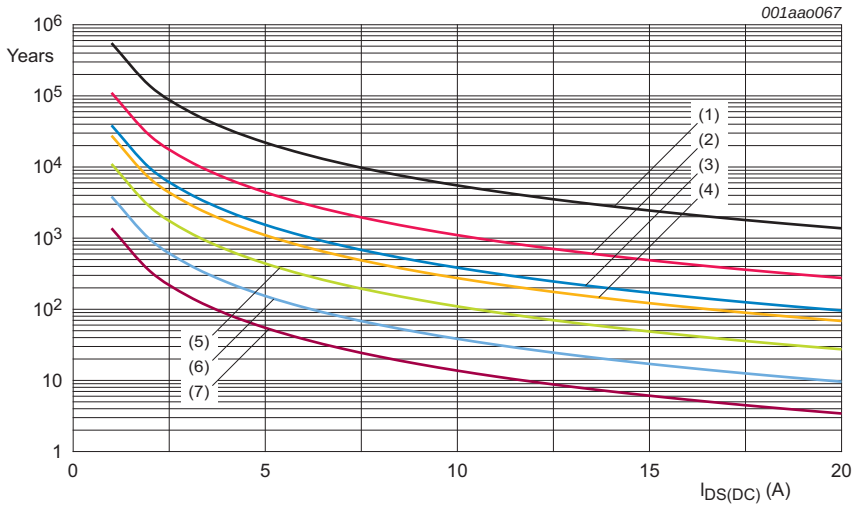
Fig 6. DVB-T peak-to-average ratio and drain efficiency as function of frequency; typical values



V_{DS} = 50 V; I_{Dq} = 1.3 A; $P_{L(AV)}$ = 65 W.

Fig 7. DVB-T power gain and intermodulation distortion shoulder as a function of frequency; typical values

7.2.3 Reliability



TTF (0.1 % failure fraction).

The reliability at pulsed conditions can be calculated as follows: TTF (0.1 %) × 1 / δ.

(1) T_j = 100 °C

(2) T_j = 120 °C

(3) T_j = 140 °C

(4) T_j = 146 °C

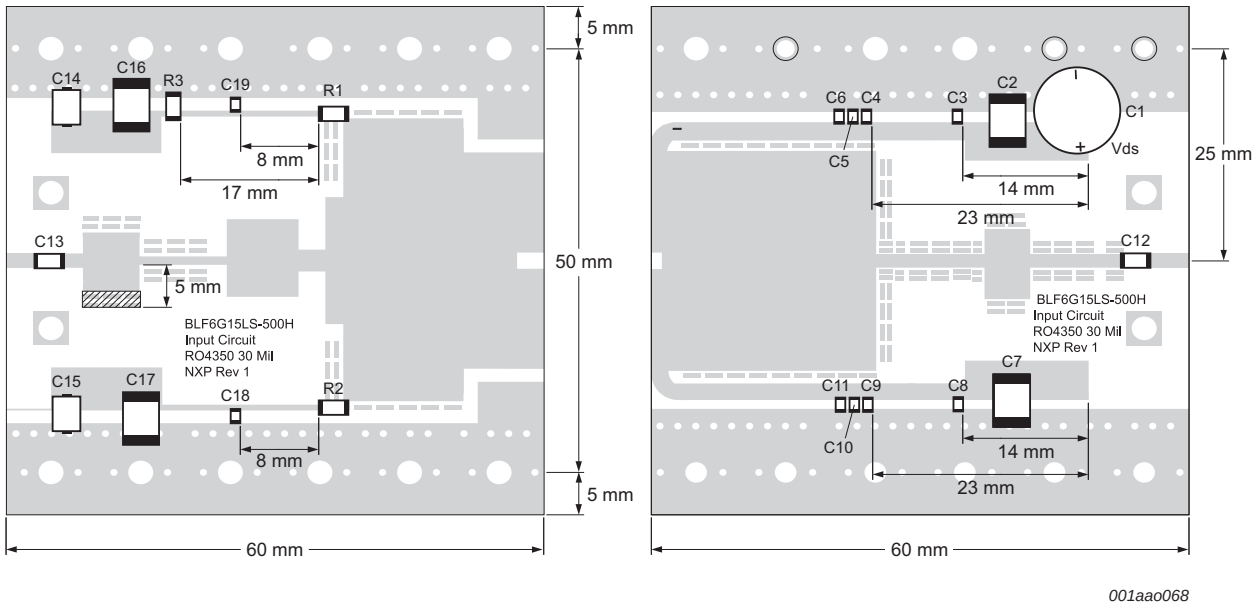
(5) T_j = 160 °C

(6) T_j = 180 °C

(7) T_j = 200 °C

Fig 8. BLF6G15LS-500H electromigration ($I_{DS(DC)}$, total device)

7.3 Test circuit



Printed-Circuit Board (PCB): Rogers 4350; ε_r = 3.66; thickness = 0.30 mm; thickness copper plating = 35 μm.

See Table 9 for list of components.

Fig 9. Component layout for class-AB common source amplifier

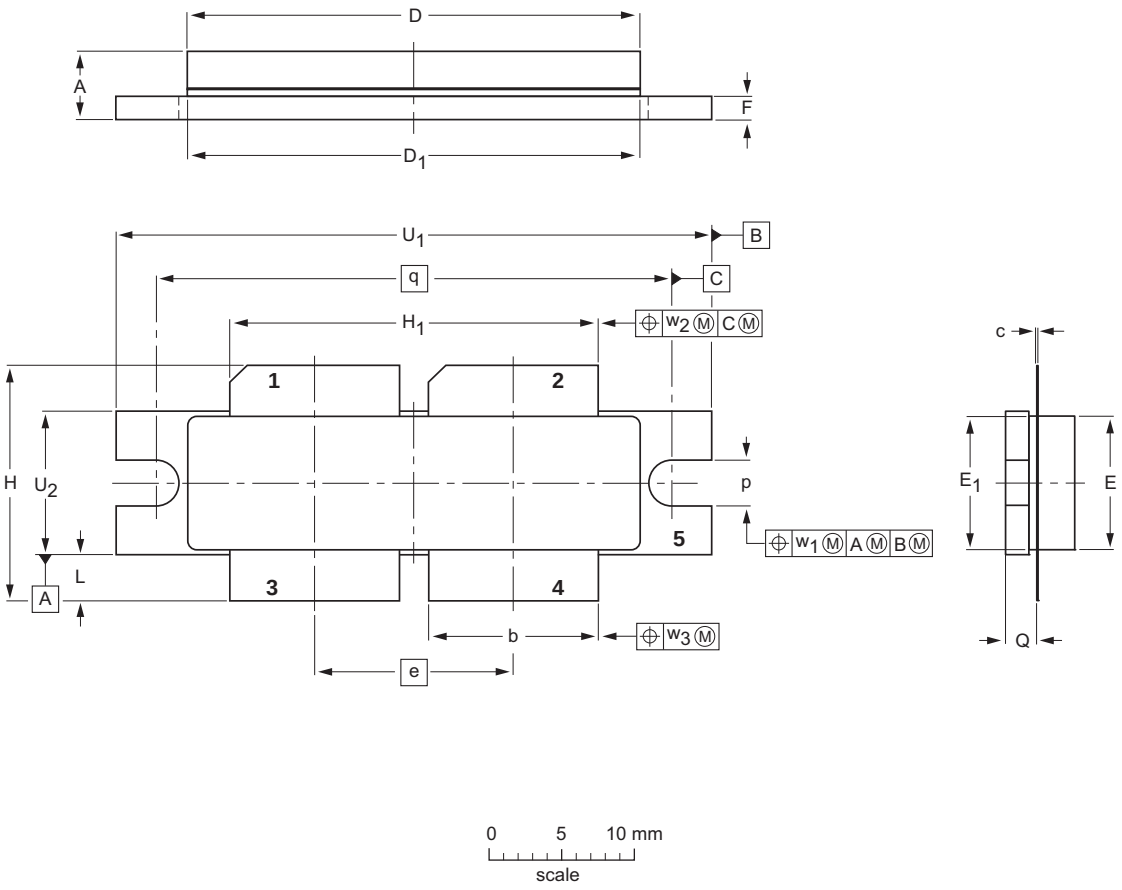
Table 9. List of components

See Figure 9 for component layout.

Component	Description	Value	Remarks
C1	electrolytic capacitor	470 μF, 63 V	Elco
C2, C7, C16, C17	multilayer ceramic chip capacitor	10 μF	TDK
C3, C8	multilayer ceramic chip capacitor	6.2 pF	ATC800B
C4, C5, C9, C10	multilayer ceramic chip capacitor	1.0 μF	1206 10 %
C6, C11	multilayer ceramic chip capacitor	10 nF	1205 10 %
C12, C13	multilayer ceramic chip capacitor	22 pF	ATC800B
C18, C19	multilayer ceramic chip capacitor	22 pF	ATC800B
C15	electrolytic capacitor	470 μF; 63 V	
R1, R2	SMD resistor	5R1 Ω	0805
R3	SMD resistor	470 Ω (not fitted)	1206

8. Package outline

Flanged balanced ceramic package; 2 mounting holes; 4 leads **SOT539A**



DIMENSIONS (millimetre dimensions are derived from the original inch dimensions)

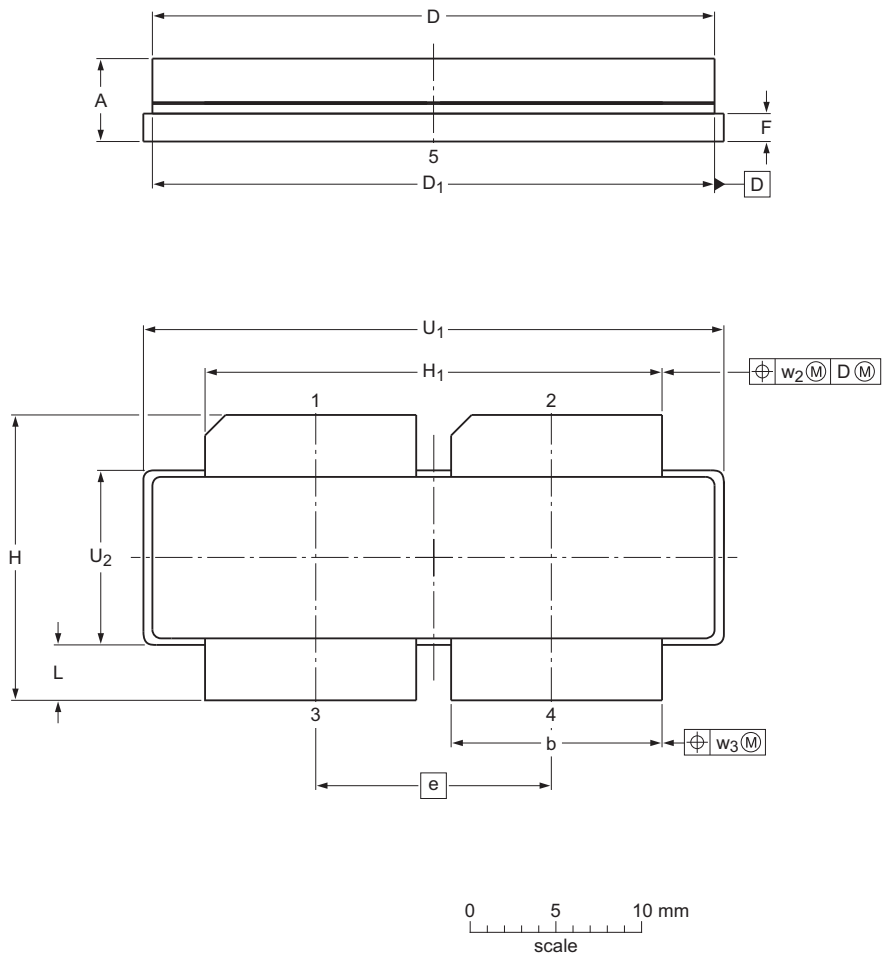
UNIT	A	b	c	D	D_1	e	E	E_1	F	H	H_1	L	p	Q	q	U_1	U_2	w_1	w_2	w_3
mm	4.7 4.2	11.81 11.56	0.18 0.10	31.55 30.94	31.52 30.96	13.72	9.50 9.30	9.53 9.27	1.75 1.50	17.12 16.10	25.53 25.27	3.48 2.97	3.30 3.05	2.26 2.01	35.56	41.28 41.02	10.29 10.03	0.25	0.51	0.25
inches	0.185 0.165	0.465 0.455	0.007 0.004	1.242 1.218	1.241 1.219	0.540	0.374 0.366	0.375 0.365	0.069 0.059	0.674 0.634	1.005 0.995	0.137 0.117	0.130 0.120	0.089 0.079	1.400	1.625 1.615	0.405 0.395	0.010	0.020	0.010

Note
1. millimeter dimensions are derived from the original inch dimensions.
2. recommended screw pitch dimension of 1.52 inch (38.6 mm) based on M3 screw.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT539A						~~10-02-02~~ 12-05-02

Fig 10. Package outline SOT539A

Earless flanged balanced ceramic package; 4 leads **SOT539B**



Dimensions

Unit[1]		A	b	c	D	D_1	E	E_1	e	F	H	H_1	L	Q	U_1	U_2	w_2	w_3
mm	max	4.7	11.81	0.18	31.55	31.52	9.5	9.53	13.72	1.75	17.12	25.53	3.48	2.26	32.39	10.29	0.25	0.25
	nom																	
	min	4.2	11.56	0.10	30.94	30.96	9.3	9.27		1.50	16.10	25.27	2.97	2.01	32.13	10.03		
inches	max	0.185	0.465	0.007	1.242	1.241	0.374	0.375	0.54	0.069	0.674	1.005	0.137	0.089	1.275	0.405	0.01	0.01
	nom																	
	min	0.165	0.455	0.004	1.218	1.219	0.366	0.365		0.059	0.634	0.995	0.117	0.079	1.265	0.395		

Note
1. millimeter dimensions are derived from the original inch dimensions.

sot539b_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT539B						~~12-05-02~~ 13-05-24

Fig 11. Package outline SOT539B

9. Handling information

CAUTION

This device is sensitive to ElectroStatic Discharge (ESD). Observe precautions for handling electrostatic sensitive devices.

Such precautions are described in the *ANSI/ESD S20.20*, *IEC/ST 61340-5*, *JESD625-A* or equivalent standards.

10. Abbreviations

Table 10. Abbreviations

Acronym	Description
CCDF	Complementary Cumulative Distribution Function
DVB-T	Digital Video Broadcast - Terrestrial
DVB	Digital Video Broadcast
ESD	ElectroStatic Discharge
LDMOS	Laterally Diffused Metal-Oxide Semiconductor
LDMOST	Laterally Diffused Metal-Oxide Semiconductor Transistor
OFDM	Orthogonal Frequency Division Multiplexing
PAR	Peak-to-Average power Ratio
RF	Radio Frequency
SMD	Surface Mounted Device
TTF	Time To Failure
VSWR	Voltage Standing-Wave Ratio

11. Revision history

Table 11. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
BLF6G15L-500H_6G15LS-500H v.3	20130712	Product data sheet	-	BLF6G15L-500H_6G15LS-500H v.2
Modifications:	• The package outline Figure 11 is updated. • Translation disclaimer added to the legal text.			
BLF6G15L-500H_6G15LS-500H v.2	20110916	Product data sheet	-	BLF6G15L-500H_6G15LS-500H v.1
Modifications:	• The status of this data sheet has been changed to Product data sheet			
BLF6G15L-500H_6G15LS-500H v.1	20110511	Objective data sheet	-	-

12. Legal information

12.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
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Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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14. Contents

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