

# AC/DC Drivers

# PWM type DC/DC converter IC Included 650V MOSFET

**BM2PXX3 Series** 

#### General

The PWM type DC/DC converter (BM2PXX3) for AC/DC provide an optimum system for all products that include an electrical outlet.

BM2PXX3 supports both isolated and non-isolated devices, enabling simpler design of various types of low-power electrical converters.

BM2PXX3 built in a HV starter circuit that tolerates 650V, it contributes to low-power consumption.

With current detection resistors as external devices, a higher degree of design freedom is achieved. Since current mode control is utilized, current is restricted in each cycle and excellent performance is demonstrated in bandwidth and transient response.

The switching frequency is 65 kHz. At light load, the switching frequency is reduced and high efficiency is achieved.

A frequency hopping function is also on chip, which contributes to low EMI.

We can design easily, because  $\mathsf{BM2PXX3}$  includes the switching MOSFET.

#### Basic specifications

- ■Operating Power Supply Voltage Range: VCC 8.9V to 26.0V DRAIN : ~650V
- Operating Current: Normal Mode

	BM2P013: 0.950mA (Typ.)
	BM2P033: 0.775mA (Typ.)
	BM2P053: 0.600mA (Typ.)
	BM2P093: 0.500mA (Typ.)
	Burst Mode: 0.400mA (Typ
■Oscillation Frequency:	65kHz (Typ.)
Operating Temperature	

Operating Temperature:
 MOSFET ON Resistance:

BM2P013: 1.4Ω (Typ.)

#### Application circuit

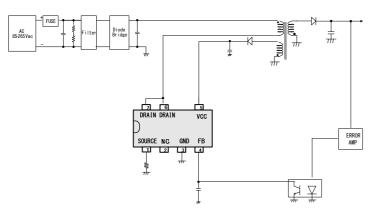


Figure 1. Application circuit

# Features

- PWM frequency : 65kHz
- PWM current mode method
- Burst operation when load is light
- Frequency reduction function
- Built-in 650V start circuit
- Built-in 650V switching MOSFET
- VCC pin under voltage protection
- VCC pin overvoltage protection
- SOURCE pin Open protection
- SOURCE pin Short protection
- SOURCE pin Leading-Edge-Blanking function
- Per-cycle over current protection circuit
- Soft start
- Secondary Over current protection circuit

#### Package

DIP7

9.20mm×6.35mm×4.30mm pitch 2.54mm (Typ.) (Typ.) (Max.) (Typ.)



#### Applications

AC adapters and household appliances (vacuum cleaners, humidifiers, air cleaners, air conditioners, IH cooking heaters, rice cookers, etc.)

#### •Line up

Product	MOSFET ON Resistor
BM2P013	1.4Ω
BM2P033	2.4Ω
BM2P053	4.0Ω
BM2P093	8.5Ω

OProduct structure : Silicon monolithic integrated circuit OThis product is not designed protection against radioactive rays

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BM2P033: 2.4Ω (Typ.) BM2P053: 4.0Ω (Typ.) BM2P093: 8.5Ω (Typ.)

# •Absolute Maximum Ratings(Ta=25°C)

Parameter	Symbol	Rating	Unit	Conditions
Maximum applied voltage 1	Vmax1	-0.3~30	V	VCC
Maximum applied voltage 2	Vmax2	-0.3~6.5	V	SOURCE, FB
Maximum applied voltage 3	V max3	650	V	DRAIN
Drain current pulse	I <sub>DP</sub>	10.40	А	P <sub>w</sub> =10us, Duty cycle=1% (BM2P013)
Drain current pulse	I <sub>DP</sub>	5.20	А	P <sub>w</sub> =10us, Duty cycle=1% (BM2P033)
Drain current pulse	I <sub>DP</sub>	2.60	А	P <sub>w</sub> =10us, Duty cycle=1% (BM2P053)
Drain current pulse	I <sub>DP</sub>	1.30	А	P <sub>w</sub> =10us, Duty cycle=1% (BM2P093)
Allowable dissipation	Pd	2000	mW	
Operating temperature range	Topr	-40 ~ +105	°C	
MAX junction temperature	T <sub>JMAX</sub>	150	°C	
Storage temperature range	Tstr	-55 ~ +150	°C	

(Note1) DIP7 : When mounted (on 74.2 mm × 74.2 mm, 1.6 mm thick, glass epoxy on double-layer substrate). Reduce to 16 mW/°C when Ta =  $25^{\circ}$ C or above.

# •Operating Conditions(Ta=25°C)

Parameter	Symbol	Rating	Unit	Conditions
Power supply voltage range 1	Vcc	8.9~26.0	V	VCC pin voltage
Power supply voltage range 2	$V_{\text{drain}}$	~650	V	DRAIN pin voltage

# •Electrical Characteristics of MOSFET part (Unless otherwise noted, Ta = 25°C, VCC = 15 V)

Parameter Symb		Specifications			Unit	Conditions	
i arameter	Symbol	Min	Тур	Max	Onit	Conditions	
[MOSFET Block]	[MOSFET Block]						
Between drain and source voltage	$V_{(\text{BR})\text{DDS}}$	650	-	-	V	$I_{D}$ =1mA / $V_{GS}$ =0V	
Drain leak current	I <sub>DSS</sub>	-	-	100	uA	V <sub>DS</sub> =650V / V <sub>GS</sub> =0V	
On resistance	$R_{DS(ON)}$	-	1.4	2.0	Ω	I <sub>D</sub> =0.25A / V <sub>GS</sub> =10V (BM2P013)	
On resistance	$R_{\text{DS(ON)}}$	-	2.4	3.6	Ω	I <sub>D</sub> =0.25A / V <sub>GS</sub> =10V (BM2P033)	
On resistance	R <sub>DS(ON)</sub>	-	4.0	5.5	Ω	I <sub>D</sub> =0.25A / V <sub>GS</sub> =10V (BM2P053)	
On resistance	R <sub>DS(ON)</sub>	-	8.5	12.0	Ω	I <sub>D</sub> =0.25A / V <sub>GS</sub> =10V (BM2P093)	

# •Electrical Characteristics of Control IC part (Unless otherwise noted, Ta = 25°C, VCC = 15 V)

Participant         Symbol         Min         Typ         Max         Util         Conductors           [Circuit current (ON) 1         Um         700         950         1200         μA         [Mayee operation)           Circuit current (ON) 1         Um         550         775         1050         μA         [Mayee operation]           Circuit current (ON) 1         Um         4m         410         600         790         μA         [Mayee operation]           Circuit current (ON) 1         Um         4m         410         600         790         μA         F8=0.0V(at burst operation)           Circuit current (ON) 2         Lsu         -         400         500         μA         F8=0.0V(at burst operation)           (VC UVLO votage 1         Vmox         7.50         8.20         8.90         V         VCC Circle ses           VCC UVLO votage 1         Vmox         -         5.30         -         V         Voca           VCC UVLO votage 1         Vmox         -         112.00         13.50         14.50         V         VCC rises           VCC UVC Votage 1         Vmox         -         Voca         -         Veca         Control IC         Control IC	•Electrical Characteristics of Cor			Specifications	, 1a - 25 C		
	Parameter	Symbol			Max	Unit	Conditions
$ \begin{array}{c} \text{Clicul durinef (UN) 1} & \left  \begin{array}{c} v_{\text{ov}} & 700 & 900 & 1200 & \mu^{\text{A}} \\ \text{Circuit durinef (ON) 1} & \left  \begin{array}{c} v_{\text{ov}} & 550 & 775 & 1050 & \mu^{\text{A}} \\ \text{MP2P03, FB=2.0V} \\ \text{(at pulse operation)} \\ \text{Circuit current (ON) 1} & \left  \begin{array}{c} v_{\text{ov}} & 410 & 600 & 790 & \mu^{\text{A}} \\ \text{MP2P03, FB=2.0V} \\ \text{(at pulse operation)} \\ \text{Circuit current (ON) 1} & \left  \begin{array}{c} v_{\text{ov}} & 350 & 500 & 650 \\ \text{MPC} & \mu^{\text{A}} \\ \text{MP2P03, FB=2.0V} \\ \text{(at pulse operation)} \\ \text{(at pulse operation)} \\ \text{Circuit current (ON) 2} & \left  \begin{array}{c} v_{\text{ov}} & 750 & 13.50 \\ \text{VCC UVLO voltage 1} \\ \text{VCC UVLO voltage 1} \\ \text{Vocous} & 7.50 & 13.50 \\ \text{VCC UVLO voltage 1} \\ \text{Vocous} & 7.50 & 13.50 \\ \text{VCC UVLO voltage 1} \\ \text{Vocous} & 7.50 & 13.50 \\ \text{VCC UVLO voltage 1} \\ \text{Vocous} & 7.50 & 13.20 \\ \text{VCC COVP oblige 2} \\ \text{Vocous} & 7.50 & 13.20 \\ \text{VCC COVP oblige 2} \\ \text{Vocous} & 7.70 & 10.70 \\ \text{VCC CRecharge star voltage 1} \\ \text{Voces} & 7.70 & 10.70 \\ \text{VCC Recharge star voltage 1} \\ \text{Voces} & 7.70 & 10.70 \\ \text{VCC Recharge star voltage 1} \\ \text{Voces} & 7.70 & 10.0 \\ \text{VCC Recharge star voltage 1} \\ \text{Voces} & 7.70 & 10.0 \\ \text{VCC Recharge star voltage 1} \\ \text{Voces} & 7.70 & 10.0 \\ \text{VCC Recharge star voltage 1} \\ \text{Voces} & 7.70 & 10.0 \\ \text{VCC Recharge star voltage 1} \\ \text{Voces} & 7.70 & 10.0 \\ \text{Thermal shut down temperature } \\ \text{Tue} & 118 \\ 145 & - \end{tabular} \\ \text{Thermal shut down temperature } \\ \text{Tue} & 118 \\ 145 & - \end{tabular} \\ \text{Conclusion frequency 1} \\ \text{Feasure Y opoling width 1} \\ \text{Freat} & - & 4.0 \\ - & \text{KHz} \\ \text{FB -2.0V \\ \text{Control ICC } \\ \text{Freadency Proping Audith 1} \\ \text{Freat} & - & 4.0 \\ - & \text{KHz} \\ \text{FB -2.0V \\ \text{Control ICC } \\ \text{Freadency Y opoling width 1} \\ \text{Freat} & - & 4.0 \\ - & \text{KHz} \\ \text{FB -2.0V \\ \text{Control ICC } \\ FFe and the fact on fore the fact on the fa$	[Circuit current]			· · · · ·			
$ \begin{array}{c cluster} (CM) 1 &  _{Sur} & Sol & 175 & 1050 & \mu^A & [at pulse operation] \\ \hline Circuit current (ON) 1 &  _{Sur} & 410 & 600 & 790 & \mu^A & [M2P053, FB=20V & [M2P053, FB=$	Circuit current (ON) 1	I <sub>ON1</sub>	700	950	1200	μA	( at pulse operation)
$ \begin{array}{c} \mbox{Circuit Current (ON) 1} & \begin{tabular}{ c c c c c c c c c c c c c c c c c c c$	Circuit current (ON) 1	I <sub>ON1</sub>	550	775	1050	μA	(at pulse operation)
$ \begin{array}{c cccc} \mbox{Current} (ON) 1 & L_{rec} & 300 & 500 & 000 & \mu^A & [at pulse operation] \\ \mbox{Circuit current} (ON) 2 & L_{rec} & - & 400 & 500 & \mu^A & FB=0.0V(at burst operation) \\ \mbox{Circuit current} (ON) 2 & L_{rec} & - & 400 & 500 & V & VCC raises \\ \mbox{VCC UVLO voltage 1} & V_{vcAcc} & 7.50 & 8.20 & 8.90 & V & VCC raises \\ \mbox{VCC UVLO voltage 2} & V_{vcAcc} & 7.50 & 8.20 & 8.90 & V & VCC raises \\ \mbox{VCC UVC UVC optimetry} & V_{vcAcc} & - & 5.30 & - & V & VCC raises \\ \mbox{VCC UVC OVP voltage 1} & V_{vcAcc} & - & 5.30 & - & V & VCC raises \\ \mbox{VCC UVC OVP voltage 1} & V_{vcAcc} & - & 7.5 & 2.90 & V & VCC raises \\ \mbox{VCC Recharge start voltage} & V_{vcac} & 7.70 & 8.70 & 9.70 & V \\ \mbox{VCC Recharge start voltage} & V_{vcac} & 12.00 & 13.00 & 14.00 & V \\ \mbox{UCC Recharge stop voltage} & V_{vcac} & 118 & 145 & - & eC \\ \mbox{Cocclustont temperature} & T_{ycac} & 50 & 100 & 150 & us \\ \mbox{Temmal shut down temperature} & T_{ycac} & 50 & 100 & 150 & us \\ \mbox{Temmal shut down temperature} & T_{ycac} & - & 4.0 & - & KHz & FB=2.0V \\ \mbox{Cocluston frequency 2} & F_{wcac} & - & 4.0 & - & KHz & FB=2.0V \\ \mbox{Cocluston frequency 2} & F_{wcac} & 0.60 & 1.00 & 1.40 & ms \\ \mbox{Cost start time 2} & T_{ssc} & 1.20 & 2.00 & 2.80 & ms \\ \mbox{Soft start time 4} & T_{ssc} & 1.20 & 2.00 & 2.80 & ms \\ \mbox{Soft start time 4} & T_{ssc} & 0.300 & 0.400 & 0.500 & V & FB falls \\ \mbox{Maximum duty} & D_{mat} & 68.0 & 75.0 & 82.0 & % \\ \mbox{FB oLP voltage 1a} & V_{vcacs} & - & 0.040 & 0.500 & V & FB falls \\ \mbox{Maximum duty} & D_{mat} & 2.60 & 2.80 & 3.00 & V & Overload is detected (FB rise) \\ \mbox{FB oLP voltage 15} & V_{vcacs} & - & 0.020 & 0.400 & 0.420 & V \\ \mbox{Corrent detection voltage SS1} & V_{vcacs} & - & 0.100 & - & V & 0 \\ \mbox{Corrent detection voltage SS1} & V_{vcacs} & - & 0.020 & - & V & 0 \\ \mbox{Corrent detection voltage SS1} & V_{vcacs} & - & 0.020 & - & V & 0 \\ \mbox{Corrent detection voltage SS1} & V_{vcacs} & - & 0.020 & 0.500 & V & 0 \\ Corrent detection voltage $	Circuit current (ON) 1	I <sub>on1</sub>	410	600	790	μA	(at pulse operation)
IVCC protection function]         VCC UVLO voltage 1         V,vont         12.50         13.50         14.50         V         VCC reses           VCC UVLO voltage 1         V,vont         -         5.30         -         V         VVcC falls           VCC OVLO hysteresis         V,vont         28.0         Z7.5         29.0         V         VVcC relates           VCC OVP obligge         V,vont         28.0         Z7.5         29.0         V         VVcC relates           VCC OVP obligge         V,vont         28.0         Z7.5         29.0         V         VVcC relates           CC CRCharge start voltage         V,vont         28.0         13.00         14.00         V           VCC Recharge start voltage         V,vont         13.00         14.00         V         VCC recharge start voltage         V,vont           VCC Recharge start voltage         V,vont         12.00         13.00         14.00         V         VCC recharge start voltage         Vont         Test         13.00         14.00         V         VCC recharge start voltage         Vont         Test         12.0         20.0         25.0         0.70         frst         FE=2.0V         PS.00         20.0         28.0         7.5         12.5	Circuit current (ON) 1	I <sub>on1</sub>	350	500	650	μA	
$ \begin{array}{cccccccccccccccccccccccccccccccccccc$	Circuit current (ON) 2	I <sub>ON2</sub>	-	400	500	μA	FB=0.0V(at burst operation)
$ \begin{array}{cccccccccccccccccccccccccccccccccccc$	[VCC protection function]						
VCC UVLO hysteresis         V <sub>unco</sub> -         5.30         -         V         Vunco:							
$\begin{array}{c c c c c c c c c c c c c c c c c c c $			7.50		8.90	-	
Latch released VCC voltage $V_{vorst}$ - $V_{vorst}^{-0.5}$ -         V           VCC Recharge start voltage $V_{caret}$ 7.70         8.70         9.70         V           VCC Recharge start voltage $V_{caret}$ 12.00         13.00         14.00         V           Latch mask time $T_{urcet}$ 50         100         150         us           Inemal shut down temperature $T_{uot}$ 50         100         150         us           Oscillation frequency 1 $F_{ment}$ 60         65         70         KHz         FB=2.0V           Oscillation frequency 2 $F_{ment}$ 60         65         70         KHz         FB=2.0V           Oscillation frequency 2 $F_{ment}$ 7         125         175         Hz         FB=2.0V           Soft start time 1 $T_{max}$ 0.30         0.50         0.70         ms           Soft start time 3 $T_{sps}$ 1.20         2.00         2.80         ms           Maximum duty         Dmax         68.0         75.0         82.0         %         FB           FB burst voltage         V <sub>eatt</sub>		V <sub>UVLO3</sub>	-				
$ \begin{array}{c c c c c c c c c c c c c c c c c c c $			26.0		29.0		VCC rises
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Latch mask time         T <sub>utom</sub> 50         100         150         us           Dermal shut down temperature         T <sub>so</sub> 118         145         -         °C         Control IC           [PWM type DCDC driver block]         Oscillation frequency 1         Fav.         60         65         70         KHz         FB=2.00V           Oscillation frequency         Frequency hopping width 1         Finn.         -         4.0         -         KHz         FB=2.0V           Oscillation frequency         Fon         75         125         175         Hz         =         -         KHz         FB=0.40V           Soft start time 1         T <sub>SS0</sub> 0.30         0.50         0.70         ms         -         Soft start time 3         T <sub>SS0</sub> 1.20         2.00         2.80         ms           Soft start time 3         T <sub>SS0</sub> 0.30         0.50         11.20         ms         -							
Latch mask time         T <sub>utom</sub> 50         100         150         us           Dermal shut down temperature         T <sub>so</sub> 118         145         -         °C         Control IC           [PWM type DCDC driver block]         Oscillation frequency 1         Fav.         60         65         70         KHz         FB=2.00V           Oscillation frequency         Frequency hopping width 1         Finn.         -         4.0         -         KHz         FB=2.0V           Oscillation frequency         Fon         75         125         175         Hz         =         -         KHz         FB=0.40V           Soft start time 1         T <sub>SS0</sub> 0.30         0.50         0.70         ms         -         Soft start time 3         T <sub>SS0</sub> 1.20         2.00         2.80         ms           Soft start time 3         T <sub>SS0</sub> 0.30         0.50         11.20         ms         -		V <sub>CHG2</sub>				-	
IPWM type DCDC driver block]         Fewr.         60         65         70         KHz         FB=2.00V           Oscillation frequency 1 $F_{ewr.}$ 20         25         30         KHz         FB=2.0V           Oscillation frequency 2 $F_{ewr.}$ 20         25         30         KHz         FB=2.0V           Prequency hopping width 1 $F_{ewr.}$ -         4.0         -         KHz         FB=2.0V           Soft start time 1 $T_{sst.}$ 0.30         0.50         0.70         ms         -           Soft start time 3 $T_{sst.}$ 0.60         1.00         1.40         ms         -           Soft start time 3 $T_{sst.}$ 0.60         75.0         82.0         %         -           PB in pull-up resistance $R_{B_1}$ 2.3         30         37         KΩ           FB burst voltage $V_{est.}$ 0.300         0.400         0.500         V         FB falls           FB burst voltage 1 $V_{rat.rell         1.100         1.250         1.400         V           FB DLP Voltage 1a         V_{rat.rell         2.60         2.80         3.00         V         <$		TLATCH					
Oscillation         Fequency 1         Fgm1         60         65         70         KHz         FB=2.00V           Oscillation         Frequency popping with 1         Fgm2         20         25         30         KHz         FB=0.40V           Frequency hopping with 1         Fgm1         75         125         175         Hz         FB=2.0V           Soft start time 1         Tss         0.30         0.50         0.70         ms         Soft start time 2         Tss           Soft start time 3         Tss         1.20         2.00         2.80         ms         Soft start time 4         Tss           Soft start time 4         Tsss         4.80         8.00         11.20         ms         Maximum duty         Dmax         68.0         75.0         82.0         %         Maximum duty         Dmax         KG         AC         A         D         Overload is det	•	T <sub>SD</sub>	118	145	-	°C	Control IC
Frequency hopping width 1       F $_{Ext}$ -       4.0       -       KHz       FB=2.0V         Hopping fluctuation frequency $F_{Cxt}$ 75       125       175       Hz       Soft start time 1       T $_{Sst}$ 0.30       0.50       0.70       ms         Soft start time 2       T $_{Sst}$ 0.60       1.00       1.40       ms       Soft start time 3       T $_{Sst}$ 0.60       11.20       ms       Soft start time 4       T $_{Sst}$ 4.80       8.00       11.20       ms       Soft start time 4       T $_{Sst}$ 4.80       8.00       11.20       ms       Soft start time 4       T $_{Sst}$ 4.80       8.00       11.20       ms       Soft start time 4       T $_{Sst}$ 4.80       8.00       11.20       ms       Soft start time 4       T $_{Sst}$ 4.00       8.00       11.20       ms       Soft start time 4       Soft start time 4       Soft start time 4       5.00       1.400       V/V       FB stalls       Soft start time 4       Soft start time 4       1.00       1.250       1.400       V       FB falls       FB stalls       FB stalls       FB stalls       FB stalls       FB start							
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Soft start time 1         Tss1         0.30         0.50         0.70         ms           Soft start time 2         Tss2         0.60         1.00         1.40         ms           Soft start time 3         Tss2         0.60         1.00         1.40         ms           Soft start time 4         Tss1         1.20         2.00         2.80         ms           Maximum duty         Dmax         68.0         75.0         82.0         %           FB pin pull-up resistance         Res         23         30         37         KΩ           AFB / $\Delta$ CS gain         Gain         -         4.00         -         V/V           FB bultge of         starting Frequency reduction mode         Vsr         1.100         1.250         1.400         V           FB OLP voltage 1a         Vrouta         2.60         2.80         3.00         V         Overload is detected (FB rise)           FB OLP Ottage 1b         Vrouta         -         2.60         -         V         Overload is detected (FB rise)           FB OLP Ottage 1b         Vrouta         -         2.60         -         V         Overload is detected (FB rise)           FB OLP OFT timer         Troucz         358			-		-		FB=2.0V
Soft start time 2 $T_{ss2}$ $0.60$ $1.00$ $1.40$ ms           Soft start time 3 $T_{ss2}$ $1.20$ $2.00$ $2.80$ ms           Maximum duty $D_{max}$ $68.0$ $75.0$ $82.0$ $\%$ FB pin pull-up resistance $R_{eg}$ $23$ $30$ $37$ $K\Omega$ $\Delta FB / \Delta CS$ gain $G_{ain}$ $ 4.00$ $ V/V$ FB burst voltage $V_{ssr}$ $0.300$ $0.400$ $0.500$ V         FB falls           FB outge of $V_{ssr}$ $0.300$ $0.400$ $0.500$ V         FB falls           FB outge of $V_{ssr}$ $1.100$ $1.250$ $1.400$ V           FB OLP voltage 1a $V_{count}$ $2.60$ $2.80$ $3.00$ V         Overload is detected (FB drop)           FB OLP Not time $T_{count}$ $2.60$ $2.80$ $3.00$ V         Overload is detected (FB drop)           FB OLP ON time $T_{count}$ $2.60$ $2.81$ $3.00$ $0.420$							
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FB burst voltage         V <sub>BST</sub> 0.300         0.400         0.500         V         FB falls           FB voltage of starting Frequency reduction mode         V <sub>DAT</sub> 1.100         1.250         1.400         V           FB OLP voltage 1a         V <sub>FOLPTA</sub> 2.60         2.80         3.00         V         Overload is detected (FB rise)           FB OLP voltage 1b         V <sub>FOLPTA</sub> 2.60         -         V         Overload is detected (FB drop)           FB OLP Not timer         T <sub>FOLPT</sub> 40         64         88         ms           FB OLP Start up timer         T <sub>FOLPT</sub> 26         32         38         ms           FB OLP OFF timer         T <sub>FOLPT</sub> 26         32         38         ms           Over current detection blockJ         U         V <sub>CS</sub> 0.380         0.400         0.420         V         Ton=0us           Overcurrent detection voltage SS1         V <sub>CS</sub> 0.380         0.400         0.420         V         Ton=0us           Overcurrent detection voltage SS2         V <sub>CS</sub> ,ssi         -         0.150         -         V         Tss1[ms]           Overcurrent detection voltage SS4         V <sub>CS</sub> ,ssi         -         0.200         -			23		57		
FB voltage of starting Frequency reduction mode $V_{BKT}$ 1.1001.2501.400VFB OLP voltage 1a $V_{F0LPLA}$ 2.602.803.00VOverload is detected (FB rise)FB OLP voltage 1b $V_{F0LPLA}$ 2.60-VOverload is detected (FB drop)FB OLP Voltage 1b $V_{F0LPLA}$ 406488msFB OLP ON timer $T_{F0LPL}$ 406488msFB OLP Start up timer $T_{F0LPL}$ 263238msFB OLP OFF timer $T_{F0LPL}$ 358512666ms <b>Over current detection blockj</b> Overcurrent detection voltage $V_{cs}$ 0.3800.4000.420VOvercurrent detection voltage SS1 $V_{cs,S81}$ -0.100-VOvercurrent detection voltage SS2 $V_{cs,S82}$ -0.150-VOvercurrent detection voltage SS3 $V_{cs,S83}$ -0.200-VTss1[ms] ~ Tss1[ms]Overcurrent detection voltage SS4 $V_{cs,S84}$ -0.300-VTss2[ms] ~ Tss4[ms]Leading Edge Blanking Time $T_{LEB}$ -250-nsOver current detection AC Voltage compensation factor $V_{cssHT}$ 0.0200.0500.080VSOURCE pin short protection voltage $V_{cssHT}$ 0.1000.5001.000mAVCC= 0VStart current 1IstrartzIstrartz1.0003.0006.000mAVCC=10V <t< td=""><td></td><td></td><td>-</td><td></td><td>-</td><td></td><td>ER falls</td></t<>			-		-		ER falls
$\begin{array}{c c c c c c c c c c c c c c c c c c c $							
$ \begin{array}{c c c c c c c c c c c c c c c c c c c $		V <sub>DLT</sub>	1.100	1.250	1.400	V	
$ \begin{array}{c c c c c c c c c c c c c c c c c c c $	FB OLP voltage 1a	V <sub>FOLP1A</sub>	2.60		3.00		
$\begin{array}{c c c c c c c c c c c c c c c c c c c $	FB OLP voltage 1b	V <sub>FOLP1B</sub>	-	2.60	-	V	Overload is detected (FB drop)
FB OLP OFF timer         T <sub>FOUP2</sub> 358         512         666         ms           [Over current detection block]           Overcurrent detection voltage $V_{CS}$ 0.380         0.400         0.420         V         Ton=0us           Overcurrent detection voltage SS1 $V_{CS}$ 0.380         0.400         -         V         0[ms] ~ Tss1[ms]           Overcurrent detection voltage SS2 $V_{CS,SS1}$ -         0.150         -         V         Tss1[ms] ~ Tss2[ms]           Overcurrent detection voltage SS3 $V_{CS,SS3}$ -         0.200         -         V         Tss2[ms] ~ Tss2[ms]           Overcurrent detection voltage SS4 $V_{CS,SS4}$ -         0.300         -         V         Tss3[ms] ~ Tss3[ms]           Overcurrent detection voltage SS4 $V_{CS,SS4}$ -         0.300         -         V         Tss3[ms] ~ Tss4[ms]           Leading Edge Blanking Time         TLEB         -         250         -         ns            Over current detection AC Voltage compensation factor         Kcs         12         20         28         mV/us            SOURCE pin short protection voltage $V_{CSHT}$ 0.020         0.050 <td></td> <td>T<sub>FOLP1</sub></td> <td></td> <td>-</td> <td></td> <td>ms</td> <td></td>		T <sub>FOLP1</sub>		-		ms	
[Over current detection block]           Overcurrent detection voltage         V <sub>CS</sub> 0.380         0.400         0.420         V         Ton=0us           Overcurrent detection voltage SS1         V <sub>CS,SS1</sub> -         0.100         -         V         0[ms] ~ Tss1[ms]           Overcurrent detection voltage SS2         V <sub>CS,SS2</sub> -         0.150         -         V         Tss1[ms] ~ Tss2[ms]           Overcurrent detection voltage SS3         V <sub>CS,SS3</sub> -         0.200         -         V         Tss1[ms] ~ Tss2[ms]           Overcurrent detection voltage SS4         V <sub>CS,SS4</sub> -         0.300         -         V         Tss3[ms]           Overcurrent detection voltage SS4         V <sub>CS,SS4</sub> -         0.300         -         V         Tss3[ms]           Over current detection AC Voltage compensation factor         TLEB         -         250         -         ns           Over current detection voltage         K <sub>CS</sub> 12         20         28         mV/us           SOURCE pin short protection voltage         V <sub>CSHT</sub> 0.020         0.050         0.080         V           [Start current 1         Istart1         0.100         0.500         1.000         mA         VCC= 0V		T <sub>FOLP1b</sub>				ms	
Overcurrent detection voltage $V_{CS}$ 0.3800.4000.420VTon=0usOvercurrent detection voltage SS1 $V_{CS_SS1}$ -0.100-V0[ms] ~ Tss1[ms]Overcurrent detection voltage SS2 $V_{CS_SS2}$ -0.150-VTss1[ms] ~ Tss2[ms]Overcurrent detection voltage SS3 $V_{CS_SS3}$ -0.200-VTss2[ms] ~ Tss2[ms]Overcurrent detection voltage SS4 $V_{CS_SS3}$ -0.300-VTss2[ms] ~ Tss3[ms]Overcurrent detection voltage SS4 $V_{CS_SS4}$ -0.300-VTss3 [ms] ~ Tss4 [ms]Leading Edge Blanking Time $T_{LEB}$ -250-nsOver current detection AC Voltage compensation factor $K_{CS}$ 122028mV/usSOURCE pin short protection voltage $V_{CSSHT}$ 0.0200.0500.080VStart current 1 $I_{START1}$ 0.1000.5001.000mAVCC=0VStart current 2 $I_{START2}$ 1.0003.0006.000mAVCC=10VOFF current $I_{START3}$ -1020uAafter UVLO released UVLO. When MOSFET is OFF		T <sub>FOLP2</sub>	358	512	666	ms	
Overcurrent detection voltage SS1 $V_{CS,SS1}$ - $0.100$ -V $0[ms] \sim Tss1[ms]$ Overcurrent detection voltage SS2 $V_{CS,SS2}$ - $0.150$ -V $Tss1[ms] \sim Tss2[ms]$ Overcurrent detection voltage SS3 $V_{CS,SS3}$ - $0.200$ -V $Tss2[ms] \sim Tss2[ms]$ Overcurrent detection voltage SS4 $V_{CS,SS3}$ - $0.200$ -V $Tss2[ms] \sim Tss2[ms]$ Overcurrent detection voltage SS4 $V_{CS,SS4}$ - $0.300$ -V $Tss3[ms] \sim Tss4[ms]$ Leading Edge Blanking Time $T_{LEB}$ - $250$ -nsOver current detection AC Voltage compensation factor $K_{CS}$ $12$ $20$ $28$ mV/usSOURCE pin short protection voltage $V_{CSSHT}$ $0.020$ $0.050$ $0.080$ V[Start current 1 $I_{START1}$ $0.100$ $0.500$ $1.000$ mAVCC= 0VStart current 2 $I_{START2}$ $1.000$ $3.000$ $6.000$ mAVCC=10VOFF current $I_{START3}$ - $10$ $20$ $uA$ Inflow current from Drain pinafter UVLO released UVLO. When MOSFET is OFF							
Overcurrent detection voltage SS2 $V_{CS\_SS2}$ - $0.150$ -V $T_{SS1}[ms] \sim T_{SS2}[ms]$ Overcurrent detection voltage SS3 $V_{CS\_SS3}$ - $0.200$ -V $T_{SS2}[ms] \sim T_{SS3}[ms]$ Overcurrent detection voltage SS4 $V_{CS\_SS4}$ - $0.300$ -V $T_{SS3}[ms] \sim T_{SS4}[ms]$ Leading Edge Blanking Time $T_{LEB}$ - $250$ -nsOver current detection AC Voltage compensation factor $K_{CS}$ $12$ $20$ $28$ mV/usSOURCE pin short protection voltage $V_{CSSHT}$ $0.020$ $0.050$ $0.080$ VIstart current 1 $I_{START1}$ $0.100$ $0.500$ $1.000$ mAVCC= 0VStart current 2 $I_{START2}$ $1.000$ $3.000$ $6.000$ mAVCC=10VOFF current $I_{START3}$ - $10$ $20$ $uA$ Inflow current from Drain pin after UVLO released UVLO. When MOSFET is OFF	•		0.380		0.420		
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$\begin{tabular}{ c c c c c c c c c c c c c c c c c c c$			-		-		
Over current detection AC Voltage compensation factor       K <sub>CS</sub> 12       20       28       mV/us         SOURCE pin short protection voltage       V <sub>CSSHT</sub> 0.020       0.050       0.080       V         [Start circuit block]       V       Start current 1       Istart1       0.100       0.500       1.000       mA       VCC= 0V         Start current 2       Istart2       1.000       3.000       6.000       mA       VCC=10V         OFF current       Istart3       -       10       20       uA       Inflow current from Drain pin after UVLO released UVLO. When MOSFET is OFF	•		-		-		I SS3 [ <b>MS</b> ] ~ I SS4 [ <b>MS</b> ]
compensation factorK_CS122028IIIV/USSOURCE pin short protection voltageV CSSHT0.0200.0500.080V[Start circuit block]Start current 1Istart10.1000.5001.000mAVCC= 0VStart current 2Istart21.0003.0006.000mAVCC=10VOFF currentIstart3-1020uAInflow current from Drain pin after UVLO released UVLO. When MOSFET is OFF		T <sub>LEB</sub>	-	250	-	ns	
short protection voltage         V <sub>CSSHT</sub> 0.020         0.050         0.080         V           [Start circuit block]         Start current 1         I <sub>START1</sub> 0.100         0.500         1.000         mA         VCC= 0V           Start current 2         I <sub>START2</sub> 1.000         3.000         6.000         mA         VCC=10V           OFF current         I <sub>START3</sub> -         10         20         uA         Inflow current from Drain pin after UVLO released UVLO. When MOSFET is OFF	compensation factor	K <sub>cs</sub>	12	20	28	mV/us	
Start current 1         I <sub>START1</sub> 0.100         0.500         1.000         mA         VCC= 0V           Start current 2         I <sub>START2</sub> 1.000         3.000         6.000         mA         VCC=10V           OFF current         I <sub>START3</sub> -         10         20         uA         Inflow current from Drain pin after UVLO released UVLO. When MOSFET is OFF		$V_{\text{CSSHT}}$	0.020	0.050	0.080	V	
Start current 2     I <sub>START2</sub> 1.000     3.000     6.000     mA     VCC=10V       OFF current     I <sub>START3</sub> -     10     20     uA     Inflow current from Drain pin after UVLO released UVLO. When MOSFET is OFF	[Start circuit block]						
Start current 2     I <sub>START2</sub> 1.000     3.000     6.000     mA     VCC=10V       OFF current     I <sub>START3</sub> -     10     20     uA     Inflow current from Drain pin after UVLO released UVLO. When MOSFET is OFF	Start current 1	ISTART1	0.100	0.500	1.000	mA	
OFF current I <sub>START3</sub> - 10 20 uA Inflow current from Drain pin after UVLO released UVLO. When MOSFET is OFF							VCC=10V
			-				after UVLO released UVLO.
	Start current switching voltage	V <sub>sc</sub>	0.800	1.500	2.100	V	

# •PIN DESCRIPTIONS

					Diode
NO.	Pin Name	I/O	Function	VCC	GND
1	SOURCE	I/O	MOSFET SOURCE pin	0	0
2	N.C.	-	-	-	-
3	GND	I/O	GND pin	0	-
4	FB	-	Feedback signal input pin	-	0
5	VCC	-	Power supply input pin	-	0
6	DRAIN	I/O	MOSFET DRAIN pin	-	-
7	DRAIN	I/O	MOSFET DRAIN pin	-	-

# Table 1 Pin Description

# •I/O Equivalent Circuit Diagram

7	DRAIN	6	DRAIN			5	VCC
Internal Circuit Intern	DRAIN DRAIN MOSFET SOURCE	Internal Circuit Intern	DRAIN DRAIN			vcc 📑	
1	SOURCE	2	N.C.	3	GND	4	FB
SOURCE Z					GND	FB T	RFB

Figure 2 I/O Equivalent Circuit Diagram

Block Diagram

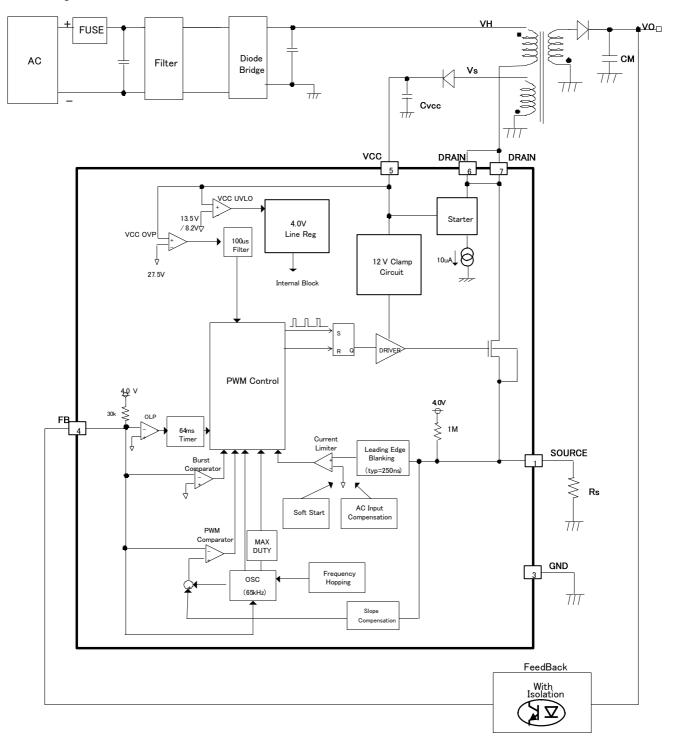


Figure 3. Block Diagram

# Description of Blocks

#### (1) Start circuit (DRIAN: 6,7pin)

This IC built in Start circuit (tolerates 650V). It enables to be low standby mode electricity and high speed starting. After starting, consumption power is idling current I<sub>START3</sub>(typ=10uA) only.

Reference values of Starting time are shown in Figure-6. When Cvcc=10uF it can start less than 0.1 sec.

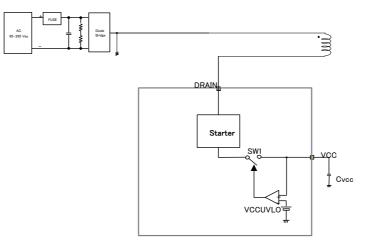
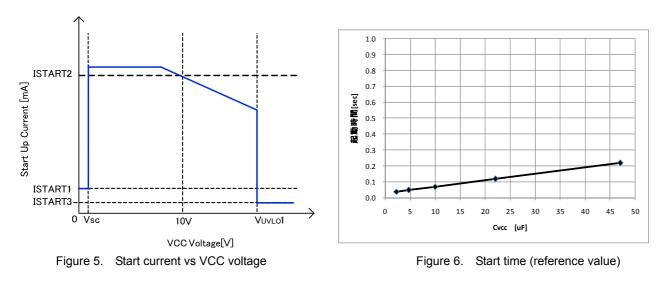


Figure 4. Block diagram of start circuit



\* Start current flows from the DRAIN pin

- Ex) Consumption power of start circuit only when the Vac=100V PVH=100V\* $\sqrt{2}$ \*10uA=1.41mW
- Ex) Consumption power of start circuit only when the Vac=240V PVH=240V\* $\sqrt{2}$ \*10uA=3.38mW

#### (2) Start sequences (Soft start operation, light load operation, and auto recovery operation during overload protection)

Start sequences are shown in Figure 7. See the sections below for detailed descriptions.

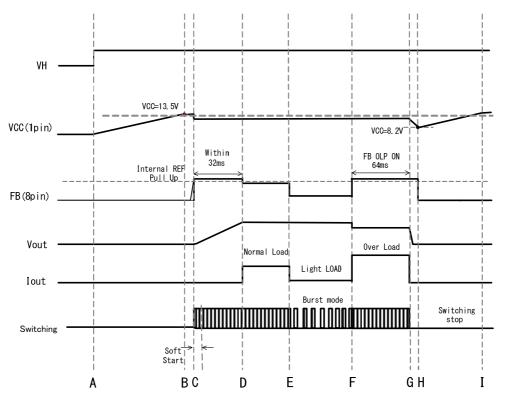


Figure 7. Start sequences Timing Chart

- A: Input voltage VH is applied
- B: This IC starts operation when VCC pin voltage rises and VCC > V<sub>UVLO1</sub> (13.5 V typ).Switching function starts when other protection functions are judged as normal. Until the secondary output voltage becomes constant level, VCC voltage drops because of the VCC consumption current. VCC recharge function start if VCC voltage < V<sub>CHG1</sub> (8.7V typ)
- C: With the soft start function, over current limit value is restricted to prevent any excessive rise in voltage or current.
- D: When the switching operation starts, VOUT rises. The output voltage become to stable state, VCC voltage also become to stable state through auxiliary winding. Please set the rated voltage within the T<sub>FOLP1b</sub> period (32ms typ) from VCC voltage > V<sub>UVLO1</sub>.
- E: During a light load, if it reaches FB voltage < V<sub>BST</sub> (= 0.4Vtyp), the IC starts burst operation to keep power consumption low. During burst operation, it becomes low-power consumption mode.
- F: When the FB Voltage> $V_{FOLP1A}$ (=2.8V typ), it becomes a overload operation.
- G: When FB pin voltage keeps V<sub>FOLP1A</sub> (= 2.8V typ) at or above T<sub>FOLP1</sub> (64ms typ), the overload protection function is triggered and switching stops 64ms later. If the FB pin voltage becomes FB<V<sub>FOLP1B</sub> even once, the IC's FB OLP timer is reset.
- H: If the VCC voltage drops to VCC < V<sub>UVLO2</sub> (8.2Vtyp) or below, restart is executed.
- I: The IC's circuit current is reduced and the VCC pin value rises. (Same as B)

# (3) VCC pin protection function

BM2PXX3 built in VCC low voltage protection function VCCUVLO (Under Voltage Lock Out), over voltage protection function VCC OVP (Over Voltage Protection) and VCC charge function that operates in case of dropping the VCC voltage.VCC UVLO and VCC OVP monitor VCC pin and prevent VCC pin from destroying switching MOSFET at abnormal voltage.

VCC charge function stabilizes the secondary output voltage by charging from the high voltage line by start circuit at dropping the VCC voltage.

#### (3-1) VCC UVLO 🗡 VCC OVP function

VCCUVLO is auto recovery protection. VCCOVP is latch protection. Refer to the operation figure-8. VCCOVP built in mask time  $T_{LATCH}$  (typ=100us).By this function, this IC masks pin generated surge etc. This function operates detection in case of continuing VCC pin voltage >  $V_{OVP1}$  (typ=27.5V).

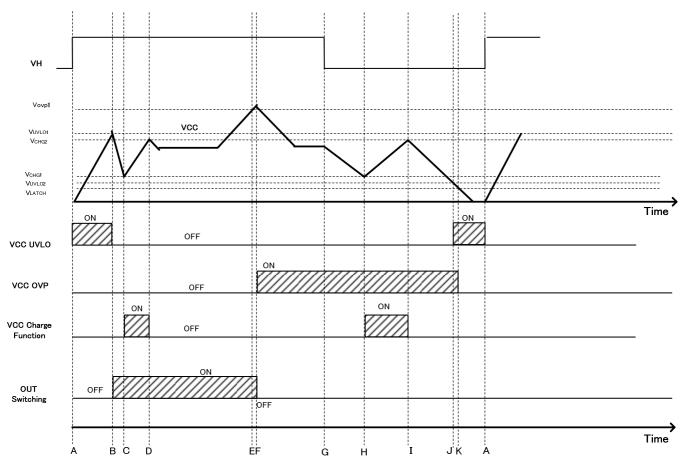


Figure 8. VCC UVLO / OVP Timing Chart

- A: DRAIN voltage input, VCC pin voltage starts rising.
- B: VCC>VUVLO1, DC/DC operation starts
- C: VCC< V<sub>CHG1</sub>, VCC charge function operates and the VCC voltage rises.
- D: VCC >  $V_{CHG2}$ , VCC charge function is stopped.
- E: VCC > V<sub>OVP1</sub>, function is detected
- F: VCC >  $V_{OVP1}$ , continues  $T_{LATCH}$  (typ =100us), switching is stopped by the VCCOVP function.
- G: VH is OPEN.VCC Voltage is fall.
- H: Same as C.
- I: Same as D.
- J: VCC<V<sub>UVLO2</sub>, Switching is stopped by the VCC UVLO function
- K: VCC<  $V_{LATCH}$ , released from latch

# (3-2) VCC Charge function

After VCC charge function operates once the VCC pin  $>V_{UVLO1}$  and the DC/DC operation starts then the VCC pin voltage drops to  $<V_{CHG1}$ . At that time the VCC pin is charged from DRAIN pin through start circuit. By this operation, BM2PXX3 doesn't occur to start failure.

When VCC pin voltage rises to VCC > $V_{CHG2}$ , charge is stopped. The operations are shown in figure 9.

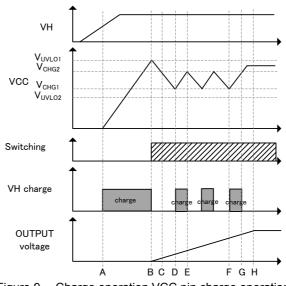


Figure 9. Charge operation VCC pin charge operation

- A: DRAIN pin voltage rises, charge starts to VCC pin by the VCC charge function.
- B: VCC > V<sub>UVL01</sub>, VCC UVLO function releases, VCC charge function stops, DC/DC operation starts.
- C: When DC/DC operation starts, the VCC voltage drops.
- D: VCC < V<sub>CHG1</sub>, VCC recharge function and VCC pin voltage rises.
- E: VCC >  $V_{CHG2}$ , VCC recharge function stops.
- F: VCC <  $V_{CHG1}$ , VCC recharge function operates and VCC pin voltage rises.
- G: VCC >  $V_{CHG2}$ , VCC recharge function stops.
- H: After start of output voltage finished, VCC is charged by the auxiliary winding VCC pin stabilizes.

# (4) DCDC driver (PWM comparator, frequency hopping, slope compensation, OSC, burst)

BM2PXX3 is current mode PWM control.

An internal oscillator sets a fixed switching frequency (65 kHz typ).

BM2PXX3 is integrated switching frequency hopping function which changes the switching frequency to fluctuate as shown in Figure 10 below.

The fluctuation cycle is 125 Hz typ.

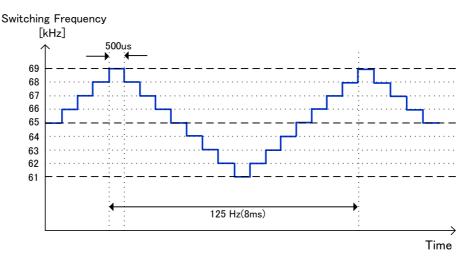


Figure 10. Frequency hopping function

Max duty cycle is fixed as 75% (typ) and MIN pulse width is fixed as 400 ns (typ).

With current mode control, when the duty cycle exceeds 50% sub harmonic oscillation may occur.

As a countermeasure to this, BM2PXX3 is built in slope compensation circuits.

BM2PXX3 is built in burst mode circuit and frequency reduction circuit to achieve lower power consumption, when the load is light.

FB pin is pull up by  $R_{FB}$  (30 k $\Omega$  typ).

FB pin voltage is changed by secondary output voltage (secondary load power).

FB pin is monitored, burst mode operation and frequency detection start.

Figure 11 shows the FB voltage, and switching frequency, DCDC operation

•mode1 : Burst operation

mode2 : Frequency reduction operation.

mode3 : Fixed frequency operation.(operate at the max frequency)

·mode4 : Over load operation.(detect the over load state and stop the pulse operation)

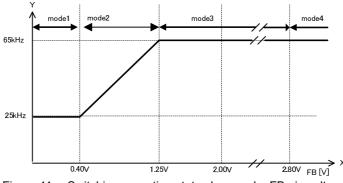


Figure 11. Switching operation state changes by FB pin voltage

# (5) Over Current limiter

BM2PXX3 is built in Over Current limiter per cycle. If the SOURCE pin exceeds a certain voltage, switching is stopped. It is also built in AC voltage compensation function. This is the function which compensates the maximum power as the AC voltage's change by increasing over current limiter with time.

Shown in figure-12, 13, and 14.

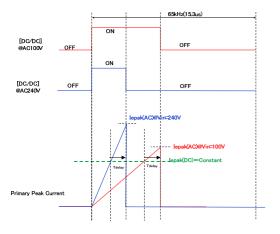


Figure 12. No AC voltage compensation function

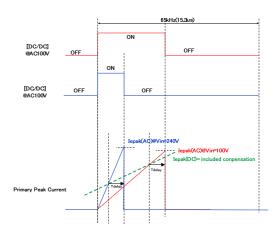


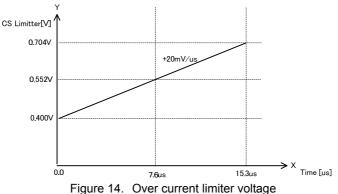
Figure 13. Built-in AC compensation voltage

Primary peak current is decided as the formula below.

Primary peak current: Ipeak = Vcs/Rs + Vdc/Lp\*Tdelay

 $V_{cs}: Over \ current \ limiter \ voltage \ internal \ IC, \ Rs: Current \ detection \ resistance, \ V_{dc} \ input \ DC \ voltage, \ L_p: Primary \ inductance,$ 

Tdelay: delay time after detection of over current limiter



#### (6) L.E.B period

When the driver MOSFET is turned ON, surge current occurs at each capacitor component and drive current. Therefore, because SOURCE pin voltage rises temporarily, the detection errors may occur in the over current limiter circuit.

To prevent detection errors, DRAIN is switched from high to low and the SOURCE signal is masked for 250 ns by the on-chip LEB (Leading Edge Blanking) function.

# (7) SOURCE pin (1pin) short protection function

When the SOURCE pin (1pin) is shorted, BM2PXX3 is over heat. BM2PXX3 built in short protection function to prevent destroying.

# (8) SOURCE pin (1pin) open protection

If the SOURCE pin becomes OPEN, BM2PXX3 may be damaged. To prevent to be damaged, BM2PXX3 built in OPEN protection circuit(auto recovery protection).

# (9) Output over load protection function (FB OLP Comparator)

The output overload protection function monitors the secondary output load status at the FB pin, and stops switching when an overload occurs. In case of an overload, the output voltage is reduced and current no longer flows to the photo coupler, so the FB pin voltage rises.

When the FB pin voltage >  $V_{FOLP1A}$  (2.8 V typ) continuously for the period  $T_{FOLP1}$  (64ms typ), it is judged as an overload and stops switching.

When the FB pin >  $V_{FOLP1A}$  (2.8 V typ), if the voltage goes lower than  $V_{FOLP1B}$  (2.6V typ) during the period  $T_{FOLP1}$  (64ms typ), the overload protection timer is reset. The switching operation is performed during this period  $T_{FOLP1}$  (64ms typ).

At startup, the FB voltage is pulled up to the IC's internal voltage, so operation starts at a voltage of  $V_{FOLP1A}$  (2.8 V typ) or above. Therefore, at startup the FB voltage must be set to go to  $V_{FOLP1B}$  (2.6 V typ) or below during the period  $T_{FOLP1}$  (64ms typ), and the secondary output voltage's start time must be set within the period  $T_{FOLP1}$  (64ms typ) following startup of the IC.

Recovery from the once detection of FBOLP, after the period  $T_{FOLP2}$  (512 ms typ)

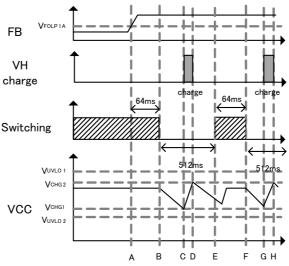


Figure 15. Over load protection (Auto recovery)

- A: The FBOLP comparator detects over load for FB>V<sub>FOLP1A</sub>
- B: If the State of A continues for the period T<sub>FOLP1</sub> (64ms typ), it is judged as an overload and stops switching after 64ms.
- C: While switching stops for the over load protection function, the VCC pin voltage drops and VCC pin voltage reaches < V<sub>CHG1</sub>, the VCC charge function operates so the VCC pin voltage rises.
- D: VCC charge function stops when VCC pin voltage > V<sub>CHG2</sub>
- E: If T<sub>FOLP2</sub> (typ =512ms) go on from B point, Switching function starts on soft start.
- F: If T<sub>FOLP1</sub> (64ms typ) go on from E point to continues an overload condition (FB>V<sub>FOLP1A)</sub>, Switching function stops at F point.
- G: While switching stops VCC pin voltage drops to < V<sub>CHG1</sub>, VCC charge function operates and VCC pin voltage rises.
- H: If VCC pin (5pin) voltage becomes over V<sub>CHG2</sub> by the VCC charge function, VCC charge function operation stops.

# •Operation mode of protection circuit

Operation mode of protection functions are shown in table2.

TableO	Onerstien	manda of		a:
Table2	Operation	mode or	protection	CITCUIL

Function	Operation mode
VCC Under Voltage Locked Out	Auto recovery
VCC Over Voltage Protection	Latch (with 100us timer)
TSD	Latch (with 100us timer)
FB Over Limited Protection	Auto recovery(with 64ms timer)
SOURCE Open Protection	Auto recovery

#### Sequence

The sequence diagram is show in Fig 16. All condition transits OFF Mode VCC<8.2V

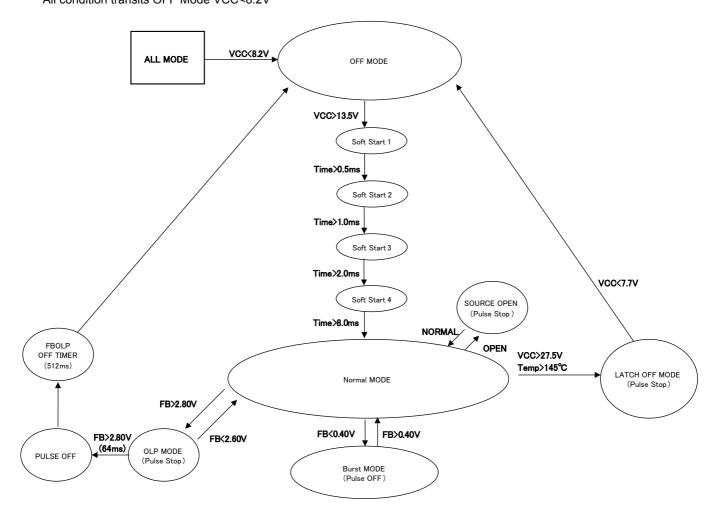


Figure 16. The sequence diagram

# • Thermal loss

The thermal design should set operation for the following conditions. (Since the temperature shown below is the guaranteed temperature, be sure to take a margin into account.)

- 1. The ambient temperature Ta must be 105°C or less.
- 2. The IC's loss must be within the allowable dissipation Pd.

The thermal abatement characteristics are as follows. (PCB: 74.2 mm × 74.2mm × 1.6 mm, mounted on glass epoxy double-layer substrate)

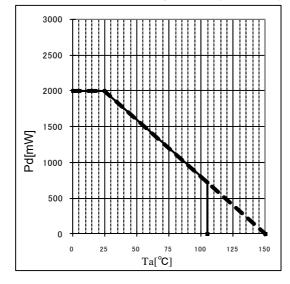
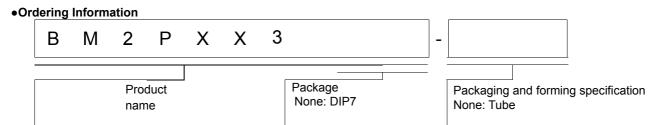


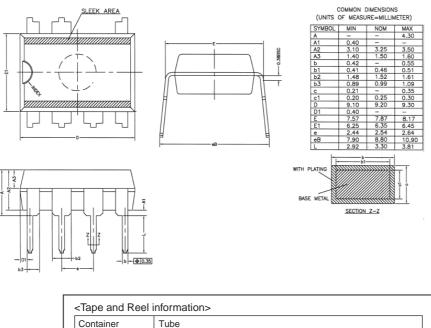
Figure 17. DIP7 Thermal Abatement Characteristics

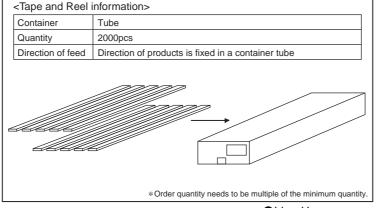




Physical Dimension Tape and Reel Information

DIP7

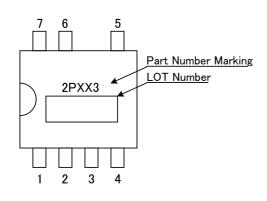




Making Diagram

●Line-Up

DIP7



Product name (B	M2PXX3)
BM2P013	5
BM2P033	5
BM2P053	}
BM2P093	}

# **Operational Notes**

# 1. Reverse Connection of Power Supply

Connecting the power supply in reverse polarity can damage the IC. Take precautions against reverse polarity when connecting the power supply, such as mounting an external diode between the power supply and the IC's power supply pins.

# 2. Power Supply Lines

Design the PCB layout pattern to provide low impedance supply lines. Separate the GND and supply lines of the digital and analog blocks to prevent noise in the GND and supply lines of the digital block from affecting the analog block. Furthermore, connect a capacitor to GND at all power supply pins. Consider the effect of temperature and aging on the capacitance value when using electrolytic capacitors.

# 3. GND Voltage

Ensure that no pins are at a voltage below that of the GND pin at any time, even during transient condition.

# 4. GND Wiring Pattern

When using both small-signal and large-current GND traces, the two GND traces should be routed separately but connected to a single GND at the reference point of the application board to avoid fluctuations in the small-signal GND caused by large currents. Also ensure that the GND traces of external components do not cause variations on the GND voltage. The GND lines must be as short and thick as possible to reduce line impedance.

# 5. Thermal Consideration

Should by any chance the power dissipation rating be exceeded the rise in temperature of the chip may result in deterioration of the properties of the chip. The absolute maximum rating of the Pd stated in this specification is when the IC is mounted on a 70mm x 70mm x 1.6mm glass epoxy board. In case of exceeding this absolute maximum rating, increase the board size and copper area to prevent exceeding the Pd rating.

# 6. Recommended Operating Conditions

These conditions represent a range within which the expected characteristics of the IC can be approximately obtained. The electrical characteristics are guaranteed under the conditions of each parameter.

# 7. Inrush Current

When power is first supplied to the IC, it is possible that the internal logic may be unstable and inrush current may flow instantaneously due to the internal powering sequence and delays, especially if the IC has more than one power supply. Therefore, give special consideration to power coupling capacitance, power wiring, width of GND wiring, and routing of connections.

# 8. Operation Under Strong Electromagnetic Field

Operating the IC in the presence of a strong electromagnetic field may cause the IC to malfunction.

# 9. Testing on Application Boards

When testing the IC on an application board, connecting a capacitor directly to a low-impedance output pin may subject the IC to stress. Always discharge capacitors completely after each process or step. The IC's power supply should always be turned off completely before connecting or removing it from the test setup during the inspection process. To prevent damage from static discharge, GND the IC during assembly and use similar precautions during transport and storage.

# 10. Inter-pin Short and Mounting Errors

Ensure that the direction and position are correct when mounting the IC on the PCB. Incorrect mounting may result in damaging the IC. Avoid nearby pins being shorted to each other especially to GND, power supply and output pin. Inter-pin shorts could be due to many reasons such as metal particles, water droplets (in very humid environment) and unintentional solder bridge deposited in between pins during assembly to name a few.

# **Operational Notes – continued**

#### 11. Unused Input Pins

Input pins of an IC are often connected to the gate of a MOS transistor. The gate has extremely high impedance and extremely low capacitance. If left unconnected, the electric field from the outside can easily charge it. The small charge acquired in this way is enough to produce a significant effect on the conduction through the transistor and cause unexpected operation of the IC. So unless otherwise specified, unused input pins should be connected to the power supply or GND line.

#### 12. Regarding the Input Pin of the IC

This monolithic IC contains P+ isolation and P substrate layers between adjacent elements in order to keep them isolated. P-N junctions are formed at the intersection of the P layers with the N layers of other elements, creating a parasitic diode or transistor. For example (refer to figure below):

When GND > Pin A and GND > Pin B, the P-N junction operates as a parasitic diode. When GND > Pin B, the P-N junction operates as a parasitic transistor.

Parasitic diodes inevitably occur in the structure of the IC. The operation of parasitic diodes can result in mutual interference among circuits, operational faults, or physical damage. Therefore, conditions that cause these diodes to operate, such as applying a voltage lower than the GND voltage to an input pin (and thus to the P substrate) should be avoided.

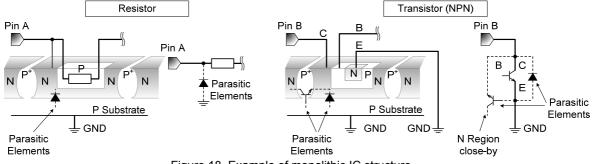


Figure 18. Example of monolithic IC structure

#### 13. Ceramic Capacitor

When using a ceramic capacitor, determine the dielectric constant considering the change of capacitance with temperature and the decrease in nominal capacitance due to DC bias and others.

# 14. Area of Safe Operation (ASO)

Operate the IC such that the output voltage, output current, and power dissipation are all within the Area of Safe Operation (ASO).

# 15. Thermal Shutdown Circuit(TSD)

This IC has a built-in thermal shutdown circuit that prevents heat damage to the IC. Normal operation should always be within the IC's power dissipation rating. If however the rating is exceeded for a continued period, the junction temperature (Tj) will rise which will activate the TSD circuit that will turn OFF all output pins. The IC should be powered down and turned ON again to resume normal operation because the TSD circuit keeps the outputs at the OFF state even if the TJ falls below the TSD threshold.

Note that the TSD circuit operates in a situation that exceeds the absolute maximum ratings and therefore, under no circumstances, should the TSD circuit be used in a set design or for any purpose other than protecting the IC from heat damage.

#### **16.** Over Current Protection Circuit (OCP)

This IC incorporates an integrated over current protection circuit that is activated when the load is shorted. This protection circuit is effective in preventing damage due to sudden and unexpected incidents. However, the IC should not be used in applications characterized by continuous operation or transitioning of the protection circuit.

date	Rev. No.	Revision Point
2012.07.19	001	New Release
2013.11.18	005	<ul> <li>P7 An explanation for Figure7</li> <li>P8 An explanation for VCC_UVLO/VCC_OVP function <ul> <li>An explanation for Figure8</li> <li>P11 An explanation for Over Current limiter</li> <li>P12 An explanation for Output over load protection function <ul> <li>An explanation for Figure15</li> <li>P13 Table2</li> <li>P13 Figure16</li> </ul> </li> </ul></li></ul>
2015.05.15	006	P13 Operation mode of protection circuit P13 Sequence
2015.09.24	007	P7 An explanation of Start sequence P8 An explanation of VCC pin protection function P8 An explanation of VCC UVLO / VCC OVP function P9 An explanation of VCC Charge function P11 An explanation of Over Current Limiter P12 An explanation of Output over load protection function
2017.03.07	008	P1 An explanation of package height P2 Format for Electrical Characteristics of MOSFET P3 Format for Electrical Characteristics of Control IC P3 An explanation of Thermal shut down temperature P7 An explanation of Start sequences P8 An explanation of Figure8 P9 An explanation of VCC pin protection function P12 An explanation of OUTPUT over load protection function P13 An explanation of Table2 value

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  - [g] Use of our Products without cleaning residue of flux (even if you use no-clean type fluxes, cleaning residue of flux is recommended); or Washing our Products by using water or water-soluble cleaning agents for cleaning residue after soldering
  - [h] Use of the Products in places subject to dew condensation
- 4. The Products are not subject to radiation-proof design.
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- 6. In particular, if a transient load (a large amount of load applied in a short period of time, such as pulse. is applied, confirmation of performance characteristics after on-board mounting is strongly recommended. Avoid applying power exceeding normal rated power; exceeding the power rating under steady-state loading condition may negatively affect product performance and reliability.
- 7. De-rate Power Dissipation depending on ambient temperature. When used in sealed area, confirm that it is the use in the range that does not exceed the maximum junction temperature.
- 8. Confirm that operation temperature is within the specified range described in the product specification.
- 9. ROHM shall not be in any way responsible or liable for failure induced under deviant condition from what is defined in this document.

# Precaution for Mounting / Circuit board design

- 1. When a highly active halogenous (chlorine, bromine, etc.) flux is used, the residue of flux may negatively affect product performance and reliability.
- 2. In principle, the reflow soldering method must be used on a surface-mount products, the flow soldering method must be used on a through hole mount products. If the flow soldering method is preferred on a surface-mount products, please consult with the ROHM representative in advance.

For details, please refer to ROHM Mounting specification

# **Precautions Regarding Application Examples and External Circuits**

- 1. If change is made to the constant of an external circuit, please allow a sufficient margin considering variations of the characteristics of the Products and external components, including transient characteristics, as well as static characteristics.
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#### **Precaution for Electrostatic**

This Product is electrostatic sensitive product, which may be damaged due to electrostatic discharge. Please take proper caution in your manufacturing process and storage so that voltage exceeding the Products maximum rating will not be applied to Products. Please take special care under dry condition (e.g. Grounding of human body / equipment / solder iron, isolation from charged objects, setting of lonizer, friction prevention and temperature / humidity control).

#### Precaution for Storage / Transportation

- 1. Product performance and soldered connections may deteriorate if the Products are stored in the places where:
  - [a] the Products are exposed to sea winds or corrosive gases, including Cl2, H2S, NH3, SO2, and NO2
  - [b] the temperature or humidity exceeds those recommended by ROHM
  - [c] the Products are exposed to direct sunshine or condensation
  - [d] the Products are exposed to high Electrostatic
- 2. Even under ROHM recommended storage condition, solderability of products out of recommended storage time period may be degraded. It is strongly recommended to confirm solderability before using Products of which storage time is exceeding the recommended storage time period.
- 3. Store / transport cartons in the correct direction, which is indicated on a carton with a symbol. Otherwise bent leads may occur due to excessive stress applied when dropping of a carton.
- 4. Use Products within the specified time after opening a humidity barrier bag. Baking is required before using Products of which storage time is exceeding the recommended storage time period.

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