

# NLX1G99

## Configurable Multifunction Gate

The NLX1G99 MiniGate™ is an advanced high-speed CMOS multifunction gate with a 3-state output. With the output enable input ( $\overline{OE}$ ) at High, the output is disabled and is kept at high impedance. With the output enable input ( $\overline{OE}$ ) at Low, the device can be configured for logic functions such as MUX, AND, OR, NAND, NOR, XOR, XNOR, INVERT and BUFFER, depending on the combination of the 4-bit input. The device has Schmitt-trigger inputs, thereby enhancing noise immunity.

The NLX1G99 input and output structures provide protection when voltages up to 7.0 V are applied, regardless of the supply voltage.

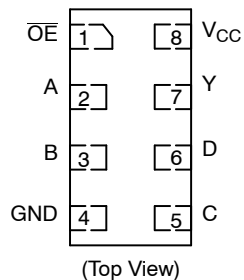
### Features

- High Speed:  $t_{PD} = 6.7$  ns (Max) @  $V_{CC} = 3.3$  V
- Low Power Dissipation:  $I_{CC} = 1$   $\mu$ A (Max) at  $T_A = 25^\circ$ C
- Power Down Protection Provided on inputs
- Balanced Propagation Delays
- Overvoltage Tolerant (OVT) Input and Output Pins
- Ultra-Small Packages
- These are Pb-Free Devices

### PIN ASSIGNMENT

1	$\overline{OE}$
2	A
3	B
4	GND
5	C
6	D
7	Y
8	$V_{CC}$

### PIN ASSIGNMENTS



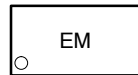
**ON Semiconductor®**

<http://onsemi.com>

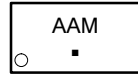
### MARKING DIAGRAMS



**ULLGA8**  
1.45 x 1.0  
CASE 613AA



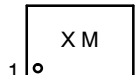
**ULLGA8**  
1.6 x 1.0  
CASE 613AB



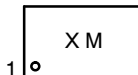
**ULLGA8**  
1.95 x 1.0  
CASE 613AC



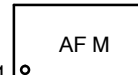
**UDFN8**  
1.45 x 1.0  
CASE 517BZ



**UDFN8**  
1.6 x 1.0  
CASE 517BY



**UDFN8**  
1.95 x 1.0  
CASE 517CA



AA or E = Specific Device Code  
M = Date Code  
▪ = Pb-Free Package

### ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 12 of this data sheet.

# NLX1G99

## FUNCTION DIAGRAM

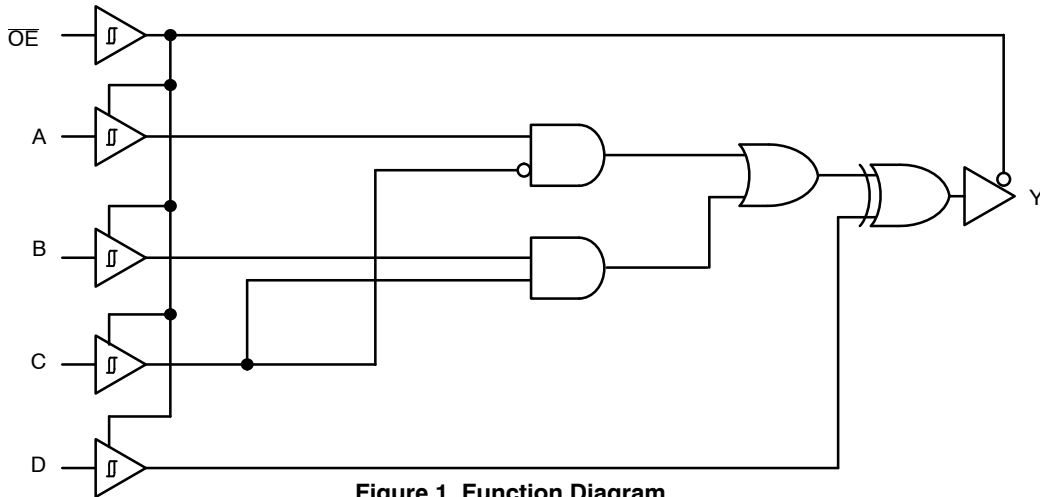


Figure 1. Function Diagram

## FUNCTION TABLE\*

INPUT					OUTPUT
OE	D	C	B	A	Y
L	L	L	L	L	L
L	L	L	L	H	H
L	L	L	H	L	L
L	L	L	H	H	H
L	L	H	L	L	L
L	L	H	L	H	L
L	L	H	H	L	H
L	L	H	H	H	H
L	H	L	L	L	H
L	H	L	L	H	L
L	H	L	H	L	H
L	H	L	H	H	L
L	H	H	L	L	H
L	H	H	L	H	H
L	H	H	H	L	L
L	H	H	H	H	L
H	H or L	H or L	H or L	H or L	Z

\*To select a logic function, please refer to "Logic Configurations" section.

FUNCTION SELECTION	LOGIC CONFIGURATION PAGE
3-State Buffers	3
3-State Inverters	3
3-State MUXes	3
3-State AND / OR / NOR	4
3-State NAND / OR	5
3-State XOR/XNOR	6

# NLX1G99

## LOGIC CONFIGURATIONS

### 3-State Buffer Functions Available

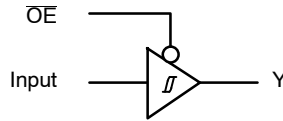


Figure 2.

Function	$\overline{OE}$	A	B	C	D
3-State Buffer	L	Input H or L L H H H or L L	H or L Input H L H or L L L	L H Input Input L H H or L	L L L H Input Input Input

### 3-State Inverter Functions Available

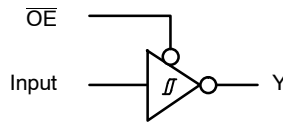


Figure 3.

Function	$\overline{OE}$	A	B	C	D
3-State Buffer	L	Input X L H H H or L H	H or L Input H L H or L H H	L H Input Input L H H or L	H H H L Input Input Input

### 3-State MUX Functions Available

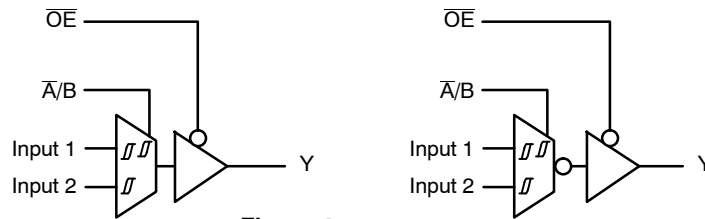


Figure 4.

Function	$\overline{OE}$	A	B	C	D
3-State 2-to-1	L	Input 1	Input 2	Input 1 or Input 2	L
3-State 2-to-1		Input 2	Input 1	$\overline{\text{Input 2}}$ or Input 1	L
3-State 2-to-1, Inverted Out		Input 1	Input 2	$\overline{\text{Input 1}}$ or Input 2	H
3-State 2-to-1, Inverted Out		Input 2	Input 1	$\overline{\text{Input 2}}$ or Input 1	H

# NLX1G99

## 3-State AND/NOR/OR Function Available

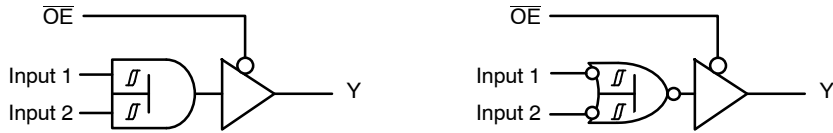


Figure 5.

No. of Inputs	AND/NAND Function	OR/NOR Function	$\overline{OE}$	A	B	C	D
2	3-State AND	3-State NOR	L	L	Input 1	Input 2	L
2	3-State AND	3-State NOR		L	Input 2	Input 1	L

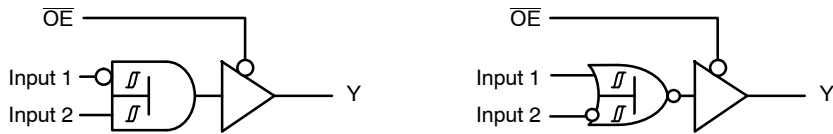


Figure 6.

No. of Inputs	AND/NAND Function	OR/NOR Function	$\overline{OE}$	A	B	C	D
2	3-State AND	3-State NOR	L	Input 2	L	Input 1	L
2	3-State AND	3-State NOR		H	Input 1	Input 2	H

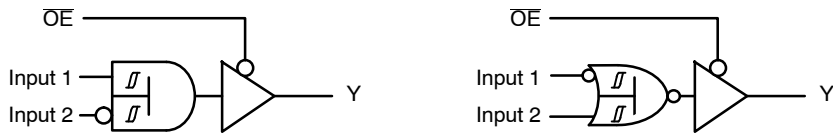


Figure 7.

No. of Inputs	AND/NAND Function	OR/NOR Function	$\overline{OE}$	A	B	C	D
2	3-State AND	3-State NOR	L	Input 1	L	Input 2	L
2	3-State AND	3-State NOR		H	Input 2	Input 1	H



Figure 8.

No. of Inputs	AND/NAND Function	OR/NOR Function	$\overline{OE}$	A	B	C	D
2	3-State AND	3-State OR	L	Input 1	H	Input 2	L
2	3-State AND	3-State OR		Input 2	H	Input 1	L

# NLX1G99

## 3-State NAND/OR Function Available

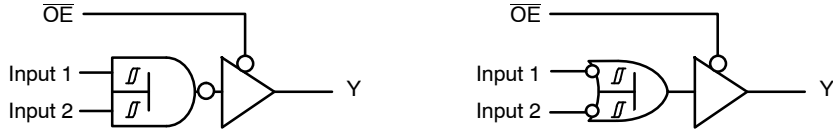


Figure 9.

No. of Inputs	AND/NAND Function	OR/NOR Function	$\overline{OE}$	A	B	C	D
2	3-State NAND	3-State OR	L	L	Input 1	Input 2	H
2	3-State NAND	3-State OR		L	Input 2	Input 1	H

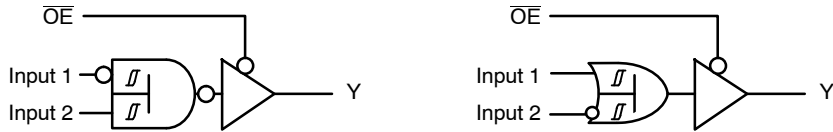


Figure 10.

No. of Inputs	AND/NAND Function	OR/NOR Function	$\overline{OE}$	A	B	C	D
2	3-State NAND	3-State OR	L	Input 2	L	Input 1	H
2	3-State NAND	3-State OR		H	Input 1	Input 2	L

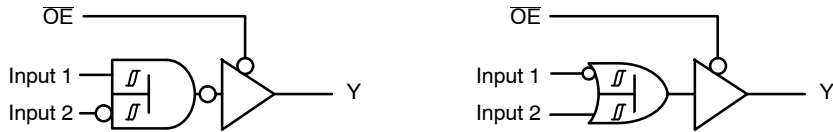


Figure 11.

No. of Inputs	AND/NAND Function	OR/NOR Function	$\overline{OE}$	A	B	C	D
2	3-State NAND	3-State OR	L	Input 1	L	Input 2	H
2	3-State NAND	3-State OR		H	Input 2	Input 1	L

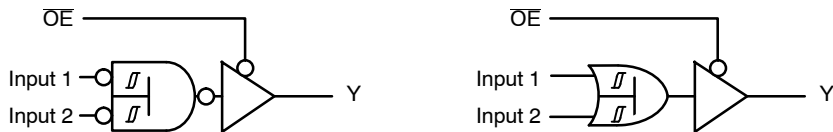


Figure 12.

No. of Inputs	AND/NAND Function	OR/NOR Function	$\overline{OE}$	A	B	C	D
2	3-State AND	3-State OR	L	Input 1	H	Input 2	L
2	3-State AND	3-State OR		Input 2	H	Input 1	L

# NLX1G99

## 3-State XOR/XNOR Function Available

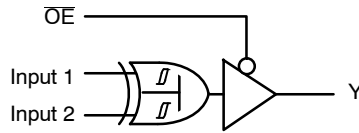


Figure 13.

Function	$\overline{OE}$	A	B	C	D
3-State XOR	L	Input 1 Input 2 H or L H or L L L	H or L H or L Input 1 Input 2 H H	L L H Input 1 Input 2	Input 2 Input 1 Input 2 Input 1 Input 2 Input 1

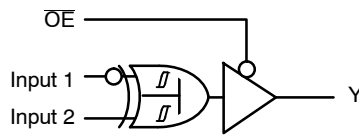


Figure 14.

Function	$\overline{OE}$	A	B	C	D
3-State XOR	L	H	L	Input 1	Input 2

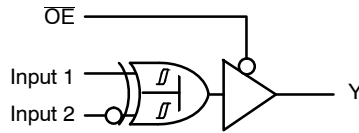


Figure 15.

Function	$\overline{OE}$	A	B	C	D
3-State XOR	L	H	L	Input 1	Input 2

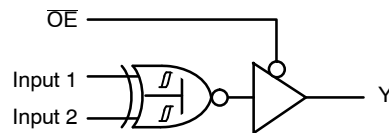


Figure 16.

Function	$\overline{OE}$	A	B	C	D
3-State XNOR	L	H	L	Input 1	Input 2
3-State XNOR	L	H	L	Input 1 Input 2	Input 2 Input 1

# NLX1G99

## MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
$V_{CC}$	DC Supply Voltage	-0.5 to +7.0	V
$V_{IN}$	DC Input Voltage	-0.5 to +7.0	V
$V_{OUT}$	DC Output Voltage Active Mode (High or Low State) Tristate Mode (Output at Hi-Z) Power Down Mode ( $V_{CC} = 0$ V)	-0.5 to $V_{CC} + 0.5$ -0.5 to +7.0 -0.5 to +7.0	V
$I_{IK}$	DC Input Diode Current $V_{IN} < GND$	-50	mA
$I_{OK}$	DC Output Diode Current $V_{OUT} < GND$	-50	mA
$I_O$	DC Output Source/Sink Current	$\pm 50$	mA
$I_{CC}$	DC Supply Current Per Supply Pin	$\pm 100$	mA
$I_{GND}$	DC Ground Current per Ground Pin	$\pm 100$	mA
$T_{STG}$	Storage Temperature Range	-65 to +150	$^{\circ}C$
$T_L$	Lead Temperature, 1 mm from Case for 10 Seconds	260	$^{\circ}C$
$T_J$	Junction Temperature Under Bias	150	$^{\circ}C$
MSL	Moisture Sensitivity	Level 1	
$F_R$	Flammability Rating Oxygen Index: 28 to 34	UL 94 V-0 @ 0.125 in	
$V_{ESD}$	ESD Withstand Voltage Human Body Model (Note 2) Machine Model (Note 3) Charged Device Model (Note 4)	> 2000 > 200 N/A	V
$I_{LATCHUP}$	Latchup Performance Above $V_{CC}$ and Below GND at 125 $^{\circ}C$ (Note 5)	$\pm 500$	mA

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Measured with minimum pad spacing on an FR4 board, using 10 mm-by-1 inch, 2 ounce copper trace no air flow.
2. Tested to EIA / JESD22-A114-A.
3. Tested to EIA / JESD22-A115-A.
4. Tested to JESD22-C101-A.
5. Tested to EIA / JESD78.

## RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
$V_{CC}$	Positive DC Supply Voltage	1.65	5.5	V
$V_{IN}$	Digital Input Voltage	0	5.5	V
$V_{OUT}$	Output Voltage Active Mode (High or Low State) Tristate Mode (Output at Hi-Z) Power Down Mode ( $V_{CC} = 0$ V)	0 0 0	$V_{CC}$ 5.5 5.5	V
$T_A$	Operating Free-Air Temperature	-55	+125	$^{\circ}C$
$\Delta t / \Delta V$	Input Transition Rise or Fall Rate $V_{CC} = 2.5$ V $\pm$ 0.2 V $V_{CC} = 3.3$ V $\pm$ 0.3 V $V_{CC} = 5.0$ V $\pm$ 0.5 V	0 0 0	No Limit No Limit No Limit	nS/V

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

# NLX1G99

## DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Conditions	V <sub>CC</sub> (V)	T <sub>A</sub> = 25°C		T <sub>A</sub> ≤ +85°C		T <sub>A</sub> = -55°C to +125°C		Unit
				Min	Max	Min	Max	Min	Max	
V <sub>T+</sub>	Positive Threshold Voltage		1.65	0.79	1.16		1.16		1.16	V
			1.8	0.87	1.28		1.28		1.28	
			2.3	1.11	1.56		1.56		1.56	
			3.0	1.5	1.87		1.87		1.87	
			4.5	2.16	2.74		2.74		2.74	
5.5	2.61	3.33		3.33		3.33				
V <sub>T-</sub>	Negative Threshold Voltage		1.65	0.35	0.62	0.35		0.35		V
			1.8	0.38	0.68	0.38		0.38		
			2.3	0.58	0.87	0.58		0.58		
			3.0	0.84	1.19	0.84		0.84		
			4.5	1.41	1.9	1.41		1.41		
5.5	1.78	2.29	1.78		1.78					
V <sub>H</sub>	Hysteresis Voltage		1.65	0.30	0.62	0.30	0.62	0.30	0.62	V
			1.8	0.33	0.68	0.33	0.68	0.33	0.68	
			2.3	0.40	0.8	0.40	0.8	0.40	0.8	
			3.0	0.53	0.87	0.53	0.87	0.53	0.87	
			4.5	0.71	1.04	0.71	1.04	0.71	1.04	
5.5	0.8	1.2	0.8	1.2	0.8	1.2				
V <sub>OH</sub>	Minimum High-Level Output Voltage	V <sub>IN</sub> = V <sub>T-MIN</sub> or V <sub>T+MAX</sub> I <sub>OH</sub> = -50 μA I <sub>OH</sub> = -100 μA	1.65-5.5 1.65-5.5	V <sub>CC</sub> -0.1 V <sub>CC</sub> -0.1		V <sub>CC</sub> -0.1 V <sub>CC</sub> -0.1		V <sub>CC</sub> -0.1 V <sub>CC</sub> -0.1		V
		V <sub>IN</sub> = V <sub>T-MIN</sub> or V <sub>T+MAX</sub> I <sub>OH</sub> = -4 mA I <sub>OH</sub> = -8 mA I <sub>OH</sub> = -12 mA I <sub>OH</sub> = -16 mA I <sub>OH</sub> = -24 mA I <sub>OH</sub> = -32 mA	1.65 2.3 2.7 3.0 3.0 4.5	1.2 1.9 2.2 2.4 2.3 3.8		1.2 1.9 2.2 2.4 2.3 3.8		1.2 1.9 2.2 2.4 2.3 3.8		V
V <sub>OL</sub>	Maximum Low-Level Output Voltage	V <sub>IN</sub> = V <sub>T-MIN</sub> or V <sub>T+MAX</sub> I <sub>OL</sub> = 50 μA I <sub>OL</sub> = 100 μA	1.65-5.5 1.65-5.5		0.1 0.1		0.1 0.1		0.1 0.1	V
		V <sub>IN</sub> = V <sub>T-MIN</sub> or V <sub>T+MAX</sub> I <sub>OL</sub> = 4 mA I <sub>OL</sub> = 8 mA I <sub>OL</sub> = 12 mA I <sub>OL</sub> = 16 mA I <sub>OL</sub> = 24 mA I <sub>OL</sub> = 32 mA	1.65 2.3 2.7 3.0 3.0 4.5		0.45 0.3 0.4 0.4 0.55 0.55		0.45 0.3 0.4 0.4 0.55 0.55		0.45 0.3 0.4 0.4 0.55 0.55	
I <sub>IN</sub>	Input Leakage Current	0 ≤ V <sub>IN</sub> ≤ 5.5 V	0 - 5.5		±0.1		±1.0		±1.0	μA
I <sub>off</sub>	Power off Leakage Current	V <sub>IN</sub> or V <sub>O</sub> = 5.5 V	0		±1.0		±10		±10	μA
I <sub>OZ</sub>	Tri-state Output Leakage Current	V <sub>O</sub> = V <sub>CC</sub> or GND	1.65-5.5		±1.0		±10		±10	μA
I <sub>CC</sub>	Quiescent Supply Current	V <sub>IN</sub> = V <sub>CC</sub> or GND, I <sub>O</sub> = 0	1.65-5.5		1.0		10		10	μA
ΔI <sub>CC</sub>	Increase in I <sub>CC</sub> Per Input	One input at (V <sub>CC</sub> -0.6) V, other inputs at V <sub>CC</sub> or GND	2.3 - 5.5		10		100		100	μA

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.



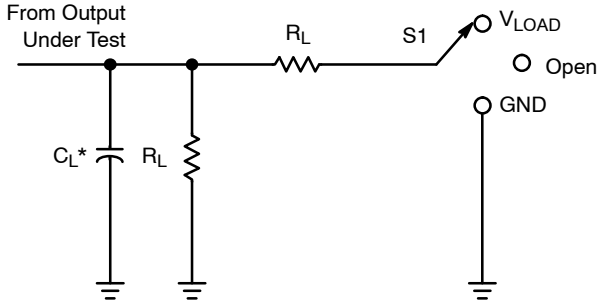
# NLX1G99

## AC ELECTRICAL CHARACTERISTICS (Input $t_r = t_f = 3.0$ ns)

Symbol	Parameter	V <sub>CC</sub> (V)	Test Condition	T <sub>A</sub> = 25°C			T <sub>A</sub> ≤ +85°C		T <sub>A</sub> = -55°C to +125°C		Unit
				Min	Typ	Max	Min	Max	Min	Max	
t <sub>PLH</sub> , t <sub>PHL</sub>	Propagation Delay, Any Input to Output Y (See Test Circuit)	1.65–1.95 2.3 – 2.7 3.0 – 3.6 4.5 – 5.5	Refer to switch positions and loading conditions in Figure 17 to 21.	4.3	12.8	25.1	4.3	25.1	4.3	25.1	ns
				2.4	7.1	10.2	2.4	10.2	2.4	10.2	
				1.7	5.2	6.7	1.7	6.9	1.7	7.0	
				1.3	4.0	4.5	1.3	4.9	1.3	5.0	
t <sub>EN</sub>	Output Enable Time, OE to Y	1.65–1.95 2.3 – 2.7 3.0 – 3.6 4.5 – 5.5	Refer to switch positions and loading conditions in Figure 17 to 21.	3.4		24.7	3.4	24.7	3.4	24.7	ns
				2.1		11	2.1	12	2.1	12.2	
				1.3		7.5	1.3	8.0	1.3	8.3	
				1.0		5.7	1.0	6.2	1.0	6.5	
t <sub>DIS</sub>	Output Disable Time, OE to Y	1.65–1.95 2.3 – 2.7 3.0 – 3.6 4.5 – 5.5	Refer to switch positions and loading conditions in Figure 17 to 21.	4.0		15.5	4.0	15.5	4.0	15.5	ns
				2.7		7.5	2.7	7.5	2.7	7.5	
				3.5		7.0	3.5	7.0	3.5	7.0	
				2.0		5.5	2.0	5.5	2.0	5.5	
t <sub>PLH</sub> , t <sub>PHL</sub>	Propagation Delay, Any Input to Output Y (See Test Circuit)	1.65–1.95 2.3 – 2.7 3.0 – 3.6 4.5 – 5.5	Refer to switch Positions and loading conditions in Figure 22 to 26.	4.3	13.6	25.7	4.3	25.7	4.3	25.7	ns
				2.5	7.8	10.7	2.5	10.7	2.5	10.7	
				2.3	5.6	7.6	2.3	7.6	2.3	7.6	
				1.6	4.4	5.2	1.6	5.2	1.6	5.2	
t <sub>EN</sub>	Output Enable Time, OE to Y	1.65–1.95 2.3 – 2.7 3.0 – 3.6 4.5 – 5.5	Refer to switch Positions and loading conditions in Figure 22 to 26.	4.2		25.2	4.2	25.2	4.2	25.2	ns
				2.4		11.3	2.4	12.2	2.4	13	
				2.0		8.0	2.0	8.5	2.0	8.7	
				1.7		6.0	1.7	6.5	1.7	6.7	
t <sub>DIS</sub>	Output Disable Time, OE to Y	1.65–1.95 2.3 – 2.7 3.0 – 3.6 4.5 – 5.5	Refer to switch Positions and loading conditions in Figure 22 to 26.	3.7		15	3.7	15	3.7	15	ns
				2.0		6.5	2.0	6.7	2.0	6.9	
				2.1		5.6	2.1	5.8	2.1	5.9	
				1.0		4.5	1.0	4.7	1.0	4.9	
C <sub>IN</sub>	Input Capacitance	3.3			3.5					pF	
C <sub>O</sub>	Output Capacitance	3.3			6.0					pF	
C <sub>PD</sub>	Power Dissipation Capacitance (Note 6)	3.3	f = 10 MHz		22					pF	

6. C<sub>PD</sub> is defined as the value of the internal equivalent capacitance which is calculated from the dynamic operating current consumption without load. Average operating current can be obtained by the equation  $I_{CC(OPR)} = C_{PD} \cdot V_{CC} \cdot f_{in} + I_{CC}$ . C<sub>PD</sub> is used to determine the no-load dynamic power consumption:  $P_D = C_{PD} \cdot V_{CC}^2 \cdot f_{in} + I_{CC} \cdot V_{CC}$ .

TEST CIRCUIT AND VOLTAGE WAVEFORMS



Test	S1
$t_{PLH}/t_{PHL}$	Open
$t_{PLZ}/t_{PZL}$	$V_{LOAD}$
$t_{PHZ}/t_{PZH}$	GND

\* $C_L$  includes probes and jig capacitance.

Figure 17. Load Circuit

$V_{CC}$	Inputs		$V_M$	$V_{LOAD}$	$C_L$	$R_L$	$V_{\Delta}$
	$V_I$	$t_r/t_f$					
$1.8\text{ V} \pm 0.15\text{ V}$	$V_{CC}$	$\leq 2\text{ ns}$	$V_{CC}/2$	$2 \times V_{CC}$	15 pF	1 M $\Omega$	0.15 V
$2.5\text{ V} \pm 0.2\text{ V}$	$V_{CC}$	$\leq 2\text{ ns}$	$V_{CC}/2$	$2 \times V_{CC}$	15 pF	1 M $\Omega$	0.15 V
$3.3\text{ V} \pm 0.3\text{ V}$	3 V	$\leq 2.5\text{ ns}$	1.5 V	6 V	15 pF	1 M $\Omega$	0.3 V
$5.5\text{ V} \pm 0.5\text{ V}$	$V_{CC}$	$\leq 2.5\text{ ns}$	$V_{CC}/2$	$2 \times V_{CC}$	15 pF	1 M $\Omega$	0.3 V

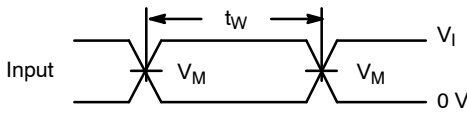


Figure 18. Voltage Waveforms Pulse Duration

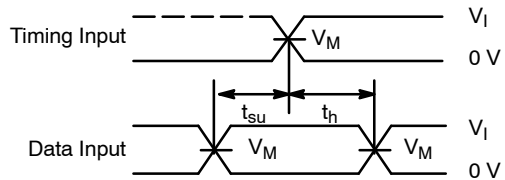


Figure 19. Voltage Waveforms Setup and Hold Times

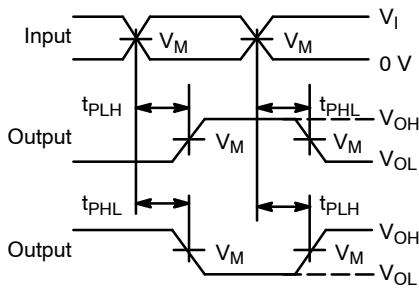


Figure 20. Voltage Waveforms Propagation Delay Times Inverting and Noninverting Outputs

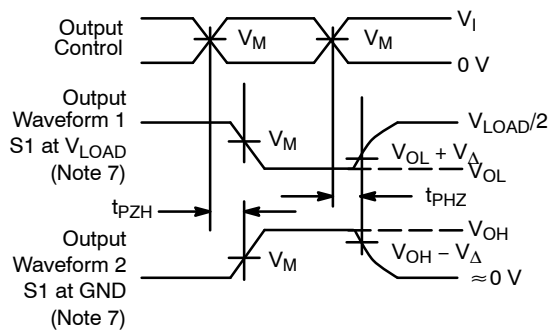
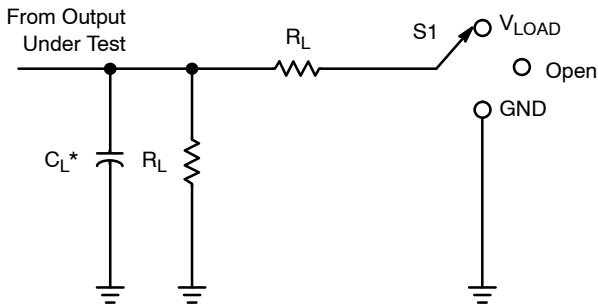


Figure 21. Voltage Waveforms Enable and Disable Times Low- and High-Level Enabling

- Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control
- All input pulses are supplied by generators having the following characteristics:  $PRR \leq 10\text{ MHz}$ ,  $Z_0 = 50\ \Omega$ .
- The outputs are measured one at a time, with one transition per measurement.
- All parameters are waveforms are not applicable to all devices.

# NLX1G99

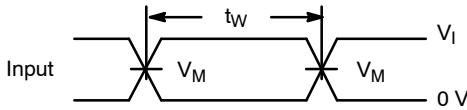


\* $C_L$  includes probes and jig capacitance.

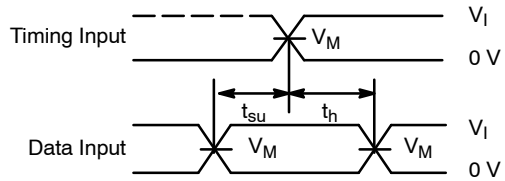
**Figure 22. Load Circuit**

Test	S1
$t_{PLH}/t_{PHL}$	Open
$t_{PLZ}/t_{PZL}$	$V_{LOAD}$
$t_{PHZ}/t_{PZH}$	GND

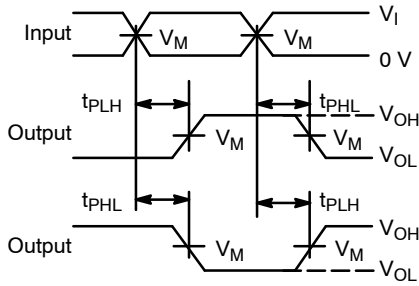
$V_{CC}$	Inputs		$V_M$	$V_{LOAD}$	$C_L$	$R_L$	$V_{\Delta}$
	$V_I$	$t_r/t_f$					
$1.8\text{ V} \pm 0.15\text{ V}$	$V_{CC}$	$\leq 2\text{ ns}$	$V_{CC}/2$	$2 \times V_{CC}$	30 pF	1 k $\Omega$	0.15 V
$2.5\text{ V} \pm 0.2\text{ V}$	$V_{CC}$	$\leq 2\text{ ns}$	$V_{CC}/2$	$2 \times V_{CC}$	30 pF	500 $\Omega$	0.15 V
$3.3\text{ V} \pm 0.3\text{ V}$	3 V	$\leq 2.5\text{ ns}$	1.5 V	6 V	50 pF	500 $\Omega$	0.3 V
$5.5\text{ V} \pm 0.5\text{ V}$	$V_{CC}$	$\leq 2.5\text{ ns}$	$V_{CC}/2$	$2 \times V_{CC}$	50 pF	500 $\Omega$	0.3 V



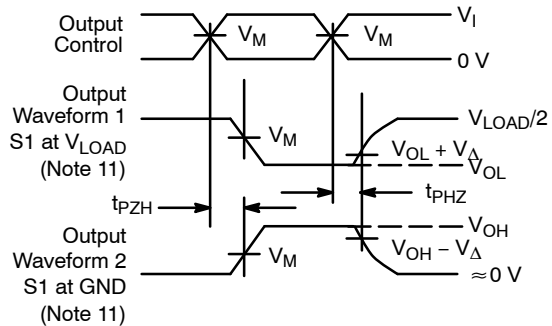
**Figure 23. Voltage Waveforms Pulse Duration**



**Figure 24. Voltage Waveforms Setup and Hold Times**



**Figure 25. Voltage Waveforms Propagation Delay Times Inverting and Noninverting Outputs**



**Figure 26. Voltage Waveforms Enable and Disable Times Low- and High-Level Enabling**

- Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
- All input pulses are supplied by generators having the following characteristics:  $PRR \leq 10\text{ MHz}$ ,  $Z_O = 50\ \Omega$ .
- The outputs are measured one at a time, with one transition per measurement.
- All parameters are waveforms are not applicable to all devices.

# NLX1G99

## ORDERING INFORMATION

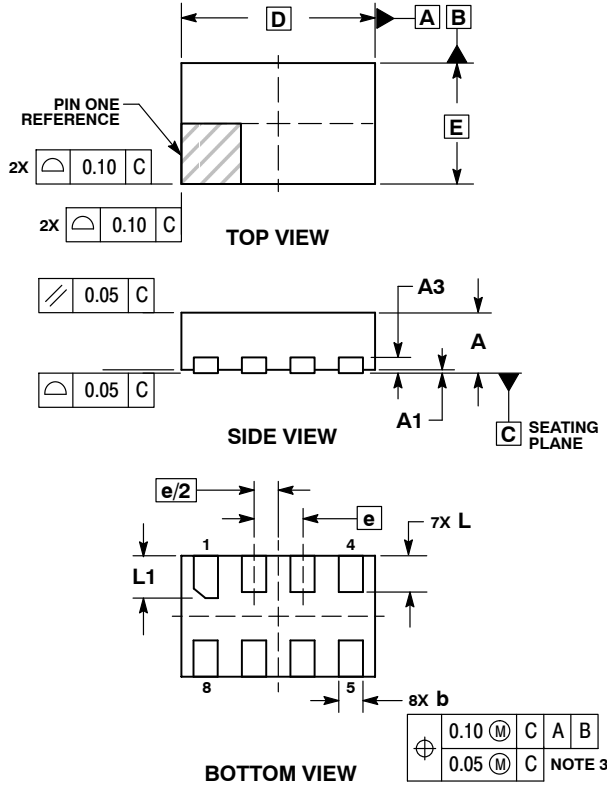
Device	Package	Shipping†
NLX1G99AMX1TCG	ULLGA8 – 0.5P (Pb-Free)	3000 / Tape & Reel
NLX1G99BMX1TCG	ULLGA8 – 0.4P (Pb-Free)	3000 / Tape & Reel
NLX1G99CMX1TCG	ULLGA8 – 0.35P (Pb-Free)	3000 / Tape & Reel
NLX1G99DMUTCG	UDFN8, 1.95 x 1.0, 0.5P (Pb-Free)	3000 / Tape & Reel
NLX1G99EMUTCG In Development	UDFN8, 1.6 x 1.0, 0.4P (Pb-Free)	3000 / Tape & Reel
NLX1G99FMUTCG In Development	UDFN8, 1.45 x 1.0, 0.35P (Pb-Free)	3000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

# NLX1G99

## PACKAGE DIMENSIONS

UDFN8 1.6x1.0, 0.4P  
CASE 517BY  
ISSUE O

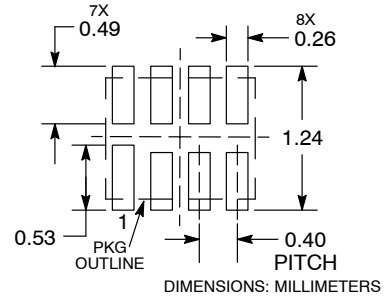


**NOTES:**

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.20 MM FROM TERMINAL TIP.
4. PACKAGE DIMENSIONS EXCLUSIVE OF BURRS AND MOLD FLASH.

DIM	MILLIMETERS	
	MIN	MAX
A	0.45	0.55
A1	0.00	0.05
A3	0.13	REF
b	0.15	0.25
D	1.60	BSC
E	1.00	BSC
e	0.40	BSC
L	0.25	0.35
L1	0.30	0.40

**RECOMMENDED SOLDERING FOOTPRINT\***

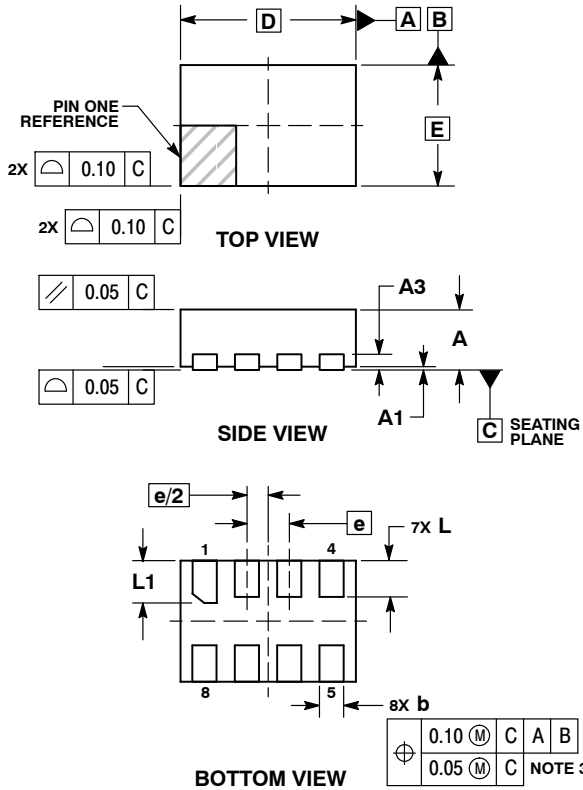


\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

# NLX1G99

## PACKAGE DIMENSIONS

UDFN8 1.45x1.0, 0.35P  
CASE 517BZ  
ISSUE O

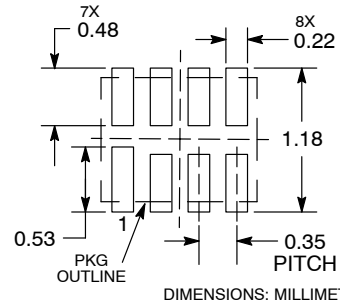


**NOTES:**

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.20 MM FROM TERMINAL TIP.
4. PACKAGE DIMENSIONS EXCLUSIVE OF BURRS AND MOLD FLASH.

DIM	MILLIMETERS	
	MIN	MAX
A	0.45	0.55
A1	0.00	0.05
A3	0.13	REF
b	0.15	0.25
D	1.45	BSC
E	1.00	BSC
e	0.35	BSC
L	0.25	0.35
L1	0.30	0.40

**RECOMMENDED SOLDERING FOOTPRINT\***

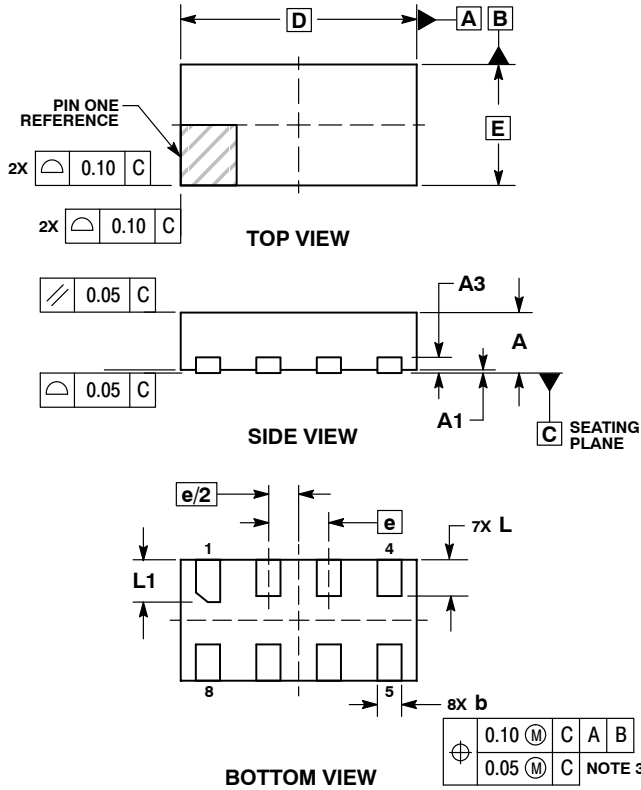


\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

# NLX1G99

## PACKAGE DIMENSIONS

UDFN8 1.95x1.0, 0.5P  
CASE 517CA  
ISSUE O

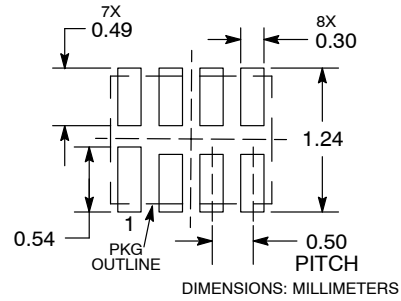


**NOTES:**

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.20 MM FROM TERMINAL TIP.
4. PACKAGE DIMENSIONS EXCLUSIVE OF BURRS AND MOLD FLASH.

MILLIMETERS		
DIM	MIN	MAX
A	0.45	0.55
A1	0.00	0.05
A3	0.13 REF	
b	0.15	0.25
D	1.95 BSC	
E	1.00 BSC	
e	0.50 BSC	
L	0.25	0.35
L1	0.30	0.40

**RECOMMENDED SOLDERING FOOTPRINT\***



\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

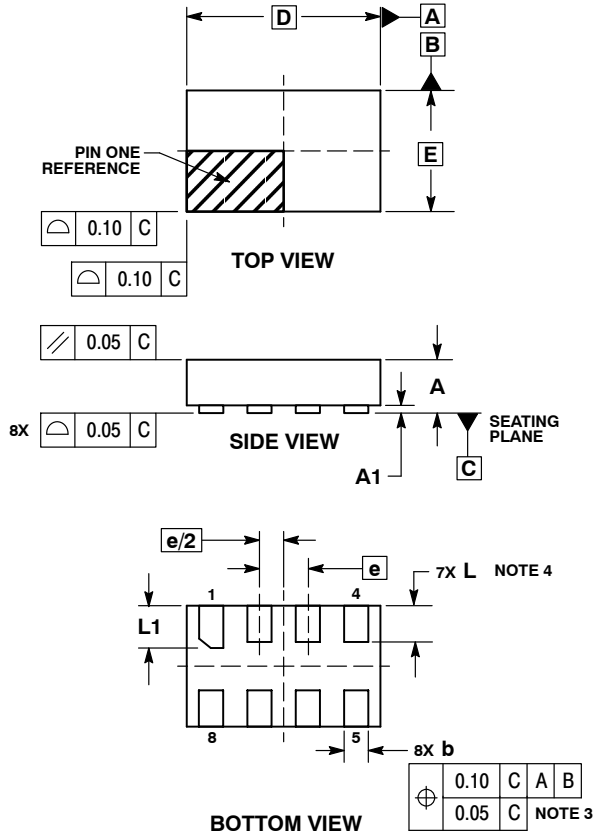




# NLX1G99

## PACKAGE DIMENSIONS

ULLGA8 1.6x1.0, 0.4P  
CASE 613AB  
ISSUE A

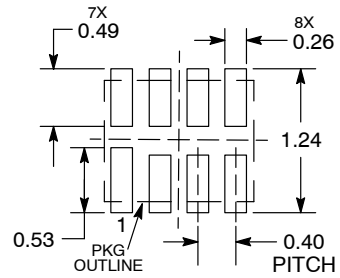


**NOTES:**

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30 mm FROM THE TERMINAL TIP.
4. A MAXIMUM OF 0.05 PULL BACK OF THE PLATED TERMINAL FROM THE EDGE OF THE PACKAGE IS ALLOWED.

DIM	MILLIMETERS	
	MIN	MAX
A	---	0.40
A1	0.00	0.05
b	0.15	0.25
D	1.60 BSC	
E	1.00 BSC	
e	0.40 BSC	
L	0.25	0.35
L1	0.30	0.40

**MOUNTING FOOTPRINT  
SOLDERMASK DEFINED\***



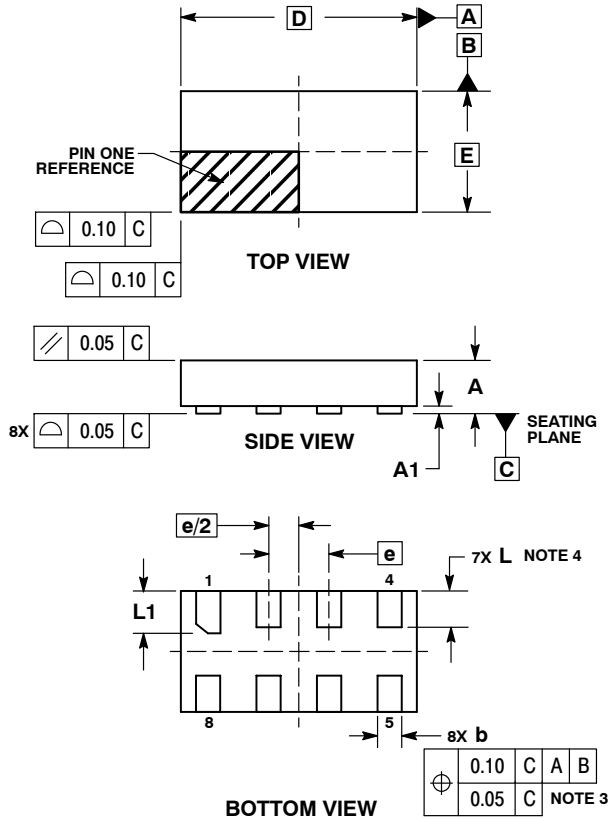
DIMENSIONS: MILLIMETERS

\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

# NLX1G99

## PACKAGE DIMENSIONS

ULLGA8 1.95x1.0, 0.5P  
CASE 613AC  
ISSUE A

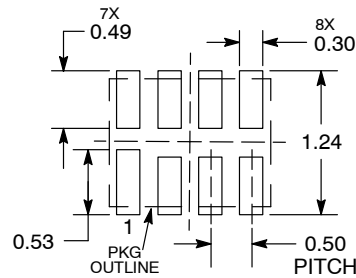


### NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30 mm FROM THE TERMINAL TIP.
4. A MAXIMUM OF 0.05 PULL BACK OF THE PLATED TERMINAL FROM THE EDGE OF THE PACKAGE IS ALLOWED.

DIM	MILLIMETERS	
	MIN	MAX
A	---	0.40
A1	0.00	0.05
b	0.15	0.25
D	1.95 BSC	
E	1.00 BSC	
e	0.50 BSC	
L	0.25	0.35
L1	0.30	0.40

### MOUNTING FOOTPRINT SOLDERMASK DEFINED\*



DIMENSIONS: MILLIMETERS

\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

MiniGate is a trademark of Semiconductor Components Industries, LLC (SCILLC).

ON Semiconductor and are registered trademarks of Semiconductor Components Industries, LLC (SCILLC). SCILLC owns the rights to a number of patents, trademarks, copyrights, trade secrets, and other intellectual property. A listing of SCILLC's product/patent coverage may be accessed at [www.onsemi.com/site/pdf/Patent-Marking.pdf](http://www.onsemi.com/site/pdf/Patent-Marking.pdf). SCILLC reserves the right to make changes without further notice to any products herein. SCILLC makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does SCILLC assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. "Typical" parameters which may be provided in SCILLC data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. SCILLC does not convey any license under its patent rights nor the rights of others. SCILLC products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the SCILLC product could create a situation where personal injury or death may occur. Should Buyer purchase or use SCILLC products for any such unintended or unauthorized application, Buyer shall indemnify and hold SCILLC and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that SCILLC was negligent regarding the design or manufacture of the part. SCILLC is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

### PUBLICATION ORDERING INFORMATION

**LITERATURE FULFILLMENT:**  
Literature Distribution Center for ON Semiconductor  
P.O. Box 5163, Denver, Colorado 80217 USA  
Phone: 303-675-2175 or 800-344-3860 Toll Free USA/Canada  
Fax: 303-675-2176 or 800-344-3867 Toll Free USA/Canada  
Email: [orderlit@onsemi.com](mailto:orderlit@onsemi.com)

**N. American Technical Support:** 800-282-9855 Toll Free  
USA/Canada  
**Europe, Middle East and Africa Technical Support:**  
Phone: 421 33 790 2910  
**Japan Customer Focus Center**  
Phone: 81-3-5817-1050

**ON Semiconductor Website:** [www.onsemi.com](http://www.onsemi.com)  
**Order Literature:** <http://www.onsemi.com/orderlit>

For additional information, please contact your local Sales Representative

## X-ON Electronics

Largest Supplier of Electrical and Electronic Components

*Click to view similar products for [Logic Gates](#) category:*

*Click to view products by [ON Semiconductor](#) manufacturer:*

Other Similar products are found below :

[5962-8769901BCA](#) [74HC85N](#) [NL17SG08P5T5G](#) [NL17SG32DFT2G](#) [NLU1G32AMUTCG](#) [NLV7SZ58DFT2G](#) [NLVHC1G08DFT1G](#)  
[NLVVHC1G14DTT1G](#) [NLX2G08DMUTCG](#) [NLX2G08MUTCG](#) [MC74HCT20ADR2G](#) [091992B](#) [091993X](#) [093560G](#) [634701C](#) [634921A](#)  
[NL17SG32P5T5G](#) [NL17SG86DFT2G](#) [NLU1G32CMUTCG](#) [NLV14001UBDR2G](#) [NLVVHC1G132DTT1G](#) [NLVVHC1G86DTT1G](#)  
[NLX1G11AMUTCG](#) [NLX1G97MUTCG](#) [746427X](#) [74AUP1G17FW5-7](#) [74LS38](#) [74LVC1G08Z-7](#) [74LVC32ADTR2G](#) [74LVC1G125FW4-7](#)  
[74LVC08ADTR2G](#) [MC74HCT20ADTR2G](#) [NLU1G08CMX1TCG](#) [NLV14093BDTR2G](#) [NLV17SZ00DFT2G](#) [NLV17SZ02DFT2G](#)  
[NLV17SZ126DFT2G](#) [NLV27WZ17DFT2G](#) [NLV74HC02ADR2G](#) [NLV74HC08ADR2G](#) [NLVVHC1GT32DFT1G](#) [74HC32S14-13](#) [74LS133](#)  
[74LVC1G32Z-7](#) [M38510/30402BDA](#) [74LVC1G86Z-7](#) [74LVC2G08RA3-7](#) [M38510/06202BFA](#) [NLV74HC08ADTR2G](#)  
[NLV74HC14ADR2G](#)