



GS2994 Adaptive Cable Equalizer

Key Features

- SMPTE 424M, SMPTE 292M and SMPTE 259M compliant
- Automatic cable equalization
- Multi-standard operation from 143Mb/s to 2.97Gb/s
- Performance optimized for 270Mb/s, 1.485Gb/s and 2.97Gb/s. Typical equalized length of Belden 1694A cable:
 - ♦ 140m at 2.97Gb/s
 - ♦ 220m at 1.485Gb/s
 - ♦ 400m at 270Mb/s
- Supports DVB-ASI at 270Mb/s
- Manual bypass (useful for low data rates with slow rise/fall times)
- Programmable carrier detect with squelch threshold adjustment
- Automatic power-down on loss of signal
 - ♦ Standby power <30mW (typical)
- Differential outputs support DC-coupling to 1.2V, 2.5V and 3.3V CML logic
- 0/6 dB gain boost selection pin
- Selectable de-emphasis: 2dB, 4dB and 6dB
- Standard EIA/JEDEC logic control and status signal levels
- Single 3.3V power supply operation
- 167mW power consumption (typical)
- Wide operating temperature range of -40°C to +85°C
- Small footprint QFN package (4mm x 4mm)
 - ♦ Footprint compatible with the GS2974 and the GS2984
- Pb-free and RoHS compliant

Applications

- SMPTE 424M, SMPTE 292M and SMPTE 259M coaxial cable serial digital interfaces

Description

The GS2994 is a high-speed BiCMOS integrated circuit designed to equalize and restore signals received over 75Ω coaxial cable.

The device is designed to support SMPTE 424M, SMPTE292M and SMPTE 259M, and is optimized for performance at 270Mb/s, 1.485Gb/s and 2.97Gb/s.

The GS2994 features DC restoration to compensate for the DC content of SMPTE pathological test patterns.

The Carrier Detect output pin (\overline{CD}) indicates whether a valid input signal has been detected. It can be connected directly to the SLEEP pin to enable automatic power-down upon loss of carrier. In the manual sleep mode, a voltage programmable threshold, which can be changed via the SQ_ADJ pin, forces \overline{CD} high when the input signal amplitude falls below the threshold. This allows the GS2994 to distinguish between low-amplitude SDI signals and noise at the input of the device.

The equalizing and DC restore stages are disengaged when the BYPASS pin is HIGH. No equalization occurs in Bypass mode.

The GS2994 includes a gain selection pin (GAIN_SEL) which, when tied HIGH, compensates for 6dB flat attenuation.

The differential outputs can be DC-coupled to Gennum 3.3V cable drivers and reclockers and to industry-standard 1.2V, 2.5V and 3.3V CML logic using the VCC_O pin. In general, DC-coupling to any termination voltage between 1.2V and 3.3V is supported.

The GS2994 also includes programmable de-emphasis with three operating levels in order to support long PCB traces.

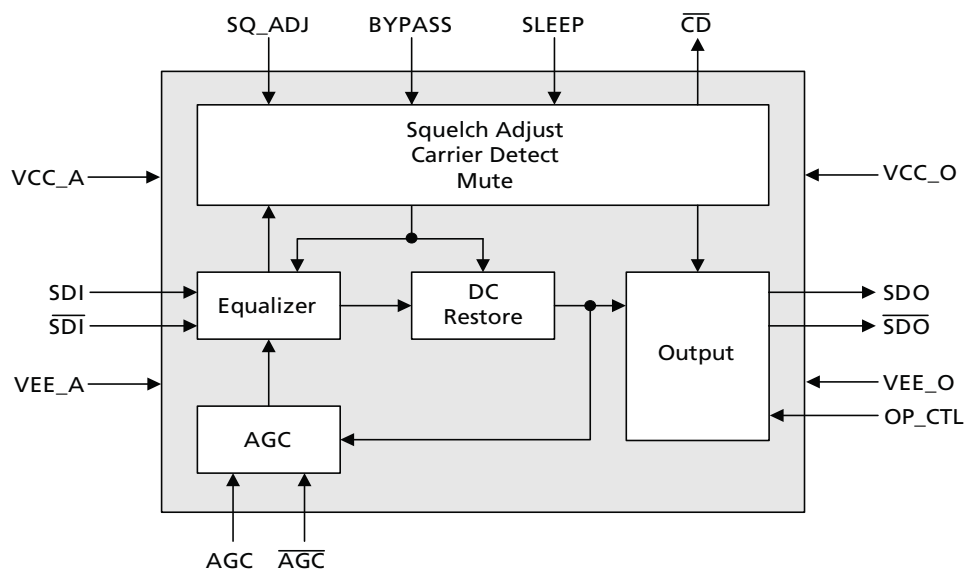
The GS2994 is footprint and drop-in compatible with existing GS2974 and GS2984 designs.

The device is available in a 16-pin, 4mm x 4mm QFN package.

Power consumption of the GS2994 is typically 167mW when DC-coupled at 1.2V.

The GS2994 is Pb-free, and the encapsulation compound does not contain halogenated flame retardant.

This component and all homogeneous subcomponents are RoHS compliant.



GS2994 Functional Block Diagram

Revision History

Version	ECR	PCN	Date	Changes and/or Modifications
4	158405	-	August 2012	Updates in GS2994 Pin Descriptions , Table 2-1: DC Electrical Characteristics , and Input/Output Circuits .
3	157635	-	February 2012	Added pull-down resistor to Figure 3-4 . Updated the descriptions for the BYPASS and SLEEP pins in Table 1-1 . Clarification to column headings in Table 4-1 .
2	157164	-	November 2011	Updated the descriptions for the GAIN_SEL and SQ_ADJ pins in Table 1-1 to indicate that they have internal pull-down resistors.
1	155124	-	October 2010	Converted to Data Sheet. Increased cable length to 220m at 1.485Gb/s.
0	154492	-	June 2010	Converted to Preliminary Data Sheet. Updated the power and current consumption values in Table 2-1: DC Electrical Characteristics .
B	153758	-	March 2010	Removed the 470nF capacitor (between \overline{AGC} and GND) from Figure 5-1: GS2994 Typical Application Circuit .
A	153233	-	January 2010	New document.

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1. Pin Out

1.1 GS2994 Pin Assignment

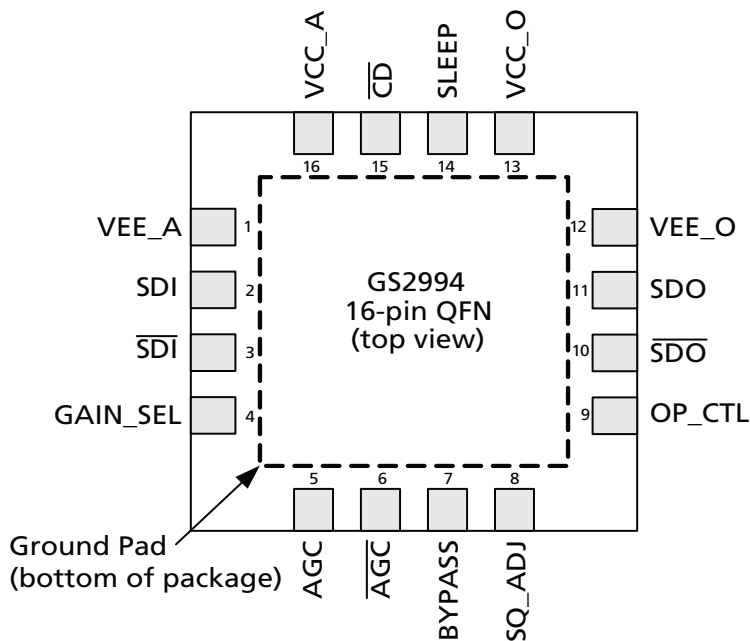


Figure 1-1: GS2994 Pin Out

1.2 GS2994 Pin Descriptions

Table 1-1: GS2994 Pin Descriptions

Pin Number	Name	Timing	Type	Description
1	VEE_A	Analog	Power	Most negative power supply connection for the input buffer, core and control circuits. Connect to GND.
2, 3	SDI, $\overline{\text{SDI}}$	Analog	Input	Serial digital differential input.
4	GAIN_SEL	Not Synchronous	Input	Input Sensitivity Control. When LOW the sensitivity is 800mV. When HIGH the sensitivity is 400mV. Includes an internal pull-down resistor.
5, 6	AGC, $\overline{\text{AGC}}$	Analog	–	External AGC capacitor. Connect pin 5 and pin 6 as shown in the Typical Application Circuit on page 16 .
7	BYPASS	Not Synchronous	Input	Core Bypass control signal input. Forces the Equalizing and DC RESTORE stages into bypass mode when HIGH. No equalization occurs in this mode. Includes an internal pull-down resistor.

Table 1-1: GS2994 Pin Descriptions (Continued)

Pin Number	Name	Timing	Type	Description
8	SQ_ADJ	Analog	Input	<p>Squelch Threshold Adjust.</p> <p>Adjusts the input signal amplitude threshold of the carrier detect function. The output can be muted when the input signal amplitude is too low by connecting the \overline{CD} and OP_CTL pins together through some external components. In this case, when \overline{CD} is LOW (0V), OP_CTL is forced LOW (0V), and when \overline{CD} is HIGH (2.5V), OP_CTL is forced HIGH (3.3V). The input level at which the part is muted can be set through the SQ_ADJ pin through suitable voltage variances as described in Section 4.4. NOTE: when the SQ_ADJ functionality is used and/or in auto_mute, the auto sleep feature is not allowed, and the SLEEP pin should be left open.</p> <p>Includes an internal pull-down resistor.</p>
9	OP_CTL	Not Synchronous	Input	<p>CONTROL SIGNAL INPUT</p> <p>Controls the Output Swing, De-emphasis, and Mute features of the SDO and \overline{SDO} outputs.</p> <p>When connected to GND, the output swing is 800mV with no de-emphasis. When connected to the 3.3V analog power supply, the output is MUTED.</p> <p>Includes an internal pull down resistor.</p> <p>See Section 4.7 for all other control options.</p>
10, 11	\overline{SDO} , SDO	Analog	Output	Equalized serial digital differential output.
12	VEE_O	Analog	Power	Most negative power supply for the output buffer. Connect to GND.
13	VCC_O	Analog	Power	Most positive power supply connection for the output buffer of the device. Connect to +1.2V ~ +3.3V DC.
14	SLEEP	Not Synchronous	Input	<p>CONTROL SIGNAL INPUT</p> <p>When set HIGH, the GS2994 is powered-down except for the Carrier Detect functionality.</p> <p>Includes an internal pull-down resistor.</p>
15	\overline{CD}	Not Synchronous	Output	<p>Carrier Detect status signal output.</p> <p>Signal levels are LVCMOS/LVTTL compatible.</p> <p>Indicates the presence of an input signal. When the \overline{CD} pin is LOW, a good input signal has been detected. When this pin is HIGH, the input signal is invalid.</p> <p>See Section 4.5.</p>
16	VCC_A	Analog	Power	Most positive power supply for the input buffer, core and control circuits of the device. Connect to +3.3V DC.
–	Center Pad	–	Power	Internally bonded to VEE_A.

2. Electrical Characteristics

2.1 Absolute Maximum Ratings

Parameter	Value
Supply Voltage - Core	-0.5V to +3.6V DC
Supply Voltage - Output Driver	-0.5V to +3.6V DC
Input ESD Voltage (HBM)	5kV
Storage Temperature Range	-50°C < T _s < 125°C
Input Voltage Range (any input)	-0.3 to (V _{CC_A} +0.3)V
Operating Temperature Range	-40°C to +85°C
Solder Reflow Temperature	260°C

2.2 DC Electrical Characteristics

Table 2-1: DC Electrical Characteristics

V_{CC_A} = 3.3V ±5%, T_A = -40°C to +85°C, unless otherwise shown

Parameter	Symbol	Conditions	Min	Typ	Max	Units	Notes
Supply Voltage - Core	V _{CC_A}	–	3.135	3.3	3.465	V	–
Supply Voltage - Output Driver	V _{CC_O}	–	1.14	1.2	1.26	V	1
		–	2.375	2.5	2.625	V	1
		–	3.135	3.3	3.465	V	1
Power Consumption	P _D	T _A = 25°C V _{CC_O} = 1.2V ΔV _{SDO} = 400mV	–	167	–	mW	2
		T _A = 25°C V _{CC_O} = 1.2V ΔV _{SDO} = 800mV	–	179	–	mW	2
		T _A = 25°C V _{CC_O} = 3.3V ΔV _{SDO} = 400mV	–	191	–	mW	2
		T _A = 25°C V _{CC_O} = 3.3V ΔV _{SDO} = 800mV	–	223	–	mW	2

Table 2-1: DC Electrical Characteristics (Continued)

$V_{CC_A} = 3.3V \pm 5\%$, $T_A = -40^\circ C$ to $+85^\circ C$, unless otherwise shown

Parameter	Symbol	Conditions	Min	Typ	Max	Units	Notes
Supply Current - Core	I_s	$T_A = 25^\circ C$	–	48.7	–	mA	2, 3
Supply Current - Output Driver	$I_{Output\ Driver}$	$T_A = 25^\circ C$, $\Delta V_{SDO} = 800mV$	–	17.3	–	mA	2
		$T_A = 25^\circ C$, $\Delta V_{SDO} = 400mV$	–	9.3	–	mA	2
Input Common Mode Voltage	V_{CMIN}	$T_A = 25^\circ C$	–	1.8	–	V	–
SQ_ADJ DC Voltage (to mute signal)	–	0m, $T_A = 25^\circ C$	–	3.2	–	V	–
SQ_ADJ Range	–	$T_A = 25^\circ C$	–	0.9	–	V	–
CD Output Voltage	$V_{\overline{CD}(OH)}$	Carrier not present	2.0	–	–	V	–
	$V_{\overline{CD}(OL)}$	Carrier present	–	–	0.4	V	–
Sleep, GAIN_SEL, BYPASS, Input High Level Voltage	V_{IH}	–	1.7	–	–	V	4
Sleep, GAIN_SEL, BYPASS, Input Low Level Voltage	V_{IL}	–	–	–	0.7	V	4

NOTES:

1. V_{CC_O} operates from 1.2V through 3.3V (+/-5%).
2. De-emphasis off.
3. An additional 3mA when de-emphasis is enabled.
4. Digital pins are 2.5V, but 3.3V tolerant.

2.3 AC Electrical Characteristics

Table 2-2: AC Electrical Characteristics

$V_{CC_A} = 3.3V \pm 5\%$, $T_A = -40^\circ C$ to $+85^\circ C$, unless otherwise shown

Parameter	Symbol	Conditions	Min	Typ	Max	Units	Notes
Serial input data rate	DR_{SDO}	–	143	–	2970	Mb/s	–
Input Voltage Swing	ΔV_{SDI}	$T_A = 25^\circ C$, differential, 270Mb/s and 1.485Gb/s	720	800	950	mV _{p-p}	1
		$T_A = 25^\circ C$, differential, 2.97Gb/s	720	800	880	mV _{p-p}	1
Output Voltage Swing	ΔV_{SDO}	100 Ω load, $T_A = 25^\circ C$, differential, OP_CTL set for high swing	–	800	–	mV _{p-p}	–
		100 Ω load, $T_A = 25^\circ C$, differential, OP_CTL set for low swing	–	400	–	mV _{p-p}	–

Table 2-2: AC Electrical Characteristics (Continued) $V_{CC_A} = 3.3V \pm 5\%$, $T_A = -40^\circ C$ to $+85^\circ C$, unless otherwise shown

Parameter	Symbol	Conditions	Min	Typ	Max	Units	Notes
Output Jitter of Various Cable Lengths and Data Rates	-	2.97Gb/s Belden 1694A: 0-120m	-	-	0.25	UI	2, 5
	-	2.97Gb/s Belden 1694A: 120-140m	-	0.3	-	UI	3, 5
	-	1.485Gb/s Belden 1694A: 0-180m	-	-	0.25	UI	2, 5
	-	1.485Gb/s Belden 1694A: 180-220m	-	0.25	-	UI	3, 5
	-	270Mb/s Belden 1694A: 0-400m	-	-	0.2	UI	2, 5
Output Rise/Fall time	-	2.97Gb/s & 1.485Gb/s 20% - 80%	-	75	-	ps	-
	-	270Mb/s	-	150	-	ps	-
Mismatch in rise/fall time	-	-	-	-	30	ps	-
Duty cycle distortion	-	3G/HD	-	-	30	ps	-
	-	SD	-	-	55	ps	-
Overshoot	-	-	-	-	10	%	-
Input Return Loss	-	-	15	21	-	dB	4
Input Resistance	-	single-ended	-	1.9	-	k Ω	-
Input Capacitance	-	single-ended	-	1.3	-	pF	-
Output Resistance	-	single-ended	-	50	-	Ω	-

NOTES:

- 0m cable length.
- All parts are production tested. In order to guarantee jitter over the full range of specification ($V_{CC_A} = 3.3V \pm 5\%$, $T_A = -40^\circ C$ to $+85^\circ C$, and 720-880mV launch swing from the SDI cable driver) the recommended applications circuit must be used.
- Based on characterization data using the recommended applications circuit, at $V_{CC_A} = 3.3V$, $T_A = 25^\circ C$ and 800mV launch swing from the SDI cable driver.
- Tested on a GS2994 board from 5MHz to 3GHz.
- GAIN_SEL = 0

3. Input/Output Circuits

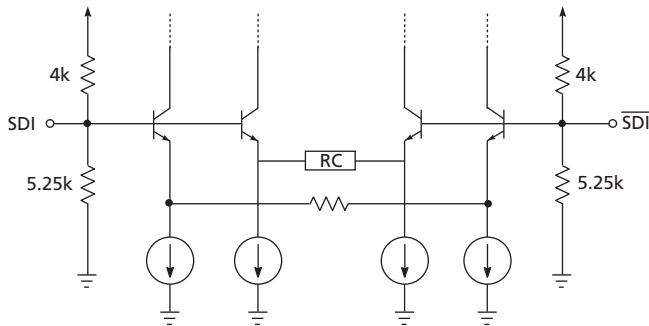


Figure 3-1: Input Equivalent Circuit

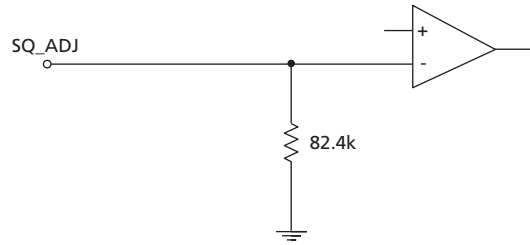


Figure 3-2: SQ_ADJ Equivalent Circuit

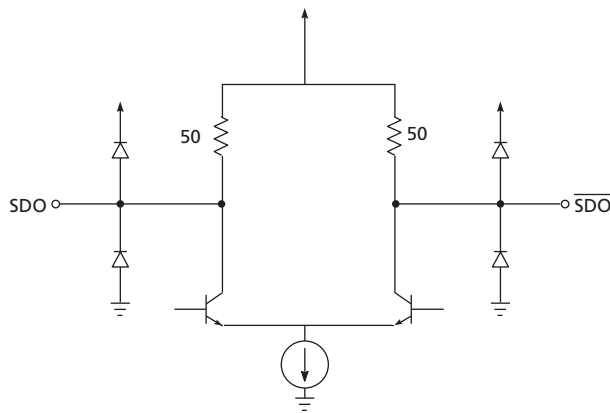


Figure 3-3: Output Circuit

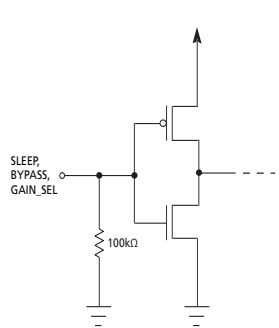


Figure 3-4: SLEEP, BYPASS and GAIN_SEL Circuits

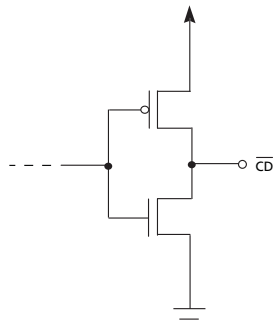


Figure 3-5: \overline{CD} Circuit

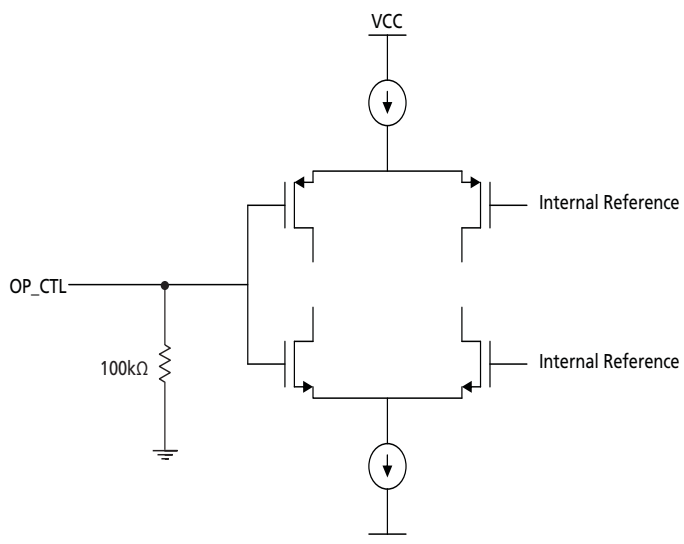


Figure 3-6: OP_CTL

4. Detailed Description

The GS2994 is a high-speed BiCMOS IC designed to equalize serial digital signals.

The GS2994 can equalize 3Gb/s, HD and SD serial digital signals, and will typically equalize 140m of Belden 1694A cable at 2.97Gb/s, 220m at 1.485Gb/s and 400m at 270Mb/s. The GS2994 can be powered from a single +3.3V power supply, and is footprint compatible with the GS2974 and GS2984 equalizers. When using 1.2V CML, the GS2994 typically consumes approximately 167mW of power.

4.1 Serial Data Inputs

The Serial Data signal can be connected to the input pins ($\overline{\text{SDI}}/\overline{\text{SDI}}$) in either a differential or single-ended configuration. AC-coupling of the inputs is recommended, as the SDI and $\overline{\text{SDI}}$ inputs are internally biased at approximately 1.8V.

4.2 Cable Equalization

The input signal passes through a variable gain equalizing stage, whose frequency response closely matches the inverse of the cable loss characteristic. In addition, the variation of the frequency response with control voltage imitates the variation of the inverse cable loss characteristic with cable length.

The edge energy of the equalized signal is monitored by a detector circuit which produces an error signal corresponding to the difference between the desired edge energy and the actual edge energy. This error signal is integrated by both an internal and an external AGC filter capacitor providing a steady control voltage for the gain stage. As the frequency response of the gain stage is automatically varied by the application of negative feedback, the edge energy of the equalized signal is kept at a constant level which is representative of the original edge energy at the transmitter. The equalized signal is also DC-restored, effectively restoring the logic threshold of the equalized signal to its correct level independent of shifts due to AC-coupling.

4.3 Serial Digital Outputs

The digital output signals have a nominal voltage of either 800mV_{p-p} or 400mV_{p-p} as set by the OP_CTL pin. Table 4-1 below shows the typical output voltage levels across different common mode voltages and swing values:

Table 4-1: Typical Output Voltage Levels

Supply Voltage - Output Driver	400mV _{p-p} Swing (DC-coupled Output)	400mV _{p-p} Swing (AC-coupled Output)	800mV _{p-p} Swing (DC-coupled Output)	800mV _{p-p} Swing (AC-coupled Output)
3.3V	3.2V	3.1V	3.1V	2.9V
2.5V	2.4V	2.3V	2.3V	2.1V
1.8V	1.7V	1.6V	1.6V	1.4V
1.2V	1.1V	1V	1V	0.8V

4.4 Programmable Squelch Adjust (SQ_ADJ)

The GS2994 incorporates a programmable Squelch Adjust (SQ_ADJ) threshold.

This feature can be useful in applications where there are multiple input channels using the GS2994 and the maximum gain can be limited to avoid crosstalk.

The SQ_ADJ pin acts to change the threshold of the Carrier Detect (\overline{CD}) pin, through voltage level variances. When the input signal drops below a certain threshold, the \overline{CD} pin will be driven HIGH, indicating that there is not a valid input signal. In applications where programmable squelch adjust is not required, the SQ_ADJ pin may be left unconnected. Figure 4-1 shows the relationship between the SQ_ADJ voltage and cable length at which \overline{CD} will assert or deassert.

This feature has been designed for use in applications such as routers, where signal crosstalk and circuit noise cause the Equalizer to output erroneous data when no input signal is present. The use of a Carrier Detect function with a fixed internal reference does not solve this problem, since the signal to noise ratio on the circuit board could be significantly less than the default signal detection level set by the on chip reference.

NOTE: SQ_ADJ is designed to operate when the device is in manual sleep mode. In this situation, \overline{CD} should not be connected to SLEEP.

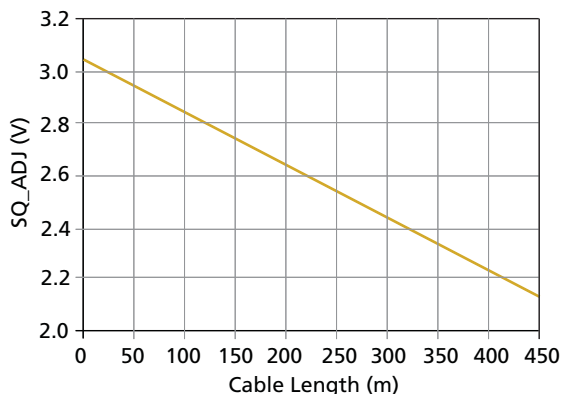


Figure 4-1: SQ_ADJ vs. Cable Length (VCC=3.3V, room temperature, 800mV launch swing)

4.5 Carrier Detect, Sleep, and Auto-Sleep

The GS2994 includes a SLEEP input pin, which allows the application interface to put the GS2994 into a low-power sleep mode, consuming less than 30mW. Set the SLEEP pin HIGH to place the chip in its sleep state. In this mode, the Carrier Detect output will still function in order to detect valid Serial Digital Input.

The Carrier Detect output pin (\overline{CD}) indicates the presence of a valid signal at the input of the GS2994. When \overline{CD} is LOW, the device has detected a valid input on SDI and \overline{SDI} . When \overline{CD} is HIGH, the device has not detected a valid input.

The Carrier Detect output still functions when the GS2994 is in sleep mode, such that a valid Serial Digital Input can be detected at all times. In the sleep state, the carrier detect functionality requires that the GAIN_SEL input be set to 0.

Auto-Sleep can be enabled by connecting \overline{CD} to SLEEP. When connected, the GS2994 will automatically go into standby mode when there is a loss of Serial Digital Input signal.

NOTE 1: \overline{CD} will only detect loss of carrier for data rates greater than 19Mb/s.

NOTE 2: If the maximum cable length is exceeded (set by the SQ_ADJ pin) and the device is not in Bypass mode, the \overline{CD} pin will not be driven LOW, even if a carrier is present.

NOTE 3: If the \overline{CD} is connected to SLEEP, SQ_ADJ should either be left open, or connected to ground.

Table 4-2: Sleep Input Table

Sleep	Function
0	The GS2994 operates normally
1	The GS2994 enters sleep mode. \overline{CD} output remains valid

Table 4-3: $\overline{\text{CD}}$ Output Table

$\overline{\text{CD}}$	Input Status
0	Valid Input on SDI, $\overline{\text{SDI}}$ pins
1	Input is not valid

4.6 GAIN_SEL

The GS2994 has an option of compensating for 6dB of flat attenuation in applications where there has been some type of attenuation prior to the equalizer.

Table 4-4: GAIN_SEL Input Table

GAIN_SEL	Function
0	No flat band gain is applied
1	6dB of flat attenuation will be compensated by the equalizer.

4.7 Adjustable Output Swing, De-Emphasis and Mute

With the GS2994, the OP_CTL input pin determines the output swing and de-emphasis settings.

The OP_CTL pin is an analog input to allow different combinations of output swing, de-emphasis and mute. The possible values are listed in [Table 4-5](#) below:

Table 4-5: OP_CTL Functions and Levels

Level	Swing	De-emphasis	Mute	Voltage
0	800mV	Off	N	0
1	800mV	2dB	N	1 x (VCC_A/8)
2	800mV	4dB	N	2 x (VCC_A/8)
3	800mV	6dB	N	3 x (VCC_A/8)
4	400mV	Off	N	4 x (VCC_A/8)
5	400mV	2dB	N	5 x (VCC_A/8)
6	400mV	4dB	N	6 x (VCC_A/8)
7	400mV	6dB	N	7 x (VCC_A/8)
8	400mV	N/A	Y	VCC_A

Auto_mute can be enabled by connecting $\overline{\text{CD}}$ to OP_CTL through external components, such that when $\overline{\text{CD}}$ is HIGH (2.5V), OP_CTL is forced HIGH (3.3V) and when $\overline{\text{CD}}$ is LOW

(0V), OP_CTL is forced LOW (0V). The input level at which the part is muted can be set by the SQ_ADJ pin through suitable voltage variances as described in [Section 4.4](#).

NOTE: when SQ_ADJ functionality is used and/or in Auto_mute, the SLEEP pin should be left open.

5. Application Information

5.1 High Gain Adaptive Cable Equalizers

The GS2994 is Gennum's latest multi-rate adaptive cable equalizer. In order to continue to extend the cable length that an equalizer will remain operational over, it is necessary to have high gain in the equalizer.

A video cable equalizer must provide wide band gain over a range of frequencies in order to accommodate the range of data rates and signal patterns that are present in a SMPTE compliant serial video stream.

The GS2994 has an increase in gain over the GS2974A at critical HD and 3Gb/s frequencies, and because of this, the GS2994 may be sensitive to signals at the input that the GS2974A will not be sensitive to.

Small levels of signal or noise present at the input pins of the Equalizer may cause chatter at the output. In order to prevent this from happening, particular attention must be paid to board layout.

5.2 PCB Layout

Special attention must be paid to component layout when designing Serial Digital Interfaces for HDTV. An FR-4 dielectric can be used, however, controlled impedance transmission lines are required for PCB traces longer than approximately 1cm. Note the following PCB artwork features used to optimize performance:

- PCB trace width for 3Gb/s rate signals is closely matched to SMT component width to minimize reflections due to change in trace impedance
- The PCB ground plane is removed under the GS2994 input components to minimize parasitic capacitance
- The PCB ground plane is removed under the GS2994 output components to minimize parasitic capacitance
- High-speed traces are curved to minimize impedance changes

5.3 Typical Application Circuit

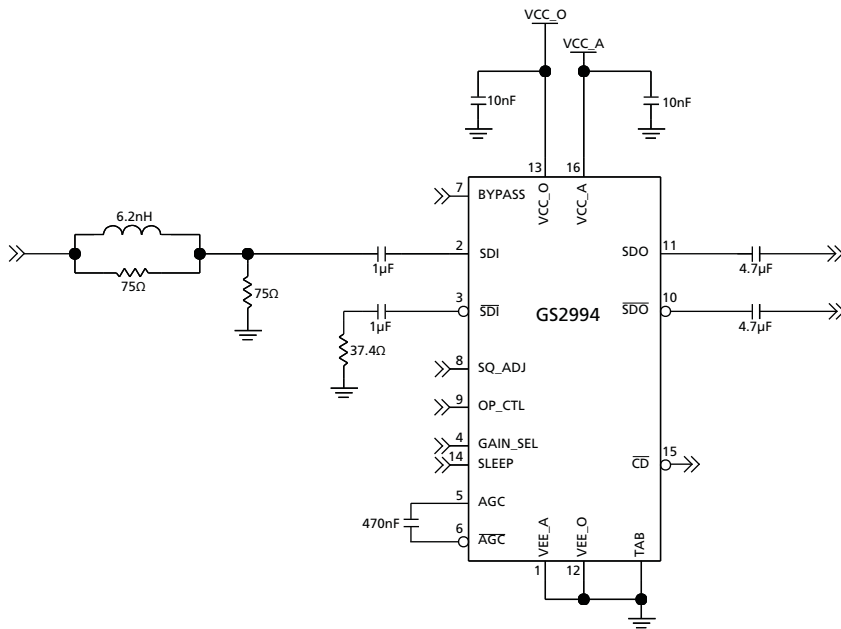
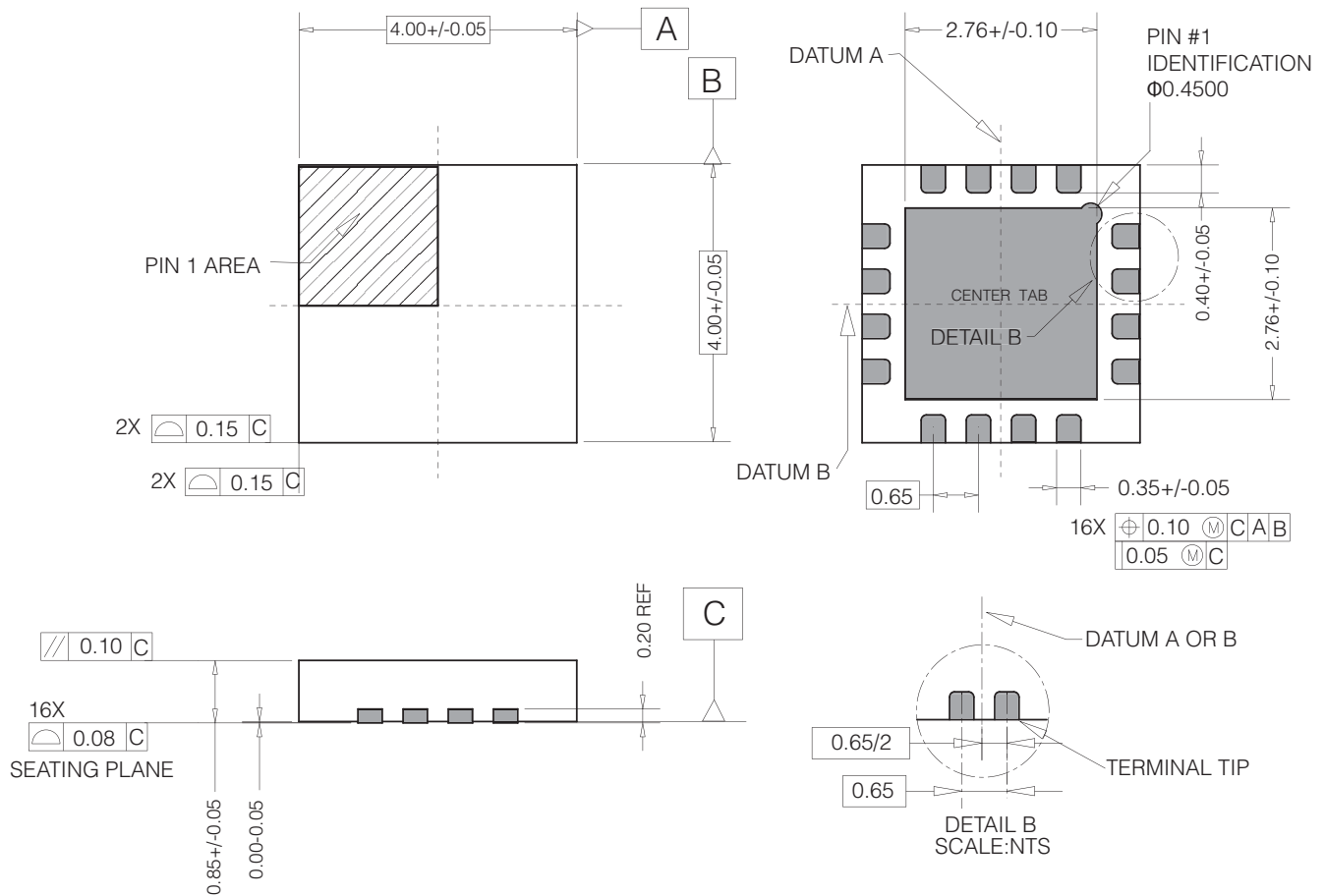


Figure 5-1: GS2994 Typical Application Circuit

6. Package & Ordering Information

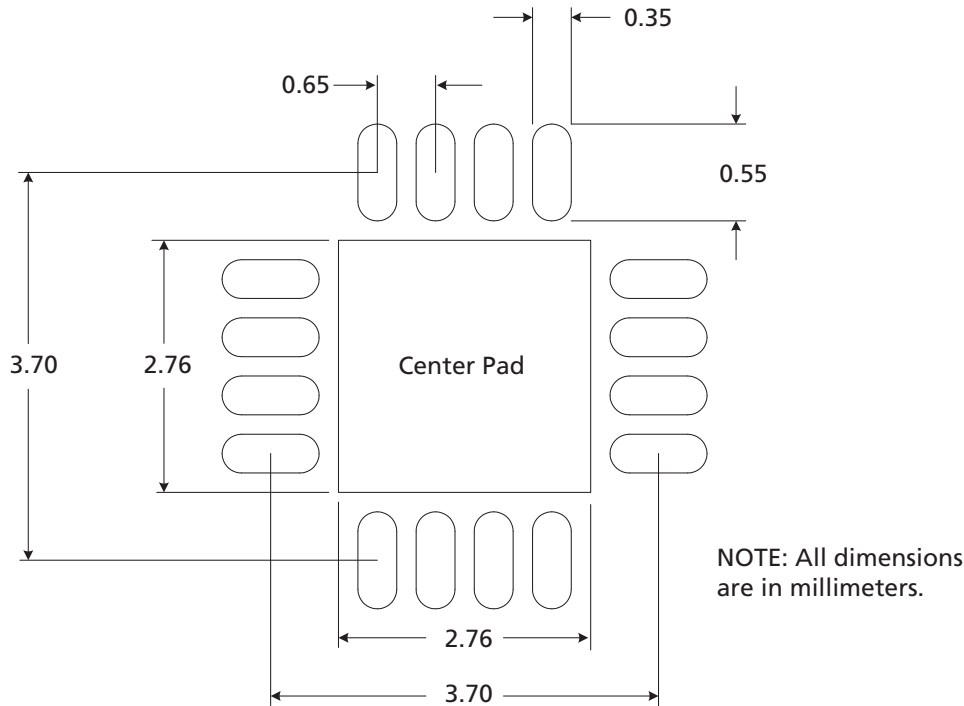
6.1 Package Dimensions



6.2 Packaging Data

Parameter	Value
Package Type	4mm x 4mm 16-pin QFN
Package Drawing Reference	JEDEC M0220
Moisture Sensitivity Level	1
Junction to Case Thermal Resistance, θ_{j-c}	31.0°C/W
Junction to Air Thermal Resistance, θ_{j-a} (at zero airflow)	43.8°C/W
Psi, ψ	11.0°C/W
Pb-free and RoHS compliant	Yes

6.3 Recommended PCB Footprint



The Center Pad should be connected to the most negative power supply plane for analog circuitry in the device (VEE_A) by a minimum of 5 vias.

NOTE: Suggested dimensions only. Final dimensions should conform to customer design rules and process optimizations.

6.4 Marking Diagram



6.5 Solder Reflow Profiles

The GS2994 is available in a Pb-free package. It is recommended that the Pb-free package be soldered with Pb-free paste using the reflow profile shown in Figure 6-1.

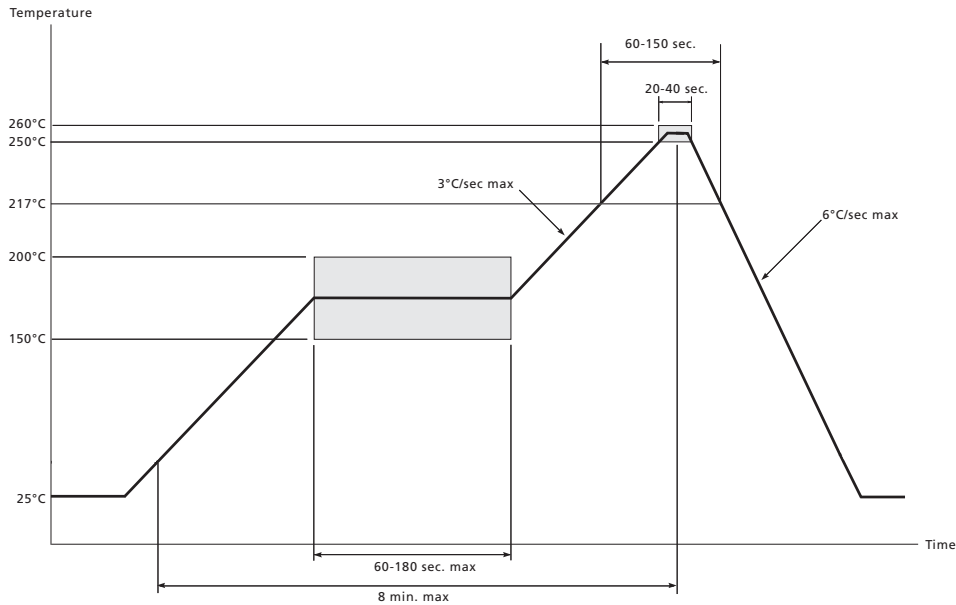


Figure 6-1: Maximum Pb-free Solder Reflow Profile

6.6 Ordering Information

	Part Number	Package	Temperature Range
GS2994	GS2994-INE3	16-pin QFN	-40°C to 85°C
GS2994	GS2994-INTE3	16-pin QFN Tape & Reel (250pcs)	-40°C to 85°C
GS2994	GS2994-INTE3Z	16-pin QFN Tape & Reel (2500pcs)	-40°C to 85°C



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