



IMPORTANT NOTICE

10 December 2015

1. Global joint venture starts operations as WeEn Semiconductors

Dear customer,

As from November 9th, 2015 NXP Semiconductors N.V. and Beijing JianGuang Asset Management Co. Ltd established Bipolar Power joint venture (JV), **WeEn Semiconductors**, which will be used in future Bipolar Power documents together with new contact details.

In this document where the previous NXP references remain, please use the new links as shown below.

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Thank you for your cooperation and understanding,

WeEn Semiconductors



DATA SHEET

BTH151S-650R

Thyristor

High Repetitive Surge

Product specification

March 2001



Thyristor High Repetitive Surge

BTH151S-650R

GENERAL DESCRIPTION

Passivated thyristor in a plastic envelope, suitable for surface mounting, intended for use in applications requiring high bidirectional blocking voltage capability and high thermal cycling performance. This thyristor has a high repetitive surge specification which makes it suitable for applications where high inrush currents or stall currents are likely to occur on a repetitive basis.

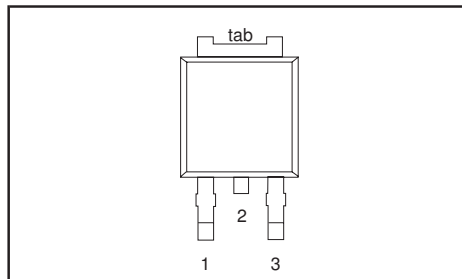
QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	UNIT
V_{DRM}, V_{RRM}	Repetitive peak off-state voltages	650	V
$I_{T(AV)}$	Average on-state current	7.5	A
$I_{T(RMS)}$	RMS on-state current	12	A
I_{TSM}	Non-repetitive peak on-state current	110	A
I_{TRM}	Repetitive peak on-state current	60	A

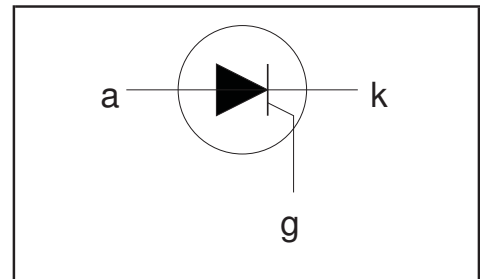
PINNING - SOT428

PIN	DESCRIPTION
1	cathode
2	anode
3	gate
tab	anode

PIN CONFIGURATION



SYMBOL



LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DRM}, V_{RRM}	Repetitive peak off-state voltages	half sine wave;	-	650	V
$I_{T(AV)}$	Average on-state current	$T_{mb} \leq 103\text{ }^\circ\text{C}$	-	7.5	A
$I_{T(RMS)}$	RMS on-state current	all conduction angles	-	12	A
I_{TSM}	Non-repetitive peak on-state current	half sine wave; $T_j = 25\text{ }^\circ\text{C}$ prior to surge	-	110	A
		$t = 10\text{ ms}$	-	121	A
		$t = 8.3\text{ ms}$	-	60	A
I_{TRM}	Repetitive peak on-state current	$t = 10\text{ms}, \tau = 3\text{s}, T_{mb} \leq 45\text{ }^\circ\text{C}, \text{no. of surges} = 100\text{k}$	-	60	A
I^2t	I^2t for fusing	$t = 10\text{ ms}$	-	61	A ² s
di_T/dt	Repetitive rate of rise of on-state current after triggering	$I_{TM} = 20\text{ A}; I_G = 50\text{ mA}; di_G/dt = 50\text{ mA}/\mu\text{s}$	-	50	A/ μs
I_{GM}	Peak gate current		-	2	A
V_{GM}	Peak gate voltage		-	5	V
V_{RGM}	Peak reverse gate voltage		-	5	V
P_{GM}	Peak gate power		-	5	W
$P_{G(AV)}$	Average gate power	over any 20 ms period	-	0.5	W
T_{stg}	Storage temperature		-40	150	$^\circ\text{C}$
T_j	Operating junction temperature		-	125	$^\circ\text{C}$

1 Although not recommended, off-state voltages up to 800V may be applied without damage, but the thyristor may switch to the on-state. The rate of rise of current should not exceed 15 A/ μs .

Thyristor
High Repetitive Surge

BTH151S-650R

THERMAL RESISTANCES

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$R_{th\ j-mb}$	Thermal resistance junction to mounting base		-	-	1.8	K/W
$R_{th\ j-a}$	Thermal resistance junction to ambient	pcb (FR4) mounted; footprint as in Fig.14	-	75	-	K/W

STATIC CHARACTERISTICS

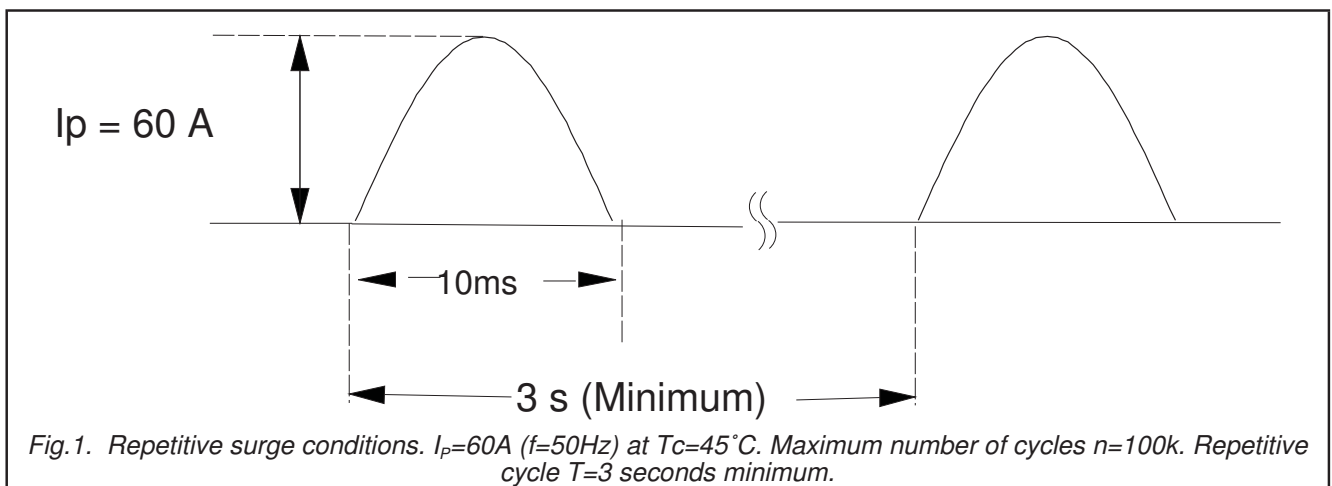
$T_j = 25\text{ }^\circ\text{C}$ unless otherwise stated

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{GT}	Gate trigger current	$V_D = 12\text{ V}; I_T = 0.1\text{ A}$	-	2	15	mA
I_L	Latching current	$V_D = 12\text{ V}; I_{GT} = 0.1\text{ A}$	-	10	40	mA
I_H	Holding current	$V_D = 12\text{ V}; I_{GT} = 0.1\text{ A}$	-	7	20	mA
V_T	On-state voltage	$I_T = 23\text{ A}$	-	1.4	1.75	V
V_{GT}	Gate trigger voltage	$V_D = 12\text{ V}; I_T = 0.1\text{ A}$	-	0.6	1.5	V
I_D, I_R	Off-state leakage current	$V_D = V_{DRM(max)}; I_T = 0.1\text{ A}; T_j = 125\text{ }^\circ\text{C}$ $V_D = V_{DRM(max)}; V_R = V_{RRM(max)}; T_j = 125\text{ }^\circ\text{C}$	0.25	0.4	-	V
			-	0.1	0.5	mA

DYNAMIC CHARACTERISTICS

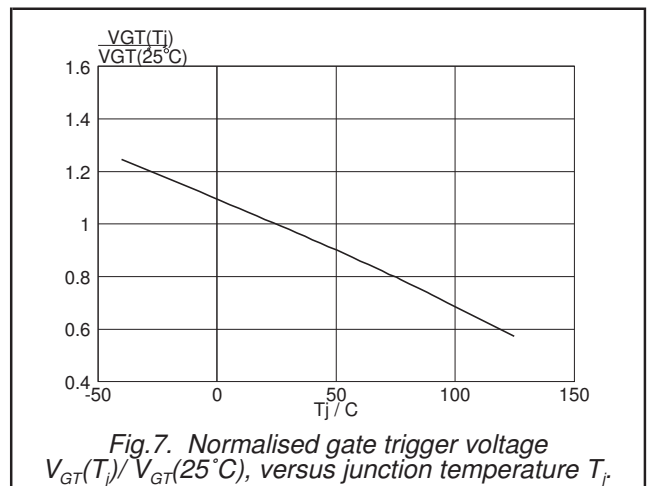
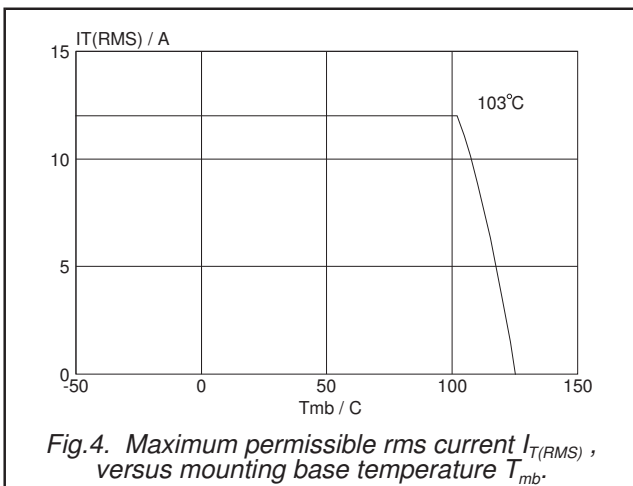
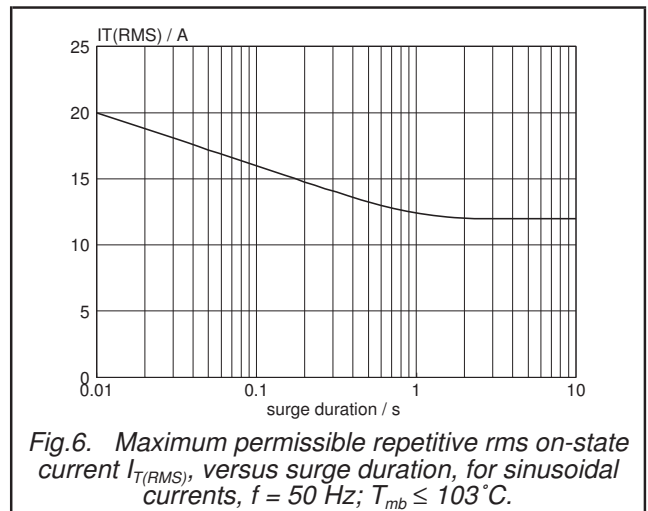
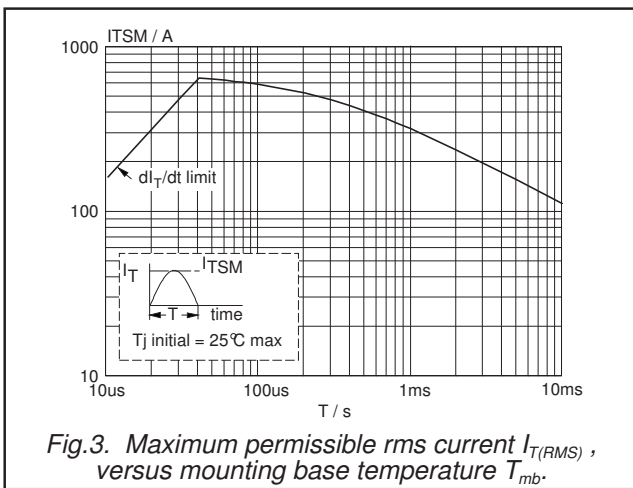
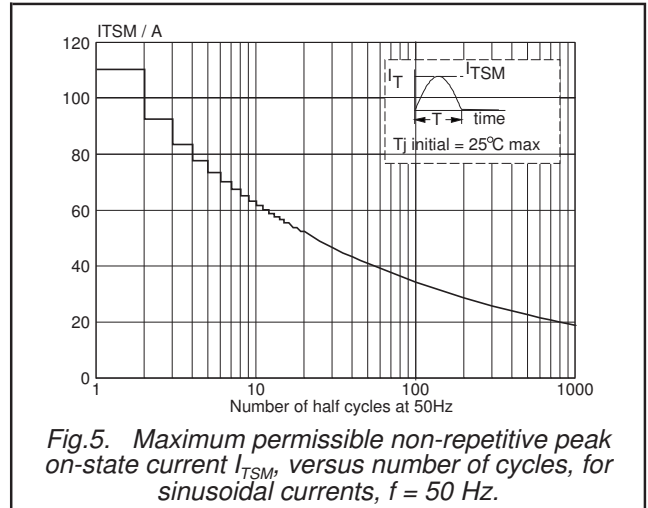
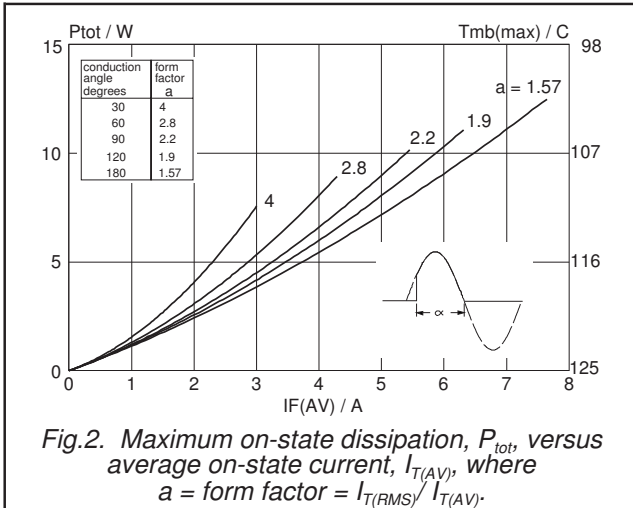
$T_j = 25\text{ }^\circ\text{C}$ unless otherwise stated

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
dV_D/dt	Critical rate of rise of off-state voltage	$V_{DM} = 67\% V_{DRM(max)}; T_j = 125\text{ }^\circ\text{C};$ exponential waveform; Gate open circuit $R_{GK} = 100\ \Omega$	50 200	130 1000	-	V/ μs V/ μs
t_{gt}	Gate controlled turn-on time	$I_{TM} = 40\text{ A}; V_D = V_{DRM(max)}; I_G = 0.1\text{ A};$ $dI_G/dt = 5\text{ A}/\mu\text{s}$	-	2	-	μs
t_q	Circuit commutated turn-off time	$V_D = 67\% V_{DRM(max)}; T_j = 125\text{ }^\circ\text{C};$ $I_{TM} = 20\text{ A}; V_R = 25\text{ V}; dI_{TM}/dt = 30\text{ A}/\mu\text{s};$ $dV_D/dt = 50\text{ V}/\mu\text{s}; R_{GK} = 100\ \Omega$	-	70	-	μs



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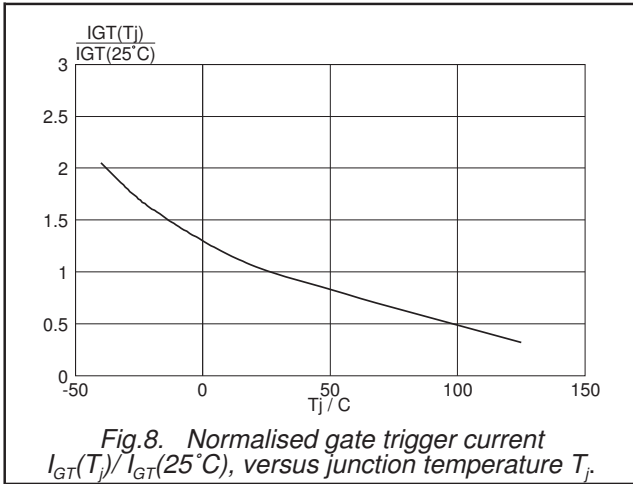


Fig.8. Normalised gate trigger current $I_{GT}(T_j)/I_{GT}(25^\circ\text{C})$, versus junction temperature T_j .

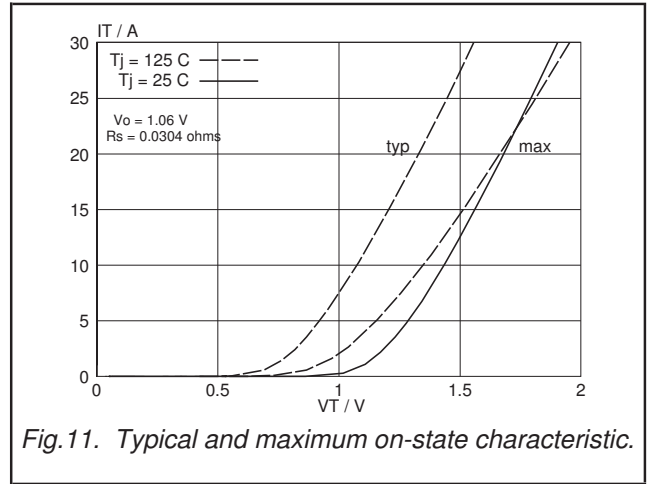


Fig.11. Typical and maximum on-state characteristic.

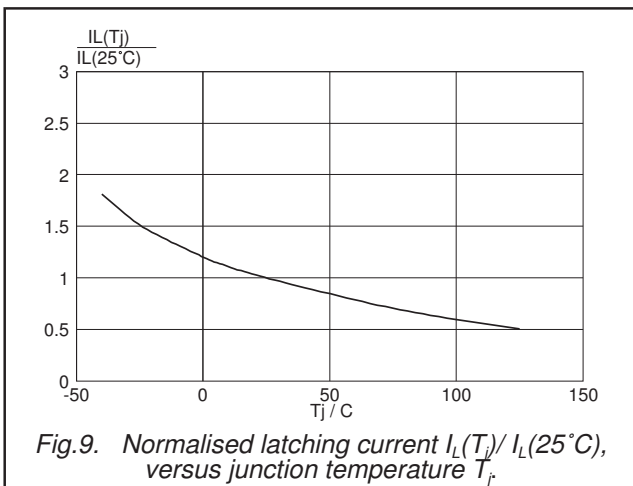


Fig.9. Normalised latching current $I_L(T_j)/I_L(25^\circ\text{C})$, versus junction temperature T_j .

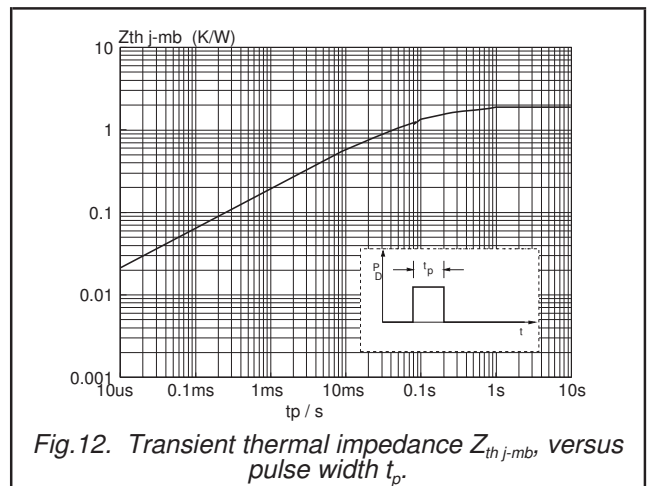


Fig.12. Transient thermal impedance $Z_{th\ j-mb}$, versus pulse width t_p .

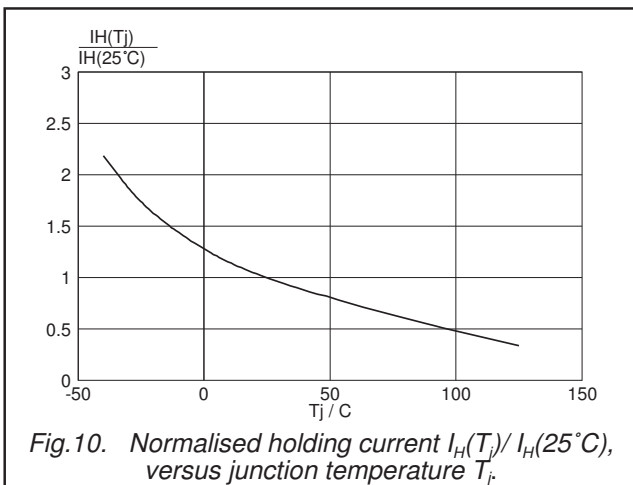


Fig.10. Normalised holding current $I_H(T_j)/I_H(25^\circ\text{C})$, versus junction temperature T_j .

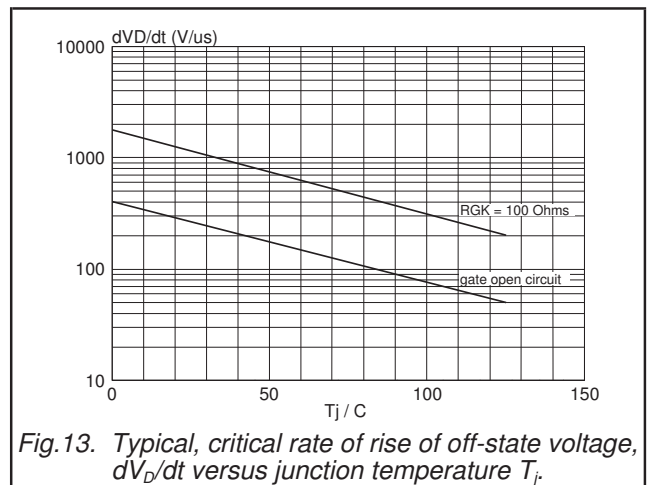
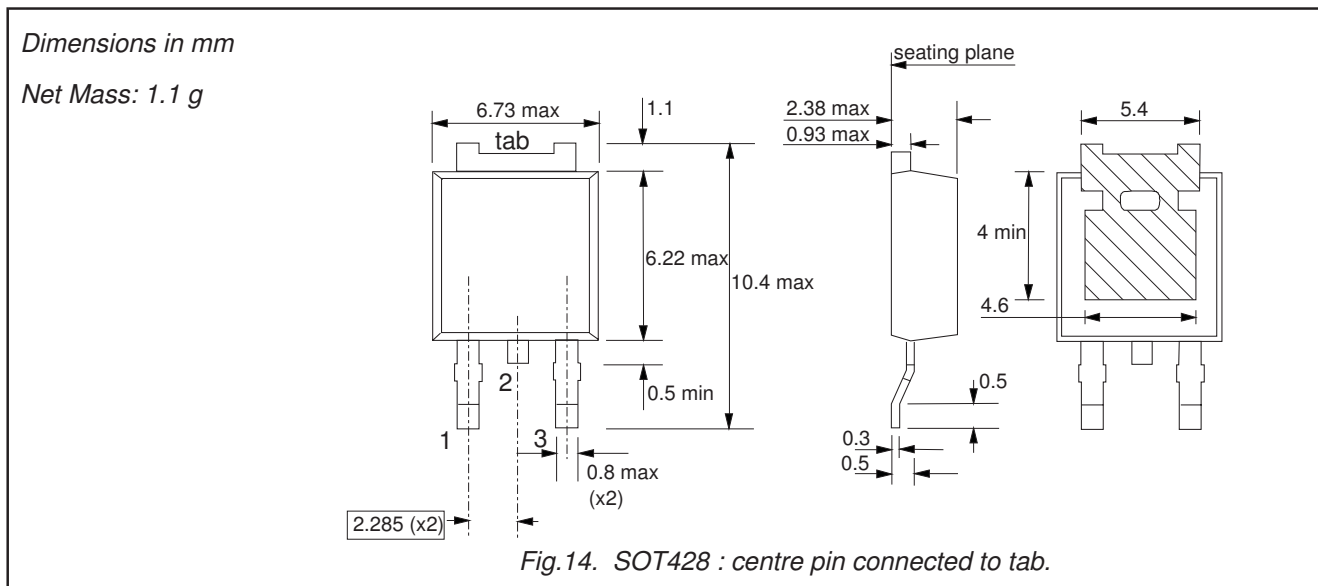


Fig.13. Typical, critical rate of rise of off-state voltage, dV_D/dt versus junction temperature T_j .

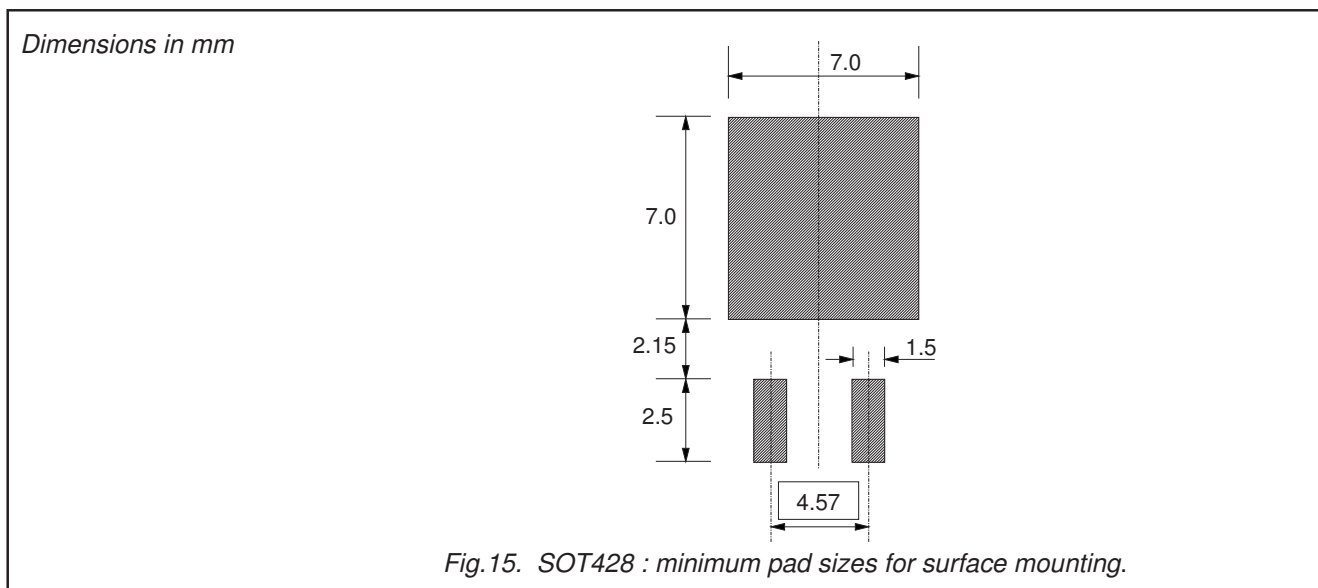
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BTH151S-650R

MECHANICAL DATA



MOUNTING INSTRUCTIONS



Notes

1. Plastic meets UL94 V0 at 1/8".

Legal information

DATA SHEET STATUS

DOCUMENT STATUS ⁽¹⁾	PRODUCT STATUS ⁽²⁾	DEFINITION
Objective data sheet	Development	This document contains data from the objective specification for product development.
Preliminary data sheet	Qualification	This document contains data from the preliminary specification.
Product data sheet	Production	This document contains the product specification.

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Contact information

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