BTS 5242-2L

Smart High-Side Power Switch

PROFET

Two Channels, 25 mΩ

Automotive Power

Never stop thinking.

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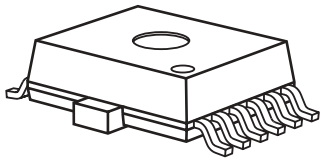
Smart High-Side Power Switch **BTS 5242-2L**
PROFET

Product Summary

The BTS 5242-2L is a dual channel high-side power switch in PG-DSO-12-9 package providing embedded protective functions.

The power transistor is built by a N-channel vertical power MOSFET with charge pump. The device is monolithically integrated in Smart SIPMOS technology.

PG-DSO-12-9



Operating voltage	$V_{bb(on)}$	4.5 .. 28 V
Over voltage protection	$V_{bb(AZ)}$	41 V
On-State resistance	$R_{DS(ON)}$	25 mΩ
Nominal load current (one channel active)	$I_{L(nom)}$	6 A
Adjustable current limitation	$I_{L(LIM)}$	7 A / 40 A
Current limitation repetitive	$I_{L(SCr)}$	7 A / 40 A
Standby current for whole device with load	$I_{bb(OFF)}$	7.5 µA

Basic Features

- Very low standby current
- 3.3 V and 5 V compatible logic pins
- Improved electromagnetic compatibility (EMC)
- Stable behavior at under voltage
- Logic ground independent from load ground
- Secure load turn-off while logic ground disconnected
- Very low leakage current from OUT to GND
- Green product (RoHS compliant)

Type	Ordering Code	Package
BTS 5242-2L	On request	PG-DSO-12-9

Protective Functions

- Reverse battery protection with external resistor
- Short circuit protection
- Overload protection
- Multi-step current limitation
- Adjustable current limitation
- Thermal shutdown with restart
- Over voltage protection with external resistor
- Loss of ground and loss of V_{bb} protection
- Electrostatic discharge protection (ESD)

Diagnostic Functions

- IntelliSense functionality for each channel
- Proportional load current sense signal by current source
- Open load detection in ON-state by load current sense
- Open load detection in OFF-state by voltage source
- Feedback on over temperature and current limitation in ON-state
- Suppressed thermal toggling of fault signal

Applications

- µC compatible high-side power switch with diagnostic feedback for 12 V grounded loads
- All types of resistive, inductive and capacitive loads
- Most suitable for loads with high inrush currents, so as lamps
- Replaces electromechanical relays, fuses and discrete circuits

1 Overview

The BTS 5242-2L is a dual channel high-side power switch (two times 25 mΩ) in PG-DSO-12-9 power package providing embedded protective functions. Integrated resistors at each input pin (IN1, IN2, CLA) reduce external components.

The load current limitation can be adjusted in two steps by the current limit adjust pin (CLA).

The IntelliSense pins IS1 and IS2 provide a sophisticated diagnostic feedback signal including current sense function, open load in off state and over load alert.

The power transistor is built by a N-channel vertical power MOSFET with charge pump. The inputs are ground referenced CMOS compatible. The device is monolithically integrated in Smart SIPMOS technology.

1.1 Block Diagram

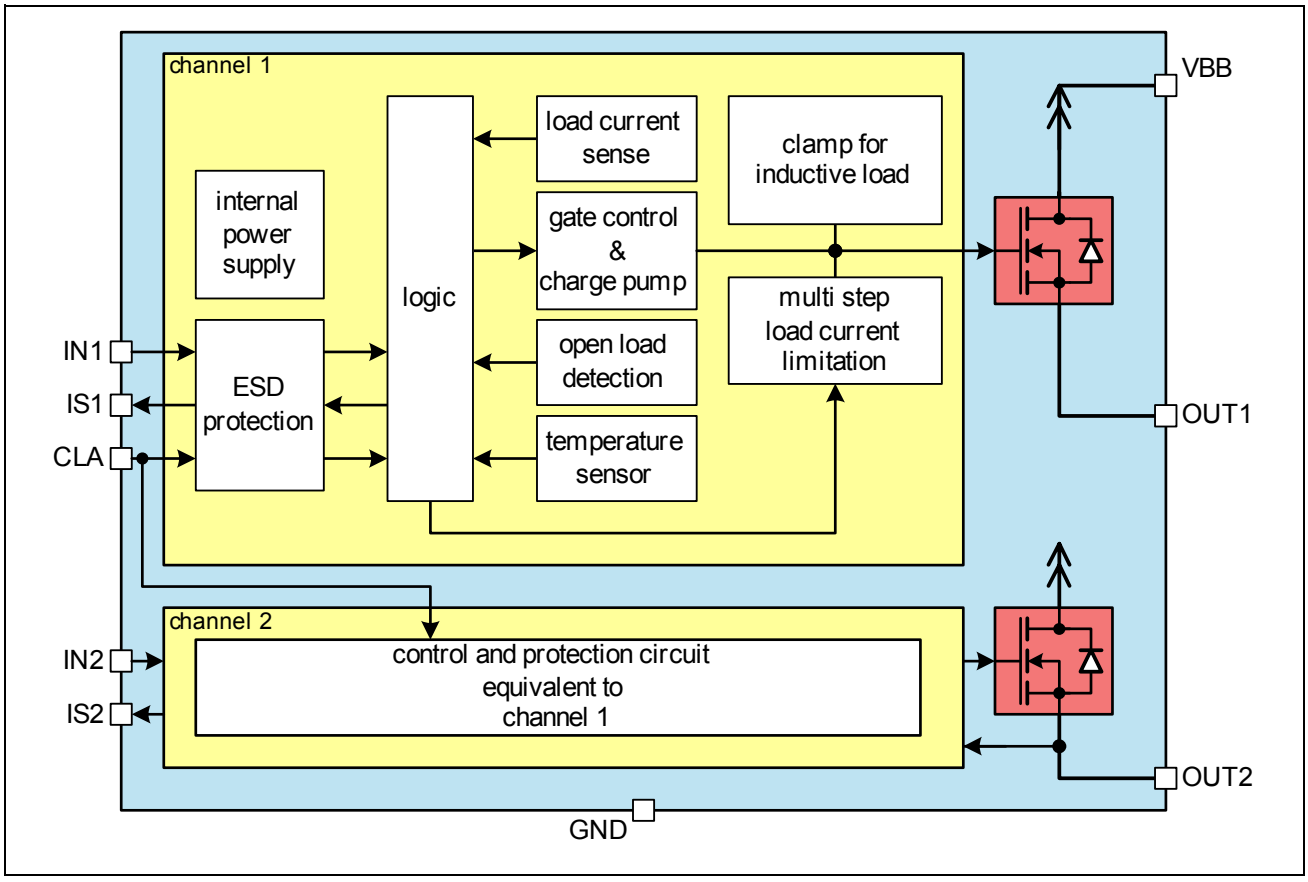


Figure 1 Block Diagram

1.2 Terms

Following figure shows all terms used in this target data sheet.

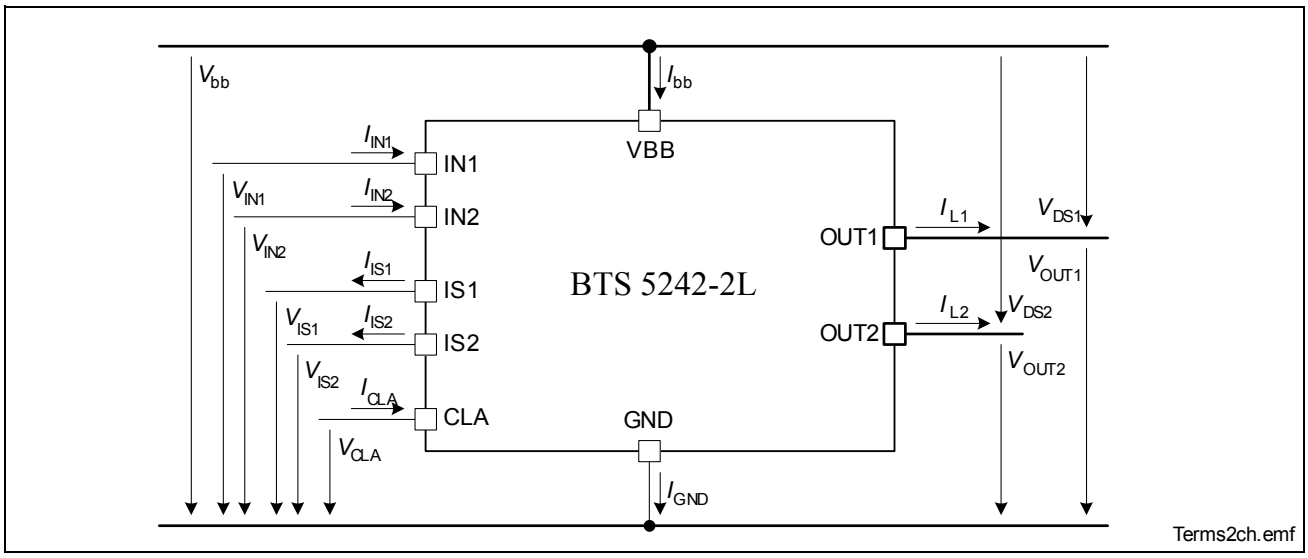


Figure 2 Terms

2 Pin Configuration

2.1 Pin Assignment BTS 5242-2L

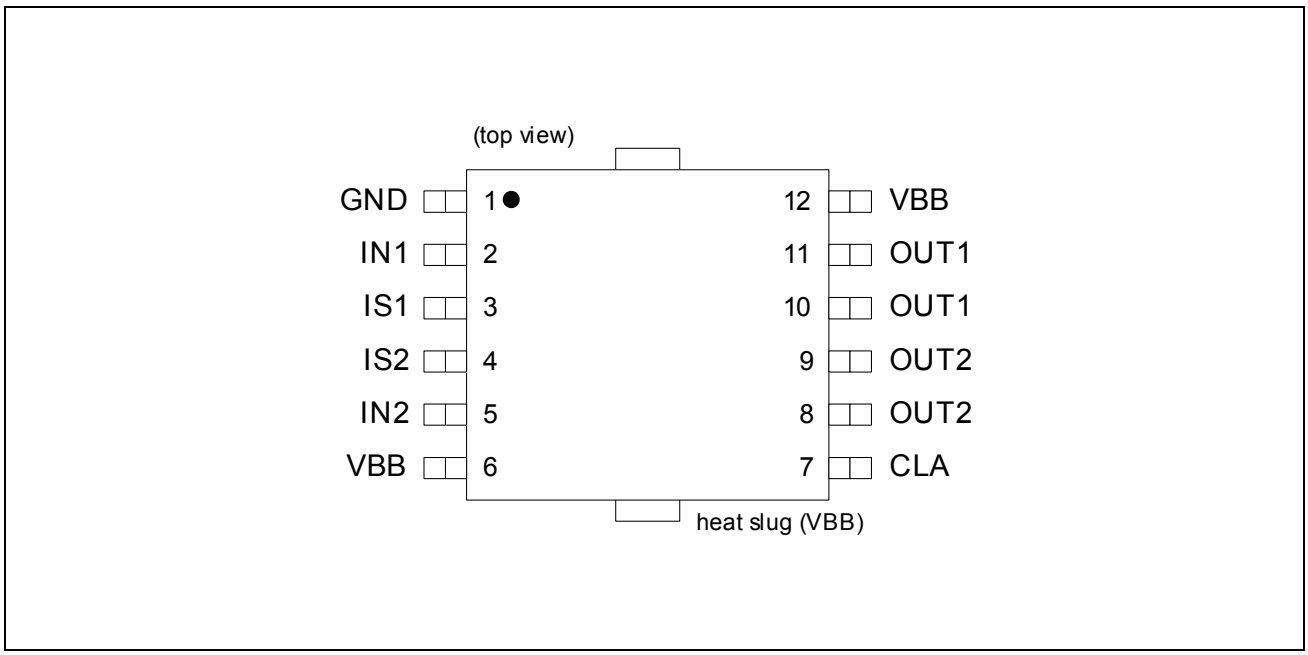


Figure 3 Pin Configuration PG-DSO-12-9

2.2 Pin Definitions and Functions

Pin	Symbol	I/O OD	Function
2	IN1	I	Input signal for channel 1
5	IN2	I	Input signal for channel 2
3	IS1	O	Diagnosis output signal channel 1
4	IS2	O	Diagnosis output signal channel 2
7	CLA	I	Current limit adjust input for channel 1&2
10,11	OUT1 [1)]	O	Protected high-side power output channel 1
8, 9	OUT2 [1)]	O	Protected high-side power output channel 2
1	GND	-	Ground connection
6,12, heat slug	VBB	-	Positive power supply for logic supply as well as output power supply

[1)] All output pins of each channel have to be connected

3 Electrical Characteristics

3.1 Maximum Ratings

Stresses above the ones listed here may cause permanent damage to the device. Exposure to maximum rating conditions for extended periods may affect device reliability.

T_j = 25 °C (unless otherwise specified)

Pos.	Parameter	Symbol	Limit Values		Unit	Test Conditions
			min.	max.		
Power Supply						
3.1.1	Supply voltage	V_{bb}		18 28	V	 $t \leq 100$ h
3.1.2	Current through ground pin	I_{GND}	-150		mA	$t \leq 2$ min
3.1.3	Supply voltage for full short circuit protection (single pulse) (T_j = -40°C .. 150°C)	$V_{bb(SC)}$	0	28	V	L = 8 µH R = 0.2 Ω [1]
3.1.4	Voltage at power transistor	V_{DS}		52	V	
3.1.5	Supply Voltage for Load Dump protection	$V_{bb(LD)}$		 40 53	V	R_I = 2 Ω [2] R_L = 2.25 Ω R_L = 6.8 Ω
Power Stages						
3.1.6	Load current	I_L		$I_{L(LIM)}$	A	[3]
3.1.7	Maximum energy dissipation single pulse	E_{AS}		130	mJ	[4] $T_{j(0)}$ = 150°C $I_{L(0)}$ = 6 A V_{bb}=12V
3.1.8	Power dissipation (DC)	P_{tot}		1.4	W	[5] T_a = 85 °C $T_j \leq 150$ °C
Logic Pins						
3.1.9	Voltage at input pin	V_{IN}	-5 -16	19	V	 $t \leq 2$ min
3.1.10	Current through input pin	I_{IN}	-2.0 -8.0	2.0	mA	 $t \leq 2$ min

T_j = 25 °C (unless otherwise specified)

Pos.	Parameter	Symbol	Limit Values		Unit	Test Conditions
			min.	max.		
3.1.11	Voltage at current limit adjust pin	V_{CLA}	-5 -16	19	V	 $t \leq 2$ min
3.1.12	Current through current limit adjust pin	I_{CLA}	-2.0 -8.0	2.0	mA	 $t \leq 2$ min
3.1.13	Current through sense pin	I_{IS}	-5	10	mA	
Temperatures						
3.1.14	Junction temperature	T_j	-40	150	°C	
3.1.15	Dynamic temperature increase while switching	ΔT_j		60	°C	
3.1.16	Storage temperature	T_{stg}	-55	150	°C	
ESD Susceptibility						
3.1.17	ESD susceptibility HBM IN, CLA IS OUT	V_{ESD}	 -1 -2 -4	 1 2 4	kV	according to EIA/JESD 22-A 114B

1) R and L describe the complete circuit impedance including line, contact and generator impedances

2) Load Dump is specified in ISO 7637, R_I is the internal resistance of the Load Dump pulse generator

3) Current limitation is a protection feature. Operation in current limitation is considered as “outside” normal operating range. Protection features are not designed for continuous repetitive operation.

4) Pulse shape represents inductive switch off: $I_L(t) = I_L(0) * (1 - t / t_{peak})$; $0 < t < t_{peak}$

5) Device mounted on PCB (50 mm x 50 mm x 1.5 mm epoxy, FR4) with 6 cm^2 copper heatsinking area (one layer, 70 µm thick) for V_{bb} connection. PCB is vertical without blown air.

4 Block Description and Electrical Characteristics

4.1 Power Stages

The power stages are built by a N-channel vertical power MOSFET (DMOS) with charge pump.

4.1.1 Output On-State Resistance

The on-state resistance $R_{DS(ON)}$ depends on the supply voltage as well as the junction temperature T_j. **Figure 4** shows that dependencies for the typical on-state resistance . The behavior in reverse polarity mode is described in **Section 4.2.2**.

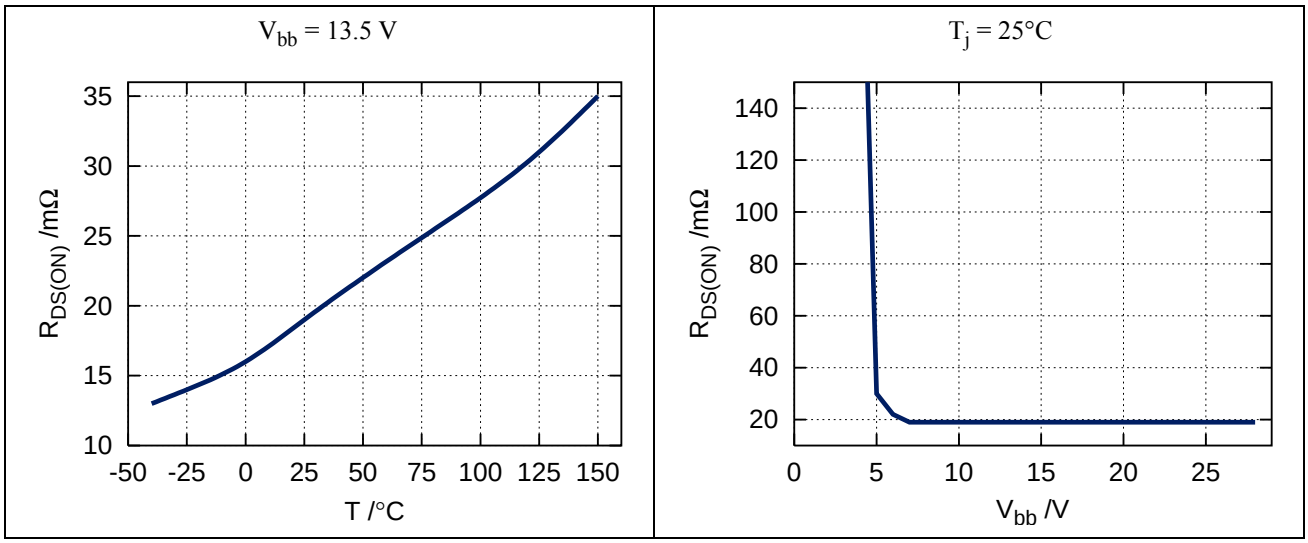


Figure 4 Typical On-State Resistance

4.1.2 Input Circuit

Figure 5 shows the input circuit of the BTS 5242-2L. There is an integrated input resistor that makes external components obsolete. The current sink to ground ensures that the device switches off in case of open input pin. The zener diode protects the input circuit against ESD pulses.

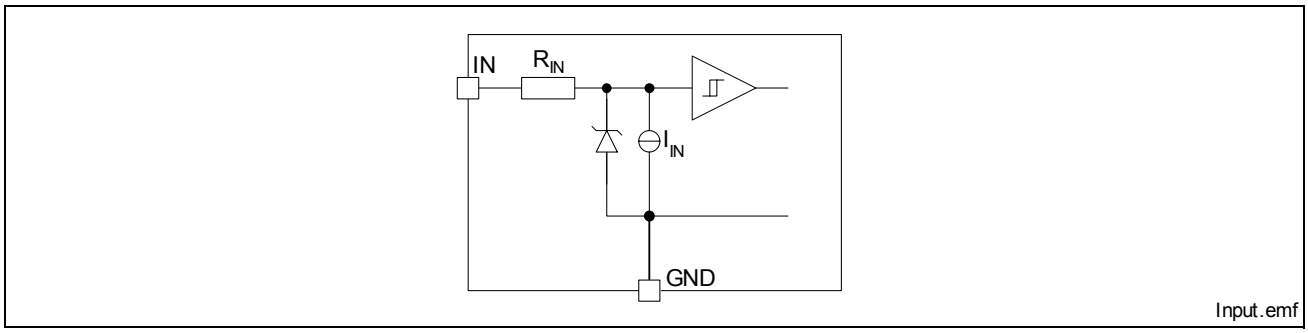


Figure 5 Input Circuit (IN1 and IN2)

A high signal at the input pin causes the power DMOS to switch on with a dedicated slope, which is optimized in terms of EMC emission.

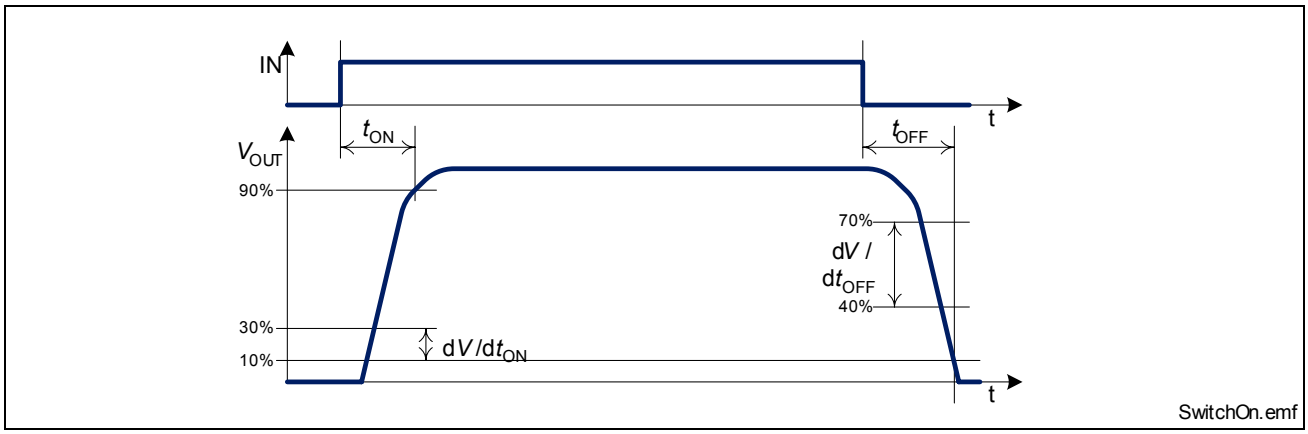


Figure 6 Switching a Load (resistive)

4.1.3 Inductive Output Clamp

When switching off inductive loads with high-side switches, the voltage V_{OUT} drops below ground potential, because the inductance intends to continue driving the current.

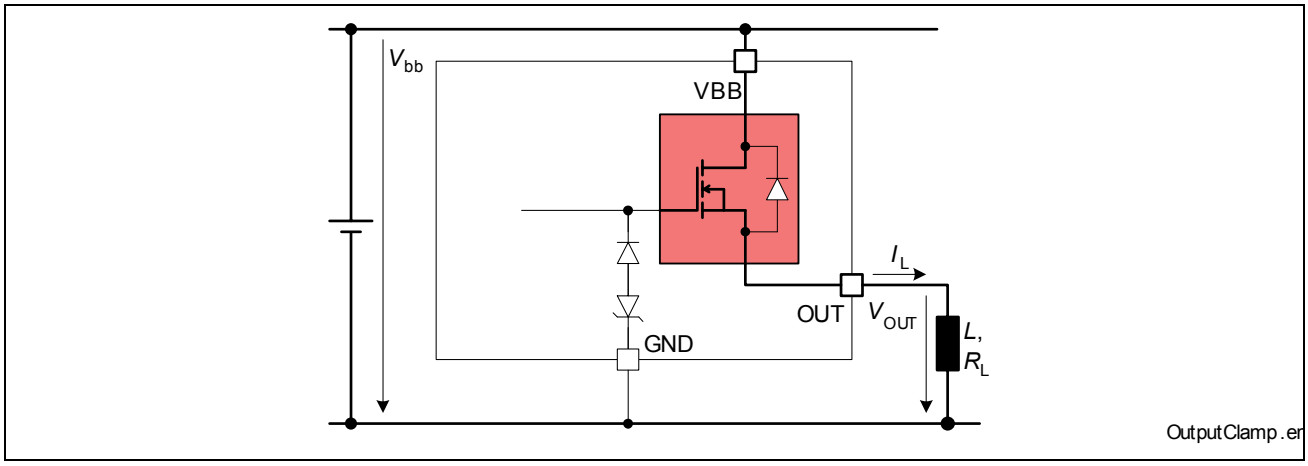


Figure 7 Output Clamp (OUT1 and OUT2)

To prevent destruction of the device, there is a voltage clamp mechanism implemented that keeps that negative output voltage at a certain level ($V_{OUT(CL)}$). See **Figure 7** and **Figure 8** for details. Nevertheless, the maximum allowed load inductance is limited.

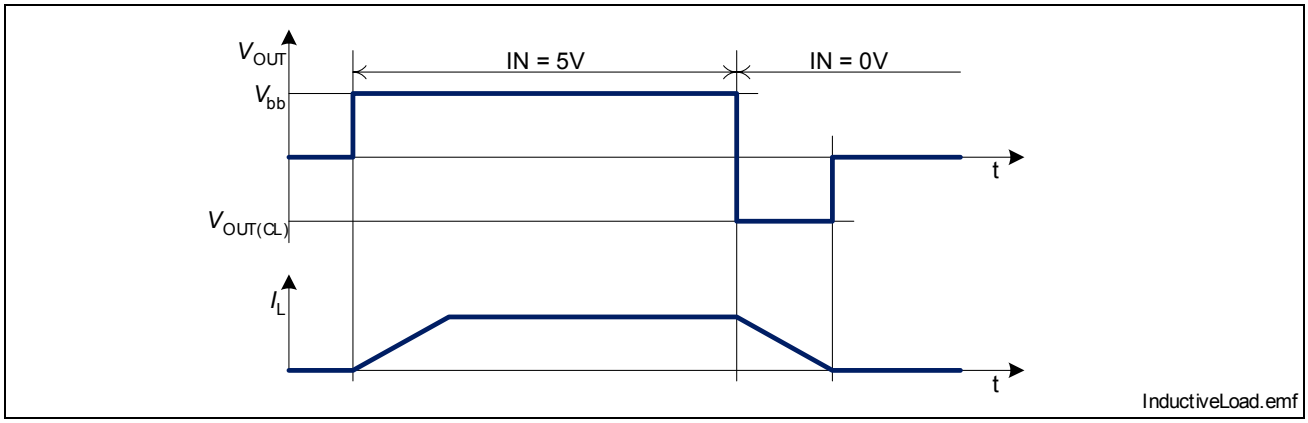


Figure 8 Switching an Inductance

Maximum Load Inductance

While demagnetization of inductive loads, energy has to be dissipated in the BTS 5242-2L. This energy can be calculated with following equation:

$$E = (V_{bb} - V_{OUT(CL)}) \cdot \left[\frac{V_{OUT(CL)}}{R_L} \cdot \ln\left(1 - \frac{R_L \cdot I_L}{V_{OUT(CL)}}\right) + I_L \right] \cdot \frac{L}{R_L}$$

Following equation simplifies under the assumption of $R_L = 0$:

$$E = \frac{1}{2} L I_L^{\,2} \cdot \left(1 - \frac{V_{bb}}{V_{OUT(CL)}}\right)$$

The energy, which is converted into heat, is limited by the thermal design of the component. See **Figure 9** for the maximum allowed energy dissipation.

To be added after characterization of first samples

Figure 9 Maximum energy dissipation single pulse, $T_{j,Start}$ = 150°C

4.1.4 Electrical Characteristics

V_{bb} = 9 V to 16 V, T_j = -40 °C to +150 °C (unless otherwise specified)
typical values: V_{bb} = 13.5 V, T_j = 25 °C

Pos.	Parameter	Symbol	Limit Values			Unit	Test Conditions
			min.	typ.	max.		
General							
4.1.1	Operating voltage	V_{bb}	4.5		28	V	V_{IN} = 4.5 V R_L = 12 Ω V_{DS} < 0.5 V
4.1.2	Operating current one channel all channels	I_{GND}		 1.6 3.2	 4 8	mA	V_{IN} = 5 V
4.1.3	Standby current for whole device with load	$I_{bb(OFF)}$		 5	 7.5 7.5 20	µA	V_{IN} = 0 V V_{CLA} = 0 V V_{OUT} < $V_{OUT(OL)}$ T_j = 25°C T_j = 105°C T_j = 150°C
Output characteristics							
4.1.4	On-State resistance per channel	$R_{DS(ON)}$		 19 35	 25 48	mΩ	I_L = 5 A T_j = 25 °C T_j = 150 °C
4.1.5	Output voltage drop limitation at small load currents	$V_{DS(NL)}$		40		mV	I_L < 0.5 A
4.1.6	Nominal load current per channel one channel active two channels active	$I_{L(nom)}$	 5.5 4.1	 6 4.5		A	T_a = 85 °C T_j ≤ 150 °C [1) 2)]
	ISO load current per channel one channel active two channels active	$I_{L(ISO)}$	 13 13	 15 15		A	T_c = 85 °C V_{DS} = 0.5 V [2)]
4.1.7	Output clamp	$V_{OUT(CL)}$	-24	-20	-17	V	I_L = 40 mA
4.1.8	Output leakage current per channel	$I_{L(OFF)}$		1.5	8	µA	V_{IN} = 0 V

V_{bb} = 9 V to 16 V, T_j = -40 °C to +150 °C (unless otherwise specified)
typical values: V_{bb} = 13.5 V, T_j = 25 °C

Pos.	Parameter	Symbol	Limit Values			Unit	Test Conditions
			min.	typ.	max.		
Thermal Resistance							
4.1.9	Junction to case	R_{thjc}			1.8	K/W	
4.1.10	Junction to ambient one channel on all channels on	R_{thja}		 40 33		K/W	1)
Input characteristics							
4.1.11	Input resistance for pin IN	R_{IN}	2.0	3.5	5.5	kΩ	
4.1.12	L-input level for pin IN	$V_{IN(L)}$	-0.3		1.0	V	
4.1.13	H-input level for pin IN	$V_{IN(H)}$	2.4			V	
4.1.14	Hysteresis for pin IN	ΔV_{IN}		0.5		V	3)
4.1.15	L-input current for pin IN	$I_{IN(L)}$	3		40	µA	V_{IN} = 0.4 V
4.1.16	H-input current for pin IN	$I_{IN(H)}$	20	50	90	µA	V_{IN} = 5 V
Timings							
4.1.17	Turn-on time to 90% V_{bb}	t_{ON}		90	250	µs	R_L = 12 Ω V_{bb} = 13.5 V
4.1.18	Turn-off time to 10% V_{bb}	t_{OFF}		100	250	µs	R_L = 12 Ω V_{bb} = 13.5 V
4.1.19	slew rate 10% to 30% V_{bb}	dV/dt_{ON}	0.1	0.25	0.45	V/µs	R_L = 12 Ω V_{bb} = 13.5 V
4.1.20	slew rate 70% to 40% V_{bb}	$-dV/dt_{OFF}$	0.1	0.25	0.45	V/µs	R_L = 12 Ω V_{bb} = 13.5 V

1) Device mounted on PCB (50 mm x 50 mm x 1.5 mm epoxy, FR4) with 6 cm^2 copper heatsinking area (one layer, 70 µm thick) for V_{bb} connection. PCB is vertical without blown air.

2) Not subject to production test, parameters are calculated from $R_{DS(ON)}$ and R_{th}

3) Not subject to production test, specified by design

Note: Characteristics show the deviation of parameter at the given supply voltage and junction temperature. Typical values show the typical parameters expected from manufacturing.

4.2 Protection Functions

The device provides embedded protective functions. Integrated protection functions are designed to prevent IC destruction under fault conditions described in the target data sheet. Fault conditions are considered as “outside” normal operating range. Protection functions are neither designed for continuous nor repetitive operation.

4.2.1 Over Load Protection

The load current I_{OUT} is limited by the device itself in case of over load or short circuit to ground. There are two steps of current limitation. They can be selected by the CLA pin, but are additionally selected automatically depending on the voltage V_{DS} across the power DMOS. Please note that the voltage at the OUT pin is V_{bb} - V_{DS}. Please refer to following figure for details.

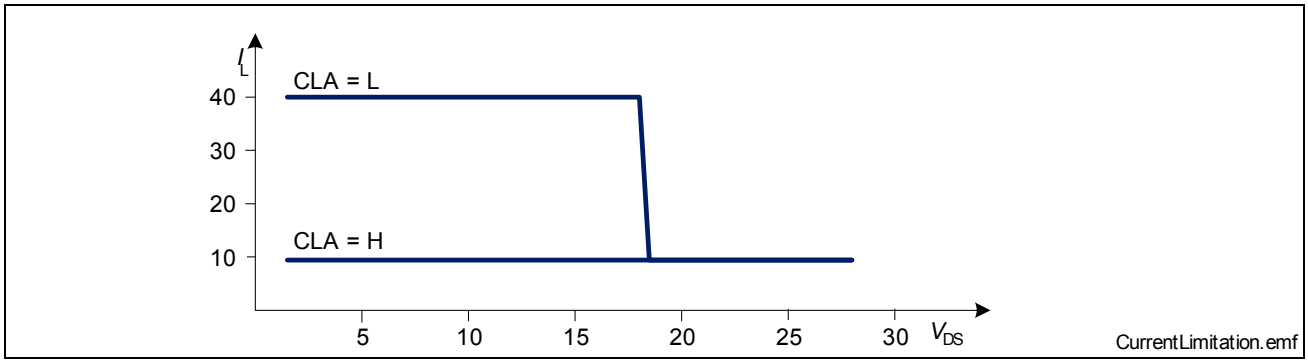


Figure 10 Current Limitation (minimum values)

Current limitation is realized by increasing the resistance of the device which leads to rapid temperature rise inside. A temperature sensor for each channel causes an overheated channel to switch off to prevent destruction. After cooling down with thermal hysteresis, the channel switches on again. Please refer to **Figure 11** for details.

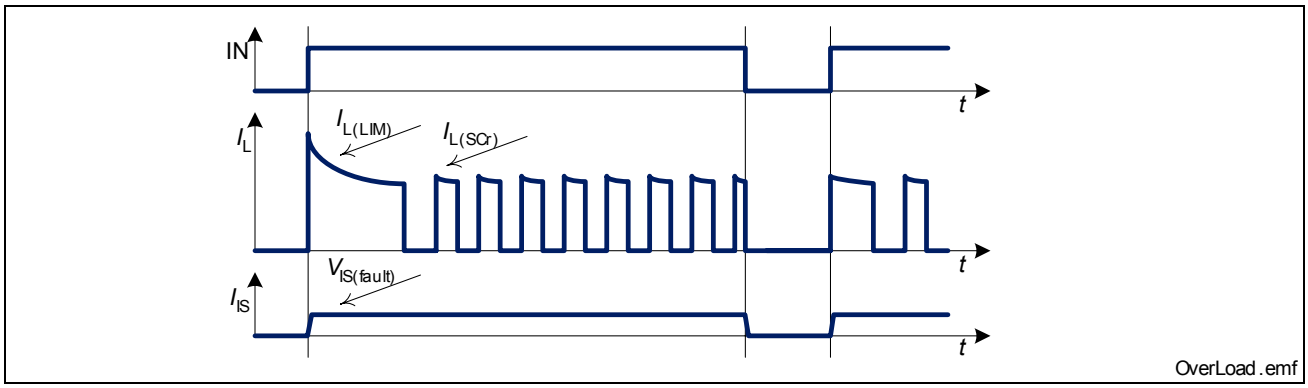


Figure 11 Shut Down by Over Temperature

The CLA pin circuit is designed equal to the input pin. Please refer to **Figure 5** for details. Please note that the thresholds for high and low state differ between IN and CLA.

4.2.2 Reverse Polarity Protection

In case of reverse polarity, the intrinsic body diode causes power dissipation. Use following fomular for estimation of total power dissipation $P_{diss(rev)}$ in reverse polarity mode.

$$P_{diss(rev)} = \sum_{\text{all channels}} (V_{DS(rev)} \cdot I_L)$$

The reverse current through the power transistors has to be limited by the connected loads. The reverse current through the ground connection has to be limited either by a resistor or by a pair of resistor and diode. The current through sense pins IS1 and IS2 has to be limited (please refer to maximum ratings on **Page 8**). The temperature protection is not active during reverse polarity.

4.2.3 Over Voltage Protection

In addition to the output clamp for inductive loads as described in **Section 4.1.3**, there is a clamp mechanism for over voltage protection. The current through the ground connection has to be limited e.g. by a resistor.

As shown in **Figure 12**, in case of supply voltages greater than $V_{bb(AZ)}$, the power transistor opens and the voltage across logic part is clamped. As a result, the ground potential rises to V_{bb} - $V_{bb(AZ)}$. Due to the ESD zener diodes, the potential at pin IN1, IN2 and CLA rises almost to that potential, depending on the impedance of the connected circuitry.

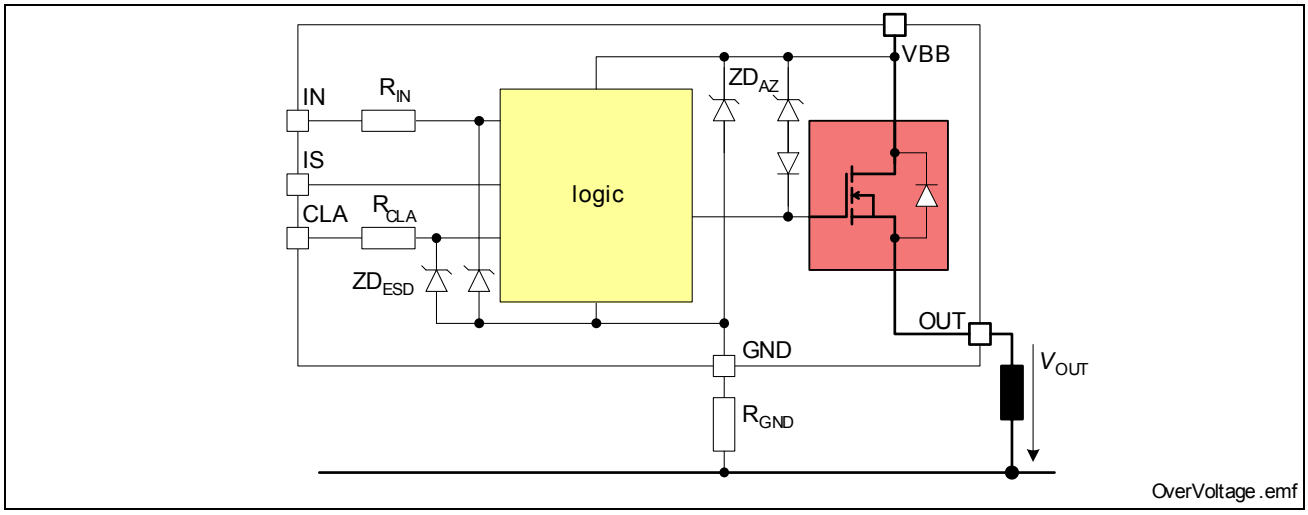


Figure 12 Over Voltage Protection

4.2.4 Loss of Ground Protection

In case of complete loss of the device ground connections, but connected load ground, the BTS 5242-2L securely changes to or stays in off state.

4.2.5 Electrical Characteristics

V_{bb} = 9 V to 16 V, T_j = -40 °C to +150 °C (unless otherwise specified)
typical values: V_{bb} = 13.5 V, T_j = 25 °C

Pos.	Parameter	Symbol	Limit Values			Unit	Test Conditions
			min.	typ.	max.		
Over Load Protection							
4.2.1	Load current limitation	$I_{L(LIM)}$	40 7	50 11	60 14	A	V_{DS} = 5 V CLA = 2 V CLA = 4 V
4.2.2	Repetitive short circuit current limitation	$I_{L(SCr)}$		40 7		A	$T_j = T_{j(SC)}$ 1) CLA = 0 V CLA = 5 V
4.2.3	Initial short circuit shut down time	$t_{OFF(SC)}$		0.8 4		ms	T_{jStart} = 25 °C 1) CLA = 0 V CLA = 5 V
4.2.4	Thermal shut down temperature	$T_{j(SC)}$	150	170 1)		°C	
4.2.5	Thermal hysteresis	ΔT_j		10		K	- 1)
Reverse Battery							
4.2.6	Drain-Source diode voltage ($V_{OUT} > V_{bb}$)	$-V_{DS(rev)}$			900	mV	I_L = -5 A T_j =150 °C
Over Voltage							
4.2.7	Over voltage protection	$V_{bb(AZ)}$	41	47	52	V	I_{bb} = 2 mA
Loss of GND							
4.2.8	Output current while GND disconnected	$I_{L(GND)}$			2	mA	I_{IN} = 0 1) 2) I_{GND} = 0 I_{IS} = 0
Current Limit Adjust (CLA)							
4.2.9	Input resistance for pin CLA	R_{CLA}	2.0	3.5	5.5	kΩ	
4.2.10	L-input level for pin CLA	$V_{CLA(L)}$	-0.3		2.0	V	
4.2.11	H-input level for pin CLA	$V_{CLA(H)}$	4.0			V	

V_{bb} = 9 V to 16 V, T_j = -40 °C to +150 °C (unless otherwise specified)
typical values: V_{bb} = 13.5 V, T_j = 25 °C

Pos.	Parameter	Symbol	Limit Values			Unit	Test Conditions
			min.	typ.	max.		
4.2.12	L-input current for pin CLA	$I_{CLA(L)}$	3		40	µA	V_{CLA} = 0.4 V
4.2.13	H-input current for pin CLA	$I_{CLA(H)}$	20	50	90	µA	V_{CLA} = 5 V

1) Not subject to production test, specified by design

2) no connection at these pins

4.3 Diagnosis

For diagnosis purpose, the BTS 5242-2L provides an IntelliSense signal at pins IS1 and IS2. This means in detail, the current sense signal I_{IS}, a proportional signal to the load current (ratio $k_{ILIS} = I_L / I_{IS}$), is provided as long as no failure mode (see **Table 1**) occurs. In case of a failure mode, the voltage $V_{IS(fault)}$ is fed to the diagnosis pin.

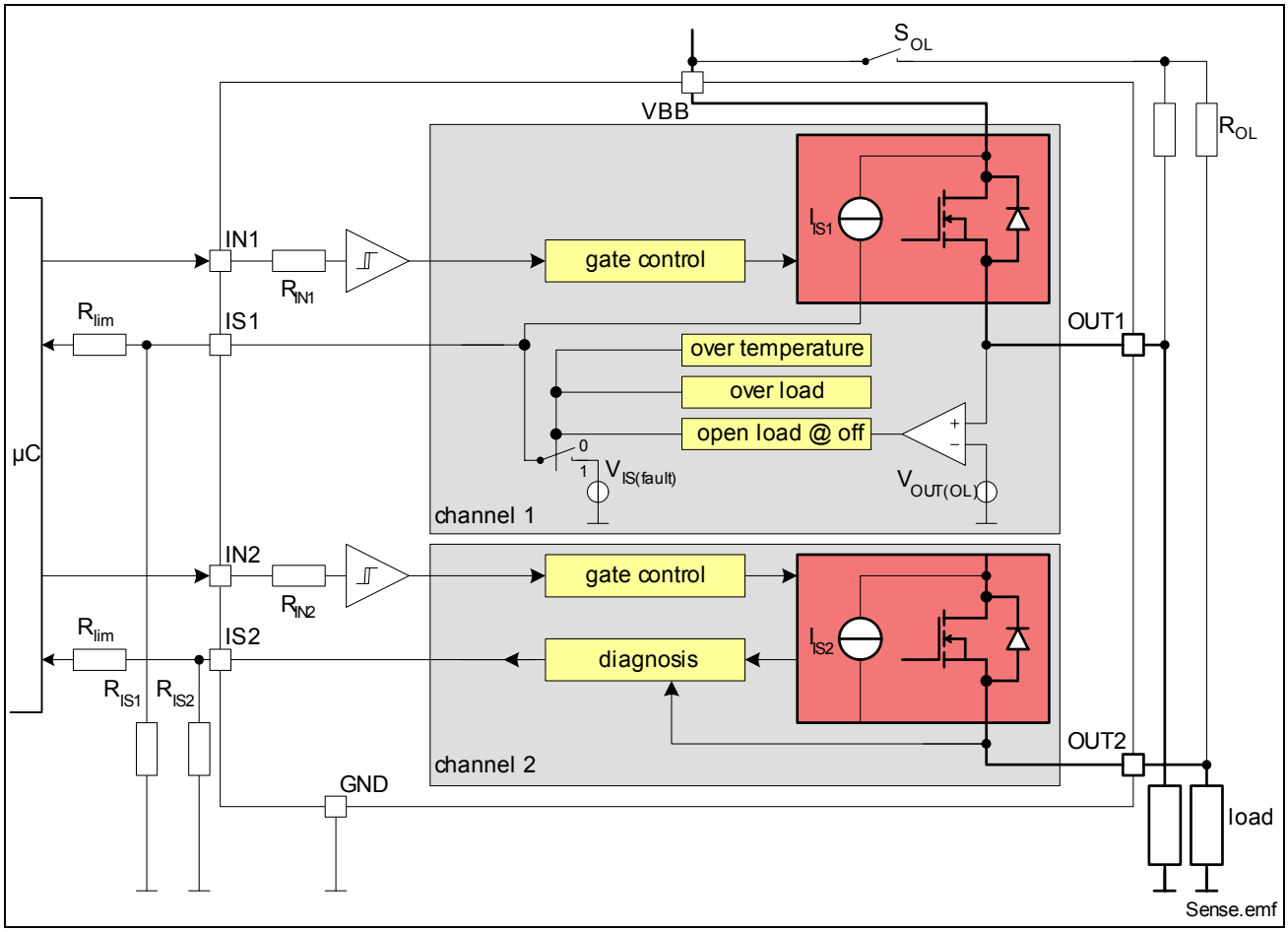


Figure 13 Block Diagram: Diagnosis

Table 1 Truth Table

Operation Mode	Input Level	Output Level	Diagnostic Output
Normal Operation (OFF)	L	Z	Z
Short Circuit to GND		Z	Z
Over Temperature		Z	Z
Short Circuit to V_{bb}		V_{bb}	$V_{IS} = V_{IS(fault)}$
Open Load		$< V_{OUT(OL)}$ $> V_{OUT(OL)}$	Z $V_{IS} = V_{IS(fault)}$

Table 1 Truth Table

Operation Mode	Input Level	Output Level	Diagnostic Output
Normal Operation (ON)	H	$\sim V_{bb}$	$I_{IS} = I_L / k_{ILIS}$
Current Limitation		$< V_{bb}$	$V_{IS} = V_{IS(fault)}$
Short Circuit to GND		~GND	$V_{IS} = V_{IS(fault)}$
Over Temperature		Z	$V_{IS} = V_{IS(fault)}$
Short Circuit to V_{bb}		V_{bb}	$I_{IS} < I_L / k_{ILIS}$
Open Load		$\sim V_{bb}$	Z

L = Low Level, H = High Level, Z = high impedance, potential depends on external circuit

4.3.1 ON-State Diagnosis

The standard diagnosis signal is a current sense signal proportional to the load current. The accuracy of the ratio ($k_{ILIS} = I_L / I_{IS}$) depends on the temperature. Please refer to **Figure 14** for details. Usually a resistor R_{IS} is connected to the current sense pin. It is recommended to use sense resistors $R_{IS} > 500\ \Omega$. A typical value is 4.7 kΩ

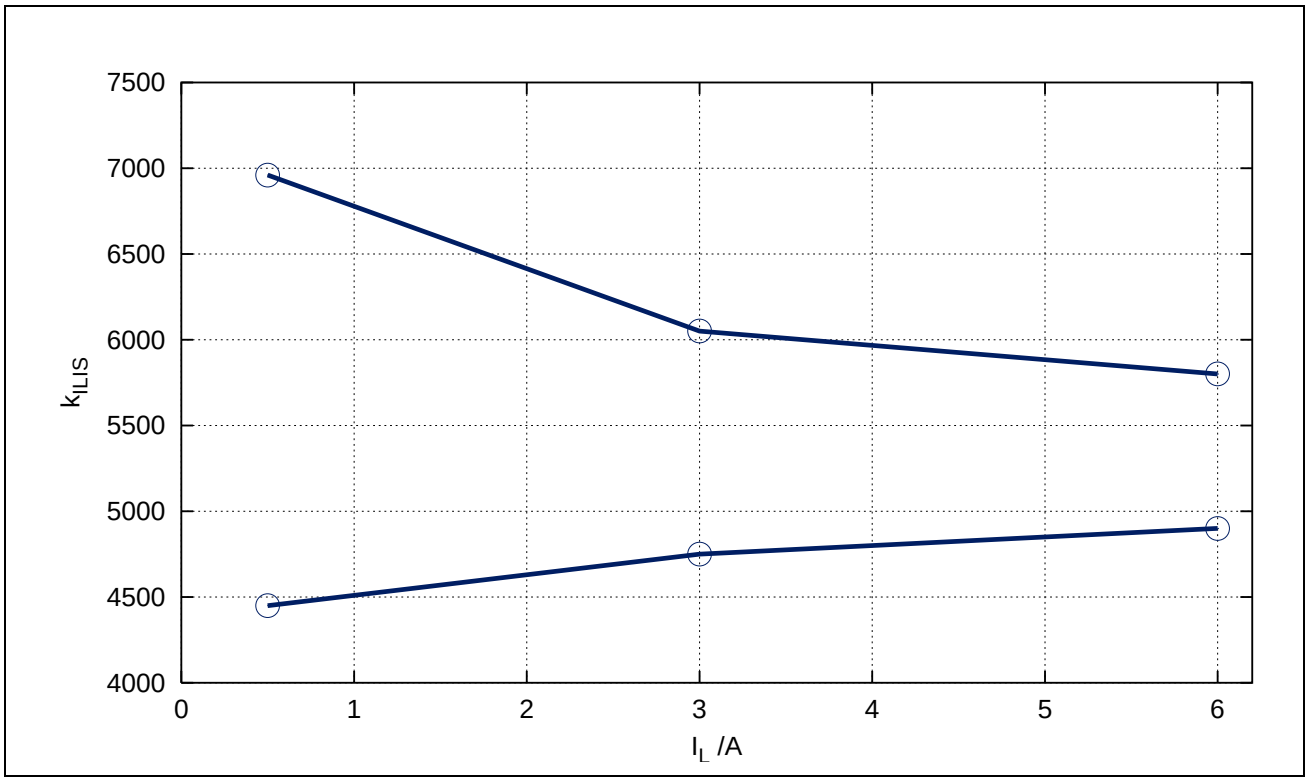


Figure 14 Current sense ratio k_{ILIS}[1)]

[1)] The curves show the behavior based on characterization data. The marked points are guaranteed in this Target Data Sheet in **Section 4.3.3** (Position **4.3.7**).

Details about timings between the diagnosis signal I_{IS} and the output voltgage V_{OUT} and the load current I_L in ON-state can be found in **Figure 15**.

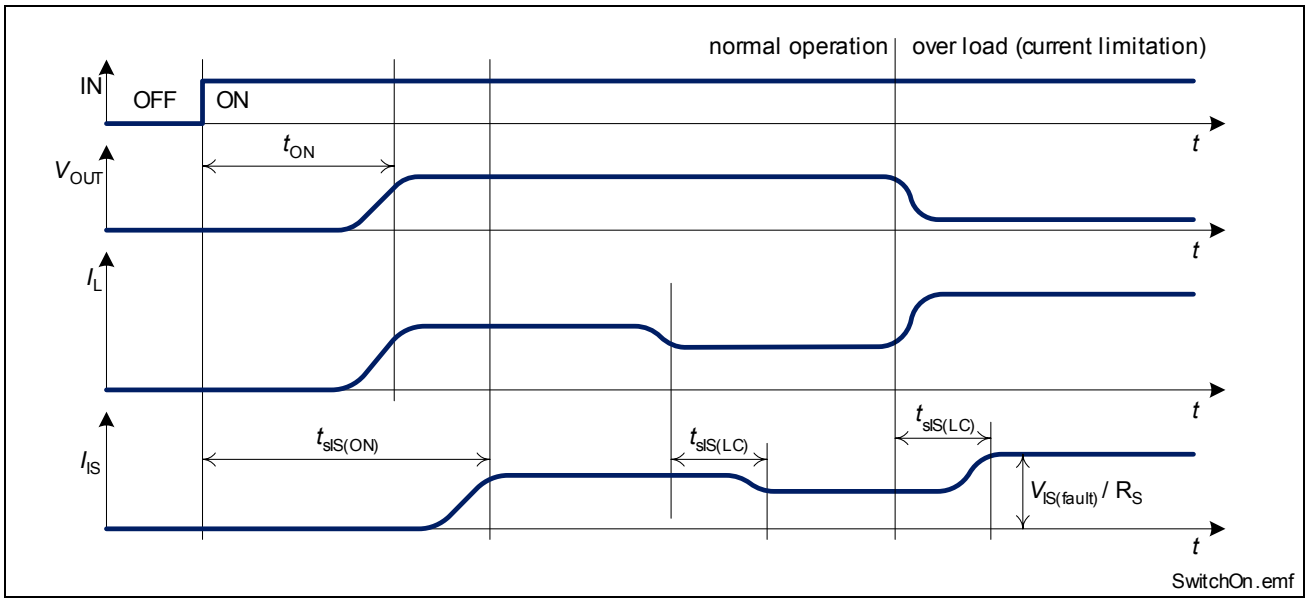


Figure 15 Timing of Diagnosis Signal in ON-state

In case of over-current as well as over-temperature, the voltage $V_{IS(fault)}$ is fed to the diagnosis pins as long as the according input pin is high. This means, even when the device keeps switching on and off in over-load condition, the failure signal is constantly available. Please refer to **Figure 16** for details.

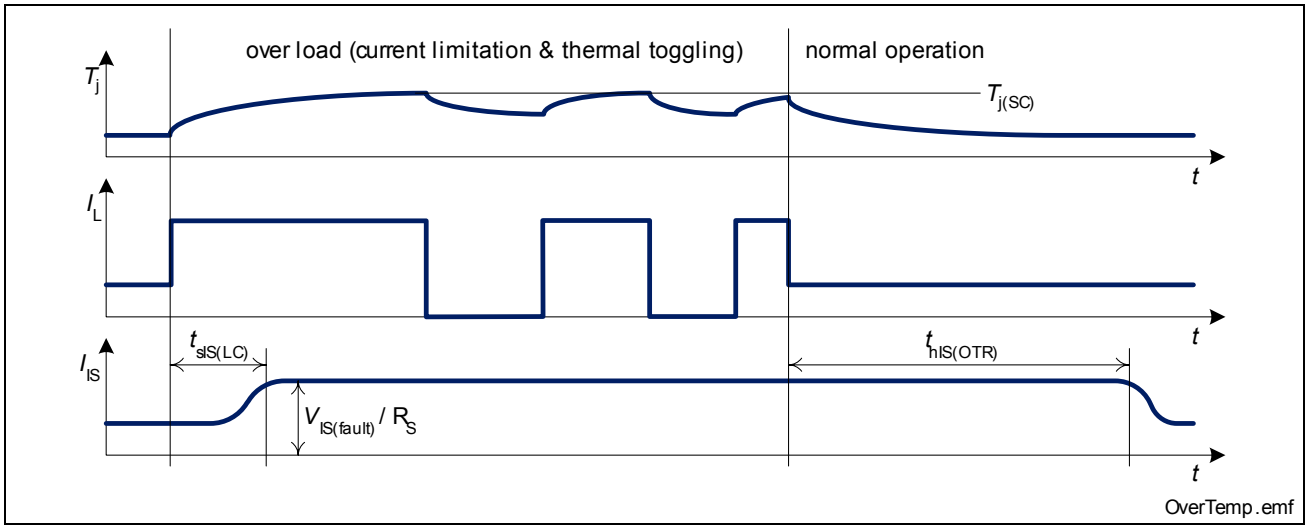


Figure 16 Timing of Diagnosis Signal in Over Load Condition

4.3.2 OFF-State Diagnosis

Details about timings between the diagnosis signal I_{IS} and the output voltgage V_{OUT} and the load current I_L in OFF-state can be found in **Figure 17**.

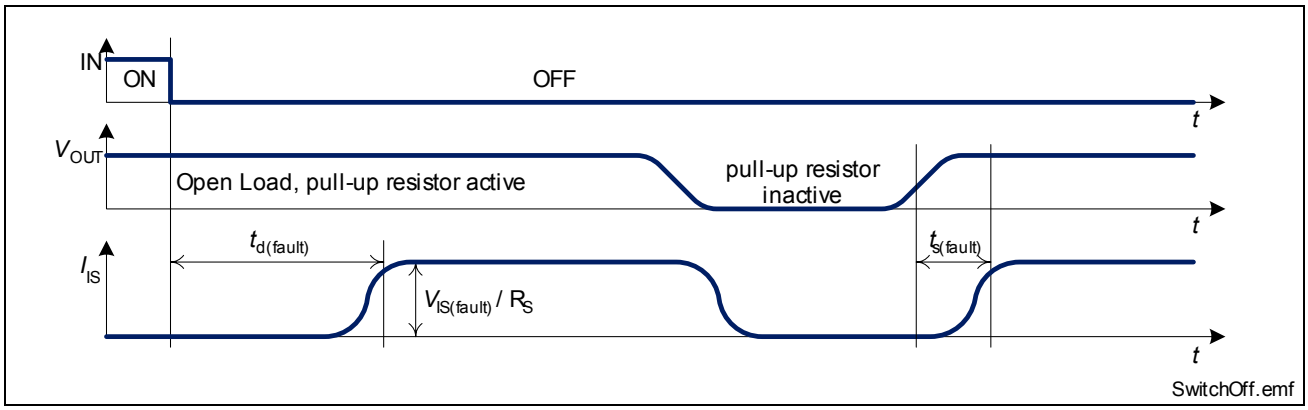


Figure 17 Timing of Diagnosis Signal in OFF-state

For open load diagnosis in off-state an external output pull-up resistor (R_{OL}) is recommended. For caluclation of pull-up resistor, the leakage currents and the open load threshold voltage $V_{OUT(OL)}$ has to be taken into account.

$$R_{OL} = \frac{V_{bb(min)} - V_{OUT(OL,max)}}{I_{leakage}}$$

$I_{leakage}$ defines the leakage current in the complete system including $I_{L(OL)}$ and external leakages e.g. due to humidity. $V_{bb(min)}$ is the minimum supply voltage at which the open load diagnosis in off-state must be ensured.

To reduce the stand-by current of the system, an open load resistor switch (S_{OL}) is recommended. The stand-by current of the BTS 5242-2L is minimized, when both input pins (IN1 and IN2) are on low level or left open and $V_{OUT} < V_{OUT(OL)}$. In case of open load in off state ($V_{OUT} > V_{OUT(OL)}$ and $V_{IN} = 0$ V), the fault voltage $V_{IS(fault)}$ drives a current through the sense resistor, which causes an increase in supply current. To reduce the stand-by current to a minimum, the open load condition needs to be suppressed.

The resistors R_{lim} are recommended to limit the current through the sense pins IS1 and IS2 in case of reverse polarity and over voltage.

4.3.3 Electrical Characteristics

V_{bb} = 9 V to 16 V, T_j = -40 °C to +150 °C (unless otherwise specified)
typical values: V_{bb} = 13.5 V, T_j = 25 °C

Pos.	Parameter	Symbol	Limit Values			Unit	Test Conditions
			min.	typ.	max.		
Open Load at OFF state							
4.3.1	Open load detection threshold voltage	$V_{OUT(OL)}$	2.0	3.2	4.4	V	
4.3.2	Leakage current into OUT	$-I_{L(OL)}$			1	µA	V_{OUT} = 5 V
4.3.3	Sense signal in case of open load	$V_{IS(fault)}$	5.0	6.2	8	V	V_{IN} = 0 V $V_{OUT} > V_{OUT(OL)}$ I_{IS} = 1 mA
4.3.4	Sense signal current limitation	$I_{IS(LIM)}$	4			mA	V_{IS} = 0 V V_{IN} = 0 V $V_{OUT} > V_{OUT(OL)}$
4.3.5	Sense signal invalid after negative input slope	$t_{d(fault)}$			1.2	ms	V_{IN} = 5 V to 0 V $V_{OUT} > V_{OUT(OL)}$
4.3.6	Fault signal settling time	$t_{s(fault)}$			200	µs	V_{IN} = 0 V [1)] V_{OUT} = 0 V to > $V_{OUT(OL)}$ I_{IS} = 1 mA
Load Current Sense							
4.3.7	Current sense ratio I_L = 0.5 A I_L = 3.0 A I_L = 6.0 A	k_{ILIS}	 4450 4750 4900	 5800 5400 5350	 6960 6050 5800		V_{IN} = 5 V
4.3.8	Current sense voltage limitation	$V_{IS(LIM)}$	5.4	6.5	7.5	V	I_L = 5 A
4.3.9	Current sense leakage/ offset current	$I_{IS(LH)}$			5	µA	V_{IN} = 5 V I_L = 0 A
4.3.10	Current sense settling time to I_{IS} static ±10% after positive input slope	$t_{sIS(ON)}$			400	µs	V_{IN} = 0 V to 5 V I_L = 5 A [1)]

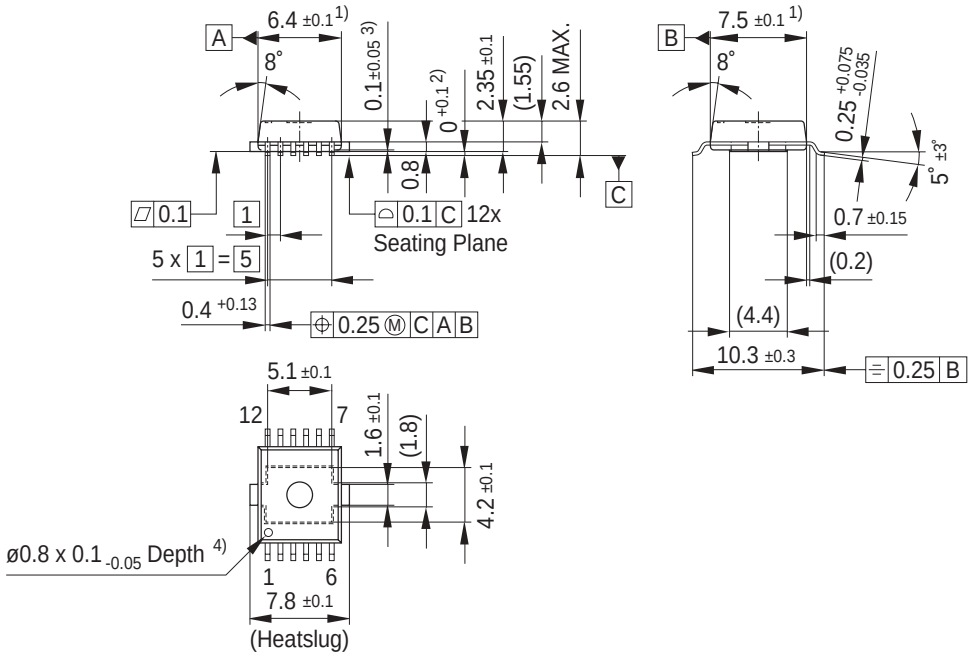
V_{bb} = 9 V to 16 V, T_j = -40 °C to +150 °C (unless otherwise specified)
typical values: V_{bb} = 13.5 V, T_j = 25 °C

Pos.	Parameter	Symbol	Limit Values			Unit	Test Conditions
			min.	typ.	max.		
4.3.11	Current sense settling time to I_{IS} static ±10% after change of load current	$t_{sIS(LC)}$			300	µs	V_{IN} = 5 V I_L = 3 A to 5 A [1]
4.3.12	Fault signal hold time after thermal restart	$t_{hIS(OTR)}$			1.2	ms	[1]

[1] Not subject to production test, specified by design

5 Package Outlines BTS 5242-2L

PG-DSO-12-9
(Plastic Dual Small Outline Package)



1) Does not include plastic or metal protrusion of 0.15 max. per side
2) Stand OFF
3) Stand OUT
4) Pin 1 Index Marking; Polish finish
All package corners max. R 0.25

green Product

To meet the world-wide customer requirements for environmentally friendly products and to be compliant with government regulations the device is available as a green product. Green products are RoHS-Compliant (i.e Pb-free finish on leads and suitable for Pb-free soldering according to IPC/JEDEC J-STD-020)

Please specifiy the package needed (e.g green package) when placing an order.

You can find all of our packages, sorts of packing and others in our Infineon Internet Page “Products”: http://www.infineon.com/products.

SMD = Surface Mounted Device

Dimensions in mm

6 Revision History

Version	Date	Changes
V1.2	2006-08-14	Creation of the green target datasheet. Delta sheet to the grey datasheet BTS5242L datasheet of October the 29th, 2004 Parameter 3.16 : change to 130mJ with 12V battery Figure 9 set to tbd Parameter 4.1.7 : .24V min, -17V max

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