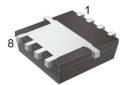


### PDFN56



Pin Definition:1. Source8. Drain2. Source7. Drain3. Source6. Drain4. Gate5. Drain

### **Key Parameter Performance**

Parameter	Value	Unit
V <sub>DS</sub>	100	V
R <sub>DS(on)</sub> (max)	12	mΩ
Qg	145	nC

#### **Block Diagram**

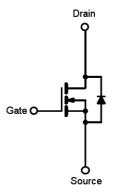
Features

- Low On-Resistance
- Low Input Capacitance
- Low Gate Charge

#### **Ordering Information**

Part No.	Package	Packing			
TSM120N10PQ56 RLG	PDFN56	2.5kpcs / 13" Reel			

**Note:** "G" denotes for Halogen- and Antimony-free as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.



N-Channel MOSFET

#### Absolute Maximum Ratings (Tc=25°C unless otherwise noted)

Parameter		Symbol	Limit	Unit	
Drain-Source Voltage		V <sub>DS</sub>	100	V	
Gate-Source Voltage		V <sub>GS</sub>	±20	V	
Continuous Drain Current (Note 3)	T <sub>C</sub> =25°C		58	А	
	T <sub>A</sub> =25°C	- I <sub>D</sub>	16.1		
Drain Current-Pulsed (Note 1)		I <sub>DM</sub>	150	А	
Single Pulse Avalanche Energy L=0.5mH		E <sub>AS</sub>	156	mJ	
Maximum Power Dissipation (Note 2)	T <sub>C</sub> =25°C		36	W	
	T <sub>A</sub> =25°C	– P <sub>D</sub>	2		
Storage Temperature Range		T <sub>STG</sub>	-55 to +150	°C	
Operating Junction Temperature Range		TJ	-55 to +150	°C	

#### **Thermal Performance**

Parameter	Symbol	Limit	Unit
Thermal Resistance - Junction to Case	R <sub>eJC</sub>	1.2	°C/W
Thermal Resistance - Junction to Ambient	$R_{\Theta JA}$	62	°C/W



#### Electrical Specifications (T<sub>J</sub>=25°C unless otherwise noted)

Parameter	Conditions	Symbol	Min	Тур	Max	Unit
Static				•		
Drain-Source Breakdown Voltage	$V_{GS} = 0V, I_D = 250\mu A$	BV <sub>DSS</sub>	100			V
Drain-Source On-State Resistance	$V_{GS} = 10V, I_D = 30A$	R <sub>DS(ON)</sub>		10	12	mΩ
Gate Threshold Voltage	$V_{DS} = V_{GS}, I_D = 250 \mu A$	V <sub>GS(TH)</sub>	2	3	4	V
Zero Gate Voltage Drain Current	$V_{DS} = 80V, V_{GS} = 0V$	I <sub>DSS</sub>			1	μA
Gate Body Leakage	$V_{GS} = \pm 20V, V_{DS} = 0V$	I <sub>GSS</sub>			±100	nA
Dynamic					•	
Total Gate Charge	$V_{DS} = 50V, I_D = 30A,$	Qg		145		nC
Gate-Source Charge		Q <sub>gs</sub>		25		
Gate-Drain Charge	V <sub>GS</sub> = 10V	$Q_{gd}$		43		
Input Capacitance	$V_{DS} = 30V, V_{GS} = 0V,$ f = 1.0MHz	C <sub>iss</sub>		3902		
Output Capacitance		C <sub>oss</sub>		251		pF
Reverse Transfer Capacitance		C <sub>rss</sub>		93		1
Switching					•	
Turn-On Delay Time		t <sub>d(on)</sub>		27		
Turn-On Rise Time	$V_{GS} = 10V, V_{DS} = 50V,$	t <sub>r</sub>		13		
Turn-Off Delay Time	$R_{\rm G} = 3\Omega, I_{\rm D} = 30A$	t <sub>d(off)</sub>		15		ns
Turn-Off Fall Time		t <sub>f</sub>		42		
Drain-Source Diode Characteristic	s and Maximum Rating	•		•		
Drain-Source Diode Forward Voltage	V <sub>GS</sub> =0V, I <sub>S</sub> =30A	$V_{SD}$			1.3	V
Reverse Recovery Time		t <sub>rr</sub>		65		ns
Reverse Recovery Charge	I <sub>S</sub> = 30A, dl/dt = 100A/μs	Q <sub>rr</sub>		175		nC

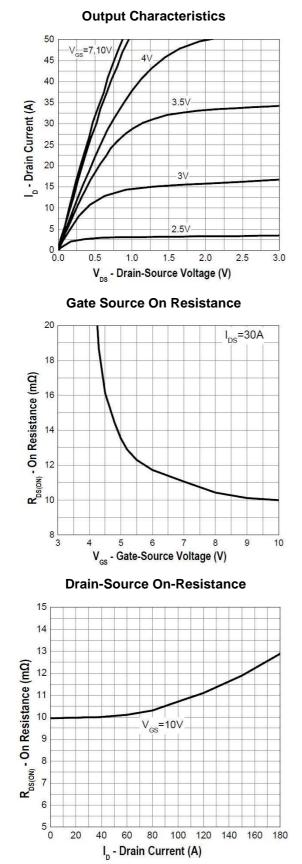
1. Pulse Test: Pulse Width  $\leq$  300µs, Duty Cycle  $\leq$  2%.

2.  $R_{\Theta JA}$  is the sum of the junction-to-case and case-to-ambient thermal resistances. The case thermal reference is defined at the solder mounting surface of the drain pins.  $R_{\Theta JA}$  is guaranteed by design while  $R_{\Theta CA}$  is determined by the user's board design.  $R_{\Theta JA}$  shown below for single device operation on FR-4 PCB in still air

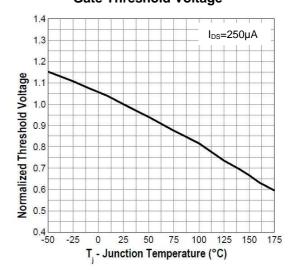
3. The maximum current is limited by package.



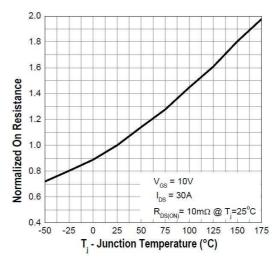
#### **Electrical Characteristics Curves**



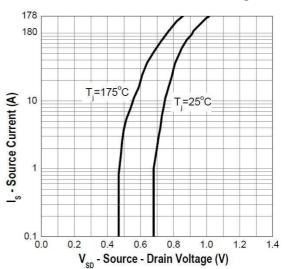
Gate Threshold Voltage



**Drain-Source On Resistance** 

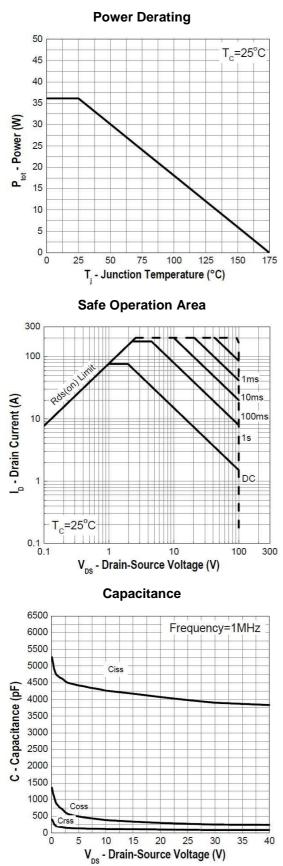


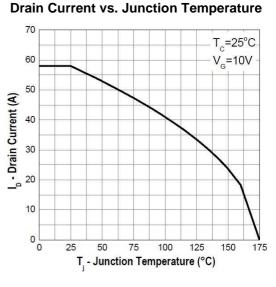
Source-Drain Diode Forward Voltage



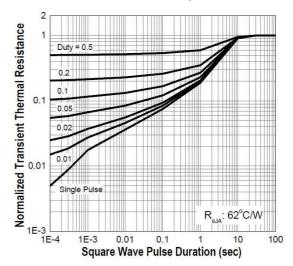


#### **Electrical Characteristics Curves**

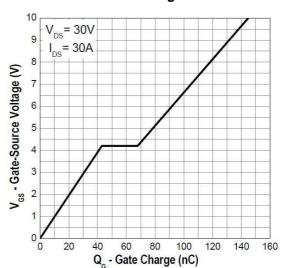




**Transient Thermal Impedance** 

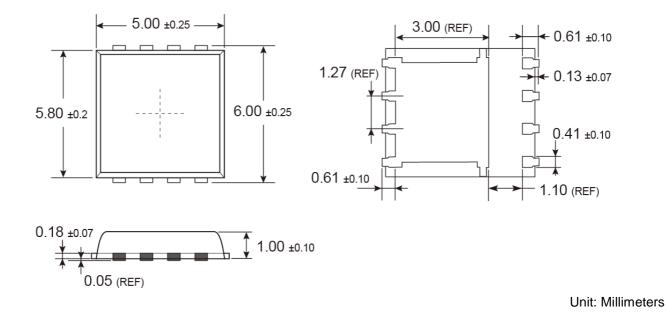


**Gate Charge** 





# **PDFN56 Mechanical Drawing**



### **Marking Diagram**



- Y = Year Code
- M = Month Code for Halogen Free Product
  (O=Jan, P=Feb, Q=Mar, R=Apl, S=May, T=Jun, U=Jul, V=Aug, W=Sep, X=Oct, Y=Nov, Z=Dec)
- L = Lot Code



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