RoHS
Available on commercial versions

N-CHANNEL MOSFET

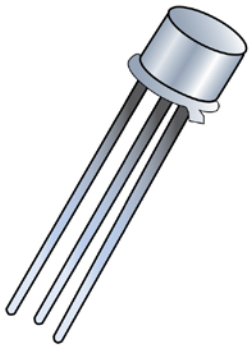
Qualified per MIL-PRF-19500/556

Qualified Levels:
JAN, JANTX, and JANTXV

DESCRIPTION

This family of 2N6782, 2N6784 and 2N6786 switching transistors are military qualified up to the JANTXV level for high-reliability applications. These devices are also available in a low profile U-18 LCC surface mount package. Microsemi also offers numerous other transistor products to meet higher and lower power ratings with various switching speed requirements in both through-hole and surface-mount packages.

Important: For the latest information, visit our website http://www.microsemi.com.



TO-205AF (TO-39) Package

FEATURES

- JEDEC registered 2N6782, 2N6784 and 2N6786 number series.
- JAN, JANTX, and JANTXV qualifications are available per MIL-PRF-19500/556. (See part nomenclature for all available options.)
- RoHS compliant versions available (commercial grade only).

Also available in:

U-18 LCC package
(surface mount)
2N6782U & 2N6786U

APPLICATIONS / BENEFITS

- Lightweight top-hat design with flexible terminals offers a variety of mounting flexibility.
- Military and other high-reliability applications.

MAXIMUM RATINGS @ T_A = +25 ºC unless otherwise stated

Parameters / Test Conditions		Symbol	Value	Unit
Operating & Storage Junction Temperature Range		T_J & T_{stg}	-55 to +150	°C
Thermal Resistance Junction-to-Case		$R_{\Theta JC}$	8.33	°C/W
Total Power Dissipation	@ T_A = +25 °C @ T_C = +25 °C (1)	P_T	0.8 15	W
Drain-Source Voltage, dc	2N6782 2N6784 2N6786	V_{DS}	100 200 400	V
Gate-Source Voltage, dc		V_{GS}	± 20	V
Drain Current, dc @ T_C = +25 ºC (2)	2N6782 2N6784 2N6786	I_{D1}	3.50 2.25 1.25	A
Drain Current, dc @ T_C = +100 ºC (2)	2N6782 2N6784 2N6786	I_{D2}	2.25 1.50 0.80	A
Off-State Current (Peak Total Value) (3)	2N6782 2N6784 2N6786	I_{DM}	14.0 9.0 5.5	A (pk)
Source Current	2N6782 2N6784 2N6786	I_S	3.50 2.25 1.25	A

See notes on next page.

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Notes: 1. Derate linearly 0.12 W/°C for T_C > +25 °C.

2. The following formula derives the maximum theoretical I_D limit. I_D is also limited by package and internal wires and may be limited due to pin diameter.

$$I_D = \sqrt{\frac{T_J(max) - T_C}{R_{\theta JC} \times R_{DS(on)} @ T_J(max)}}$$

3. I_{DM} = 4 x I_{D1} as calculated in note 1.

MECHANICAL and PACKAGING

- CASE: Hermetically sealed, kovar base, nickel cap.
- TERMINALS: Tin/lead solder dip nickel plate or RoHS compliant pure tin plate (commercial grade only).
- MARKING: Part number, date code, manufacturer's ID.
- WEIGHT: Approximately 1.064 grams.
- See Package Dimensions on last page.

PART NOMENCLATURE

JAN 2N6782 (e3)

Reliability Level
JAN = JAN Level
JANTX = JANTX Level
JANTXV = JANTXV Level
Blank = Commercial

JEDEC type number
(see Electrical Characteristics table)

RoHS Compliance
e3 = RoHS compliant (available on commercial grade only)
Blank = non-RoHS compliant

SYMBOLS & DEFINITIONS

Symbol	Definition
di/dt	Rate of change of diode current while in reverse-recovery mode, recorded as maximum value.
I_F	Forward current
R_G	Gate drive impedance
V_{DD}	Drain supply voltage
V_{DS}	Drain source voltage, dc
V_{GS}	Gate source voltage, dc

ELECTRICAL CHARACTERISTICS @ T_A = +25 °C, unless otherwise noted

Parameters / Test Conditions		Symbol	Min.	Max.	Unit
OFF CHARACTERISTICS					
Drain-Source Breakdown Voltage					
V_{GS} = 0 V, I_D = 1.0 mA	2N6782 2N6784 2N6786	$V_{(BR)DSS}$	100 200 400		V
Gate-Source Voltage (Threshold)					
$V_{DS} \geq V_{GS}$, I_D = 0.25 mA		$V_{GS(th)1}$	2.0	4.0	V
$V_{DS} \geq V_{GS}$, I_D = 0.25 mA, T_J = +125 °C		$V_{GS(th)2}$	1.0		
$V_{DS} \geq V_{GS}$, I_D = 0.25 mA, T_J = -55 °C		$V_{GS(th)3}$		5.0	
Gate Current					
V_{GS} = ± 20 V, V_{DS} = 0 V		I_{GSS1}		±100	nA
V_{GS} = ± 20 V, V_{DS} = 0 V, T_J = +125 °C		I_{GSS2}		±200	
Drain Current					
V_{GS} = 0 V, V_{DS} = 80 V	2N6782				
V_{GS} = 0 V, V_{DS} = 160 V	2N6784	I_{DSS1}		25	µA
V_{GS} = 0 V, V_{DS} = 320 V	2N6786				
Drain Current					
V_{GS} = 0 V, V_{DS} = 80 V, T_J = +125 °C	2N6782				
V_{GS} = 0 V, V_{DS} = 160 V, T_J = +125 °C	2N6784	I_{DSS2}		0.25	mA
V_{GS} = 0 V, V_{DS} = 320 V, T_J = +125 °C	2N6786				
Static Drain-Source On-State Resistance					
V_{GS} = 10 V, I_D = 2.25 A pulsed	2N6782			0.60	
V_{GS} = 10 V, I_D = 1.50 A pulsed	2N6784	$r_{DS(on)1}$		1.50	Ω
V_{GS} = 10 V, I_D = 0.80 A pulsed	2N6786			3.60	
Static Drain-Source On-State Resistance					
V_{GS} = 10 V, I_D = 3.50 A pulsed	2N6782			0.61	
V_{GS} = 10 V, I_D = 2.25 A pulsed	2N6784	$r_{DS(on)2}$		1.60	Ω
V_{GS} = 10 V, I_D = 1.25 A pulsed	2N6786			3.70	
Static Drain-Source On-State Resistance					
T_J = +125 °C					
V_{GS} = 10 V, I_D = 2.25 A pulsed	2N6782			1.08	
V_{GS} = 10 V, I_D = 1.50 A pulsed	2N6784	$r_{DS(on)3}$		2.81	Ω
V_{GS} = 10 V, I_D = 0.80 A pulsed	2N6786			7.92	
Diode Forward Voltage					
V_{GS} = 0 V, I_D = 3.50 A pulsed	2N6782			1.5	
V_{GS} = 0 V, I_D = 2.25 A pulsed	2N6784	V_{SD}		1.5	V
V_{GS} = 0 V, I_D = 1.25 A pulsed	2N6786			1.4	

ELECTRICAL CHARACTERISTICS @ T_A = +25 °C, unless otherwise noted (continued)

DYNAMIC CHARACTERISTICS

Parameters / Test Conditions		Symbol	Min.	Max.	Unit
Gate Charge:					
On-State Gate Charge					
V_{GS} = 10 V, I_D = 3.50 A, V_{DS} = 50 V	2N6782	$Q_{g(on)}$		8.1	nC
V_{GS} = 10 V, I_D = 2.25 A, V_{DS} = 100 V	2N6784			8.6	
V_{GS} = 10 V, I_D = 1.25 A, V_{DS} = 200 V	2N6786			12	
Gate to Source Charge					
V_{GS} = 10 V, I_D = 3.50 A, V_{DS} = 50 V	2N6782	Q_{gs}		1.7	nC
V_{GS} = 10 V, I_D = 2.25 A, V_{DS} = 100 V	2N6784			1.5	
V_{GS} = 10 V, I_D = 1.25 A, V_{DS} = 200 V	2N6786			1.8	
Gate to Drain Charge					
V_{GS} = 10 V, I_D = 3.50 A, V_{DS} = 50 V	2N6782	Q_{gd}		4.5	nC
V_{GS} = 10 V, I_D = 2.25 A, V_{DS} = 100 V	2N6784			5.5	
V_{GS} = 10 V, I_D = 1.25 A, V_{DS} = 200 V	2N6786			7.6	

SWITCHING CHARACTERISTICS

Parameters / Test Conditions		Symbol	Min.	Max.	Unit
Turn-on delay time					
I_D = 3.50 A, V_{GS} = 10 V, R_G = 7.5 Ω, V_{DD} = 50 V	2N6782	$t_{d(on)}$		15	ns
I_D = 2.25 A, V_{GS} = 10 V, R_G = 7.5 Ω, V_{DD} = 100 V	2N6784				
I_D = 1.25 A, V_{GS} = 10 V, R_G = 7.5 Ω, V_{DD} = 200 V	2N6786				
Rinse time					
I_D = 3.50 A, V_{GS} = 10 V, R_G = 7.5 Ω, V_{DD} = 50 V	2N6782	t_r		25	ns
I_D = 2.25 A, V_{GS} = 10 V, R_G = 7.5 Ω, V_{DD} = 100 V	2N6784			20	
I_D = 1.25 A, V_{GS} = 10 V, R_G = 7.5 Ω, V_{DD} = 200 V	2N6786			20	
Turn-off delay time					
I_D = 3.50 A, V_{GS} = 10 V, R_G = 7.5 Ω, V_{DD} = 50 V	2N6782	$t_{d(off)}$		25	ns
I_D = 2.25 A, V_{GS} = 10 V, R_G = 7.5 Ω, V_{DD} = 100 V	2N6784			30	
I_D = 1.25 A, V_{GS} = 10 V, R_G = 7.5 Ω, V_{DD} = 200 V	2N6786			35	
Fall time					
I_D = 3.50 A, V_{GS} = 10 V, R_G = 7.5 Ω, V_{DD} = 50 V	2N6782	t_f		20	ns
I_D = 2.25 A, V_{GS} = 10 V, R_G = 7.5 Ω, V_{DD} = 100 V	2N6784			20	
I_D = 1.25 A, V_{GS} = 10 V, R_G = 7.5 Ω, V_{DD} = 200 V	2N6786			30	
Diode Reverse Recovery Time					
di/dt ≤ 100 A/µs, V_{DD} ≤ 50 V, I_F = 3.50 A	2N6782	t_{rr}		180	ns
di/dt ≤ 100 A/µs, V_{DD} ≤ 50 V, I_F = 2.25 A	2N6784			350	
di/dt ≤ 100 A/µs, V_{DD} ≤ 50 V, I_F = 1.25 A	2N6786			540	

GRAPHS

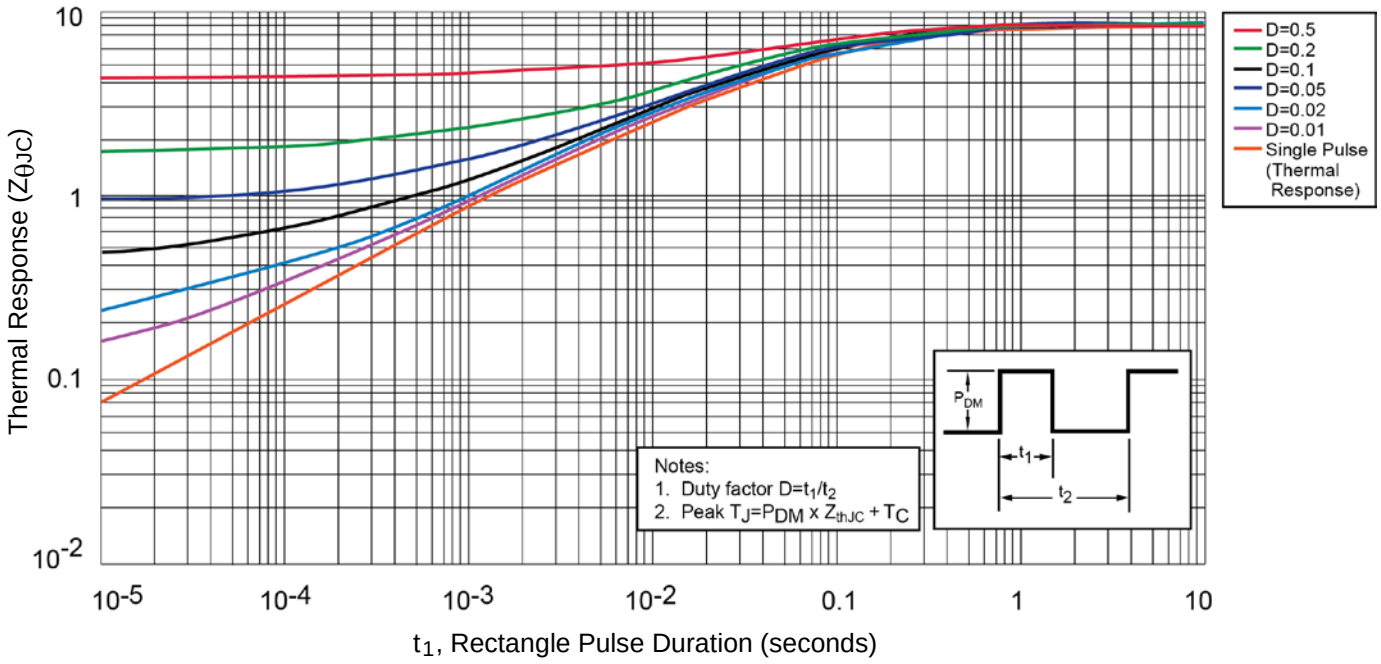
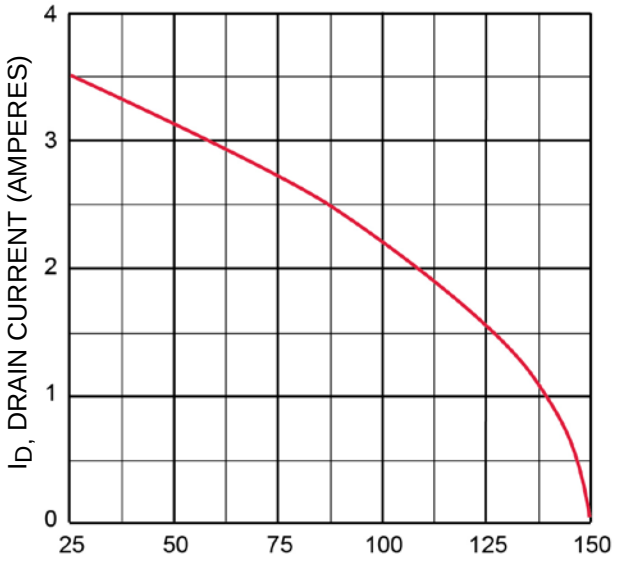


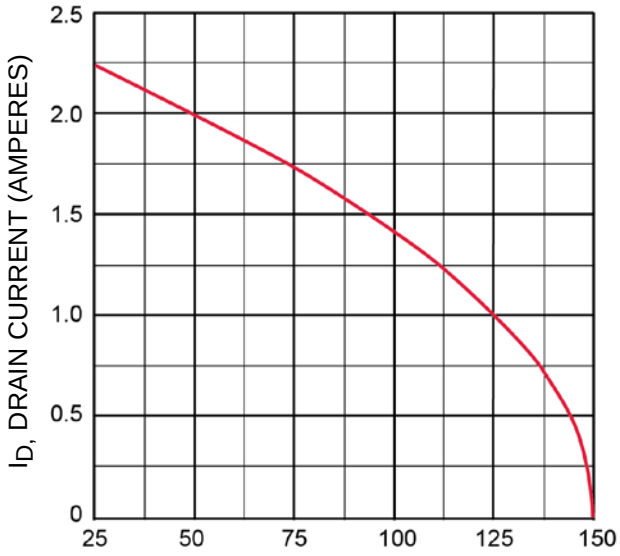
FIGURE 1
Thermal Response Curves

GRAPHS (continued)

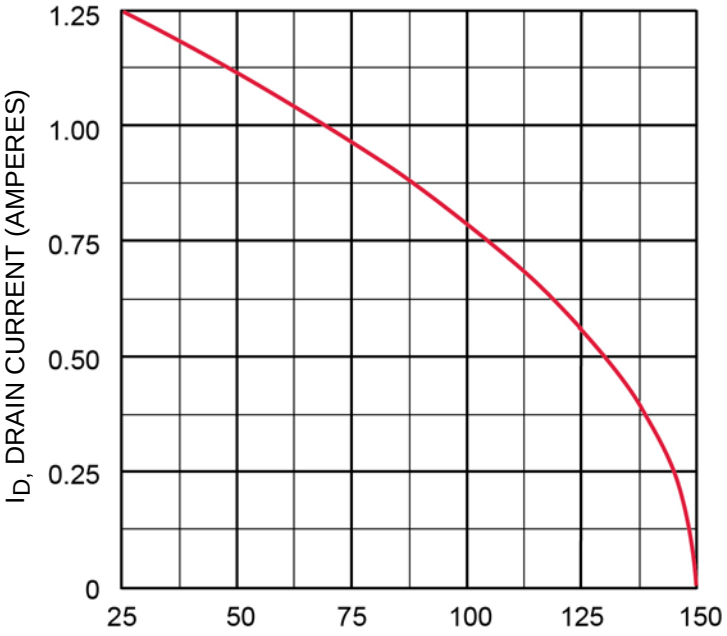
FIGURE 2 – Maximum Drain Current vs Case Temperature Graphs



For 2N6782



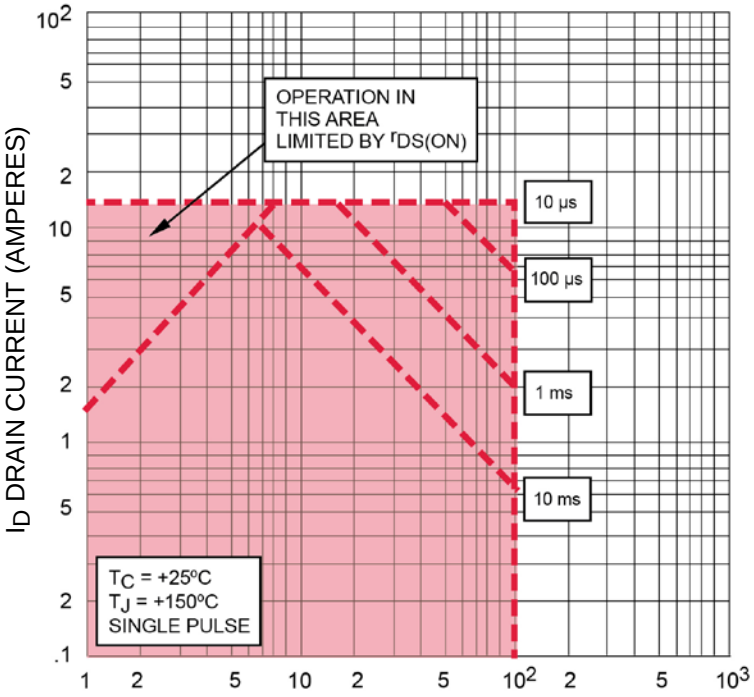
For 2N6784

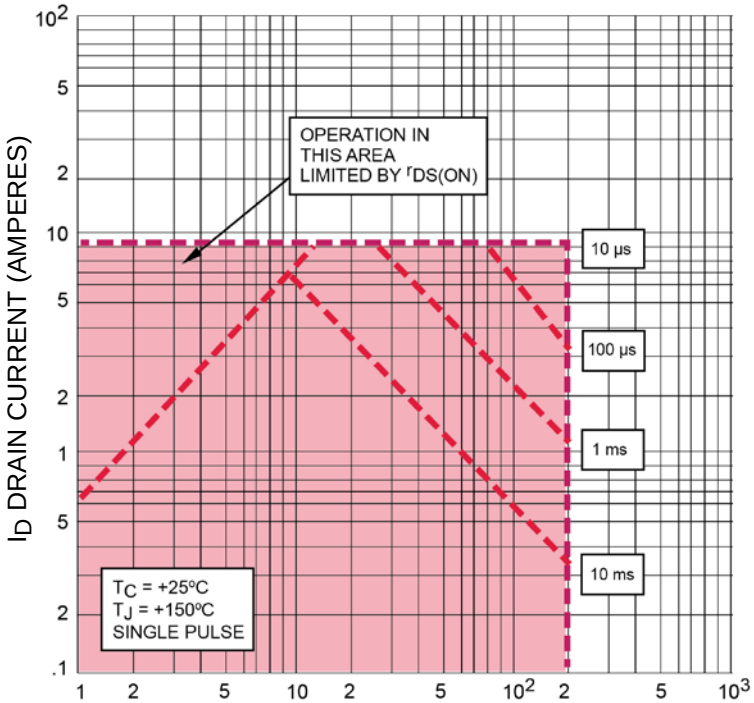


For 2N6786

GRAPHS (continued)

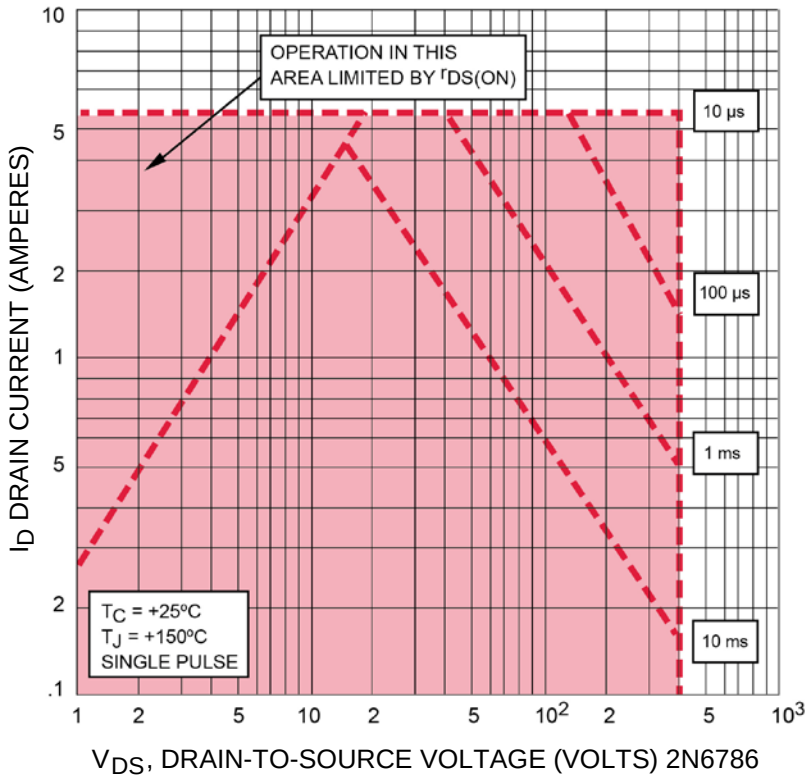
FIGURE 3 – Maximum Safe Operating Area



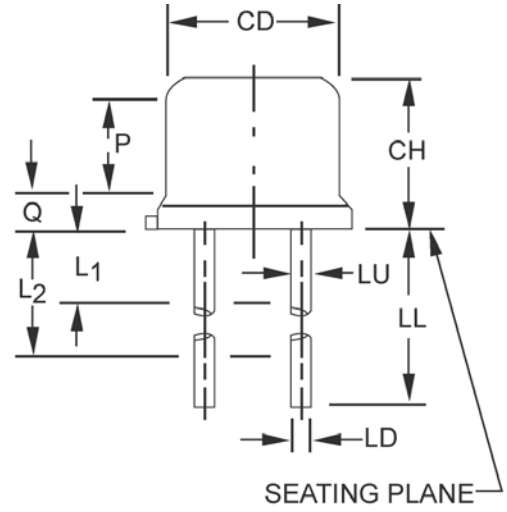


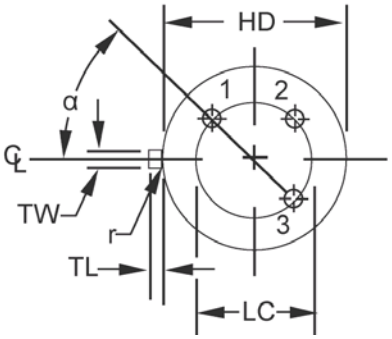
GRAPHS (continued)

FIGURE 3 – Maximum Safe Operating Area



PACKAGE DIMENSIONS





Symbol	Dimensions				Note
	Inch		Millimeters		
	Min	Max	Min	Max	
CD	0.305	0.335	7.75	8.51	
CH	0.160	0.180	4.06	4.57	
HD	0.335	0.370	8.51	9.40	
LC	0.200 TP		5.08 TP		6
LD	0.016	0.021	0.41	0.53	7, 8
LL	0.500	0.750	12.70	19.05	7, 8
LU	0.016	0.019	0.41	0.48	7, 8
L1		0.050		1.27	7, 8
L2	0.250		6.35		7, 8
P	.100		2.54		5
Q		0.050		1.27	4
TL	0.029	0.045	0.74	1.14	3
TW	0.028	0.034	0.72	0.86	2
r		0.010		0.25	9
α	45° TP		45° TP		6

NOTES:

1. Dimensions are in inches. Millimeters are given for general information only.
2. Beyond radius (r) maximum, J shall be held for a minimum length of .011 (0.028 mm).
3. Dimension TL measured from maximum HD.
4. Outline in this zone is not controlled.
5. Dimension CD shall not vary more than .010 (0.25 mm) in zone P. This zone is controlled for automatic handling.
6. Leads at gauge plane .054 +.001, -.000 (1.37 +0.03, -0.00 mm) below seating plane shall be within .007 (0.18 mm) radius of true position (TP) at maximum material condition (MMC) relative to tab at MMC.
7. LU applies between L1 and L2. LD applies between L2 and L minimum. Diameter is uncontrolled in L1 and beyond LL minimum.
8. All three leads.
9. Radius (r) applies to both inside corners of tab.
10. Drain is electrically connected to the case.
11. In accordance with ASME Y14.5M, diameters are equivalent to Φx symbology.

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