To our customers,

Old Company Name in Catalogs and Other Documents

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Renesas Electronics website: http://www.renesas.com

April 1st, 2010
Renesas Electronics Corporation

Issued by: Renesas Electronics Corporation (http://www.renesas.com)

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RENESAS

MOS FIELD EFFECT TRANSISTOR
2SJ598

SWITCHING
P-CHANNEL POWER MOS FET

DESCRIPTION

The 2SJ598 is P-channel MOS Field Effect Transistor designed for solenoid, motor and lamp driver.

ORDERING INFORMATION

PART NUMBER	PACKAGE
2SJ598	TO-251 (MP-3)
2SJ598-Z	TO-252 (MP-3Z)

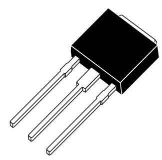
FEATURES

- Low on-state resistance:
  $R_{DS(on)1}$ = 130 mΩ MAX. (V_{GS} = –10 V, I_D = –6 A)
  $R_{DS(on)2}$ = 190 mΩ MAX. (V_{GS} = –4.0 V, I_D = –6 A)
- Low C_{iss}: C_{iss} = 720 pF TYP.
- Built-in gate protection diode
- TO-251/TO-252 package

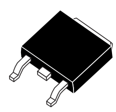
ABSOLUTE MAXIMUM RATINGS (T_A = 25°C)

Drain to Source Voltage (V_{GS} = 0 V)	V_{DSS}	–60	V
Gate to Source Voltage (V_{DS} = 0 V)	V_{GSS}	$\mp$20	V
Drain Current (DC) (T_C = 25°C)	$I_{D(DC)}$	$\mp$12	A
Drain Current (pulse) Note1	$I_{D(pulse)}$	$\mp$30	A
Total Power Dissipation (T_C = 25°C)	P_T	23	W
Total Power Dissipation (T_A = 25°C)	P_T	1.0	W
Channel Temperature	T_{ch}	150	°C
Storage Temperature	T_{stg}	–55 to +150	°C
Single Avalanche Current Note2	I_{AS}	–12	A
Single Avalanche Energy Note2	E_{AS}	14.4	mJ

(TO-251)



(TO-252)



Notes 1. PW ≤ 10 μs, Duty Cycle ≤ 1%

2. Starting T_{ch} = 25°C, V_{DD} = –30 V, R_G = 25 Ω, V_{GS} = –20 → 0 V

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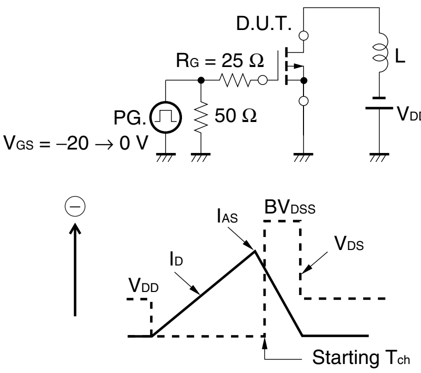
Printed in Japan

The mark <R> shows major revised points.
The revised points can be easily searched by copying an "<R>" in the PDF file and specifying it in the "Find what:" field.

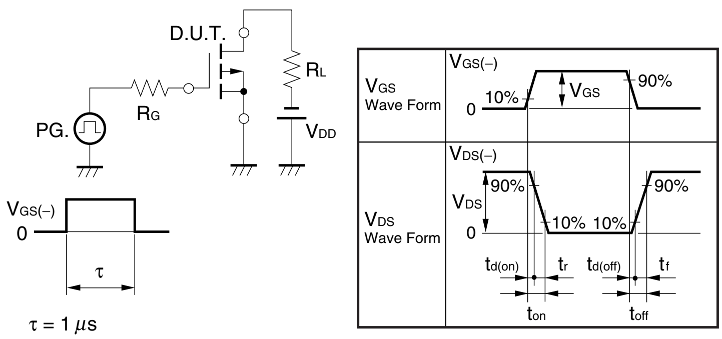
ELECTRICAL CHARACTERISTICS (T_A = 25°C)

CHARACTERISTICS	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = –60 V, V_{GS} = 0 V			–10	μA
Gate Leakage Current	I_{GSS}	V_{GS} = ∓16 V, V_{DS} = 0 V			∓10	μA
Gate Cut-off Voltage	$V_{GS(off)}$	V_{DS} = –10 V, I_D = –1 mA	–1.5	–2.0	–2.5	V
Forward Transfer Admittance	$\| y_{fs} \|$	V_{DS} = –10 V, I_D = –6 A	5	11		S
Drain to Source On-state Resistance	$R_{DS(on)1}$	V_{GS} = –10 V, I_D = –6 A		102	130	mΩ
	$R_{DS(on)2}$	V_{GS} = –4.0 V, I_D = –6 A		131	190	mΩ
Input Capacitance	C_{iss}	V_{DS} = –10 V		720		pF
Output Capacitance	C_{oss}	V_{GS} = 0 V		150		pF
Reverse Transfer Capacitance	C_{rss}	f = 1 MHz		50		pF
Turn-on Delay Time	$t_{d(on)}$	I_D = –6 A		7		ns
Rise Time	t_r	V_{GS} = –10 V		4		ns
Turn-off Delay Time	$t_{d(off)}$	V_{DD} = –30 V		35		ns
Fall Time	t_f	R_G = 0 Ω		10		ns
Total Gate Charge	Q_G	I_D = –12 A		15		nC
Gate to Source Charge	Q_{GS}	V_{DD}= –48 V		3		nC
Gate to Drain Charge	Q_{GD}	V_{GS} = –10 V		4		nC
Body Diode Forward Voltage	$V_{F(S-D)}$	I_F = 12 A, V_{GS} = 0 V		0.98		V
Reverse Recovery Time	t_{rr}	I_F = 12 A, V_{GS} = 0 V		50		ns
Reverse Recovery Charge	Q_{rr}	di/dt = 100 A/μs		100		nC

TEST CIRCUIT 1 AVALANCHE CAPABILITY

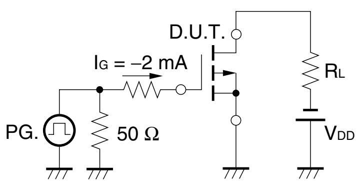


TEST CIRCUIT 2 SWITCHING TIME



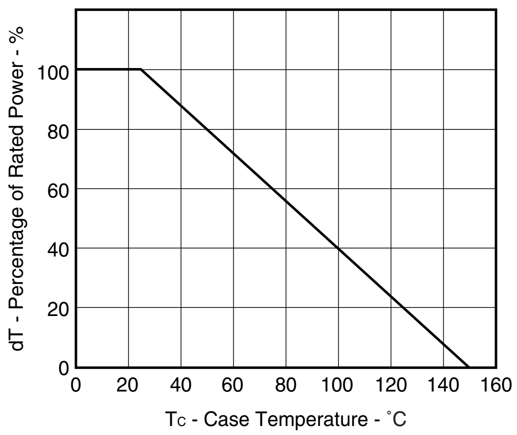
τ = 1 μs
Duty Cycle ≤ 1%

TEST CIRCUIT 3 GATE CHARGE

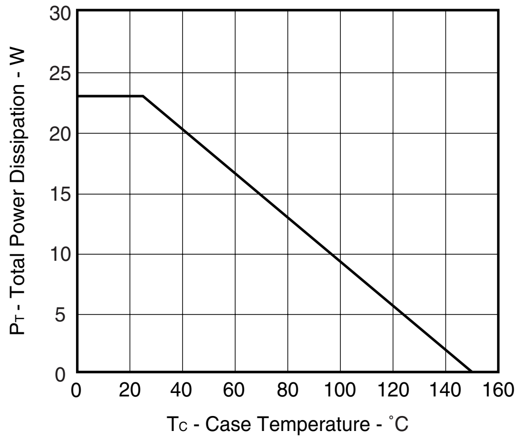


TYPICAL CHARACTERISTICS (T_A = 25°C)

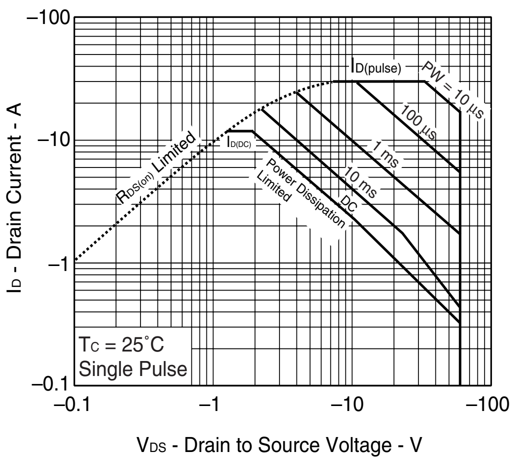
DERATING FACTOR OF FORWARD BIAS SAFE OPERATING AREA



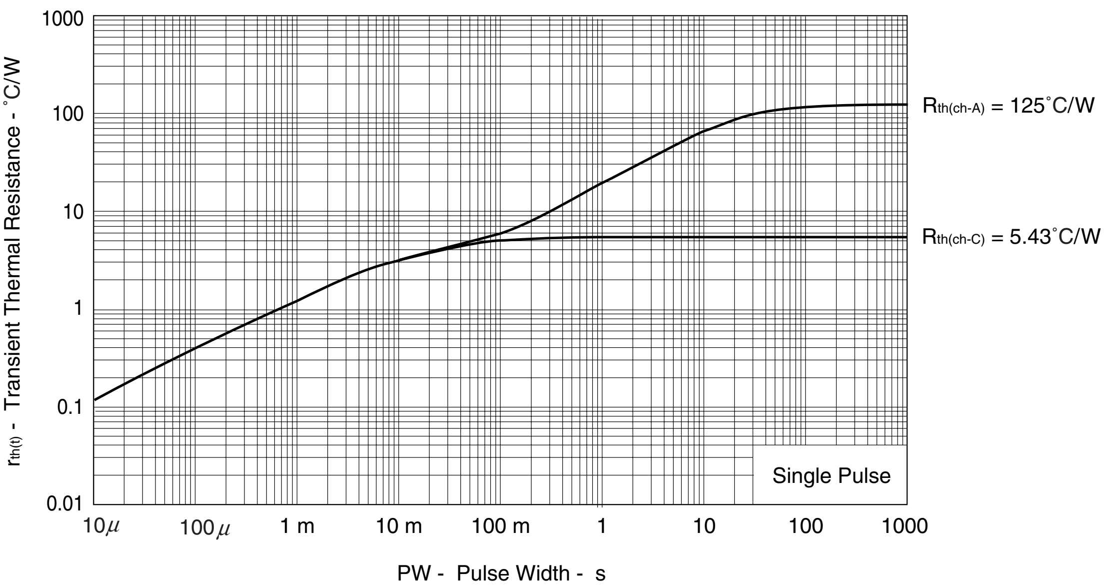
TOTAL POWER DISSIPATION vs. CASE TEMPERATURE



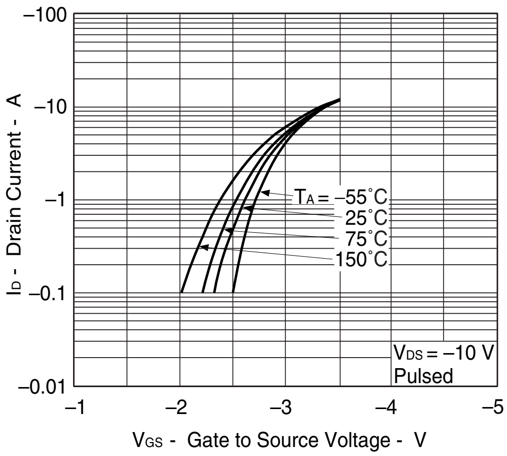
FORWARD BIAS SAFE OPERATING AREA



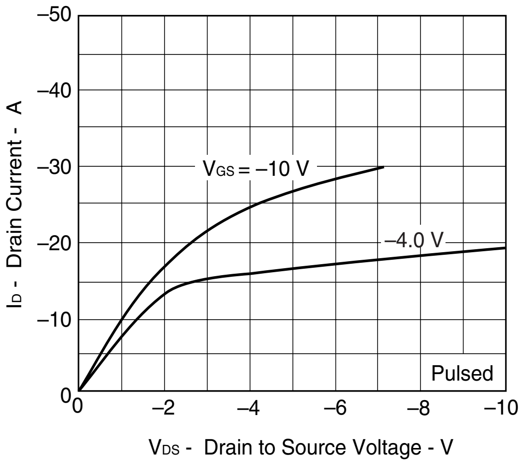
TRANSIENT THERMAL RESISTANCE vs. PULSE WIDTH



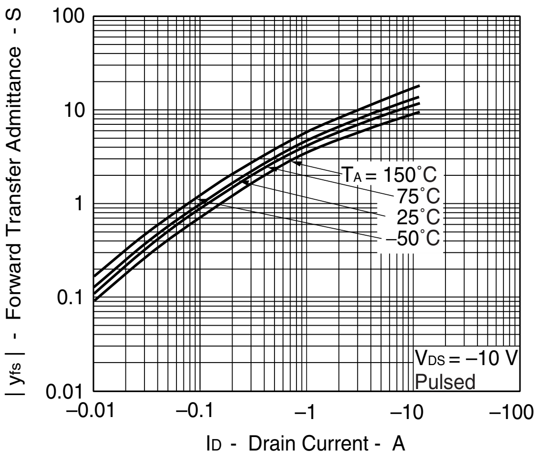
FORWARD TRANSFER CHARACTERISTICS



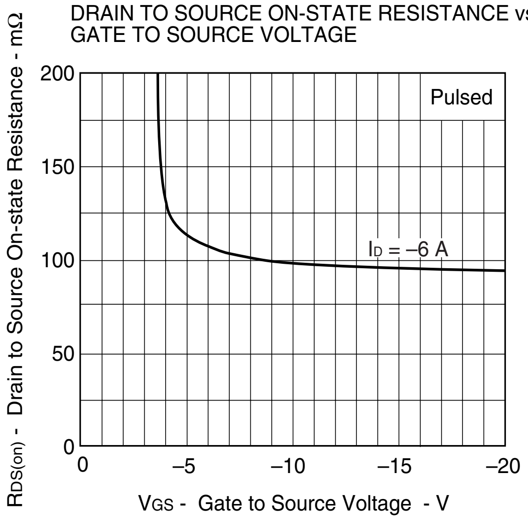
DRAIN CURRENT vs.
DRAIN TO SOURCE VOLTAGE



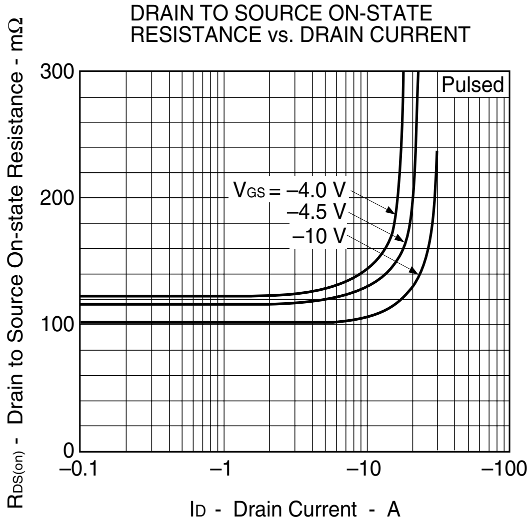
FORWARD TRANSFER ADMITTANCE vs.
DRAIN CURRENT



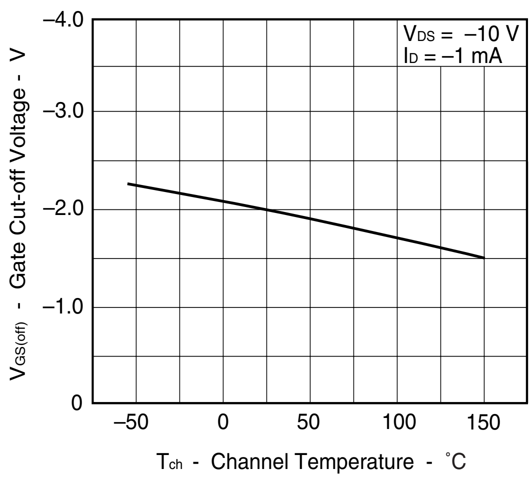
DRAIN TO SOURCE ON-STATE RESISTANCE vs.
GATE TO SOURCE VOLTAGE



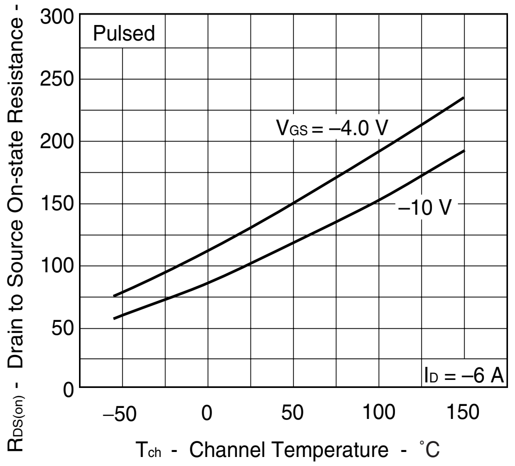
DRAIN TO SOURCE ON-STATE
RESISTANCE vs. DRAIN CURRENT



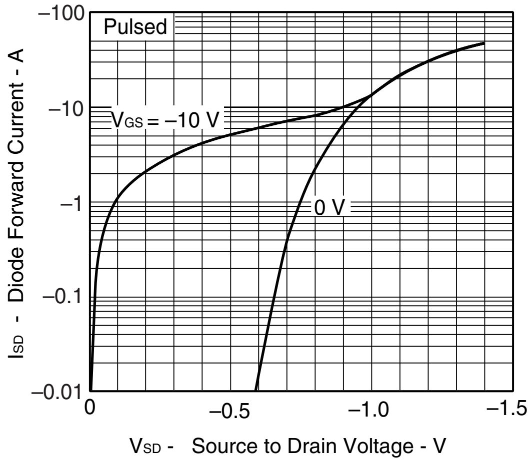
GATE CUT-OFF VOLTAGE vs.
CHANNEL TEMPERATURE



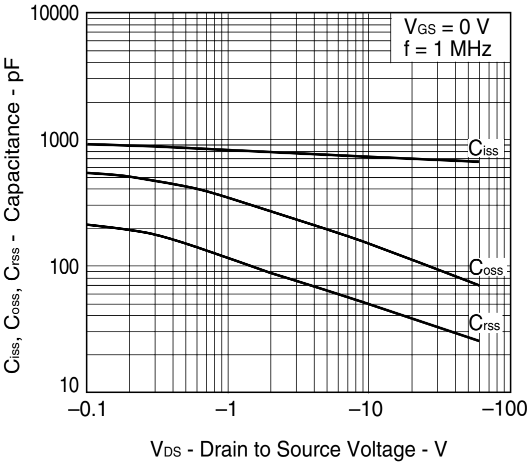
DRAIN TO SOURCE ON-STATE RESISTANCE vs. CHANNEL TEMPERATURE



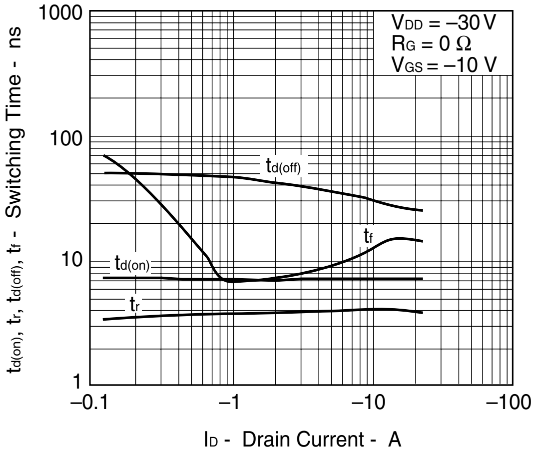
SOURCE TO DRAIN DIODE FORWARD VOLTAGE



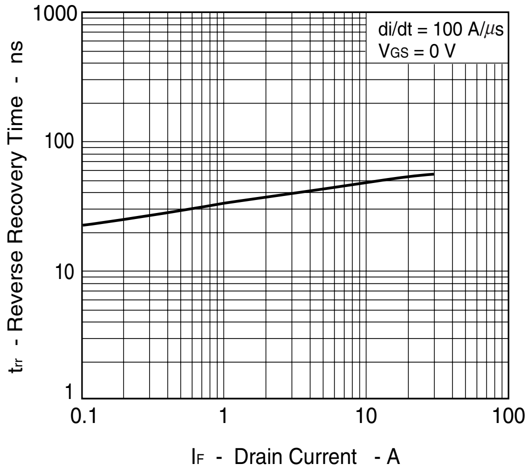
CAPACITANCE vs. DRAIN TO SOURCE VOLTAGE



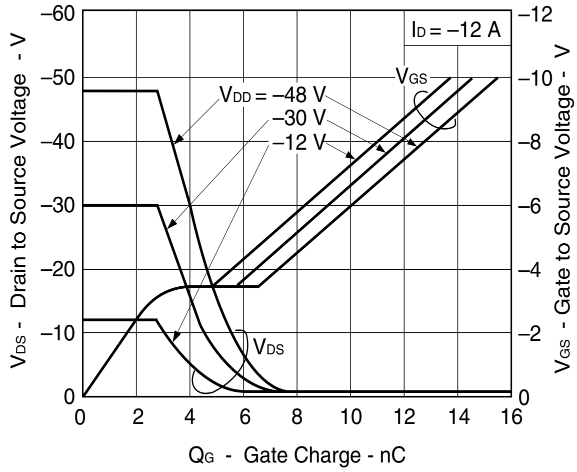
SWITCHING CHARACTERISTICS



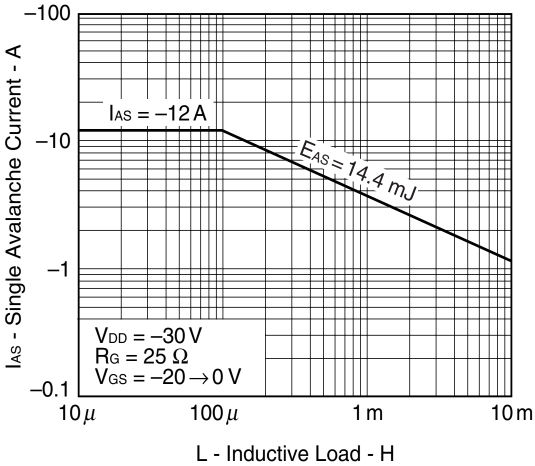
REVERSE RECOVERY TIME vs. DRAIN CURRENT



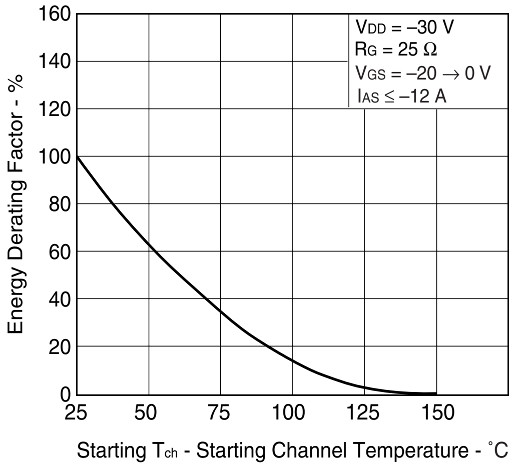
DYNAMIC INPUT/OUTPUT CHARACTERISTICS



SINGLE AVALANCHE CURRENT vs. INDUCTIVE LOAD

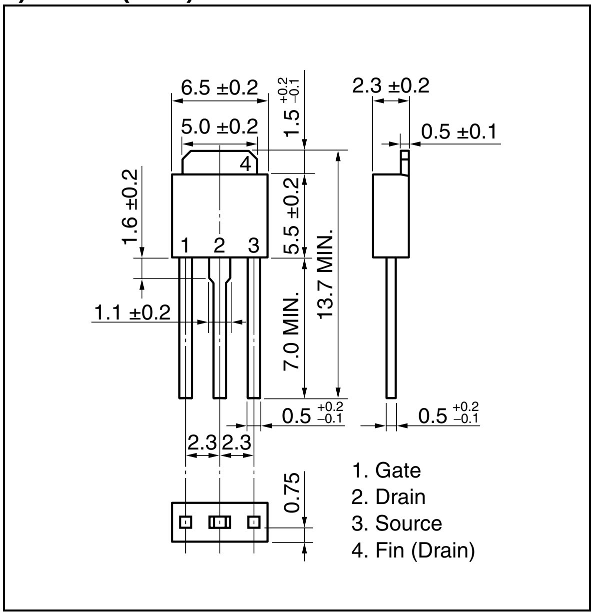


SINGLE AVALANCHE ENERGY DERATING FACTOR

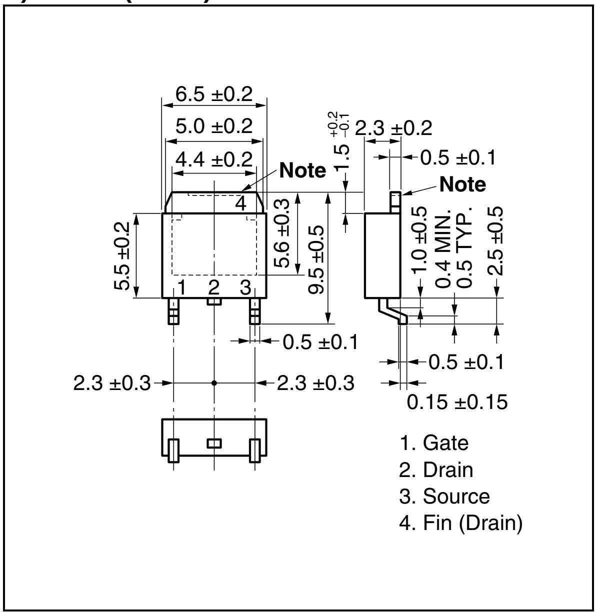


PACKAGE DRAWINGS (Unit: mm)

1) TO-251 (MP-3)

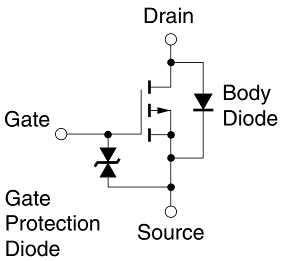


<R> **2) TO-252 (MP-3Z)**



Note The depth of notch at the top of the fin is from 0 to 0.2 mm.

EQUIVALENT CIRCUIT



Remark The diode connected between the gate and source of the transistor serves as a protector against ESD. When this device actually used, an additional protection circuit is externally required if a voltage exceeding the rated voltage may be applied to this device.