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April 1st, 2010 Renesas Electronics Corporation

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RENESAS

MOS FIELD EFFECT TRANSISTOR 2SJ598

SWITCHING P-CHANNEL POWER MOS FET

DESCRIPTION

The 2SJ598 is P-channel MOS Field Effect Transistor designed for solenoid, motor and lamp driver.

PART NUMBER	PACKAGE		
2SJ598	TO-251 (MP-3)		
2SJ598-Z	TO-252 (MP-3Z)		

FEATURES

- Low on-state resistance: R_{DS(on)1} = 130 mΩ MAX. (V_{GS} = -10 V, I_D = -6 A)
- $R_{DS(on)2} = 190 \text{ m}\Omega \text{ MAX.} (V_{GS} = -4.0 \text{ V}, \text{ ID} = -6 \text{ A})$
- Low Ciss: Ciss = 720 pF TYP.
- Built-in gate protection diode
- TO-251/TO-252 package

ABSOLUTE MAXIMUM RATINGS (TA = 25°C)

Drain to Source Voltage (Vgs = 0 V)	Vdss	-60	V
Gate to Source Voltage (VDS = 0 V)	Vgss	∓20	V
Drain Current (DC) (Tc = 25°C)	ID(DC)	∓12	А
Drain Current (pulse) Note1	D(pulse)	∓30	А
Total Power Dissipation (Tc = 25°C)	Рт	23	W
Total Power Dissipation ($T_A = 25^{\circ}C$)	Рт	1.0	W
Channel Temperature	Tch	150	°C
Storage Temperature	Tstg	–55 to +150	°C
Single Avalanche Current Note2	las	-12	А
Single Avalanche Energy Note2	Eas	14.4	mJ

(TO-251)



(TO-252)



Notes 1. PW \leq 10 μ s, Duty Cycle \leq 1%

2. Starting T_{ch} = 25°C, V_{DD} = -30 V, R_G = 25 Ω , V_{GS} = $-20 \rightarrow 0$ V

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or revised points.

The revised points can be easily searched by copying an "<R>" in the PDF file and specifying it in the "Find what:" field.

90%

90%

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tof

VGS

10% 10%

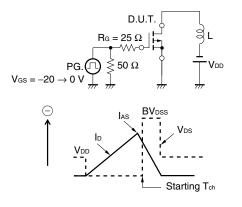
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td(off)

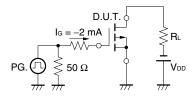
ELECTRICAL CHARACTERISTICS (TA = 25°C)

CHARACTERISTICS	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Zero Gate Voltage Drain Current	IDSS	$V_{DS} = -60 V, V_{GS} = 0 V$			-10	μA
Gate Leakage Current	lgss	$V_{GS} = \mp 16 \text{ V}, \text{ V}_{DS} = 0 \text{ V}$			∓10	μA
Gate Cut-off Voltage	VGS(off)	$V_{DS} = -10 V$, $I_D = -1 mA$	-1.5	-2.0	-2.5	V
Forward Transfer Admittance	y _{fs}	$V_{DS} = -10 V$, $I_D = -6 A$	5	11		S
Drain to Source On-state Resistance	RDS(on)1	$V_{GS} = -10 V$, $I_D = -6 A$		102	130	mΩ
	RDS(on)2	$V_{GS} = -4.0 V$, $I_{D} = -6 A$		131	190	mΩ
Input Capacitance	Ciss	V _{DS} = -10 V		720		pF
Output Capacitance	Coss	$V_{GS} = 0 V$		150		pF
Reverse Transfer Capacitance	Crss	f = 1 MHz		50		pF
Turn-on Delay Time	td(on)	$I_D = -6 A$		7		ns
Rise Time	tr	$V_{GS} = -10 V$		4		ns
Turn-off Delay Time	td(off)	$V_{DD} = -30 \text{ V}$		35		ns
Fall Time	tr	$R_G = 0 \Omega$		10		ns
Total Gate Charge	QG	$I_D = -12 A$		15		nC
Gate to Source Charge	Q _{GS}	$V_{DD} = -48 V$		3		nC
Gate to Drain Charge	Qgd	$V_{GS} = -10 V$		4		nC
Body Diode Forward Voltage	VF(S-D)	$I_F = 12 A, V_{GS} = 0 V$		0.98		V
Reverse Recovery Time	trr	IF = 12 A, VGS = 0 V		50		ns
Reverse Recovery Charge	Qrr	di/dt = 100 A/µs		100		nC

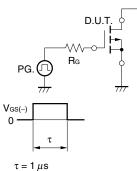
TEST CIRCUIT 1 AVALANCHE CAPABILITY



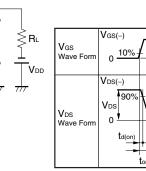
TEST CIRCUIT 3 GATE CHARGE



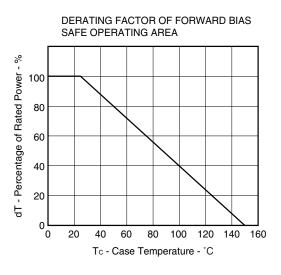
TEST CIRCUIT 2 SWITCHING TIME



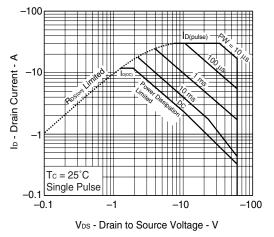
Duty Cycle $\leq 1\%$

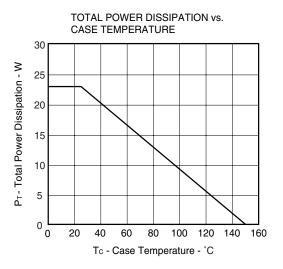


TYPICAL CHARACTERISTICS (TA = 25°C)

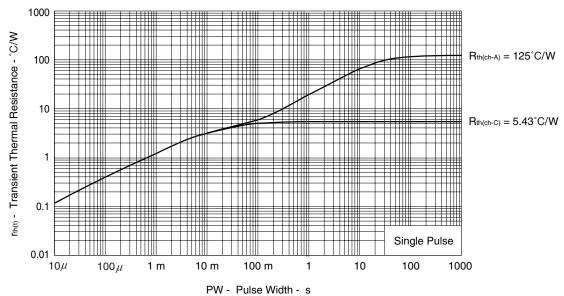


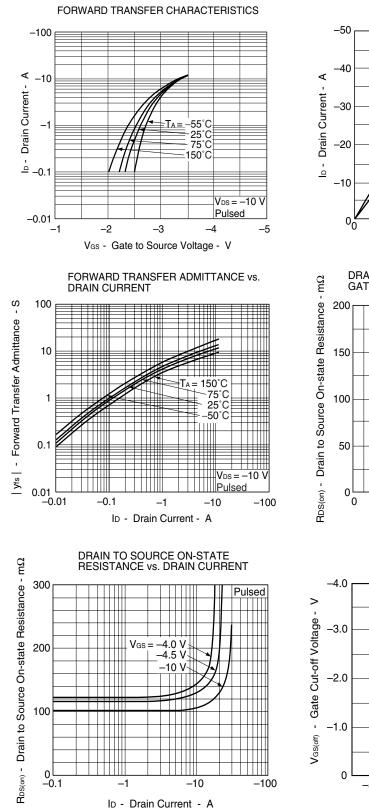


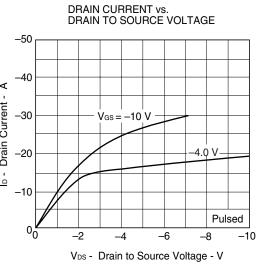




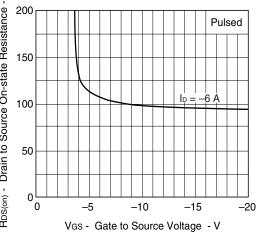
TRANSIENT THERMAL RESISTANCE vs. PULSE WIDTH



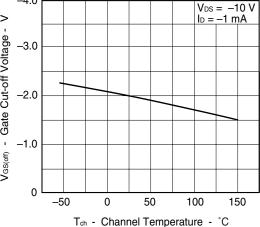




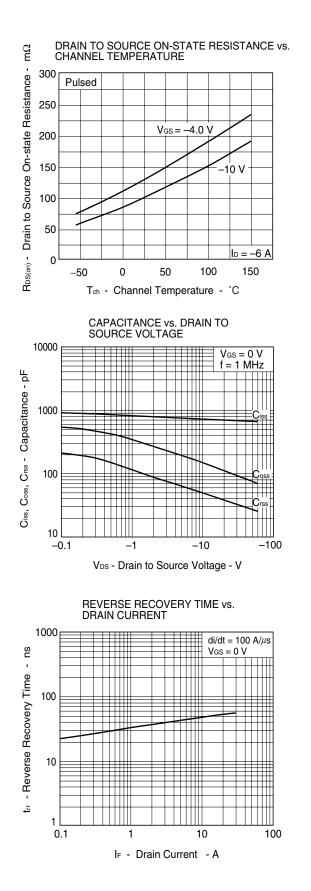




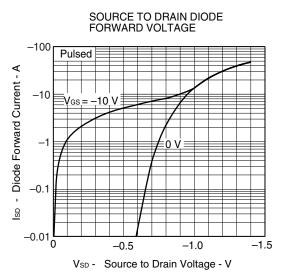




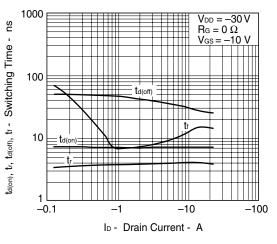
2SJ598

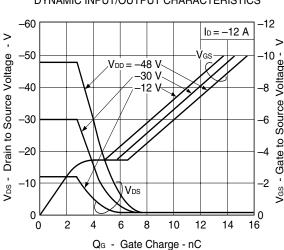


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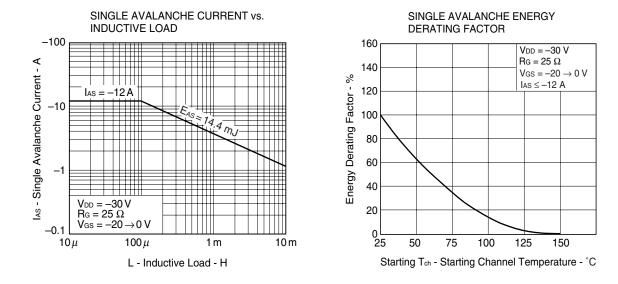


SWITCHING CHARACTERISTICS



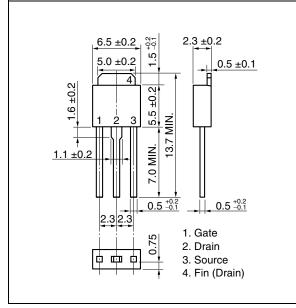


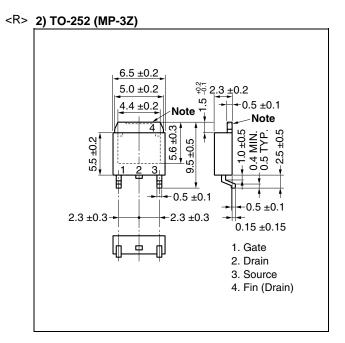
DYNAMIC INPUT/OUTPUT CHARACTERISTICS



PACKAGE DRAWINGS (Unit: mm)

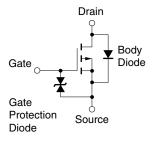
1) TO-251 (MP-3)





Note The depth of notch at the top of the fin is from 0 to 0.2 mm.

EQUIVALENT CIRCUIT



Remark The diode connected between the gate and source of the transistor serves as a protector against ESD. When this device actually used, an additional protection circuit is externally required if a voltage exceeding the rated voltage may be applied to this device.

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