



#### N-CHANNEL ENHANCEMENT MODE MOSFET

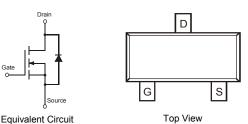
#### **Features**

- Low On-Resistance
  - 29mΩ @V<sub>GS</sub> = 4.5V
  - 50mΩ @V<sub>GS</sub> = 2.5V
  - 100mΩ @V<sub>GS</sub> = 2.0V
- Very Low Gate Threshold Voltage
- Low Input Capacitance
- Fast Switching Speed
- Totally Lead-Free & Fully RoHS Compliant (Notes 1 & 2)
- Halogen and Antimony Free. "Green" Device (Note 3)
- Qualified to AEC-Q101 Standards for High Reliability

#### **Mechanical Data**

- Case: SOT23
- Case Material: Molded Plastic, "Green" Molding Compound. UL Flammability Classification Rating 94V-0
- Moisture Sensitivity: Level 1 per J-STD-020D
- Terminal Connections: See Diagram
- Terminals: Finish Matte Tin annealed over Copper leadframe. Solderable per MIL-STD-202, Method 208 @3
- Weight: 0.008 grams (approximate)

Top View



#### Ordering Information (Note 4)

Part Number	Case	Packaging
DMN2050L-7	SOT23	3000/Tape & Reel

1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS) & 2011/65/EU (RoHS 2) compliant. Notes:

ΥN

2. See http://www.diodes.com/quality/lead\_free.html for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.

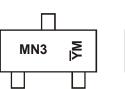
3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.

4. For packaging details, go to our website at http://www.diodes.com/products/packages.html.

MN3

Shanghai A/T Site

### **Marking Information**



Chengdu A/T Site

MN3 = Marking Code

YM = Date Code Marking for SAT (Shanghai Assembly/ Test site) YM = Date Code Marking for CAT (Chengdu Assembly/ Test site) Y or  $\overline{Y}$  = Year (ex: A = 2013) M = Month (ex: 9 = September)

Date Code Kev

Year	2008		2009	2010		2011	2012		2013	2014		2015
Code	V		W	Х		Y	Z		А	В		С
Month	Jan	Feb	Mar	Apr	May	Jun	Jul	Aug	Sep	Oct	Nov	Dec
Code	1	2	3	4	5	6	7	8	9	0	N	D

SOT23



### Maximum Ratings (@T<sub>A</sub> = +25°C, unless otherwise specified.)

Characteristic	Symbol	Value	Units
Drain-Source Voltage	V <sub>DSS</sub>	20	V
Gate-Source Voltage	V <sub>GSS</sub>	±12	V
Drain Current (Note 5)	ID	5.9	А
Pulsed Drain Current (Note 6)	I <sub>DM</sub>	21	A

### **Thermal Characteristics**

Characteristic	Symbol	Value	Units
Total Power Dissipation (Note 5)	PD	1.4	W
Thermal Resistance, Junction to Ambient (Note 5)	R <sub>0JA</sub>	90	°C/W
Operating and Storage Temperature Range	T <sub>J</sub> , T <sub>STG</sub>	-55 to +150	°C

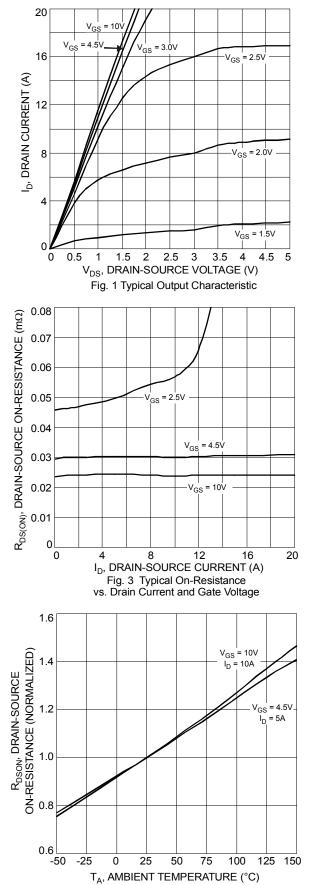
### Electrical Characteristics (@T<sub>A</sub> = +25°C, unless otherwise specified.)

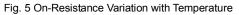
Characteristic	Symbol	Min	Тур	Max	Unit	Test Condition	
OFF CHARACTERISTICS (Note 7)	,		,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,	1	1		
Drain-Source Breakdown Voltage	BV <sub>DSS</sub>	20		—	V	V <sub>GS</sub> = 0V, I <sub>D</sub> = 250µA	
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	_		1	μA	V <sub>DS</sub> = 20V, V <sub>GS</sub> = 0V	
Gate-Source Leakage	I <sub>GSS</sub>	_		±100	nA	V <sub>GS</sub> = ±12V, V <sub>DS</sub> = 0V	
ON CHARACTERISTICS (Note 7)							
Gate Threshold Voltage	V <sub>GS(th)</sub>	0.45		1.4	V	$V_{DS}$ = $V_{GS}$ , $I_D$ = 250 $\mu$ A	
		_	24	29		V <sub>GS</sub> = 4.5V, I <sub>D</sub> = 5.0A	
Static Drain-Source On-Resistance	R <sub>DS(ON)</sub>		42	50	mΩ	V <sub>GS</sub> = 2.5V, I <sub>D</sub> = 3.1A	
			68	100		V <sub>GS</sub> = 2.0V, I <sub>D</sub> = 1.5A	
Forward Transfer Admittance	Y <sub>fs</sub>	_	8	_	S	V <sub>DS</sub> =5V, I <sub>D</sub> = 2.1A	
Diode Forward Voltage (Note 7)	V <sub>SD</sub>	_	0.9	1.4	V	V <sub>GS</sub> = 0V, I <sub>S</sub> = 2.0A	
DYNAMIC CHARACTERISTICS (Note 8)							
Input Capacitance	Ciss		532		pF		
Output Capacitance	Coss		144		pF	−V <sub>DS</sub> = 10V, V <sub>GS</sub> = 0V _f = 1.0MHz	
Reverse Transfer Capacitance	C <sub>rss</sub>		117	_	pF		
Gate Resistance	R <sub>G</sub>	_	1.3	_	Ω	$V_{DS} = 0V, V_{GS} = 0V, f = 1.0MHz$	
SWITCHING CHARACTERISTICS (Note 8)							
Total Gate Charge	Qg	_	6.7	—		$V_{DS}$ = 10V, $V_{GS}$ = 4.5V, $I_{D}$ = 5.0A	
Gate-Source Charge	Q <sub>gs</sub>		0.8	_	nC	V <sub>DS</sub> = 10V, V <sub>GS</sub> = 4.5V, I <sub>D</sub> = 5.0A	
Gate-Drain Charge	Q <sub>gd</sub>		3.0			V <sub>DS</sub> = 10V, V <sub>GS</sub> = 4.5V, I <sub>D</sub> = 5.0A	

Notes: 5. Device mounted on FR-4 PCB, on 2oz Copper pad layout with  $R_{\theta JA}$  = 90°C/W.

Borte integrating pulse width limited by junction temperature.
Short duration pulse test used to minimize self-heating effect.
Guaranteed by design. Not subject to production testing.







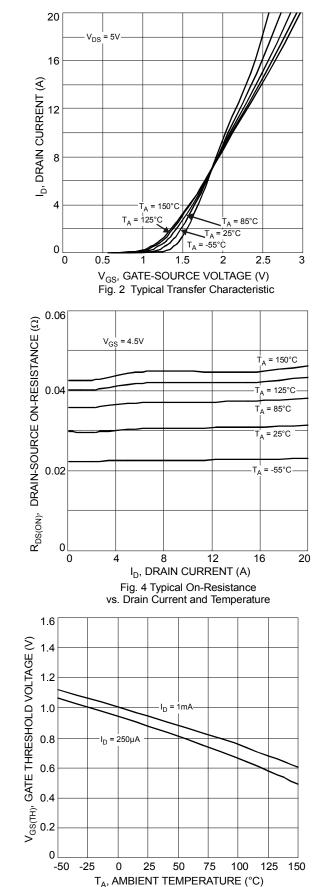


Fig. 6 Gate Threshold Variation vs. Ambient Temperature

DMN2050L Document number: DS31502 Rev. 4 - 2



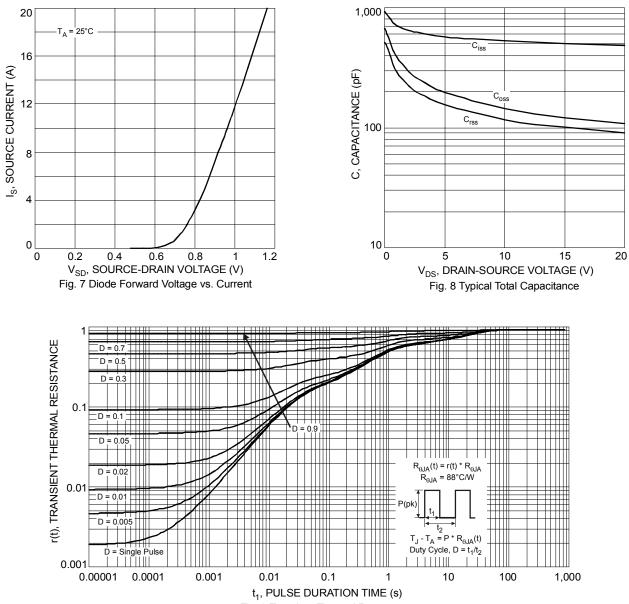
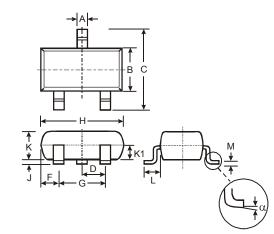


Fig. 9 Transient Thermal Response



# Package Outline Dimensions

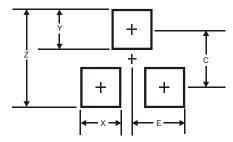
Please see AP02002 at http://www.diodes.com/datasheets/ap02002.pdf for latest version.



SOT23							
Dim	Min	Max	Тур				
Α	0.37	0.51	0.40				
в	1.20	1.40	1.30				
С	2.30	2.50	2.40				
D	0.89	1.03	0.915				
F	0.45	0.60	0.535				
G	1.78	2.05	1.83				
Н	2.80	3.00	2.90				
J	0.013	0.10	0.05				
Κ	0.903	1.10	1.00				
K1	-	-	0.400				
L	0.45	0.61	0.55				
М	0.085	0.18	0.11				
α	0°	8°	-				
All	All Dimensions in mm						

# Suggested Pad Layout

Please see AP02001 at http://www.diodes.com/datasheets/ap02001.pdf for latest version.



Dimensions	Value (in mm)
Z	2.9
Х	0.8
Y	0.9
С	2.0
E	1.35



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