Intel® IXF6048

51/155/622/2488 Mbit/s SONET/SDH Cell/Packet Interface

Datasheet

Intel IXF6048 is a single-chip interface solution for the transport of ATM cells or HDLC frames over SONET/SDH. Intel IXF6048 can operate as a quad 51/155/622 Mbit/s or as a single 2488 Mbit/s SONET/SDH processor. When configured in ATM UNI mode, it interfaces with an ATM layer device using the industry standard UTOPIA interface (Levels 3/2/1). When configured in Packet Over SONET mode, it transfers the PPP frames using a UTOPIA-enhanced interface, based on the ATM industry standard UTOPIA, which supports the transfer of variable length frames.

Product Features

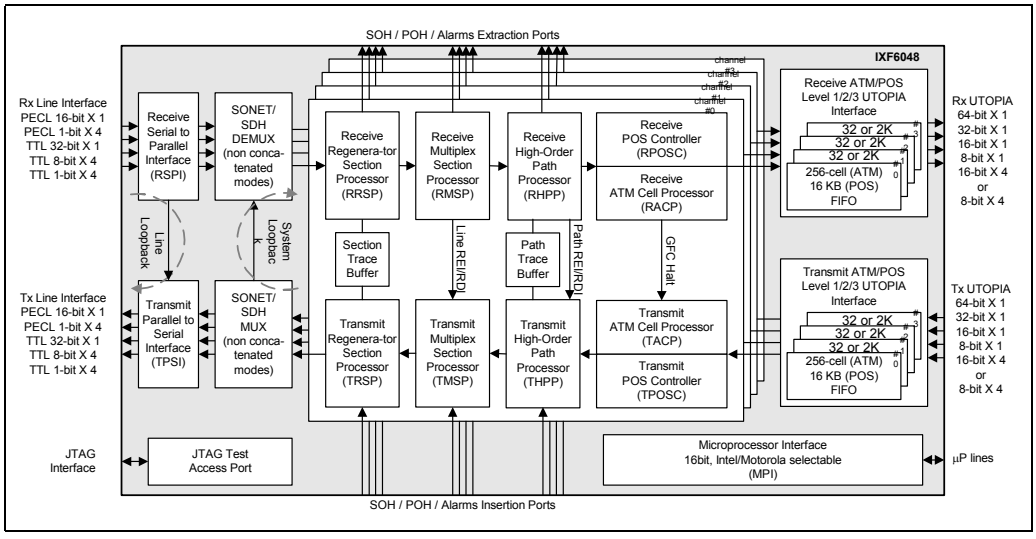
Applications

- WAN and edge ATM switches
- Layer 3 switches
- Video and File Servers
- Broadband Switching Systems

Features

- Maps ATM cells or HDLC frames into one STS-48c/STM-16c/STS-48/STM-16/STM-4 or four STS-12c/STM-4c/STS-3c/STM-1/STS-1 SONET/SDH signals.
- In POS mode, each channel performs SPE scrambling ($1 + X^{43}$), HDLC processing, and offers a UTOPIA-type FIFO-based POS interface.
- Supports the UTOPIA Level 3 (single 64-bit, 32-bit, or quad 8-bit), Level 2 (single 8/16-bit), and Level 1 (quad 8/16-bit) interface modes.
- Implements a GFC halt function (ITU I.150 and I.361).
- Handles full J0/J1 trace identifier processing.
- SOH, POH and Alarm insertion/extraction ports.
- Hardware assistance for APS implementation, via K1 and K2 bytes.
- Provides a 16-bit microprocessor port. One-second counters for B1/B2/B3, M1/G1 REI, etc.
- 600 TBGA package; -40 °C to +85 °C operating conditions; low power, 3.3 V operation, 5 V tolerant I/O

Figure 1. Block Diagram



Order Number: 273644-004
September 2003

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Revision History

Date	Revision	Description
September 2003	004	Please refer to the change bars.
July 2003	003	Please refer to the change bars.
January 2003	002	Corrected typographical errors. Removed the Xmt/Rcv PeclMsb_cnf bit.
November 2001	001	Initial release.

1.0 Pin Description

Figure 2. Intel IXF6048 Application Diagram

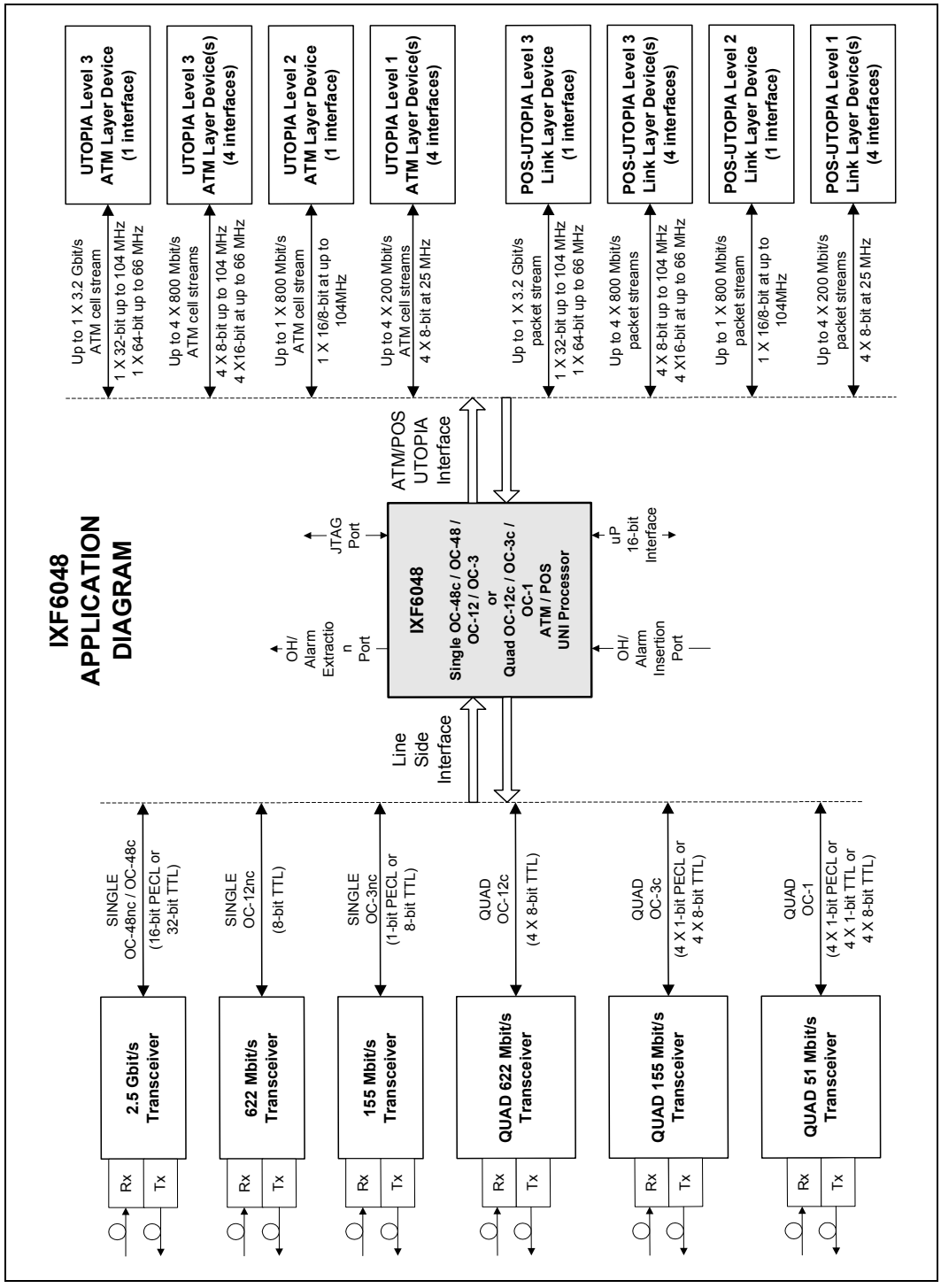


Table 1. Intel IXF6048 Main Configurations

Operation Mode	Line Side Interfaces	ATM/POS-UTOPIA Interfaces
Single STS-48c/STM-16c	1 x 16-bit PECL at 155.52 MHz 1 x 32-bit TTL at 77.76 MHz	1 x 32-bit at up to 104 MHz (UL3) 1 x 64-bit at up to 52 MHz (UL3)
Single STS-48/STM-16	1 x 16-bit PECL at 155.52 MHz 1 x 32-bit TTL at 77.76 MHz	1 x 32-bit at up to 104 MHz (UL3) 1 x 64-bit at up to 52 MHz (UL3) 4 x 8-bit at up to 104 MHz (UL3) 4 x 16-bit at up to 52 MHz (UL2 x 4)
Single STS-12/STM-4	1 x 8-bit TTL at 77.76 MHz	1 x 16-bit at up to 104 MHz (UL2) 1 x 8-bit at up to 104 MHz (UL2) 4 x 8-bit at up to 104 MHz (UL1 x 4)
Single STS-3/STM-1	1 x 1-bit PECL at 155.52 MHz 1 x 8-bit TTL at 19.44 MHz	1 x 8-bit at up to 104 MHz (UL2) 1 x 16-bit at up to 104 MHz (UL2) 3 x 8-bit at up to 104 MHz (UL1 x 3)
Quad STS-12c/STM-4c	4 x 8-bit TTL at 77.76 MHz	1 x 32-bit at up to 104 MHz (UL3) 1 x 64-bit at up to 52 MHz (UL3) 4 x 8-bit at up to 104 MHz (UL3) 4 x 16-bit at up to 52 MHz (UL2 x 4)
Quad STS-3c/STM-1	4 x 1-bit PECL at 155.52 MHz 4 x 8-bit TTL at 19.44 MHz	1 x 16-bit at up to 104 MHz (UL2) 4 x 8-bit at up to 104 MHz (UL1 x 4)
Quad STS-1	4 x 1-bit PECL at 51.84 MHz 4 x 1-bit TTL at 51.84 MHz 4 x 8-bit TTL at 6.48 MHz	1 x 8-bit at up to 104 MHz (UL2) 1 x 16-bit at up to 104 MHz (UL2) 4 x 8-bit at up to 104 MHz (UL1 x 3)

Table 2. Intel IXF6048 Pin Diagram (Bottom View)

	A	B	C	D	E	F	G	H	J	K	L	M	N	P	R	T
1	GND_TTL	GND_TTL	TXDATA[22] TXDAT_1[6] TXDATA_2[6]	TXPRTY_2	TXDATA[12] TXDAT_0[12] TXDATA_1[4]	VDD_CORE	TXDATA[3] TXDATA_0[3]	TXEOF TXEOF_0	TPAL_3 TDOW_3 TXDATA[63]	TPOHINS_3 TXDATA[59]	TPOH_3 TXDATA[55]	TPOH_2 TXDATA[54]	TPOHFR_0 TOWC_0 TXDATA[48]	TPOHCK_0 TMOW_0 TXDATA[44]	GND_TTL	GND_TTL
2	GND_TTL	GND_TTL	TXSOF_3	TXDATA[17] TXDATA_1[1] TXDATA_2[1]	TXDATA[15] TXDAT_0[15] TXDATA_1[7]	GND_CORE	TXEOF_1	TXDATA[6] TXDATA_0[6]	TXPRTY TXPRTY_0	VDD_CORE	TPAL_0 TDOW_0 TXDATA[60]	GND_CORE	TPOHFR_3 TOWC_3 TXDATA[51]	TPOHCK_1 TMOW_1 TXDATA[45]	GND_TTL	GND_TTL
3	TXDATA[27] TXDAT_1[11] TXDATA_3[3]	TXDATA[25] TXDATA_1[9] TXDATA_3[1]	VDD_CORE	TXDATA[16] TXDATA_1[0] TXDATA_2[0]	TXERR_2	TXDATA[10] TXDAT_0[10] TXDATA_1[2]	TXDATA[8] TXDATA_0[8] TXDATA_1[0]	VDD_TTL	TXDATA[1] TXDATA_0[1]	TXDATA[0] TXDATA_0[0]	TPAL_2 TDOW_2 TXDATA[62]	TPOHINS_0 TXDATA[56]	TPOH_0 TXDATA[52]	TPOHCK_2 TMOW_2 TXDATA[46]	TSAL TROW_0 TXDATA[40]	TPOW2 TSALFR_3 TXDATA[39]
4	TXDATA[26] TXDAT_1[10] TXDATA_3[2]	TXDATA[31] TXDAT_1[15] TXDATA_3[7]	TXERR_3	TXDATA[20] TXDATA_1[4] TXDATA_2[4]	TXDATA[19] TXDATA_1[3] TXDATA_2[3]	TXDATA[14] TXDAT_0[14] TXDATA_1[6]	TXDATA[13] TXDAT_0[13] TXDATA_1[5]	TXPRTY_1	TXDATA[5] TXDATA_0[5]	TXERR TXERR_0	GND_CORE	TPOHINS_1 TXDATA[57]	VDD_CORE	TPOHCK_3 TMOW_3 TXDATA[47]	TSAL_1 TROW_1 TXDATA[41]	TSALFR TSALFR_0 TXDATA[36]
5	TXFA_1	GND_CORE	TXSFA	VDD_TTL	TXDATA[23] TXDATA_1[7] TXDATA_2[7]	TXDATA[18] TXDATA_1[2] TXDATA_2[2]	TXEOF_2	TXDATA[9] TXDATA_0[9] TXDATA_1[1]	TXERR_1	TXSOF_1	TXDATA[2] TXDATA_0[2]	TPAL_1 TDOW_1 TXDATA[61]	TPOH_1 TXDATA[53]	TPOHFR_1 TOWC_1 TXDATA[49]	TSAL_3 TROW_3 RXDATA[43]	TSALCK_3 TOWBYC_3 TXDATA[35]
6	TXFA_2	TXPFA	VDD_CORE	GND_CORE	TXPRTY_3	TXEOF_3	TXDATA[21] TXDATA_1[5] TXDATA_2[5]	TXSOF_2	TXDATA[11] TXDAT_0[11] TXDATA_1[3]	TXDATA[7] TXDATA_0[7]	TXDATA[4] TXDATA_0[4]	TXSOF TXS0F_0	TPOHINS_2 TXDATA[58]	TPOHFR_2 TOWC_2 TXDATA[50]	TROW TSAL_2 TXDATA[42]	TDOW TSALCK_2 TXDATA[34]
7	TXPADL[0]	TXPADL_3	TXPADL[1]	TXDATA[28] TXDAT_1[12] TXDATA_3[4]	TXDATA[24] TXDATA_1[8] TXDATA_3[0]	TXDATA[29] TXDAT_1[13] TXDATA_3[5]										
8	TXADDR[0]	TXENB_2	TXPADL[2]	TXFA_0	TXFA_3	TXDATA[30] TXDAT_1[14] TXDATA_3[6]										
9	TXADDR[3]	RXPFA	TXADDR[1]	TXENB TXENB_0	TXENB_3	TXENB_1										
10	RXPADL_3	RXPADL[0]	VDD_TTL	TXADDR[2]	TXCLK_1	TXCLK TXCLK_0										
11	VDD_CORE	RXSOF RXSOF_0	GND_CORE	TXADDR[4]	TXCLK_3	TXCLK_2										
12	RXDATA[2] RXDATA_0[2]	RXFA_0	RXEOF RXEOF_0	RXPRTY RXPRTY_0	RXPADL[2]	RXPADL[1]										
13	RXDATA[4] RXDATA_0[4]	RXDATA[1] RXDATA_0[1]	VDD_TTL	RXDATA[0] RXDATA_0[0]	RXERR RXERR_0	RXVAL RXVAL_0										
14	RXDATA[3] RXDATA_0[3]	RXDATA[7] RXDATA_0[7]	RXSOF_1	RXDATA[5] RXDATA_0[5]	VDD_TTL	RXDATA[6] RXDATA_0[6]										
15	GND_TTL	GND_TTL	RXPRTY_1	RXEOF_1	RXVAL_1	VDD_TTL										
16	GND_TTL	GND_TTL	RXERR_1	RXDATA[8] RXDATA_0[8] RXDATA_1[0]	VDD_CORE	RXDATA[14] RXDAT_0[14] RXDATA_1[6]										
17	RXFA_1	RXDATA[10] RXDAT_0[10] RXDATA_1[2]	GND_CORE]	RXDATA[11] RXDAT_0[11] RXDATA_1[3]	RXCLK RXCLK_0	RXCLK_1										
18	RXDATA[12] RXDAT_0[12] RXDATA_1[4]	RXDATA[9] RXDATA_0[9] RXDATA_1[1]	RXADDR[0]	VDD_TTL	RXCLK_2	RXCLK_3										
19	RXDATA[13] RXDAT_0[13] RXDATA_1[5]	RXADDR[1]	RXADDR[2]	RXENB_1	RXENB RXENB_0	RXENB_2										
20	RXDATA[15] RXDAT_0[15] RXDATA_1[7]	RXADDR[3]	RXENB_3	VDD_TTL	RXFA_2	RXDATA[16] RXDATA_1[0] RXDATA_2[0]										
21	RXADDR[4]]	RXEOF_2	RXERR_2	RXDATA[21] RXDATA_1[5] RXDATA_2[5]	RXDATA[20] RXDATA_1[4] RXDATA_2[4]	GND_CORE										
22	RXSOF_2	RXPRTY_2	RXDATA[19] RXDATA_1[3] RXDATA_2[3]	RXDATA[23] RXDATA_1[7] RXDATA_2[7]	VDD_CORE	VDD_TTL										
23	RXVAL_2	RXDATA[17] RXDATA_1[1] RXDATA_2[1]	RXDATA[22] RXDATA_1[6] RXDATA_2[6]	RXPRTY_3	RXDAT_1[11] RXDATA_3[3] RXDATA[27]	RXDAT_1[15] RXDATA_3[7] RXDATA[31]										
24	VDD_TTL	RXDATA[18] RXDATA_1[2] RXDATA_2[2]	RXERR_3	RXVAL_3	VDD_TTL	RPAL_3 RXDATA[35]										
25	RXEOF_3	RXSOF_3	RXDATA_1[9] RXDATA_3[1] RXDATA[25]	RXDAT_1[13] RXDATA_3[5] RXDATA[29]	VDD_TTL	VDD_CORE										
26	RXFA_3	RXDAT_1[10] RXDATA_3[2] RXDATA[26]	RXDAT_1[12] RXDATA_3[4] RXDATA[28]	RPAL_0 TXDATA[32]	RPOH_0 RDOW_0 RXDATA[36]	RPOHFR_0 ROWBYC_0 RXDATA[40]	VDD_TTL	RMDC RSALFR_1 RXDATA[53]	RSALCK_2 RMOW_2 RXDATA[58]	RSOH_1 RRD_1	RRDC RRDC_1 RSOHCK_1	JTMS	WRB/RWB	A[0]	A[8]	D[3]
27	RXDATA_1[8] RXDATA_3[0] RXDATA[24]	RXDAT_1[14] RXDATA_3[6] RXDATA[30]	RPAL_2 RXDATA[34]	RPOH_3 RDOW_3 RXDATA[39]	RPOHFR_1 ROWBYC_1 RXDATA[41]	RMD RSAL_1 RXDATA[49]	RSAL_2 RMDC_2 RXDATA[50]	RSALCK RMOW_0 RXDATA[56]	RXDATA[63]	RPOWBYC RSOHFR_3 RMD_3	JTDO	VDD_CORE	CSB	UOEN	A[7]	D[2]
28	RPAL_1 RXDATA[33]	RPOH_2 RDOW_2 RXDATA[38]	RPOHFR_2 ROWBYC_2 RXDATA[42]	RPOHCK_2 ROWC_2 RXDATA[46]	RSAL RMDC_0 RXDATA[48]	ROW2 RSALFR_3 RXDATA[55]	RSALCK_3 RMOW_3 RXDATA[59]	RXDATA[62]	RSOH_2 RRD_2	RSOHCK RRDC_0 RSOHCK_0	JTCK	GND_CORE	ALE	A[2]	A[6]	D[1]
29	RPOH_1 RDOW_1 RXDATA[37]	GND_CORE	RPOHFR_3 ROWBYC_3 RXDATA[43]	RPOHCK_3 ROWC_3 RXDATA[47]	RSAL_3 RMDC_3 RXDATA[51]	RSALCK_1 RMOW_1 RXDATA[57]	VDD_CORE	RSOH_0 RRD_0	RSOHFR RMD_0 RSOHFR_0	VDD_TTL	JTRS	SCANTEST	MCUTYPE	A[3]	A[5]	D[0]
30	GND_TTL	GND_TTL	RPOHCK_0 ROWC_0 RXDATA[44]	GND_CORE	RSALFR RROW_0 RXDATA[52]	RXDATA[61]	GND_CORE	RRD RSOHFR_1 RMD_1	ROWC RSOHCK_2 RRDC_2	NC	JTDI	SCANEN	RESET	A[4]	A[10]	GND_TTL
31	GND_TTL	GND_TTL	RPOHCK_1 ROWC_1 RXDATA[45]	VDD_CORE	RSALFR_2 RROW_2 RXDATA[54]	RXDATA[60]	RSOH_3 RRD_3	ROWBYC RSOHFR_2 RMD_2	RPOWC RSOHCK_3 RRDC_3	GENIO	INT	RDB/E	OEN	A[1]	A[9]	GND_TTL

Table 3. Intel IXF6048 Pin Diagram (Bottom View)

U	V	W	Y	AA	AB	AC	AD	AE	AF	AG	AH	AJ	AK	AL	
TMOW TSALFR_2 TXDATA[38]	GND_CORE	TSOHINS_3 TRD_3	TSOH_3 TMD_3	TPOWBYC TSOHFR_3 TRDC_3	TPCI_3 TSCI_3	TPDO[30] TXDATA[62]	TPDO[27] TXDATA[59]	TPDO[23] TXDATA[55]	TPDO[21] TXDATA[53]	TPCI_1 TSCI_1	TPDO[11] TXDATA[43]	TPDO[7] TXDATA[39]	GND_TTL	GND_TTL	1
TSALFR_1 TXDATA[37]	VDD_CORE	TSOHINS_0 TRD_0	TSOH_1 TMD_1	TPOWC TSOHCK_3 TMDC_3	TPCO_3 TSCO_3	TPDO[26] TXDATA[58]	VDD_TTL	TPDO[22] TXDATA[54]	TPCO_1 TSCO_1	TPDO[13] TXDATA[45]	GND_CORE	TPDO[5] TXDATA[37]	GND_TTL	GND_TTL	2
TSALCK_1 TOWBYC_1 TXDATA[33]	TSALCK TOWBYC_0 TXDATA[32]	TSOH_0 TMD_0	TSOHFR TSOHFR_0 TRDC_0	TSOHCK TSOHCK_0 TMDC_0	TPDO[29] TXDATA[61]	TPCO_2 TSCO_2	GND_CORE	VDD_TTL	TPDO[12] TXDATA[44]	TPDO[10] TXDATA[42]	TPCO TSCO_0 TPCO_0	VDD_TTL	GND_TTL	GND_TTL	3
VDD_TTL	TSOHINS_2 TRD_2	TOWBYC TSOHFR_2 TRDC_2	TRDC TSOHCK_1 TMDC_1	VDD_TTL	TPDO[25] TXDATA[57]	TPDO[20] TXDATA[52]	TPDO[19] TXDATA[51]	TPDO[14]] TXDATA[46]	TPDO[9] TXDATA[41]	VDD_CORE	TPDO[2] TXDATA[34]	TPDO[1] TXDATA[33]	GND_TTL	GND_TTL	4
VDD_TTL	TSOH_2 TMD_2	TOWC TSOHCK_2 TMDC_2	TPDO[28] TXDATA[60]	TPCI_2 TSCI_2	TPDO[18] TXDATA[50]	TPDO[17] TXDATA[49]	TPDO[15] TXDATA[47]	TPDO[8] TSDO_1 TXDATA[40]	TPDO[6] TXDATA[38]	TPDO[3] TXDATA[35]	TFPO	VDD_TTL	VDD_TTL	VDD_TTL	5
TSOHINS_1 TRD_1	TMDC TSOHFR_1 TRDC_1	TPDO[31] TXDATA[63]	TPDO[24] TSDO_3 TXDATA[56]	VDD_CORE	TPDO[16] TSDO_2 TXDATA[48]	VDD_TTL	TPCI TSCI_0 TPCI_0	TPDO[4] TXDATA[36]	TPDO[0] TSDO_0 TXDATA[32]	TFPI	VDD_TTL	TPDO_N[15]	TPDO_P[15]	GND_PECL	6
									VDD_TTL	VDD_TTL	GND_PECL	VDD_PECL	TPDO_N[14] TSCO_N3	TPDO_P[14] TSCO_P3	7
									GND_PECL	TPDO_N[13]	TPDO_P[13]	VDD_PECL	TPDO_N[12] TSDO_N3	TPDO_P[12] TSDO_P3	8
									VDD_TTL	GND_CORE	VDD_CORE	GND_PECL	TPDO_N[11]	TPDO_P[11]	9
									VDD_ PECL	TPDO_N[10] TSCO_N2	TPDO_P[10] TSCO_P2	GND_PECL	TPDO_N[9]	TPDO_P[9]	10
									VDD_PECL	TPDO_N[8] TSDO_N2	TPDO_P[8] TSDO_P2	VDD_CORE	GND_PECL	GND_CORE	11
									TPDO_N[7]	TPDO_P[7]	VDD_PECL	GND_PECL	TPDO_P[6] TSCO_P1	TPDO_N[6] TSCO_N1	12
									TPDO_N[5]	TPDO_P[5]	VDD_PECL	TPDO_N[4] TSDO_N1	TPDO_P[4] TSDO_P1	GND_PECL	13
									TPDO_N[3]	TPDO_P[3]	VDD_PECL	TPDO_N[2] TSCO_N0	TPDO_P[2] TSCO_P0	GND_PECL	14
									TPDO_N[1]	TPDO_P[1]	VDD_PECL	TPDO_N[0] TSDO_N0	TPDO_P[0] TSDO_P0	GND_CORE	15
									GND_PECL	TPRTY_N	TPRTY_P	VDD_PECL	TFPO_N	VDD_CORE	16
									TPCO_N	TPCO_P	VDD_PECL	GND_CORE	TFPO_P	GND_PECL	17
									TPCI_N TCCI_N	TPCI_P TCCI_P	TFPI_P	TFPI_N	GND_PECL	VDD_CORE	18
									RFPI_P	RFPI_N	RPCI_P	RPCI_N	GND_PECL	VDD_PECL	19
									RPDI_P[1]	RPDI_N[1]	RPDI_P[0] TSCI_P0	RPDI_N[0] TSCI_N0	RPRTY_P	RPRTY_N	20
									RPDI_P[4] TSCI_P2	RPDI_N[4] TSCI_N2	RPDI_P[3]	RPDI_N[3]	RPDI_P[2] TSCI_P1	RPDI_N[2] TSCI_N1	21
									GND_PECL	VDD_CORE	GND_CORE	VDD_PECL	RPDI_P[5]	RPDI_N[5]	22
									RPDI_P[8] RSDI_P0	RPDI_N[8] RSDI_N0	RPDI_P[7]	RPDI_N[7]	RPDI_P[6] TSCI_P3	RPDI_N[6] TSCI_N3	23
									RPDI_P[11] RSCI_P1	RPDI_N[11] RSCI_N1	RPDI_P[10] RSDI_P1	RPDI_N[10] RSDI_N1	RPDI_P[9] RSCI_P0	RPDI_N[9] RSCI_N0	24
									RPDI_P[14] RSDI_P3	RPDI_N[14] RSDI_N3	RPDI_P[13] RSCI_P2	RPDI_N[13] RSCI_N2	RPDI_P[12] RSDI_P2	RPDI_N[12] RSDI_N2	25
D[9]	GND_CORE	RPDI[0] RSDI_0 RXDATA[32]	RPCI RSCI_0 RPCI_0	RPDI[8] RSDI_1 RXDATA[40]	RPCI_1 RSCI_1	RPDI[16] RSDI_2 RXDATA[48]	RFPI_2	RPDI[24] RSDI_3 RXDATA[56]	RPCI_3 RSCI_3	VDD_TTL	VDD_TTL	VDD_PECL	RPDI_P[15] RSCI_P3	RPDI_N[15] RSCI_N3	26
D[8]	VDD_TTL	RPDI[1] RXDATA[33]	RLOCK_0 RLOCK	ROOF ROOF_0	RPDI[15] RXDATA[47]	RPDI[17] RXDATA[49]	RPDI[22] RXDATA[54]	RPCO_2 RSCO_2	RPDI[29] RXDATA[61]	RFPI_3	RPCO_3 RSCO_3	ROOF_3	VDD_TTL	VDD_TTL	27
D[7]	VDD_TTL	D[14]	RPDI[6] RXDATA[38]	GND_CORE	RPDI[13] RXDATA[45]	RPCO_1 RSCO_1	VDD_TTL	RPDI[21] RXDATA[53]	GND_CORE	RPDI[27] RXDATA[59]	RPDI[31] RXDATA[63]	RLOCK_3	GND_TTL	GND_TTL	28
D[6]	VDD_CORE	D[15]	RPDI[4] RXDATA[36]	RPDI[7] RXDATA[39]	VDD_CORE	RPDI[11] RXDATA[43]	RPDI[14] RXDATA[46]	ROOF_1	RPDI[20] RXDATA[52]	ROOF_2	RPDI[25] RXDATA[57]	RPDI[30] RXDATA[62]	GND_TTL	GND_TTL	29
GND_TTL	D[5]	D[11]	D[12]	RPDI[2] RXDATA[34]	RFPI RFPI_0	RPDI[10] RXDATA[42]	RPDI[12] RXDATA[44]	RFPI_1	RPDI[19] RXDATA[51]	RPCI_2 RSCI_2	VDD_CORE	RPDI[28] RXDATA[60]	GND_TTL	GND_TTL	30
GND_TTL	D[4]	D[10]	D[13]	RPDI[3] RXDATA[35]	RPDI[5] RXDATA[37]	RPCO RSCO_0 RPCO_0	RPDI[9] RXDATA[41]	RLOCK_1	RPDI[18] RXDATA[50]	RPDI[23] RXDATA[55]	RLOCK_2	RPDI[26] RXDATA[58]	GND_TTL	GND_TTL	31

Table 4. Pin Description (Sheet 1 of 66)

Pin Name	Pin	Type	Description
Receive 2,488 Mbit/s Differential PECL Single 16-Bit Parallel Line Side Interface			
RPDI_P[0] RPDI_P[1] RPDI_P[2] RPDI_P[3] RPDI_P[4] RPDI_P[5] RPDI_P[6] RPDI_P[7] RPDI_P[8] RPDI_P[9] RPDI_P[10] RPDI_P[11] RPDI_P[12] RPDI_P[13] RPDI_P[14] RPDI_P[15] RPDI_N[0] RPDI_N[1] RPDI_N[2] RPDI_N[3] RPDI_N[4] RPDI_N[5] RPDI_N[6] RPDI_N[7] RPDI_N[8] RPDI_N[9] RPDI_N[10] RPDI_N[11] RPDI_N[12] RPDI_N[13] RPDI_N[14] RPDI_N[15]	AH20 AF20 AK21 AH21 AF21 AK22 AK23 AH23 AF23 AK24 AH24 AF24 AK25 AH25 AF25 AK26 AJ20 AG20 AL21 AJ21 AG21 AL22 AL23 AJ23 AG23 AL24 AJ24 AG24 AL25 AJ25 AG25 AL26	Diff. LVPECL Input	**Receive Parallel Data Input PECL** The receive PECL single parallel line side interface provides high speed connection (155.52 MHz) to a 2,488 Mbit/s 1:16 demultiplexer. The single 16-bit PECL mode can be used when Intel IXF6048 is configured as a single STS-48c, STM-16c, STS-48, or STM-16 transceiver. RPDI_P/N[15:0] carries the incoming 2,488 Mbit/s data stream in 16-bit format. RPDI_P/N[15:0] are sampled on the rising edge of RPCI_P. RPDI_P/N[15] is the most significant bit (MSB) or first received bit. Connect this pin to the MSB of the deserializer/Demux device, in other words, pin[15] to the MSB through pin[0] to the least significant bit (LSB). For the Intel® GD16524, for example, pin[15] (the MSB on the Intel IXF6048) would be connected to pin[0] (the MSB on the Intel® GD16524).
RPCI_P RPCI_N	AH19 AJ19	Diff. LVPECL Input	**Receive Parallel Clock Input PECL**. RPCI_P/N provides timing for the Intel IXF6048 receiver operation. RPCI_P/N is a 155.52 MHz 50% duty cycle clock that provides timing for the 2,488 Mbit/s receive operation.
RPRTY_P RPRTY_N	AK20 AL20	Diff. LVPECL Input	**Receive Parity Input PECL**. RPRTY_P/N carries the even or odd parity over the receive parallel data input PECL bus (RPDI_P/N[15:0]). RPRTY_P/N is sampled on the rising edge of RPCI_P.
NOTE: See notes 1, 2, and 3 at the end of the table.			

Table 4. Pin Description (Sheet 2 of 66)

Pin Name	Pin	Type	Description
RFPI_P RFPI_N	AF19 AG19	Diff. LVPECL Input	**Receive Frame Position Input PECL**. RFPI_P/N is an active-high frame position input allowing connection to an external OC-192 SONET/SDH demultiplexer. RFPI_P/N indicates the SONET/SDH frame position on the RPDI_P/N[15:0] bus. The byte position indicated by RFPI_P/N is selected by using RcvFPICnf[7:0] (global register R_FPCNF). RFPI_P/N should be active-high for a single RPCI_P/N period. Intel IXF6048 ignores pulses on RFPI_P/N while “in frame” (ROOF_0 = '0'). RFPI_P/N is sampled on the rising edge of RPCI_P When frame alignment is enabled (bit RcvFBaDsbl = ‘0’ in register R_RSTC), RFPI_P have to be tied to GND_PECL and RFPI_N should be tied to VDD_PECL.
RLOCK	Y27	LVTTL Input	**Receive Lock Detect TTL**. RLOCK is the active-high Lock Detect input. RLOCK indicates that the external clock recovery PLL is locked. RLOCK is not required to be synchronous with RPCI_P/N.
ROOF	AA27	LVTTL Output 12 mA	**Receive Out of Frame TTL**. ROOF is high while the receiver is “out of frame” and low while it is “in frame.” ROOF is updated on the rising edge of RPCI_P.
RPCO	AC31	LVTTL Output 12 mA	**Receive Parallel Clock Output TTL**. RPCO is a divided version of RPCI_P. RcvCOCnf[2:0] (register R_COCNF) configures the RPCO output as a 77.76 MHz, 38.88 MHz, 19.44 MHz, or 8 KHz clock.
NOTE: See notes 1, 2, and 3 at the end of the table.			

Table 4. Pin Description (Sheet 3 of 66)

Pin Name	Pin	Type	Description
Transmit 2,488 Mbit/s Differential PECL Single 16-Bit Parallel Line Side Interface			
TPDO_P[0] TPDO_P[1] TPDO_P[2] TPDO_P[3] TPDO_P[4] TPDO_P[5] TPDO_P[6] TPDO_P[7] TPDO_P[8] TPDO_P[9] TPDO_P[10] TPDO_P[11] TPDO_P[12] TPDO_P[13] TPDO_P[14] TPDO_P[15] TPDO_N[0] TPDO_N[1] TPDO_N[2] TPDO_N[3] TPDO_N[4] TPDO_N[5] TPDO_N[6] TPDO_N[7] TPDO_N[8] TPDO_N[9] TPDO_N[10] TPDO_N[11] TPDO_N[12] TPDO_N[13] TPDO_N[14] TPDO_N[15]	AK15 AG15 AK14 AG14 AK13 AG13 AK12 AG12 AH11 AL10 AH10 AL9 AL8 AH8 AL7 AK6 AJ15 AF15 AJ14 AF14 AJ13 AF13 AL12 AF12 AG11 AK10 AG10 AK9 AK8 AG8 AK7 AJ6	Diff. LVPECL Output	**Transmit Parallel Data Output PECL** The transmit PECL single parallel line side interface provides high speed connection (155.52 MHz) to a 2,488 Mbit/s 16:1 multiplexer. The single 16-bit PECL mode can be used when Intel IXF6048 is configured as a single STS-48c, STM-16c, STS-48, or STM-16 transceiver. TPDO_P/N[15:0] carries the outgoing 2,488 Mbit/s data stream. TPDO_P/N[15:0] are updated on the rising edge of the selected transmit clock (either TPCI_P or RPCI_P)—see T_COCNF:XmtTimRef. TPDO_P/N[15] is the MSB or first transmitted bit. Connect this pin to the MSB of the serializer/Mux device, in other words, pin[15] to the MSB through pin[0] to the LSB. For the Intel® GD16523, for example, pin[15] (the MSB on the Intel IXF6048) would be connected to pin[0] (the MSB on the Intel® GD16523).
TPCI_P TPCI_N	AG18 AF18	Diff. LVPECL Input	**Transmit Parallel Clock Input PECL**. TPCI_P/N provides timing for the Intel IXF6048 transmitter operation. TPCI_P/N is a 155.52 MHz 50% duty cycle clock which provides timing for the 2,488 Mbit/s transmit operation.
TPRTY_P TPRTY_N	AH16 AG16	Diff. LVPECL Output	**Transmit Parity Output**. TPRTY_P/N carries the even/odd parity over the transmit parallel data output PECL bus (TPDO_P/N[15:0]). TPRTY_P/N is updated on the rising edge of TPCO_P.
NOTE: See notes 1, 2, and 3 at the end of the table.			

Table 4. Pin Description (Sheet 4 of 66)

Pin Name	Pin	Type	Description
TPCO_P TPCO_N	AG17 AF17	Diff. LVPECL Output	**Transmit Parallel Clock Output PECL**. TPCO_P/N is the transmit output timing reference when Intel IXF6048 is configured in single transceiver mode. TPCO_P/N is a flowed through version of the clock used by the transmitter (TPCI_P/N or RPCI_P/N). XmtPClkOut (configuration register T_COCNF) allows tristating of the TPCO_P/N output. The transmitter can be configured in two different modes (XmtTimRef, register T_COCNF): • Clocked by the transmit parallel clock input TPCI_P/N (XmtTimRef[1:0] = '10') • Clocked by the receive parallel clock input RPCI_P/N (XmtTimRef[1:0] = '01') **NOTE:** In the line loopback mode of operation, the TPCO_P/N clocks are derived from the RPCI_P/N clock input, because the transmitter's internal clock source is automatically switched to the RPCI_P/N clock input in that case.
TFPI_P TFPI_N	AH18 AJ18	Diff. LVPECL Input	**Transmit Frame Position Input PECL**. TFPI_P/N is an active-high frame position input providing connection to an external OC-192 SONET/SDH multiplexer. TFPI_P/N is used to align the SONET/SDH frames generated by Intel IXF6048 to an external 8-KHz system reference. Select the byte position indicated by TFPI_P/N by configuring XmtFPICnf[7:0] (global register T_FPCNF). TFPI_P/N should be active-high for a single TPCI_P/N period. TFPI_P/N is sampled on the rising edge of TPCI_P. If it is not required that the frames are aligned to an external source, TFPI_P have to be tied to GND_PECL and TFPI_N to VCC_PECL.
TFPO_P TFPO_N	AK17 AK16	Diff. LVPECL Output	**Transmit Frame Position Output PECL**. TFPO_P/N is an active-high frame position output pulse. TFPO_P is an active-high 8-KHz pulse indicating the position of the SONET/SDH frame on the TPDO_P/N bus. Select the byte position indicated by TFPO_P/N by configuring XmtFPOCnf[7:0] (global register T_FPCNF). TFPO_P/N is active-high for a single TPCI_P/N period. TFPO_P/N is updated on the rising edge of TPCI_P.
TPCO	AH3	LVTTL Output 12 mA	**Transmit Parallel Clock Output TTL**. TPCO is a flowed through or divided version of the clock used by the transmitter (TPCI_P or RPCI_P). XmtCOCnf (register T_COCNF) configures the TPCO output as a 77.76 MHz, 38.88 MHz, 19.44 MHz, or 8-KHz clock. **NOTE:** In the line loopback mode of operation, the TPCO clock is derived from the RPCI_P clock input, because the transmitter's internal clock source is automatically switched to the RPCI_P clock input in that case.
NOTE: See notes 1, 2, and 3 at the end of the table.			

Table 4. Pin Description (Sheet 5 of 66)

Pin Name	Pin	Type	Description
Receive 155/51 Mbit/s Differential PECL Quad 1-Bit Serial Line Side Interface			
RSDI_P0 RSDI_P1 RSDI_P2 RSDI_P3 RSDI_N0 RSDI_N1 RSDI_N2 RSDI_N3	AF23 AH24 AK25 AF25 AG23 AJ24 AL25 AG25	Diff. LVPECL Input	**Receive Serial Data Input PECL** RSDI_Pi/Ni (i = 0, 1, 2, 3) carries the incoming 155/51 Mbit/s SONET/SDH data stream processed by channel #i. When Intel IXF6048 is configured as a single STS-3 (non-concatenated) transceiver, RSDI_P1/N1, RSDI_P2/N2, and RSDI_P3/N3 are unused inputs. RSDI_Pi/Ni is sampled on the rising edge of RSCI_Pi (i = 0, 1, 2, 3).
RSCI_P0 RSCI_P1 RSCI_P2 RSCI_P3 RSCI_N0 RSCI_N1 RSCI_N2 RSCI_N3	AK24 AF24 AH25 AK26 AL24 AG24 AJ25 AL26	Diff. LVPECL Input	**Receive Serial Clock Input PECL** RSCI_Pi/Ni (i = 0, 1, 2, 3) provides timing for channel #i receiver operation. RSCI_Pi/Ni is a 51.84 MHz (STS-1) or a 155.52 MHz (STS-3c/STM-1) 50% duty cycle clock, providing timing for the receive operation on channel #i (i = 0, 1, 2, 3). When Intel IXF6048 is configured as a single STS-3 (non-concatenated) transceiver, RSCI_P1/N1, RSCI_P2/N2 and RSCI_P3/N3 are unused inputs.
RSCO_0 RSCO_1 RSCO_2 RSCO_3	AC31 AC28 AE27 AH27	LVTTL Output 12 mA	**Receive Serial Clock Output TTL**. RSCO_i (i = 0, 1, 2, 3) is a divided version of RSCI_Pi. RcvCOCnf (register R_COCNF) configures the RSCO_i (i = 0, 1, 2, 3) outputs as a 77.76 MHz/38.88 MHz/19.44 MHz/8-KHz clock (OC-3) or as a 51.84 MHz/25.92 MHz/12.96 MHz/6.48 MHz/8-KHz clock (OC-1). When the Intel IXF6048 is configured as a single STS-3 (non-concatenated) transceiver, RSCO_1, RSCO_2, and RSCO_3 are tristated.
RLOCK_0 RLOCK_1 RLOCK_2 RLOCK_3	Y27 AE31 AH31 AJ28	LVTTL Input	**Receive Lock Detect TTL**. RLOCK_i (i = 0, 1, 2, 3) is the active-high Lock Detect input for channel #i. RLOCK_i indicates that the external clock recovery PLL used by channel #i is locked. When Intel IXF6048 is configured as a single STS-3 (non-concatenated) transceiver, RLOCK_1, RLOCK_2, and RLOCK_3 are unused inputs. RLOCK_i (i = 0, 1, 2, 3) does not require synchronization with RSCI_Pi/Ni.
ROOF_0 ROOF_1 ROOF_2 ROOF_3	AA27 AE29 AG29 AJ27	LVTTL Output 12 mA	**Receive Out of Frame TTL**. ROOF_i (i = 0, 1, 2, 3) is high while receive channel #i is “out of frame” and low while it is “in frame”. When Intel IXF6048 is configured as a single STS-3 (non-concatenated) transceiver, ROOF_1, ROOF_2, and ROOF_3 are tristated. ROOF_i is updated on the rising edge of RSCI_i (i = 0, 1, 2, 3).
NOTE: See notes 1, 2, and 3 at the end of the table.			

Table 4. Pin Description (Sheet 6 of 66)

Pin Name	Pin	Type	Description
Transmit 155/51 Mbit/s Differential PECL Quad 1-Bit Serial Line Side Interface			
TSDO_P0 TSDO_P1 TSDO_P2 TSDO_P3 TSDO_N0 TSDO_N1 TSDO_N2 TSDO_N3	AK15 AK13 AH11 AL8 AJ15 AJ13 AG11 AK8	Diff. LVPECL Output	**Transmit Serial Data Output PECL** TSDO_Pi/Ni (i = 0, 1, 2, 3) carries the outgoing 155/51 Mbit/s SONET/SDH data stream generated by channel #i. TSDO_Pi/Ni is updated on the rising edge of TSCI_Pi (i = 0, 1, 2, 3).
TSCO_P0 TSCO_P1 TSCO_P2 TSCO_P3 TSCO_N0 TSCO_N1 TSCO_N2 TSCO_N3	AK14 AK12 AH10 AL7 AJ14 AL12 AG10 AK7	Diff. LVPECL Output	**Transmit Serial Clock Output PECL**. TSCO_P/N[i] (i = 0, 1, 2, 3) is a flowed through version of the clock used by transmit channel #i (RSCI_P/N[i], TSCI_P/N[i] or TCCI_P/N). XmtPClkOut (configuration register T_COCNF) allows tristating the TSCO_P/N[i] outputs. In the line loopback mode of operation, the TSCO_P/N[i] clocks are derived from the RSCI_P/N[i] clock input, because the transmitter's internal clock source is automatically switched to the RSCI_P/N[i] clock input in that case. XmtTimRef (register T_COCNF) configures the transmitter clock source for each channel: • Clocked by the corresponding receive serial clock input RSCI_P/N[i] (XmtTimRef[1:0] = '01') • Clocked by its own (per channel) clock input TSCI_P/N[i] (XmtTimRef[1:0] = '10') • Clocked by the transmit common clock input TCCI_P/N (XmtTimRef[1:0] = '11') **NOTE:** In the line loopback mode of operation, the TSCO_P/N[i] clocks are derived from the RSCI_P/N[i] clock input, because the transmitter's internal clock source is automatically switched to the RSCI_P/N[i] clock input in that case.
TSCI_P0 TSCI_P1 TSCI_P2 TSCI_P3 TSCI_N0 TSCI_N1 TSCI_N2 TSCI_N3	AH20 AK21 AF21 AK23 AJ20 AL21 AG21 AL23	Diff. LVPECL Input	**Transmit Serial Clock Input PECL**. TSCI_P/N[i] (i = 0, 1, 2, 3) provides timing for channel #i transmitter operation. TSCI_Pi/Ni is a 155.52 MHz (STS-3c/STM-1) or a 51.84 MHz (STS-1) 50% duty cycle clock that provides timing for the transmit operation of channel #i (i = 0, 1, 2, 3).
NOTE: See notes 1, 2, and 3 at the end of the table.			

Table 4. Pin Description (Sheet 7 of 66)

Pin Name	Pin	Type	Description
TSCO_0 TSCO_1 TSCO_2 TSCO_3	AH3 AF2 AC3 AB2	LVTTL Output 12 mA	**Transmit Serial Clock Output TTL**. TSCO_i (i = 0, 1, 2, 3) is a flowed through or divided version of the clock used by the transmit channel #i (RSCI_Pi, TSCI_Pi or TCCI_P). XmtCOCnf (register R_COCNF) configures the TSCO_i (i = 0, 1, 2, 3) outputs as a 77.76 MHz/38.88 MHz/19.44 MHz/8 KHz clock (OC-3) or as a 51.84 MHz/25.92 MHz/12.96 MHz/6.48 MHz/8 KHz clock (OC-1). XmtTimRef (register T_COCNF) configures the transmitter clock source for each channel: • Clocked by the corresponding receive serial clock input RSCI_Pi (XmtTimRef[1:0] = '01') • Clocked by its own (per channel) clock input TSCI_Pi (XmtTimRef[1:0] = '10') • Clocked by the transmit common clock input TCCI_P (XmtTimRef[1:0] = '11') **NOTE:** In the line loopback mode of operation, the TSCO_i clocks are derived from the RSCI_Pi clock input, because the transmitter's internal clock source is automatically switched to the RSCI_Pi clock input in that case.
TCCI_P TCCI_N	AG18 AF18	Diff. LVPECL Input	**Transmit Common Clock Input PECL**. TCCI_P/N can be used as a common timing reference for each Intel IXF6048 transmit channel. TCCI_P/N is a 155.52 MHz (STS-3c/STM-1) or a 51.84 MHz (STS-1) 50% duty cycle clock that provides timing for the four transmitters.
NOTE: See notes 1, 2, and 3 at the end of the table.			

Table 4. Pin Description (Sheet 8 of 66)

Pin Name	Pin	Type	Description
Receive 2,488 Mbit/s TTL Single 32-Bit Parallel Line Side Interface			
RPDI[0] RPDI[1] RPDI[2] RPDI[3] RPDI[4] RPDI[5] RPDI[6] RPDI[7] RPDI[8] RPDI[9] RPDI[10] RPDI[11] RPDI[12] RPDI[13] RPDI[14] RPDI[15] RPDI[16] RPDI[17] RPDI[18] RPDI[19] RPDI[20] RPDI[21] RPDI[22] RPDI[23] RPDI[24] RPDI[25] RPDI[26] RPDI[27] RPDI[28] RPDI[29] RPDI[30] RPDI[31]	W26 W27 AA30 AA31 Y29 AB31 Y28 AA29 AA26 AD31 AC30 AC29 AD30 AB28 AD29 AB27 AC26 AC27 AF31 AF30 AF29 AE28 AD27 AG31 AE26 AH29 AJ31 AG28 AJ30 AF27 AJ29 AH28	LVTTL Input	**Receive Parallel Data Input TTL** The receive TTL single parallel line side interface provides low speed connection (≤ 77.76 MHz) to 2,488 Mbit/s demultiplexers. The single 32-bit mode can be used when Intel IXF6048 is configured as a single STS-48c, STM-16c, STS-48, or STM-16 transceiver. RPDI[31:0] carries the incoming 2,488 Mbit/s data stream in 32-bit format. RPDI[31] is the most significant bit (first received bit) and RPDI[0] is the least significant bit (last received bit). RPDI[31:0] are sampled on the rising edge of RPCI. RPDI_P/N[31] is the MSB or first received bit. Connect this pin to the MSB of the deserializer/Demux device, in other words, pin[31] to the MSB through pin[0] to the LSB.
RPCI	Y26	LVTTL Input	**Receive Parallel Clock Input TTL**. RPCI provides timing for the Intel IXF6048 receiver operation. RPCI is a 77.76 MHz 50% duty cycle clock that provides timing for the 2,488 Mbit/s receive operation.
RPCO	AC31	LVTTL Output 12 mA	**Receive Parallel Clock Output TTL**. RPCO is a divided version of RPCI. RcvCOCnf (register R_COCNF) configures the RPCO output as a 77.76 MHz, 38.88 MHz, 19.44 MHz, or 8-KHz clock.
RLOCK	Y27	LVTTL Input	**Receive Lock Detect TTL**. RLOCK is the active-high Lock Detect input. RLOCK indicates that the external clock recovery PLL is locked. RLOCK is an asynchronous input.
ROOF	AA27	LVTTL Output 12 mA	**Receive Out of Frame TTL**. ROOF is high while the receiver is “out of frame” and low while it is “in frame”. ROOF is updated on the rising edge of RPCI.
NOTE: See notes 1, 2, and 3 at the end of the table.			

Table 4. Pin Description (Sheet 9 of 66)

Pin Name	Pin	Type	Description
RFPI	AB30	LVTTL Input	**Receive Frame Position Input TTL**. RFPI is an active-high frame position input allowing connection to an external OC-192 SONET/SDH demultiplexer. RFPI indicates the SONET/SDH frame position on the RPDI[31:0] bus. Select the byte position indicated by RFPI by using RcvFPICnf[7:0] (global register R_FPCNF). RFPI should be active-high for a single RPCI period. Intel IXF6048 ignores pulses on RFPI while “in frame” (ROOF = '0'). RFPI is sampled on the rising edge of RPCI. When frame alignment is enabled (bit RcvFBaDsbl = ‘0’ in register R_RSTC), RFPI have to be tied to GND.
NOTE: See notes 1, 2, and 3 at the end of the table.			

Table 4. Pin Description (Sheet 10 of 66)

Pin Name	Pin	Type	Description
Transmit 2,488 Mbit/s TTL Single Parallel Line Side Interface			
TPDO[0] TPDO[1] TPDO[2] TPDO[3] TPDO[4] TPDO[5] TPDO[6] TPDO[7] TPDO[8] TPDO[9] TPDO[10] TPDO[11] TPDO[12] TPDO[13] TPDO[14] TPDO[15] TPDO[16] TPDO[17] TPDO[18] TPDO[19] TPDO[20] TPDO[21] TPDO[22] TPDO[23] TPDO[24] TPDO[25] TPDO[26] TPDO[27] TPDO[28] TPDO[29] TPDO[30] TPDO[31]	AF6 AJ4 AH4 AG5 AE6 AJ2 AF5 AJ1 AE5 AF4 AG3 AH1 AF3 AG2 AE4 AD5 AB6 AC5 AB5 AD4 AC4 AF1 AE2 AE1 Y6 AB4 AC2 AD1 Y5 AB3 AC1 W6	LVTTL Output 12 mA	**Transmit Parallel Data Output TTL** The transmit TTL single parallel line side interface provides low speed connection (≤ 77.76 MHz) to 2,488 Mbit/s multiplexers. The single 32-bit mode can be used when Intel IXF6048 is configured as a single STS-48c, STM-16c, STS-48, or STM-16 transceiver. TPDO[31:0] carry the outgoing 2,488 Mbit/s data stream in 32-bit format. TPDO[31] is the most significant bit (first transmitted bit) and TPDO[0] is the least significant bit (last transmitted bit). TPDO[31:0] is updated on the rising edge of TPCO. TPDO[31] is the MSB or first transmitted bit. Connect this pin to the MSB of the serializer/Mux device, in other words, pin[31] to the MSB through pin[0] to the LSB.
TPCI	AD6	LVTTL Input	**Transmit Parallel Clock Input TTL**. TPCI is a 77.76 MHz 50% duty cycle clock, providing timing for the transmit operation at 2,488 Mbit/s.
TPCO	AH3	LVTTL Output 12 mA	**Transmit Parallel Clock Output TTL**. TPCO is a flow-through or divided version of the clock used by the transmitter (TPCI or RPCI). XmtCOCnf (register T_COCNF) configures the TPCO output as a 77.76 MHz, 38.88 MHz, 19.44 MHz, or 8-KHz clock. XmtTimRef (register T_COCNF) configures the transmitter in two different modes: • Clocked by the transmit parallel clock input TPCI (XmtTimRef = '10') • Clocked by the receive parallel clock input RPCI (XmtTimRef = '01') **NOTE:** In the line loopback mode of operation, the TPCO clock is derived from the RPCI clock input, because the transmitter's internal clock source is automatically switched to the RPCI clock input in that case.
NOTE: See notes 1, 2, and 3 at the end of the table.			

Table 4. Pin Description (Sheet 11 of 66)

Pin Name	Pin	Type	Description
TFPI	AG6	LVTTL Input	**Transmit Frame Position Input TTL**. TFPI is an active-high frame position input providing connection to an external OC-192 SONET/SDH multiplexer. TFPI is used to align the SONET/SDH frames generated by Intel IXF6048 to an external 8-KHz system reference. Select the byte position indicated by TFPI by configuring XmtFPICnf[7:0] (global register T_FPCNF). TFPI should be active-high for a single TPCI period. TFPI is sampled on the rising edge of TPCI. If it is not required that the frames are aligned to an external source, TFPI have to be tied to GND
TFPO	AH5	LVTTL Output 12 mA	**Transmit Frame Position Output TTL**. TFPO is an active-high frame position output. TFPO is an active-high pulse indicating the position of the SONET/SDH frame on the TPDO bus. The byte position indicated by TFPO is selected by configuring XmtFPOCnf[7:0] (global register T_FPCNF). TFPO is active-high for a single TPCI period. TFPO is updated on the rising edge of TPCI.
NOTE: See notes 1, 2, and 3 at the end of the table.			

Table 4. Pin Description (Sheet 12 of 66)

Pin Name	Pin	Type	Description
Receive 622/155/51 Mbit/s TTL Quad Parallel Line Side Interface			
RPDI_0[0] RPDI_0[1] RPDI_0[2] RPDI_0[3] RPDI_0[4] RPDI_0[5] RPDI_0[6] RPDI_0[7] RPDI_1[0] RPDI_1[1] RPDI_1[2] RPDI_1[3] RPDI_1[4] RPDI_1[5] RPDI_1[6] RPDI_1[7] RPDI_2[0] RPDI_2[1] RPDI_2[2] RPDI_2[3] RPDI_2[4] RPDI_2[5] RPDI_2[6] RPDI_2[7] RPDI_3[0] RPDI_3[1] RPDI_3[2] RPDI_3[3] RPDI_3[4] RPDI_3[5] RPDI_3[6] RPDI_3[7]	W26 W27 AA30 AA31 Y29 AB31 Y28 AA29 AA26 AD31 AC30 AC29 AD30 AB28 AD29 AB27 AC26 AC27 AF31 AF30 AF29 AE28 AD27 AG31 AE26 AH29 AJ31 AG28 AJ30 AF27 AJ29 AH28	LVTTL Input	**Receive Parallel Data Input TTL** The receive TTL quad parallel line side interface provides low speed connection (≤ 77.76 MHz) to 622, 155, or 51 Mbit/s demultiplexers. The quad 8-bit mode can be used when Intel IXF6048 is configured as a quad STS-12c, STM-4c, STS-3c, STM-1, STS-1, or STM-0 transceiver. RPDI_i[7:0] (i = 0, 1, 2, 3) carry the incoming 622, 155, or 51 Mbit/s data stream, in byte format, for channel #i. RPDI_i[7] is the MSB (first received bit) and RPDI_i[0] is the LSB (last received bit). Connect pin[7] to the MSB of the deserializer/Demux device, in other words, pin[7] to the MSB through pin[0] to the LSB. For the Intel® GD16592A, for example, pin[7] (the MSB on the Intel IXF6048) would be connected to pin[0] (the MSB on the Intel® GD16592A). When Intel IXF6048 is configured as a single STS-12, STM-4, or STS-3 (non-concatenated or concatenated) transceiver, RPDI_1[7:0], RPDI_2[7:0] and RPDI_3[7:0] are unused inputs. RPDI_i[7:0] (i = 0, 1, 2, 3) are sampled on the rising edge of RPCI_i.
RPCI_0 RPCI_1 RPCI_2 RPCI_3	Y26 AB26 AG30 AF26	LVTTL Input	**Receive Parallel Clock Input TTL**. RPCI_i (i = 0, 1, 2, 3) provide timing for receive channel #i operation. RPCI_i is a 77.76 MHz (622.08 Mbit/s), a 19.44 MHz (155.52 Mbit/s), or a 6.48 MHz (51.84 Mbit/s) 50% duty cycle clock that provides timing for the receive operation on channel #i (i = 0, 1, 2, 3). When Intel IXF6048 is configured as a single STS-12, STM-4, or STS-3 (non-concatenated or concatenated) transceiver, RPCI_1, RPCI_2, and RPCI_3 are unused inputs.
NOTE: See notes 1, 2, and 3 at the end of the table.			

Table 4. Pin Description (Sheet 13 of 66)

Pin Name	Pin	Type	Description
RPCO_0 RPCO_1 RPCO_2 RPCO_3	AC31 AC28 AE27 AH27	LVTTL Output 12 mA	**Receive Parallel Clock Output TTL**. RPCO_i (i = 0, 1, 2, 3) is a flow-through or divided version of RPCI_i. RcvCOCnf (register R_COCNF) configures the RPCO_i (i = 0, 1, 2, 3) outputs as a 77.76 MHz, 38.88 MHz, 19.44 MHz, or 8-KHz clock. When Intel IXF6048 is configured as a single STS-12, STM-4, or STS-3 (non-concatenated or concatenated) transceiver, RPCO_1, RPCO_2, and RPCO_3 are tristated.
RLOCK_0 RLOCK_1 RLOCK_2 RLOCK_3	Y27 AE31 AH31 AJ28	LVTTL Input	**Receive Lock Detect TTL**. RLOCK_i (i = 0, 1, 2, 3) is the active-high Lock Detect input for channel #i. RLOCK_i indicates that the external clock recovery PLL used by channel #i is locked. When Intel IXF6048 is configured as a single STS-12, STM-4, or STS-3 (non-concatenated or concatenated) transceiver, RLOCK_1, RLOCK_2, and RLOCK_3 are unused inputs. RLOCK_i (i = 0, 1, 2, 3) are asynchronous inputs.
ROOF_0 ROOF_1 ROOF_2 ROOF_3	AA27 AE29 AG29 AJ27	LVTTL Output 12 mA	**Receive Out of Frame TTL**. ROOF_i (i = 0, 1, 2, 3) is high while receive channel #i is “out of frame” and low while it is “in frame”. When Intel IXF6048 is configured as a single STS-12/STM-4/STS-3 (non-concatenated or concatenated) transceiver, ROOF_1, ROOF_2 and ROOF_3 are tristated. ROOF_i is updated on the rising edge of RPCI_i (i = 0, 1, 2, 3).
RFPI_0 RFPI_1 RFPI_2 RFPI_3	AB30 AE30 AD26 AG27	LVTTL Input	**Receive Frame Position Input TTL**. RFPI_i (i = 0, 1, 2, 3) are active-high frame position inputs providing connection to an external SONET/SDH demultiplexer. RFPI_i (i = 0, 1, 2, 3) indicates the SONET/SDH frame position on the RPDI_i[7:0] bus. Select the byte position indicated by RFPI_i (i = 0, 1, 2, 3) by using RcvFPICnf[7:0] (global register R_FPCNF). RFPI_i (i = 0, 1, 2, 3) should be active-high for a single RPCI_i period. Receive channel #i ignores pulses on RFPI_i while “in frame” (ROOF_i = '0'). When Intel IXF6048 is configured as a single STS-12, STM-4, or STS-3 (non-concatenated or concatenated) transceiver, RFPI_1, RFPI_2, and RFPI_3 are unused inputs. RFPI_i is sampled on the rising edge of RPCI_i (i = 0, 1, 2, 3). When frame alignment is enabled (bit RcvFBaDsbl = ‘0’ in register R_RSTC), RFPI_i have to be tied to GND.
NOTE: See notes 1, 2, and 3 at the end of the table.			

Table 4. Pin Description (Sheet 14 of 66)

Pin Name	Pin	Type	Description
Transmit 622/155/51 Mbit/s TTL Quad Parallel Line Side Interface			
TPDO_0[0] TPDO_0[1] TPDO_0[2] TPDO_0[3] TPDO_0[4] TPDO_0[5] TPDO_0[6] TPDO_0[7] TPDO_1[0] TPDO_1[1] TPDO_1[2] TPDO_1[3] TPDO_1[4] TPDO_1[5] TPDO_1[6] TPDO_1[7] TPDO_2[0] TPDO_2[1] TPDO_2[2] TPDO_2[3] TPDO_2[4] TPDO_2[5] TPDO_2[6] TPDO_2[7] TPDO_3[0] TPDO_3[1] TPDO_3[2] TPDO_3[3] TPDO_3[4] TPDO_3[5] TPDO_3[6] TPDO_3[7]	AF6 AJ4 AH4 AG5 AE6 AJ2 AF5 AJ1 AE5 AF4 AG3 AH1 AF3 AG2 AE4 AD5 AB6 AC5 AB5 AD4 AC4 AF1 AE2 AE1 Y6 AB4 AC2 AD1 Y5 AB3 AC1 W6	LVTTL Input 12 mA	**Transmit Parallel Data Output TTL** The transmit TTL quad parallel line side interface provides low speed connection (≤ 77.76 MHz) to 622/155/51 Mbit/s multiplexers. The quad 8-bit mode can be used when Intel IXF6048 is configured as a Quad STS-12c/STM-4c/STS-3c/STM-1/STS-1/STM-0 transceiver. TPDO_i[7:0] (i = 0, 1, 2, 3) carries the outgoing 622/155/51 Mbit/s data stream in byte format for channel #i. TPDO_i[7] is the MSB (first transmitted bit) and TPDO_i[0] is the LSB (last transmitted bit). Connect pin[7] to the MSB of the serializer/Mux device, in other words, pin[7] to the MSB through pin[0] to the LSB. For the Intel® GD16591A, for example, pin[7] (the MSB on the Intel IXF6048) would be connected to pin[0] (the MSB on the Intel® GD16591A). When Intel IXF6048 is configured as a single STS-12/STM-4/STS-3 (non-concatenated or concatenated) transceiver, TPDO_1[7:0], TPDO_2[7:0], and TPDO_3[7:0] are tristated. TPDO_i[7:0] (i = 0, 1, 2, 3) is updated on the rising edge of TPCO_i.
TPCI_0 TPCI_1 TPCI_2 TPCI_3	AD6 AG1 AA5 AB1	LVTTL Input	**Transmit Parallel Clock Input TTL**. TPCI_i (i = 0, 1, 2, 3) provides timing for receive channel #i operation. TPCI_i is a 77.76 MHz (622.08 Mbit/s), a 19.44 MHz (155.52 Mbit/s), or a 6.48 MHz (51.84 Mbit/s) 50% duty cycle clock, providing timing for the receive operation on channel #i (i = 0, 1, 2, 3). When Intel IXF6048 is configured as a single STS-12/STM-4/STS-3 (non-concatenated or concatenated) transceiver, TPCI_1, TPCI_2, and TPCI_3 are unused inputs.
NOTE: See notes 1, 2, and 3 at the end of the table.			

Table 4. Pin Description (Sheet 15 of 66)

Pin Name	Pin	Type	Description
TPCO_0 TPCO_1 TPCO_2 TPCO_3	AH3 AF2 AC3 AB2	LVTTL Output 12 mA	**Transmit Parallel Clock Output TTL**. TPCO_i (i = 0, 1, 2, 3) is a flow-through or divided version of TPCI_i or RPCI_i. XmtCOCnf (register T_COCNF) configures the TPCO_i (i = 0, 1, 2, 3) outputs as a 77.76 MHz/38.88 MHz/19.44 MHz/8-KHz clock. When Intel IXF6048 is configured as a single STS-12/STM-4/STS-3 (non-concatenated or concatenated) transceiver, TPCO_1, TPCO_2, and TPCO_3 are tristated XmtTimRef (register T_COCNF) configures the transmitter in two different modes: • Clocked by the transmit parallel clock input TPCI_i (XmtTimRef = '10') • Clocked by the receive parallel clock input RPCI_i (XmtTimRef = '01') **NOTE:** In the line loopback mode of operation, the TPCO_i clocks are derived from the RPCI_i clock input, because the transmitter's internal clock source is automatically switched to the RPCI_i clock input in that case.
TFPI	AG6	LVTTL Input	**Transmit Frame Position Input TTL**. TFPI is the active-high frame position input. TFPI can only be used when the four transmit channels use the common clock input (TPCI_0). TFPI is used to align the SONET/SDH frames generated by the four transmit channels to an external 8-KHz system reference. The byte position indicated by TFPI is selected by configuring XmtFPICnf[7:0] (global register T_FPCNF). TFPI should be active-high for a single TPCI_0 period. TFPI is sampled on the rising edge of TPCI_0. If it is not required that the frames are aligned to an external source, TFPI have to be tied to GND
TFPO	AH5	LVTTL Output 12 mA	**Transmit Frame Position Output TTL**. TFPO is an active-high frame position output. TFPO is an active-high pulse indicating the position of the SONET/SDH frame on the TPDO_0[7:0]. The byte position indicated by TFPO is selected by configuring XmtFPOCnf[7:0] (global register T_FPCNF). TFPO is active-high for a single TPCI_0 period. TFPO is updated on the rising edge of TPCI_0.
NOTE: See notes 1, 2, and 3 at the end of the table.			

Table 4. Pin Description (Sheet 16 of 66)

Pin Name	Pin	Type	Description
Receive 51 Mbit/s TTL Quad Serial Line Side Interface			
RSDI_0 RSDI_1 RSDI_2 RSDI_3	W26 AA26 AC26 AE26	LVTTL Input	**Receive Serial Data Input TTL** The receive TTL quad serial line side interface provides connection to serial 51.84 Mbit/s demultiplexers. The quad serial mode can be used when Intel IXF6048 is configured as a Quad STS-1/STM-0 transceiver. RSDI_i (i = 0, 1, 2, 3) carries the incoming 51 Mbit/s serial data stream for channel #i. RSDI_i (i = 0, 1, 2, 3) is sampled on the rising edge of RSCI_i.
RSCI_0 RSCI_1 RSCI_2 RSCI_3	Y26 AB26 AG30 AF26	LVTTL Input	**Receive Serial Clock Input TTL**. RSCI_i (i = 0, 1, 2, 3) provides timing for receive channel #i operation. RSCI_i is a 51.84 MHz 50% duty cycle clock, providing timing for the receive operation on channel #i (i = 0, 1, 2, 3).
RSCO_0 RSCO_1 RSCO_2 RSCO_3	AC31 AC28 AE27 AH27	LVTTL Output 12 mA	**Receive Serial Clock Output TTL**. RSCO_i (i = 0, 1, 2, 3) is a flow-through or divided version of RSCI_i. RcvCOCnf (register R_COCNF) configures the RSCO_i (i = 0, 1, 2, 3) outputs as a 51.84 MHz/25.92 MHz/12.96 MHz/6.48 MHz, or 8-KHz clock.
RLOCK_0 RLOCK_1 RLOCK_2 RLOCK_3	Y27 AE31 AH31 AJ28	LVTTL Input	**Receive Lock Detect TTL**. RLOCK_i (i = 0, 1, 2, 3) is the active-high Lock Detect input for channel #i. RLOCK_i indicates that the external clock recovery PLL used by channel #i is locked. In single 32-bit mode, RLOCK_1, RLOCK_2, and RLOCK_3 are unused inputs. RLOCK_i (i = 0, 1, 2, 3) are asynchronous inputs.
ROOF_0 ROOF_1 ROOF_2 ROOF_3	AA27 AE29 AG29 AJ27	LVTTL Output 12 mA	**Receive Out of Frame TTL**. ROOF_i (i = 0, 1, 2, 3) is high while receive channel #i is “out of frame” and low while it is “in frame”. In single 32-bit mode, ROOF_1, ROOF_2, and ROOF_3 are tristated. ROOF_i is updated on the rising edge of RSCI_i (i = 0, 1, 2, 3).
RFPI_0 RFPI_1 RFPI_2 RFPI_3	AB30 AE30 AD26 AG27	LVTTL Input	**Receive Frame Position Input TTL**. RFPI_i (i = 0, 1, 2, 3) are active-high frame position inputs providing connection to an external SONET/SDH demultiplexer. RFPI_i (i = 0, 1, 2, 3) indicates the SONET/SDH frame position on the RPDI_i[7:0] bus. Select the byte position indicated by RFPI_i (i = 0, 1, 2, 3) by using RcvFPICnf[7:0] (global register R_FPCNF). RFPI_i (i = 0, 1, 2, 3) should be active-high for a single RPCI_i period. Receive channel #i ignores pulses on RFPI_i while “in frame” (ROOF_i = '0'). In single mode RFPI_1, RFPI_2, and RFPI_3 are unused inputs. RFPI_i is sampled on the rising edge of RPCI_i (i = 0, 1, 2, 3). When frame alignment is enabled (bit RcvFBaDsbl = ‘0’ in register R_RSTC), RFPI_i have to be tied to GND.
NOTE: See notes 1, 2, and 3 at the end of the table.			

Table 4. Pin Description (Sheet 17 of 66)

Pin Name	Pin	Type	Description
Transmit 51 Mbit/s TTL Quad Serial Line Side Interface			
TSDO_0 TSDO_1 TSDO_2 TSDO_3	AF6 AE5 AB6 Y6	LVTTL Output 12 mA	**Transmit Serial Data Output TTL** The transmit TTL quad serial line side interface provides connection to serial 51.84 Mbit/s demultiplexers. The quad serial mode can be used when Intel IXF6048 is configured as a Quad STS-1/STM-0 transceiver. TSDO_i (i = 0, 1, 2, 3) carries the outgoing 51 Mbit/s serial data stream for channel #i. TSDO_i (i = 0, 1, 2, 3) is updated on the rising edge of TSCI_i.
TSCI_0 TSCI_1 TSCI_2 TSCI_3	AD6 AG1 AA5 AB1	LVTTL Input	**Transmit Serial Clock Input TTL**. TSCI_i (i = 0, 1, 2, 3) provides timing for transmit channel #i operation. TSCI_i is a 51.84 MHz 50% duty cycle clock, providing timing for the transmit operation on channel #i (i = 0, 1, 2, 3).
TSCO_0 TSCO_1 TSCO_2 TSCO_3	AH3 AF2 AC3 AB2	LVTTL Output 12 mA	**Transmit Serial Clock Output TTL**. TSCO_i (i = 0, 1, 2, 3) is a flowed through or divided version of the clock used by transmit channel #i (RSCI_i or TSCI_i). XmtCOCnf (register R_COCNF) configures the TSCO_i (i = 0, 1, 2, 3) outputs as a 51.84 MHz/25.92 MHz/12.96 MHz/6.48 MHz/8 KHz clock (OC-1). XmtTimRef (register T_COCNF) configures the transmitter in two different modes: • Clocked by the transmit serial clock input TSCI_i (XmtTimRef = '10') • Clocked by the receive serial clock input RSCI_i (XmtTimRef = '01') **NOTE:** In the line loopback mode of operation, the TSCO_i clocks are derived from the RSCI_i clock input, because the transmitter's internal clock source is automatically switched to the RSCI_i clock input in that case.
NOTE: See notes 1, 2, and 3 at the end of the table.			

Table 4. Pin Description (Sheet 18 of 66)

Pin Name	Pin	Type	Description
OH, Alarm, DCC and Orderwire Insertion/Extraction Ports Single PHY Mode (OH Ports Logical Interface #1) (Single OC-48c, OC-48, OC-12, and OC-3 Modes)			
RSOH_0 RSOH_1 RSOH_2 RSOH_3	H29 K26 J28 G31	LVTTL Output 4 mA	**Receive SOH Extraction Bus**. RSOH_i (i = 0, 1, 2, 3) outputs the SOH bytes extracted from the Incoming SONET/SDH frames. • In OC-48c, OC-48, and OC-12 modes, RSOH_i (i = 0, 1, 2, 3) extracts the SOH bytes received in columns #i + 1, #i + 5, #i + 9, etc. • In OC-3 mode, RSOH_i (i = 0, 1, 2, 3) extracts the SOH bytes received in columns #i + 1, #i + 4, #i + 7, etc. RSOH_3 is held in high impedance. RSOH_i (i = 0, 1, 2, 3) is clocked out by RSOHCK.
RSOHFR	J29	LVTTL Output 4 mA	**Receive SOH Frame Pulse**. RSOHFR is an 8-KHz pulse indicating the start of the SOH (A1 MSB position) on RSOH_i (i = 0, 1, 2, 3). RSOHFR is clocked out by RSOHCK.
RSOHCK	K28	LVTTL Output 4 mA	**Receive SOH Extraction Clock**. RSOHCK is a 20.736 MHz (OC-48c/ OC-48), 5.184 MHz (OC-12), or 1.728 MHz (OC-3) timing reference signal used to clock out the RSOH_i (i = 0, 1, 2, 3) data.
RSAL	E28	LVTTL Output 4 mA	**Receive Section Alarm Bus**. RSAL outputs the receive side section alarms, detected section errors, generated remote defects, receive filtered K1 and K2 APS bytes, and the filtered S1 SSM. RSAL is clocked out by RSALCK.
RSALFR	E30	LVTTL Output 4 mA	**Receive Section Alarm Pulse**. RSALFR is an 8-KHz pulse indicating the position of the generated RDI bit at RSAL. The RSALFR pulse repeats every 72 clock cycles of RMDC. RSALFR is clocked out by RSALCK.
RSALCK	H27	LVTTL Output 4 mA	**Receive Section Alarm Clock**. RSALCK is a 576-KHz timing reference signal used to clock out the RSAL and RSALFR outputs.
TSOH_0 TSOH_1 TSOH_2 TSOH_3	W3 Y2 V5 Y1	LVTTL Input	**Transmit SOH Insertion Bus**. TSOH_i (i = 0, 1, 2, 3) inputs the SOH bytes to be inserted in the outgoing SONET/SDH frames. • In OC-48c, OC-48 and OC-12 modes, TSOH_i (i = 0, 1, 2, 3) inserts the SOH bytes to be transmitted in columns #i + 1, #i + 5, #i + 9, etc. • In OC-3 mode, TSOH_i (i = 0, 1, 2) inserts the SOH bytes to be transmitted in columns #i + 1, #i + 4, #i + 7, etc. TSOH_3 is an unused input. TSOH_i (i = 0, 1, 2, 3) is clocked in by TSOHCK.
TSOHINS_0 TSOHINS_1 TSOHINS_2 TSOHINS_3	W2 U6 V4 W1	LVTTL Input	**Transmit SOH Insertion Enable**. TSOHINS_i (i = 0, 1, 2, 3) is the active-high SOH insertion enable. TSOHINS_i (i = 0, 1, 2, 3) controls the insertion of the bytes transported on TSOH_i in the outgoing SONET/ SDH frames. The byte transported in TSOH_i (i = 0, 1, 2, 3) is inserted in the outgoing frame if TSOHINS_i is asserted during its most significant bit. TSOHINS_i (i = 0, 1, 2, 3) control pin may be disabled via microprocessor configuration register T_SC_RSOH[15] (TSOHINS_Ena = '0' in register address (1cc)E1H). TSOHINS_i (i = 0, 1, 2, 3) is clocked in by TSOHCK.
TSOHFR	Y3	LVTTL Output 4 mA	**Transmit SOH Frame Pulse**. TSOHFR is an 8-KHz pulse indicating the start of the SOH (A1 MSB position) on TSOH_i (i = 0, 1, 2, 3). TSOHFR is clocked out by RSOHCK.
NOTE: See notes 1, 2, and 3 at the end of the table.			

Table 4. Pin Description (Sheet 19 of 66)

Pin Name	Pin	Type	Description
TSOHCK	AA3	LVTTL Output 4 mA	**Transmit SOH Insertion Clock**. TSOHCK is a 20.736 MHz (OC-48c/ OC-48), 5.184 MHz (OC-12), or 1.728 MHz (OC-3) timing reference signal used to clock in the TSOH_i (i = 0, 1, 2, 3) data.
TSAL	R3	LVTTL Input	**Transmit Section Alarm Bus**. TSAL allows the insertion of the remote defect indication (MS-RDI and MS-REI) and/or the insertion of the APS bytes K1 and K2 into the transmit SOH. TSAL is clocked in by TSALCK.
TSALFR	T4	LVTTL Bidir 4 mA	**Transmit Section Alarm Pulse**. TSALFR is an 8-KHz pulse indicating the expected position of RDI at the TSAL input. The TSALFR pulse is repeated every 72 clock cycles of TMDC. TsalBusCnfg (register T_SC_MSOH) configures the transmit section alarm bus as a codirectional or a contradirectional interface: • When TsalBusCnfg = '0', TSALFR is configured as an output pin. • When TsalBusCnfg = '1', TSALFR is configured as an input pin. TSALFR is clocked out by TSALCK.
TSALCK	V3	LVTTL Bidir 4 mA	**Transmit Section Alarm Clock**. TSALCK is a 576-KHz timing reference signal used to clock in the TSAL input. TsalBusCnfg (register T_SC_MSOH) configures the transmit section alarm bus as a codirectional or a contradirectional interface: • When TsalBusCnfg = '0', TSALCK is configured as an output pin. • When TsalBusCnfg = '1', TSALCK is configured as an input pin.
RPOH_0 RPOH_1 RPOH_2 RPOH_3	E26 A29 B28 D27	LVTTL Output 4 mA	**Receive POH Extraction Bus**. RPOH_i (i = 0, 1, 2, 3) outputs the POH bytes extracted from the incoming SONET/SDH frames. • In OC-48c mode, RPOH_0 extracts the POH of the VC-4-16c processed by channel #0. RPOH_1, RPOH_2, and RPOH_3 are held in high impedance. • In OC-48/OC-12 mode, RPOH_i (i = 0, 1, 2, 3) extracts the POH bytes of the VC-4-4c/VC-4 processed by channel #i. • In OC-3 mode, RPOH_i (i = 0, 1, 2, 3) extracts the POH bytes of the VC-3 processed by channel #i. RPOH_3 is held in high impedance. RPOH_i (i = 0, 1, 2, 3) is clocked out by RPOHCK_i.
RPOHFR_0 RPOHFR_1 RPOHFR_2 RPOHFR_3	F26 E27 C28 C29	LVTTL Output 4 mA	**Receive POH Frame Pulse**. RPOHFR_i (i = 0, 1, 2, 3) is an 8-KHz pulse indicating the start of the POH (J1 MSB position) on RPOH_i. RPOHFR_i (i = 0, 1, 2, 3) is clocked out by RPOHCK_i.
RPOHCK_0 RPOHCK_1 RPOHCK_2 RPOHCK_3	C30 C31 D28 D29	LVTTL Output 4 mA	**Receive POH Extraction Clock**. RPOHCK_i (i = 0, 1, 2, 3) is a 576-KHz timing reference signal used to clock out the RPOH_i data. In OC-48c mode, RPOHCK_1, RPOHCK_2, and RPOHCK_3 are held in high impedance. In OC-3 mode, RPOHCK_3 is held in high impedance.
RPAL_0 RPAL_1 RPAL_2 RPAL_3	D26 A28 C27 F24	LVTTL Output 4 mA	**Receive Path Alarm Bus**. RPAL_i (i = 0, 1, 2, 3) outputs the receive side path alarms, detected path errors, the filtered receive signal label, and the generated remote defects on channel #i. The position of the generated “server defect” bit at the RPAL_i output (i = 0, 1, 2, 3) is indicated by the 8-KHz pulse RPOHFR_i. RPAL_i (i = 0, 1, 2, 3) is clocked out by RPOHCK_i.
NOTE: See notes 1, 2, and 3 at the end of the table.			

Table 4. Pin Description (Sheet 20 of 66)

Pin Name	Pin	Type	Description
TPOH_0 TPOH_1 TPOH_2 TPOH_3	N3 N5 M1 L1	LVTTL Input	**Transmit POH Insertion Bus**. TPOH_i (i = 0, 1, 2, 3) inputs the POH bytes to be inserted in the outgoing SONET/SDH frames. • In OC-48c mode, TPOH_0 inserts the POH bytes of the VC-4-16c processed by channel #0. TPOH_1, TPOH_2, and TPOH_3 are unused inputs. • In OC-48/OC-12 mode, TPOH_i (i = 0, 1, 2, 3) inserts the POH bytes of the VC-4-4c/VC-4 processed by channel #i. • In OC-3 mode, TPOH_i (i = 0, 1, 2, 3) inserts the POH bytes of the VC-3 processed by channel #i. TPOH_3 is held in high impedance. When the transmit path alarm bus is configured in codirectional mode (TpalBusCnfg = '1', register T_HPT_OPC), TPOH_i and TPOHINS_i (i = 0, 1, 2, 3) are unused inputs TPOH_i (i = 0, 1, 2, 3) is clocked in by TPOHCK_i.
TPOHINS_0 TPOHINS_1 TPOHINS_2 TPOHINS_3	M3 M4 N6 K1	LVTTL Input	**Transmit POH Insertion Enable**. TPOHINS_i (i = 0, 1, 2, 3) is the active-high POH insertion enable, controlling the insertion of the bytes transported on TPOH_i in the SONET/SDH frames generated by channel #i. The byte transported in TPOH_i (i = 0, 1, 2, 3) is inserted in the outgoing frame if TPOHINS_i is asserted during its most significant bit. TPOHINS_i (i = 0, 1, 2, 3) control pin may be disabled via microprocessor configuration register T_HPT_C[15] (TPOHINS_Ena = ‘0’ in register address (1cc)E8H). When the transmit path alarm bus is configured in codirectional mode (TpalBusCnfg = '1', register T_HPT_OPC), TPOH_i and TPOHINS_i (i = 0, 1, 2, 3) are unused inputs TPOHINS_i (i = 0, 1, 2, 3) is clocked in by TPOHCK_i.
TPOHFR_0 TPOHFR_1 TPOHFR_2 TPOHFR_3	N1 P5 P6 N2	LVTTL Bidir 4 mA	**Transmit POH Insertion Frame Pulse**. TPOHFR_i (i = 0, 1, 2, 3) is an 8-KHz pulse indicating the start of the frames transported on the TPOH_i and TPAL_i inputs. TpalBusCnfg (register T_HPT_OPC) configures the transmit path alarm bus as a codirectional or a contradirectional interface: • When TpalBusCnfg = '0', TPOHFR_i (i = 0, 1, 2, 3) is configured as an output pin. • When TpalBusCnfg = '1', TPOHFR_i (i = 0, 1, 2, 3) is configured as an input pin. TPOHFR_i (i = 0, 1, 2, 3) is clocked by TPOHCK_i.
TPOHCK_0 TPOHCK_1 TPOHCK_2 TPOHCK_3	P1 P2 P3 P4	LVTTL Bidir 4 mA	**Transmit POH Insertion Clock**. TPOHCK_i (i = 0, 1, 2, 3) is a 576-KHz timing reference signal used to clock in the TPOH_i and TPAL_i data on channel #i. TpalBusCnfg (register T_HPT_OPC) configures the transmit path alarm bus as a codirectional or a contradirectional interface: • When TpalBusCnfg = '0', TPOHCK_i (i = 0, 1, 2, 3) is configured as an output pin. • When TpalBusCnfg = '1', TPOHCK_i (i = 0, 1, 2, 3) is configured as an input pin.
TPAL_0 TPAL_1 TPAL_2 TPAL_3	L2 M5 L3 J1	LVTTL Input	**Transmit Path Alarm Bus**. TPAL_i (i = 0, 1, 2, 3) allows the insertion of the remote path defect information (HP-RDI and HP-REI) on channel #i. The expected position of the “server defect” bit at the TPAL_i input (i = 0, 1, 2, 3) is indicated by the 8-KHz pulse TPOHFR_i. TpalBusCnfg (register T_HPT_OPC) configures the transmit path alarm bus as a codirectional or a contradirectional interface. TPAL_i (i = 0, 1, 2, 3) is clocked in by TPOHCK_i.
NOTE: See notes 1, 2, and 3 at the end of the table.			

Table 4. Pin Description (Sheet 21 of 66)

Pin Name	Pin	Type	Description
RRD	H30	LVTTL Output 4 mA	**Receive RSOH D1-D3 Data**. RRD is a 192-Kbit/s data output for the received RSOH D1-D3 data. RRD is clocked out by RRDC.
RRDC	L26	LVTTL Output 4 mA	**Receive RSOH D1-D3 Data Clock**. RRDC is a 192-KHz reference signal used to clock out the RRD data.
RMD	F27	LVTTL Output 4 mA	**Receive MSOH D4-D12 Data**. RMD is a 576-Kbit/s data output for the received RSOH D4-D12 data. RMD is clocked out by RMDC.
RMDC	H26	LVTTL Output 4 mA	**Receive MSOH D4-D12 Data Clock**. RMDC is a 576-KHz reference signal used to clock out the RMD data.
TRD	U2	LVTTL Input	**Transmit RSOH D1-D3 Data**. TRD is a 192-Kbit/s data input for the transmit RSOH D1-D3 data. TRD is clocked in by TRDC.
TRDC	Y4	LVTTL Output 4 mA	**Transmit RSOH D1-D3 Data Clock**. TRDC is a 192-KHz reference signal used to clock in the TRD data.
TMD	R4	LVTTL Input	**Transmit MSOH D4-D12 Data**. TMD is a 576-Kbit/s data input for the transmit RSOH D4-D12 data. TMD is clocked in by TMDC.
TMDC	V6	LVTTL Output 4 mA	**Transmit MSOH D1-D3 Data Clock**. TMDC is a 576-KHz reference signal used to clock in the TMD data.
RROW	G27	LVTTL Output 4 mA	**Receive RSOH E1 Orderwire**. RROW is a 64-Kbit/s output for the received orderwire byte E1. RROW is synchronized with ROWBYC and clocked out by ROWC.
RMOW	E31	LVTTL Output 4 mA	**Receive MSOH E2 Orderwire**. RMOW is a 64-Kbit/s output for the received orderwire byte E2. RMOW is synchronized with ROWBYC and clocked out by ROWC.
RDOW	J26	LVTTL Output 4 mA	**Receive MSOH F1 Orderwire**. RDOW is a 64-Kbit/s output for the received orderwire byte F1. RDOW is synchronized with ROWBYC and clocked out by ROWC.
ROWBYC	H31	LVTTL Output 4 mA	**Receive RSOH and MSOH Orderwire Synchronization**. ROWBYC is an 8-KHz reference signal used to byte-synchronize the received E1, E2, and F1 bytes (RROW, RMOW, and RDOW outputs).
ROWC	J30	LVTTL Output 4 mA	**Receive RSOH and MSOH Orderwire Clock**. ROWC is a 64-KHz reference signal used to clock out RROW, RMOW, and RDOW.
TROW	R6	LVTTL Input	**Transmit RSOH E1 Orderwire**. TROW is a 64-Kbit/s input for the transmitted orderwire byte E1. TROW is synchronized with TOWBYC and clocked in by TOWC.
TMOW	U1	LVTTL Input	**Transmit MSOH E2 Orderwire**. TMOW is a 64-Kbit/s input for the transmitted orderwire byte E2. TMOW is synchronized with TOWBYC and clocked in by TOWC.
NOTE: See notes 1, 2, and 3 at the end of the table.			

Table 4. Pin Description (Sheet 22 of 66)

Pin Name	Pin	Type	Description
TDOW	T6	LVTTL Input	**Transmit MSOH F1 Orderwire**. TDOW is a 64-Kbit/s input for the transmitted orderwire byte F1. TDOW is synchronized with TOWBYC and clocked in by TOWC.
TOWBYC	W4	LVTTL Output 4 mA	**Transmit RSOH and MSOH Orderwire Synchronization**. TOWBYC is an 8-KHz reference signal used to byte-synchronize E1, E2, and F1 (TROW, TMOW, and TDOW inputs).
TOWC	W5	LVTTL Output 4 mA	**Transmit RSOH and MSOH Orderwire Clock**. TOWC is a 64-KHz reference signal used to clock in TROW, TMOW, and TDOW.
RPOW1	E29	LVTTL Output 4 mA	**Receive POH F2 Orderwire**. RPOW1 is a 64-Kbit/s output for the received orderwire byte F2. Data is synchronized with RPOWBYC and clocked out by RPOWC.
RPOW2	F28	LVTTL Output 4 mA	**Receive POH F3 Orderwire**. RPOW2 is a 64-Kbit/s output for the received orderwire byte F3. Data is synchronized with RPOWBYC and clocked out by RPOWC.
RPOWBYC	K27	LVTTL Output 4 mA	**Receive POH Orderwire Synchronization**. RPOWBYC is an 8-KHz reference signal used to byte-synchronize the received F2 and F3 data streams (RPOW1 and RPOW2 outputs).
RPOWC	J31	LVTTL Output 4 mA	**Receive POH Orderwire Clock**. RPOWC is a 64-KHz reference signal used to clock out RPOW1 and RPOW2.
TPOW1	R5	LVTTL Input	**Transmit POH F2 Orderwire**. TPOW1 is a 64-Kbit/s input for the transmitted orderwire byte F2. TPOW1 is synchronized with TPOWBYC and clocked in by TPOWC.
TPOW2	T3	LVTTL Input	**Transmit POH F3 Orderwire**. TPOW2 is a 64-Kbit/s input for the transmitted orderwire byte F3. TPOW2 is synchronized with TPOWBYC and clocked in by TPOWC.
TPOWBYC	AA1	LVTTL Output 4 mA	**Transmit POH Orderwire Synchronization**. TOWBYC is an 8-KHz reference signal used to byte-synchronize F2 and F3 data streams (TPOW1 and TPOW2 inputs).
TPOWC	AA2	LVTTL Output 4 mA	**Transmit POH Orderwire Clock**. TPOWC is a 64-KHz reference signal used to clock in TPOW1 and TPOW2 and clock out TPOWBYC.
NOTE: See notes 1, 2, and 3 at the end of the table.			

Table 4. Pin Description (Sheet 23 of 66)

Pin Name	Pin	Type	Description
OH and Alarm Insertion/Extraction Ports Quad PHY Mode (OH Ports Logical Interface #2) (Quad OC-12c, OC-3c, and OC-1 Modes)			
RSOH_0 RSOH_1 RSOH_2 RSOH_3	H29 K26 J28 G31	LVTTL Output 4 mA	**Receive SOH Extraction Bus**. RSOH_i (i = 0, 1, 2, 3) outputs the SOH bytes extracted from the incoming SONET/SDH frames on channel #i. RSOH_i (i = 0, 1, 2, 3) is clocked out by RSOHCK_i.
RSOHFR_0 RSOHFR_1 RSOHFR_2 RSOHFR_3	J29 H30 H31 K27	LVTTL Output 4 mA	**Receive SOH Extraction Frame Pulse**. RSOHFR_i (i = 0, 1, 2, 3) is an 8-KHz pulse indicating the start of the SOH (A1 MSB position) on RSOH_i. RSOHFR_i (i = 0, 1, 2, 3) is clocked out by RSOHCK_i.
RSOHCK_0 RSOHCK_1 RSOHCK_2 RSOHCK_3	K28 L26 J30 J31	LVTTL Output 4 mA	**Receive SOH Extraction Clock**. RSOHCK_i (i = 0, 1, 2, 3) is a 20.736 MHz (Quad OC-12c), 5.184 MHz (Quad OC-3c), or 1.728 MHz (Quad OC-1) timing reference signal used to clock out the RSOH_i data on channel #i.
RSAL_0 RSAL_1 RSAL_2 RSAL_3	E28 F27 G27 E29	LVTTL Output 4 mA	**Receive Section Alarm Bus**. RSAL_i (i = 0, 1, 2, 3) outputs the receive side section alarms, detected section errors, generated remote defects, receive filtered K1 and K2 APS bytes, and the filtered S1 SSM on channel #i. RSAL_i (i = 0, 1, 2, 3) is clocked out by RSALCK_i.
RSALFR_0 RSALFR_1 RSALFR_2 RSALFR_3	E30 H26 E31 F28	LVTTL Output 4 mA	**Receive Section Alarm Pulse**. RSALFR_i (i = 0, 1, 2, 3) is an 8-KHz pulse indicating the position of the generated RDI bit at RSAL_i. The RSALFR_i pulse (i = 0, 1, 2, 3) is repeated every 72 clock cycles of RSALCK_i. RSALFR_i (i = 0, 1, 2, 3) is clocked out by RSALCK_i.
RSALCK_0 RSALCK_1 RSALCK_2 RSALCK_3	H27 F29 J26 G28	LVTTL Output 4 mA	**Receive Section Alarm Clock**. RSALCK_i (i = 0, 1, 2, 3) is a 576-KHz timing reference signal used to clock out the RSAL_i and RSALFR_i outputs on channel #i.
TSOH_0 TSOH_1 TSOH_2 TSOH_3	W3 Y2 V5 Y1	LVTTL Input	**Transmit SOH Insertion Bus**. TSOH_i (i = 0, 1, 2, 3) inputs the SOH bytes to be inserted in the outgoing SONET/SDH frames on channel #i. TSOH_i (i = 0, 1, 2, 3) is clocked in by TSOHCK.
TSOHINS_0 TSOHINS_1 TSOHINS_2 TSOHINS_3	W2 U6 V4 W1	LVTTL Input	**Transmit SOH Insertion Enable**. TSOHINS_i (i = 0, 1, 2, 3) is the active-high SOH insertion enable. TSOHINS_i (i = 0, 1, 2, 3) controls the insertion of the bytes transported on TSOH_i in the SONET/SDH frames generated by channel #i. The byte transported in TSOH_i (i = 0, 1, 2, 3) is inserted in the outgoing frame if TSOHINS_i is asserted during its most significant bit. TSOHINS_i (i = 0, 1, 2, 3) control pin may be disabled via microprocessor configuration register T_SC_RSOH[15] (TSOHINS_Ena = '0' in register address (1cc)E1H). TSOHINS_i (i = 0, 1, 2, 3) is clocked in by TSOHCK_i.
TSOHFR_0 TSOHFR_1 TSOHFR_2 TSOHFR_3	Y3 V6 W4 AA1	LVTTL Output 4 mA	**Transmit SOH Insertion Frame Pulse**. TSOHFR_i (i = 0, 1, 2, 3) is an 8-KHz pulse indicating the start of the SOH (A1 MSB position) on TSOH_i. TSOHFR_i (i = 0, 1, 2, 3) is clocked out by TSOHCK_i.
NOTE: See notes 1, 2, and 3 at the end of the table.			

Table 4. Pin Description (Sheet 24 of 66)

Pin Name	Pin	Type	Description
TSOHCK_0 TSOHCK_1 TSOHCK_2 TSOHCK_3	AA3 Y4 W5 AA2	LVTTL Output 4 mA	**Transmit SOH Insertion Clock**. TSOHCK_i (i = 0, 1, 2, 3) is a 20.736 MHz (Quad OC-12c), 5.184 MHz (Quad OC-3c), or 1.728 MHz (Quad OC-1) timing reference signal used to clock in the TSOH_i data on channel #i.
TSAL_0 TSAL_1 TSAL_2 TSAL_3	R3 R4 R6 R5	LVTTL Input	**Transmit Section Alarm Bus**. TSAL_i (i = 0, 1, 2, 3) allows the insertion of the remote defect indication (MS-RDI and MS-REI) and/or the insertion of the APS bytes K1 and K2 into the transmit SOH on channel #i. TSAL_i (i = 0, 1, 2, 3) is clocked in by TSALCK_i.
TSALFR_0 TSALFR_1 TSALFR_2 TSALFR_3	T4 U2 U1 T3	LVTTL Bidir 4 mA	**Transmit Section Alarm Pulse**. TSALFR_i (i = 0, 1, 2, 3) is an 8-KHz pulse indicating the expected position of RDI at the TSAL_i input on channel #i. The TSALFR_i pulse (i = 0, 1, 2, 3) is repeated every 72 clock cycles of TSALCK_i. TsalBusCnfg (register T_SC_MSOH) configures the transmit section alarm bus as a codirectional or a contradirectional interface: • When TsalBusCnfg = '0', TSALFR_i (i = 0, 1, 2, 3) is configured as an output pin. • When TsalBusCnfg = '1', TSALFR_i (i = 0, 1, 2, 3) is configured as an input pin. TSALFR_i (i = 0, 1, 2, 3) is clocked out by TSALCK_i.
TSALCK_0 TSALCK_1 TSALCK_2 TSALCK_3	V3 U3 T6 T5	LVTTL Bidir 4 mA	**Transmit Section Alarm Clock**. TSALCK_i (i = 0, 1, 2, 3) is a 576-KHz timing reference signal used to clock in the TSAL_i input on channel #i. TsalBusCnfg (register T_SC_MSOH) configures the transmit section alarm bus as a codirectional or a contradirectional interface: • When TsalBusCnfg = '0', TSALCK_i (i = 0, 1, 2, 3) is configured as an output pin. • When TsalBusCnfg = '1', TSALCK_i (i = 0, 1, 2, 3) is configured as an input pin.
RPOH_0 RPOH_1 RPOH_2 RPOH_3	E26 A29 B28 D27	LVTTL Output 4 mA	**Receive POH Extraction Bus**. RPOH_i (i = 0, 1, 2, 3) outputs the POH bytes extracted from the incoming SONET/SDH frames on channel #i. RPOH_i (i = 0, 1, 2, 3) is clocked out by RPOHCK_i.
RPOHFR_0 RPOHFR_1 RPOHFR_2 RPOHFR_3	F26 E27 C28 C29	LVTTL Output 4 mA	**Receive POH Extraction Frame Pulse**. RPOHFR_i (i = 0, 1, 2, 3) is an 8-KHz pulse indicating the start of the POH (J1 MSB position) on RPOH_i. RPOHFR_i (i = 0, 1, 2, 3) is clocked out by RPOHCK_i.
RPOHCK_0 RPOHCK_1 RPOHCK_2 RPOHCK_3	C30 C31 D28 D29	LVTTL Output 4 mA	**Receive POH Extraction Clock**. RPOHCK_i (i = 0, 1, 2, 3) is a 576-KHz timing reference signal used to clock out the RPOH_i data on channel #i.
RPAL_0 RPAL_1 RPAL_2 RPAL_3	D26 A28 C27 F24	LVTTL Output 4 mA	**Receive Path Alarm Bus**. RPAL_i (i = 0, 1, 2, 3) outputs the receive side path alarms, detected path errors, the filtered receive signal label, and the generated remote defects on channel #i. The position of the generated “server defect” bit at the RPAL_i output (i = 0, 1, 2, 3) is indicated by the 8-KHz pulse RPOHFR_i. RPAL_i (i = 0, 1, 2, 3) is clocked out by RPOHCK_i.
NOTE: See notes 1, 2, and 3 at the end of the table.			

Table 4. Pin Description (Sheet 25 of 66)

Pin Name	Pin	Type	Description
TPOH_0 TPOH_1 TPOH_2 TPOH_3	N3 N5 M1 L1	LVTTL Input	**Transmit POH Insertion Bus**. TPOH_i (i = 0, 1, 2, 3) inputs the POH bytes to be inserted in the outgoing SONET/SDH frames on channel #i. When the transmit path alarm bus is configured in codirectional mode (TpalBusCnfg = '1', register T_HPT_OPC) TPOH_i and TPOHINS_i (i = 0, 1, 2, 3) are unused inputs. TPOH_i (i = 0, 1, 2, 3) is clocked in by TPOHCK_i.
TPOHINS_0 TPOHINS_1 TPOHINS_2 TPOHINS_3	M3 M4 N6 K1	LVTTL Input	**Transmit POH Insertion Enable**. TPOHINS_i (i = 0, 1, 2, 3) is the active-high POH insertion enable, controlling the insertion of the bytes transported on TPOH_i in the SONET/SDH frames generated by channel #i. The byte transported in TPOH_i (i = 0, 1, 2, 3) is inserted in the outgoing frame if TPOHINS_i is asserted during its most significant bit. TPOHINS_i (i = 0, 1, 2, 3) control pin may be disabled via microprocessor configuration register T_HPT_C[15] (TPOHINS_Ena = '0' in register address (1cc)E8H). When the transmit path alarm bus is configured in codirectional mode (TpalBusCnfg = '1', register T_HPT_OPC), TPOH_i and TPOHINS_i (i = 0, 1, 2, 3) are unused inputs. TPOHINS_i (i = 0, 1, 2, 3) is clocked in by TPOHCK_i.
TPOHFR_0 TPOHFR_1 TPOHFR_2 TPOHFR_3	N1 P5 P6 N2	LVTTL Bidir 4 mA	**Transmit POH Insertion Frame Pulse**. TPOHFR_i (i = 0, 1, 2, 3) is an 8-KHz pulse indicating the start of the frames transported on the TPOH_i and TPAL_i inputs. TpalBusCnfg (register T_HPT_OPC) configures the transmit path alarm bus as a codirectional or a contradirectional interface: • When TpalBusCnfg = '0', TPOHFR_i (i = 0, 1, 2, 3) is configured as an output pin. • When TpalBusCnfg = '1', TPOHFR_i (i = 0, 1, 2, 3) is configured as an input pin. TPOHFR_i (i = 0, 1, 2, 3) is clocked out by TPOHCK_i.
TPOHCK_0 TPOHCK_1 TPOHCK_2 TPOHCK_3	P1 P2 P3 P4	LVTTL Bidir 4 mA	**Transmit POH Insertion Clock**. TPOHCK_i (i = 0, 1, 2, 3) is a 576-KHz timing reference signal used to clock in the TPOH_i and TPAL_i data on channel #i. TpalBusCnfg (register T_HPT_OPC) configures the transmit path alarm bus as a codirectional or a contradirectional interface: • When TpalBusCnfg = '0', TPOHCK_i (i = 0, 1, 2, 3) is configured as an output pin. • When TpalBusCnfg = '1', TPOHCK_i (i = 0, 1, 2, 3) is configured as an input pin.
TPAL_0 TPAL_1 TPAL_2 TPAL_3	L2 M5 L3 J1	LVTTL Input	**Transmit Path Alarm Bus**. TPAL_i (i = 0, 1, 2, 3) allows the insertion of the remote path defect information (HP-RDI and HP-REI) on channel #i. The expected position of the "server defect" bit at the TPAL_i input (i = 0, 1, 2, 3) is indicated by the 8-KHz pulse TPOHFR_i. TpalBusCnfg (register T_HPT_OPC) configures the transmit path alarm bus as a codirectional or a contradirectional interface. TPAL_i (i = 0, 1, 2, 3) is clocked in by TPOHCK_i.
NOTE: See notes 1, 2, and 3 at the end of the table.			

Table 4. Pin Description (Sheet 26 of 66)

Pin Name	Pin	Type	Description
DCC and Orderwire Insertion/Extraction Ports Quad PHY Mode (OH Ports Logical Interface #3) (Quad OC-12c, OC-3c, and OC-1 modes)			
RRD_0 RRD_1 RRD_2 RRD_3	H29 K26 J28 G31	LVTTL Output 4 mA	**Receive RSOH D1-D3 Data**. RRD_i (i = 0, 1, 2, 3) is a 192-Kbit/s data output for the received RSOH D1-D3 data on channel #i. RRD_i (i = 0, 1, 2, 3) is clocked out by RRDC_i.
RRDC_0 RRDC_1 RRDC_2 RRDC_3	K28 L26 J30 J31	LVTTL Output 4 mA	**Receive RSOH D1-D3 Data Clock**. RRDC_i (i = 0, 1, 2, 3) is a 192-KHz reference signal used to clock out the RRD_i data.
RMD_0 RMD_1 RMD_2 RMD_3	J29 H30 H31 K27	LVTTL Output 4 mA	**Receive MSOH D4-D12 Data**. RMD_i (i = 0, 1, 2, 3) is a 576-Kbit/s data output for the received RSOH D4-D12 data on channel #i. RMD_i (i = 0, 1, 2, 3) is clocked out by RMDC_i.
RMDC_0 RMDC_1 RMDC_2 RMDC_3	E28 F27 G27 E29	LVTTL Output 4 mA	**Receive MSOH D4-D12 Data Clock**. RMDC_i (i = 0, 1, 2, 3) is a 576-KHz reference signal used to clock out the RMD_i data.
TRD_0 TRD_1 TRD_2 TRD_3	W2 U6 V4 W1	LVTTL Input	**Transmit RSOH D1-D3 Data**. TRD_i (i = 0, 1, 2, 3) is a 192-Kbit/s data input for the transmit RSOH D1-D3 data on channel #i. TRD_i (i = 0, 1, 2, 3) is clocked in by TRDC_i.
TRDC_0 TRDC_1 TRDC_2 TRDC_3	Y3 V6 W4 AA1	LVTTL Output 4 mA	**Transmit RSOH D1-D3 Data Clock**. TRDC_i (i = 0, 1, 2, 3) is a 192-KHz reference signal used to clock in the TRD_i data.
TMD_0 TMD_1 TMD_2 TMD_3	W3 Y2 V5 Y1	LVTTL Input	**Transmit MSOH D4-D12 Data**. TMD_i (i = 0, 1, 2, 3) is a 576-Kbit/s data input for the transmit RSOH D4-D12 data on channel #i. TMD_i (i = 0, 1, 2, 3) is clocked in by TMDC_i.
TMDC_0 TMDC_1 TMDC_2 TMDC_3	AA3 Y4 W5 AA2	LVTTL Output 4 mA	**Transmit MSOH D4-D12 Data Clock**. TMDC_i (i = 0, 1, 2, 3) is a 576-KHz reference signal used to clock in the TMD_i data.
RROW_0 RROW_1 RROW_2 RROW_3	E30 H26 E31 F28	LVTTL Output 4 mA	**Receive RSOH E1 Orderwire**. RROW_i (i = 0, 1, 2, 3) is a 64-Kbit/s output for the received orderwire byte E1 on channel #i. RROW_i (i = 0, 1, 2, 3) is synchronized with ROWBYC_i and clocked out by ROWC_i.
RMOW_0 RMOW_1 RMOW_2 RMOW_3	H27 F29 J26 G28	LVTTL Output 4 mA	**Receive MSOH E2 Orderwire**. RMOW_i (i = 0, 1, 2, 3) is a 64-Kbit/s output for the received orderwire byte E2 on channel #i. RMOW_i (i = 0, 1, 2, 3) is synchronized with ROWBYC_i and clocked out by ROWC_i.
NOTE: See notes 1, 2, and 3 at the end of the table.			

Table 4. Pin Description (Sheet 27 of 66)

Pin Name	Pin	Type	Description
RDOW_0 RDOW_1 RDOW_2 RDOW_3	E26 A29 B28 D27	LVTTL Output 4 mA	**Receive MSOH F1 Orderwire**. RDOW_i (i = 0, 1, 2, 3) is a 64-Kbit/s output for the received orderwire byte F1 on channel #i. RDOW_i (i = 0, 1, 2, 3) is synchronized with ROWBYC_i and clocked out by ROWC_i.
ROWBYC_0 ROWBYC_1 ROWBYC_2 ROWBYC_3	F26 E27 C28 C29	LVTTL Output 4 mA	**Receive RSOH and MSOH Orderwire Synchronization**. ROWBYC_i (i = 0, 1, 2, 3) is an 8-KHz reference signal used to byte-synchronize the received E1, E2, and F1 bytes on channel #i (RROW_i, RMOW_i, and RDOW_i outputs).
ROWC_0 ROWC_1 ROWC_2 ROWC_3	C30 C31 D28 D29	LVTTL Output 4 mA	**Receive RSOH and MSOH Orderwire Clock**. ROWC_i (i = 0, 1, 2, 3) is a 64 KHz reference signal used to clock out RROW_i, RMOW_i, RDOW_i, and ROWBYC_i.
TROW_0 TROW_1 TROW_2 TROW_3	R3 R4 R6 R5	LVTTL Input	**Transmit RSOH E1 Orderwire**. TROW_i (i = 0, 1, 2, 3) is a 64-Kbit/s input for the transmitted orderwire byte E1 on channel #i. TROW_i (i = 0, 1, 2, 3) is synchronized with TOWBYC_i and clocked in by TOWC_i.
TMOW_0 TMOW_1 TMOW_2 TMOW_3	P1 P2 P3 P4	LVTTL Input	**Transmit MSOH E2 Orderwire**. TMOW_i (i = 0, 1, 2, 3) is a 64-Kbit/s input for the transmitted orderwire byte E2 on channel #i. TMOW_i (i = 0, 1, 2, 3) is synchronized with TOWBYC_i and clocked in by TOWC_i.
TDOW_0 TDOW_1 TDOW_2 TDOW_3	L2 M5 L3 J1	LVTTL Input	**Transmit MSOH F1 Orderwire**. TDOW_i (i = 0, 1, 2, 3) is a 64-Kbit/s input for the transmitted orderwire byte F1 on channel #i. TDOW_i (i = 0, 1, 2, 3) is synchronized with TOWBYC_i and clocked in by TOWC_i.
TOWBYC_0 TOWBYC_1 TOWBYC_2 TOWBYC_3	V3 U3 T6 T5	LVTTL Output 4 mA	**Transmit RSOH and MSOH Orderwire Synchronization**. TOWBYC_i (i = 0, 1, 2, 3) is an 8-KHz reference signal used to byte-synchronize E1, E2, and F1 on channel #i (TROW_i, TMOW_i, and TDOW_i inputs).
TOWC_0 TOWC_1 TOWC_2 TOWC_3	N1 P5 P6 N2	LVTTL Output 4 mA	**Transmit RSOH and MSOH Orderwire Clock**. TOWC_i (i = 0, 1, 2, 3) is a 64-KHz reference signal used to clock in TROW_i, TMOW_i, and TDOW_i.
RPOW1	D26	LVTTL Output 4 mA	**Receive POH F2 Orderwire**. RPOW1 is a 64-Kbit/s output for the received orderwire byte F2. Data is synchronized with RPOWBYC and clocked out by RPOWC.
RPOW2	A28	LVTTL Output 4 mA	**Receive POH F3 Orderwire**. RPOW2 is a 64-Kbit/s output for the received orderwire byte F3. Data is synchronized with RPOWBYC and clocked out by RPOWC.
RPOWBYC	C27	LVTTL Output 4 mA	**Receive POH Orderwire Synchronization**. RPOWBYC is an 8-KHz reference signal used to byte-synchronize the received F2 and F3 data streams (RPOW1 and RPOW2 outputs).
RPOWC	F24	LVTTL Output 4 mA	**Receive POH Orderwire Clock**. RPOWC is a 64-KHz reference signal used to clock out RPOW1 and RPOW2.
NOTE: See notes 1, 2, and 3 at the end of the table.			

Table 4. Pin Description (Sheet 28 of 66)

Pin Name	Pin	Type	Description
TPOW1	M3	LVTTL Input	**Transmit POH F2 Orderwire**. TPOW1 is a 64-Kbit/s input for the transmitted orderwire byte F2. TPOW1 is synchronized with TPOWBYC and clocked in by TPOWC.
TPOW2	N3	LVTTL Input	**Transmit POH F3 Orderwire**. TPOW2 is a 64-Kbit/s input for the transmitted orderwire byte F3. TPOW2 is synchronized with TPOWBYC and clocked in by TPOWC.
TPOWBYC	T4	LVTTL Output 4 mA	**Transmit POH Orderwire Synchronization**. TOWBYC is an 8-KHz reference signal used to byte-synchronize F2 and F3 data streams (TPOW1 and TPOW2 inputs).
TPOWC	U2	LVTTL Output 4 mA	**Transmit POH Orderwire Clock**. TPOWC is a 64-KHz reference signal used to clock in TPOW1 and TPOW2 and clock out TPOWBYC.
NOTE: See notes 1, 2, and 3 at the end of the table.			

Table 4. Pin Description (Sheet 29 of 66)

Pin Name	Pin	Type	Description
Receive Single MPHY ATM/POS-UTOPIA Interface (Level 3 and Level 2 Modes)			
RXDATA[0] RXDATA[1] RXDATA[2] RXDATA[3] RXDATA[4] RXDATA[5] RXDATA[6] RXDATA[7] RXDATA[8] RXDATA[9] RXDATA[10] RXDATA[11] RXDATA[12] RXDATA[13] RXDATA[14] RXDATA[15] RXDATA[16] RXDATA[17] RXDATA[18] RXDATA[19] RXDATA[20] RXDATA[21] RXDATA[22] RXDATA[23] RXDATA[24] RXDATA[25] RXDATA[26] RXDATA[27] RXDATA[28] RXDATA[29] RXDATA[30] RXDATA[31]	D13 B13 A12 A14 A13 D14 F14 B14 D16 B18 B17 D17 A18 A19 F16 A20 F20 B23 B24 C22 E21 D21 C23 D22 A27 C25 B26 E23 C26 D25 B27 F23	LVTTL Output 12 mA	**Receive UTOPIA Data Bus** RXDATA[63:0] carries the frame (cell or packet) word that is read from the receive FIFO memories. RXDATA[63:0] transports the cell/packet data in 64-bit, 32-bit, 16-bit, or 8-bit format (RcvUWidth, register R_UICNF). • When configured in 64-bit mode, RXDATA[63:56] transports the most significant byte. • When configured in 32-bit mode, RXDATA[31:24] transports the most significant byte. • When configured in 16-bit mode, RXDATA[31:16] are held in high impedance and RXDATA[15:0] contains valid data. RXDATA[15:8] transports the most significant byte. When configured in 8-bit mode, RXDATA[31:8] are held in high impedance and RXDATA[7:0] contains valid data. RXDATA is driven when the receive interface has been selected for a data transfer **or** RcvMphyDevCnf = '0' (register R_UICNF). RXDATA is tristated when the receive interface has **not** been selected for a data transfer **and** RcvMphyDevCnf = '1' (register R_UICNF). **NOTE:** Depending on the configuration of RcvDRCnf (register R_UICHCNF), a data transfer happens one (UTOPIA Level 2) or two (UTOPIA Level 3) clock cycles after the assertion of RXENB. **NOTE:** To operate in Level 3 mode (Intel IXF6048 does not share the interface with other PHYs) RcvMphyDevCnf must be set to logic zero. **NOTE:** If the receive interface operates in Level 2 or Level 1 modes and Intel IXF6048 does not share the interface with other PHYs, then RcvMphyDevCnf should be set to logic zero. RXDATA[63:0] are updated on the rising edge of RXCLK.
NOTE: See notes 1, 2, and 3 at the end of the table.			

Table 4. Pin Description (Sheet 30 of 66)

Pin Name	Pin	Type	Description
RXDATA[32] RXDATA[33] RXDATA[34] RXDATA[35] RXDATA[36] RXDATA[37] RXDATA[38] RXDATA[39] RXDATA[40] RXDATA[41] RXDATA[42] RXDATA[43] RXDATA[44] RXDATA[45] RXDATA[46] RXDATA[47] RXDATA[48] RXDATA[49] RXDATA[50] RXDATA[51] RXDATA[52] RXDATA[53] RXDATA[54] RXDATA[55] RXDATA[56] RXDATA[57] RXDATA[58] RXDATA[59] RXDATA[60] RXDATA[61] RXDATA[62] RXDATA[63]		LVTTL Output 4 mA	**NOTE:** The 32 most significant bits of the receive UTOPIA data bus (RXDATA[63:32]) can be located in two different sets of pins. See "I/O Pin Equivalence on the Receive TTL Line Side Interface" on page 82 and "TTL I/O Pin Equivalence on the Receive OH/Alarm Extraction Ports" on page 85. When the 64-bit operation mode is selected (RcvUWidth = '11', register R_UICNF), the RXDATA[63:32] bus can be located at one of two different sets of pins: • If U64Mode (register GOCNF) is set to logic zero, then RXDATA[63:32] uses the receive TTL line side interface pins. In this configuration, the device can only use the PECL line side interface. This configuration may be used in OC-48/OC-48c. • If U64Mode (register GOCNF) is set to logic one, then RXDATA[63:32] uses the receive OH/Alarm extraction interface pins. In this configuration, the device uses only section overhead extraction. This configuration may be used in OC-12 and Quad OC-12c modes.
RXCLK	E17	LVTTL Input	**Receive UTOPIA Clock**. This input clock provides timing for the Intel IXF6048 receive system interface. RXCLK must cycle at a 104 MHz, or lower, instantaneous rate.
NOTE: See notes 1, 2, and 3 at the end of the table.			

Table 4. Pin Description (Sheet 31 of 66)

Pin Name	Pin	Type	Description
RXENB	E19	LVTTL Input	**Receive Read Enable**. RXENB is the active-low receive enable and controls read access from the Intel IXF6048 receive interface. RXENB can be used in two different ways: **Normal Mode** (with port selection phase) This is the default configuration (RcvSelMode = '0', register R_UICNF) compatible with the UTOPIA Level 3 and Level 2 specifications. • Port selection phase: when RXENB is deasserted, no read operations are performed and RXADDR[4:0] are sampled into latches to select (or reselect) a port for a data transfer. • Data transfer phase: when RXENB is asserted, the FIFO selected during the port selection phase is read and the data is output in RXDATA, RXPRTY, RXSOF, RXEOF, RXERR, and RXVAL after one or two clock cycles (see RcvDRCnf bit in register R_UICHCNF). **Memory Mapped Device Mode** (with no port selection phase) This configuration (RcvSelMode = '1', register R_UICNF) simplifies the standard UTOPIA interface by eliminating the port selection phase. Port selection is performed on a clock cycle basis: • When RXENB is deasserted, nothing happens. • When RXENB is asserted, the FIFO indicated by RXADDR[4:0] (during the same clock cycle) is read and the data is output in RXDATA, RXPRTY, RXSOF, RXEOF, RXERR, and RXVAL after one or two clock cycles (see RcvDRCnf bit in register R_UICNF). RXENB is sampled on the rising edge of RXCLK.
RXADDR[0] RXADDR[1] RXADDR[2] RXADDR[3] RXADDR[4]	C18 B19 C19 B20 A21	LVTTL Input	**Receive Address Bus**. RXADDR[4:0] are used to perform two different processes: • To select a particular FIFO for a data transfer • To poll the status of a particular FIFO (independently of RXENB) The most significant three bits of the address (RXADDR[4:2]) are compared with the base-address programmed value (UAddrBase[2:0], global register GOCNF) to determine if the device has been selected. The least significant two bits of the address (RXADDR[1:0]) are hard-wired to select a specific channel ('00' = channel 0, '01' = channel 1, '10' = channel 2, '11' = channel 3). The address value 1FH is the null physical address and cannot be assigned to any PHY port. RXADDR[4:0] are sampled on the rising edge of RXCLK.
RXSOF	B11	LVTTL Output 12 mA	**Receive Start-of-Frame**. RXSOF (active-high) marks the first word of a frame (cell or packet) in RXDATA. In reception, all the cells/packets are transferred in RXDATA with the first byte of the frame located in the most significant byte position (see the RXDATA description). RXSOF is driven or tristated following the same rules as RXDATA. RXSOF is updated on the rising edge of RXCLK.
RXEOF	C12	LVTTL Output 12 mA	**Receive End-of-Frame**. RXEOF (active-high) marks the last word of a frame (cell or packet) in RXDATA. RXEOF is used only in POS mode; in ATM mode, this output is held in high impedance (see RcvTestOen in register R_UICNF). RXEOF is driven or tristated following the same rules as RXDATA. RXEOF is updated on the rising edge of RXCLK.
NOTE: See notes 1, 2, and 3 at the end of the table.			

Table 4. Pin Description (Sheet 32 of 66)

Pin Name	Pin	Type	Description
RXPRTY	D12	LVTTL Output 12 mA	**Receive Data Parity**. This output signal indicates the parity of RXDATA. Odd or even parity are selectable (see RcvPrtyCnf in register R_UICHCNF). RXPRTY is driven or tristated following the same rules as RXDATA. RXPRTY is updated on the rising edge of RXCLK.
RXERR	E13	LVTTL Output 12 mA	**Receive Packet Error**. RXERR (active-high) indicates that the received packet contains an error and must be discarded. RXERR is used only in POS mode; in ATM mode, this output is held in high impedance (see RcvTestOen in register UICNF). RXERR is driven or tristated following the same rules as RXDATA. RXERR is only asserted on the last word of a packet (when RXEOF is also asserted). When RXERR is asserted, the packet must be discarded by the Data Link Layer device. RXERR is asserted if any of the following conditions are true: • The packet was aborted by the remote transmitter (the packet was received ending with an Abort sequence). • The packet contains an FCS error and RcvFCSErr (register R_PHCCNF) is set to logic one. • The packet is smaller than the programmable minimum packet length (register R_MINPL) and RcvMinPLDEn (register R_PHCCNF) is set to logic one. • The packet is longer than the programmable maximum packet length (register R_MAXPL) and RcvMaxPLDEn (register R_PHCCNF) is set to logic one. RXERR is updated on the rising edge of RXCLK. When a FIFO overflow occurs, the frame is locally aborted and RXERR is asserted.
NOTE: See notes 1, 2, and 3 at the end of the table.			

Table 4. Pin Description (Sheet 33 of 66)

Pin Name	Pin	Type	Description
RXVAL	F13	LVTTL Output 12 mA	**Receive Valid Data Output**. RXVAL (active-high) validates the receive output signals RXDATA, RXSOF, RXEOF, RXERR, and RXPADL. Note that RXPRTY is valid independently of RXVAL. RXVAL is used only in POS mode; in ATM mode, this output is held in high impedance. RXVAL is driven or tristated following the same rules as RXDATA. Depending on the setting of RcvValCnf (register R_UICNF), RXVAL can be used in two different ways: **RcvValCnf = '0'** RXVAL assertion and deassertion is based only on the status of the receive FIFO. RXVAL is deasserted when attempting to read an empty FIFO (receive FIFO underflow). When the Data Link Layer device tries to read an empty receive FIFO, the read command is disregarded, the receive FIFO is not modified and the Data Link Layer device must ignore the value of the RXDATA, RXSOF, RXEOF, RXERR, and RXPADL. The receive FIFO underflow is not considered an error (no data is lost). **RcvValCnf = '1'** RXVAL is used in the same way as for RcvValCnf = '0' (invalidation of RXDATA, RXSOF, RXEOF, RXERR, and RXPADL, if the FIFO is empty). In addition, RXVAL is also deasserted after reading the last word of a packet, i.e., the next word (start of the next packet) is not read from the FIFO. When RXVAL is deasserted, the conditions FIFO-empty and end-of packet are differentiated using RXEOF. This configuration allows the Link Layer device to be synchronized with the packet boundaries. • If RXVAL has been deasserted due to an interpacket boundary (when RcvValCnf = '1'), the Data Link Layer device is required to deassert RXENB, i.e., the Data Link Layer device **must select a new port or reselect the same port**. • If RXVAL is deasserted because the FIFO is empty (RcvValCnf = '0' or '1'), the Data Link Layer device is not required to deassert RXENB. Once new data is received and written into the same FIFO, the Data Link Layer device can continue reading. RXVAL is updated on the rising edge of RXCLK.
NOTE: See notes 1, 2, and 3 at the end of the table.			

Table 4. Pin Description (Sheet 34 of 66)

Pin Name	Pin	Type	Description
RXPADL[0] RXPADL[1] RXPADL[2]	B10 F12 E12	LVTTL Output 12 mA	**Receive Padding Length**. RXPADL[2:0] indicates the number of padding bytes included in the last word of the packet transferred in RXDATA. RXPADL[2:0] are used only in POS mode; in ATM mode, RXPADL[2:0] are held in high impedance. RXPADL[2:0] are driven or tristated following the same rules as RXDATA. Intel IXF6048 only outputs complete words on RXDATA except in the last word of a packet. RXPADL[2:0] should be used only when RXEOF is asserted (in the last word of a packet). When RXEOF is not asserted, RXPADL[2:0] outputs the value '000' indicating that all the bytes are valid. When configured in 64-bit mode, the last word may contain zero, one, two, three, four, five, six, or seven padding bytes. When configured in 32-bit mode, the last word may contain zero, one, two, or three padding bytes and only RXPADL[1:0] are used. RXPADL[2] is held in high impedance. When configured in 16-bit mode, the last word may contain zero or one padding byte and only RXPADL[0] is used. RXPADL[1] is held in high impedance. When configured in 8-bit mode, RXPADL[2:0] are held in high impedance. **RXPADL[2:0] (64-Bit Mode)** '000' = Packet ends on RXDATA[7:0] (RXDATA = DDDDDDDD) '001' = Packet ends on RXDATA[15:8] (RXDATA = DDDDDDDP) '010' = Packet ends on RXDATA[23:16] (RXDATA = DDDDDDPP) '011' = Packet ends on RXDATA[31:24] (RXDATA = DDDDDPPP) '100' = Packet ends on RXDATA[39:32] (RXDATA = DDDDPPPP) '101' = Packet ends on RXDATA[47:40] (RXDATA = DDDPPPPP) '110' = Packet ends on RXDATA[55:48] (RXDATA = DDPPPPPP) '111' = Packet ends on RXDATA[63:56] (RXDATA = DPPPPPPP) **RXPADL[1:0] (32-Bit Mode)** '00' = Packet ends on RXDATA[7:0] (RXDATA = DDDD) '01' = Packet ends on RXDATA[15:8] (RXDATA = DDDP) '10' = Packet ends on RXDATA[23:16] (RXDATA = DDPP) '11' = Packet ends on RXDATA[31:24] (RXDATA = DPPP) **RXPADL[0] (16-Bit Mode)** '0' = Packet ends on RXDATA[7:0] (RXDATA = ZZDD) '1' = Packet ends on RXDATA[15:8] (RXDATA = ZZDP) **NOTE:** D = valid data byte, P = padding byte, Z = HiZ byte RXPADL[2:0] are updated on the rising edge of RXCLK.
NOTE: See notes 1, 2, and 3 at the end of the table.			

Table 4. Pin Description (Sheet 35 of 66)

Pin Name	Pin	Type	Description
RXPFA	B9	LVTTL Output 12 mA	**Receive Polled Frame-Available Output**. RXPFA (active-high) is a tristatable signal used to indicate that the polled receive FIFO contains data. RXPFA is driven only after one (RcvDRCnf = '0', register R_UICHCNF) or two (RcvDRCnf = '1', register R_UICHCNF) clock cycles with an address in the RXADDR bus matching the programmed base-address value (UAddrBase[2:0], global register GOCNF). **ATM-UTOPIA Mode** RXPFA is used to perform cell-level handshake (polled receive cell-available indication) and is asserted when the polled receive FIFO contains one or more complete ATM cells. When the ATM cell being read in the UTOPIA interface is the last complete cell in the FIFO, RXPFA is deasserted on the next RXCLK rising edge, after the word output in the RXDATA bus contains the payload byte (1, 2, … 48) indicated by RcvCADeassert[5:0] (register R_UICHCNF). Configuring RcvCADeassert[5:0] to an appropriate value ensures that the ATM Layer device can detect that the current ATM cell is the last cell in the FIFO four clock cycles (or more) before reading the last word. **POS-UTOPIA Mode** RXPFA indicates the availability of data in the polled receive FIFO. RXPFA is asserted when the polled FIFO contains an end-of-packet **OR** contains a number of 32-bit words greater than or equal to the “receive programmable watermark” (channel register R_PWM). RXPFA is deasserted when the polled receive FIFO does not contain an end of packet **AND** contains a number of 32-bit words smaller than the “receive programmable watermark” (register R_PWM). RXPFA is updated on the rising edge of RXCLK.
NOTE: See notes 1, 2, and 3 at the end of the table.			

Table 4. Pin Description (Sheet 36 of 66)

Pin Name	Pin	Type	Description
RXFA_0 RXFA_1 RXFA_2 RXFA_3	B12 A17 E20 A26	LVTTL Output 12 mA	**Receive Direct Frame-Available Outputs**. RXFA_i (i = 0, 1, 2, 3) is a tristatable active-high signal used to indicate the status of receive FIFO #i. RcvDirStatCnf (global register R_UICNF) uses the RXFA_i outputs in two different ways: • When RcvDirStatCnf = '1' (direct status indication mode), the RXFA_i (i = 0, 1, 2, 3) outputs are always driven. • When RcvDirStatCnf = '0' (multiplexed status polling), the RXFA_i (i = 0, 1, 2, 3) outputs are driven (all four at the same time) only after one (RcvDRCnf = '0', register R_UICNF) or two (RcvDRCnf = '1', register R_UICNF) clock cycles, with an address in the RXADDR bus matching the programmed base-address value (UAddrBase[2:0], global register GOCNF). **ATM-UTOPIA Mode** RXFA_i (i = 0, 1, 2, 3) is used to perform cell-level handshake on receive FIFO #i and goes high when the receive FIFO #i contains one or more complete ATM cells. When the ATM cell being read in the UTOPIA interface is the last complete cell in FIFO #i, RXFA_i (i = 0, 1, 2, 3) is deasserted on the next RXCLK rising edge, after the word output in the RXDATA bus contains the payload byte (1, 2, … 48) indicated by RcvCADeassert[5:0] (register R_UICHCNF). Configuring RcvCADeassert[5:0] to an appropriate value ensures that the ATM Layer device can detect that the current ATM cell is the last cell in the FIFO, four clock cycles (or more) before reading the last word. **POS-UTOPIA Mode** RXFA_i (i = 0, 1, 2, 3) indicates the availability of data in FIFO #i. RXFA_i is asserted when the receive FIFO #i contains an end-of-packet **or** contains a number of 32-bit words equal to or greater than the “receive programmable watermark” (channel register R_PWM). RXFA_i (i = 0, 1, 2, 3) is deasserted when the receive FIFO #i does not contain an end of packet **and** contains a number of 32-bit words smaller than the “receive programmable watermark” (channel register R_PWM). The RXFA_i (i = 0, 1, 2, 3) are updated on the rising edge of RXCLK.
NOTE: See notes 1, 2, and 3 at the end of the table.			

Table 4. Pin Description (Sheet 37 of 66)

Pin Name	Pin	Type	Description
Transmit Single MPHY ATM/POS-UTOPIA Interface (Level 3 and Level 2 Modes)			
TXDATA[0]	K3	LVTTL Input	**Transmit UTOPIA Data Bus** TXDATA[63:0] carries the frame (cell or packet) word that is written to the transmit FIFO. TXDATA[63:0] are considered valid and written to a transmit FIFO only when the transmit interface is selected by using TXENB. TXDATA[63:0] transports the cell/packet data in 64-bit, 32-bit, 16-bit, or 8-bit format: • When configured in 64-bit mode, TXDATA[63:56] transports the most significant byte. • When configured in 32-bit mode, TXDATA[31:24] transports the most significant byte. • When configured in 16-bit mode, TXDATA[31:16] are unused inputs, TXDATA[15:0] are written into the FIFO and TXDATA[15:8] transports the most significant byte. • When configured in 8-bit mode, TXDATA[31:8] are unused inputs and TXDATA[7:0] are written into the FIFO. TXDATA[63:0] are sampled on the rising edge of TXCLK.
TXDATA[1]	J3		
TXDATA[2]	L5		
TXDATA[3]	G1		
TXDATA[4]	L6		
TXDATA[5]	J4		
TXDATA[6]	H2		
TXDATA[7]	K6		
TXDATA[8]	G3		
TXDATA[9]	H5		
TXDATA[10]	F3		
TXDATA[11]	J6		
TXDATA[12]	E1		
TXDATA[13]	G4		
TXDATA[14]	F4		
TXDATA[15]	E2		
TXDATA[16]	D3		
TXDATA[17]	D2		
TXDATA[18]	F5		
TXDATA[19]	E4		
TXDATA[20]	D4		
TXDATA[21]	G6		
TXDATA[22]	C1		
TXDATA[23]	E5		
TXDATA[24]	E7		
TXDATA[25]	B3		
TXDATA[26]	A4		
TXDATA[27]	A3		
TXDATA[28]	D7		
TXDATA[29]	F7		
TXDATA[30]	F8		
TXDATA[31]	B4		
NOTE: See notes 1, 2, and 3 at the end of the table.			

Table 4. Pin Description (Sheet 38 of 66)

Pin Name	Pin	Type	Description
TXDATA[32] TXDATA[33] TXDATA[34] TXDATA[35] TXDATA[36] TXDATA[37] TXDATA[38] TXDATA[39] TXDATA[40] TXDATA[41] TXDATA[42] TXDATA[43] TXDATA[44] TXDATA[45] TXDATA[46] TXDATA[47] TXDATA[48] TXDATA[49] TXDATA[50] TXDATA[51] TXDATA[52] TXDATA[53] TXDATA[54] TXDATA[55] TXDATA[56] TXDATA[57] TXDATA[58] TXDATA[59] TXDATA[60] TXDATA[61] TXDATA[62] TXDATA[63]		LVTTL Input	**NOTE:** The 32 most significant bits of the transmit UTOPIA data bus (TXDATA[63:32]) can be located in two different sets of pins. See "I/O Pin Equivalence on the Transmit TTL Line Side Interface" on page 84 and "TTL I/O Pin Equivalence on the Transmit OH/Alarm Insertion Ports" on page 87. When the 64-bit operation mode is selected (XmtUWidth = '11', register T_UICNF), the TXDATA[63:32] bus can be located in one of two different sets of pins: • If U64Mode (register GOCNF) is set to logic zero, then TXDATA[63:32] uses the transmit TTL line side interface pins. In this configuration, the device can only use the PECL line side interface. This configuration may be used in OC-48/OC-48c. • If U64Mode (register GOCNF) is set to logic one, then TXDATA[63:32] uses the transmit OH/Alarm insertion interface pins. In this configuration, the device uses only section overhead insertion. This configuration may be used in OC-12 and Quad OC-12c modes.
TXCLK	F10	LVTTL Input	**Transmit UTOPIA Clock**. TXCLK provides timing for the Intel IXF6048 transmit UTOPIA interface. TXCLK must cycle at a 104 MHz, or lower, instantaneous rate.
NOTE: See notes 1, 2, and 3 at the end of the table.			

Table 4. Pin Description (Sheet 39 of 66)

Pin Name	Pin	Type	Description
TXENB	D9	LVTTL Input	**Transmit Write Enable**. TXENB (active-low) controls write access to the transmit interface. TXENB can be used in two different ways: **Normal mode** (with port selection phase) This is the default mode of configuration (XmtSelMode = '0', register T_UICNF), compatible with the UTOPIA Level 3 and Level 2 specifications. • Port selection phase: when TXENB is deasserted, no read operations are performed and TXADDR[4:0] are sampled into latches to select (or reselect) a port for a data transfer. • Data transfer phase: when TXENB is asserted, the FIFO selected during the port selection phase is written. **Memory mapped device mode** (with no port selection phase) This configuration (XmtSelMode = '1', register T_UICNF) simplifies the standard UTOPIA interface by eliminating the port selection phase. Port selection is performed in a clock cycle basis: • When TXENB is deasserted, nothing happens. • When TXENB is asserted, the FIFO indicated by TXADDR[4:0] (on a clock cycle basis) is written. TXENB is sampled on the rising edge of TXCLK.
TXADDR[0] TXADDR[1] TXADDR[2] TXADDR[3] TXADDR[4]	A8 C9 D10 A9 D11	LVTTL Input	**Transmit Address Bus**. TXADDR[4:0] are used to perform two different processes: • To select a particular FIFO for a data transfer. • To poll the status of a particular FIFO (independently of TXENB). The most significant three bits of the address (TXADDR[4:2]) are compared with the base-address programmed value (UAddrBase[2:0], global register GOCNF) to determine if the device has been selected. The least significant two bits of the address (TXADDR[1:0]) are hard-wired to select a specific channel ('00' = channel 0, '01' = channel 1, '10' = channel 2, '11' = channel 3). The address value 1FH is the null physical address and cannot be assigned to any PHY port. TXADDR[4:0] are sampled on the rising edge of TXCLK.
TXSOF	M6	LVTTL Input	**Transmit Start-of-Frame**. TXSOF (active-high) marks the first word of a frame (cell or packet) in TXDATA. In transmission, all the frames (cells or packets) are input in TXDATA with the first frame byte located in the most significant byte position. TXSOF is sampled on the rising edge of TXCLK.
TXEOF	H1	LVTTL Input	**Transmit End-of-frame**. TXEOF (active-high) marks the last word of a frame (cell or packet) in TXDATA. TXEOF is used only in POS mode; in ATM mode, TXEOF is an unused input. TXEOF is sampled on the rising edge of TXCLK.
TXPRTY	J2	LVTTL Input	**Transmit Data Parity**. TXPRTY indicates the parity of TXDATA. Odd or even parity is selectable (see XmtPrtyCng in register T_UICHCNF). TXPRTY is sampled on the rising edge of TXCLK.
NOTE: See notes 1, 2, and 3 at the end of the table.			

Table 4. Pin Description (Sheet 40 of 66)

Pin Name	Pin	Type	Description
TXERR	K4	LVTTL Input	**Transmit Packet Error**. TXERR (active-high) is used only in POS mode; in ATM mode, TXERR is an unused input. TXERR is used by the Data Link Layer device to indicate that the current packet must be aborted (transmitted ending with an Abort sequence). After asserting TXERR, the next word written into the transmit FIFO should be the first word of the next packet (TXSOF asserted). After asserting TXERR, the writings to the FIFO are ignored until a start-of-frame (TXSOF asserted) is detected. When TXERR is asserted, both TXSOF and TXEOF are ignored. TXERR is sampled on the rising edge of TXCLK.
TXPADL[0] TXPADL[1] TXPADL[2]	A7 C7 C8	LVTTL Input	**Transmit Padding Length**. TXPADL[2:0] indicates the number of padding bytes included in the last word of the packet transferred in TXDATA. TXPADL[2:0] are used only in POS mode; in ATM-UTOPIA mode TXPADL[2:0] are unused inputs. Intel IXF6048 only accepts complete words on TXDATA except in the last word of a packet. Intel IXF6048 uses TXPADL[2:0] only when TXEOF is asserted (in the last word of a packet). When configured in 64-bit mode, the last word may contain zero, one, two, three, four, five, six, or seven padding bytes. In 32-bit mode, the last word may contain zero, one, two, or three padding bytes and only TXPADL[1:0] are used. When configured in 16-bit mode, the last word may contain zero or one padding byte and only TXPADL[0] is used. In 8-bit mode, TXPADL[1:0] are not used. **TXPADL[2:0] (64-bit mode)** '000' = Packet ends on TXDATA[7:0] (TXDATA = DDDDDDDD) '001' = Packet ends on TXDATA[15:8] (TXDATA = DDDDDDDP) '010' = Packet ends on TXDATA[23:16] (TXDATA = DDDDDDPP) '011' = Packet ends on TXDATA[31:24] (TXDATA = DDDDDPPP) '100' = Packet ends on TXDATA[39:32] (TXDATA = DDDDPPPP) '101' = Packet ends on TXDATA[47:40] (TXDATA = DDDPPPPP) '110' = Packet ends on TXDATA[55:48] (TXDATA = DDPPPPPP) '111' = Packet ends on TXDATA[63:56] (TXDATA = DPPPPPPP) **TXPADL[1:0] (32-bit mode)** '00' = Packet ends on TXDATA[7:0] (TXDATA = DDDD) '01' = Packet ends on TXDATA[15:8] (TXDATA = DDDP) '10' = Packet ends on TXDATA[23:16] (TXDATA = DDPP) '11' = Packet ends on TXDATA[31:24] (TXDATA = DPPP) **TXPADL[0] (16-bit mode)** '0' = Packet ends on TXDATA[7:0] (TXDATA = UUDD) '1' = Packet ends on TXDATA[15:8] (TXDATA = UUDP) **NOTE:** D = valid data byte, P = padding byte, U = unused byte TXPADL[2:0] are sampled on the rising edge of TXCLK.
NOTE: See notes 1, 2, and 3 at the end of the table.			

Table 4. Pin Description (Sheet 41 of 66)

Pin Name	Pin	Type	Description
TXPFA	B6	LVTTL Output 12 mA	**Transmit Polled Frame-Available Output**. TXPFA (active-high) is a tristatable signal used to indicate that the polled transmit FIFO has free available space. TXPFA is driven only after one (XmtDRCnf = '0', register T_UICHCNF) or two (XmtDRCnf = '1', register T_UICHCNF) clock cycles with an address in the TXADDR bus matching the programmed base-address value (UAddrBase[2:0], global register GOCNF). **ATM-UTOPIA Mode** TXPFA is used to perform cell-level handshake (polled transmit cell-available indication) and is asserted when the polled transmit FIFO has free available space to write one or more complete ATM cells. When the ATM cell being written into the UTOPIA interface is using the last cell-space available in the FIFO, TXPFA is deasserted on the same TXCLK rising edge that samples the word, written in the TXDATA bus, that contains the payload byte (1, 2, … 48) indicated by XmtCADeassert[5:0] (register T_UICHCNF). Only values of 9 to 48 are valid payload byte positions for XmtCADeassert[5:0]. Configuring XmtCADeassert[5:0] to an appropriate value, ensures that the ATM Layer device detects that the current ATM cell is going to fill up the transmit FIFO, four clock cycles (or more) before writing the last word. **POS-UTOPIA Mode** TXPFA indicates the availability of free space in the polled transmit FIFO. TXPFA is asserted when the polled FIFO available space (in 32-bit words) is greater than or equal to the “transmit nearly empty programmable watermark” (XmtNEPWM, channel register T_NEPWM). TXPFA is deasserted when the polled transmit FIFO is full or the available space (in 32-bit words) is less than the “transmit nearly full programmable watermark” (XmtNFPWM, channel register T_NFPWM). TXPFA is updated on the rising edge of TXCLK.
TXSFA	C5	LVTTL Output 12 mA	**Transmit Selected Frame-Available Output**. TXSFA (active-high) is a tristatable signal indicating the status of the selected transmit FIFO. TXSFA is used only in POS mode. TXSFA indicates the availability of free space in the selected FIFO while using TXPFA to poll a different PHY port. If the transmit interface is not selected for a transfer, TXSFA is tristated. TXSFA is driven one (XmtDRCnf = '0', register T_UICHCNF) or two (XmtDRCnf = '1', register T_UICHCNF) clock cycles after TXENB is asserted. TXSFA is asserted when the polled FIFO available space (in 32-bit words) is greater than or equal to the “transmit nearly empty programmable watermark” (XmtNEPWM, channel register T_NEPWM). TXSFA is deasserted when the polled transmit FIFO is full or the available space (in 32-bit words) is less than the “transmit nearly full programmable watermark” (XmtNFPWM, channel register T_NFPWM). TXSFA is updated on the rising edge of TXCLK.
NOTE: See notes 1, 2, and 3 at the end of the table.			

Table 4. Pin Description (Sheet 42 of 66)

Pin Name	Pin	Type	Description
TXFA_0 TXFA_1 TXFA_2 TXFA_3	D8 A5 A6 E8	LVTTL Output 12 mA	**Transmit Direct Frame-Available Outputs**. TXFA_i (i = 0, 1, 2, 3) is a tristatable active-high signal used to indicate the status of transmit FIFO #i. XmtDirStatCnf (global register T_UICNF) uses the TXFA_i outputs in two different ways: • When XmtDirStatCnf = '1' (direct status indication mode), the TXFA_i outputs (i = 0, 1, 2, 3) are always driven. • When XmtDMStatCnf = '0' (multiplexed status polling), the TXFA_i outputs (i = 0, 1, 2, 3) are driven (all four at the same time) only after one (XmtDRCnf = '0', register T_UICNF) or two (XmtDRCnf = '1', register T_UICNF) clock cycles, with an address in the TXADDR bus matching the programmed base-address value (UAddrBase[2:0], global register GOCNF). **ATM-UTOPIA Mode** TXFA_i (i = 0, 1, 2, 3) is used to perform cell-level handshake on transmit FIFO #i and goes high when the transmit FIFO #i has free available space to write one or more complete ATM cells. When the ATM cell being written into the UTOPIA interface is using the last cell-space available in FIFO #i, TXFA_i (i = 0, 1, 2, 3) is deasserted on the same TXCLK rising edge that samples the word written in the TXDATA bus that contains the payload byte (1, 2, … 48) indicated by XmtCADeassert[5:0] (register T_UICHCNF). Only values of 9 to 48 are valid payload byte positions for XmtCADeassert[5:0]. Configuring XmtCADeassert[5:0] to an appropriate value, ensures that the ATM Layer device will detect that the current ATM cell is going to fill up the transmit FIFO, four clock cycles (or more) before writing the last word. **POS-UTOPIA Mode** TXFA_i (i = 0, 1, 2, 3) indicates the availability of free space in FIFO #i. TXFA_i is asserted when the available space (in 32-bit words) of FIFO #i is equal to or greater than the “transmit nearly empty programmable watermark” (XmtNEPWM, channel register T_NEPWM). TXFA_i is deasserted when FIFO #i is full or the available space (in 32-bit words) is less than the “transmit nearly full programmable watermark” (XmtNFPWM, channel register T_NFPWM). The TXFA_i (i = 0, 1, 2, 3) outputs are updated on the rising edge of TXCLK.
NOTE: See notes 1, 2, and 3 at the end of the table.			

Table 4. Pin Description (Sheet 43 of 66)

Pin Name	Pin	Type	Description
Receive Quad 8-Bit Mode ATM/POS-UTOPIA Interface (Level 3 and Level 1 Modes)			
RXDATA_0[0] RXDATA_0[1] RXDATA_0[2] RXDATA_0[3] RXDATA_0[4] RXDATA_0[5] RXDATA_0[6] RXDATA_0[7] RXDATA_1[0] RXDATA_1[1] RXDATA_1[2] RXDATA_1[3] RXDATA_1[4] RXDATA_1[5] RXDATA_1[6] RXDATA_1[7] RXDATA_2[0] RXDATA_2[1] RXDATA_2[2] RXDATA_2[3] RXDATA_2[4] RXDATA_2[5] RXDATA_2[6] RXDATA_2[7] RXDATA_3[0] RXDATA_3[1] RXDATA_3[2] RXDATA_3[3] RXDATA_3[4] RXDATA_3[5] RXDATA_3[6] RXDATA_3[7]	D13 B13 A12 A14 A13 D14 F14 B14 D16 B18 B17 D17 A18 A19 F16 A20 F20 B23 B24 C22 E21 D21 C23 D22 A27 C25 B26 E23 C26 D25 B27 F23	LVTTL Output 12 mA	Receive UTOPIA data bus. RXDATA_i[7:0] (i = 0, 1, 2, 3) carries the frame (cell or packet) byte that is read from the receive FIFO #i. RXDATA_i[7:0] (i = 0, 1, 2, 3) is always driven. **NOTE:** Depending on the configuration of RcvDRCnf (register R_UICNF), a data transfer on RXDATA_i[7:0] happens one (UTOPIA Level 1) or two (UTOPIA Level 3) clock cycles after the assertion of RXENB_i (i = 0, 1, 2, 3). RXDATA_i[7:0] are updated on the rising edge of RXCLK_i (i = 0, 1, 2, 3).
RXCLK_0 RXCLK_1 RXCLK_2 RXCLK_3	E17 F17 E18 F18	LVTTL Input	**Receive UTOPIA Clock**. RXCLK_i (i = 0, 1, 2, 3) provides timing for the Intel IXF6048 receive system interface #i. RXCLK_i (i = 0, 1, 2, 3) must cycle at a 104 MHz, or lower, instantaneous rate.
NOTE: See notes 1, 2, and 3 at the end of the table.			

Table 4. Pin Description (Sheet 44 of 66)

Pin Name	Pin	Type	Description
RXENB_0 RXENB_1 RXENB_2 RXENB_3	E19 D19 F19 C20	LVTTL Input	**Receive Read Enable**. RXENB_i (i = 0, 1, 2, 3) is the active-low receive enable that controls read access from receive interface #i. • When RXENB_i (i = 0, 1, 2, 3) is deasserted, nothing happens on interface #i. • When RXENB_i (i = 0, 1, 2, 3) is asserted, FIFO #i is read and the data is output on RXDATA_i[7:0], RXPRTY_i, RXSOF_i, RXEOF_i, RXERR_i, and RXVAL_i after one or two clock cycles (see RcvDRCnf bit in register R_UICHCNF). RXENB_i (i = 0, 1, 2, 3) is sampled on the rising edge of RXCLK_i.
RXSOF_0 RXSOF_1 RXSOF_2 RXSOF_3	B11 C14 A22 B25	LVTTL Output 12 mA	**Receive Start-of-Frame**. RXSOF_i (i = 0, 1, 2, 3) (active-high) marks the first byte of a frame (cell or packet) in RXDATA_i[7:0]. RXSOF_i (i = 0, 1, 2, 3) is always driven. RXSOF_i (i = 0, 1, 2, 3) is updated on the rising edge of RXCLK_i.
RXEOF_0 RXEOF_1 RXEOF_2 RXEOF_3	C12 D15 B21 A25	LVTTL Output 12 mA	**Receive End-of-Frame**. RXEOF_i (i = 0, 1, 2, 3) (active-high) marks the last byte of a frame (cell or packet) in RXDATA_i. RXEOF_i is used only in POS mode; in ATM mode, this output is held in high impedance (see RcvTestOen in register R_UICNF). RXEOF_i (i = 0, 1, 2, 3) is always driven. RXEOF_i (i = 0, 1, 2, 3) is updated on the rising edge of RXCLK_i.
RXPRTY_0 RXPRTY_1 RXPRTY_2 RXPRTY_3	D12 C15 B22 D23	LVTTL Output 12 mA	**Receive Data Parity**. RXPRTY_i (i = 0, 1, 2, 3) indicates the parity of RXDATA_i[7:0]. Odd or even parity is selectable (see RcvPrtyCnf in register UICHCNF). RXPRTY_i (i = 0, 1, 2, 3) is always driven. RXPRTY_i (i = 0, 1, 2, 3) is updated on the rising edge of RXCLK_i.
RXERR_0 RXERR_1 RXERR_2 RXERR_3	E13 C16 C21 C24	LVTTL Output 12 mA	**Receive Packet Error**. RXERR_i (i = 0, 1, 2, 3) is the active-high packet error indication signal. RXERR_i is used only in POS mode; in ATM mode, this output is held in high impedance (see RcvTestOen in register UICNF). RXERR_i (i = 0, 1, 2, 3) is always driven. RXERR_i (i = 0, 1, 2, 3) is only asserted on the last word of a packet (when RXEOF_i is also asserted). When RXERR_i (i = 0, 1, 2, 3) is asserted, the packet must be discarded by the Data Link Layer device. RXERR_i is asserted if any of the following conditions are true: • The packet was aborted by the remote transmitter (received ending with an Abort sequence). • The packet contains an FCS error and RcvFCSErr (register R_PHCCNF) is set to logic one. • The packet is smaller than the programmable minimum packet length (register R_MINPL) and RcvMinPLDEn (register R_PHCCNF) is set to logic one. • The packet is longer than the programmable maximum packet length (register R_MAXPL) and RcvMaxPLDEn (register R_PHCCNF) is set to logic one. RXERR_i (i = 0, 1, 2, 3) is updated on the rising edge of RXCLK_i. When a FIFO overflow occurs, the frame is locally aborted and RXERR is asserted.
NOTE: See notes 1, 2, and 3 at the end of the table.			

Table 4. Pin Description (Sheet 45 of 66)

Pin Name	Pin	Type	Description
RXVAL_0 RXVAL_1 RXVAL_2 RXVAL_3	F13 E15 A23 D24	LVTTL Output 12 mA	**Receive Valid Data Output**. RXVAL_i (i = 0, 1, 2, 3) is the active-high data validation signal. RXVAL_i validates the receive output signals for interface #i: RXDATA_i, RXSOF_i, RXEOF_i, and RXERR_i. Note that RXPRTY_i (i = 0, 1, 2, 3) is valid independently of RXVAL_i. RXVAL_i (i = 0, 1, 2, 3) is used only in POS mode; in ATM mode, this output is held in high impedance (see RcvTestOen in register R_UICNF). RXVAL_i (i = 0, 1, 2, 3) is always driven. Depending on the configuration on RcvValCnf (register R_UICNF), RXVAL_i (i = 0, 1, 2, 3) can be used in two different ways: **RcvValCnf = '0'** RXVAL_i (i = 0, 1, 2, 3) assertion and deassertion is based only on the status of the receive FIFO #i. RXVAL_i is deasserted when attempting to read an empty FIFO (receive FIFO underflow). When the Data Link Layer device tries to read an empty receive FIFO #i, the read command is disregarded, the receive FIFO #i is not modified and the Data Link Layer device must ignore the value of the RXDATA_i, RXSOF_i, RXEOF_i, and RXERR_i. The receive FIFO underflow is not considered an error (no data is lost). **RcvValCnf = '1'** RXVAL_i (i = 0, 1, 2, 3) is used in the same way as for RcvValCnf = '0' (invalidation of RXDATA_i, RXSOF_i, RXEOF_i, and RXERR_i if FIFO #i is empty). In addition, RXVAL_i is also deasserted after reading the last byte of a packet, i.e., the next byte (start of the next packet) is not read from FIFO #i. When RXVAL_i is deasserted, the conditions FIFO-empty and end-of-packet are differentiated using RXEOF_i. This configuration allows the Link Layer device to synchronize with the packet boundaries. • If RXVAL_i (i = 0, 1, 2, 3) has been deasserted due to an interpacket boundary (when RcvValCnf = '1'), the Data Link Layer device must deassert RXENB_i during a clock cycle (or more) before reading the next packet. Otherwise, the receive FIFO will be blocked. • If RXVAL_i (i = 0, 1, 2, 3) is deasserted because FIFO #i is empty (RcvValCnf = '0' or '1'), the Data Link Layer device is not required to deassert RXENB_i. Once new data is received and written into FIFO #i, the Data Link Layer device can continue reading. RXVAL_i (i = 0, 1, 2, 3) is updated on the rising edge of RXCLK_i.
NOTE: See notes 1, 2, and 3 at the end of the table.			

Table 4. Pin Description (Sheet 46 of 66)

Pin Name	Pin	Type	Description
RXFA_0 RXFA_1 RXFA_2 RXFA_3	B12 A17 E20 A26	LVTTL Output 12 mA	**Receive Direct Frame-Available Output**. RXFA_i (i = 0, 1, 2, 3) is the active-high output signal indicating the status of receive FIFO #i. RXFA_i (i = 0, 1, 2, 3) outputs are always driven. **ATM-UTOPIA Mode** RXFA_i (i = 0, 1, 2, 3) is used to perform cell-level handshake on receive FIFO #i and goes high when receive FIFO #i contains one or more complete ATM cells. When the ATM cell being read in the UTOPIA interface is the last complete cell in FIFO #i, RXFA_i (i = 0, 1, 2, 3) is deasserted on the next RXCLK_i rising edge, after the word output in the RXDATA_i bus contains the payload byte (1, 2, … 48) indicated by RcvCADeassert[5:0] (register R_UICHCNF). Configuring RcvCADeassert[5:0] to an appropriate value, ensures that the ATM Layer device can detect that the current ATM cell is the last cell in the FIFO, four clock cycles (or more) before reading the last word. **POS-UTOPIA Mode** RXFA_i (i = 0, 1, 2, 3) indicates the availability of data in FIFO #i. RXFA_i is asserted when the receive FIFO #i contains an end-of-packet **or** contains a number of 32-bit words equal to or greater than the “receive programmable watermark” (channel register R_PWM). RXFA_i (i = 0, 1, 2, 3) is deasserted when the receive FIFO #i does not contain an end of packet **and** contains a number of 32-bit words smaller than the “receive programmable watermark” (channel register R_PWM). RXFA_i (i = 0, 1, 2, 3) is updated on the rising edge of RXCLK_i.
NOTE: See notes 1, 2, and 3 at the end of the table.			

Table 4. Pin Description (Sheet 47 of 66)

Pin Name	Pin	Type	Description
Transmit Quad 8-Bit Mode ATM/POS-UTOPIA Interface (Level 3 and Level 1 Modes)			
TXDATA_0[0] TXDATA_0[1] TXDATA_0[2] TXDATA_0[3] TXDATA_0[4] TXDATA_0[5] TXDATA_0[6] TXDATA_0[7] TXDATA_1[0] TXDATA_1[1] TXDATA_1[2] TXDATA_1[3] TXDATA_1[4] TXDATA_1[5] TXDATA_1[6] TXDATA_1[7] TXDATA_2[0] TXDATA_2[1] TXDATA_2[2] TXDATA_2[3] TXDATA_2[4] TXDATA_2[5] TXDATA_2[6] TXDATA_2[7] TXDATA_3[0] TXDATA_3[1] TXDATA_3[2] TXDATA_3[3] TXDATA_3[4] TXDATA_3[5] TXDATA_3[6] TXDATA_3[7]	K3 J3 L5 G1 L6 J4 H2 K6 G3 H5 F3 J6 E1 G4 F4 E2 D3 D2 F5 E4 D4 G6 C1 E5 E7 B3 A4 A3 D7 F7 F8 B4	LVTTL Input	**Transmit UTOPIA Data Bus** TXDATA_i[7:0] (i = 0, 1, 2, 3) carries the frame (cell or packet) byte that is written to the transmit FIFO #i. TXDATA_i[7:0] are considered valid and written to transmit FIFO #i only when TXENB_i is asserted. TXDATA_i[7:0] (i = 0, 1, 2, 3) is sampled on the rising edge of TXCLK_i.
TXCLK_0 TXCLK_1 TXCLK_2 TXCLK_3	F10 E10 F11 E11	LVTTL Input	**Transmit UTOPIA Clock**. TXCLK_i (i = 0, 1, 2, 3) provides timing for the Intel IXF6048 transmit UTOPIA interface. TXCLK_i must cycle at a 104 MHz, or lower, instantaneous rate.
NOTE: See notes 1, 2, and 3 at the end of the table.			

Table 4. Pin Description (Sheet 48 of 66)

Pin Name	Pin	Type	Description
TXENB_0 TXENB_1 TXENB_2 TXENB_3	D9 F9 B8 E9	LVTTL Input	**Transmit Write Enable**. TXENB_i (i = 0, 1, 2, 3) is the active-low transmit enable that controls write access to transmit interface #i. • When TXENB_i (i = 0, 1, 2, 3) is deasserted, nothing happens on interface #i. • When TXENB_i (i = 0, 1, 2, 3) is asserted, the transmit FIFO #i is written. TXENB_i (i = 0, 1, 2, 3) is sampled on the rising edge of TXCLK_i.
TXSOF_0 TXSOF_1 TXSOF_2 TXSOF_3	M6 K5 H6 C2	LVTTL Input	**Transmit Start-of-Frame**. TXSOF_i (i = 0, 1, 2, 3) (active-high) marks the first byte of a frame (cell or packet) in TXDATA_i[7:0]. TXSOF_i (i = 0, 1, 2, 3) is sampled on the rising edge of TXCLK_i.
TXEOF_0 TXEOF_1 TXEOF_2 TXEOF_3	H1 G2 G5 F6	LVTTL Input	**Transmit End-of-Frame**. TXEOF_i (i = 0, 1, 2, 3) (active-high) marks the last byte of a frame (cell or packet) in TXDATA_i[7:0]. TXEOF_i is used only in POS mode; in ATM mode, TXEOF_i is an unused input. TXEOF_i (i = 0, 1, 2, 3) is sampled on the rising edge of TXCLK_i.
TXPRTY_0 TXPRTY_1 TXPRTY_2 TXPRTY_3	J2 H4 D1 E6	LVTTL Input	**Transmit Data Parity**. TXPRTY (i = 0, 1, 2, 3) indicates the parity of TXDATA_i[7:0]. Either odd or even parity is selectable (see XmtPrtyCnf in register T_UICHCNF). TXPRTY_i (i = 0, 1, 2, 3) is sampled on the rising edge of TXCLK_i.
TXERR_0 TXERR_1 TXERR_2 TXERR_3	K4 J5 E3 C4	LVTTL Input	**Transmit Packet Error**. TXERR_i (i = 0, 1, 2, 3) is an active-high input allowing the Data Link Layer device to indicate that the current packet must be aborted (transmitted ending with an Abort sequence). TXERR_i is used only in POS mode; in ATM mode, TXERR_i is an unused input. After asserting TXERR_i (i = 0, 1, 2, 3), the next word written into transmit FIFO #i should be the first word of the next packet (TXSOF_i asserted). After asserting TXERR_i, the writings to transmit FIFO #i are ignored until a start-of-frame (TXSOF_i asserted) is detected. When TXERR_i is asserted, both TXSOF_i and TXEOF_i are ignored. TXERR_i (i = 0, 1, 2, 3) is sampled on the rising edge of TXCLK_i.
NOTE: See notes 1, 2, and 3 at the end of the table.			

Table 4. Pin Description (Sheet 49 of 66)

Pin Name	Pin	Type	Description
TXFA_0 TXFA_1 TXFA_2 TXFA_3	D8 A5 A6 E8	LVTTL Output 12 mA	**Transmit Direct Frame-Available Outputs**. TXFA_i (i = 0, 1, 2, 3) is the active-high output signal indicating the status of transmit FIFO #i. TXFA_i (i = 0, 1, 2, 3) outputs are always driven. **ATM-UTOPIA Mode** TXFA_i (i = 0, 1, 2, 3) is used to perform cell-level handshake on transmit FIFO #i and goes high when the transmit FIFO #i has free available space to write one or more complete ATM cells. When the ATM cell being written into the UTOPIA interface is using the last cell-space available in FIFO #i, TXFA_i (i = 0, 1, 2, 3) is deasserted on the same TXCLK_i rising edge that samples the word written in the TXDATA_i bus that contains the payload byte (1, 2, … 48) indicated by XmtCADeassert[5:0] (register T_UICHCNF). Only values 9 to 48 are valid payload byte positions for XmtCADeassert[5:0]. Configuring XmtCADeassert[5:0] to an appropriate value ensures that the ATM Layer device can detect that the current ATM cell is going to fill up the transmit FIFO four clock cycles (or more) before writing the last word. **POS-UTOPIA Mode** TXFA_i (i = 0, 1, 2, 3) indicates the availability of free space in FIFO #i. TXFA_i is asserted when the available space (in 32-bit words) of FIFO #i is equal to or greater than the “transmit nearly empty programmable watermark” (XmtNEPWM, channel register T_NEPWM). TXFA_i is deasserted when FIFO #i is full or the available space (in 32-bit words) is less than the “transmit nearly full programmable watermark” (XmtNFPWM, channel register T_NFPWM). The TXFA_i (i = 0, 1, 2, 3) outputs are updated on the rising edge of TXCLK_i.
NOTE: See notes 1, 2, and 3 at the end of the table.			

Table 4. Pin Description (Sheet 50 of 66)

Pin Name	Pin	Type	Description
Receive Quad 16-Bit Mode ATM/POS-UTOPIA Interface (Level 3 and Level 1 Modes)			
RXDATA_0[0]	D13		Receive UTOPIA data bus. RXDATA_i[15:0] (i = 0, 1, 2, 3) carries the frame (cell or packet) word that is read from the receive FIFO #i. The most significant (first received) byte is transported in RXDATA_i[15:8]. RXDATA_i[15:0] (i = 0, 1, 2, 3) is always driven. **NOTE:** Depending on the configuration of RcvDRCnf (register R_UICNF), a data transfer on RXDATA_i[15:0] happens one (UTOPIA Level 1) or two (UTOPIA Level 3) clock cycles after the assertion of RXENB_i (i = 0, 1, 2, 3). RXDATA_i[15:0] are updated on the rising edge of RXCLK_i (i = 0, 1, 2, 3).
RXDATA_0[1]	B13		
RXDATA_0[2]	A12		
RXDATA_0[3]	A14		
RXDATA_0[4]	A13		
RXDATA_0[5]	D14		
RXDATA_0[6]	F14		
RXDATA_0[7]	B14		
RXDATA_0[8]	D16		
RXDATA_0[9]	B18		
RXDATA_0[10]	B17		
RXDATA_0[11]	D17		
RXDATA_0[12]	A18		
RXDATA_0[13]	A19		
RXDATA_0[14]	F16		
RXDATA_0[15]	A20	LVTTL Output 12 mA	
RXDATA_1[0]	F20		
RXDATA_1[1]	B23		
RXDATA_1[2]	B24		
RXDATA_1[3]	C22		
RXDATA_1[4]	E21		
RXDATA_1[5]	D21		
RXDATA_1[6]	C23		
RXDATA_1[7]	D22		
RXDATA_1[8]	A27		
RXDATA_1[9]	C25		
RXDATA_1[10]	B26		
RXDATA_1[11]	E23		
RXDATA_1[12]	C26		
RXDATA_1[13]	D25		
RXDATA_1[14]	B27		
RXDATA_1[15]	F23		
NOTE: See notes 1, 2, and 3 at the end of the table.			

Table 4. Pin Description (Sheet 51 of 66)

Pin Name	Pin	Type	Description
RXDATA_2[0] RXDATA_2[1] RXDATA_2[2] RXDATA_2[3] RXDATA_2[4] RXDATA_2[5] RXDATA_2[6] RXDATA_2[7] RXDATA_2[8] RXDATA_2[9] RXDATA_2[10] RXDATA_2[11] RXDATA_2[12] RXDATA_2[13] RXDATA_2[14] RXDATA_2[15] RXDATA_3[0] RXDATA_3[1] RXDATA_3[2] RXDATA_3[3] RXDATA_3[4] RXDATA_3[5] RXDATA_3[6] RXDATA_3[7] RXDATA_3[8] RXDATA_3[9] RXDATA_3[10] RXDATA_3[11] RXDATA_3[12] RXDATA_3[13] RXDATA_3[14] RXDATA_3[15]		LVTTL Output 4 mA	**NOTE:** When the interface is configured in Quad mode (RcvUQuad = '1', register R_UICNF) and the data bus width is 16-bits (RcvUWidth = '01', register R_UICNF) the RXDATA_2[15:0] and RXDATA_3[15:0] can be located in two different sets of pins. See "I/O Pin Equivalence on the Receive TTL Line Side Interface" on page 82 and "TTL I/O Pin Equivalence on the Receive OH/Alarm Extraction Ports" on page 85: • If U64Mode (register GOCNF) is set to logic zero, RXDATA_2[15:0] and RXDATA_3[15:0] use the receive TTL line side interface pins. In this configuration, the device can only use the PECL line side interface. This configuration could be used in OC-48. • If U64Mode (register GOCNF) is set to logic one, RXDATA_2[15:0] and RXDATA_3[15:0] use the receive OH/Alarm extraction interface pins. In this configuration, the device uses only section overhead extraction. This configuration could be used in Quad OC-12c mode.
RXCLK_0 RXCLK_1 RXCLK_2 RXCLK_3	E17 F17 E18 F18	LVTTL Input	**Receive UTOPIA Clock**. RXCLK_i (i = 0, 1, 2, 3) provides timing for the Intel IXF6048 receive system interface #i. RXCLK_i (i = 0, 1, 2, 3) must cycle at a 66 MHz or lower instantaneous rate.
RXENB_0 RXENB_1 RXENB_2 RXENB_3	E19 D19 F19 C20	LVTTL Input	**Receive Read Enable**. RXENB_i (i = 0, 1, 2, 3) is the active-low receive enable that controls read access from receive interface #i. • When RXENB_i (i = 0, 1, 2, 3) is deasserted, nothing happens on interface #i. • When RXENB_i (i = 0, 1, 2, 3) is asserted, FIFO #i is read and the data is output in RXDATA_i[15:0], RXPRTY_i, RXSOF_i, RXEOF_i, RXERR_i, and RXVAL_i after one or two clock cycles (see RcvDRCnf bit in register R_UICHCNF). RXENB_i (i = 0, 1, 2, 3) is sampled on the rising edge of RXCLK_i.
NOTE: See notes 1, 2, and 3 at the end of the table.			

Table 4. Pin Description (Sheet 52 of 66)

Pin Name	Pin	Type	Description
RXSOF_0 RXSOF_1 RXSOF_2 RXSOF_3	B11 C14 A22 B25	LVTTL Output 12 mA	**Receive Start-of-Frame**. RXSOF_i (i = 0, 1, 2, 3) marks (active-high) the first word of a frame (cell or packet) in RXDATA_i[15:0]. RXSOF_i (i = 0, 1, 2, 3) is always driven. RXSOF_i (i = 0, 1, 2, 3) is updated on the rising edge of RXCLK_i.
RXEOF_0 RXEOF_1 RXEOF_2 RXEOF_3	C12 D15 B21 A25	LVTTL Output 12 mA	**Receive End-of-Frame**. RXEOF_i (i = 0, 1, 2, 3) marks (active-high) the last word of a frame (cell or packet) in RXDATA_i[15:0]. RXEOF_i is used only in POS mode; in ATM mode, this output is held in high impedance (see RcvTestOen in register R_UICNF). RXEOF_i (i = 0, 1, 2, 3) is always driven. RXEOF_i (i = 0, 1, 2, 3) is updated on the rising edge of RXCLK_i.
RXPRTY_0 RXPRTY_1 RXPRTY_2 RXPRTY_3	D12 C15 B22 D23	LVTTL Output 12 mA	**Receive Data Parity**. RXPRTY_i (i = 0, 1, 2, 3) indicates the parity of RXDATA_i[15:0]. Odd or even parity are selectable (see RcvPrtyCnf in register UICHCNF). RXPRTY_i (i = 0, 1, 2, 3) is always driven. RXPRTY_i (i = 0, 1, 2, 3) is updated on the rising edge of RXCLK_i.
RXERR_0 RXERR_1 RXERR_2 RXERR_3	E13 C16 C21 C24	LVTTL Output 12 mA	**Receive Packet Error**. RXERR_i (i = 0, 1, 2, 3) is the active-high packet error indication signal. RXERR_i is used only in POS mode; in ATM mode, this output is held in high impedance (see RcvTestOen in register UICNF). RXERR_i (i = 0, 1, 2, 3) is always driven. RXERR_i (i = 0, 1, 2, 3) is only asserted on the last word of a packet (when RXEOF_i is also asserted). When RXERR_i (i = 0, 1, 2, 3) is asserted, the packet must be discarded by the Data Link Layer device. RXERR_i is asserted if any of the following conditions are true: • The packet was aborted by the remote transmitter (received ending with an Abort sequence). • The packet contains an FCS error and RcvFCSErr (register R_PHCCNF) is set to logic one. • The packet is smaller than the programmable minimum packet length (register R_MINPL) and RcvMinPLDEn (register R_PHCCNF) is set to logic one. • The packet is longer than the programmable maximum packet length (register R_MAXPL) and RcvMaxPLDEn (register R_PHCCNF) is set to logic one. RXERR_i (i = 0, 1, 2, 3) is updated on the rising edge of RXCLK_i. When a FIFO overflow occurs, the frame is locally aborted and RXERR is asserted.
NOTE: See notes 1, 2, and 3 at the end of the table.			

Table 4. Pin Description (Sheet 53 of 66)

Pin Name	Pin	Type	Description
RXVAL_0 RXVAL_1 RXVAL_2 RXVAL_3	F13 E15 A23 D24	LVTTL Output 12 mA	**Receive Valid Data Output**. RXVAL_i (i = 0, 1, 2, 3) is the active-high data validation signal. RXVAL_i validates the receive output signals for interface #i: RXDATA_i, RXSOF_i, RXEOF_i, and RXERR_i; note that RXPRTY_i (i = 0, 1, 2, 3) is valid independently of RXVAL_i. RXVAL_i (i = 0, 1, 2, 3) is used only in POS mode; in ATM mode, this output is held in high impedance (see RcvTestOen in register R_UICNF). RXVAL_i (i = 0, 1, 2, 3) is always driven. Depending on the configuration on RcvValCnf (register R_UICNF), RXVAL_i (i = 0, 1, 2, 3) can be used in two different ways: **RcvValCnf = '0'** RXVAL_i (i = 0, 1, 2, 3) assertion and deassertion is based only on the status of the receive FIFO #i. RXVAL_i is deasserted when attempting to read an empty FIFO (receive FIFO underflow). When the Data Link Layer device tries to read an empty receive FIFO #i, the read command is disregarded, the receive FIFO #i is not modified and the Data Link Layer device must ignore the value of the RXDATA_i, RXSOF_i, RXEOF_i, and RXERR_i. The receive FIFO underflow is not considered an error (no data is lost). **RcvValCnf = '1'** RXVAL_i (i = 0, 1, 2, 3) is used in the same way as for RcvValCnf = '0' (invalidation of RXDATA_i, RXSOF_i, RXEOF_i, and RXERR_i if FIFO #i is empty). In addition, RXVAL_i is also deasserted after reading the last byte of a packet, i.e. the next byte (start of the next packet) is not read from FIFO #i. When RXVAL_i is deasserted, the conditions FIFO-empty and end-of-packet are differentiated using RXEOF_i. This configuration allows the Link Layer device to synchronize with the packet boundaries. • If RXVAL_i (i = 0, 1, 2, 3) has been deasserted due to an interpacket boundary (when RcvValCnf = '1'), the Data Link Layer device must deassert RXENB_i during a clock cycle (or more) before reading the next packet. Otherwise, the receive FIFO will be blocked. • If RXVAL_i (i = 0, 1, 2, 3) is deasserted because FIFO #i is empty (RcvValCnf = '0' or '1'), the Data Link Layer device is not required to deassert RXENB_i. Once new data is received and written into FIFO #i, the Data Link Layer device can continue reading. RXVAL_i (i = 0, 1, 2, 3) is updated on the rising edge of RXCLK_i.
RXPADL_0 RXPADL_1 RXPADL_2 RXPADL_3	B10 F12 E12 A10	LVTTL Output 12 mA	**Receive Padding Length**. RXPADL_i (i = 0, 1, 2, 3) indicates the number of padding bytes included in the last word of the packet transferred in RXDATA_i[15:0]. RXPADL_i is used only in POS mode; in ATM mode, RXPADL_i is held in high impedance. Intel IXF6048 only outputs complete words on RXDATA_i (i = 0, 1, 2, 3) except in the last word of a packet. RXPADL_i should be used only when RXEOF_i is asserted (in the last word of a packet); when RXEOF_i is not asserted RXPADL_i outputs the value '0' indicating that the two bytes are valid. When configured in 8-bit mode, RXPADL_i (i = 0, 1, 2, 3) is held in high impedance. RXPADL_i, i = 0, 1, 2, 3 (16-bit mode) '0' = packet ends on RXDATA_i[7:0] (RXDATA_i = DD) '1' = packet ends on RXDATA_i[15:8] (RXDATA_i = DP) **NOTE:** D = valid data byte, P = padding byte RXPADL_i (i = 0, 1, 2, 3) is updated on the rising edge of RXCLK_i.
NOTE: See notes 1, 2, and 3 at the end of the table.			

Table 4. Pin Description (Sheet 54 of 66)

Pin Name	Pin	Type	Description
RXFA_0 RXFA_1 RXFA_2 RXFA_3	B12 A17 E20 A26	LVTTL Output 12 mA	**Receive Direct Frame-Available Output**. RXFA_i (i = 0, 1, 2, 3) is the active-high output signal indicating the status of receive FIFO #i. RXFA_i (i = 0, 1, 2, 3) outputs are always driven. **ATM-UTOPIA Mode** RXFA_i (i = 0, 1, 2, 3) is used to perform cell-level handshake on receive FIFO #i and goes high when the receive FIFO #i contains one or more complete ATM cells. When the ATM cell being read in the UTOPIA interface is the last complete cell in FIFO #i, RXFA_i (i = 0, 1, 2, 3) is deasserted on the next RXCLK_i rising edge, after the word output in the RXDATA_i bus contains the payload byte (1, 2, … 48) indicated by RcvCADeassert[5:0] (register R_UICHCNF). Configuring RcvCADeassert[5:0] to an appropriate value ensures that the ATM Layer device can detect that the current ATM cell is the last cell in the FIFO, four clock cycles (or more) before reading the last word. **POS-UTOPIA Mode** RXFA_i (i = 0, 1, 2, 3) indicates the availability of data in FIFO #i. RXFA_i is asserted when the receive FIFO #i contains an end-of-packet **or** contains a number of 32-bit words equal to or greater than the “receive programmable watermark” (channel register R_PWM). RXFA_i (i = 0, 1, 2, 3) is deasserted when the receive FIFO #i does not contain an end of packet **and** contains a number of 32-bit words smaller than the “receive programmable watermark” (channel register R_PWM). RXFA_i (i = 0, 1, 2, 3) is updated on the rising edge of RXCLK_i.
NOTE: See notes 1, 2, and 3 at the end of the table.			

Table 4. Pin Description (Sheet 55 of 66)

Pin Name	Pin	Type	Description
Transmit Quad 16-Bit Mode ATM/POS-UTOPIA Interface (Level 3 and Level 1 Modes)			
TXDATA_0[0]	K3	LVTTL Input	**Transmit UTOPIA Data Bus** TXDATA_i[15:0] (i = 0, 1, 2, 3) carries the frame (cell or packet) word that is written to the transmit FIFO #i. The most significant (first transmitted) byte is transported in TXDATA_i[15:8]. TXDATA_i[15:0] are considered valid and written to transmit FIFO #i only when TXENB_i is asserted. TXDATA_i[15:0] (i = 0, 1, 2, 3) is sampled on the rising edge of TXCLK_i.
TXDATA_0[1]	J3		
TXDATA_0[2]	L5		
TXDATA_0[3]	G1		
TXDATA_0[4]	L6		
TXDATA_0[5]	J4		
TXDATA_0[6]	H2		
TXDATA_0[7]	K6		
TXDATA_0[8]	G3		
TXDATA_0[9]	H5		
TXDATA_0[10]	F3		
TXDATA_0[11]	J6		
TXDATA_0[12]	E1		
TXDATA_0[13]	G4		
TXDATA_0[14]	F4		
TXDATA_0[15]	E2		
TXDATA_1[0]	D3		
TXDATA_1[1]	D2		
TXDATA_1[2]	F5		
TXDATA_1[3]	E4		
TXDATA_1[4]	D4		
TXDATA_1[5]	G6		
TXDATA_1[6]	C1		
TXDATA_1[7]	E5		
TXDATA_1[8]	E7		
TXDATA_1[9]	B3		
TXDATA_1[10]	A4		
TXDATA_1[11]	A3		
TXDATA_1[12]	D7		
TXDATA_1[13]	F7		
TXDATA_1[14]	F8		
TXDATA_1[15]	B4		
NOTE: See notes 1, 2, and 3 at the end of the table.			

Table 4. Pin Description (Sheet 56 of 66)

Pin Name	Pin	Type	Description
TXDATA_2[0] TXDATA_2[1] TXDATA_2[2] TXDATA_2[3] TXDATA_2[4] TXDATA_2[5] TXDATA_2[6] TXDATA_2[7] TXDATA_2[8] TXDATA_2[9] TXDATA_2[10] TXDATA_2[11] TXDATA_2[12] TXDATA_2[13] TXDATA_2[14] TXDATA_2[15] TXDATA_3[0] TXDATA_3[1] TXDATA_3[2] TXDATA_3[3] TXDATA_3[4] TXDATA_3[5] TXDATA_3[6] TXDATA_3[7] TXDATA_3[8] TXDATA_3[9] TXDATA_3[10] TXDATA_3[11] TXDATA_3[12] TXDATA_3[13] TXDATA_3[14] TXDATA_3[15]		LVTTL Input	**NOTE:** When the interface is configured in Quad mode (XmtUQuad = '1', register T_UICNF) and the data bus width is 16-bits (XmtUWidth = '01', register T_UICNF) the TXDATA_2[15:0] and TXDATA_3[15:0] buses can be located in one of two different sets of pins. See "I/O Pin Equivalence on the Transmit TTL Line Side Interface" on page 84 and "TTL I/O Pin Equivalence on the Transmit OH/Alarm Insertion Ports" on page 87: • If U64Mode (register GOCNF) is set to logic zero, TXDATA_2[15:0] and TXDATA_3[15:0] use the transmit TTL line side interface pins. In this configuration, the device can only use the PECL line side interface. This configuration could be used in OC-48. • If U64Mode (register GOCNF) is set to logic one, TXDATA_2[15:0] and TXDATA_3[15:0] use the transmit OH/Alarm extraction interface pins. In this configuration, the device uses only section overhead extraction. This configuration could be used in Quad OC-12c mode.
TXCLK_0 TXCLK_1 TXCLK_2 TXCLK_3	F10 E10 F11 E11	LVTTL Input	**Transmit UTOPIA Clock**. TXCLK_i (i = 0, 1, 2, 3) provides timing for the Intel IXF6048 transmit UTOPIA interface. TXCLK_i must cycle at a 66 MHz or lower instantaneous rate.
TXENB_0 TXENB_1 TXENB_2 TXENB_3	D9 F9 B8 E9	LVTTL Input	**Transmit Write Enable**. TXENB_i (i = 0, 1, 2, 3) is the active-low transmit enable that controls write access to transmit interface #i. • When TXENB_i (i = 0, 1, 2, 3) is deasserted, nothing happens on interface #i. • When TXENB_i (i = 0, 1, 2, 3) is asserted, the transmit FIFO #i is written. TXENB_i (i = 0, 1, 2, 3) is sampled on the rising edge of TXCLK_i.
NOTE: See notes 1, 2, and 3 at the end of the table.			

Table 4. Pin Description (Sheet 57 of 66)

Pin Name	Pin	Type	Description
TXSOF_0 TXSOF_1 TXSOF_2 TXSOF_3	M6 K5 H6 C2	LVTTL Input	**Transmit Start-of-Frame**. TXSOF_i (i = 0, 1, 2, 3) marks (active-high) the first byte of a frame (cell or packet) in TXDATA_i[15:0]. TXSOF_i (i = 0, 1, 2, 3) is sampled on the rising edge of TXCLK_i.
TXEOF_0 TXEOF_1 TXEOF_2 TXEOF_3	H1 G2 G5 F6	LVTTL Input	**Transmit End-of-Frame**. TXEOF_i (i = 0, 1, 2, 3) marks (active-high) the last byte of a frame (cell or packet) in TXDATA_i[15:0]. TXEOF_i is used only in POS mode; in ATM mode, TXEOF_i is an unused input. TXEOF_i (i = 0, 1, 2, 3) is sampled on the rising edge of TXCLK_i.
TXPRTY_0 TXPRTY_1 TXPRTY_2 TXPRTY_3	J2 H4 D1 E6	LVTTL Input	**Transmit Data Parity**. TXPRTY (i = 0, 1, 2, 3) indicates the parity of TXDATA_i[15:0]. Odd or even parity are selectable (see XmtPrtyCnf in register T_UICHCNF). TXPRTY_i (i = 0, 1, 2, 3) is sampled on the rising edge of TXCLK_i.
TXERR_0 TXERR_1 TXERR_2 TXERR_3	K4 J5 E3 C4	LVTTL Input	**Transmit Packet Error**. TXERR_i (i = 0, 1, 2, 3) is an active-high input allowing the Data Link Layer device to indicate that the current packet must be aborted (transmitted ending with an Abort sequence). TXERR_i is used only in POS mode; in ATM mode, TXERR_i is an unused input. After asserting TXERR_i (i = 0, 1, 2, 3), the next word written into transmit FIFO #i should be the first word of the next packet (TXSOF_i asserted). After asserting TXERR_i, the writings to transmit FIFO #i are ignored until a start-of-frame (TXSOF_i asserted) is detected. When TXERR_i is asserted, both TXSOF_i and TXEOF_i are ignored. TXERR_i (i = 0, 1, 2, 3) is sampled on the rising edge of TXCLK_i.
TXPADL_0 TXPADL_1 TXPADL_2 TXPADL_3	A7 C7 C8 B7	LVTTL Input	**Transmit Padding Length**. TXPADL_i (i = 0, 1, 2, 3) indicates the number of padding bytes included in the last word of the packet transferred in TXDATA_i[15:0]. TXPADL_i is used only in POS mode; in ATM-UTOPIA mode TXPADL_i (i = 0, 1, 2, 3) are unused inputs. Intel IXF6048 only accepts complete words on TXDATA_i[15:0] except in the last word of a packet. Intel IXF6048 uses TXPADL_i only when TXEOF_i (i = 0, 1, 2, 3) is asserted (in the last word of a packet). When configured in 16-bit mode, the last word may contain zero or one padding byte. In 8-bit mode, TXPADL_i (i = 0, 1, 2, 3) is not used. **TXPADL_i, i = 0, 1, 2, 3 (16-Bit Mode)** '0' = packet ends on TXDATA[7:0] (TXDATA = DD) '1' = packet ends on TXDATA[15:8] (TXDATA = DP) **NOTE:** D = valid data byte, P = padding byte TXPADL_i (i = 0, 1, 2, 3) is sampled on the rising edge of TXCLK_i.
NOTE: See notes 1, 2, and 3 at the end of the table.			

Table 4. Pin Description (Sheet 58 of 66)

Pin Name	Pin	Type	Description
TXFA_0 TXFA_1 TXFA_2 TXFA_3	D8 A5 A6 E8	LVTTL Output 12 mA	**Transmit Direct Frame-Available Outputs**. TXFA_i (i = 0, 1, 2, 3) is the active-high output signal indicating the status of transmit FIFO #i. TXFA_i (i = 0, 1, 2, 3) outputs are always driven. **ATM-UTOPIA Mode** TXFA_i (i = 0, 1, 2, 3) is used to perform cell-level handshake on transmit FIFO #i and goes high when the transmit FIFO #i has free available space to write one or more complete ATM cells. When the ATM cell being written into the UTOPIA interface is using the last cell-space available in FIFO #i, TXFA_i (i = 0, 1, 2, 3) is deasserted on the same TXCLK_i rising edge that samples the word written in the TXDATA_i bus that contains the payload byte (1, 2, … 48) indicated by XmtCADeassert[5:0] (register T_UICHCNF). Only values 9 to 48 are valid payload byte positions for XmtCADeassert[5:0]. Configuring XmtCADeassert[5:0] to an appropriate value ensures that the ATM Layer device can detect that the current ATM cell is going to fill up the transmit FIFO four clock cycles (or more) before writing the last word. **POS-UTOPIA Mode** TXFA_i (i = 0, 1, 2, 3) indicates the availability of free space in FIFO #i. TXFA_i is asserted when the available space (in 32-bit words) of FIFO #i is equal to or greater than the “transmit nearly empty programmable watermark” (XmtNEPWM, channel register T_NEPWM). TXFA_i is deasserted when FIFO #i is full or the available space (in 32-bit words) is less than the “transmit nearly full programmable watermark” (XmtNFPWM, channel register T_NFPWM). The TXFA_i (i = 0, 1, 2, 3) outputs are updated on the rising edge of TXCLK_i.
NOTE: See notes 1, 2, and 3 at the end of the table.			

Table 4. Pin Description (Sheet 59 of 66)

Pin Name	Pin	Type	Description
Microprocessor Interface			
A[0] A[1] A[2] A[3] A[4] A[5] A[6] A[7] A[8] A[9] A[10]	P26 P31 P28 P29 P30 R29 R28 R27 R26 R31 R30	LVTTL Input	**Address Bus 10 Bits**. Microprocessor interface address bus. **NOTE:** As Intel IXF6048 is a sixteen-bit device (software registers are sixteen-bit wide) the address bus of most microcontrollers has to be connected to Intel IXF6048 address bus in the following way: Intel IXF6048 A[0] ≡ microcontroller A[1] (Least significant bit) Intel IXF6048 A[1] ≡ microcontroller A[2] …… Intel IXF6048 A[10] ≡ microcontroller A[11] (Most significant bit)
D[0] D[1] D[2] D[3] D[4] D[5] D[6] D[7] D[8] D[9] D[10] D[11] D[12] D[13] D[14] D[15]	T29 T28 T27 T26 V31 V30 U29 U28 U27 U26 W31 W30 Y30 Y31 W28 W29	LVTTL Bidir 4 mA	**Data Bus 16 Bits**. Microprocessor interface data bus. D[0] is the least significant bit. D[15] is the least significant bit.
WRB/RWB	N26	LVTTL Input	**Write-Bar Intel; Read/Write Bar Motorola***
RDB/E	M31	LVTTL Input	**Read-Bar Intel; Enable Motorola***
INT	L31	LVTTL Output 2 mA	**Interrupt Request**. INT goes low when an Intel IXF6048 interrupt bit is active and unmasked. After clearing the interrupt bit (by reading the corresponding register), INT goes to high impedance. INT is an open-drain output that requires an external pull-up resistor.
CSB	N27	LVTTL Input	**Chip Select**. The active-low chip select signal is low during Intel IXF6048 register accesses.
ALE	N28	LVTTL Input (60K pull up)	**Address Latch Enable**. The address latch enable latches the address bus when low, which allows interfacing to a multiplexed address/data bus. When ALE is high, the internal latches are transparent. ALE has an internal pull-up resistor.
MCUTYPE	N29	LVTTL Input	**Motorola*/Intel Interface Mode Select** '0' = Intel Microprocessor '1' = Motorola* Microprocessor
NOTE: See notes 1, 2, and 3 at the end of the table.			

Table 4. Pin Description (Sheet 60 of 66)

Pin Name	Pin	Type	Description
GENIO	K31	LVTTL Bidir 4 mA	**Generic Input/output Controllable Via the Microprocessor Interface** If configuration bit GenIOMode (register GOCNF) is set to '0', then GENIO ball is an input. The value of GENIO input can be read via the microprocessor interface (status bit GenIOVal in register GOCNF). If configuration bit GenIOMode (register GOCNF) is set to '1', then GENIO ball is an output. GENIO output value can be set via the microprocessor interface (configuration bit GenIOVal in register GOCNF).
RESET	N30	LVTTL Input (60K pull up)	**Asynchronous Chip Reset**. A low resets all registers to their default values. RESET is a Schmitt-triggered input and uses an internal pull-up resistor.
OEN	N31	LVTTL Input (60K pull up)	**Master Chip Output Enable**. Active-high. A low sets all outputs and bidirectional pins to high impedance. In order to avoid collisions that could damage the device when several PHY devices are connected into the same UTOPIA interface, **the software must configure the UTOPIA interface (physical address of the device, decode-response delay, ATM/POS mode, etc.) before setting OEN to logic one.** OEN is internally ORed to configuration bit OutEn (register GOCNF)
UOEN	P27	LVTTL Input (60K pull up)	**UTOPIA Output Enable**. Active-high. A low sets all UTOPIA outputs to high impedance if bits RcvUOutEnCnf and XmtUOutEnCnf (register GOCNF) are also low. In order to avoid collisions that could damage the device when several PHY devices are connected into the same UTOPIA interface, **the software must configure the UTOPIA interface (physical address of the device, decode-response delay, ATM/POS mode, etc.) before setting UOEN to logic one.** UOEN is internally ORed to configuration bit UOutEn (register GOCNF) and the result is ANDed with the inversion of RcvUOutEnCnf to generate an output enable signal for the receive UTOPIA interface and ANDed with the inversion of XmtUOutEnCnf to generate an output enable signal for the transmit UTOPIA interface.
NOTE: See notes 1, 2, and 3 at the end of the table.			

Table 4. Pin Description (Sheet 61 of 66)

Pin Name	Pin	Type	Description
JTAG and SCAN Test Ports			
JTCK	L28	LVTTL Input	**JTAG Clock**. Clock for all boundary scan circuitry.
JTMS	M26	LVTTL Input (60K pull up)	**JTAG Test Mode Select**. Determine state of TAP controller.
JTRS	L29	LVTTL Input (60K pull up)	**JTAG Reset**. (Active-low)
JTDI	L30	LVTTL Input (60K pull up)	**JTAG Data Input**. Input signal used to shift in instructions and data.
JTDO	L27	LVTTL Output 2 mA	**JTAG Data Output**. Output signal used to shift out instructions and data.
SCANTEST	M29	LVTTL Input (60K pull up)	**Scan Test Mode**. (Active-low)
SCANEN	M30	LVTTL Input (60K pull up)	**Scan Enable**. (Active-low)
NOTE: See notes 1, 2, and 3 at the end of the table.			

Table 4. Pin Description (Sheet 62 of 66)

Pin Name	Pin	Type	Description
Power Supply			
VDD_CORE	A11	Digital Power Core	**2.5 V Core Supply**
VDD_CORE	C6		
VDD_CORE	AA6		
VDD_CORE	AB29		
VDD_CORE	AG4		
VDD_CORE	AG22		
VDD_CORE	AH9		
VDD_CORE	AH30		
VDD_CORE	AJ11		
VDD_CORE	AL16		
VDD_CORE	AL18		
VDD_CORE	C3		
VDD_CORE	D31		
VDD_CORE	E16		
VDD_CORE	E22		
VDD_CORE	F1		
VDD_CORE	F25		
VDD_CORE	G29		
VDD_CORE	K2		
VDD_CORE	M27		
VDD_CORE	N4		
VDD_CORE	V2		
VDD_CORE	V29		
NOTE: See notes 1, 2, and 3 at the end of the table.			

Table 4. Pin Description (Sheet 63 of 66)

Pin Name	Pin	Type	Description
GND_CORE	AA28	Digital Ground Core	**GND**. Ground pin for Core supply.
GND_CORE	AD3		
GND_CORE	AF28		
GND_CORE	AG9		
GND_CORE	AH2		
GND_CORE	AH22		
GND_CORE	AJ17		
GND_CORE	AL11		
GND_CORE	AL15		
GND_CORE	C11		
GND_CORE	B29		
GND_CORE	B5		
GND_CORE	C17		
GND_CORE	D6		
GND_CORE	F2		
GND_CORE	F21		
GND_CORE	D30		
GND_CORE	G30		
GND_CORE	L4		
GND_CORE	M2		
GND_CORE	M28		
GND_CORE	V1		
GND_CORE	V26		
NOTE: See notes 1, 2, and 3 at the end of the table.			

Table 4. Pin Description (Sheet 64 of 66)

Pin Name	Pin	Type	Description
VDD_TTL	A24		
VDD_TTL	AA4		
VDD_TTL	AC6		
VDD_TTL	AD2		
VDD_TTL	AD28		
VDD_TTL	AE3		
VDD_TTL	AF7		
VDD_TTL	AF9		
VDD_TTL	AG7		
VDD_TTL	AG26		
VDD_TTL	AH6		
VDD_TTL	AH26		
VDD_TTL	AJ3		
VDD_TTL	AJ5		
VDD_TTL	AK5		
VDD_TTL	AK27		
VDD_TTL	AL5	Power	
VDD_TTL	AL27	TTL	**3.3 V I/O Supply**
VDD_TTL	C10	IO	
VDD_TTL	C13		
VDD_TTL	D20		
VDD_TTL	D5		
VDD_TTL	D18		
VDD_TTL	E14		
VDD_TTL	F15		
VDD_TTL	F22		
VDD_TTL	E24		
VDD_TTL	E25		
VDD_TTL	G26		
VDD_TTL	H3		
VDD_TTL	K29		
VDD_TTL	U4		
VDD_TTL	U5		
VDD_TTL	V27		
VDD_TTL	V28		

NOTE: See notes 1, 2, and 3 at the end of the table.

Table 4. Pin Description (Sheet 65 of 66)

Pin Name	Pin	Type	Description
GND_TTL	A1	Ground TTL IO	**GND**. Ground pin for I/O supply.
GND_TTL	A2		
GND_TTL	A15		
GND_TTL	A16		
GND_TTL	A30		
GND_TTL	A31		
GND_TTL	AK1		
GND_TTL	AK2		
GND_TTL	AK3		
GND_TTL	AK4		
GND_TTL	AK28		
GND_TTL	AK29		
GND_TTL	AK30		
GND_TTL	AK31		
GND_TTL	AL1		
GND_TTL	AL2		
GND_TTL	AL3		
GND_TTL	AL4		
GND_TTL	AL28		
GND_TTL	AL29		
GND_TTL	AL30		
GND_TTL	AL31		
GND_TTL	B1		
GND_TTL	B2		
GND_TTL	B15		
GND_TTL	B16		
GND_TTL	B30		
GND_TTL	B31		
GND_TTL	R1		
GND_TTL	R2		
GND_TTL	T1		
GND_TTL	T2		
GND_TTL	T30		
GND_TTL	T31		
GND_TTL	U30		
GND_TTL	U31		
NOTE: See notes 1, 2, and 3 at the end of the table.			

Table 4. Pin Description (Sheet 66 of 66)

Pin Name	Pin	Type	Description
VDD_PECL VDD_PECL VDD_PECL VDD_PECL VDD_PECL VDD_PECL VDD_PECL VDD_PECL VDD_PECL VDD_PECL VDD_PECL VDD_PECL	AJ26 AJ22 AL19 AH17 AJ16 AH14 AH15 AH12 AH13 AF10 AF11 AJ7 AJ8	Power PECL IO	**3.3 V I/O Supply**
GND_PECL GND_PECL GND_PECL GND_PECL GND_PECL GND_PECL GND_PECL GND_PECL GND_PECL GND_PECL GND_PECL GND_PECL GND_PECL	AF22 AK19 AK18 AL17 AF16 AL13 AL14 AJ12 AK11 AJ9 AJ10 AF8 AH7 AL6	Ground PECL IO	**GND**. Ground pin for I/O supply.
NOT CONNECTED	K30	N/C	Not connected.

NOTES:
1. When the UTOPIA interface (receive or transmit) is configured in 64-bit mode, the 32 most significant bits of the data bus (RXDATA[63:32] and TXDATA[63:32]) can be connected to one of two different groups of pins. See Table 5–Table 11 for more details.
2. When the UTOPIA interface (receive or transmit) is configured in quad 16-bit mode, the 8 most significant bits of each data bus (RXDATA_i[15:8] and TXDATA_i[15:8], i = 0, 1, 2, 3) can be connected to one of two different groups of pins. See Table 5–Table 11 for more details.
3. Unused LVTTL inputs should be tied directly to ground except RPDI pins for which, since they can be configured as bidirectional via a register setting, it is highly recommended to tie the unused input pins to ground through a 1 KΩ resistor. This protects against UTOPIA port damage in case of accidental activation of the 64-bit UTOPIA mode. For unused PECL inputs, P pins should be tied to VDD_PECL and N pins to GND_PECL

NOTE: See notes 1, 2, and 3 at the end of the table.

Table 5. PECL I/O Pin Equivalence on the Line Side Interface

Pin #	Rx PECL Parallel Single	PECL Serial Quad	Pin #	Tx PECL Parallel Single	PECL Serial Quad
AH20	RPDI_P[0]	TSCI_P0	AK15	TPDO_P[0]	TSDO_P0
AJ20	RPDI_N[0]	TSCI_N0	AJ15	TPDO_N[0]	TSDO_N0
AF20	RPDI_P[1]		AG15	TPDO_P[1]	
AG20	RPDI_N[1]		AF15	TPDO_N[1]	
AK21	RPDI_P[2]	TSCI_P1	AK14	TPDO_P[2]	TSCO_P0
AL21	RPDI_N[2]	TSCI_N1	AJ14	TPDO_N[2]	TSCO_N0
AH21	RPDI_P[3]		AG14	TPDO_P[3]	
AJ21	RPDI_N[3]		AF14	TPDO_N[3]	
AF21	RPDI_P[4]	TSCI_P2	AK13	TPDO_P[4]	TSDO_P1
AG21	RPDI_N[4]	TSCI_N2	AJ13	TPDO_N[4]	TSDO_N1
AK22	RPDI_P[5]		AG13	TPDO_P[5]	
AL22	RPDI_N[5]		AF13	TPDO_N[5]	
AK23	RPDI_P[6]	TSCI_P3	AK12	TPDO_P[6]	TSCO_P1
AL23	RPDI_N[6]	TSCI_N3	AL12	TPDO_N[6]	TSCO_N1
AH23	RPDI_P[7]		AG12	TPDO_P[7]	
AJ23	RPDI_N[7]		AF12	TPDO_N[7]	
AF23	RPDI_P[8]	RSDI_P0	AH11	TPDO_P[8]	TSDO_P2
AG23	RPDI_N[8]	RSDI_N0	AG11	TPDO_N[8]	TSDO_N2
AK24	RPDI_P[9]	RSCI_P0	AL10	TPDO_P[9]	
AL24	RPDI_N[9]	RSCI_N0	AK10	TPDO_N[9]	
AH24	RPDI_P[10]	RSDI_P1	AH10	TPDO_P[10]	TSCO_P2
AJ24	RPDI_N[10]	RSDI_N1	AG10	TPDO_N[10]	TSCO_N2
AF24	RPDI_P[11]	RSCI_P1	AL9	TPDO_P[11]	
AG24	RPDI_N[11]	RSCI_N1	AK9	TPDO_N[11]	
AK25	RPDI_P[12]	RSDI_P2	AL8	TPDO_P[12]	TSDO_P3
AL25	RPDI_N[12]	RSDI_N2	AK8	TPDO_N[12]	TSDO_N3
AH25	RPDI_P[13]	RSCI_P2	AH8	TPDO_P[13]	
AJ25	RPDI_N[13]	RSCI_N2	AG8	TPDO_N[13]	
AF25	RPDI_P[14]	RSDI_P3	AL7	TPDO_P[14]	TSCO_P3
AG25	RPDI_N[14]	RSDI_N3	AK7	TPDO_N[14]	TSCO_N3
AK26	RPDI_P[15]	RSCI_P3	AK6	TPDO_P[15]	
AL26	RPDI_N[15]	RSCI_N3	AJ6	TPDO_N[15]	
AH19	RPCI_P		AG18	TPCI_P	TCCI_P
AJ19	RPCI_N		AF18	TPCI_N	TCCI_N
AF19	RFPI_P		AH18	TFPI_P	
AG19	RFPI_N		AJ18	TFPI_N	
AK20	RPRTY_P		AG17	TPCO_P	
AL20	RPRTY_N		AF17	TPCO_N	
			AK17	TFPO_P	
			AK16	TFPO_N	
			AH16	TPRTY_P	
			AG16	TPRTY_N	

Table 6. I/O Pin Equivalence on the Receive TTL Line Side Interface (Sheet 1 of 2)

Pin #	Rx TTL Parallel Single	Rx TTL Parallel Quad	Rx TTL Serial Quad	Rx UTOPIA Single 64-Bit	Rx UTOPIA Quad 16-Bit
W26	RPDI[0]	RPDI_0[0]	RSDI_0	RXDATA[32]	RXDATA_2[0]
W27	RPDI[1]	RPDI_0[1]		RXDATA[33]	RXDATA_2[1]
AA30	RPDI[2]	RPDI_0[2]		RXDATA[34]	RXDATA_2[2]
AA31	RPDI[3]	RPDI_0[3]		RXDATA[35]	RXDATA_2[3]
Y29	RPDI[4]	RPDI_0[4]		RXDATA[36]	RXDATA_2[4]
AB31	RPDI[5]	RPDI_0[5]		RXDATA[37]	RXDATA_2[5]
Y28	RPDI[6]	RPDI_0[6]		RXDATA[38]	RXDATA_2[6]
AA29	RPDI[7]	RPDI_0[7]		RXDATA[39]	RXDATA_2[7]
AA26	RPDI[8]	RPDI_1[0]	RSDI_1	RXDATA[40]	RXDATA_2[8]
AD31	RPDI[9]	RPDI_1[1]		RXDATA[41]	RXDATA_2[9]
AC30	RPDI[10]	RPDI_1[2]		RXDATA[42]	RXDATA_2[10]
AC29	RPDI[11]	RPDI_1[3]		RXDATA[43]	RXDATA_2[11]
AD30	RPDI[12]	RPDI_1[4]		RXDATA[44]	RXDATA_2[12]
AB28	RPDI[13]	RPDI_1[5]		RXDATA[45]	RXDATA_2[13]
AD29	RPDI[14]	RPDI_1[6]		RXDATA[46]	RXDATA_2[14]
AB27	RPDI[15]	RPDI_1[7]		RXDATA[47]	RXDATA_2[15]
AC26	RPDI[16]	RPDI_2[0]	RSDI_2	RXDATA[48]	RXDATA_3[0]
AC27	RPDI[17]	RPDI_2[1]		RXDATA[49]	RXDATA_3[1]
AF31	RPDI[18]	RPDI_2[2]		RXDATA[50]	RXDATA_3[2]
AF30	RPDI[19]	RPDI_2[3]		RXDATA[51]	RXDATA_3[3]
AF29	RPDI[20]	RPDI_2[4]		RXDATA[52]	RXDATA_3[4]
AE28	RPDI[21]	RPDI_2[5]		RXDATA[53]	RXDATA_3[5]
AD27	RPDI[22]	RPDI_2[6]		RXDATA[54]	RXDATA_3[6]
AG31	RPDI[23]	RPDI_2[7]		RXDATA[55]	RXDATA_3[7]
AE26	RPDI[24]	RPDI_3[0]	RSDI_3	RXDATA[56]	RXDATA_3[8]
AH29	RPDI[25]	RPDI_3[1]		RXDATA[57]	RXDATA_3[9]
AJ31	RPDI[26]	RPDI_3[2]		RXDATA[58]	RXDATA_3[10]
AG28	RPDI[27]	RPDI_3[3]		RXDATA[59]	RXDATA_3[11]
AJ30	RPDI[28]	RPDI_3[4]		RXDATA[60]	RXDATA_3[12]
AF27	RPDI[29]	RPDI_3[5]		RXDATA[61]	RXDATA_3[13]
AJ29	RPDI[30]	RPDI_3[6]		RXDATA[62]	RXDATA_3[14]
AH28	RPDI[31]	RPDI_3[7]		RXDATA[63]	RXDATA_3[15]
Y26	RPCI	RPCI_0	RSCI_0		
AC31	RPCO	RPCO_0	RSCO_0		
Y27	RLOCK	RLOCK_0	RLOCK_0		

Table 6. I/O Pin Equivalence on the Receive TTL Line Side Interface (Sheet 2 of 2)

Pin #	Rx TTL Parallel Single	Rx TTL Parallel Quad	Rx TTL Serial Quad	Rx UTOPIA Single 64-Bit	Rx UTOPIA Quad 16-Bit
AA27	ROOF	ROOF_0	ROOF_0		
AB30	RFPI	RFPI_0			
AB26		RPCI_1	RSCI_1		
AC28		RPCO_1	RSCO_1		
AE31		RLOCK_1	RLOCK_1		
AE29		ROOF_1	ROOF_1		
AE30		RFPI_1			
AG30		RPCI_2	RSCI_2		
AE27		RPCO_2	RSCO_2		
AH31		RLOCK_2	RLOCK_2		
AG29		ROOF_2	ROOF_2		
AD26		RFPI_2			
AF26		RPCI_3	RSCI_3		
AH27		RPCO_3	RSCO_3		
AJ28		RLOCK_3	RLOCK_3		
AJ27		ROOF_3	ROOF_3		
AG27		RFPI_3			

Table 7. I/O Pin Equivalence on the Transmit TTL Line Side Interface

Pin #	Tx TTL Parallel Single	Tx TTL Parallel Quad	Tx TTL Serial Quad	Tx UTOPIA Single 64-Bit	Tx UTOPIA Quad 16-Bit
AF6	TPDO[0]	TPDO_0[0]	TSDO_0	TXDATA[32]	TXDATA_2[0]
AJ4	TPDO[1]	TPDO_0[1]		TXDATA[33]	TXDATA_2[1]
AH4	TPDO[2]	TPDO_0[2]		TXDATA[34]	TXDATA_2[2]
AG5	TPDO[3]	TPDO_0[3]		TXDATA[35]	TXDATA_2[3]
AE6	TPDO[4]	TPDO_0[4]		TXDATA[36]	TXDATA_2[4]
AJ2	TPDO[5]	TPDO_0[5]		TXDATA[37]	TXDATA_2[5]
AF5	TPDO[6]	TPDO_0[6]		TXDATA[38]	TXDATA_2[6]
AJ1	TPDO[7]	TPDO_0[7]		TXDATA[39]	TXDATA_2[7]
AE5	TPDO[8]	TPDO_1[0]	TSDO_1	TXDATA[40]	TXDATA_2[8]
AF4	TPDO[9]	TPDO_1[1]		TXDATA[41]	TXDATA_2[9]
AG3	TPDO[10]	TPDO_1[2]		TXDATA[42]	TXDATA_2[10]
AH1	TPDO[11]	TPDO_1[3]		TXDATA[43]	TXDATA_2[11]
AF3	TPDO[12]	TPDO_1[4]		TXDATA[44]	TXDATA_2[12]
AG2	TPDO[13]	TPDO_1[5]		TXDATA[45]	TXDATA_2[13]
AE4	TPDO[14]	TPDO_1[6]		TXDATA[46]	TXDATA_2[14]
AD5	TPDO[15]	TPDO_1[7]		TXDATA[47]	TXDATA_2[15]
AB6	TPDO[16]	TPDO_2[0]	TSDO_2	TXDATA[48]	TXDATA_3[0]
AC5	TPDO[17]	TPDO_2[1]		TXDATA[49]	TXDATA_3[1]
AB5	TPDO[18]	TPDO_2[2]		TXDATA[50]	TXDATA_3[2]
AD4	TPDO[19]	TPDO_2[3]		TXDATA[51]	TXDATA_3[3]
AC4	TPDO[20]	TPDO_2[4]		TXDATA[52]	TXDATA_3[4]
AF1	TPDO[21]	TPDO_2[5]		TXDATA[53]	TXDATA_3[5]
AE2	TPDO[22]	TPDO_2[6]		TXDATA[54]	TXDATA_3[6]
AE1	TPDO[23]	TPDO_2[7]		TXDATA[55]	TXDATA_3[7]
Y6	TPDO[24]	TPDO_3[0]	TSDO_3	TXDATA[56]	TXDATA_3[8]
AB4	TPDO[25]	TPDO_3[1]		TXDATA[57]	TXDATA_3[9]
AC2	TPDO[26]	TPDO_3[2]		TXDATA[58]	TXDATA_3[10]
AD1	TPDO[27]	TPDO_3[3]		TXDATA[59]	TXDATA_3[11]
Y5	TPDO[28]	TPDO_3[4]		TXDATA[60]	TXDATA_3[12]
AB3	TPDO[29]	TPDO_3[5]		TXDATA[61]	TXDATA_3[13]
AC1	TPDO[30]	TPDO_3[6]		TXDATA[62]	TXDATA_3[14]
W6	TPDO[31]	TPDO_3[7]		TXDATA[63]	TXDATA_3[15]
AD6	TPCI	TPCI_0	TSCI_0		
AH3	TPCO	TPCO_0	TSCO_0		
AG6	TFPI	TFPI			
AH5	TFPO	TFPO			
AG1		TPCI_1	TSCI_1		
AF2		TPCO_1	TSCO_1		
AA5		TPCI_2	TSCI_2		
AC3		TPCO_2	TSCO_2		
AB1		TPCI_3	TSCI_3		
AB2		TPCO_3	TSCO_3		

Table 8. TTL I/O Pin Equivalence on the Receive OH/Alarm Extraction Ports (Sheet 1 of 2)

Pin #	OH Extraction Logical Interface #1	OH Extraction Logical Interface #2	OH Extraction Logical Interface #3	Rx UTOPIA Single 64-bit	Rx UTOPIA Quad 16-bit
H29	RSOH_0	RSOH_0	RRD_0	RSOH_0	RSOH_0
J29	RSOHFR	RSOHFR_0	RMD_0	RSOHFR_0	RSOHFR_0
K28	RSOHCK	RSOHCK_0	RRDC_0	RSOHCK_0	RSOHCK_0
E28	RSAL	RSAL_0	RMDC_0	RXDATA[48]	RXDATA_3[0]
E30	RSALFR	RSALFR_0	RROW_0	RXDATA[52]	RXDATA_3[4]
H27	RSALCK	RSALCK_0	RMOW_0	RXDATA[56]	RXDATA_3[8]
E26	RPOH_0	RPOH_0	RDOW_0	RXDATA[36]	RXDATA_2[4]
F26	RPOHFR_0	RPOHFR_0	ROWBYC_0	RXDATA[40]	RXDATA_2[8]
C30	RPOHCK_0	RPOHCK_0	ROWC_0	RXDATA[44]	RXDATA_2[12]
D26	RPAL_0	RPAL_0	RPOW1	RXDATA[32]	RXDATA_2[0]
K26	RSOH_1	RSOH_1	RRD_1	RSOH_1	RSOH_1
H30	RRD	RSOHFR_1	RMD_1	RSOHFR_1	RSOHFR_1
L26	RRDC	RSOHCK_1	RRDC_1	RSOHCK_1	RSOHCK_1
F27	RMD	RSAL_1	RMDC_1	RXDATA[49]	RXDATA_3[1]
H26	RMDC	RSALFR_1	RROW_1	RXDATA[53]	RXDATA_3[5]
F29		RSALCK_1	RMOW_1	RXDATA[57]	RXDATA_3[9]
A29	RPOH_1	RPOH_1	RDOW_1	RXDATA[37]	RXDATA_2[5]
E27	RPOHFR_1	RPOHFR_1	ROWBYC_1	RXDATA[41]	RXDATA_2[9]
C31	RPOHCK_1	RPOHCK_1	ROWC_1	RXDATA[45]	RXDATA_2[13]
A28	RPAL_1	RPAL_1	RPOW2	RXDATA[33]	RXDATA_2[1]
J28	RSOH_2	RSOH_2	RRD_2	RSOH_2	RSOH_2
H31	ROWBYC	RSOHFR_2	RMD_2	RSOHFR_2	RSOHFR_2
J30	ROWC	RSOHCK_2	RRDC_2	RSOHCK_2	RSOHCK_2
G27	RROW	RSAL_2	RMDC_2	RXDATA[50]	RXDATA_3[2]
E31	RMOW	RSALFR_2	RROW_2	RXDATA[54]	RXDATA_3[6]
J26	RDOW	RSALCK_2	RMOW_2	RXDATA[58]	RXDATA_3[10]
B28	RPOH_2	RPOH_2	RDOW_2	RXDATA[38]	RXDATA_2[6]
C28	RPOHFR_2	RPOHFR_2	ROWBYC_2	RXDATA[42]	RXDATA_2[10]
D28	RPOHCK_2	RPOHCK_2	ROWC_2	RXDATA[46]	RXDATA_2[14]
C27	RPAL_2	RPAL_2	RPOWBYC	RXDATA[34]	RXDATA_2[2]
G31	RSOH_3	RSOH_3	RRD_3	RSOH_3	RSOH_3
K27	RPOWBYC	RSOHFR_3	RMD_3	RSOHFR_3	RSOHFR_3
J31	RPOWC	RSOHCK_3	RRDC_3	RSOHCK_3	RSOHCK_3
E29	RPOW1	RSAL_3	RMDC_3	RXDATA[51]	RXDATA_3[3]
F28	RPOW2	RSALFR_3	RROW_3	RXDATA[55]	RXDATA_3[7]
G28		RSALCK_3	RMOW_3	RXDATA[59]	RXDATA_3[11]
D27	RPOH_3	RPOH_3	RDOW_3	RXDATA[39]	RXDATA_2[7]
C29	RPOHFR_3	RPOHFR_3	ROWBYC_3	RXDATA[43]	RXDATA_2[11]
D29	RPOHCK_3	RPOHCK_3	ROWC_3	RXDATA[47]	RXDATA_2[15]
F24	RPAL_3	RPAL_3	RPOWC	RXDATA[35]	RXDATA_2[3]
F31				RXDATA[60]	RXDATA_3[12]

Table 8. TTL I/O Pin Equivalence on the Receive OH/Alarm Extraction Ports (Sheet 2 of 2)

Pin #	OH Extraction Logical Interface #1	OH Extraction Logical Interface #2	OH Extraction Logical Interface #3	Rx UTOPIA Single 64-bit	Rx UTOPIA Quad 16-bit
F30				RXDATA[61]	RXDATA_3[13]
H28				RXDATA[62]	RXDATA_3[14]
J27				RXDATA[63]	RXDATA_3[15]

Table 9. TTL I/O Pin Equivalence on the Transmit OH/Alarm Insertion Ports (Sheet 1 of 2)

Pin #	OH Insertion Logical Interface #1	OH Insertion Logical Interface #2	OH Insertion Logical Interface #3	Tx UTOPIA Single 64-Bit	Tx UTOPIA Quad 16-Bit
W2	TSOHINS_0	TSOHINS_0	TRD_0	TSOHINS_0	TSOHINS_0
W3	TSOH_0	TSOH_0	TMD_0	TSOH_0	TSOH_0
Y3	TSOHFR	TSOHFR_0	TRDC_0	TSOHFR_0	TSOHFR_0
AA3	TSOHCK	TSOHCK_0	TMDC_0	TSOHCK_0	TSOHCK_0
R3	TSAL	TSAL_0	TROW_0	TXDATA[40]	TXDATA_2[8]
T4	TSALFR	TSALFR_0	TPOWBYC	TXDATA[36]	TXDATA_2[4]
V3	TSALCK	TSALCK_0	TOWBYC_0	TXDATA[32]	TXDATA_2[0]
M3	TPOHINS_0	TPOHINS_0	TPOW1	TXDATA[56]	TXDATA_3[8]
N3	TPOH_0	TPOH_0	TPOW2	TXDATA[52]	TXDATA_3[4]
N1	TPOHFR_0	TPOHFR_0	TOWC_0	TXDATA[48]	TXDATA_3[0]
P1	TPOHCK_0	TPOHCK_0	TMOW_0	TXDATA[44]	TXDATA_2[12]
L2	TPAL_0	TPAL_0	TDOW_0	TXDATA[60]	TXDATA_3[12]
U6	TSOHINS_1	TSOHINS_1	TRD_1	TSOHINS_1	TSOHINS_1
Y2	TSOH_1	TSOH_1	TMD_1	TSOH_1	TSOH_1
V6	TMDC	TSOHFR_1	TRDC_1	TSOHFR_1	TSOHFR_1
Y4	TRDC	TSOHCK_1	TMDC_1	TSOHCK_1	TSOHCK_1
R4	TMD	TSAL_1	TROW_1	TXDATA[41]	TXDATA_2[9]
U2	TRD	TSALFR_1	TPOWC	TXDATA[37]	TXDATA_2[5]
U3		TSALCK_1	TOWBYC_1	TXDATA[33]	TXDATA_2[1]
M4	TPOHINS_1	TPOHINS_1		TXDATA[57]	TXDATA_3[9]
N5	TPOH_1	TPOH_1		TXDATA[53]	TXDATA_3[5]
P5	TPOHFR_1	TPOHFR_1	TOWC_1	TXDATA[49]	TXDATA_3[1]
P2	TPOHCK_1	TPOHCK_1	TMOW_1	TXDATA[45]	TXDATA_2[13]
M5	TPAL_1	TPAL_1	TDOW_1	TXDATA[61]	TXDATA_3[13]
V4	TSOHINS_2	TSOHINS_2	TRD_2	TSOHINS_2	TSOHINS_2
V5	TSOH_2	TSOH_2	TMD_2	TSOH_2	TSOH_2
W4	TOWBYC	TSOHFR_2	TRDC_2	TSOHFR_2	TSOHFR_2
W5	TOWC	TSOHCK_2	TMDC_2	TSOHCK_2	TSOHCK_2
R6	TROW	TSAL_2	TROW_2	TXDATA[42]	TXDATA_2[10]
U1	TMOW	TSALFR_2		TXDATA[38]	TXDATA_2[6]
T6	TDOW	TSALCK_2	TOWBYC_2	TXDATA[34]	TXDATA_2[2]
N6	TPOHINS_2	TPOHINS_2		TXDATA[58]	TXDATA_3[10]
M1	TPOH_2	TPOH_2		TXDATA[54]	TXDATA_3[6]
P6	TPOHFR_2	TPOHFR_2	TOWC_2	TXDATA[50]	TXDATA_3[2]
P3	TPOHCK_2	TPOHCK_2	TMOW_2	TXDATA[46]	TXDATA_2[14]

Table 9. TTL I/O Pin Equivalence on the Transmit OH/Alarm Insertion Ports (Sheet 2 of 2)

Pin #	OH Insertion Logical Interface #1	OH Insertion Logical Interface #2	OH Insertion Logical Interface #3	Tx UTOPIA Single 64-Bit	Tx UTOPIA Quad 16-Bit
L3	TPAL_2	TPAL_2	TDOW_2	TXDATA[62]	TXDATA_3[14]
W1	TSOHINS_3	TSOHINS_3	TRD_3	TSOHINS_3	TSOHINS_3
Y1	TSOH_3	TSOH_3	TMD_3	TSOH_3	TSOH_3
AA1	TPOWBYC	TSOHFR_3	TRDC_3	TSOHFR_3	TSOHFR_3
AA2	TPOWC	TSOHCK_3	TMDC_3	TSOHCK_3	TSOHCK_3
R5	TPOW1	TSAL_3	TROW_3	TXDATA[43]	TXDATA_2[11]
T3	TPOW2	TSALFR_3		TXDATA[39]	TXDATA_2[7]
T5		TSALCK_3	TOWBYC_3	TXDATA[35]	TXDATA_2[3]
K1	TPOHINS_3	TPOHINS_3		TXDATA[59]	TXDATA_3[11]
L1	TPOH_3	TPOH_3		TXDATA[55]	TXDATA_3[7]
N2	TPOHFR_3	TPOHFR_3	TOWC_3	TXDATA[51]	TXDATA_3[3]
P4	TPOHCK_3	TPOHCK_3	TMOW_3	TXDATA[47]	TXDATA_2[15]
J1	TPAL_3	TPAL_3	TDOW_3	TXDATA[63]	TXDATA_3[15]

Table 10. TTL I/O Pin Equivalence on the Receive UTOPIA Interface (Sheet 1 of 2)

Pin #	Rx UTOPIA Single	Rx UTOPIA Quad 8-Bit	Rx UTOPIA Quad 16-Bit
D13	RXDATA[0]	RXDATA_0[0]	RXDATA_0[0]
B13	RXDATA[1]	RXDATA_0[1]	RXDATA_0[1]
A12	RXDATA[2]	RXDATA_0[2]	RXDATA_0[2]
A14	RXDATA[3]	RXDATA_0[3]	RXDATA_0[3]
A13	RXDATA[4]	RXDATA_0[4]	RXDATA_0[4]
D14	RXDATA[5]	RXDATA_0[5]	RXDATA_0[5]
F14	RXDATA[6]	RXDATA_0[6]	RXDATA_0[6]
B14	RXDATA[7]	RXDATA_0[7]	RXDATA_0[7]
D16	RXDATA[8]	RXDATA_1[0]	RXDATA_0[8]
B18	RXDATA[9]	RXDATA_1[1]	RXDATA_0[9]
B17	RXDATA[10]	RXDATA_1[2]	RXDATA_0[10]
D17	RXDATA[11]	RXDATA_1[3]	RXDATA_0[11]
A18	RXDATA[12]	RXDATA_1[4]	RXDATA_0[12]
A19	RXDATA[13]	RXDATA_1[5]	RXDATA_0[13]
F16	RXDATA[14]	RXDATA_1[6]	RXDATA_0[14]
A20	RXDATA[15]	RXDATA_1[7]	RXDATA_0[15]
F20	RXDATA[16]	RXDATA_2[0]	RXDATA_1[0]
B23	RXDATA[17]	RXDATA_2[1]	RXDATA_1[1]
B24	RXDATA[18]	RXDATA_2[2]	RXDATA_1[2]
C22	RXDATA[19]	RXDATA_2[3]	RXDATA_1[3]
E21	RXDATA[20]	RXDATA_2[4]	RXDATA_1[4]
D21	RXDATA[21]	RXDATA_2[5]	RXDATA_1[5]
C23	RXDATA[22]	RXDATA_2[6]	RXDATA_1[6]
D22	RXDATA[23]	RXDATA_2[7]	RXDATA_1[7]
A27	RXDATA[24]	RXDATA_3[0]	RXDATA_1[8]
C25	RXDATA[25]	RXDATA_3[1]	RXDATA_1[9]
B26	RXDATA[26]	RXDATA_3[2]	RXDATA_1[10]
E23	RXDATA[27]	RXDATA_3[3]	RXDATA_1[11]
C26	RXDATA[28]	RXDATA_3[4]	RXDATA_1[12]
D25	RXDATA[29]	RXDATA_3[5]	RXDATA_1[13]
B27	RXDATA[30]	RXDATA_3[6]	RXDATA_1[14]
F23	RXDATA[31]	RXDATA_3[7]	RXDATA_1[15]
C18	RXADDR[0]		
B19	RXADDR[1]		
C19	RXADDR[2]		
B20	RXADDR[3]		
A21	RXADDR[4]		
B10	RXPADL[0]		RXPADL[0]
F12	RXPADL[1]		RXPADL[1]
E12	RXPADL[2]		RXPADL[2]
A10			RXPADL[3]
B9	RXPFA		

Table 10. TTL I/O Pin Equivalence on the Receive UTOPIA Interface (Sheet 2 of 2)

Pin #	Rx UTOPIA Single	Rx UTOPIA Quad 8-Bit	Rx UTOPIA Quad 16-Bit
E17	RXCLK	RXCLK_0	RXCLK_0
E19	RXENB	RXENB_0	RXENB_0
B11	RXSOF	RXSOF_0	RXSOF_0
C12	RXEOF	RXEOF_0	RXEOF_0
D12	RXPRTY	RXPRTY_0	RXPRTY_0
E13	RXERR	RXERR_0	RXERR_0
B12	RXFA_0	RXFA_0	RXFA_0
F13	RXVAL	RXVAL_0	RXVAL_0
F17		RXCLK_1	RXCLK_1
D19		RXENB_1	RXENB_1
C14		RXSOF_1	RXSOF_1
D15		RXEOF_1	RXEOF_1
C15		RXPRTY_1	RXPRTY_1
C16		RXERR_1	RXERR_1
A17	RXFA_1	RXFA_1	RXFA_1
E15		RXVAL_1	RXVAL_1
E18		RXCLK_2	RXCLK_2
F19		RXENB_2	RXENB_2
A22		RXSOF_2	RXSOF_2
B21		RXEOF_2	RXEOF_2
B22		RXPRTY_2	RXPRTY_2
C21		RXERR_2	RXERR_2
E20	RXFA_2	RXFA_2	RXFA_2
A23		RXVAL_2	RXVAL_2
F18		RXCLK_3	RXCLK_3
C20		RXENB_3	RXENB_3
B25		RXSOF_3	RXSOF_3
A25		RXEOF_3	RXEOF_3
D23		RXPRTY_3	RXPRTY_3
C24		RXERR_3	RXERR_3
A26	RXFA_3	RXFA_3	RXFA_3
D24		RXVAL_3	RXVAL_3

Table 11. TTL I/O Pin Equivalence on the Transmit UTOPIA Interface (Sheet 1 of 2)

Pin #	Tx UTOPIA Single	Tx UTOPIA Quad 8-Bit	Tx UTOPIA Quad 16-Bit
K3	TXDATA[0]	TXDATA_0[0]	TXDATA_0[0]
J3	TXDATA[1]	TXDATA_0[1]	TXDATA_0[1]
L5	TXDATA[2]	TXDATA_0[2]	TXDATA_0[2]
G1	TXDATA[3]	TXDATA_0[3]	TXDATA_0[3]
L6	TXDATA[4]	TXDATA_0[4]	TXDATA_0[4]
J4	TXDATA[5]	TXDATA_0[5]	TXDATA_0[5]
H2	TXDATA[6]	TXDATA_0[6]	TXDATA_0[6]
K6	TXDATA[7]	TXDATA_0[7]	TXDATA_0[7]
G3	TXDATA[8]	TXDATA_1[0]	TXDATA_0[8]
H5	TXDATA[9]	TXDATA_1[1]	TXDATA_0[9]
F3	TXDATA[10]	TXDATA_1[2]	TXDATA_0[10]
J6	TXDATA[11]	TXDATA_1[3]	TXDATA_0[11]
E1	TXDATA[12]	TXDATA_1[4]	TXDATA_0[12]
G4	TXDATA[13]	TXDATA_1[5]	TXDATA_0[13]
F4	TXDATA[14]	TXDATA_1[6]	TXDATA_0[14]
E2	TXDATA[15]	TXDATA_1[7]	TXDATA_0[15]
D3	TXDATA[16]	TXDATA_2[0]	TXDATA_1[0]
D2	TXDATA[17]	TXDATA_2[1]	TXDATA_1[1]
F5	TXDATA[18]	TXDATA_2[2]	TXDATA_1[2]
E4	TXDATA[19]	TXDATA_2[3]	TXDATA_1[3]
D4	TXDATA[20]	TXDATA_2[4]	TXDATA_1[4]
G6	TXDATA[21]	TXDATA_2[5]	TXDATA_1[5]
C1	TXDATA[22]	TXDATA_2[6]	TXDATA_1[6]
E5	TXDATA[23]	TXDATA_2[7]	TXDATA_1[7]
E7	TXDATA[24]	TXDATA_3[0]	TXDATA_1[8]
B3	TXDATA[25]	TXDATA_3[1]	TXDATA_1[9]
A4	TXDATA[26]	TXDATA_3[2]	TXDATA_1[10]
A3	TXDATA[27]	TXDATA_3[3]	TXDATA_1[11]
D7	TXDATA[28]	TXDATA_3[4]	TXDATA_1[12]
F7	TXDATA[29]	TXDATA_3[5]	TXDATA_1[13]
F8	TXDATA[30]	TXDATA_3[6]	TXDATA_1[14]
B4	TXDATA[31]	TXDATA_3[7]	TXDATA_1[15]
A8	TXADDR[0]		
C9	TXADDR[1]		
D10	TXADDR[2]		
A9	TXADDR[3]		

Table 11. TTL I/O Pin Equivalence on the Transmit UTOPIA Interface (Sheet 2 of 2)

Pin #	Tx UTOPIA Single	Tx UTOPIA Quad 8-Bit	Tx UTOPIA Quad 16-Bit
D11	TXADDR[4]		
A7	TXPADL[0]		TXPADL[0]
C7	TXPADL[1]		TXPADL[1]
C8	TXPADL[2]		TXPADL[2]
B7			TXPADL[3]
B6	TXPFA		
C5	TXSFA		
F10	TXCLK	TXCLK_0	TXCLK_0
D9	TXENB	TXENB_0	TXENB_0
M6	TXSOF	TXSOF_0	TXSOF_0
H1	TXEOF	TXEOF_0	TXEOF_0
J2	TXPRTY	TXPRTY_0	TXPRTY_0
K4	TXERR	TXERR_0	TXERR_0
D8	TXFA_0	TXFA_0	TXFA_0
E10		TXCLK_1	TXCLK_1
F9		TXENB_1	TXENB_1
K5		TXSOF_1	TXSOF_1
G2		TXEOF_1	TXEOF_1
H4		TXPRTY_1	TXPRTY_1
J5		TXERR_1	TXERR_1
A5	TXFA_1	TXFA_1	TXFA_1
F11		TXCLK_2	TXCLK_2
B8		TXENB_2	TXENB_2
H6		TXSOF_2	TXSOF_2
G5		TXEOF_2	TXEOF_2
D1		TXPRTY_2	TXPRTY_2
E3		TXERR_2	TXERR_2
A6	TXFA_2	TXFA_2	TXFA_2
E11		TXCLK_3	TXCLK_3
E9		TXENB_3	TXENB_3
C2		TXSOF_3	TXSOF_3
F6		TXEOF_3	TXEOF_3
E6		TXPRTY_3	TXPRTY_3
C4		TXERR_3	TXERR_3
E8	TXFA_3	TXFA_3	TXFA_3

2.0 Main Features

2.1 General

- Intel IXF6048 maps/demaps both ATM cells or byte-synchronous HDLC frames (packet over SONET mode) over SONET/SDH.
- The device processes the following SONET/SDH frame formats:
  - Single STS-48c/STM-16c
  - Single STS-48/STM-16
  - Single STS-12/STM-4
  - Single STS-3
  - Quad STS-12c/STM-4c
  - Quad STS-3c/STM-1
  - Quad STS-1/STM-0
- Each channel can be configured fully independently.
- Two different system interfaces:
  - ATM-UTOPIA Level 3/2/1
  - POS-UTOPIA Level 3/2/1
- 16-bit Intel or Motorola* microprocessor interface.

2.1.1 SONET/SDH Receiver Block

- Programmable in repeater or demultiplexer mode.
- Byte alignment (serial or parallel interface), frame acquisition, descrambling, and Section Overhead extraction of one STS-48c/48/12/3 or four STS-12c/3c/1 data streams. Byte alignment and/or descrambling may be disabled via microprocessor configuration.
- Received payload pointer (H1, H2 bytes) interpreter, path overhead extraction, and payload bytes demultiplexing.
- Loss Of Signal (LOS), Out Of Frame (OOF), Loss Of Frame (LOF), Regenerator Section Trace Identifier Mismatch (RS-TIM), Excessive Error Defect (EED: fully programmable BER alarm), Degraded Signal Defect (DSD: fully programmable BER alarm), Multiplexer Section Alarm Indication Signal (MS-AIS), Multiplexer Section Remote Defect Indication (MS-RDI), Loss Of Pointer (LOP), Loss Of Pointer Concatenation indication (LOPC), Administrative Unit alarm indication signal (AU-AIS), Path Unequipped (UNEQ), Path Signal Label Mismatch (SLM), path alarm indication Signal (VC-AIS), Path Trace Identifier Mismatch (HP-TIM), Path Remote Defect Identification (enhanced or not HP-RDI) alarms detection on an incoming STS/STM stream.
- Signal Fail (SF) and Signal Degrade (SD) alarm automatic generation.
- Automatic or via microprocessor insertion of Alarm Identification Signal at the different layers (regenerator, multiplexer, adaptation, and path).

- K1, K2 (APS), S1 (synchronization message status), and C2 (path Signal Label) received bytes filtering; parallel access (via microprocessor) and serial access (via Receive Section serial Alarm bus: RSAL output).
- Full J0 and J1 (Trace Identifiers) processing programmable as a 1-, 16- (with CRC-7), or 64-byte trace. Programmable expected J0 and J1 traces, and parallel access to the received accepted J0 and J1 traces.
- Programmable Expected Signal label (C2 byte).
- BIP/Block error detection and count for: B1 (regeneration section BIP-8), B2 (multiplexer section BIP-8/24/96/392), and B3 (path layer BIP-8). Demultiplexing and BIP/Block error count of the received Multiplexer Section Remote Error Indication (MS-REI in M1 byte), and received Path layer Remote Error Indication (HP-REI in G1 byte). Pointer justification events count (positive and negative).
- The Data Communication Channels (D1-D3, D4 to D12), the Section Orderwires (E1 and E2), and the user channel (F1) are all demultiplexed and then output either on the dedicated serial ports (at 192 Kbit/s 576 Kbit/s) or on the Receive Section serial OverHead bus (RSOH).
- The Section Orderwires (E1 and E2) and user channel (F1) are both demultiplexed and then extracted either on the dedicated serial ports (at 64 Kbit/s) or on the Receive Section serial OverHead bus (RSOH).
- The Path Orderwires (F2 and F3) are demultiplexed and extracted either on the dedicated serial ports (at 64 Kbit/s) or on the Receive Path serial OverHead bus (RPOH).
- Serial access to all receive section overhead bytes via either a 1.728 Mbit/s bus (OC-1), a 5.184 Mbit/s bus (OC-3c), a 20.736 Mbit/s bus (OC-12c), or 4 × 20.736 Mbit/s busses (OC-48): (RSOH).
- Serial access to all the receive path overhead bytes via a 576-Kbit/s bus: (RPOH).
- Serial access to all the receive section and path alarms, generated remote indications, and error count, output on two 576-Kbit/s buses (RSAL and RPAL).

2.1.2 SONET/SDH Transmitter Block

- Programmable in repeater or demultiplexer mode.
- Insertion of microprocessor programmable 1-, 16- (with CRC-7), or 64-byte Trace Identifier (J1 byte) and Signal Label (C2 byte).
- Insertion of path Remote Defect and Error Identification (HP-RDI—enhanced or not—and HP-REI in G1 byte) either via automatic feedback from the receive, via the Transmit Path serial input Alarm port (TPAL), or via the microprocessor.
- Path BIP-8 (B3 byte) calculation and insertion.
- Serial access and insertion of any POH bit via the Transmit Path OverHead bus input (TPOH).
- Microprocessor fully programmable transmit pointer value insertion (H1, H2).
- Insertion of section Remote Defect and Error Identification (MS-RDI—enhanced or not—and MS-REI in both K2 and M1 bytes) either via automatic feedback from the receive, via the Transmit Section serial input Alarm port (TSAL), or via the microprocessor.
- Insertion of APS bytes (K1, K2) and synchronization byte (S1) either from the serial insertion port or from micro-processor programming.

- Insertion of DCC channels (D1-D3, D4 to D12) and orderwire channels (E1, E2, F1) either from the dedicated serial ports (at 192-, 576- and 64-Kbit/s) or from the Transmit Section serial OverHead bus (TSOH).
- Calculation (after scrambling) and insertion of multiplexer section BIP-8/24/96/392 (B2 bytes) and regenerator section BIP-8 (B1).
- Serial access and insertion of any other SOH byte via the Transmit Section OverHead bus input (TSOH).
- Data scrambling and multiplexing of the first RSOH row: Microprocessor programmable 1-, 16- (with CRC-7), or 64-byte section Trace Identifier (J0 byte) insertion, microprocessor configurable Z0 bytes insertion, and framing bytes (A1, A2) insertion.
- Microprocessor programmable Path unequipped generation. Microprocessor programmable AIS insertion at the different layers (path, adaptation, section).
- Microprocessor configurable option to pass through each received RSOH byte in repeater mode.
- The DCC channels may be provided via dedicated serial accesses at 192-Kbit/s (D1-D3) and 576-Kbit/s (D4 to D12). The section orderwires and user channels may be provided via 3 dedicated 64-Kbit/s serial ports (E1, E2, and F1). The path orderwires may be provided via 2 dedicated 64-Kbit/s serial ports (F2 and F3).
- Transmitter diagnostic and test features: Microprocessor interface allows pointer movements, NDF generation, B1, B2, B3, BIP inversion, A1 framing bytes inversion, and scrambler disabling of B1, B2, BIP, or A1.

2.1.3 Receive ATM Cell Processor Block

- Demaps ATM cells from the received STS-48c/STM-16c/STS-48/STM-16/STS-12c/STM-4c/STS-12/STM-4/STS-3c/STM-1/STS-1 signal.
- HEC-based cell delineation and filtering using HUNT state, PRESYNCH state, SYNC state, and the LCD defect.
- Correction and Detection modes within SYNC state.
- Single- and multiple-bit error detection.
- Single-bit error correction if correction is enabled.
- Cell payload self-synchronous descrambling.
- Programmable filter for Idle/Unassigned cell detection and discarding.
- Write control of four, independent, 32-cell deep, cell-rate decoupling, FIFO memories (Single non-concatenated transceiver and Quad transceiver modes).
- Write control of one, 256-cell deep, cell-rate decoupling, FIFO memory (Single concatenated mode).
- GFC bits monitored to determine the remote device configuration (controller device, controlled device, or no GFC functions implemented). GFC halt bit monitored when configured as a controlled device.
- The number of cells that have been written into the receive FIFO (cells passing the configured cell filter) are counted in a 24-bit counter.
- The number of cells matching the Idle/Unassigned programmable filter are counted in an 24-bit counter.

- The number of cells containing a correctable error in the header are counted in a 16-bit counter.
- The number of cells containing an uncorrectable error in the header are counted in a 16-bit counter.
- The number of accepted cells that have been lost due to a FIFO overflow are counted in a 16-bit counter.

2.1.4 Transmit ATM Cell Processor Block

- Maps ATM cells into the transmitted STS-48c/STM-16c/STS-48/STM-16/STS-12c/STM-4c/STS-12/STM-4/STS-3c/STM-1/STS-1 signal.
- Read control of four, independent, 32-cell deep, cell-rate decoupling, FIFO memories (Single non-concatenated transceiver and Quad transceiver modes).
- Read control of one, 256-cell deep, cell-rate decoupling, FIFO memory (Single concatenated mode)
- HEC generation/insertion.
- Cell payload self-synchronous scrambling.
- Idle cell insertion (cell rate decoupling process).
- GFC cyclic halt function when configured as a controller device.
- Unassigned cell insertion when configured as a controlled device.
- The number of ATM cells that have been read from the transmit FIFO (assigned or unassigned ATM Layer cells) are counted in a 24-bit counter.
- The number of idle cells generated and mapped into the transmitted SONET/SDH frames are counted in a 24-bit counter. It only counts the idle cells inserted by the cell rate decoupling process, not the idle/unassigned cells inserted by the Generic Flow Control function.

2.1.5 Receive Byte-Synchronous HDLC Controller (Receive POS Block)

- Demaps byte-synchronous HDLC frames cells from the received STS-48c/STM-16c/STS-48/STM-16/STS-12c/STM-4c/STS-12/STM-4/STS-3c/STM-1/STS-1 signal.
- SPE self-synchronous descrambling before frame demapping.
- FLAG-based HDLC frame delineation.
- Control Escape stuffing removal (byte destuffing).
- FCS-16/32 verification.
- Optional HDLC Address and Control fields checking/dropping.
- Programmable minimum and maximum packet lengths. Optional packet discarding based on packet length.
- Write control of four, independent, 2K-byte deep, packet-rate decoupling, FIFO memories (Single non-concatenated transceiver and Quad transceiver modes).
- Write control of one, 16K-byte deep, packet-rate decoupling, FIFO memory (Single concatenated transceiver mode).

- The number of received frames written into the receive FIFO and not marked as errored (“good frames”) are counted in a 24-bit counter.
- The number of bytes received and written into the receive FIFO are counted in an 32-bit counter. Intel IXF6048 can be configured to count all the bytes written into the FIFO (good frames + frames marked as errored) or only the bytes received within good frames.
- A 16-bit counter tallies the number of received aborted frames (finishing with an Abort sequence).
- A 16-bit counter tallies the number of received frames with an incorrect FCS field.
- A 16-bit counter tallies the number of received frames that have been partially lost due to a FIFO overrun.
- Two 16-bit counters tally the number of frames received and written into the receive FIFO that have packet lengths which are smaller/longer than the programmed minimum/maximum packet length.

2.1.6 Transmit Byte-Synchronous HDLC Controller (Transmit POS Block)

- Maps byte-synchronous HDLC frames into the transmitted STS-48c/STM-16c/STS-48/STM-16/STS-12c/STM-4c/STS-12/STM-4/STS-3c/STM-1/STS-1 signal.
- Read control of four, independent, 2K-byte deep, packet-rate decoupling, FIFO memories (Single non-concatenated transceiver and Quad transceiver modes).
- Read control of one, 16K-byte deep, packet-rate decoupling, FIFO memory (Single concatenated mode).
- HDLC frame generation.
- HDLC Address and Control fields can be generated or read from the FIFO (part of the packet).
- FCS-16/32 generation.
- Control Escape stuffing insertion (byte stuffing).
- Two different transmit flow control methods (using interframe FLAG character insertion).
- SPE self-synchronous scrambling, after frame mapping.
- The number of packets read from the transmit FIFO and transmitted into HDLC frames are counted in a 24-bit counter (only the non aborted frames).
- The number of bytes read from the transmit FIFO and transmitted into the generated HDLC frames are counted in an 32-bit counter (all the bytes or only the not-aborted frames).
- The number of HDLC frames that have been aborted by the user are counted in a 16-bit counter.
- The number of HDLC frames that have been aborted by the HDLC controller, due to a transmit FIFO underflow, are counted in a 16-bit counter.

2.1.7 ATM-UTOPIA Interface

- Supports all different versions of the ATM-Forum UTOPIA interface:
  - — UTOPIA Level 3 with 64-bit data bus
  - — UTOPIA Level 3 with 32-bit data bus

  - — UTOPIA Level 3 with four independent 16-bit data buses
  - — UTOPIA Level 3 with four independent 8-bit data buses
  - — UTOPIA Level 2 with 16-bit data bus
  - — UTOPIA Level 2 with 8-bit data bus
  - — UTOPIA Level 1 (four independent interfaces)
- Implements cell-based handshaking.
- Operates at up to 104 MHz in the following configurations:
  - — Single 32-bit data bus
  - — Single 16-bit data bus
  - — Single 8-bit data bus
  - — Quad 8-bit data bus
- Operates at up to 52 MHz in the following configurations:
  - — Single 64-bit data bus
  - — Quad 16-bit data bus
- Four, 32-cell deep, cell-rate decoupling, FIFO memories (single non-concatenated transceiver and quad transceiver modes) or one, 256-cell deep, cell-rate decoupling, FIFO memory (single concatenated transceiver mode).
- Eight different ATM cell data structures (independent configuration in reception and transmission):
  - — 64-bit × 7-word
  - — 32-bit × 13-word
  - — 32-bit × 14-word
  - — 16-bit × 26-word
  - — 16-bit × 27-word
  - — 8-bit × 52-word
  - — 8-bit × 53-word
- Configurable “decode-response” delay of one or two clock cycles (independent configuration in reception and transmission). Configuration is independent of bus-data width and ATM cell-data structure which allows the implementation of any standard or nonstandard mode.
- Configurable as a Single device (no tristated outputs) or a multiple device (tristate outputs when not selected/addressed).
- Supports operation with one receive-cell-available and one transmit-cell-available signal (polling).
- The deassertion of the receive- and transmit-cell-available status outputs can be configured at any byte position of the cell.
- Also supports Direct Status Indication and Multiplexed Status Polling modes.
- Fully independent configuration per physical port.
- Fully independent configuration in the receive and transmit directions.

2.1.8 POS-UTOPIA Interface

- POS-UTOPIA interface, based on the ATM industry standard UTOPIA and supporting the transfer of variable length packets:
  - POS-UTOPIA Level 3 with 64-bit data bus
  - POS-UTOPIA Level 3 with 32-bit data bus
  - POS-UTOPIA Level 3 with four independent 16-bit data buses
  - POS-UTOPIA Level 3 with four independent 8-bit data buses
  - POS-UTOPIA Level 2 with 16-bit data bus
  - POS-UTOPIA Level 2 with 8-bit data bus
  - POS-UTOPIA Level 1 (four independent interfaces)
- Operates at up to 104 MHz in the following configurations:
  - Single 32-bit data bus
  - Single 16-bit data bus
  - Single 8-bit data bus
  - Quad 8-bit data bus
- Operates at up to 52 MHz in the following configurations:
  - Single 64-bit data bus
  - Quad 16-bit data bus
- Four, 2K-byte deep, packet-rate decoupling, FIFO memories (single non-concatenated transceiver and quad transceiver modes) or one, 16K-byte deep, packet-rate decoupling, FIFO memory (single concatenated transceiver mode)
- Three different packet formats are transferred to/from the Link Layer device:
  - HDLC frame “Information” field (PPP frame)
  - HDLC frame “Address + Control + Information” fields
  - HDLC frame “Information + FCS” fields
- Receive and transmit FIFO status indications controlled by means of programmable watermarks.
- Configurable “decode-response” delay of one or two clock cycles (independent configuration in reception and transmission). Configuration is independent of bus-data width.
- Configurable as a Single device (no tristated outputs) or a multiple device (tristate outputs when not selected/addressed).
- Supports two different Port Selection methods:
  - An ATM-UTOPIA-like method, with port-selection and data-transfer cycles.
  - A memory mapped interface method. In this mode, there is no port-selection cycle and the interface is only active when the enable signal (TXENB or RXENB) is active.
- Fully independent configuration per physical port.
- Fully independent configuration in the receive and transmit directions.

3.0 Line Side Interface

Intel IXF6048's Line Side Interface uses differential PECL I/O running at up to 155.52 MHz and TTL I/O running at up to 77.76 MHz. The line side interface can be configured in the following modes:

- Single OC-48c or single OC-48 (2488 Mbit/s):
  - 16-bit differential PECL parallel interface at 155.52 MHz
  - 32-bit TTL parallel interface at 77.76 MHz
- Single OC-12 (622 Mbit/s):
  - 8-bit TTL parallel interface at 77.76 MHz
- Single OC-3 (155 Mbit/s):
  - 1-bit differential PECL serial interface at 155.52 MHz
  - 8-bit TTL parallel interface at 19.44 MHz
- Quad OC-12c (4 × 622 Mbit/s):
  - Four independent 8-bit TTL parallel interfaces at 77.76 MHz
- Quad OC-3c (4 × 155 Mbit/s):
  - Four independent 1-bit differential PECL serial interfaces at 155.52 MHz
  - Four independent 8-bit TTL parallel interfaces at 19.44 MHz
- Quad OC-1 (4 × 51 Mbit/s):
  - Four independent 1-bit differential PECL serial interfaces at 51.84 MHz
  - Four independent 1-bit TTL serial interfaces at 51.84 MHz
  - Four independent 8-bit TTL parallel interfaces at 6.48 MHz

The Line Side Interface can be configured totally independently in the receive and transmit directions. However, in order to use the Line Loopback mode or to clock a transmit channel with the corresponding receive channel timing reference, it is necessary to configure the receive and transmit line side interfaces in the same mode. These are the main configuration features of Intel IXF6048 line side interface:

- Configuration bit QMode (register GOCNF) controls the configuration of the line side interface I/O as a single parallel interface or as four independent serial interfaces.
- When configured as a Single transceiver (QMode = '0'), configuration bits RcvIFMode[2:0] (register R_COCNF) and XmtIFMode[2:0] (register T_COCNF) configure the receive and transmit line side interfaces as a 16-bit PECL interface, an 8-bit PECL interface, a 1-bit PECL interface, a 32-bit TTL interface, a 8-bit TTL interface, or a 1-bit TTL interface (independently for each direction).
- When configured as a Quad transceiver (QMode = '1'), configuration bits RcvIFMode[2:0] (register R_COCNF) and XmtIFMode[2:0] (register T_COCNF) configure each receive and transmit line side interface as a 1-bit PECL interface, an 8-bit TTL interface, or a 1-bit TTL interface (independently for each direction and on each channel).

The different interfaces do not require external frame acquisition circuitry, i.e., the input data bus is not required to carry byte-aligned SONET/SDH data. Intel IXF6048 performs internal (on-chip) frame acquisition and word rotation.

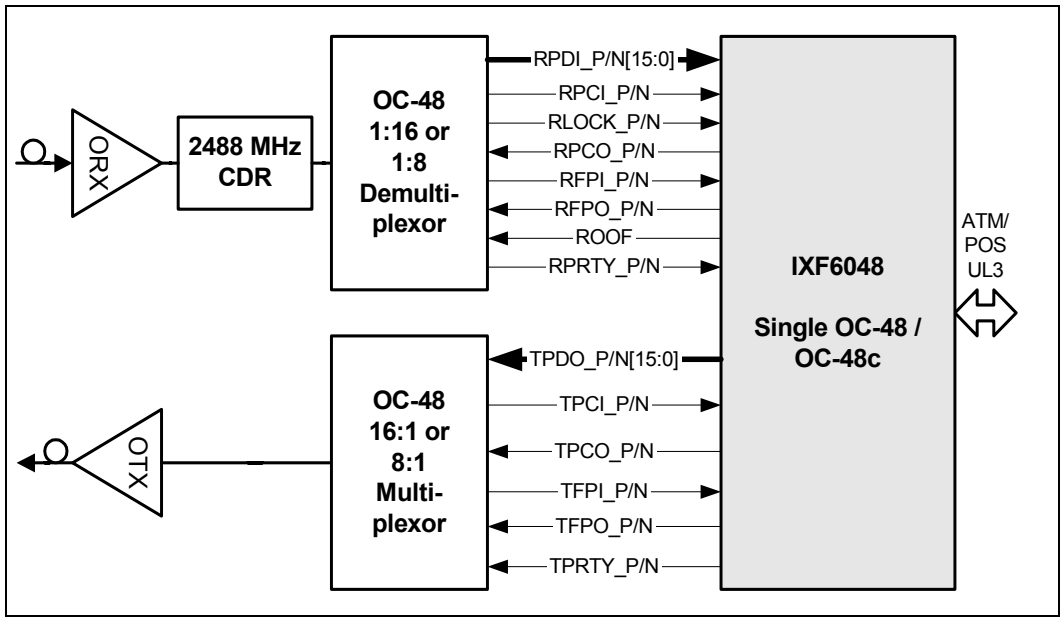
3.1 Differential PECL Single Parallel Line Side Interface

When configured as a Single 2,488 Mbit/s transceiver (Single STS-48c/STS-48), the Intel IXF6048 line side interface I/O can be configured as a 16-bit differential PECL single parallel-data interface.

Figure 3 shows an example of an Intel IXF6048 connected to a 2488 Mbit/s Mux/Demux PECL chipset. Optionally, Intel IXF6048 can be controlled by an external frame acquisition block by using the input RFPI_P/N (receive frame position input). The parallel transmit interface can also be controlled by an external 8-KHz system reference by using the input TFPI_P/N. That allows the use of four Intel IXF6048 devices to build an OC-48/OC-192 Multiplexer/Demultiplexer.

Odd/even parity bits (TPRTY_P/N and RPRTY_P/N) protect the data buses (TPDO_P/N[15:0] and RPDI_P/N[15:0]) and optionally the frame pulses (TFPO_P/N and RFPI_P/N).

Figure 3. 2488 Mbit/s Line Side Interface Example



3.2 Differential PECL Quad Serial Line Side Interface (155/51 Mbit/s)

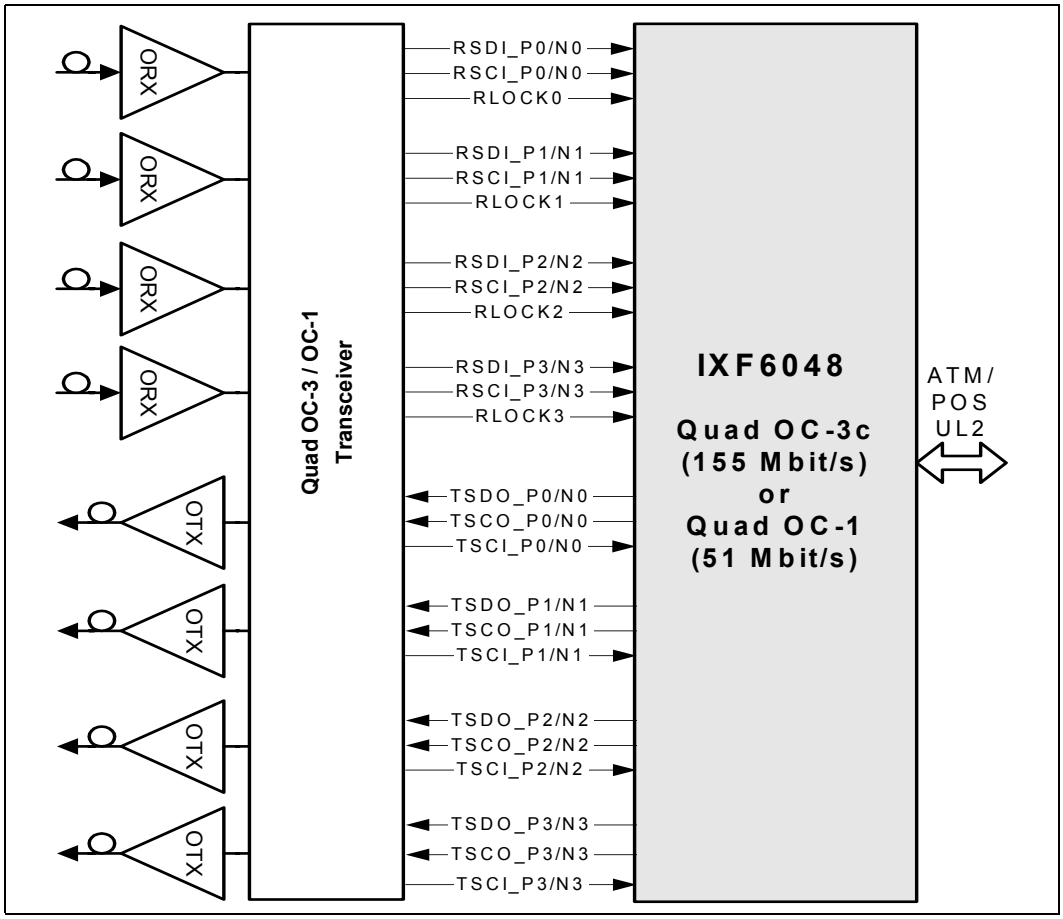
When configured as a Quad 155/51 Mbit/s transceiver (Quad STS-3c/STS-1), the Intel IXF6048 line side interface I/O can be configured as four independent differential PECL serial-data interfaces.

Each receive interface provides the serial data and clock inputs, a tristatable output timing reference, a Lock detect input, and an OOF output alarm.

The four independent transmit serial clock inputs (TSCI_P0/N0, TSCI_P1/N1, TSCI_P2/N2, and TSCI_P3/N3) allow the independent configuration of each channel rate. Optionally, a common clock input (TCCI_P/N) allows using a single timing clock reference to the four channels. Figure 4 shows a configuration example for quad 155 Mbit/s or 51 Mbit/s. Each transmit channel has been configured to use an independent input timing reference (TSCI_Pi/Ni, i = 0, 1, 2, 3).

The serial line side interface can also be used when Intel IXF6048 is configured as a single STS-3 (non concatenated) processor. In this configuration, only one serial line side interface (channel 0) is active.

Figure 4. Quad 155/51 Mbit/s Line Side Interface Example



3.3 TTL Single Parallel Line Side Interface

When Intel IXF6048 is configured as a Single 2,488 Mbit/s transceiver (STS-48c/STM-16c/STS-48/STS-48c), the line side interface I/O can be configured as a TTL single parallel-data interface: RPDI[31:0] and TPDO[31:0].

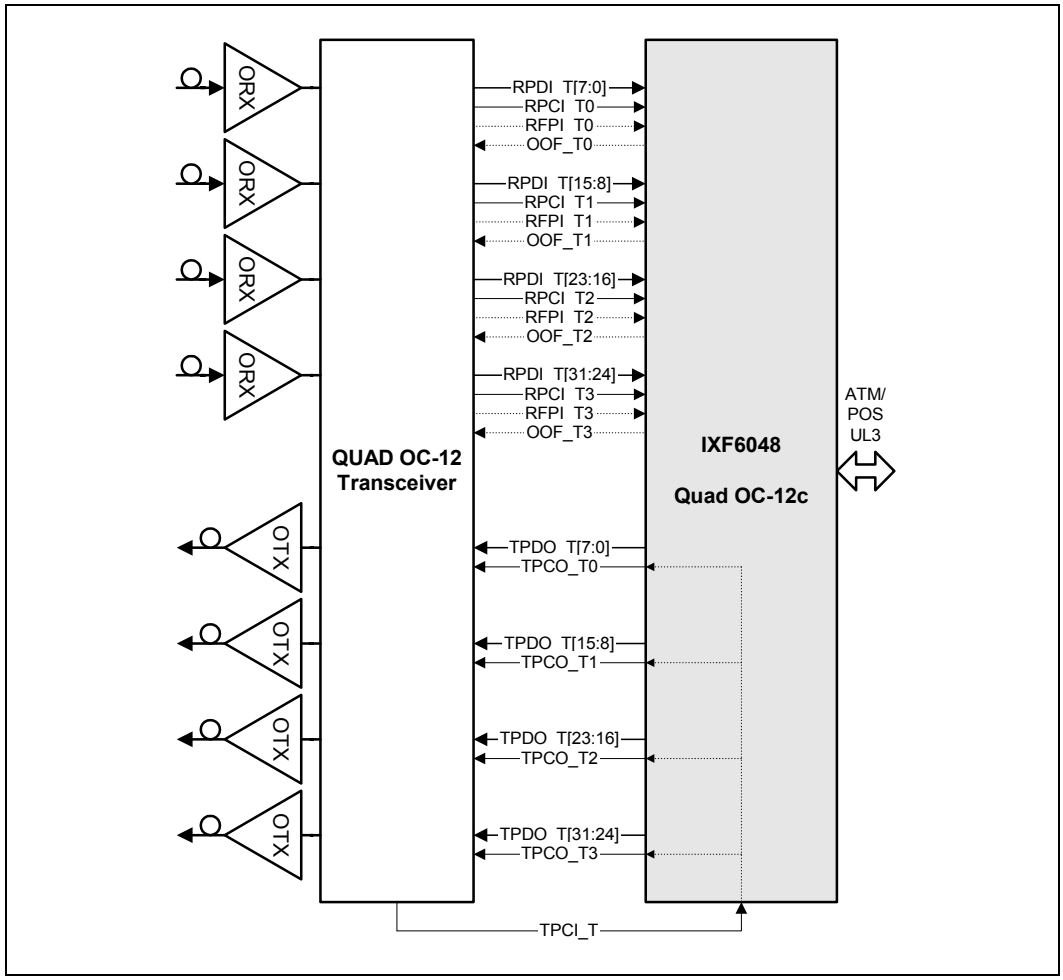
The interface data-width can be configured independently for each direction (reception and transmission). The TTL single parallel receive interface does not require external frame acquisition circuitry, i.e., the input data bus RPDI[31:0] are not required to carry byte-aligned SONET/SDH data; Intel IXF6048 performs internal (on-chip) frame acquisition and word rotation. Optionally,

Intel IXF6048 can be controlled by an external frame acquisition block by using the input RFPI (receive frame position input). The parallel transmit interface can also be controlled by an external 8-KHz system reference by using the input TFPI.

3.4 TTL Quad Parallel Line Side Interface

When Intel IXF6048 is configured as a Quad 622/155/51 Mbit/s transceiver (Quad STS-12c/STS-3c/STS-1), the line side interface I/O can be configured as four independent TTL single parallel-data interfaces: RPDI_i[7:0] and TPDO_i[7:0] (i = 0, 1, 2, 3). Each TTL parallel receive interface does not require external frame acquisition circuitry, i.e., the input on each data bus RPDI_i[7:0] (i = 0, 1, 2, 3) is not required to carry byte-aligned SONET/SDH data; Intel IXF6048 performs internal (on-chip) frame acquisition and word rotation on each data stream. Optionally, each Intel IXF6048 receive interface can be controlled by an external frame acquisition block by using the input RFPI_i (receive frame position input). Each parallel transmit interface can also be controlled by an external 8-KHz system reference by using the input TFPI_i (i = 0, 1, 2, 3).

Figure 5. Quad OC-12c Example: Four Independent 8-Bit Parallel TTL Interfaces



The TTL 8-bit parallel line side interface can also be used when Intel IXF6048 is configured as a single STS-12 (non concatenated) processor. In this configuration, only one TTL parallel line side interface (channel 0) is active.

3.5 TTL Quad Serial Line Side Interface

When configured as a Quad 51 Mbit/s transceiver (Quad STS-1), the Intel IXF6048 line side interface I/O can be configured as four independent TTL serial-data interfaces. Each receive interface provides the serial data and clock inputs, a tristatable output timing reference, a Lock detect input, and an OOF output alarm.

4.0 SONET/SDH Framer Block Functional Description

4.1 Modes of Operation

4.1.1 Frame Format Configuration

4.1.1.1 Concatenated Frames

The Intel IXF6048 implements all the different concatenated framing formats dedicated to cell/packet mapping over SONET/SDH, from 51.84 Mb/s up to a 2.5 Gb/s data rate.

In the cases of 51.84 Mb/s (STS-1/STM-0), 155 Mb/s (STS-3c/STM-1), and 622.08 Mb/s (STS-12c/STM-4c), Intel IXF6048 integrates up to four fully independent framer processors (four channels) in a single device. Each processor can have a framing format configuration different from the other three.

When working at 2.5 Gb/s (STS-48c/STM-16c), Intel IXF6048 is configured as a single OC-48 processor. In this configuration, just one framer processor is enabled (channel 0), the other three channels being completely disabled.

4.1.1.2 Non-Concatenated Frames

The four internal processors configured with the same framing format may be synchronized together with the same clock and rate, so that the chip is able to generate and to demultiplex a higher order rate, based on a non-concatenated frame transporting of up to four independent payloads.

The Intel IXF6048 can thus fully process a non-concatenated STM-4 (622.08 Mb/s) with four independent pointers.

When working at 2.5 Gb/s (OC-48), Intel IXF6048 can multiplex four STM-4c signals into a 2.5 Gb/s aggregate, and can demultiplex four STM-4c signals from a single 2.5 Gb/s aggregate. The OC-48 signal integrates four STS-12c/STM-4c equivalent signals (i.e., four VC-4-4c) with independent pointers. In other words, a single non-concatenated OC-3 (STS-3/STM-1) is three concatenated OC-1s (STS-1/STM-0); a single non-concatenated OC-12 (STS-12/STM-4) is four concatenated OC-3cs (STS-3c/STM-1); and a single non-concatenated OC-48 (STS-48/STM-12) is four concatenated OC-12cs (STS-12c/STM-4c).

4.1.2 Operational Configuration

The SONET/SDH block can be programmed in two different master configuration:

- Repeater mode
- Multiplexer mode

4.1.2.1 Repeater Mode Configuration

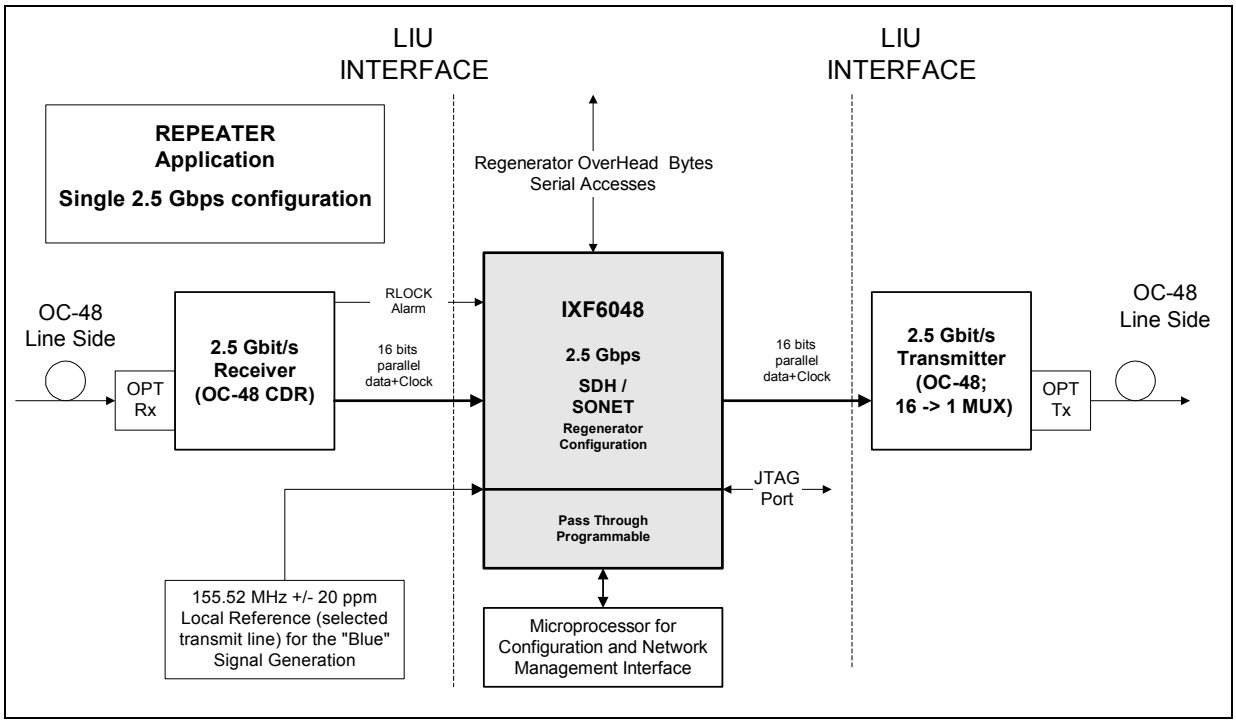
All MSOH, HPOH, and VC data are passed through internally and no off-chip connection is required between the transmit and receive sides. The transmit source of the RSOH bytes is configurable via a microprocessor register. Figure 6 is an example of an OC-48 repeater. The timing is recovered by the high-speed line interface unit and passed to the transmit side via the Intel IXF6048. In the event of a receiver failure (i.e., a LOS of Signal Alarm), the Intel IXF6048 switches to the selected transmit line (Blue) clock signal reference (if so configured—TPCI/TCCI/TSCI) using the corresponding microprocessor register.

Note: The Intel IXF6048 must be configured in concatenated mode to enable repeater mode. The traffic passing through the device can be either concatenated or non-concatenated, since only the Section Layer is processed.

4.1.2.2 Multiplexer Mode Configuration

In this mode of operation, receiver and transmitter operate independently. On the transmit side, the SONET/SDH block provides clock and timing (container data enable) to the ATM/POS mapper block. The data coming from the ATM/POS block are multiplexed together with the inserted HPOH, AU pointers, MSOH, and RSOH data. The OC-1/3/12/48 frame is then output towards the line. On the receive side, the data coming from the high-speed line interface unit is framed, descrambled, and the extracted payload container is output towards the cell/packet demapping block.

Figure 6. OC-48 Repeater Application



4.2 Transmit Data Flow

Figure 1 shows the functional blocks of the SONET/SDH Block for the 4 channels. For each transmitter (lower half of Figure 1), the input interface is the bus coming from the ATM/POS mapping block, with 32-bit (OC-12/48) or byte (OC-1/3) wide data MDATAi[31:0] and timing signal for the payload active signal CENi.

The data flow starts with the Transmit Higher order Path termination Processor (THPP block) which adds the concatenated VC(s) path overhead:

- The 1-, 16-, or 64-byte J1 string is sourced from the microprocessor programmable registers (Path Trace Buffer) or TPOH serial input. The microprocessor must calculate the CRC-7 byte of the 16-byte J1 transmit string and store it in the first byte of the registers storing the string.
- The B3 byte is calculated internally and inserted. The microprocessor can invert the values of B3 for system testing purposes.
- The C2 byte is sourced from the microprocessor programmable register or TPOH serial input.
- The G1 byte is sourced from the microprocessor programmable register, TPOH serial input, the Transmit Path Alarm serial bus input (TPAL), or from the receive portion of the chip if automatic RDI and REI insertion is enabled by the microprocessor.
- The F2 and F3/Z3 bytes are two optional 64-Kbit/s channels that can be sourced from dedicated serial accessor from the serial bus TPOH. They may also be internally set to their default value of either all ‘1’s or all ‘0’s. In the case of a dedicated serial ports, a 64-KHz reference clock is supplied at TPOWC and an 8-KHz sync pulse at TPOWBYC.

- The other HPOH bytes (H4, K3/Z4, N1/Z5) are normally unused. Their value is set to the default (all '0's) or sourced from the TPOH serial input.

After the HPOH data has been added, the Higher Order Connection Supervision block can insert an unequipped payload if configured by the microprocessor to do so.

Pointer generation is performed by the Multiplexer Section Adaptation (MSA) block of the Transmit Multiplex Section Processor (TMSP). The pointer value is sourced from the microprocessor programmable register, and is fixed by default. Positive and negative pointer movement, as well as NDF events, may be generated via the microprocessor interface. The resulting parallel data stream is supplied to the Multiplexer Section Termination (MST) block of the Transmit Multiplex Section Processor (TMSP).

Next, the MST function adds the Multiplexer Section Overhead (MSOH):

- The K1 and K2 APS bytes are sourced from a microprocessor programmable register, the Transmit Section Alarm serial bus input (TSAL), or the TSOH serial input. In the particular case of K2, an internal process inserts the MS-RDI bits (K2[2:0]) based on the receive information (if automatic MS-RDI insertion is enabled by the microprocessor) or sources the MS-RDI defect from either the TSAL serial bus input or from a microprocessor programmable register.
- The D4-D12 bytes (DCC channel) are sourced from the TMD dedicated serial input or TSOH serial bus input. In the case of a dedicated serial port, a 576-KHz reference clock is supplied as TMDC.
- S1 is sourced from the microprocessor programmable register or TSOH serial bus input.
- M1 is sourced from the TSOH input, the Transmit Section Alarm serial bus input (TSAL), or an internal process that sets M1 based on the receive B2 byte(s) errors from the receive portion of the Intel IXF6048 if automatic MS-REI insertion is enabled.
- E2 may be sourced from the TMOW dedicated serial port, if so configured, or the TSOH serial input. In the case of a dedicated serial port, a 64-KHz reference clock is supplied at TOWC and an 8-KHz sync pulse at TOWBYC.
- The B2 bytes are calculated internally and inserted. The microprocessor can invert the values of B2 for system testing purposes.
- The other MSOH bytes are normally unused. Their value can be internally set to the default (all '0's) or sourced from the TSOH serial bus input.

Finally, the Regenerator Section Overhead (RSOH) is added by the Transmit Regenerator Section termination Processor (TRSP).

- A1 and A2 framing bytes are inserted. The microprocessor can invert the values of A1 for system testing purposes.
- J0 byte is sourced from the microprocessor (Section Trace Buffer), TSOH input, or received J0 byte. It can be either a 1-, 16-, or 64-byte trace message. For a 16-byte trace, the microprocessor must calculate the CRC-7 byte of the J0 transmit string and store it in the first byte of the registers storing the string.
- The D1-D3 bytes (DCC channel) are sourced from the dedicated TRD serial input or the TSOH serial bus input. In the case of a dedicated serial port, a 192-KHz reference clock is supplied as TRDC. In repeater mode, this byte can also be passed through unchanged.
- E1 may be sourced from the TROW dedicated serial input, if configured as such, or the TSOH serial bus input. In the case of a dedicated serial port, a 64-KHz reference clock is supplied at

TOWC and an 8-KHz sync pulse at TOWBYC. In repeater mode, this byte can also be passed through unchanged.

- F1 may be sourced from the TDOW dedicated serial input, if so configured, or the TSOH serial bus input. In the case of a dedicated serial port, a 64-KHz reference clock is supplied at TOWC and an 8-KHz sync pulse at TOWBYC. In repeater mode, this byte can also be passed through unchanged.
- Z0/NU (1st row) bytes may be set to all '0's, all '1's, xAAH, or a previous STS-1 ID definition. They may also be sourced from the TSOH input. In repeater mode, these byte can also be passed through, unchanged.
- The B1 byte is calculated internally (after scrambling) and inserted (before scrambling). The microprocessor can invert the values of B1 for system testing purposes.
- The other RSOH bytes are unused. They can be passed through unchanged in repeater mode, their value can be set to the default (all '0's), or they can be sourced from the TSOH input.

Finally, the data is scrambled and then framing bytes A1/A2, section trace byte J0, and Z0 bytes, are added.

For OC-1/3, each data stream is then either serialized and output on the TSDO_P/Ni pin synchronous with the TSCO_P/Ni clock or output on the byte parallel bus TPDO_i[7:0]. For OC-12, the data stream is output on the byte parallel output bus TPDO_i[7:0] with the TPCO_i clock. For OC-48 application, data is output on the 8/16-bit parallel bus TPDO_P/N[15:0] with the TPCO_P/N clock or on the 32-bit parallel bus TPDO[31:0].

4.3 Receive Data Flow

OC-1/3 data is input on the RSDI_P/Ni pin or RPDI_i[7:0]. The serial clock input is RSCI_P/Ni, and the parallel clock is RPCI_i.

OC-12 data is input on the parallel 8-bit RPDI_i[7:0] input bus (parallel interface). OC-48 data is input either on the parallel 8/16-bit RPDI_P/N[15:0] or the parallel 32-bit RPDI[31:0] input bus.

First, the interface block detects Loss Of Signal alarm condition based on data transition or all '0's in the incoming stream.

The input data is then fed to the framing and descrambling block (Receive Frame Acquisition block). The framing block synchronizes the timing generator to the incoming data and provides Out Of Frame and Loss Of Frame alarm signals. These alarms are based on frame counts that are programmed via the microprocessor interface, as the ITU specifications are unclear at this time.

After frame synchronization and descrambling, the Receive Regenerator Section termination Processor (RRSP) extracts the RSOH:

- The expected value of the J0 string is stored via the microprocessor interface (Section Trace Buffer). The received J0 string is checked for stability, compared with the stored version, and in the case of a 16-byte trace message, used to calculate a CRC-7 byte. Three alarms can be generated: a J0 (Trace ID) Unstable alarm, a J0 Mismatch alarm, and J0 CRC-7 Error alarm. The accepted receive J0 trace is accessible and can be read by the microprocessor interface. Receive J0 byte is also provided at RSOH output.
- B1 byte is calculated internally and compared to the incoming B1 value. The errors are stored into a set of counters that can be read by the microprocessor interface, and provided serially at RSAL Section Alarm bus output pin.

- E1 is provided serially either at the RROW dedicated output or at the serial output bus RSOH.
- F1 is provided serially at the RDOW dedicated output or at the RSOH output bus. In the case of a dedicated serial ports, E1 and F1 are synchronous and can be accessed using the 64-KHz clock provided at RROWC and the 8-KHz synchronization pulse provided at ROWBYC.
- D1-D3 (DCC) are provided serially at the dedicated RRD output or at the RSOH output bus. In the case of a dedicated serial port, the 192-KHz clock reference for this output is provided at RRDC.
- The other RSOH bytes are normally unused, and their value is provided serially at RSOH bus output.

Next, the Multiplexer Section Termination (MST) function of the Receive Multiplexer Section Processor (RMSP block) extracts the MSOH:

- K1 and K2 bytes are provided via a microprocessor register. A filter based on 3 consecutive identical values of K1 and K2 gates the update of the microprocessor registers. Those filtered values are serially accessible at the Receive section Alarm port RSAL output. The received value of K1 and K2 are also provided at the RSOH serial bus output. The detected K2-MS-RDI alarm is accessible to the microprocessor via a maskable interrupt and provided serially at RSAL output.
- D4-D12 (DCC) are provided serially at the RMD dedicated output or at the RSOH output. In the case of a dedicated serial access, the 576-KHz clock reference for this output is provided at RMDC.
- S1 filtered value is provided via a microprocessor register, and at the Receive Section Alarm port RSAL serial output. A filter based on 3 consecutive identical values of S1 gates the update of the microprocessor register. S1 received byte is also provided serially at RSOH.
- M1 is provided serially at the RSOH output and updates MST REI counters accessible by the microprocessor. The received MST REI is also provided serially at RSAL output.
- E2 is provided serially at the dedicated RMOW output or at the RSOH output bus. In the case of a dedicated serial output, the 64-KHz clock reference for this output is provided at ROWC and the 8-KHz sync pulse at ROWBYC.
- B2 byte is calculated internally and compared to the incoming B2 value. The errors are stored into a set of counters that can be read by the microprocessor interface. These errors are also inserted in the transmitted M1 byte if enabled (see register T_RMST_OP). Excessive Error Defect (EED) and Degraded Signal Defect (DSD) fully configurable and independent BER alarms thresholds are internally detected. Both detected encoded errors (generated MS REI) and consecutive alarms are serially accessible at the Receive Section Alarm bus output (RSAL).
- The other MSOH bytes are normally unused, and their value is provided serially at RSOH output.

The MSA function of the Receive Multiplexer Section Processor (RMSP block) is to interpret the H1-H3 payload point bytes to determine the location of the concatenated VC-3s or VC-4s payload structure. Positive and negative pointer movement events are stored in counters that can be accessed via the microprocessor interface. The data from the MSA section is then output to the HPT section.

The Receive Higher order Path Processor (RHPP) extracts the HPOH:

- The expected value of the 1-, 16-, or 64-byte J1 string is stored internally via the microprocessor interface (Path Trace Buffer). The received J1 string is checked for stability, compared with the stored version, and in the case of a 16-byte trace message, used to calculate

a CRC-7 byte. Three alarms can be generated: a J1 Unstable, a J1 Mismatch, and J1 CRC-7 mismatch. In addition, to differentiate between “supervisory” and “non supervisory” unequipped, an automatic detection of an all '0' (of the first received J1 byte), stable, received J1 trace is processed on chip, providing both interrupt and status bit to the microprocessor. The accepted receive J1 trace is accessible and can be read by the microprocessor interface. The received J1 read is provided serially at RSOH output.

Note: For automatic detection of all ‘0’, only the first byte of a J1 trace is checked. In the case of 16 and 64-byte modes, if the first byte is all zeros and the following bytes are other than zero, an all-zero alarm is triggered after three to five frames (depending on the configuration). Software can be used to distinguish between the J1 traces.

- B3 byte is calculated internally and compared to the incoming B3 value. The errors are stored into a set of counters that can be read by the microprocessor interface. These errors are also inserted in the transmitted G1 REI bits (G1[7:4]) if enabled, and serially output at the Receive Path Alarm bus pin (RPAL) as a generated HP-REI code.
- The C2 byte is monitored for changes or a mismatch from the expected value programmed in a register. Defects are indicated as either Signal Label Mismatch, AIS, or Unequipped alarms, depending on the value. The filtered value of C2 can also be read from a register and is provided at the Receive Path Alarm serial bus output (RPAL). C2 receive byte is also provided serially at RPOH output. The number of filtering frames can be programmed by the microprocessor.
- G1 is provided serially at the RPOH output and is used to update HPTREI-CNT registers accessible by the microprocessor. The received HPT REI is also provided serially at RPAL output.
- F2 and F3 are provided serially at the RPOW1 and RPOW2 dedicated outputs or at the RPOH output bus. In the case of dedicated serial ports, F2 and F3 are synchronous and can be accessed using the 64-KHz clock provided at RROWC and the 8-KHz synchronization pulse provided at ROWBYC.
- The other POH bytes are normally unused, and their value is provided serially at RPOH output.

The output of each SONET/SDH block is then sent to the ATM/POS demapping block with the receive clock and container data enable.

4.3.1 Reference Clocks

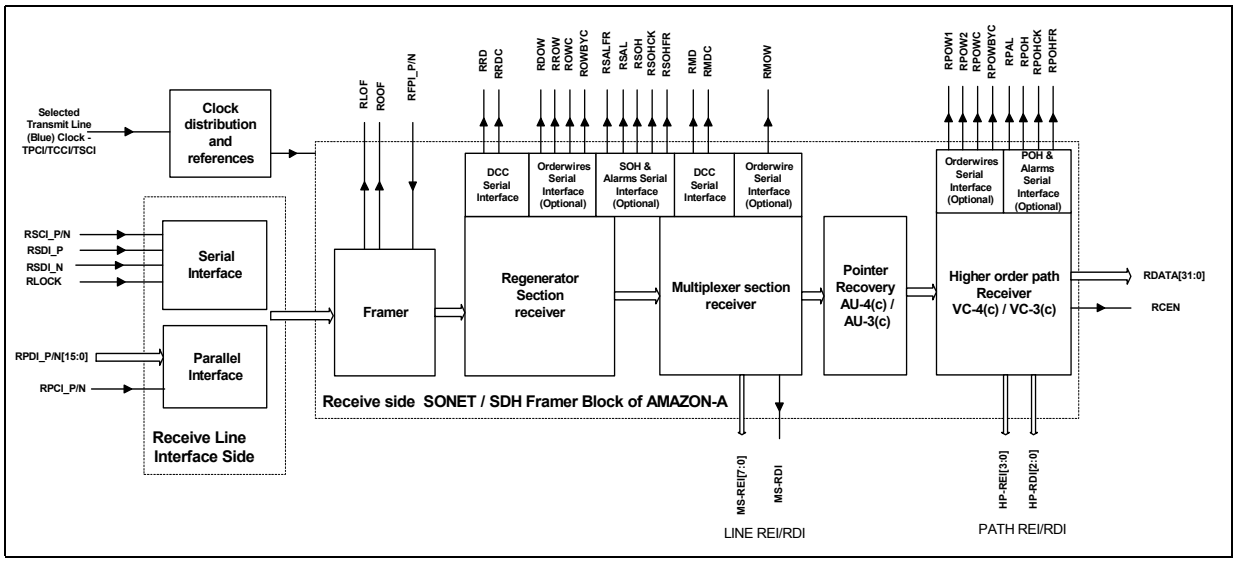
The transmit and the receive side of the 4 channels of the Intel IXF6048 operate independently.

4.4 Detailed Functional Description Per Channel

4.4.1 Receiver Default Operation Per Channel

Figure 7 is a block diagram of the receive section of one SONET/SDH block of the Intel IXF6048. The detailed description below follows the data flow from left to right, describing the functionality and configuration of each SONET/SDH receive framer block. Note that all status change alarms, counter overflow alarms, and receive byte change alarms mentioned, can cause the INT output pin to be activated if they are unmasked. Please refer to the register definition for location of alarms, masks, and interrupts.

Figure 7. SONET/SDH Receiver Blocks



4.4.1.1 Line Interface Processing

A filter for the RLOCK (Receiver Loss Of Synchronization) alarm input is provided by the line interface circuit (register R_RSTC). The filtering on the RLOCK can be integrated over 128 or 4096 bits for OC-1/3 and over 512 or 16384 bits for OC-12/OC-48. A RLOCK status change is indicated in register S_RG. In addition, Intel IXF6048 internally processes a configurable receiver Loss Of Signal (LOS) detection based on data transition or all ‘0’s detection, configured via register R_RSTC. LOS alarm is set when no transition (or all ‘0’s, if configured) occurs in the incoming data for at least X µs (X is configurable to 20 or 25 µs) and cleared if two consecutive framewords are detected and there is no LOS condition between (see register R_RSTC).

For each of the four channels, the interface block accepts a serial format input at RSDI_P/Ni in OC-1/3 mode or an 8-bit parallel input format at RPDI_i[7:0] in OC-1/3/12 mode (four channel operation). For single OC-48 channel operation, the input data may be parallel with an 8- or 16-bit wide bus input at RPDI_P/N[15:0] or a 32-bit wide bus input at RPDI[31:0]. No specific order on the 8-bit, 16-bit, or 32-bit is required for the Intel IXF6048 to operate. The parallel clock is input at RPCI or RPCI_P/N, and the serial clock at RSCI_P/N.

The transmit clock is used for the selected transmit line (Blue) clock signal reference (if so configured—TPCI/TCCI/TSCI):

An active RLOCK (external LOS) or internal LOS can have two consequent actions that can be enabled or disabled (see register R_RSTC):

- Clock switches from receive clock (RPCI/RSCI) to selected transmit line reference (Blue) clock (TPCI/TSCI/TCCI)
- Insert AIS towards the ATM/POS demapping block from the RST section

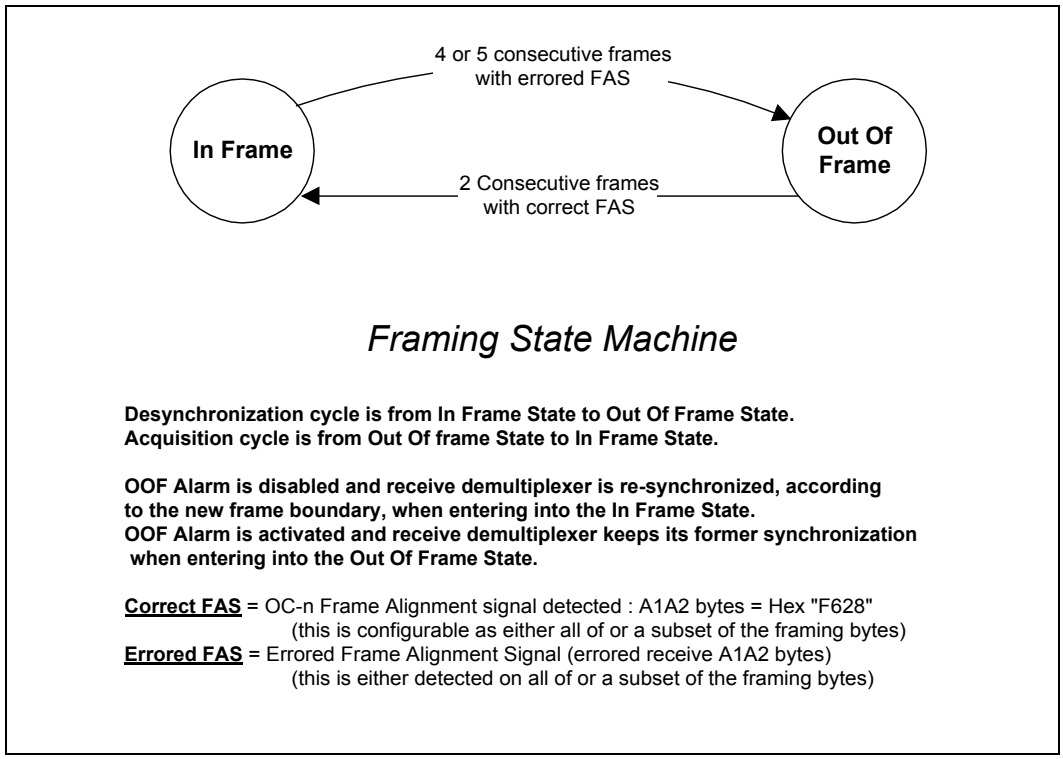
4.4.1.2 Framer

The framer operates on a serial (OC-1/3), parallel 8-bit wide (OC-1/3/12), or parallel 8/16/32-bit wide (OC-48) data input stream. It does not require any external framing in the Line Interface chip as the 8/16/32-bit data input does not have to be aligned in the byte boundary. As an example, when using a 16-bit wide parallel interface at OC-48, the framer eliminates the sixteen phases (bits) of ambiguity and memorizes the position of the framing word. When interfacing with an external line transceiver that performs frame alignment, this function can be disabled in register R_RSTC. Synchronization is then accomplished with an external frame pulse input on pin RFPI. The frame pulse input position regarding frameword is programmable (see register R_FPCNF).

Two consecutive frames with correct framewords are required to change from an Out Of Frame State (OOF) to an In Frame State (INF). In OC-3 and OC-1 mode of operation, the frameword checking is done on **all** the A1 and A2 bytes. In OC-12 mode of operation, the frameword checking is done either on **all** 24 bytes of A1 and A2 or on a **subset** (6 bytes) of the A1 and A2 framing bytes. This is configurable via register R_RSTC, bit RcvFwdOnCfng. In the OC-48 mode, the frameword checking is always done on a subset of the A1 and A2 framing bytes: it is either done on twelve A1 bytes followed by twelve A2 bytes, or done on 6 consecutive bytes at the A1 to A2 transition. This is configurable via register R_RSTC, bit RcvFwdOnCfng.

To declare an OOF condition, either four or five (configurable via register LOF_LMN, bit RcvOofCnfg) consecutive frames with incorrect framewords are required. Again, depending on the mode of operation and configuration of register R_RSTC, bit RcvFwdOofCnfg, an incorrect frameword is declared when the receive frameword is not matching either **all** or a **subset** of the A1 and A2 framing bytes; this configuration is independent of the acquisition configuration. In OC-1 and OC-3 modes of operation, the checking is always done on all the framing bytes. In OC-12 mode of operation, this is either done on all 24 of the framing bytes or on a subset of 6 framing bytes. In the OC-48 mode of operation, it is either done on a subset of 24 bytes (12 A1 followed by 12 A2 bytes) or on a subset of 6 framing bytes.

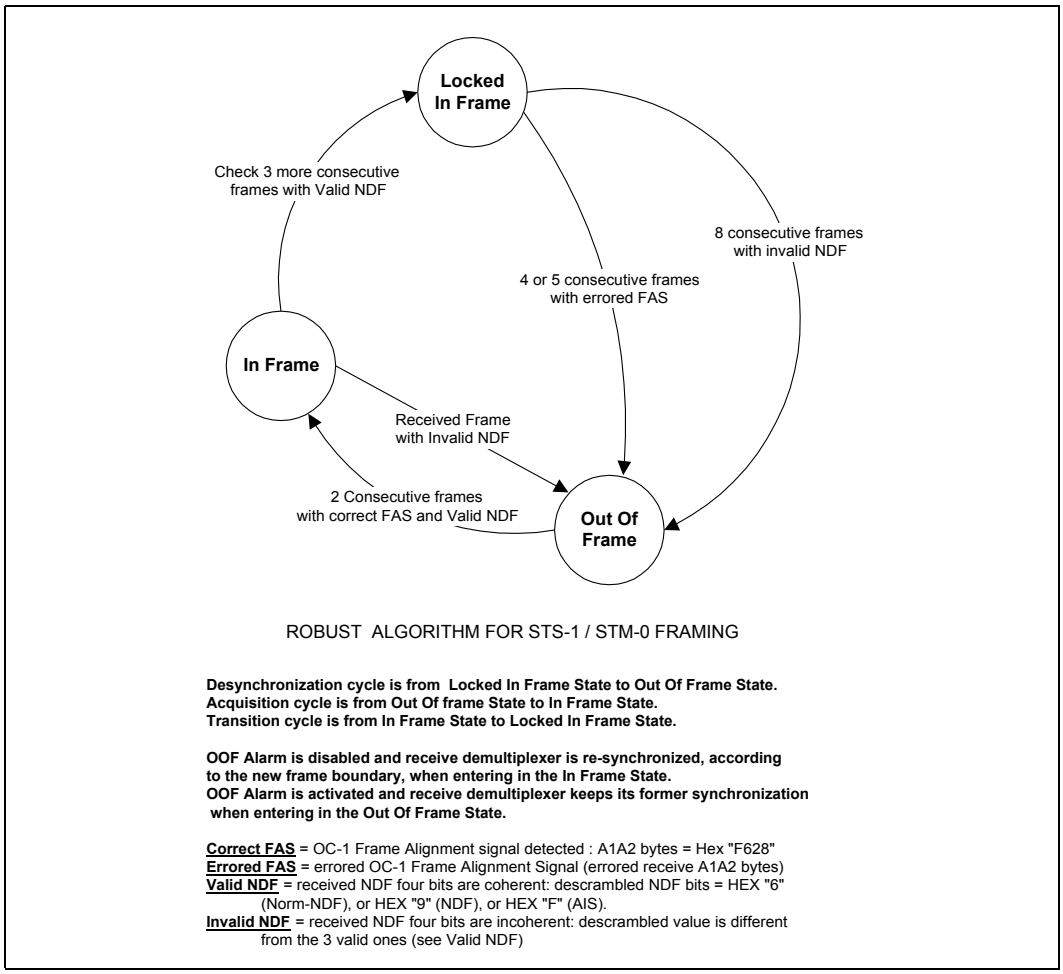
Figure 8. Framing State Machine



For STS-1/STM-0 operation, as the frameword is only 2 bytes (A1A2), two settings are available for the frame acquisition state machine. One follows ITU-T G.783 as described above; the other one also identifies the position of the new data flag (NDF).

This second configuration (called robust configuration) requires five consecutive frames with identical NDF and two consecutive frames with the correct frameword for frame acquisition. This minimizes the probability of incorrect synchronization. To ensure that an OOF condition is activated when an incorrect synchronization occurs, the state machine desynchronizes when eight consecutive frames not having identical NDF bits.

Figure 9. STS-1/STM-0 Robust Framing State Machine



Upon frame acquisition, the framer de-scrambles the signal. The standard scrambler defined by the ITU is (2^7 - 1) is implemented. For testing purposes, the descrambler can be disabled (see register R_RSTC).

4.4.1.2.1 Loss of Frame (LOF) Detection

Upon detection of an Out Of Frame condition, no consecutive action is required by the ITU specifications. The number of Out of Frame events are counted and stored in a 13-bit counter accessible via register OOF_ECNT.

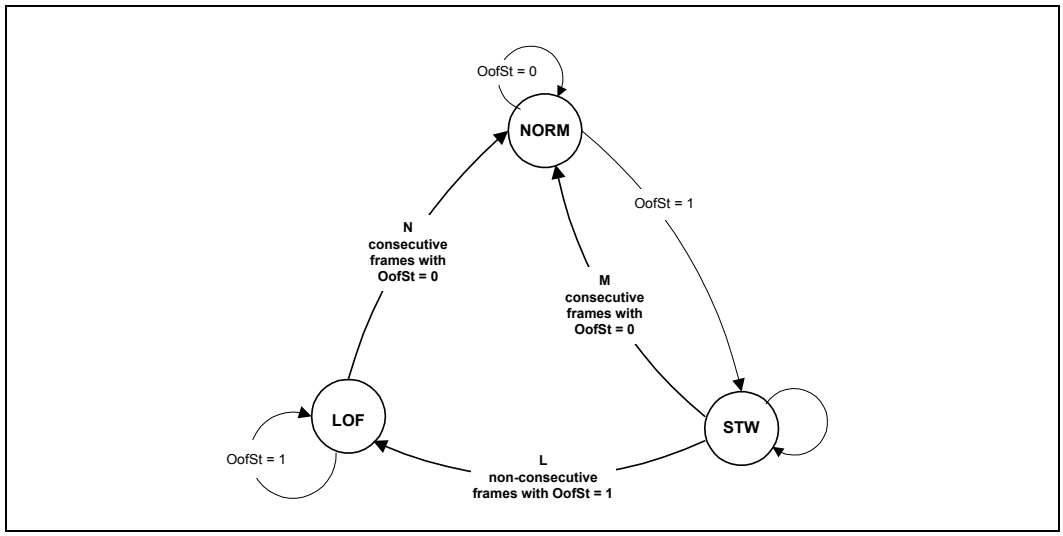
The Loss Of Frame state machine can be configured via the register LOF_LMN. Three parameters are programmable (from 1 to 32 frames) in the state machine:

'M' is the number of consecutive frames with no Out Of Frame conditions required to reenter a normal state—this value is the LOF_LMN register bits[9:5] setting plus 1 (in other words, M = bits[9:5] + 1). **'N'** is the number of consecutive frames with no Out Of Frame conditions required to reenter a normal state from a Loss Of Frame state—this value is the LOF_LMN register bits[4:0] setting plus 1 (in other words, N = bits[4:0] + 1). **'L'** is the number of nonconsecutive frames with

Out Of Frame conditions required to enter a Loss Of Frame state—this value is the LOF_LMN register bits[14:10] setting plus 1 (in other words, L = bits[14:10] + 1). The value of L, M or N is always 1 through 32.

Status changes in the OOF and LOF detectors generate OOF and LOF alarms. Also, output from these detectors is provided at the OOF and LOF output pins.

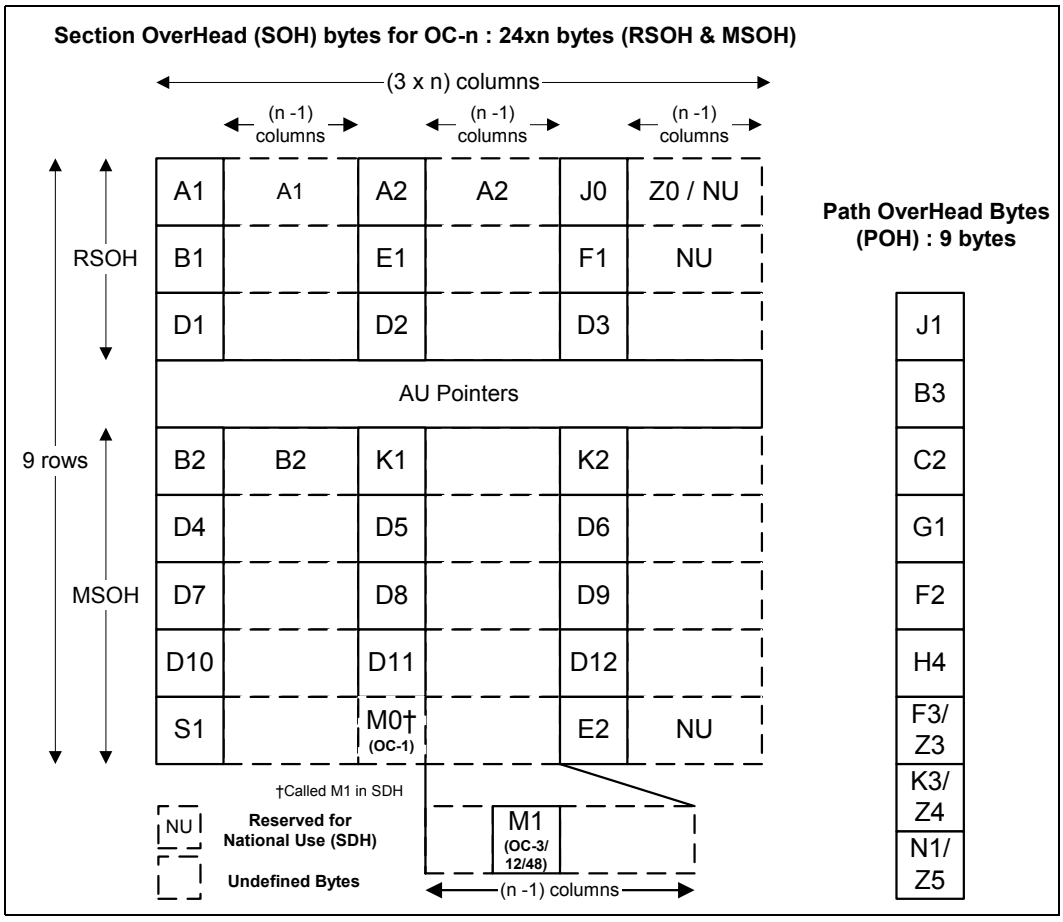
Figure 10. LOF State Machine



4.4.1.3 Regenerator Section Receiver

This section provides access to the Regenerator Section Overhead Bytes required for ATM/POS Physical Layer operation.

Figure 11. Overhead Bytes for the OC-n



4.4.1.3.1 The Regenerator Section Trace J0

This byte is used to repetitively transmit a Section Access Identifier so that a section receiver can verify its continued connection to the intended transmitter. This byte has been defined in the latest specification of ITU. To avoid compatibility problems with in-service equipment, the chip can ignore J0 processing via register J0_RSTC. The J0 string length is configurable via register J0_RSTC to either 1-byte, 16-byte (with CRC-7), 64-byte free format trace message, or 64-byte framed format message (with carriage return and line feed ASCII characters in the last two bytes location). The expected J0 string content is configurable (see register R_J0_ESTRA). For 16-byte trace message operation, this J0 string value needs to have the correct CRC-7 bits per G.707 specifications.

A stable received trace is declared when 3 or 5 (configurable via register J0_RSTC) identical consecutive traces have been detected. The accepted receive J0 trace is then stored in an internal memory that can be accessed by the microprocessor interface via register R_J0_ASTRA. If 8 consecutive received trace are different from the accepted trace, then an unstable trace is declared and J0UnStable alarm is indicated in register IS_RG.

For a 16-byte trace message, the receiver calculates the CRC-7 of the received J0 string. In the case of a a transmission error in the J0 string, a J0 string CRC-7 error (J0Crc7Err) is indicated in register IS_RG.

If a specific byte of the received J0 trace is not equal to its expected value for 3 consecutive received traces (64 × 3 frames), a J0Mismatch (J0MsMtch) is indicated in register IS_RG. This default is cleared when a full received trace message matches with the expected, and, if configured so (see register J0_RSTC), a stable received trace with no CRC-7 errors has been accepted.

In the case of a a mismatch between the expected and received J0 string, a J0MsMtch is indicated in register IS_RG. In the case of a a transmission error in the J0 string, a J0Crc7Err is indicated (16-byte case only) in register IS_RG.

Unstable, mismatch, and CRC-7 error detection are 3 fully independent processes, but it is possible via configuration register J0_RSTC to force the J0Mismatch alarm (RS Trace Identification Mismatch Alarm) when a received trace is unstable or to mask it when the CRC-7 alarm (if 16-byte trace mode) has been.

Note: During changes in the starting position of the trace, which can occur in an APS operation where a byte can be lost or repeated, ignore mismatch and unstable alarms. The new Bellcore* 2000 R6-406/7 specification says to ignore mismatch and unstable alarms when there are phase changes in the incoming signal.

4.4.1.3.2 BIP-8 B1 Byte

This byte is used for Regenerator Section error monitoring. The error events are counted in a 16-bit counter accessible via registers B1_ERRCNT.

The B1 counter can be configured as either a bit or a block counter (see register R_RSTC).

4.4.1.3.3 E1 Orderwire Byte (Optional)

This 64-Kbit/s channel is used to optionally provide an orderwire channel for voice communication. The data is accessible serially either via RROW dedicated port or via the RSOH bus output. In the case of a dedicated port, the 64-KHz clock and the 8-KHz byte synchronization signals are used to receive both the E2 and F1 bytes and can be provided at pins ROWC and ROWBYC.

4.4.1.3.4 F1 Byte (Optional)

This 64-Kbit/s channel is used for optional user purposes and can be used as extra maintenance orderwire channel. The data is accessible either via RDOW dedicated port or via the RSOH serial bus. In the case of a dedicated port, the 64-KHz clock and the 8-KHz byte synchronization signals are used to receive both the E2 and F1 bytes and are provided at pins ROWC and ROWBYC. Note that the access to this channel is limited in quad processor mode (due to pin count) as it is multiplexed on the same pin as the DCC channel.

4.4.1.3.5 D1 to D3 Data Communication Channels

This 192-Kbit/s channel (DCC) may be used by the network management as a data channel. The data is accessible either via dedicated pin RRD (clock is provided by RRDC) or via serial output bus RSOH. In the case of a dedicated serial access, note that ROWBYC can be used as an 8-KHz synchronization if required.

4.4.1.3.6 National Used/Z0 Bytes, Media Dependent, and Undefined Bytes of the RSOH

These bytes are only relevant in OC-3/12/48 mode and can only be accessed via the serial RSOH output.

4.4.1.3.7 Receive Regenerator Section AIS (RstAIS)

The AIS generated after the Regenerator Section is labeled RstAis. It can be inserted on the following conditions:

- Internally processed Loss Of Signal (LOS)
- External Receive Loss Of Clock Synchronization alarm input (RLOCK)
- Loss Of Frame (LOF)
- Trace Identification Mismatch (J0MsMtch)

These conditions can be individually enabled or disabled (see register R_RSTC). A test register that can force an RstAis for test purposes is also available. RstAis insertion is indicated in global register S_AIS for each of the 4 channel.

4.4.1.4 Multiplexer Section Receiver

The Multiplexer Section receiver handles the MSOH overhead bytes required for ATM/POS Physical Layer operation.

4.4.1.4.1 B2 Error Bytes

These bytes are used for Multiplexer Section error monitoring. The B2 errors are counted either as block error in registers B2_BLKCNT (17-bit) or as bit errors in registers B2_BIPCNT (22-bit counter). In STM-1 mode, a block is equivalent to an entire frame. In STM-4 and STM-16 modes, a block has two definitions (see register configuration R_MST_C):

- The entire STM-4 or STM-16 frame.
- An STM-1 equivalent frame, which is four blocks in STM-4 and sixteen blocks in STM-16.

An **Excessive Error Defect (EED)** indication (see register IS_MUX) is generated by integrating the B2 errors in a sliding window. Integration is also used when clearing the EED indication. Six registers allow the configuration of EED indication thresholds, hysteresis, and probability of detection. They are WINSZ_SB2, CWIN_SB2, E#_EXCWIN_SB2, WINSZ_CB2, CWIN_CB2, and E#_NEXCWIN_CB2 registers. These six registers allow configuring the EED thresholds (BER setting and clearing thresholds are fully independent) from a Bit Error Rate of 10–3 to a bit error rate of 10–8 or lower, even in the case of a non-Gaussian statistical distribution of errors. An active EED indication can be configured to insert an AIS signal, to generate Signal Fault defect, and/or to generate an RDI defect (see register R_MST_C, bit #7 and #2).

Table 12. EED Register Settings

	BER[1]	10^{-3}	10^{-4}	10^{-5}	10^{-6}	10^{-7}	10^{-8}	10^{-9}
STS-1 Rate settings	ExcB2Min[3] - V_{Set} ExcB2Max[4] - V_{Clear}	154	1000 52	100 50	10 2	1	1	NA
	ExcB2SetWinSz[5] - SZ_{Set} ExcB2ClrWinSz[6] - SZ_{Clear}	2	194 9	194 96	194 38	194	1949	NA
	ExcB2SetWinNum[7] - W_{Set}[2] ExcB2ClrWinNum[8] - W_{Clear}[2]	4 1	6 1	127 1	127 25	127 51	127 51	NA
STS-3 Rate settings	ExcB2Min[3] - V_{Set} ExcB2Max[4] - V_{Clear}	1538	308 31	140	2	1	1	NA
	ExcB2SetWinSz[5] - SZ_{Set} ExcB2ClrWinSz[6] - SZ_{Clear}	9	19 1	90	12	64	649	NA
	ExcB2SetWinNum[7] - W_{Set}[2] ExcB2ClrWinNum[8] - W_{Clear}[2]	1	61 5	127 1	127 76	127	127	NA
STS-12 Rate settings	ExcB2Min[3] - V_{Set} ExcB2Max[4] - V_{Clear}	1231	185	400 80	40	4	1	1
	ExcB2SetWinSz[5] - SZ_{Set} ExcB2ClrWinSz[6] - SZ_{Clear}	1	2	64 12	64	64	161	1624
	ExcB2SetWinNum[7] - W_{Set}[2] ExcB2ClrWinNum[8] - W_{Clear}[2]	6 1	127 3	127 1	127 3	127 38	127	127
STS-48 Rate settings	ExcB2Min[3] - V_{Set} ExcB2Max[4] - V_{Clear}	2461	1477	320 197	32	32	32	3
	ExcB2SetWinSz[5] - SZ_{Set} ExcB2ClrWinSz[6] - SZ_{Clear}	0	5	12 7	12	129	1299	1218
	ExcB2SetWinNum[7] - W_{Set}[2] ExcB2ClrWinNum[8] - W_{Clear}[2]	11 1	127 1	127 1	127 4	127 4	127 4	127 34

NOTES:
1. These BER values may not be exactly 1.000. See Equation 1 below for calculating this value.
2. The value of these register fields depend upon the system requirements and application. The values given meet ITU-T G.806 max setting and max clearing requirements (Tables 6-4 & 6-6) and Telcordia* GR 253 max clearing and objective clearing requirements (Table 5-3).
3. This field is in register E#_EXCWIN_SB2.
4. This field is in register E#_NEXCWIN_CB2.
5. This field is in register WINSZ_SB2.
6. This field is in register WINSZ_CB2.
7. This field is in register CWIN_SB2.
8. This field is in register CWIN_CB2.

A **Degraded Signal Defect (DSD)** indication (see register IS_MUX) is also generated by integrating the B2 errors in a different sliding window. Integration is also used when clearing the DSD indication. Six registers allow the configuration of DSD indication thresholds, hysteresis, and probability of detection. They are WINSZ_SDEGB2, CWIN_SDEGB2, E#_DEGWIN, WINSZ_CDEGB2, CWIN_CDEGB2, and E#_NDEGWIN_CB2 registers. These six registers allow configuring the DSD thresholds (BER setting and clearing thresholds are fully independent) from a Bit Error Rate of 10–3 to a bit error rate of 10–11 or lower, even in the case of a non-Gaussian statistical distribution of errors (including bursty distribution of errors).

Table 13. DSD Registers Setting

	BER[1]	10^{-5}	10^{-6}	10^{-7}	10^{-8}	10^{-9}	10^{-10}	10^{-11}	10^{-12}	10^{-13}
STS-1 Rate settings	DegB2Min[3] - V_{Set} DegB2Max[4] - V_{Clear}	20	2	1	1	1	1	1	NA	NA
	DegB2SetWinSz[5] - SZ_{Set} DegB2ClrWinSz[6] - SZ_{Clear}	38	38	194	1949	19505	195059	1950599	NA	NA
	DegB2SetWinNum[7] - W_{Set}[2] DegB2ClrWinNum[8] - W_{Clear}[2]	127 2	127 25	127 51	127 51	127 51	127 51	127 51	NA	NA
STS-3 Rate settings	DegB2Min[3] - V_{Set} DegB2Max[4] - V_{Clear}	20	2	1	1	1	1	1	1	NA
	DegB2SetWinSz[5] - SZ_{Set} DegB2ClrWinSz[6] - SZ_{Clear}	12	12	64	649	6501	65019	650199	6501999	NA
	DegB2SetWinNum[7] - W_{Set}[2] DegB2ClrWinNum[8] - W_{Clear}[2]	127 7	127 76	127	127	127 102	127 82	127 8	127 1	NA
STS-12 Rate settings	DegB2Min[3] - V_{Set} DegB2Max[4] - V_{Clear}	80	80	80	80	1	1	1	1	NA
	DegB2SetWinSz[5] - SZ_{Set} DegB2ClrWinSz[6] - SZ_{Clear}	12	129	1299	12999	1624	16254	162549	1625490	NA
	DegB2SetWinNum[7] - W_{Set}[2] DegB2ClrWinNum[8] - W_{Clear}[2]	127 1	127 1	127 1	127 1	127 102	127 81	127 8	127 1	NA
STS-48 Rate settings	DegB2Min[3] - V_{Set} DegB2Max[4] - V_{Clear}	320 197	64	64	64	64	1	1	1	1
	DegB2SetWinSz[5] - SZ_{Set} DegB2ClrWinSz[6] - SZ_{Clear}	12 7	25	259	2599	25999	4062	40637	406390	4063900
	DegB2SetWinNum[7] - W_{Set}[2] DegB2ClrWinNum[8] - W_{Clear}[2]	127 1	127 2	127 2	127 2	127 1	127 83	127 8	127 1	127 1

NOTES:
1. These BER values may not be exactly 1.000. See Equation 1 below for calculating this value.
2. The value of these registers fields depend upon the system requirements and application. The values given meet ITU-T G.806 max setting and max clearing requirements (Tables 6-4 & 6-6) and Telcordia* GR 253 max clearing and objective clearing requirements (Table 5-3).
3. This field is in register E#_DEGWIN_SB2.
4. This field is in register E#_NDEGWIN_CB2.
5. This field is in register WINSZ_SDEGB2.
6. This field is in register WINSZ_CDEGB2.
7. This field is in register CWIN_SDEGB2.
8. This field is in register CWIN_CDEGB2.

Based on B2 detected errors per frame, an MS-REI value is encoded (as BIP or Block errors: see configuration register R_MST_C). This value is internally looped to the transmitter and provided serially at the Receive Section Alarm bus output, RSAL.

The BER threshold is derived by the following formula:

Equation 1. BER = V / ((SZ + 1) · N · 51264)

Where V is the number-of-B2-errors register field value for setting or clearing; SZ is the window-size-component register field value for setting or clearing and is used to derive the number of frames in a window; and N is the STS line rate. See the *Intel® Framer B2 Error Threshold Calculation (EED/DSD) Application Note* (order number 273717) for more details on BER threshold setting.

4.4.1.4.2 K1 and K2 Bytes: Automatic Protection Switching Channel

These bytes are assigned for the APS signaling. A change in K1 byte for three consecutive frames is indicated in register IS_MUX (RcvK1Chg bit) and allows the updating of register R_K2K1 (8 LSB bits). A change in K2 byte for three consecutive frames is indicated in register IS_MUX (RcvK2Chg bit) and allows the updating of register R_K2K1 (8 MSB bits). Register R_K2K1 provides so microprocessor access to both K1 and K2 received filtered values. When the value of K1 byte has not been detected identical for 3 consecutive frames in a window of 16 frames, a RcvK1Unstable alarm is indicated in register IS_MUX. When the value of K2 byte has not been detected identical for 3 consecutive frames in a window of 16 frames, a RcvK2Unstable alarm is indicated in register IS_MUX.

It is possible to configure the K1/K2 process as for a single channel (see configuration register R_MST_C). In this mode, a change in K1/K2 bytes for three consecutive frames is indicated in register IS_MUX and allows the updating of register R_K2K1, providing K1/K2 received APS filtered value.

The K1 and K2 received filtered values (APS channel), the indications of K1 and K2 change, and the K1 and K2 Unstable alarms are provided serially at the Receive Section Alarm bus output, RSAL.

The K1 and K2 receive bytes are provided serially at RSOH serial bus output.

4.4.1.4.3 MS-RDI Via K2 Byte (Generation and Detection)

The Multiplex Section Remote Defect Indication (MS-RDI) is used to tell the transmit end that the received end has detected an incoming section defect or is receiving MS-AIS. The MS-RDI generated defect is internally looped to the transmitter and provided serially at the Receive Section Alarm bus output, RSAL.

An MS-RDI is detected when the three received K2[2:0] bits have a value of '110' for three, five, ten, or 16 consecutive frames (configurable via register R_MST_C). MS-RDI detector status changes are indicated in register IS_MUX. The detected MS-RDI defect is provided serially at the Receive Section Alarm bus output, RSAL.

4.4.1.4.4 MS-AIS Via K2 Byte (Detection)

The Multiplex Section AIS is detected when the three received K2[2:0] bits have a value of '111' for three or five (configurable via register R_MST_C) consecutive frames. MS-AIS detector status changes are indicated in register IS_MUX. The detected MS-AIS defect is provided serially at the Receive Section Alarm bus output, RSAL.

4.4.1.4.5 MS-REI Via M1 Byte

This byte is allocated for the Remote Error Indication. Remote BIP errors are accumulated in a 21-bit counter, accessible via registers MR_BIPCNT. Remote block errors are accumulated in an 17-bit counter, accessible via registers MR_BLKCNT.

Note: In concatenated mode for all line rates, the errors are accumulated in the associated port/interfaces MR_BIPCNT/MR_BLKCNT register (for example, for traffic received on port interface 0, the values would be accumulated in register 0's MR_BIPCNT/MR_BLKCNT).

Note: In non-concatenated mode for STS-3 and STS-12/STM-4 line rates, the errors are accumulated in port/interface 2's MR_BIPCNT/MR_BLKCNT register (for example, for traffic received on port interface 0, the only line side port usable with non-concatenated traffic, the values would be accumulated in register 2's MR_BIPCNT/MR_BLKCNT).

Note: In non-concatenated mode for STS-48/STM-16 line rates, the errors are accumulated in port/interface 0's MR_BIPCNT/MR_BLKCNT register (for example, for traffic received on port interface 0, the only line side port usable with non-concatenated traffic, the values would be accumulated in register 0's MR_BIPCNT/MR_BLKCNT).

A block can be considered over a frame or as per STM-1 equivalent (see register configuration R_MST_C), meaning that an OC-48 contains either 1 or 16 blocks. M1 receive byte is provided serially at RSOH serial bus output.

4.4.1.4.6 S1 Byte: Synchronization Status

S1[3:0] bits are allocated for Synchronization Status Messages. A change in S1 byte for three consecutive frames is indicated in register IS_MUX and allows the updating of register R_S1. Register R_S1 provides microprocessor access to S1 received filtered value. When the value of S1 byte has not been detected identical for 3 consecutive frames, in a window of 16 frames, a RcvS1Unstable alarm is indicated in register IS_MUX.

S1 receive byte is also provided serially at RSOH serial bus output.

4.4.1.4.7 D4 to D12 Data Communication Channels

This 576-Kbit/s channel (DCC) may be used to by the network management as a data channel. The data is accessible via pin RMD and the clock is provided by RMDC. D4 to D12 receive bytes are also provided serially at RSOH serial bus output.

4.4.1.4.8 E2 Byte: Orderwire Byte (Optional)

This 64-Kbit/s channel is used to optionally provide an orderwire channel for voice communication. The data is accessible via RMOW. The 64-KHz clock and the 8-KHz byte synchronization signals are used to receive both the E2 and F1 bytes and are provided at pins ROWC and ROWBYC. Note that the access to this channel is limited in quad processor mode (due to pin count) as it is multiplexed on the same pin as the DCC channel. E2 receive byte is also provided serially at RSOH serial bus output.

4.4.1.4.9 National Used and Undefined Bytes of the MSOH

These bytes are only relevant in OC-3/12/48 mode and can only be accessed via the serial RSOH output.

4.4.1.4.10 Receive Multiplexer Section AIS (MS-AIS)

The AIS generated after the multiplexer section is labeled MstAis. It can be inserted on the following conditions:

- MS-AIS detection in K2
- EED detection

The AIS insertion can disabled or forced via register R_MST_C. The EED dependency can be disabled via register R_MST_C (ITU specification). MstAis insertion is indicated in register S_AIS.

4.4.1.5 Pointer Recovery

4.4.1.5.1 Pointer Recovery Block

The pointer recovery block interprets the value of the incoming pointer associated with a VC-3 (STS-1/STM-0), a 3x VC-3 concatenated/VC-4 (STS-3c/STM-1), a 12x VC-3 concatenated/4 VC-4 concatenated (STS-12c/STM-4c), or a 48x VC-3 concatenated/16x VC-4x concatenated (STS-48c/STM-16c) single payload. The AU pointer includes two SS undefined bits. These bits can be either ignored or recovered in the receive pointer processor (see register R_MSA_C) to be compared with their expected value (programmed in register R_MSA_C).

The monitoring function of the receive pointer processor includes the following counters:

- An 11-bit Positive Justification Counter accessible via register R_AU_PCNT.
- An 11-bit Negative Justification Counter accessible via register R_AU_NCNT.

This block indicates the following conditions via register IS_ADP: an AU-AIS (all '1's. in the pointer), Loss of Pointer (LOP), or New Data Flag (NDF).

The LOP detection follows the ITU G.783 recommendation using eight consecutive frames.

The pointer bytes are serially accessible at the RSOH bus output.

In the case of a contiguous concatenation (AU-4, AU-4-4c, AU-4-16c), the pointer recovery block also performs verification of the presence of concatenation indicators. The algorithm follows the one specified by ITU-T rec. G.783, annex C.2. The check of the concatenation identification may be performed either on all the H1/H2 pairs not transporting the current pointer value or only on a subset of them (per STM-1 equivalent in the case of an STM-N). This is configurable via register R_MSA_C. A Loss Of Pointer Concatenation identification (LOPC) defect is indicated to the monitoring function via register IS_ADP when the configured concatenation indicators (H1/H2 pairs) receive value is different from “1001SS11 11111111” (concatenation) or different from all '1's (AISC) for eight consecutive receive frames. The LOPC detected defect may create an HP-RDI or an AIS generation, if configured so via register R_MSA_C. If configured so via register R_MSA_C, the AU-AIS defect may be asserted only if both the pointer interpreter and concatenation verification state machines are in the AIS state (both receive pointer and configured pointer identification H1/H2 are all '1's).

4.4.1.5.2 Receive Adaptation Section AIS (DmsaAIS)

The AIS generated after the Pointer recovery section is labeled DmsaAis. It can be inserted on the following conditions:

- AU-AIS detection (all '1's. pointer for three consecutive frames and, if configured as such, all '1's. in the concatenation indicator bytes)
- LOP detection
- LOPC detection (the Loss Of Pointer Concatenation indication action on DmsaAis may be disabled/enabled via configuration register R_MSA_C).

The AIS can be disabled or forced via register R_MSA_C. DmsaAis insertion is indicated in register S_AIS.

4.4.1.6 Higher Order Path Receiver

The Higher Order Path Receiver processes the overhead bytes associated with the Higher Order Path Overhead which are required for ATM/POS Physical Layer operation.

4.4.1.6.1 J1 Byte Path Trace

This byte is used to repetitively transmit a Path Access Identifier so that a path receiver can verify its continued connection to the intended transmitter. The length of the expected J1 string can be programmed to either 64-bytes free format (non-specified), 64-bytes framed format (carriage return and line feed ASCII characters in the last two byte locations), 16-bytes framed format with CRC-7, or 1-byte (see register R_HPT_C2). The 16-byte expected J1 string value needs to have the correct CRC-7 bits per G.707 specifications. The expected J1 string content is configurable (see register R_J1_ESTRA).

A stable receive trace is declared when 3 or 5 (configurable via register R_HPT_C2) identical consecutive traces have been detected. The accepted receive J1 trace is then stored in an internal memory that can be accessed by the microprocessor interface via register R_J1_ASTRA. If 8 consecutive received traces are different from the accepted trace, then an unstable trace is declared and J1UnStable is indicated in register IS_HPT. If the accepted receive trace is detected to be all '0's, then a J1 all zero interrupt bit is set in register IS_HPT (this may be used for “non supervisory unequipped” detection).

Note: For automatic detection of all ‘0’, only the first byte of a J1 trace is checked. In the case of 16 and 64-byte modes, if the first byte is all zeros and the following bytes are other than zero, an all-zero alarm is triggered after three to five frames (depending on the configuration). Software can be used to distinguish between the J1 traces.

In the case of a mismatch between the expected and received J1 string, a J1MsMtch is indicated in register IS_HPT. In the case of a transmission error in the J1 string, a J1Crc7Err is indicated (16-byte case only) in register IS_HPT and masks the J1MsMtch indication.

The J1 received path trace can be ignored via configuration register R_HPT_C2.

Unstable, mismatch, and CRC-7 error detection are 3 independent processes, but it is possible via configuration register R_HPT_C2 to force the J1Mismatch alarm (HPath Trace Identification Mismatch Alarm) when received trace is unstable or to mask it when the CRC-7 alarm (if 16-byte trace mode) has been active.

Note: During changes in the starting position of the trace, which can occur in an APS operation where a byte can be lost or repeated, ignore mismatch and unstable alarms. The new Bellcore* 2000 R6-

406/7 specification says to ignore mismatch and unstable alarms when there are phase changes in the incoming signal.

The Trace Identifier Mismatch is also provided at the RPAL serial alarm bus output and the J1 received byte is serially accessible at RPOH bus output pin.

4.4.1.6.2 B3 Byte

This byte is used for Higher Order Path error monitoring. The error events are counted in a 16-bit counter accessible via registers B3_ECNT.

The B3 counter can be used either as a bit or a block counter configurable via register R_HPT_C1.

Based on the number of the B3 detected errors per frame, an HP-REI value is encoded. This value is internally looped to the transmitter and provided serially at the Receive Path Alarm bus output, RPAL.

4.4.1.6.3 C2 Byte Signal Label

This byte indicates the composition of the payload (value 13H for ATM mapping). A change in the C2 byte for three or five (configurable via register R_HPT_C1) consecutive frames is indicated in register IS_HPT and allows the updating of register R_C2 providing the value of the receive accepted C2 Signal Label (filtered value). This value is also provided at RSAL serial alarm bus output.

An unstable receive signal label is declared when the receive C2 byte has been detected different from the C2 of the previous frame for 3 or 5 times (configurable via register R_HPT_C2), and during this integration period, the value of C2 has not been stable for 3 (or 5) consecutive received frames. C2Unstable alarm is indicated in register IS_HPT. If 3 (or 5) consecutive received C2 values are detected as identical, the C2Unstable alarm is cleared.

An expected value of C2 can be programmed in register EXP_C2. If the received filtered C2 value (accepted signal label) is not equal to the expected value and is not 00H (Unequipped Indication) or 01H (equipped-non specific), this is indicated in register IS_HPT via the HptSlm (HPT Signal Label Mismatch). The HptSlm alarm is also provided at the RPAL serial alarm bus output.

Unstable and mismatch detection are two independent processes, but it is possible via configuration register R_HPT_C1 to force the HptSlm (C2 Signal Label Mismatch Alarm) when received C2 is unstable.

VC-AIS is defined as all '1's. in C2 (new G.783 specifications). Five consecutive frames are required for the VC-AIS detection which is indicated in register IS_HPT.

The C2 received byte is also serially accessible at RPOH bus output pin.

4.4.1.6.4 Unequipped Detection

The unequipped detector (C2 = all '0's) requires 5 frames before it is indicated in register IS_HPT. The unequipped alarm is also provided at the RPAL_i (i = 0, 1, 2, 3) serial alarm bus output.

All the necessary information is provided to and from the monitoring function to support either “supervisory unequipped” or “non supervisory unequipped” in the case of a network not supporting the Tandem Connection. The following alarms and indication are accessible in registers IS_HPT, and B3_ECNT:

- C2 equal to all '0's (Unequipped)
- First byte of the J1 accepted trace is equal to all '0's
- J1 trace correct or incorrect (J1 Mismatch/Unstable)
- B3 detected BIP/Block errors (B3 error counter)

In addition, for the support of "supervisory unequipped", it is possible to disable HP-RDI generation and/or AIS generation because of the Unequipped (C2 = all '0's) detection, via configuration register R_HPT_C2. In this case, the HP-TIM alarm would trigger both HP-RDI and AIS generation instead of the detected Unequipped (C2 = all '0's).

4.4.1.6.5 G1 Byte

This byte conveys the path status and performance back to a VC-Nc trail termination source as detected by a trail termination sink.

G1[7:4] bits act as a Remote Error Indication (REI). They report the number of B3 errors detected at the remote end. These REI errors are accumulated in the REI counter register HPTREI_CNT. The REI counter can be selected as a bit counter or as a block counter via register R_HPT_C1.

G1[3:1] bits act as a Remote Detection Indication (RDI). They, along with G1[0] (spare bit), are accessible via register R_HPT_RDI. The contents of this register is filtered over 3, 5, 10, or 16 frames, configurable via register R_HPT_C1. An update to register R_HPT_RDI is indicated in register IS_HPT. It is possible to configure the receive path RDI as non enhanced (see register R_HPT_RDI), so that update and detection of the path RDI is only based on G1[3] bit.

The receive path REI bits and filtered value of receive RDI are serially accessible at the RPAL serial alarm bus output and the receive G1 byte is serially accessible at RPOH bus output pin.

An RDI is reported to the far-end upon detection of an LOP, AU-AIS, TIM (J1 Mismatch), SLM (C2 Mismatch), unequipped alarm, or an LCD (Loss Of ATM Cell Delineation). The dependency and coding of RDI on either of these conditions is configurable via R_HPT_C1 (generated RDI as enhanced or non enhanced). This ensures compatibility of the new equipment with an installed equipment base. (See Table 14). The generated RDI bits are so internally looped to the transmitter and serially accessible at the RPAL serial alarm bus output.

4.4.1.6.6 F2 Byte (Optional)

This 64-Kbit/s channel is used for optional user purposes and can be used as an extra maintenance orderwire channel. The data is accessible via RPOW1. The 64-KHz clock and the 8-KHz byte synchronization signals are also used to receive the F3 byte and are provided at pins RPOWC and RPOWBYC. Note that the access to this channel is limited in quad processor mode (due to pin count).

The receive F2 byte may be also serially accessible at RPOH bus output pin.

4.4.1.6.7 F3/Z3 Byte (Optional)

This 64-Kbit/s channel is used for optional user purposes and can be used as extra maintenance orderwire channel. The data is accessible via RPOW2. The 64-KHz clock and the 8-KHz byte synchronization signals are used to receive also the F2 byte and are provided at pins RPOWC and RPOWBYC. Note that the access to this channel is limited in quad processor mode (due to pin count).

The receive F3 byte may be also serially accessible at RPOH bus output pin.

4.4.1.6.8 K3/Z4, H4, and N1/Z5 Bytes (Unused)

These three bytes can only be accessed via the serial RPOH output bus pin.

4.4.1.6.9 Receive Higher Order Path AIS (HptAIS)

The AIS generated after the HPOH receiver is labeled HptAis. It can be inserted on the following conditions:

- SLM (C2 byte mismatches)
- TIM (J1 string mismatches)
- Unequipped detection

These conditions can be individually enabled or disabled (see register R_HPT_C2). The AIS can also be forced via register R_HPT_C2. Its status is accessible via global register S_AIS.

4.4.1.6.10 STS-1/STM-0 Stuff Columns

In OC-1 mode, the 30th and 59th columns of the STS-1-SPE (designated as “stuff columns”) can be configured via register R_HPT_C1 to be part of the payload or not. When configured as stuff columns, their contents is not part of the B3 BIP calculation as they are not part of the VC-3 and these bytes are unused. When configured to be part of the payload, these bytes transport regular traffic.

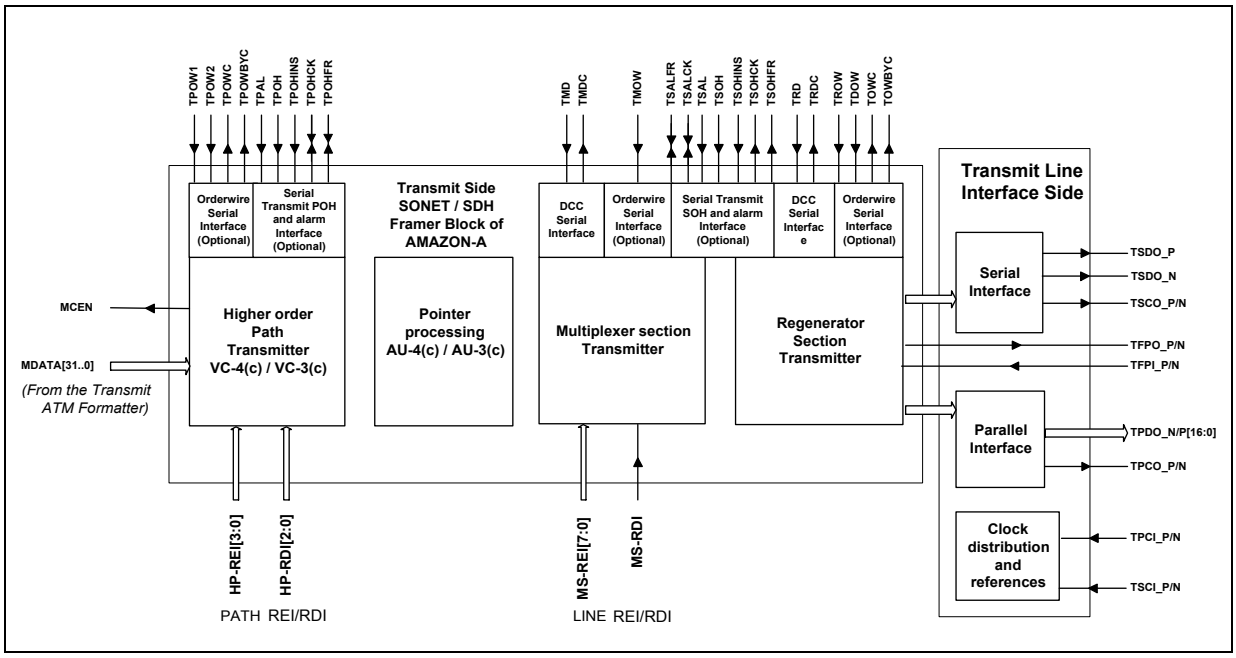
4.4.2 Transmitter Default Operation Per Channel

4.4.2.1 Higher Order Path Transmitter

The HPT transmitter receives its input signal from the transmit ATM cell mapper or HDLC processor block. It inserts the Higher Order Path Overhead and synchronizes the VC-Nc payload.

All HPOH bytes can be sourced from the serial TPOH or TPAL inputs, microprocessor registers, internal processing, or downstream data (non insertion mode). An AIS signal can be forced on the incoming payload data via register (1cc)E8H.

Figure 12. SONET/SDH Transmitter Blocks



4.4.2.1.1 J1 Byte: Path Trace Identifier

This byte is used to transmit a repetitive Path Trace Identifier so that a path receiver can verify its continued connection to the intended transmitter. The length of the transmit J1 string can be programmed to either 64-bytes (non-specified or framed), 16-bytes with CRC-7, or 1-byte via register T_HPT_OPC. The J1 byte may also be set to its default value (if not used) 01H.

The 16-byte expected J1 string value needs to have the correct CRC-7 bits per G.707 specifications. If the higher order concatenated VCs are configured unequipped in the case of “non supervisory unequipped” (see register T_HPT_OPC), then J1 byte can be automatically set to all '0's (see register T_HPT_OPC). If the payload is configured other than “non supervisory unequipped”, J1 is provided by the internal RAM (up to 64-bytes), if it is not set to the default value. If the VC is not configured as unequipped and the transmit trace not set to its default value, J1 is provided by one of the three sources configured in register T_HPT_C, combined with the serial bus control TPOHINS input pin:

- The serial TPOH interface (TPOH input pin).
- The incoming byte from the downstream data—when **all POH** bytes are configured in pass-through mode.
- An internal RAM (up to 64-bytes).

The RAM is accessed via register T_J1_STRA. Note that a complete 16-byte string with CRC-7 is required by the ITU for proper operation.

4.4.2.1.2 B3 Byte

The transmit B3 can be provided by one of the three sources configured in register T_HPT_C, combined with the serial bus control TPOHINS input pin

- The serial TPOH interface (TPOH input pin).
- The incoming byte from the downstream data—when **all POH** bytes are configured in pass-through mode.
- The BIP-8 calculation on the previous concatenated payload (default setting). For testing purposes, it is possible to invert the B3 value via software configuration (see register T_HPT_OPC). The B3 value can be inverted for a single frame (8 errors) or for an indefinite duration.

4.4.2.1.3 C2 Byte: Path Label

If the concatenated higher order VCs are configured unequipped (see register T_HPT_OPC), then the C2 byte is automatically set to '0'. Otherwise, the C2 source is specified by register T_HPT_C, combined with input control pin TPOHINS, as coming from:

- The serial TPOH interface (TPOH input pin).
- The incoming byte from the downstream data—when **all POH** bytes are configured in pass-through mode.
- An internal register (MP_TC2) programmed by the microprocessor.

4.4.2.1.4 G1 Byte: Higher Order Path Remote Error Indication HP-REI

The G1-REI bits (G1[7:4]) source is specified by the register T_HPT_C, combined with input serial bus control pin TPOHINS. It can be either provided by:

- The serial TPOH interface (TPOH input pin).
- The serial Transmit Path Alarm port (TPAL input pin).
- The incoming byte from the downstream data—when **all POH** bytes are configured in pass-through mode.
- Internal processing (see register R_HPT_C1).

In the case of internal processing, the REI bits can be either provided by the B3 error value on the receiver or be disabled (set to '000').

4.4.2.1.5 G1 Byte: Higher Order Path Remote Defect Indication HP-RDI

The G1-RDI bits (G1[3:1]) and Spare bit (G1[0]) source is specified by the register T_HPT_C, combined with input serial bus control pin TPOHINS. It can be either provided by:

- The serial TPOH interface (TPOH input pin).
- The serial Transmit Path Alarm port (TPAL input pin).
- The incoming byte from the downstream data—when **all POH** bytes are configured in pass-through mode).
- An internal register (register MP_THPTRDI) programmed by the microprocessor. (In this case, the G1 spare bit is also sourced from MP_THPTRDI).
- The Receiver defects (Automatic insertion: internal feedback, see Table 14 and register R_HPT_C1).

When internally supplied by the receiver, the HP-RDI bit generation and coding is configurable via register R_HPT_C1. Intel IXF6048 supports both enhanced or not enhanced HP-RDI (configurable via register T_HPT_OPC). The following defects in the receiver may generate an HP-RDI:

- AU-AIS: pointer in AIS.
- LOP: Loss Of Pointer.
- UNEQ: Unequipped alarm. Its consequence on RDI may be disabled; see register R_HPT_C1.
- J1MSMtch: Trace Identifier Mismatch. Its consequence on RDI may be disabled.
- SLM: Signal Label Mismatch. Its consequence on RDI is configurable as a connectivity or a payload defect. It may also be disabled.
- LCD: Loss Of ATM Cell Delineation. Its consequence on RDI may be disabled.

Table 14. G1x RDI Bit Coding

G1[3:1] RDI Bits Coding (Non Enhanced-RDI)		G1[3:1] RDI Bits Coding (Enhanced-RDI)	Meaning	Triggered by	Priority
ITU	JT				
'000'	'011'	'001'	No Remote Defect	No Remote Defect	0
'100'	'111'	'101'	Remote Defect (Server)	AU-AIS, LOP, LOPC[1]	1
'100'	'111'	'110'	Remote Defect (Connectivity)	UNEQ[1], TIM[1], SLM[2]	2
'100'	'111'	'010'	Remote Defect (Payload)	SLM[2], LCD[1]	3

NOTES:
1. If insertion of HP-RDI is enabled on this specific active alarm. See register definition R_HPT_C1 and R_MSA_C.
2. When insertion of HP-RDI is enabled on SLM active alarm, this may be configured as either a Connectivity or a Payload defect. See register definition R_HPT_C1.

When the HPT-RDI is inserted in the transmit frame, following a defect detected in the receiver, its value is kept stable for at least 'N' consecutive frames. This number of frames is configurable via register T_HPT_OPC with 'N' being 20, 10, 5, or 1. This is relevant for both enhanced and non-enhanced RDI.

In the case of automatic insertion from the receiver, the G1 Spare bit (G1[0]) value is set to the Transmit Overhead default value ('0').

4.4.2.1.6 H4 Byte: Unused

The H4 source is specified by register T_HPT_C, combined with input control pin TPOHINS, as coming from:

- The serial TPOH interface (TPOH input pin).
- The incoming byte from the downstream data—when **all POH** bytes are configured in pass-through mode.
- The H4 internal default transmit value ('0')

4.4.2.1.7 F2 Byte: Order Wire Channel (Optional)

The F2 source is specified by register T_SC_RSOH, combined with input control pin TPOHINS, as coming from:

- The 64-Kbit/s dedicated serial TPOW1 input port.
- The serial TPOH interface (TPOH input pin).
- The incoming byte from the downstream data—when **all POH** bytes are configured in pass-through mode.
- The internal common unused Overhead byte transmit default value (all ‘0’s).

4.4.2.1.8 Z3/F3 Byte: Order Wire Channel (Optional)

The F3/Z3 source is specified by register T_HPT_C, combined with input control pin TPOHINS, as coming from:

- The 64-Kbit/s dedicated serial TPOW2 input port.
- The serial TPOH interface (TPOH input pin).
- The incoming byte from the downstream data—when **all POH** bytes are configured in pass-through mode.
- The internal common unused Overhead byte transmit default value (all '0's).

4.4.2.1.9 Z4/K3, Z5/N1 Bytes: Unused

Those POH bytes are normally unused. Their source is specified by register T_HPT_C, combined with input control pin TPOHINS, as coming from:

- The serial TPOH interface (TPOH input pin).
- The incoming byte from the downstream data—when **all POH** bytes are configured in pass-through mode.
- The internal common unused Overhead byte transmit default value (all '0's).

4.4.2.1.10 STS-1/STM-0 Stuff Columns

In OC-1 mode, the 30th and 59th columns of the STS-1-SPE (designated as “stuff columns”) can be configured via register T_HPT_C to be part of the payload or not. When configured as stuff columns, their contents are not part of the B3 BIP calculation, as they are not part of the VC-3. These bytes are unused. When configured to be part of the payload, these bytes transport regular traffic.

4.4.2.2 Transmit Multiplexer Section Adaptation Function

4.4.2.2.1 AU Pointer Generator

The inserted transmit AU pointer value (first H1 and H2 bytes) is a fixed value. The value is set via register T_AU_PTS. It can be programmed to any value between 0 and 782. Invalid pointer values (between 783 and 1023) may also be set via this register. For 155 Mb/s, 622 Mb/s, and 2.5 Gb/s modes of operation, the unused H1 and H2 bytes indicate concatenation. The two SS bits are also fully programmable via register T_AU_PTS. By default the four NDF bits are set to a value of '0110' (no NDF).

The transmit current AU pointer value is accessible via register T_CAU_PT. Note that this value may be different from the programmed (register T_AU_PTS) value, if some pointer movement has been generated via the microprocessor (see Section 4.4.2.2.2).

4.4.2.2.2 Testing Features: Transmit AU Pointer Operations

For testing purposes, positive or negative pointer movements, as well as NDF indication (NDF transmit bits are set to '1001'), may be generated via the microprocessor (see AU pointer operational configuration register T_AU_PTS). The Intel IXF6048 only allows the generation of consecutive pointer movements separated by at least 4 frames.

In the case of a concatenated payload, it is possible to invert the concatenation indication value in the unused H1 bytes via configuration register T_HPT_OPC.

4.4.2.2.3 AU-AIS Insertion

It is possible to force AU-AIS (all '1's into AU) via register T_HPT_OPC.

4.4.2.3 Multiplexer Section Transmitter

The multiplexer section inserts the MSOH overhead bytes into the transmit frame.

Note that in the case of a regenerator, all the received MSOH bytes are passed through unchanged.

4.4.2.3.1 B2 Byte(s) Interleaved Parity

The B2 bytes (BIP-8 in OC-1 mode, BIP-24 in OC-3 mode, BIP-96 in OC-12 mode, and BIP-384 in OC-48 mode) are provided by one of three sources configured in register T_SC_MSOH, combined with input serial bus control pin TSOHINS:

- The serial TSOH interface (TSOH input pin).
- The incoming byte from the downstream data—when **all internally Processed MSOH (B2, K1, K2, S1 and M1)** bytes are configured in pass-through mode).
- The BIP-8/24/96/384 internal calculation on the previous concatenated payload (default setting). For testing purposes, it is possible to invert the B2 value via software configuration (see register T_RMST_OP). The B2 value can be inverted for a single frame (8/24/96/384 errors) or for an indefinite duration.

4.4.2.3.2 K1 and K2 Automatic Protection Channel Bytes and MS-RDI

These bytes are assigned for APS signaling and the transmission of a Multiplex Section Remote Defect Indication.

The **K1** source is specified by register T_SC_MSOH, combined with input serial bus control pin TSOHINS, as coming from:

- The serial TSOH interface (TSOH input pin).
- The serial Transmit Section Alarm port (TSAL input pin).
- The incoming byte from the downstream data—when **all internally Processed MSOH (B2, K1, K2, S1, and M1)** bytes are configured in pass-through mode.

— An internal register (register MP_TK2K1) programmed by the microprocessor (default setting).

The **K2-APS** source is specified by register T_SC_MSOH, combined with input serial bus control pin TSOHINS, as coming from:

— The serial TSOH interface (TSOH input pin).

— The serial Transmit Section Alarm port (TSAL input pin).

— The incoming byte from the downstream data—when **all internally Processed MSOH (B2, K1, K2, S1 and M1)** bytes are configured in pass-through mode.

— An internal register (MP_TK2K1) programmed by the microprocessor (default setting).

The **K2-MS-RDI** source is specified by register T_SC_MSOH, combined with input serial bus control pin TSOHINS, as coming from:

— The serial TSOH interface (TSOH input pin, in which case the K2-APS bits are also updated from the TSOH input).

— The serial Transmit Section Alarm port (TSAL input pin).

— The incoming byte from the downstream data—when **all internally Processed MSOH (B2, K1, K2, S1 and M1)** bytes are configured in pass-through mode, in which case, the K2-APS bits are also updated from the same source.

— An internal register (register MP_TK2K1) programmed by the microprocessor, in which case the K2-APS bits are also updated from register MP_TK2K1.

— A microprocessor force command (register R_MST_C). The K2[2:0] RDI bits take a value of '110', see Table 15.

— Receiver section defect. Automatic insertion of the RDI output from the receiver, internally looped back. The K2[2:0] RDI bits take a value of '110', see Table 15.

— TSAL input alarm bus. The K2[2:0] RDI bits take the value of K2-APS.

— Register MP_TK2K1. The K2[2:0] RDI bits take the value of K2-APS.

Table 15. K2 RDI Bit Coding

K2[2:0] RDI Bits Coding	Meaning	Triggered by
'000'	No Remote Defect	No Remote Defect
'110'	Remote Defect	MS-AIS, EED[1] Microprocessor[2]

NOTES:
1. The Excessive Error Defect trigger can be disabled via register R_MST_C.
2. It is possible to force insertion of RDI by configuring register R_MST_C.

When MS-RDI is inserted in the transmit frame, following a defect detected in the receiver, it remains active for at least ‘N’ consecutive frames. This number of frames is configurable via register T_SC_MSOH with ‘N’ being 20, 10, 5, or 1.

4.4.2.3.3 S1 Byte: Synchronization Status

The S1[3:0] bits are allocated for Synchronization Status Messages. The S1 source is specified by register T_SC_MSOH, combined with input serial bus control pin TSOHINS, as coming from:

— The serial TSOH interface (TSOH input pin).

— The incoming byte from the downstream data—when **all internally Processed MSOH (B2, K1, K2, S1 and M1)** bytes are configured in pass-through mode.

— An internal register (MP_TS1) programmed by the microprocessor (default setting).

4.4.2.3.4 M1 Byte: MS-REI

This byte is allocated for the Multiplex Section Remote Error Indication. The M1 source is specified by register T_SC_MSOH, combined with input serial bus control pin TSOHINS, as coming from:

— The serial TSOH interface (TSOH input pin).

— The serial Transmit Section Alarm port (TSAL input pin).

— The incoming byte from the downstream data—when **all internally Processed MSOH (B2, K1, K2, S1 and M1)** bytes are configured in pass-through mode.

— The internal processing configured by (T_SC_MSOH. The M1[7:0] REI bits can be provided by the detected B2 errors from the receiver or disabled (set to '0000000'). If not used, the MSB undefined bits are always set to '0'. The transmit Remote Error Indication (based on B2 BIP detected errors) can be inserted as BIP or Block errors. This is configured by register R_MST_C.

4.4.2.3.5 D4 to D12 Bytes: Data Communication Channel

The D4-D12 byte source is specified by the register T_SC_MSOH, combined with input serial bus control pin TSOHINS, as coming from:

— The serial TSOH interface (TSOH input pin).

— A dedicated 576-Kbit/s serial interface (TMD input pin). A 576-KHz clock output is provided at pin TMDC.

— The incoming byte from the downstream data (possible in non repeater mode only).

— The internal common unused Overhead byte transmit default value (all '0's).

4.4.2.3.6 E2 Byte: Orderwire (Optional)

This byte may be used to provide orderwire channel for voice communication channel. The E2 byte source is specified by global register OHPCNF, register T_SC_MSOH, combined with input serial bus control pin TSOHINS, as coming from:

— The serial TSOH interface (TSOH input pin).

— A dedicated 64-Kbit/s serial interface (TMOW input pin). A 64-KHz clock output and an 8-KHz sync are provided at pin TOWC and TOWBYC.

— The incoming byte from the downstream data (possible in non repeater mode only).

— The internal common unused Overhead byte transmit default value (all '0's).

— The “Quiet” default value for orderwire channel dedicated to voice communication. This default value is '01111111'.

4.4.2.3.7 Undefined MSOH Bytes

The undefined MSOH bytes of the ATM/POS physical layer are unused. Their source is specified by register T_SC_MSOH, combined with input serial bus control pin TSOHINS, as coming from:

- The serial TSOH interface (TSOH input pin).
- The incoming byte from the downstream data. Only possible in non repeater mode. In this case, **all undefined MSOH** bytes are configured in pass-through mode.
- The internal common unused Overhead byte transmit default value (all '0's).

4.4.2.4 Regenerator Section Transmitter

The Regenerator section inserts the RSOH overhead bytes. In a repeater configuration, the received RSOH byte (except A1, A2, and B1) can be in a group or passed through individually, unchanged.

4.4.2.4.1 A1 and A2 Framing Bytes

The frame keyword bytes are always regenerated in the Intel IXF6048 transmitter regardless of the configuration. For testing purposes, it is possible to invert A1 value (via register T_RMST_OP). The A1 value can be inverted for four frames only (to generate an OOF alarm for 2 frames in the receiver) or for an indefinite duration.

These bytes may also be sourced from the TSOH serial bus input, when this interface is enabled and the TSOHINS control input pin is set high on the framing byte time slots.

4.4.2.4.2 The Regenerator Section Trace J0

This byte is inserted to repetitively transmit a Section Access Identifier so that a section receiver can verify its continued connection to the intended transmitter.

The J0 string length is configurable via register T_RMST_OP to be either a 1-byte, a 16-byte (with CRC-7), or a 64-byte trace message. When configured as a 16-byte message, the 16-byte expected J0 string value needs to have the correct CRC-7 bits per G.707 specifications.

J0 is provided by one of the three sources configured in register T_SC_RSOH, combined with input serial bus control pin TSOHINS:

- The serial TSOH interface (TSOH input pin).
- The incoming byte from the downstream data (The received byte (Repeater mode) from the Regenerator Section receiver).
- An internal RAM (up to 64-bytes).

The RAM is accessed via register T_J0_STRA. Note that a complete 16-byte string, with CRC-7, is required by the ITU for proper operation.

Compatibility of J0 with in-service equipment can be provided by either writing a value into the transmit J0 RAM (when configured in 1-byte string length mode) or by setting J0 byte to its default value 01H (if not used, or as former C1 byte), via register T_RMST_OP.

4.4.2.4.3 B1 BIP-8 Byte

The B1 byte is always regenerated in the Intel IXF6048 transmitter. This byte is used for the Regenerator Section error monitoring function. It is the result of a BIP-8 calculation done on the previously scrambled frame and is inserted into transmit RSOH before scrambling. For testing purpose, it is possible to invert the B1 value (register T_RMST_OP). The B1 value can be inverted either for a single frame (8 errors), or indefinitely.

The B1 byte may also be sourced from the TSOH serial bus input, when this interface is enabled and TSOHINS control input pin is set high on the B1 time slot.

4.4.2.4.4 Z0/NU (Bytes Reserved for a National Use) Bytes of the First Row of the RSOH

The Z0/NU bytes are located in row number one of the RSOH. Register T_SC_RSOH, combined with input serial bus control pin TSOHINS, specify the source of these bytes. The possibilities are:

- The serial TSOH interface (TSOH input pin).
- The incoming byte from the downstream data, i.e., the received byte from the Regenerator Section receiver. In this case, **all Z0/NU bytes of the first SOH row** are configured in pass-through mode.
- Internal hardware processing. In this case, register T_RMST_OP configures the value of these transmit bytes to be the default value of unused OH bytes (all '0's), the default value xAAH (as those byte are unscrambled), or the previous STS-1 ID definition (former C1 time slots 2 through N), for interworking with older equipment. In the last case, in an STS-12c framing mode, value 02H is set in the first Z0, 03H in the second Z0, 04H in the third one, and so on, until value 0CH in the eleventh Z0 byte.

4.4.2.4.5 D1 to D3 Bytes: Data Communication Channel

The D1-D3 byte source is specified by global configuration register OHPCNF and register T_SC_RSOH, combined with input serial bus control pin TSOHINS, as coming from:

- The serial TSOH interface (TSOH input pin).
- A dedicated 192-Kbit/s serial interface (TRD input pin). A 192-KHz clock output is provided at pin TRDC.
- The incoming byte from the downstream data, i.e., the received byte from the Regenerator Section receiver.
- The internal common unused Overhead byte transmit default value (all '0's).

4.4.2.4.6 E1 Byte: Orderwire Channel (Optional)

This byte may be used to provide orderwire channel for voice communication channel. The E1 byte source is specified by global configuration register OHPCNF and register T_SC_RSOH, combined with input serial bus control pin TSOHINS. The source can be either:

- The serial TSOH interface (TSOH input pin).
- A dedicated 64-Kbit/s serial interface (TROW input pin). A 64-KHz clock output and an 8-KHz sync are provided at pin TOWC and TOWBYC.
- The incoming byte from the downstream data The received byte from the Regenerator Section receiver.

— The internal common unused Overhead byte transmit default value (all '0's).

— The “Quiet” default value for orderwire channel dedicated to voice communication. This default value is '01111111'.

4.4.2.4.7 F1 Byte: Orderwire Channel (Optional)

This byte is reserved for user purposes. It can be used as extra maintenance orderwire channel. The F1 byte source is specified by global register OHPCNF and register T_SC_RSOH, combined with input serial bus control pin TSOHINS. The source can be either:

— The serial TSOH interface (TSOH input pin).

— A dedicated 64-Kbit/s serial interface (TDOW input pin). A 64-KHz clock output and an 8-KHz sync are provided at pin TOWC and TOWBYC.

— The incoming byte from the downstream data (The received byte (Repeater mode) from the Regenerator Section receiver).

— The internal common unused Overhead byte transmit default value (all '0's).

4.4.2.4.8 NU Bytes (Bytes Reserved for a National Use) of the Second Row of the RSOH: Unused

These NU bytes are located in row number two of the RSOH. Register T_SC_RSOH specifies the source of these bytes. The possibilities are:

— The serial TSOH interface (TSOH input pin).

— The incoming bytes from the downstream data (The received byte (Repeater mode) from the Regenerator Section receiver). In this case, **all NU bytes of the second SOH row** are configured in pass-through mode.

— The internal common unused Overhead byte transmit default value (all '0's).

4.4.2.4.9 UN Bytes: Undefined RSOH Bytes

These RSOH bytes are normally unused, including the SDH Media Dependent bytes. Register T_SC_RSOH specifies the source of these bytes. The possibilities are:

— The serial TSOH interface (TSOH input pin).

— The incoming bytes from the downstream data (The received byte (Repeater mode) from the Regenerator Section receiver). In this case, **all RSOH undefined bytes** are configured in pass-through mode.

— The internal common unused Overhead byte transmit default value (all '0's).

4.4.2.4.10 Scrambler

After inserting the RSOH bytes, the data is scrambled. The ITU Standard scrambler is 2^7 - 1. The data scrambling can be disabled via register T_RMST_OP.

4.4.2.4.11 External Frame Synchronization

The Intel IXF6048 provides an external frame pulse reference when configured in single processor mode with a parallel interface (output pin TFPO). It is an 8-KHz reference signal with a pulse duration of 6.4 ns (OC-48) or 12.8 ns (OC-12). This pulse is used to identify the position of the frame start. The pulse's position is programmable, relative to the A1A2 bytes. This signal is synchronous with the output transmit frame clock.

4.4.2.4.12 Transmit Frame Alignment

The transmit frame can be synchronized by using an external 8-KHz reference connected to the TFPI input pin (except in repeater mode, in which case, it is locked to the received frame). This input signal is active-high and can be either a square wave or a pulse.

This feature can be used by an Upper Level Multiplexer (OC-192) to align several Intel IXF6048 chips. The alignment can be done by cascading the reference signals (output pin TFPO of chip #2 connected to input pin TFPI of chip #3, etc.).

If TFPI is not used, it **must** be tied to GND.

4.4.2.5 Clock Distribution and Reference

Depending on the chip configuration, the source of the Transmit Clock references may be different.

- Repeater Mode: the transmit clock source is always coming from the receiver (RPCI/RSCI).
- Multiplexer Mode: the transmit clock source is either the receiver clock (RPCI/RSCI) or the transmit local reference (Blue) clock input (global TCCI or the per channel local reference inputs TPCI_i/TSCI_i).

4.5 Overhead Bytes and Alarms Serial Access

4.5.1 Section OverHead Access

4.5.1.1 Transmit Side: TSOH Serial Bus

The transmit side of the SOH serial interface allows insertion of each SOH byte into the transmit MSOH and RSOH via up to four serial contradirectional interfaces. Each interface is dedicated to a specific OC-1, OC-3c, or OC-12c channel and the four of them may be used for an OC-48 or OC-12 (non concatenated STM-4) application.

For each interface, the reference clock is supplied by TSOHCK[i] at:

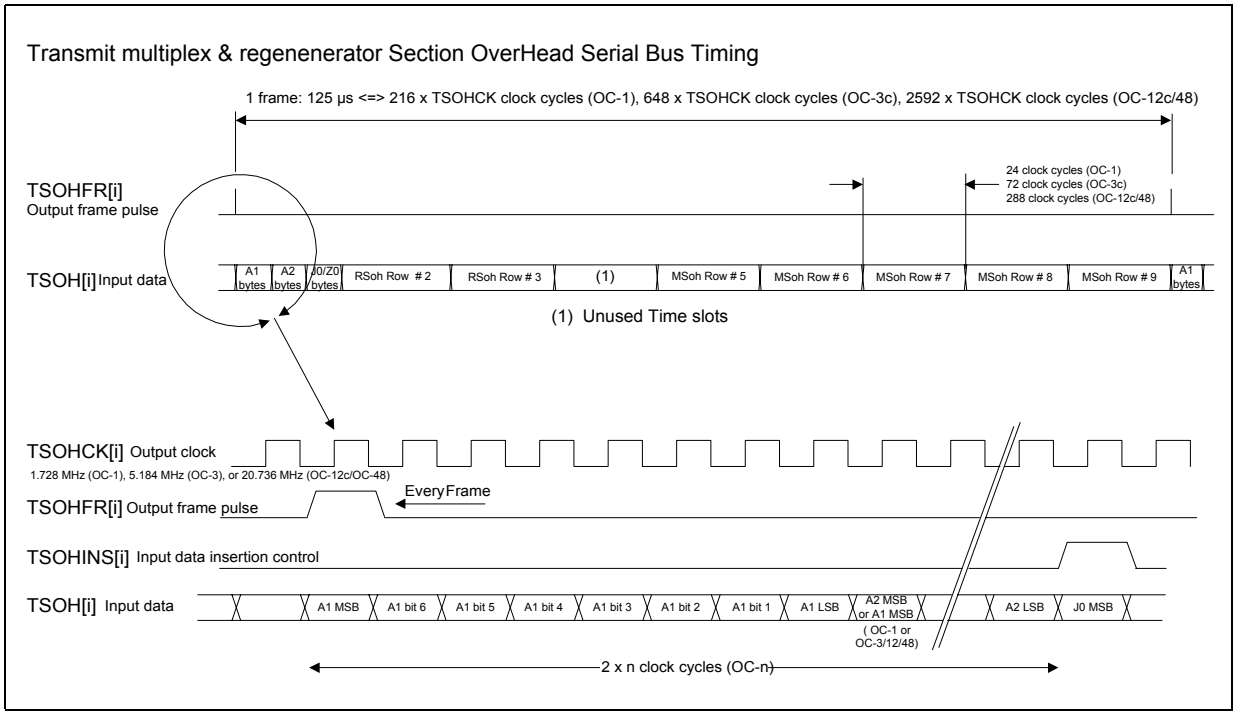
- 1.728 MHz if channel[i] is in OC-1 mode (up to 27 bytes/time slots)
- 5.184 MHz if channel[i] is in OC-3c mode (up to 81 bytes/time slots)
- 5.184 MHz in OC-12 mode (non concatenated STM-4; the four interfaces are used to access the full OC-12 SOH, column by column: up to 4 x 81 bytes/time slots).
- 20.736 MHz if channel [i] is in OC-12c mode (up to 324 bytes/time slots).
- 20.736 MHz in OC-48 mode (the four interfaces are used to access the full OC-48 SOH, column by column: up to 4 x 324 bytes/time slots).

TSOHCK[i] is synchronous with the transmit clock. Frame pulse output TSOHFR[i] indicates the start of the frame (A1 MSB position). The SOH bytes are transported serially in the same order as in the SONET/SDH frame, MSB first. As row four of the SONET/SDH frame doesn't include any SOH (pointer location), the corresponding time slots in the TSOH serial bus remains unused.

The Intel IXF6048 latches the data on the TSOH pin, synchronized with the timing signals. If the TSOHINS input insert control pin is high at the MSB location of a specific SOH byte in the TSOH bus, this value is inserted into the transmit frame and output from the Intel IXF6048 one SDH row after it is latched. If the TSOHINS input control pin is low at the MSB location of a specific SOH byte in the TSOH bus, the transmit value of this byte comes from the source specified by the configuration registers T_SC_RSOH and T_SC_MSOH (default value, internal hardware process, microprocessor, dedicated serial accesses, or received byte).

When the TSOHINS insert control pin is enabled via the microprocessor interface (TSOHINS_Ena = '1' in register T_SC_RSOH[15]), it takes precedence over any software configuration regarding the SOH bytes transmit source. If the TSOHINS insert control pin is disabled via the microprocessor interface (TSOHINS_Ena = '0' in register T_SC_RSOH[15]), then the transmit SOH bytes cannot be sourced from the TSOH serial interface.

Figure 13. Transmit TSOH Serial Bus Timing



4.5.1.2 Receive Side: RSOH Serial Bus

The Receive side SOH interface provides all the signals necessary to collect the RSOH and MSOH receive bytes via the serial codirectional interfaces (up to four) described below.

- Frame pulse RSOHFR[i] indicates the start of the frame (A1 MSB position). It is repeated every 125 µs.
- The RSOHCK[i] clock is used for clocking the RSOH[i] output.
- The data is output on the RSOH[i] pin, one SDH row after it is received (13.9 µs delay).

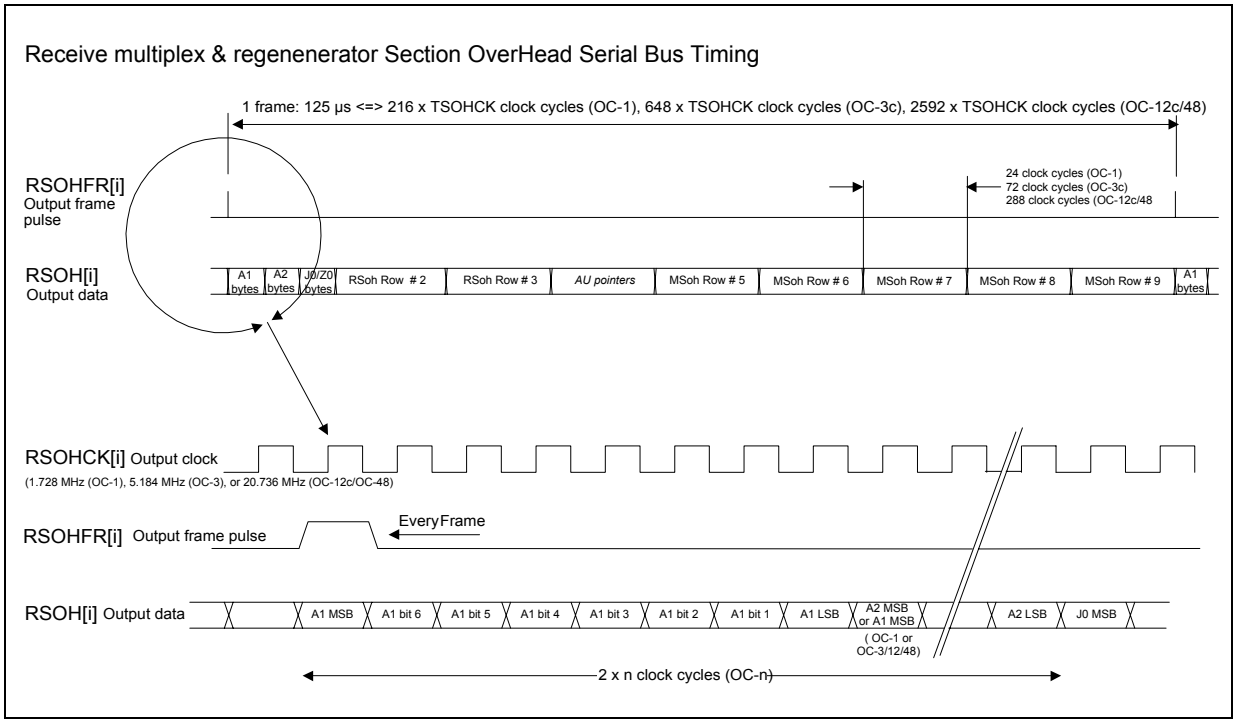
Each interface is dedicated to the transport of a specific OC-1, OC-3c, or OC-12c channel SOH and the four of them may be used for an OC-48 or OC-12 (non concatenated STM-4) application.

RSOHCK[i] clock frequency is at:

- 1.728 MHz if channel[i] is in OC-1 mode.
- 5.184 MHz if channel[i] is in OC-3c mode.
- 5.184 MHz in OC-12 mode (non concatenated STM-4). The four interfaces are used to access the full OC-12 SOH in 4 columns.
- 20.736 MHz if channel [i] is in OC-12c mode.
- 20.736 MHz in OC-48 mode. The four interfaces are used to access the full OC-48 SOH, in 4 columns.

Even if they are not part of the SOH, the received AU pointer bytes are serially supplied at the RSOH output.

Figure 14. Receive RSOH Timing



4.5.2 Higher Order Path OverHead Access

4.5.2.1 Transmit Side: TPOH Serial Bus

The transmit side of the POH serial interface allows insertion of each POH byte, or some bit of a byte, into the transmit HPOH via a serial contradirectional interface. As it can process four independent paths, Intel IXF6048 provides up to four TPOH interfaces (one per channel or concatenated higher order VCs).

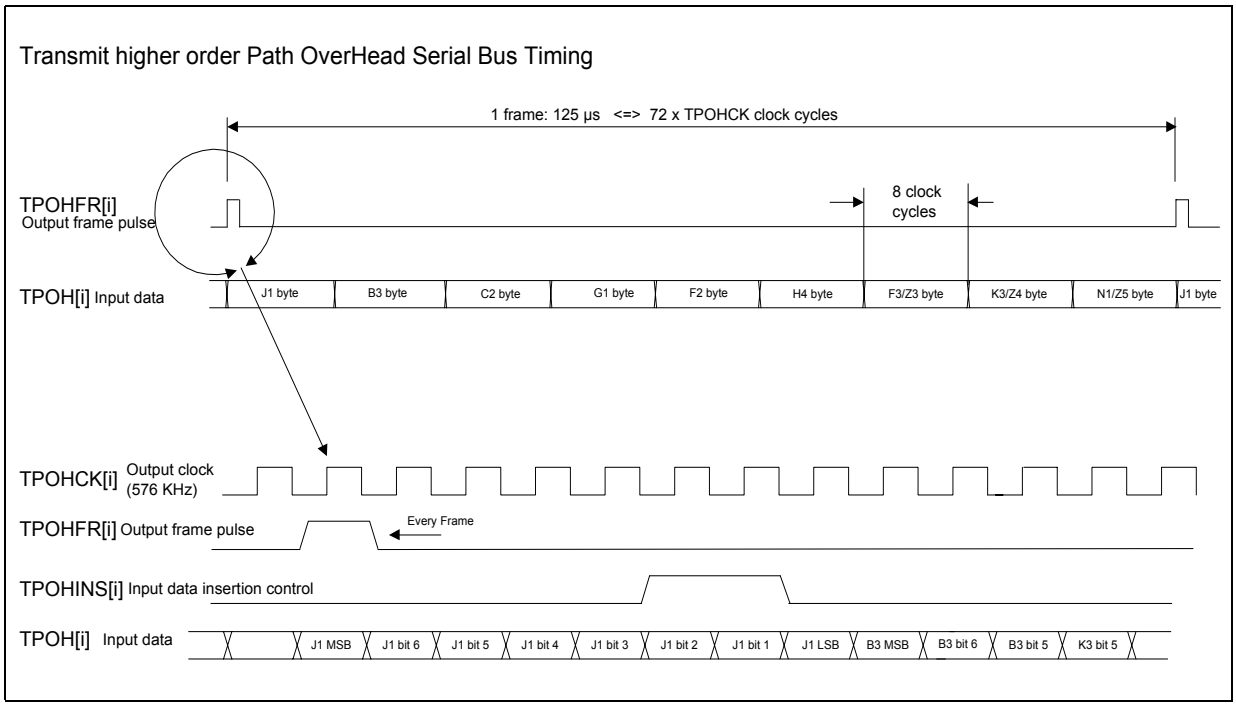
For each interface, the reference clock is supplied by TPOHCK[i] at 576-KHz. TPOHCK[i] is synchronous with the transmit Higher Order Payload rate.

Frame pulse output TPOHFR[i] indicates the expected presence of J1 MSB at TPOH input. It is repeated every 125 µs.

The Intel IXF6048 latches the data on the TPOH pin, synchronized with the timing signals. If the TPOHINS input insert control pin is high at any bit location of a specific POH byte in the TSOH input bus, this bit value is inserted into the transmit POH byte and output from the Intel IXF6048. If the TPOHINS input control pin is low at the bit location of a specific POH byte in the TPOH input bus, the transmit bit value of this POH byte comes from the source specified by configuration register T_HPT_C (default value, internal hardware process, microprocessor, dedicated serial accesses, or received byte).

When the TPOHINS insert control pin is enabled via the microprocessor interface (TPOHINS_Ena = '1' in register T_HPT_C[15]), it takes precedence on any software configuration regarding the POH bytes transmit source; TPOHINS control logic is based on a bit-per-bit insertion from the TPOH serial input. If the TPOHINS insert control pin is disabled via the microprocessor interface (TPOHINS_Ena = '0' in register T_HPT_C[15]), then the transmit POH bytes cannot be sourced from the TPOH serial interface.

Figure 15. Transmit HPOH Serial Bus Timing



4.5.2.2 Receive Side: RPOH Serial Bus

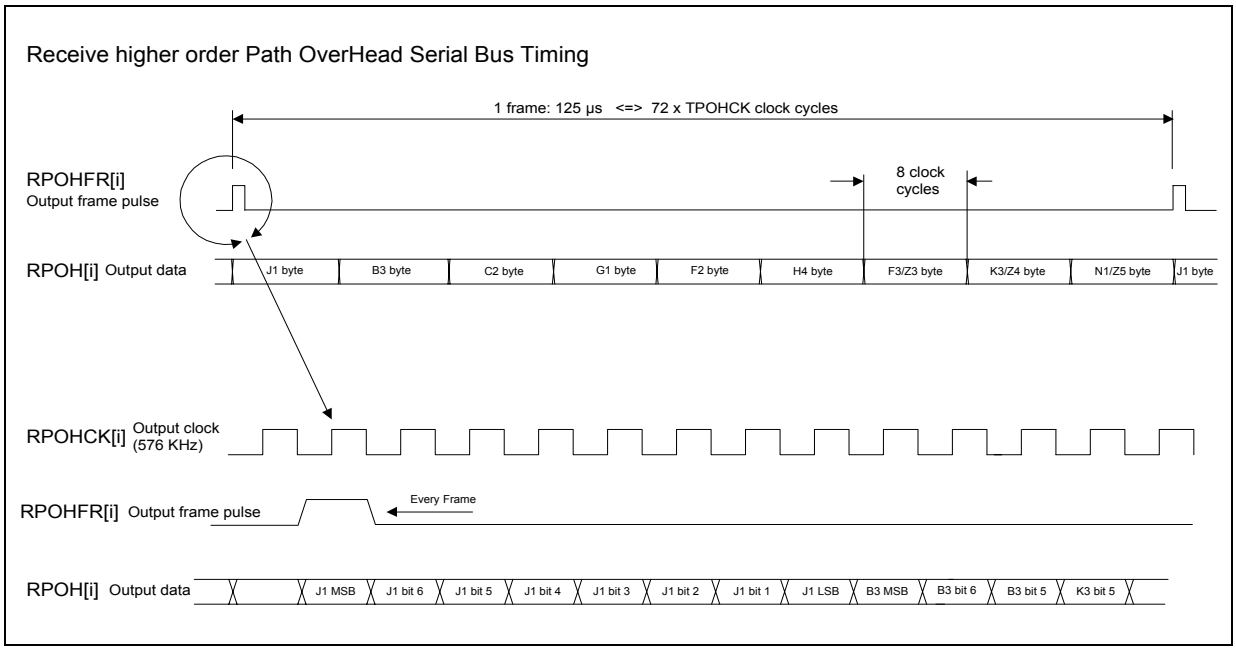
The Receive side POH interface provides all the signals necessary to serially collect the POH receive bytes via the serial codirectional interfaces (up to four) described below.

- Frame pulse RPOHFR[i] indicates the presence of J1 MSB at RPOH output. It is repeated every 125 µs.
- The RPOHCK[i] reference clock at 576-KHz is used for clocking the RPOH[i] output.

— The data is output on the RPOH[i] pin.

— Each of the four interfaces is dedicated to accessing the nine POH bytes of a specific channel. Intel IXF6048 processes up to four independent higher order paths.

Figure 16. Receive HPOH Serial Bus Timing



4.5.3 Section (Line) Alarms, APS and Ring Bus

4.5.3.1 Receive Side: RSAL Serial Bus

The Receive side section alarms port provides all the signals necessary to serially collect the section alarms, the detected section errors, the generated remote defects, the receive filter K1 and K2 APS bytes, and the filtered S1 SSM via a serial codirectional interface.

As it can process four independent sections (four channels), Intel IXF6048 provides up to four RSAL interfaces (one per channel). For each channel, RSAL[i] provides the following detected alarms and information:

— Loss Of Signal (LOS)

— Out Of Frame (OOF)

— Loss Of Frame (LOF)

— Section Trace Identifier Mismatch (RS-TIM)

— Section Trace Unstable (J0Unstable)

— Section Trace CRC-7 alarm (J0CRC7Err)

— Excessive Error Defect (EED)

— Degraded Signal Defect (DSD)

— Multiplex Section AIS (MS-AIS in K2)

- Detected Remote Defect Indication (RDI in K2)
- Signal Fail Alarm (SF)
- B1 receive detected errors (coded on 4 bits)
- AIS signal inserted at the regenerator section level (DRSTAIS)
- AIS signal inserted at the multiplexer section Termination level (DMSTAIS)
- AIS signal inserted at the multiplexer section Adaptation level (DMSAAIS).

RSAL[i] gives access to all the necessary information needed to externally process the APS protocol:

- K1 APS receive filtered value
- K2 APS receive filtered value
- Receive K1 unstable alarm (APS defect)
- Receive K2 unstable alarm
- K1 receive filtered value change detection (high for a frame when a different filtered K1 value is output).
- K2 receive filtered value change detection (high for a frame when a different filtered K2 value is output). Note that with a specific software configuration, this may indicate a change of both K1 and K2 APS—see register R_MST_C).

RSAL[i] may be configured as a ring port by connecting directly to the transmit alarm port (TSAL input) of another Intel IXF6048 chip. The Line RDI (MS-RDI) and line REI (MS-REI) information is now externally fed back. Therefore, the internal chip feedback of the remote defects is disabled. For this purpose, it provides:

- The encoded detected receive B2 error as an REI.
- The generated RDI based on the detected major defect in the receiver.
- Finally, RSAL[i] gives access to the Synchronization Status Messages:
- S1 SSM receive filtered value.
- Receive S1 unstable alarm (SSM defect).
- S1 receive filtered value change detection (high for a frame when a different filtered S1 value is output).

For data error checking of the RSAL serial bus, especially in the case of a ring port type of application, a CRC-4 calculation is performed over the entire RSAL frame. The result is then inserted in the last four bits of the same RSAL frame (bit 1 is inserted first). The 4-bit CRC-4 word is the remainder after multiplication by X^4 and then division (modulo 2) by the generator polynomial $X^4 + X + 1$.The CRC-4 bits are replaced by '0's during computation. The default value of the unused bits is also '0'. The RSAL serial output then outputs 68 bits of information followed by 4 bits of code redundancy (CRC-4) between two consecutive frame pulses.

The RSAL interface is described below.

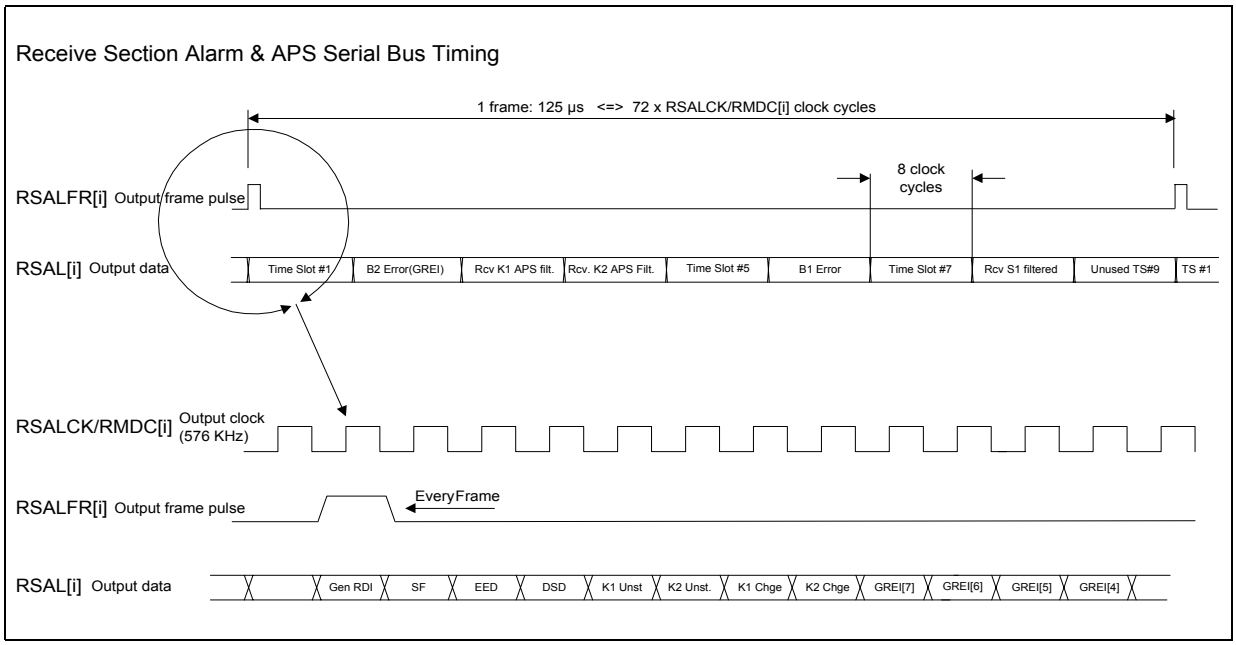
- Frame pulse RSALFR[i] indicates the position of the generated RDI bit at RSAL output. It is repeated every 125 µs (every 72 clock cycles of TMDC/RSALCK[i] clock).
- The TMDC/RSALCK[i] reference clock at 576-KHz is used for clocking the RSAL[i] output. Note that this clock is the same one used for DCC (D4-D12).

— The data is output on the RSAL[i] pin. See Table 16 for the bus format.

Table 16. RSAL[i] Bus Frame

RSALFR[i] Status	Time Slot #	Bit Position	Content	Port Type
High	1	1	Generated RDI	Ring port
Low (See Figure 17)		2	SF	APS/Alarm port
		3	EED	APS/Alarm port
		4	DSD	APS/Alarm port
		5	K1 Unstable	APS port
		6	K2 Unstable	APS port
		7	K1 Change	APS port
		8	K2 Change	APS port
	2	1:8	B2 Encoded Error/Generated REI [7:0]	Ring port
	3	1:8	K1[7:0] filtered APS	APS port
	4	1:8	K2 [7:0] filtered APS	APS port
	5	1	Reserved	APS
		2	LOS	Alarm port
		3	OOF	Alarm port
		4	LOF	Alarm port
		5	RS-TIM	Alarm port
		6	J0Unstable	Alarm port
		7	J0CRC7Err	Alarm port
		8	MS-AIS	Alarm port
	6	1:4	Unused	
		4:8	B1 Encoded Detected Error [3:0]	Alarm port
	7	1	DRSTAIS	Alarm port
		2	DMSTAIS	Alarm port
		3	DMSAAIS	Alarm port
		4	Detected RDI in K2	Alarm port
		5	S1Unstable	SSM port
		6	S1 Change	SSM port
		7:8	Unused	
	8	1:8	S1[7:0] filtered SSM	SSM port
	9	1:4	Unused	
		5	CRC-4 bit 1	Control (for error check)
		6	CRC-4 bit 2	Control (for error check)
		7	CRC-4 bit 3	Control (for error check)
		8	CRC-4 bit 4	Control (for error check)

Figure 17. Receive Section Alarm and APS Serial Bus Timing



4.5.3.2 Transmit Side: TSAL Serial Bus

The transmit side of the serial Alarm and APS interface allows insertion of the remote defect information (MS-RDI and MS-REI) feedback from the receive, and/or the insertion of the APS bytes K1 and K2 into the transmit SOH via a serial co- or contra-directional interface. As it can process four independent sections, Intel IXF6048 provides up to four TSAL interfaces (one per channel). The co- or contra-directional mode is configured via register T_SC_MSOH.

Contradirectional Interface: This mode simplifies the external processing of the APS protocol as the timing is supplied by the Intel IXF6048.

- The reference clock is supplied by TSALCK[i] at 576-KHz. TSALCK[i] is synchronous with the frame rate.
- Frame pulse output TSALFR[i] indicates the expected presence of RDI at TSAL input. It is repeated every 125 µs.
- The Intel IXF6048 latches the data on the TSAL pin, synchronized with the output timing signals.

Codirectional Interface: This allows a direct connection from the RSAL output port of an Intel IXF6048 chip to the TSAL input port of a second Intel IXF6048 chip, to provide external feedback of both RDI and REI defects from receive to transmit.

- The clock is input on TSALCK[i] at 576-KHz.
- Frame pulse input TSALFR[i] indicates the expected presence of RDI at TSAL input. It is repeated every 125 µs.
- The Intel IXF6048 latches the data on the TSAL pin, using the input timing signals. As TSALCK[i] might not be synchronous with the transmit frame rate, some information may be lost once in a while, due to the frequency deviation.

For each channel, TSAL[i] provides the following information regarding the transmit APS:

— K1 APS input value.

— K2 APS input value.

TSAL[i], when configured as a ring port, is used to input the line RDI (MS-RDI) and line REI (MS-REI) information from an external source. In this case, the internal feedback of the remote defects is disabled. For this purpose, it provides:

— The generated REI value to be transmitted.

— The generated RDI defect to be transmitted.

Configuration register T_SC_MSOH independently specifies the transmit source of K1, K2 APS, K2 RDI, and M1 REI as coming from the TSAL input port or not. Note that the TSAL bus may be used as the transmit source for these bytes only if the TSOHINS input control pin is active-low during these bytes' time slots on the TSOH input bus.

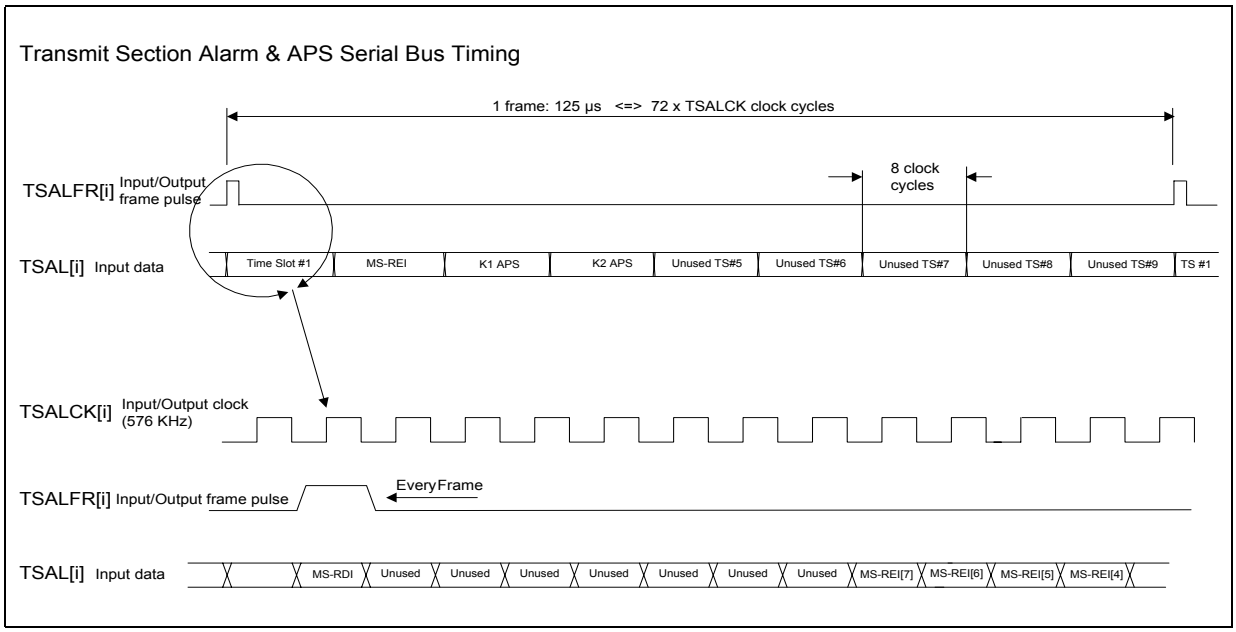
The CRC-4 bits located in the 4 last bits of the TSAL frame are computed for data error checking of the TSAL serial input bus. The CRC-4 calculation is performed over the entire TPAL frame including the unused bits. The 4-bit CRC-4 calculated word is the remainder after multiplication by X^4 and then division (modulo 2) by the generator polynomial $X^4 + X + 1$.The CRC-4 bits are replaced by '0's during computation. The remainder result is then compared on a bit-by-bit basis with the CRC-4 bits received in the last four bits of the same TSAL frame (bit 1 is received first). If the remainder calculated does not correspond to the CRC-4 bits received, then the checked TSAL frame (between 2 consecutive frame pulses) is assumed to have some errors. This detected default sets a maskable interrupt that can be accessed via global register TALBINT.

When TSAL[i] is configured as a codirectional interface, Intel IXF6048 detects the absence of clock (TSALCK[i]) and/or framing pulse (TSALFR[i]) on the incoming timings. If no input framing pulse is detected within 250 µs or there is less then 16 clock cycles within 125 µs, then a maskable interrupt is set that can be accessed via global register TALBINT.

Table 17. TSAL[i] Bus Frame

TSALFR[i] Status	Time Slot #	Bit Position	Content	Port Type
High	1	1	Generated RDI to be transmitted	Ring port
Low (See Figure 18)		2:8	Unused	
	2	1:8	Generated REI [7:0] to be transmitted	Ring port
	3	1:8	K1[7:0] transmit APS	APS port
	4	1:8	K2 [7:0] transmit APS	APS port
	5	1:8	Unused	
	6	1:8	Unused	
	7	1:8	Unused	
	8	1:8	Unused	
	9	1:4	Unused	
		5	CRC-4 bit 1	Control (for data error check)
		6	CRC-4 bit 2	Control (for data error check)
		7	CRC-4 bit 3	Control (for data error check)
		8	CRC-4 bit 4	Control (for data error check)

Figure 18. Transmit Section Alarm and APS Serial Bus Timing



4.5.4 Path Alarms and Ring Bus

4.5.4.1 Receive Side: RPAL Serial Bus

The Receive side path alarms port provides all the signals necessary to serially collect the path alarms, the detected path errors, the filtered receive signal label, and the generated remote defects via a serial codirectional interface.

As it can process four independent paths (four channels), Intel IXF6048 provides up to four RPAL interfaces (one per channel). For each channel, RPAL[i] provides the following detected alarms and information:

- Server Defect (LOP or AU-AIS)
- Loss Of Pointer (LOP)
- Loss Of Pointer Concatenation Indication (LOPC)
- Pointer in AIS (AU-AIS)
- Path Trace Identifier Mismatch (HP-TIM)
- Path Trace Unstable (J1Unstable)
- Path Trace CRC-7 alarm (J1CRC7Err)
- Unequipped detection (UNEQ)
- Signal Label Mismatch (SLM)
- Receive C2 Unstable alarm (unstable SL)
- Detected Remote Defect Indication (RDI in G1)
- Loss Of Cell Delineation (LCD)

- Detected VCAIS alarm (VCAIS)
- AIS signal inserted at the path level (DHPTAIS) S1 SSM receive filtered value.
- C2 receive filtered value change detection (high for a frame when a different filtered C2 value is output)
- C2 receive Signal Label filtered value

RPAL[i] may also be used as a ring port by being connected directly to the transmit alarm port (TPAL input) of another Intel IXF6048 chip, to externally feedback the path RDI (HP-RDI) and path REI (HP-REI) information. In this case, the chip's internal feedback of the remote defects is disabled. For this purpose, it provides:

- The encoded detected receive B3 error as an REI.
- The generated RDI (enhanced or not) is based on the detected major defects in the receiver.

For data error checking of the RPAL serial bus (especially in the case of a ring port type of application), a CRC-4 calculation is performed over the entire RPAL frame; the result is then inserted in the last four bits of the same RPAL frame (bit 1 is inserted first). The 4-bit CRC-4 word is the remainder after multiplication by X^4 and then division (modulo 2) by the generator polynomial $X^4 + X + 1$. The CRC-4 bits are replaced by '0's during computation. The default value of the unused bits is also '0'. The RPAL serial output then outputs 68 bits of information, followed by 4 bits of code redundancy (CRC-4), between two consecutive frame pulses.

The RPAL interface is described below.

- Frame pulse RPOHFR[i] indicates the position of the generated Server Defect bit at RPAL output. It is repeated every 125 µs (72 clock cycles of RPOHCK[i] clock).
- The RPOHCK[i] reference clock, at 576-KHz, is used for clocking the RPAL[i] output. Note that this clock is the same one used for RPOH output.
- The data is output on the RPOH[i] pin. See Table 18 for the bus format.

Figure 19. Receive Path Alarm Serial Bus Timing

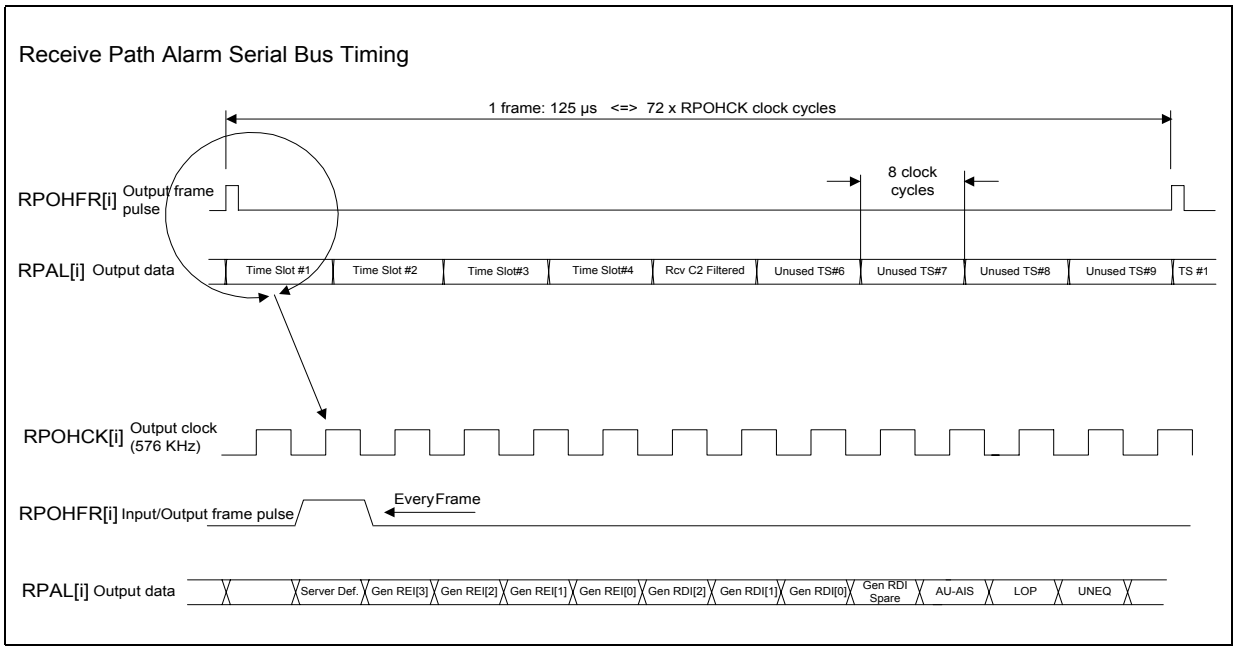


Table 18. RPAL[i] Bus Frame

RPOHFR[i] Status	Time Slot #	Bit Position	Content	Port Type
High	1	1	Server Defect (LOP or AU-AIS) I	Ring port
Low (See Figure 19)		2:5	B3 Encoded Error/Generated REI [3:0]	Ring port
		7	Generated RDI[2]	Ring port
		8	Generated RDI[1:0]	Ring port
	2	1	RDI Spare	Ring port
		2	AU-AIS	Alarm port
		3	LOP	Alarm port
		4	UNEQ	Alarm port
		5	HP-TIM	Alarm port
		6	SLM	Alarm port
		7	LCD	Alarm port
		8	J1Unstable	
	3	1	J1CRC7Err	Alarm port
		2	VCAIS	Alarm port
		3	DHPTAIS	Alarm port
		4	Receive RDI Change	Alarm port
		5	C2 change	SL port
		6	C2 Unstable	SL port
		7:8	Unused	
	4	1	LOPC	Alarm port
		2:4	Unused	
		4	Receive filtered RDI[2]	Alarm port
		2:3	Receive filtered RDI[1:0]	Alarm port
		1	Unused	
	5	1:8	C2[7:0] filtered SL	SL port
	6	1:8	Unused	
	7	1:8	Unused	
	8	1:8	Unused	
	9	1:4	Unused	
		5	CRC-4 bit 1	Control (for error check)
		6	CRC-4 bit 2	Control (for error check)
		7	CRC-4 bit 3	Control (for error check)
		8	CRC-4 bit 4	Control (for error check)

4.5.4.2 Transmit Side: TPAL Serial Bus

The transmit side of the path Alarm serial interface allows insertion of the remote path defect information (HP-RDI and HP-REI) feedback from the receive into the transmit POH via a serial co- or contra-directional interface. As it can process four independent paths, Intel IXF6048 provides up to four TPAL interfaces (one per channel). The co- or contra-directional mode is configured via register T_HPT_OPC.

Contradirectional Interface: This mode allows using the same timings as the TPOH bus.

- The reference clock is supplied by TPALCK/TPOHCK[i] at 576-KHz. TPALCK/TPOHCK[i] is synchronous with the VC path rate.
- Frame pulse output TPALFR/TPOHFR[i] indicates the expected presence of “Server Defect” at TPAL input. It is repeated every 125 µs.
- The Intel IXF6048 latches the data on the TPAL pin, synchronized with the output timing signals.

Codirectional Interface: This mode allows directly connecting the RPAL output port of an Intel IXF6048 chip to the TPAL input port of a second Intel IXF6048 chip. This provides external feedback of both HP-RDI and HP-REI defects from receive to transmit.

- The clock is input on TPALCK[i] at 576-KHz.
- Frame pulse input TPALFR[i] indicates the expected presence of “Server Defect” at TPAL input. It is repeated every 125 µs.
- The Intel IXF6048 latches the data on the TPAL pin, using the input timing signals. As TPALCK[i] might not be synchronous with the transmit VC rate, some information may be lost.

TSAL[i] is used as a ring port to input the path RDI (HP-RDI) and line REI (HP-REI) information from an external source. The chip internal feedback of the remote defects is disabled. For this purpose, it provides:

- The generated REI value to be transmitted.
- The generated RDI defect to be transmitted.

Configuration register T_HPT_C independently specifies the transmit source of G1-RDI and G1-REI as coming from the TPAL input port or not. Note that the TPAL bus may be used as the transmit source for these bytes only if the TPOHINS input control pin is active-low during these bytes time slots on the TPOH input bus.

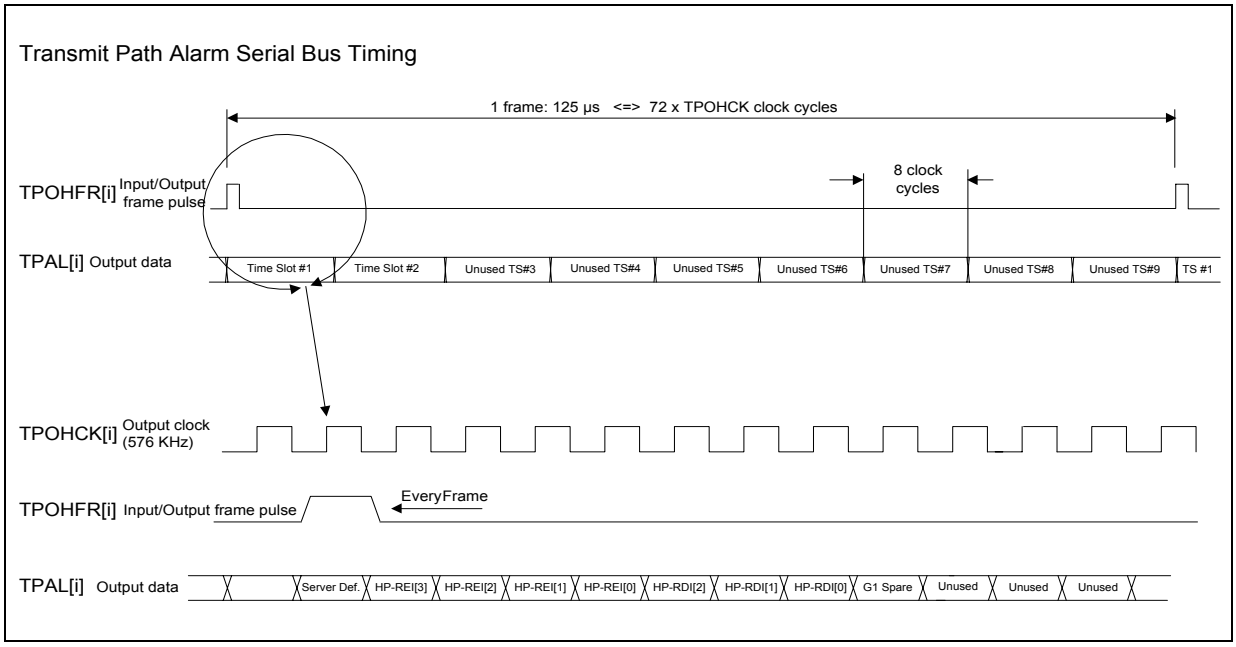
The CRC-4 bits, located in the 4 last bits of the TPAL frame, are computed for data error checking of the TPAL serial input bus. The CRC-4 calculation is performed over the entire TPAL frame including the unused bits. The 4-bit CRC-4 calculated word is the remainder after multiplication by X^4 and then division (modulo 2) by the generator polynomial $X^4 + X + 1$. The CRC-4 bits are replaced by '0's during computation. The remainder result is then compared on a bit-by-bit basis with the CRC-4 bits received in the last four bits of the same TPAL frame (bit 1 is received first). If the remainder calculated does not correspond to the CRC-4 bits received, then the checked TPAL frame (between 2 consecutive frame pulse) is assumed to have some errors. This detected default sets a maskable interrupt that can be accessed via global register TALBINT.

When TPAL[i] is configured as a codirectional interface, Intel IXF6048 also detects the absence of clock (TPALCK[i]) and/or framing pulse (TPALFR[i]) on the incoming timings. If no input framing pulse is detected within 250 µs or there is less than 16 clock cycles within 125 µs, then a maskable interrupt sets that can be accessed via global register TALBINT.

Table 19. TPAL[i] Bus Frame

TPOHFR[i] Status	Time Slot #	Bit Position	Content	Port Type
High	1	1	Server Defect (LOP or AU-AIS) I	Ring port
Low (See Figure 20)		2:5	HP-REI [3:0] to be transmitted in G1	Ring port
		7	HP-RDI[2] to be transmitted in G1	Ring port
		8	HP-RDI[1:0] to be transmitted in G1	Ring port
	2	1	G1 Spare bit (G1[0])	Ring port
		2:8	Unused	
	3	1:8	Unused	
	4	1:8	Unused	
	5	1:8	Unused	
	6	1:8	Unused	
	7	1:8	Unused	
	8	1:8	Unused	
	9	1:4	Unused	
		5	CRC-4 bit 1	Control (for data error check)
		6	CRC-4 bit 2	Control (for data error check)
		7	CRC-4 bit 3	Control (for data error check)
		8	CRC-4 bit 4	Control (for data error check)

Figure 20. Transmit Path Alarm Serial Bus Timing



4.5.5 Dedicated Serial Accesses to DCC and Orderwires

4.5.5.1 D1 to D3 Data Communication Channel

For each regenerator section processed in the Intel IXF6048 (up to four), the interface is described below.

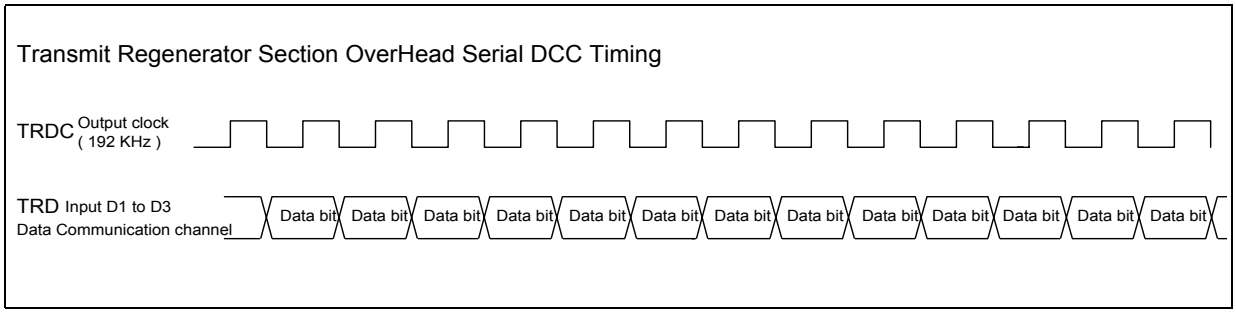
4.5.5.1.1 Transmit Side Access (i = 0, 1, 2, 3)

— Data input is TRD[i] (192-Kbit/s serial access).

— Clock reference is TRDC[i]. This 192-KHz signal is a square wave, synchronous with the transmit clock.

— TOWBYC[i] can be used to identify the byte position, relative to the transmit frame.

Figure 21. Transmit D1 to D3 Timing



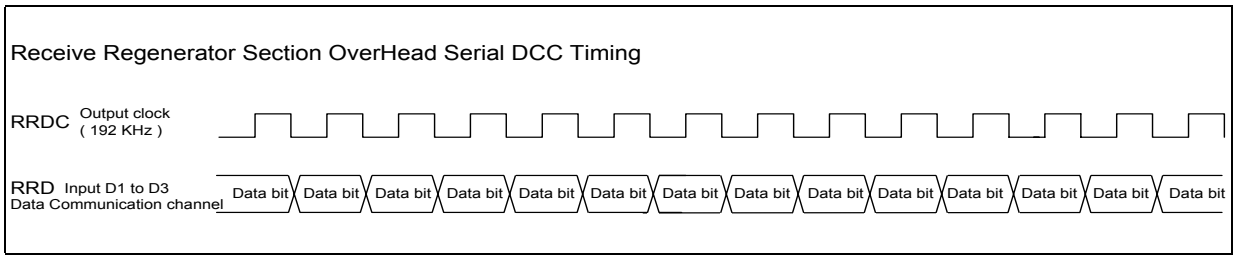
4.5.5.1.2 Receive Side Access (i = 0, 1, 2, 3)

— Data Output is RRD[i].

— Clock reference is RRDC[i]. This 192-KHz signal is a square wave, synchronous with the receive clock.

— ROWBYC[i] can be used to identify the byte position, relative to the receive frame.

Figure 22. Receive D1 to D3 Timing



4.5.5.2 D4 to D12 Data Communication Channel

For each multiplex section processed in the Intel IXF6048 (up to four), the interface is described below.

4.5.5.2.1 Transmit Side Access (i = 0, 1, 2, 3)

— Data input is TMD[i] (576-Kbit/s serial access).

— Clock reference is TMDC[i]. This 576-KHz signal is a square wave, synchronous with the transmit clock.

4.5.5.2.2 Receive Side Access (i = 0, 1, 2, 3)

— Data Output is RMD [i].

— Clock reference is RMDC[i]. This 576-KHz signal is a square wave, synchronous with the receive clock.

Figure 23. Transmit D4 to D12 Timing

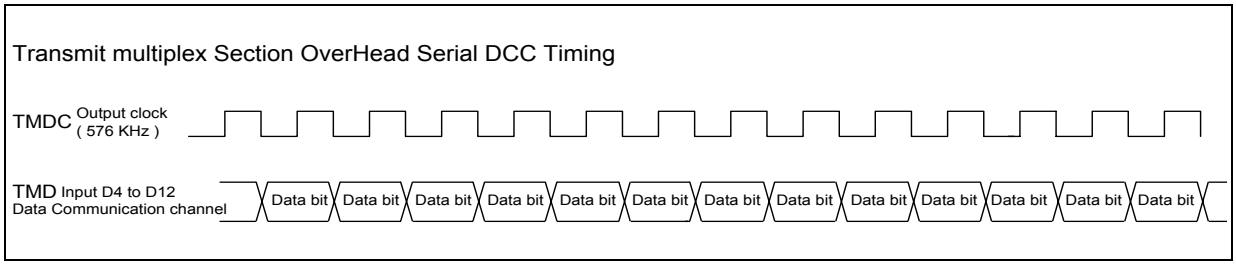
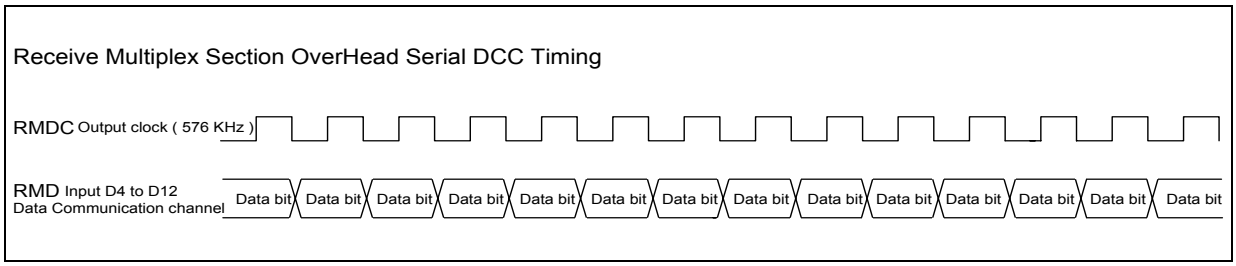


Figure 24. Receive D4 to D12 Timing



4.5.5.3 E1, E2, and F1 Section Orderwire Channel

The interface of each STS/STM aggregate processed in the Intel IXF6048 (up to four) is described below.

4.5.5.3.1 Transmit Side Access (i = 0, 1, 2, 3)

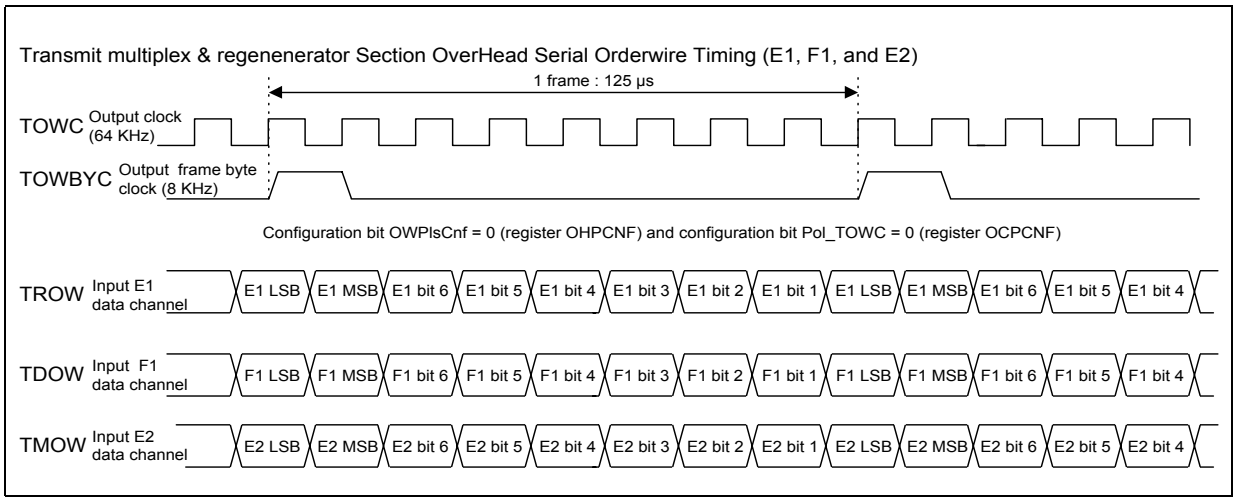
— Data inputs are TROW[i], TMOW[i], and TDOW[i].

— Clock reference is TOWC[i]. This 64-KHz signal is a square wave. Its phase, relative to the data transition, may be inverted via global configuration register OCPCNF, bit Pol_TOWC.

— Byte reference is TOWBYC[i]. By default, it is active-high on the MSB of each byte (see Figure 25). However, it may be configured to be active on the LSB (see global configuration register OHPCNF, bit OWPlsCnf).

— Both the clock reference and the byte reference are synchronous with the transmit clock.

Figure 25. Transmit Orderwire E1, E2, and F1 Timing



4.5.5.3.2 Receive Side Access (i = 0, 1, 2, 3)

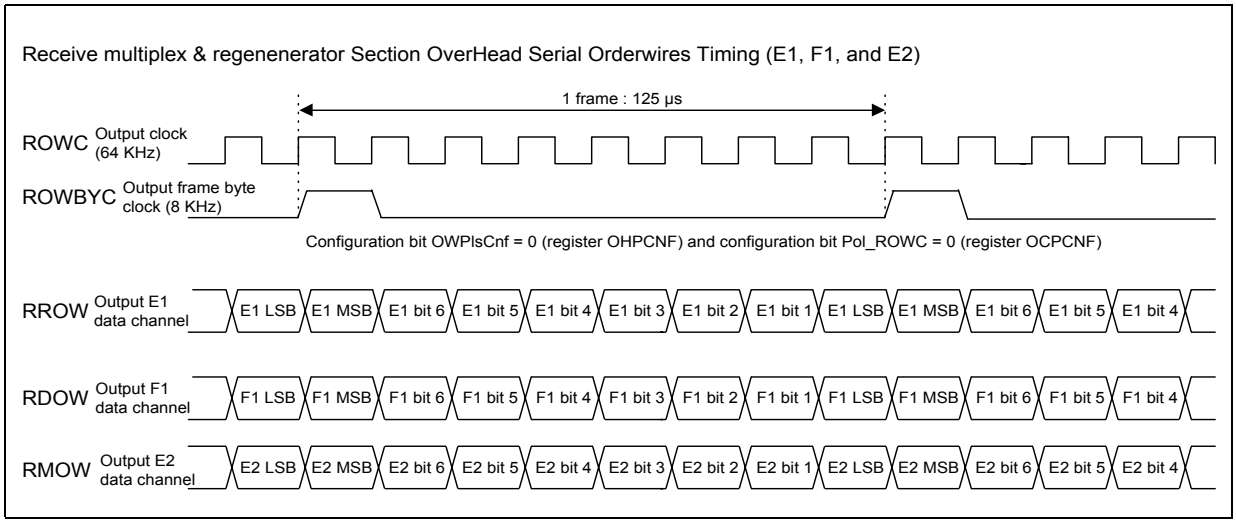
— Data outputs are RROW[i], RMOW[i], and RDOW[i].

— Clock reference is ROWC[i]. This 64-KHz signal is a square wave. Its phase, relative to the data transition, may be inverted via global configuration register OCPCNF, bit Pol_ROWC.

— Byte reference is ROWBYC[i]. By default, it is active-high on the MSB of each byte (see Figure 26). However, it may be configured so that it is active on the LSB (see global configuration register OHPCNF, bit OWPlsCnf).

— Both the clock reference and the byte reference are synchronous with the receive clock.

Figure 26. Receive Section Orderwire E1, F1, and E2 Timing



4.5.5.4 F2 and F3 Path Orderwire Channel

For each path processed in the Intel IXF6048 (up to four), the interface is described below.

4.5.5.4.1 Transmit Side Access (i = 0, 1, 2, 3)

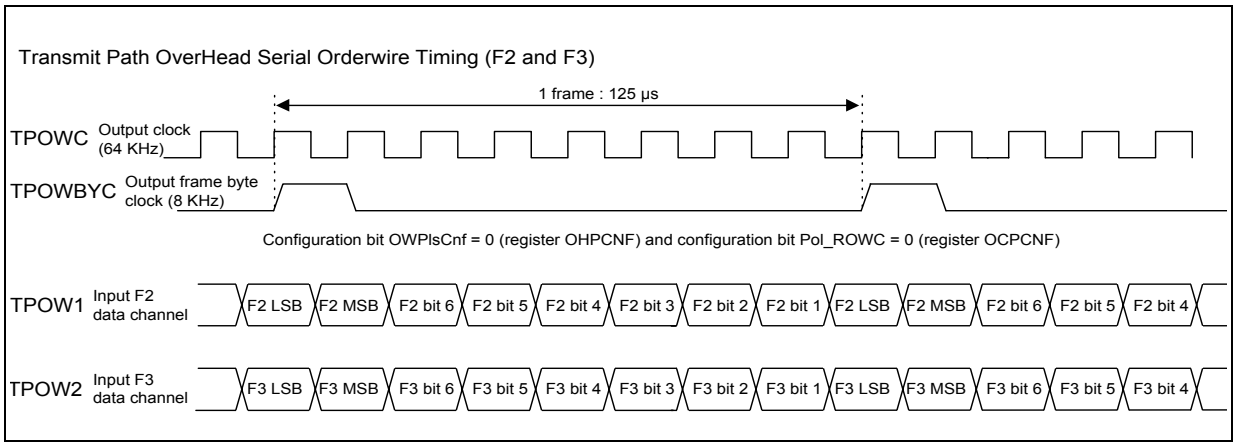
— Data inputs are TPOW1 and TPOW2.

— Clock reference is TPOWC. This 64-KHz signal is a square wave. Its phase, relative to the data transition, may be inverted via global configuration register OCPCNF, bit Pol_TOWC.

— Byte reference is TPOWBYC. By default, it is active-high on the MSB of each byte (see Figure 27). However, it may be configured so that it is active on the LSB of each byte (see global configuration register OHPCNF, bit OWPlsCnf).

— Both the clock reference and the byte reference are synchronous with the transmit VC.

Figure 27. Transmit F2 and F3 Orderwire Timing



4.5.5.4.2 Receive Side Access (i = 0, 1, 2, 3)

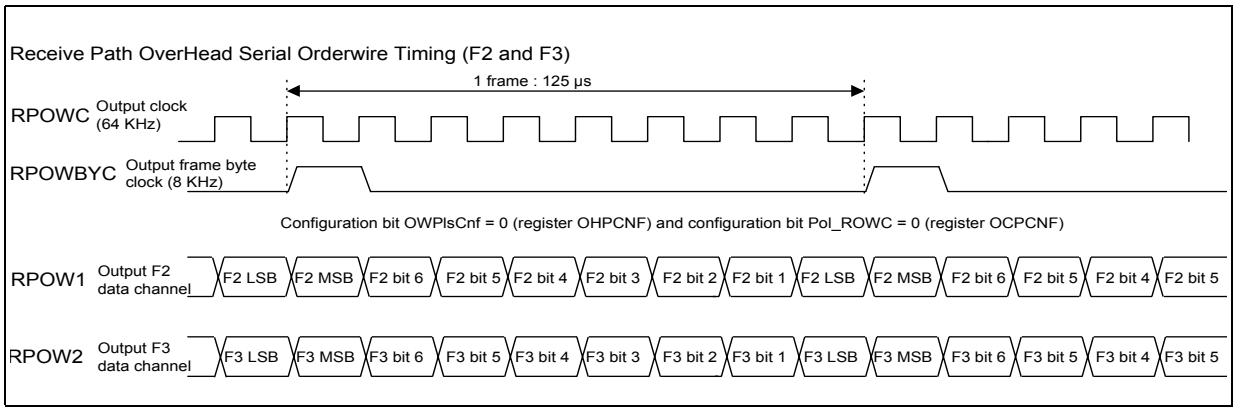
— Data outputs are RPOW1 and RPOW2.

— Clock reference is RPOWC. This 64-KHz signal is a square wave. Its phase, relative to the data transition, may be inverted via global configuration register OCPCNF, bit Pol_ROWC.

— Byte reference is RPOWBYC. By default, it is active-high on the MSB of each byte (see Figure 28). However, it may be configured so that it is active on the LSB of each byte (see global configuration register OHPCNF, bit OWPlsCnf).

— Both the clock reference and the byte reference are synchronous with the receive VC.

Figure 28. Receive F2 and F3 Orderwire Timing



5.0 ATM Cell Processor Functional Description

Intel IXF6048 maps ATM cells asynchronously into one or four SONET/SDH payloads, in accordance with the ITU-T Recommendation I.432 and the ATM Forum BISDN-ICI Specification. Intel IXF6048 complies with the latest ATM Forum User Network Interface (UNI) and ITU-T I.432 specifications by implementing all the Transmission Convergence Sublayer (TCS) functions necessary to adapt the service offered by the SONET/SDH physical layer to the service required by the ATM layer. Intel IXF6048 also implements a GFC halt function, in accordance with ITU-T Recommendations I.150 and I.361. Figure 29 and Figure 30 show the mapping of ATM cells into the SONET SPE and the ATM cell format, respectively.

Figure 29. ATM Cell Mapping

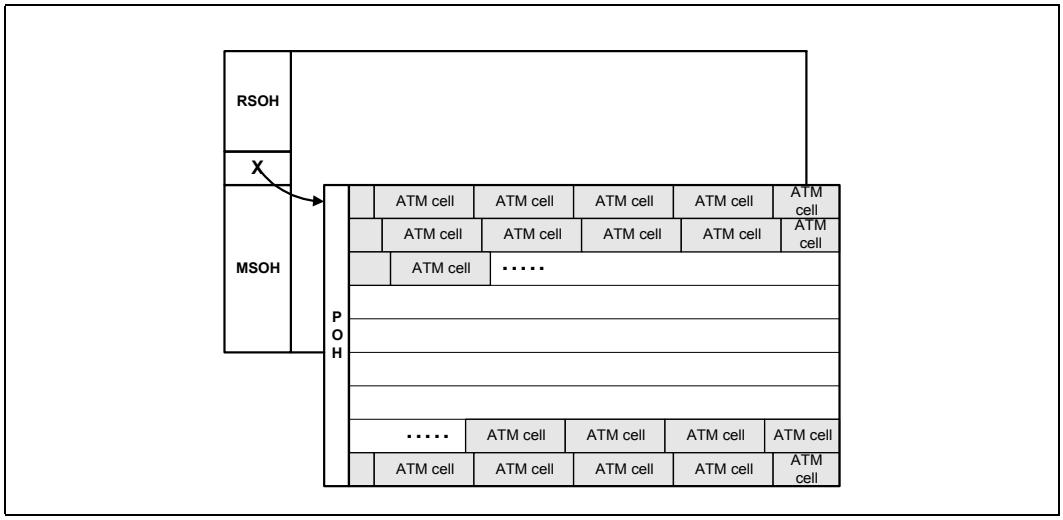
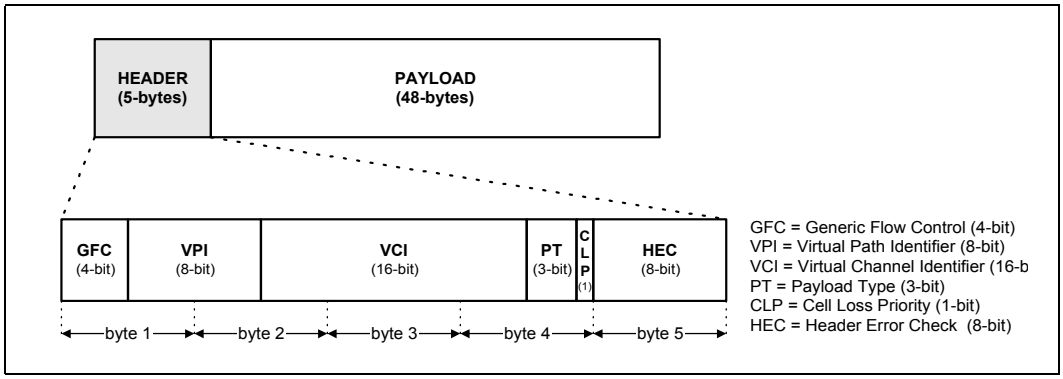


Figure 30. ATM Cell Format



Each receive ATM cell processor (RACP) performs HEC-based cell delineation, HEC checking (and optional cell header correction), cell filtering, cell payload descrambling, and optional GFC monitoring for halt bits. Each transmit ATM cell processor (TACP) provides cell rate adaptation via idle cell insertion, HEC generation and insertion, ATM cell payload scrambling, and optional use of the received GFC halt commands.

5.1 Receive ATM Cell Processing

When Intel IXF6048 is configured as a Quad transceiver (STS-1/STS-3c/STM-1/STS-12c/STM-4c) or as a Single OC-48/STM-16/STM-4 (non-concatenated) transceiver, each of the four receive ATM cell processors (RACP) extracts the incoming ATM cells from the corresponding SPE and writes them into a FIFO memory. The FIFO memory is 256-cell deep in the first channel and 32-cell deep in the other three channels.

When Intel IXF6048 is configured as a Single OC-48c/STM-12c (concatenated) transceiver, only one RACP is active, extracting the incoming ATM cells from the SPE and writing them into a 256-cell deep FIFO memory.

5.1.1 HEC-Based Cell Delineation

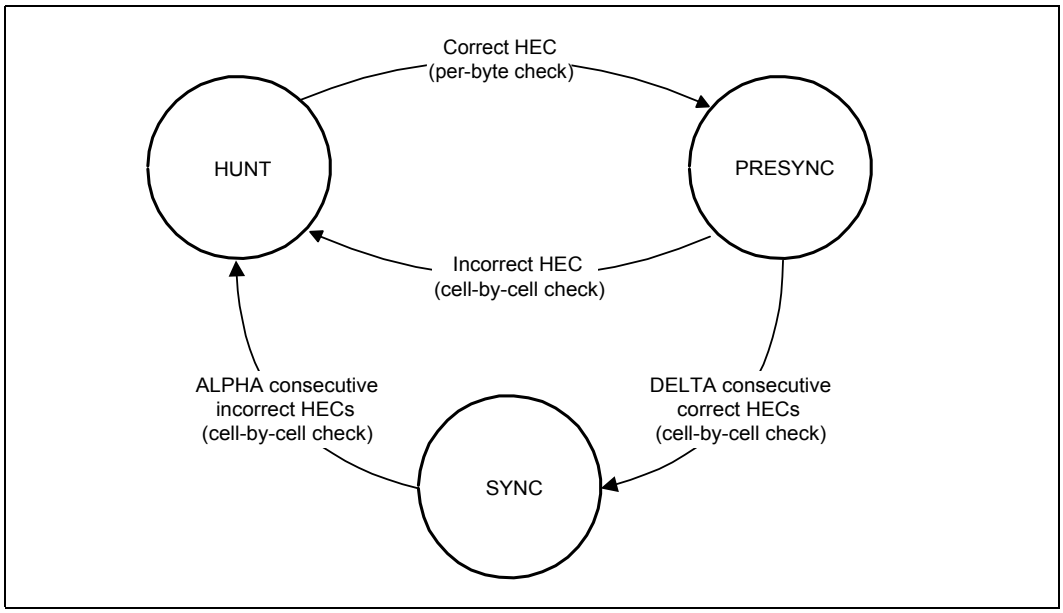
The RACP performs cell delineation based on HEC correct calculations in accordance with ITU-T I.432. Intel IXF6048 offers some additional optional features to this standard process. The following describes the Intel IXF6048 cell delineation process.

The HEC is a CRC-8 calculation over the first 4 bytes of the ATM cell header based on the polynomial $X^8 + X^2 + X + 1$. The co-set polynomial $X^6 + X^4 + X^2 + 1$ ('01010101') is added to the received HEC octet before checking. While searching for the cell boundary location, the RACP is in the HUNT state. In this state, the RACP checks one of the 53 possible boundary candidates (per-byte checking). When a correct HEC is found (a cell header candidate), the RACP enters the PRESYNC state.

The PRESYNC state validates the cell boundary location detected in the HUNT state. If no HEC errors are detected during DELTA consecutive cells (cell-by-cell checking), the SYNC state is entered.

While in the SYNC state, synchronization is maintained until ALPHA consecutive incorrect HECs are detected. The values of ALPHA and DELTA, determining the robustness against false misalignments and false delineations, are ALPHA = 7 and DELTA = 6.

Figure 31. Cell Delineation State Diagram



5.1.1.1 HEC Verification and HEC-Based Cell Filtering

Normally, while in the PRESYNC state, no ATM cells are accepted. However, configuration bit RcvPRESYNCCnf (channel register R_ACPCNF) allows passing (writing into the receive FIFO) the correct ATM cells received while in the PRESYNC state.

While in the SYNC state, two operational modes are possible: Correction mode (normal operation) and Detection mode.

In the Correction mode, the incoming ATM cells are processed as follows:

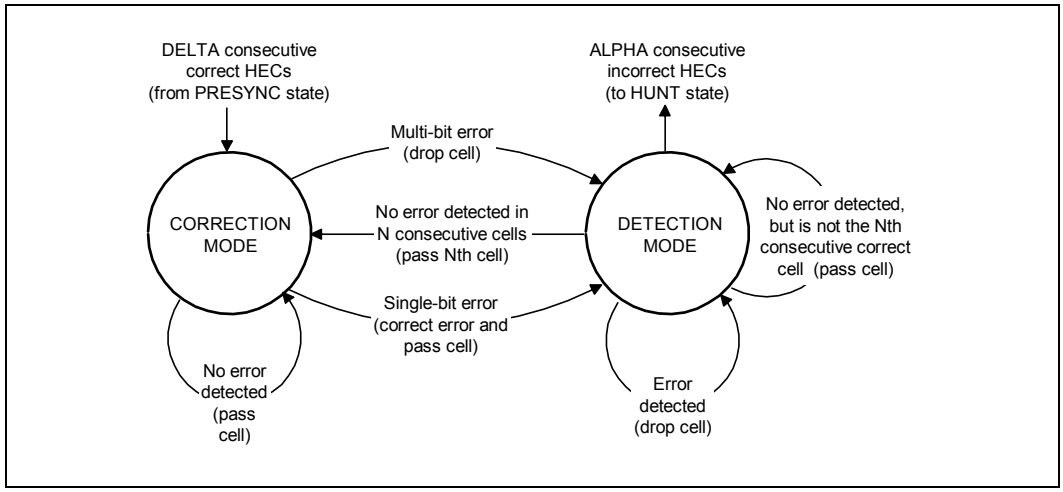
- Incoming ATM cells with no HEC errors are accepted.
- Incoming ATM cells with single-bit error are corrected and accepted.
- Incoming ATM cells with multiple-bit errors are dropped.

Upon discovery of a single- or multiple-bit error, the operation enters the Detection mode. While in the Detection mode, the operation returns to the Correction mode after detecting ‘N’ consecutive cells having a correct HEC sequence. All cells with correct HEC are accepted. The value of ‘N’ can be set to four different values (1, 2, 4, or 8) by configuring RcvCorrDetCnf[1:0] (channel register R_ACPCNF). Configuration bit RcvSYNCCnf (channel register R_ACPCNF) disables the HEC-based cell filtering performed while in the SYNC state. If RcvSYNCCnf is set to logic one, all the ATM cells received while in the SYNC state are accepted, regardless of the errors detected in the HEC field.

Seven (ALPHA) consecutive cells with incorrect HEC, forces transition into the OCD (out of cell delineation) state (PRESYNCH or HUNT states). Seven (1 + DELTA) consecutive cells with correct HEC, forces the chip to exit the OCD state by going into the SYNC state). If OCD persists for ‘M’ ms, the RACP enters the LCD (loss of cell delineation) state. The RACP leaves the LCD state when the cell delineation process enters and remains in the SYNC state for longer than ‘M’

ms. Parameter ‘M’ defaults to 1 ms for OC-48c but it can be changed by using channel register R_LCDFLTR. Software status bits (channel register R_ATMINT) and maskable interrupt bits (channel register R_ATMINT) indicate the current OCD and LCD states.

Figure 32. HEC Verification State Diagram (While in SYNC State)



5.1.1.2 Idle/Unassigned Cell Filtering

A programmable filter, consisting of 8-bit patterns and an 8-bit mask (channel register R_IUCFLTR), allows identification and dropping of the idle/unassigned cells by comparing the incoming GFC, PTI, and CLP bits with the programmed mask. A cell is dropped if the cell header matches this mask while both VPI and VCI fields contain the all '0's pattern. This function can optionally be disabled.

5.1.1.3 Cell Payload Descrambling

The 48-byte cell payload is descrambled using a self-synchronizing descrambler with the polynomial $X^{43} + 1$. This function can optionally be disabled.

5.1.1.4 GFC Processing

Intel IXF6048 allows the software to monitor the incoming Generic Flow Control (GFC) bits to determine the remote device configuration: controller device, controlled device, or no GFC functions implemented. When the GFC is enabled in the system, Intel IXF6048 can be configured as a controlled or a controlling device. When configured as a controlled device, every time a cell is received with the “halt bit” GFC[3] set, an idle/unassigned cell is inserted in the transmit stream.

5.1.1.5 Performance Monitoring Counters

— The number of cells that have been sent to the receive FIFO (cells passing the configured cell filter) are counted in a 24-bit counter (channel register R_ACELLCNT).

— The number of cells matching the Idle/Unassigned programmable filter (channel register R_IUCFLTR) are counted in an 24-bit counter (channel register R_ICELLCNT).

— The number cells containing a correctable error in the header are counted in a 16-bit counter (channel register R_CHECNT).

— The number cells containing an uncorrectable error in the header are counted in a 16-bit counter (channel register R_UHECNT).

— The number of accepted cells that have been lost, due to a FIFO overflow, are counted in a 16-bit counter (channel register R_CFOCNT).

5.1.1.6 Receive FIFO Control

The receive FIFO memory—one 32/256-cell deep and three 32-cell deep FIFOs in a four-channel application or a single 32/256-cell deep FIFO in a one-channel application—stores the received non-dropped ATM cells, thereby providing for the separation of the TCS timing from the ATM layer timing. The channel 0 receive FIFO is configurable to either 32 or 256 cells deep by the user. It is then read by the receive ATM-UTOPIA interface. The receive FIFO is controlled on a cell basis. If the FIFO is full of cells and there is a cell to be stored—the ATM layer has failed to keep up with the incoming ATM cell traffic—the cell is discarded and the problem is indicated via a maskable software interrupt.

5.2 Transmit ATM Cell Processing

When Intel IXF6048 is configured as a Quad transceiver (STS-1/STS-3c/STM-1/STS-12c/STM-4c) or as a Single transceiver (OC-48/STM-16/STM-4 (non-concatenated)), each of the four transmit ATM cell processors (TACP) reads the ATM Layer cells from a FIFO memory and maps them as a continuous ATM-cell stream on the corresponding SPE. The FIFO memory is 32/256-cell deep in the first channel and 32-cell deep in the other three channels.

When Intel IXF6048 is configured as a Single transceiver (OC-48c/STM-12c (concatenated)), only one TACP is active. It reads the ATM Layer cells from a 32/256-cell deep FIFO memory and maps them as a continuous ATM-cell stream on the outgoing SPE. The channel 0 transmit FIFO is configurable to either 32 or 256 cells deep by the user.

5.2.1 Transmit FIFO Control

The transmit FIFO memory—one 32/256-cell deep and three 32-cell deep FIFOs in a 4-channel application or a single 32/256-cell deep FIFO in a one-channel application—stores the ATM Layer cells to be transmitted, thereby providing for the separation of the TCS timing from the ATM layer timing It is then read by the corresponding TACP. The transmit FIFO is controlled on a cell basis. Prior to mapping a new cell in the outgoing SONET/SDH frame, the TACP checks the transmit FIFO status. If the FIFO contains an entire ATM cell, the TACP reads the cell and begins its transmission. Otherwise, an idle cell is automatically generated (cell rate decoupling process).

5.2.2 Idle/Unassigned Cell Insertion

Channel register T_ICELLP is used to configure the values of the CFG, PTI, and CLP fields, as well as the payload pattern for the cells generated and inserted in the cell rate decoupling process. The inserted cells are generated with VPI and VCI containing the all '0's pattern.

5.2.3 HEC Generation/Insertion

The HEC field is automatically generated and inserted in all the transmitted ATM cells. The HEC is a CRC-8 calculation over the first four bytes of the ATM cell header, based on the polynomial $X^8 + X^2 + X + 1$. The co-set polynomial $X^6 + X^4 + X^2 + 1$ '01010101' is added to the calculated HEC before transmission. Intel IXF6048 allows inserting continuous single- or multiple-bit HEC errors via software control (channel register T_ACPCNF).

5.2.4 Cell Payload Scrambling

The 48-byte cell payload is scrambled using a self-synchronizing scrambler with the polynomial $X^{43} + 1$. This function can optionally be disabled.

5.2.5 GFC Processing

When configured as a controller device, Intel IXF6048 implements the cyclic halt function by periodically setting the “halt bit” CFG[3]. By setting a 3-bit parameter (XmfGFCCnf[2:0] in channel register T_ACPCNF) the software configures how many ATM cells are transmitted with GFC[3] = '1' for every cell transmitted with GFC[3] = '0'.

When configured as a controlled device, Intel IXF6048 automatically sends an idle/unassigned cell every time a cell with the halt bit GFC[3] set is received.

5.2.6 Performance Monitoring Counters

— The number of ATM cells that have been read from the transmit FIFO (assigned or unassigned ATM Layer cells) are counted in a 24-bit counter (channel register T_ACELLCNT).

— The number of idle cells generated and mapped into the transmitted SONET/SDH frames are counted in a 24-bit counter. Intel IXF6048 only counts the idle cells inserted by the cell rate decoupling process, not the idle/unassigned cells inserted by the Generic Flow Control function (channel register T_ICELLCNT).

6.0 ATM-UTOPIA Interface Functional Description

The Intel IXF6048 UTOPIA interface is configured in either ATM mode (ATM-UTOPIA interface) or in POS mode (POS-UTOPIA), depending on the configuration of the channel being accessed through the interface. The configuration of the interface is totally independent in both the transmit and the receive directions. When a transmit (or receive) channel is configured in ATM mode—RcvChMode[1:0] = '10' in register R_COCNF or XmtChMode[1:0] = '10' in register T_COCNF—the transmit (or receive) UTOPIA interface operates in ATM mode for this channel. It is possible to have a mixed configuration of channels operating in ATM mode and channels operating in POS mode.

The ATM-UTOPIA interface connects an ATM Layer device to the Intel IXF6048 (a Physical Layer device). The interface complies with the ATM Forum UTOPIA Level 3 and Level 2 specifications.

The interface supports cell-level handshaking using a single cell available signal, as well as direct status indication, which uses a separate cell-available signal for each channel.

The interface operates at up to 104 MHz in the single 32-, 16-, and 8-bit modes, as well as the quad 8-bit mode. The interface operates at up to 52 MHz in the single 64-bit mode and the quad 16-bit mode.

The receive and transmit cell rate decoupling FIFO memories provide for the separation of the Physical Layer timing and the ATM Layer timing:

- When Intel IXF6048 is configured as a single concatenated transceiver—a single physical port transporting a single ATM cell stream—only one channel is enabled and it connects to the interface using a 32 or 256-cell FIFO memory (selectable).
- When Intel IXF6048 is configured as a quad transceiver, four physical ports, or as a single non-concatenated transceiver—a single physical port transporting four independent ATM cell streams—channel #0 connects to the interface using a 256-cell FIFO memory, while channels #1, #2, and #3 use a 32-cell FIFO memory. Optionally, the size of the FIFO for channel #0 can be limited to 32-cells by setting XmtSmallMem (transmission) in register T_UICNF and RcvSmallMem (reception) in register R_UICNF.

The FIFO depth at which status signals are asserted in the transmit direction, is configured using register T_UIFDP. This register specifies the required number of stored-cells in the transmit FIFO to deassert TXFA and TXPFA.

The interface is configured as a single interface or as four independent UTOPIA interfaces by setting XmtUQuad in register T_UICNF (transmit direction) and RcvUQuad in register R_UICNF (receive direction).

Figure 33. Cell Rate Decoupling FIFOs in ATM-UTOPIA Multi-Channel Configuration

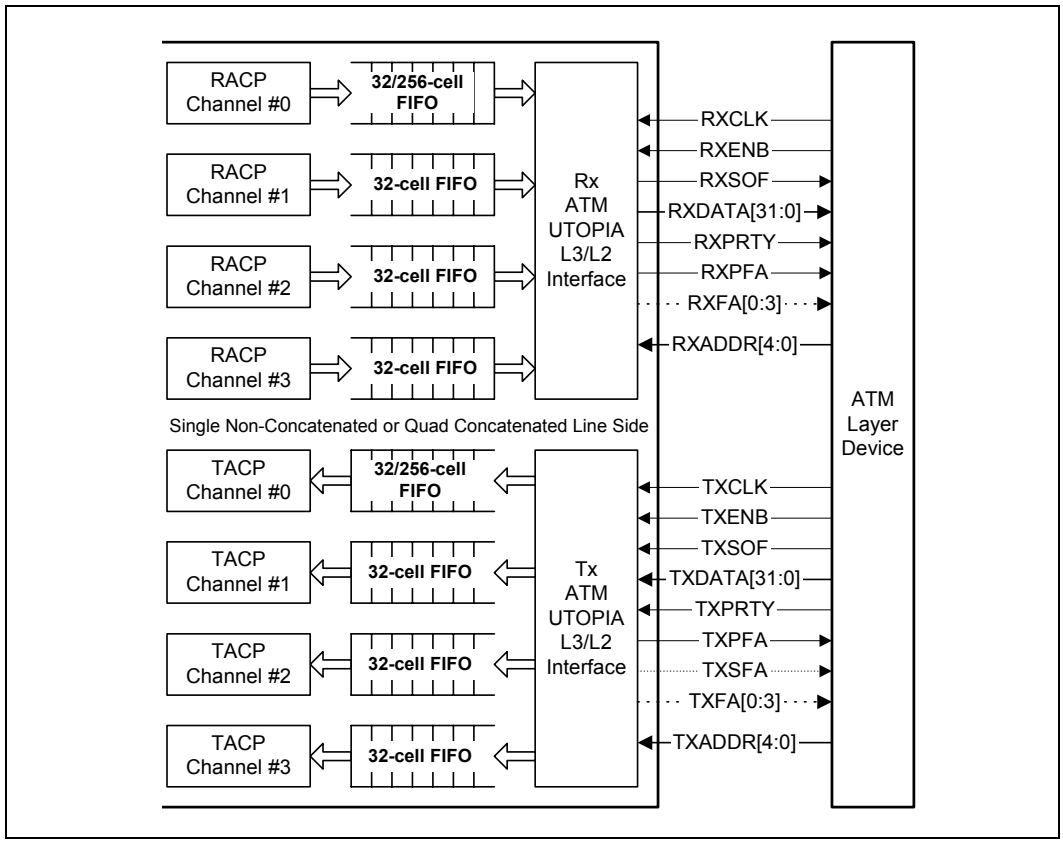


Figure 34. Cell Rate Decoupling FIFO in ATM-UTOPIA Single-Channel Configuration

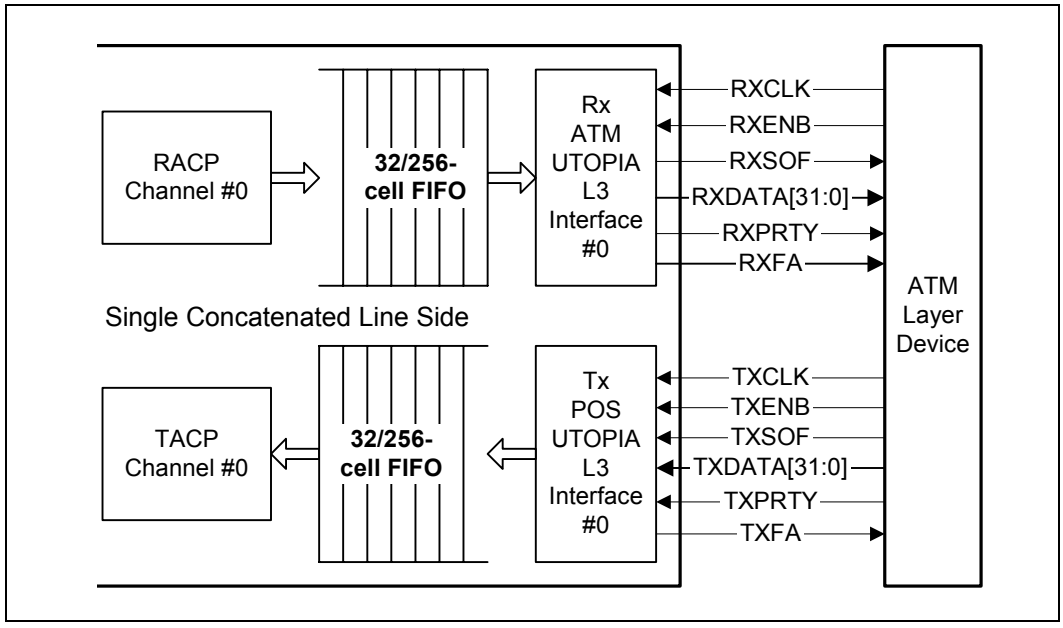
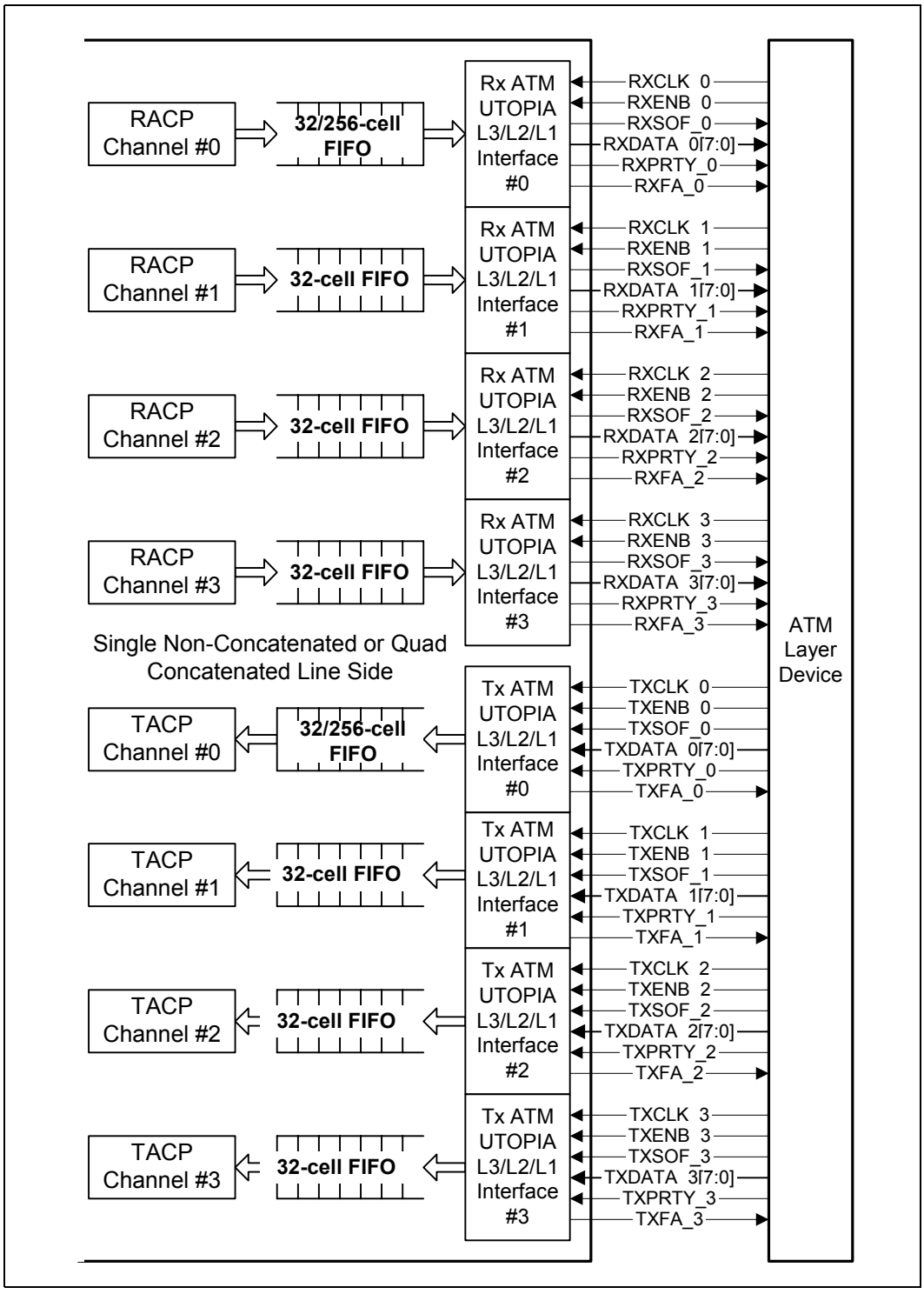
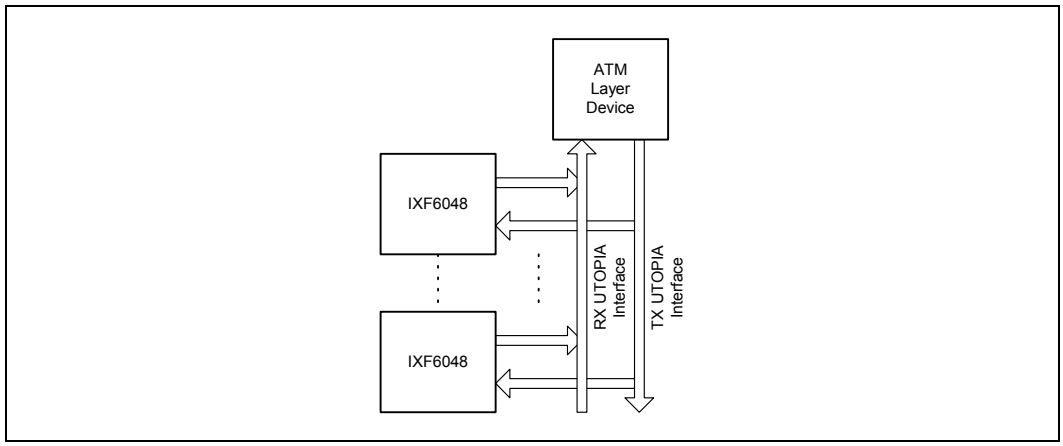


Figure 35. Four Independent ATM-UTOPIA Interfaces



Intel IXF6048 can share the UTOPIA interface with other PHY devices.

Figure 36. ATM-UTOPIA Multiple Physical Device Mode



6.1 Data Bus Width and ATM Cell Data Structure

The transmit data bus width and receive data bus width can be set independently.

The receive data bus width is configured by setting RcvUMode[1:0] in global register R_UICNF. Outputs RXDATA[31:0] are always part of the UTOPIA interface. However, RXDATA[63:32] use outputs from the TTL line side interface or, when enabled, from the overhead ports (see the pinout description).

Table 20. UTOPIA Receive Data Bus Width

RcvUMode[1:0]	Data Bus Width	Line Status
'00'	8-bit	**Single Mode**: RXDATA[7:0] data bus. RXDATA [31:8] tristated. RXDATA[63:32] are not used in the UTOPIA interface. **Quad Mode**: RXDATA[7:0] ch 0 data. RXDATA[15:8] ch 1 data. RXDATA[23:16] ch 2 data. RXDATA[31:24] ch 3 data. RXDATA[63:32] are not used in the UTOPIA interface.
'01'	16-bit	**Single Mode**: RXDATA[15:0] data bus. RXDATA[31:16] tristated. RXDATA[63:32] are not used in the UTOPIA interface. **Quad Mode**: RXDATA[15:0] ch 0 data. RXDATA[31:16] ch 1 data. RXDATA[47:32] ch 2 data. RXDATA[63:48] ch 3 data.
'10'	32-bit	RXDATA[31:0] data bus. RXDATA[63:32] are not used in the UTOPIA interface.
'11'	64-bit	RXDATA[63:0] data bus.

The transmit data bus width is configured by setting XmtUMode[1:0] in global register T_UICNF. Inputs TXDATA[31:0] are always part of the UTOPIA interface, whereas, TXDATA[63:32] use inputs from the TTL line side interface or from overhead ports (see the pinout description).

Table 21. UTOPIA Transmit Data Bus Width

XmtUMode[1:0]	Data Bus Width	Line Status
'00'	8-bit	**Single Mode**: TXDATA[7:0] data bus. TXDATA[31:8] tristated. TXDATA[63:32] are not used in the UTOPIA interface. **Quad Mode**: TXDATA[7:0] ch 0 data. TXDATA[15:8] ch 1 data. TXDATA[23:16] ch 2 data. TXDATA[31:24] ch 3 data. TXDATA[63:32] are not used in the UTOPIA interface.
'01'	16-bit	**Single Mode**: TXDATA[15:0] data bus. TXDATA[31:16] tristated. TXDATA[63:32] are not used in the UTOPIA interface. **Quad Mode**: TXDATA[15:0] ch 0 data. TXDATA[31:16] ch 1 data. TXDATA[47:32] ch 2 data. TXDATA[63:48] ch 3 data.
'10'	32-bit	TXDATA[31:0] data bus. TXDATA[63:32] are not used in the UTOPIA interface.
'11'	64-bit	TXDATA[63:0] data bus.

The ATM cells are transferred using one of eight possible formats:

- 64-bit × 7-word
- 32-bit × 13-word
- 32-bit × 14-word
- 16-bit × 26-word
- 16-bit × 27-word
- 8-bit × 52-word
- 8-bit × 53-word

The most significant bit of a word is the first transmitted/received bit. The first word of the data structure (word one) in the RXDATA (TXDATA) bus is coincident with the RXSOF (TXSOF) indication.

The ATM cell data structure in the transmit and the receive directions can be configured independently for every channel when the interface is configured in quad mode (RcvUQuad = '1' in receive direction; XmtUQuad = '1' in transmit direction). However, when configured in single mode, the cell data structure for all channels is the one configured for channel #0.

The receive ATM cell structure is configured by setting RcvCellStruct in channel register R_UICHCNF; the transmit ATM cell structure is configured by setting XmtCellStruct in channel register T_UICHCNF. When the receive (transmit) interface is configured to use a 64-bit wide data bus, the value of RcvCellStruct (XmtCellStruct) is ignored and the interface transfers a single 56-byte cell format:

- When the receive (or transmit) data bus width is 64-bits, it transports 56-byte cells (7 words) and the configuration value of RcvCellStruct (or XmtCellStruct) is ignored. The first word transports the cell header (bits 63:32) plus four additional unused bytes (bits 31:0). The remaining 6 words transport the cell payload. Figure 37 shows the 64-bit cell data structure.
- When the receive (or transmit) data bus width is 32-, 16-, or 8-bits, the ATM cell data structure depends on the configuration value of RcvCellStruct (or XmtCellStruct):
  - When RcvCellStruct (or XmtCellStruct) is set to logic zero, the ATM cell data structure in the receive (or transmit) interface transports 52-byte cells. The first four bytes transport the cell header (with no HEC field) and the next 48 bytes transport the cell payload. Depending on the data bus width configuration, this corresponds to a cell data structure of 13 words (32-bit interface), 26 words (16-bit interface), or 52 words (8-bit interface). Figure 38, Figure 40, and Figure 42 show the ATM cell data structure, with RcvCellStruct = '0' (or XmtCellStruct = '0'), for the various data bus configurations (32-, 16-, and 8-bit).
  - When RcvCellStruct (XmtCellStruct) is set to logic one, the ATM cell data structure in the receive (transmit) interface transports an additional word (unused word), after the header bytes. The first four bytes transport the cell header (with no HEC field). The next word (one, two, or four bytes) transports unused byte(s). The last 48 bytes transport the cell payload. Depending on the data bus width configuration, this corresponds to a cell data structure of 14 words (32-bit interface), 27 words (16-bit interface), or 53 words (8-bit interface). Figure 39, Figure 41, and Figure 43 show the ATM cell data structure, with RcvCellStruct = '1' (or XmtCellStruct = '1'), for the different data bus configurations (32-, 16-, and 8-bit).

Figure 37. 7-Word ATM Cell Structure (64-Bit UTOPIA Interface)

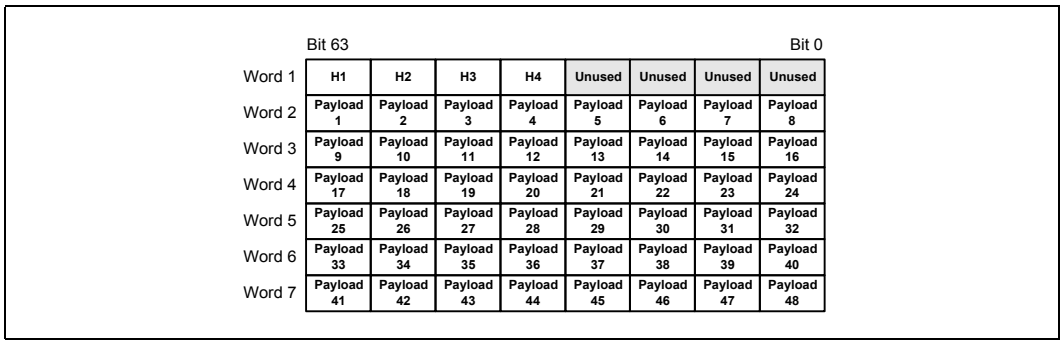


Figure 38. 13-Word ATM Cell Structure (32-Bit UTOPIA Interface)

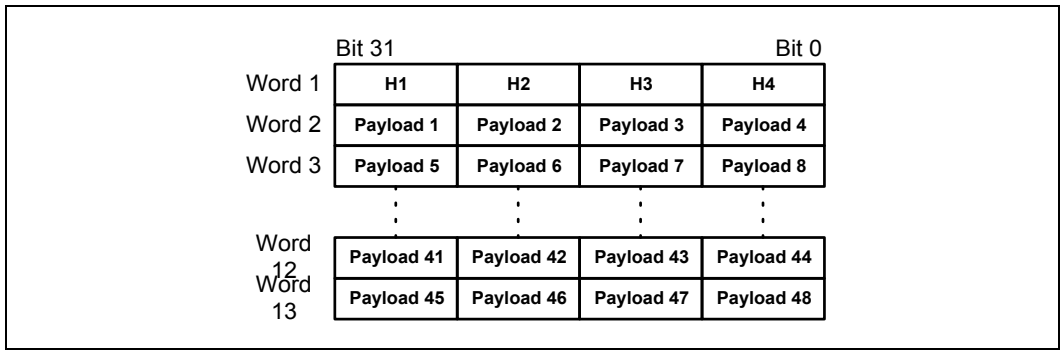


Figure 39. 14-Word ATM Cell Structure (32-Bit UTOPIA Interface)

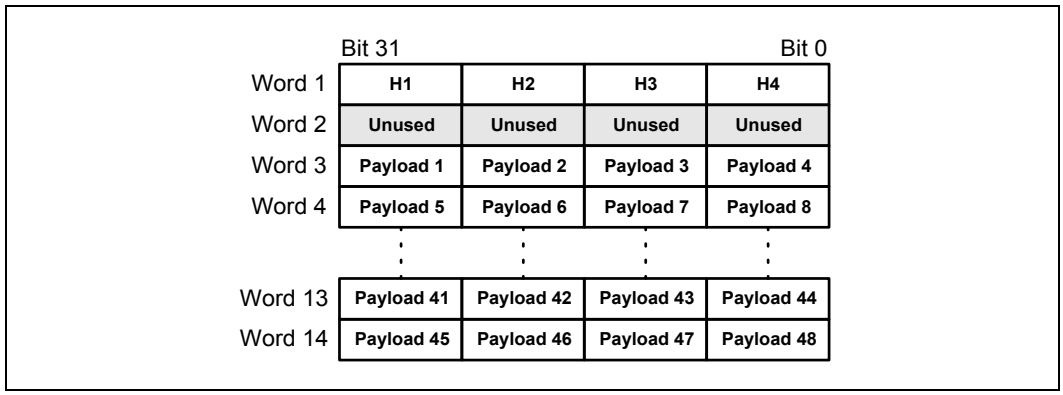


Figure 40. 26-Word ATM Cell Structure (16-Bit UTOPIA Interface)

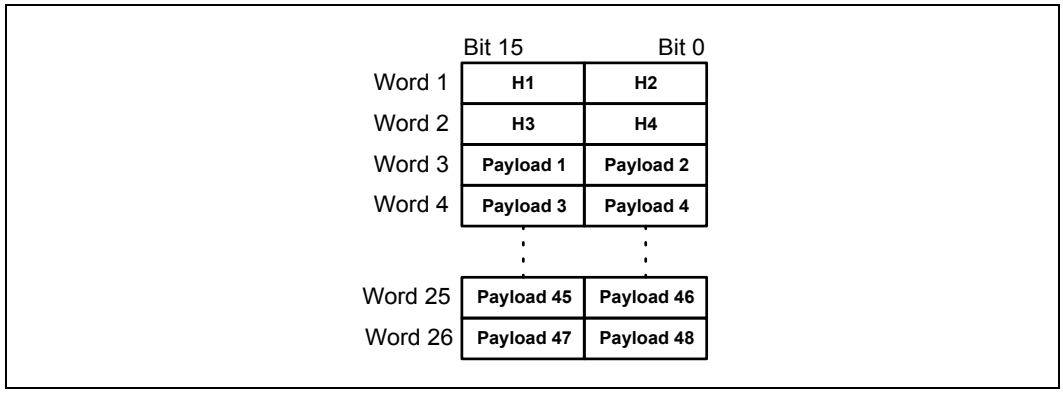


Figure 41. 27-Word ATM Cell Structure (16-Bit UTOPIA Interface)

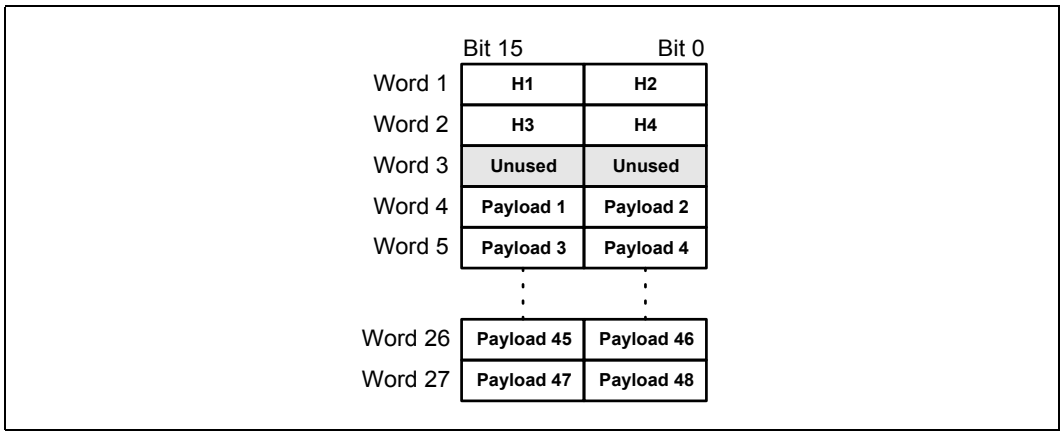


Figure 42. 52-Word ATM Cell Structure (8-Bit UTOPIA Interface)

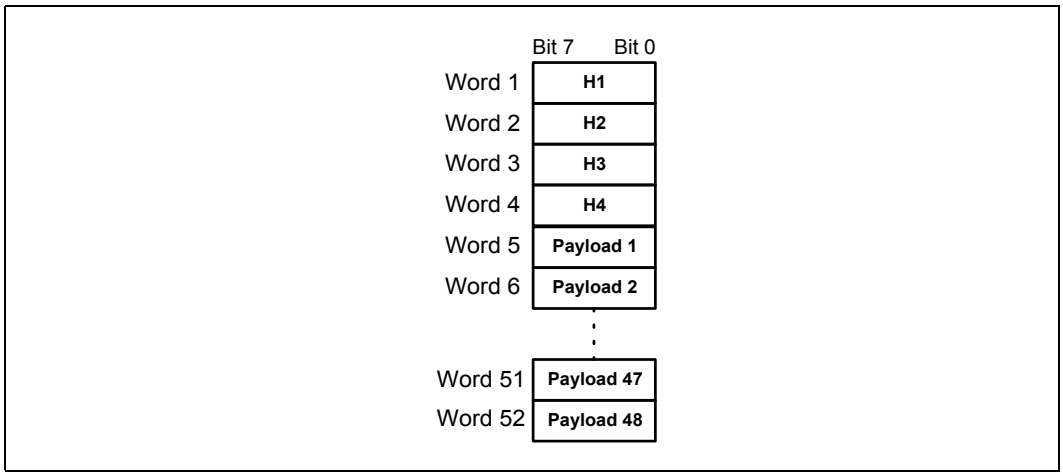
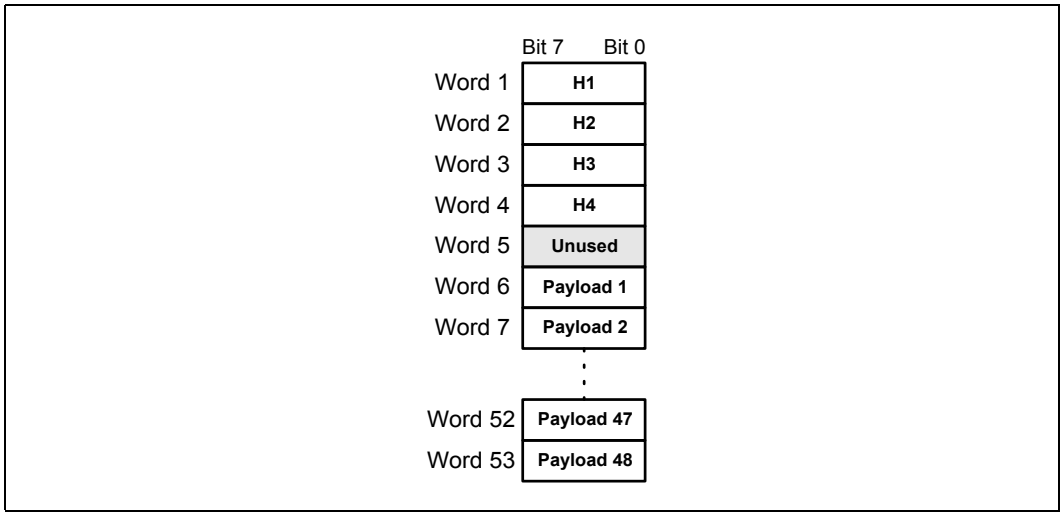


Figure 43. 53-Word ATM Cell Structure (8-Bit UTOPIA Interface)



6.2 Mixed POS and ATM Configuration

When Intel IXF6048 is configured as a Quad transceiver, four Physical ports, or as a Single non-concatenated transceiver—a single Physical port transporting four independent streams—it is possible to have channels operating in ATM mode and channels operating in POS mode, both sharing the same interface with the link layer device. However, the link layer interface behaves in different ways, depending on which channel is selected.

The selection mechanism is common to ATM and POS interfaces. Memory mapped selection mode (see Section 8.0, “POS-UTOPIA Interface Functional Description” on page 191) can be used with channels configured in ATM mode.

In the receive direction, when an ATM channel is selected, outputs RXEOF, RXPADL, RXERR, and RXVAL are driven: RXEOF indicates the last word of a cell, RXPADL and RXERROR are always set to '0', and RXVAL indicates whether the read word is valid. Reading is stopped after RXEOF is asserted, if RcvValCnf is set. This allows resynchronization after reading a cell, in the same way as in the POS interface. However, RXPFA and RXFA behave according to the ATM-UTOPIA interface configuration. Programmable watermarks for POS are not taken into account.

In the transmit direction, when an ATM channel is selected, it is not necessary to drive inputs TXEOF and TXPADL. If a TXSOP is received, when writing a cell into the FIFO, the incomplete cell is overwritten by the new cell, as in the ATM-UTOPIA interface. TXPFA, TXSFA, and TXFA behave according to the configuration of the ATM-UTOPIA interface (XmtDeassert and XmtFDCnf) meaning programmable watermarks for POS are not taken into account.

6.3 Receive ATM-UTOPIA Interface

6.3.1 Decode-Response Configuration

UTOPIA Level 1 and Level 2 specifications use a single clock cycle delay for the decode-response process. UTOPIA Level 3 defines a two clock cycle decode-response delay. This feature has been introduced to simplify the design of the Physical device, allowing elimination of critical decoding (gates) between the I/O and the flip-flops.

Intel IXF6048 allows using both decode-response configurations (one or two clock cycles) individually on each direction (receive and transmit) independent of the other configuration settings (data bus width, etc.). The decode-response configuration is set independently for each channel when the interface is configured in quad mode. When working in single mode, it uses the configuration for channel #0.

RcvDRCnf (channel register R_UICHCNF) sets the decode-response delay for the receive interface:

When RcvDRCnf = '0', the decode-response delay in the receive UTOPIA interface is one clock cycle:

- The delay from the receive address (RXADDR) to the receive polled frame available signal (RXPFA) is one clock cycle.
- The delay from the receive enable (RXENA) to the receive data (RXDATA[31:0], RXSOF, and RXPRTY) is one clock cycle.

When RcvDRCnf = '1', the decode-response delay in the receive UTOPIA interface is two clock cycles:

- The delay from the receive address (RXADDR) to the receive polled frame available signal (RXPFA) is two clock cycles.
- The delay from the receive enable (RXENA) to the receive data (RXDATA[31:0], RXSOF, and RXPRTY) is two clock cycles.

6.3.2 Single-Device/Multiple-Device Configuration

Intel IXF6048 can be configured to operate as the only device in the interface (driving the outputs always) or sharing the interface with other PHY devices (driving the outputs only when it is selected). This feature can be configured independently in the receive and transmit directions.

RcvMPhyDevCnf in global register R_UICNF controls the receive interface:

- When RcvMPhyDevCnf = '1', the receive outputs RXDATA, RXSOF, and RXPRTY are only driven when the device is selected for a receive cell transfer and RXPFA is only driven when RXADDR matches the programmed device address. This setting **must** be used when Intel IXF6048 shares the receive interface with **other PHY devices**.
- When RcvMPhyDevCnf = '0', the receive outputs RXDATA, RXSOF, RXPRTY, and RXFA are always driven. This setting **can** be used when Intel IXF6048 is the **only PHY device** in the receive interface.

The direct indication outputs RXFA_i (i = 0, 1, 2, 3) can be configured to be driven always or driven only when RXADDR matches the programmed device address.

RcvDirStatCnf (global register R_UICNF) configures the RXFA_i outputs in two different ways:

- When RcvDirStatCnf = '1' (direct status indication mode), the RXFA_i (i = 0, 1, 2, 3) outputs are always driven.
- When RcvDirStatCnf = '0' (multiplexed status polling), the RXFA_i (i = 0, 1, 2, 3) outputs are driven when RXADDR bus matches the programmed base-address value (UAddrBase, register GOCNF).

6.3.3 Receive ATM-UTOPIA Interface Functional Timing Examples

Figure 44 shows an example where the receive interface has been configured in UTOPIA Level 3 mode using a 64-bit data bus. This could be for a single OC-3/12/48 non-concatenated line side input or four OC-1/3/12 concatenated line side inputs. This example corresponds to the following configuration:

- RcvUQuad = '0' (single UTOPIA interface)
- RcvUWidth[1:0] = '11' (64-bit interface)
- RcvDRCnf = '0' (1 clock cycle decode-response time)
- RcvMPhyDevCnf = '0' (single PHY device)

Figure 46 shows an example where the receive interface has been configured in UTOPIA Level 3 mode. This could be for a single OC-3/12/48 non-concatenated line side input or four OC-1/3/12 concatenated line side inputs. This example corresponds to the following configuration:

- RcvUQuad = '0' (single interface)

- RcvUWidth[1:0] = '10' (32-bit interface)
- RcvCellStruct = '1' (14-word cell data structure)
- RcvDRCnf = '1' (2 clock cycle decode-response time)
- RcvMPhyDevCnf = '0' (single PHY device)

Figure 48 shows an example where the receive interface has been configured as a 32-bit MPHY device. This could be for a single OC-3/12/48 non-concatenated line side input or four OC-1/3/12 concatenated line side inputs. This example corresponds to the following configuration:

- RcvUQuad = '0' (single interface)
- RcvUWidth[1:0] = '10' (32-bit interface)
- RcvCellStruct = '1' (14-word cell data structure)
- RcvDRCnf = '1' (2 clock cycle decode-response time)
- RcvMPhyDevCnf = '1' (multiple PHY device)

Figure 50 shows an example where the receive interface has been configured as a 16-bit single device. This could be for a single OC-3/12 non-concatenated line side input or four OC-1/3 concatenated line side inputs. This example corresponds to the following configuration:

- RcvUQuad = '0' (single interface)
- RcvUWidth[1:0] = '01' (16-bit interface)
- RcvCellStruct = '1' (27-word cell data structure)
- RcvDRCnf = '0' (1 clock cycle decode-response time)
- RcvMPhyDevCnf = '0' (single PHY device)

Figure 52 shows an example where the receive interface has been configured in UTOPIA Level 2 mode. This could be for a single OC-3/12 non-concatenated line side input or four OC-1/3 concatenated line side inputs. This example corresponds to the following configuration:

- RcvUQuad = '0' (single interface)
- RcvUWidth[1:0] = '01' (16-bit interface)
- RcvCellStruct = '1' (27-word cell data structure)
- RcvDRCnf = '0' (1 clock cycle decode-response time)
- RcvMPhyDevCnf = '1' (multiple PHY device)

6.4 Transmit ATM-UTOPIA Interface

6.4.1 Decode-Response Configuration

XmtDRCnf (channel register T_UICHCNF) sets the decode-response delay for the transmit interface:

When XmtDRCnf = '0', the decode-response delay in the transmit UTOPIA interface is one clock cycle:

- The delay from the transmit address (TXADDR) to the transmit polled frame available signal (TXPFA) is one clock cycle.

When XmtDRCnf = '1', the decode-response delay in the transmit UTOPIA interface is two clock cycles:

- The delay from the transmit address (TXADDR) to the transmit polled frame available signal (TXPFA) is two clock cycles.

In quad mode, the decode-response delay can be configured independently for every channel whereas in single mode the configuration for channel zero is used.

6.4.2 Single-Device/Multiple-Device Configuration

Intel IXF6048 can be configured to operate as the only device in the interface (driving the outputs always) or sharing the interface with other PHY devices (driving the outputs only when it is selected). This feature can be configured independently in the receive and transmit directions.

XmtMPhyDevCnf in global register R_UICNF controls the transmit interface:

- When XmtMPhyDevCnf = '1', the transmit output TXPFA is only driven when TXADDR matches the programmed device address (Level 2 mode). This setting **must** be used when Intel IXF6048 shares the transmit interface with **other PHY devices**.
- When XmtMPhyDevCnf = '0', the transmit output TXPFA is always driven. This setting **can** be used when Intel IXF6048 is the **only PHY device** in the transmit interface.

The direct indication outputs TXFA_i (i = 0, 1, 2, 3) can be configured to be driven always or driven only when TXADDR matches the programmed device address.

XmtDirStatCnf (global register UICNF) configures the TXFA_i outputs in two different ways:

- When XmtDirStatCnf = '1' (direct status indication mode), the TXFA_i (i = 0, 1, 2, 3) outputs are always driven.
- When XmtDirStatCnf = '0' (multiplexed status polling), the TXFA_i (i = 0, 1, 2, 3) outputs are driven when TXADDR bus matches the programmed base-address value (UAddrBase, register GOCNF).

6.4.3 Transmit ATM-UTOPIA Interface Functional Timing Examples

Figure 45 shows an example where the transmit interface has been configured in UTOPIA Level 3 mode. This could be for a single OC-3/12/48 non-concatenated line side input or four OC-1/3/12 concatenated line side inputs. This example corresponds to the following configuration:

- XmtUQuad = '0' (single interface)
- XmtUWidth[1:0] = '11' (64-bit interface)
- XmtDRCnf = '0' (1 clock cycle decode-response time)
- XmtMPhyDevCnf = '0' (single PHY device)

Figure 47 shows an example where the transmit interface has been configured in UTOPIA Level 3 mode. This could be for a single OC-3/12/48 non-concatenated line side input or four OC-1/3/12 concatenated line side inputs. This example corresponds to the following configuration:

- XmtUQuad = '0' (single interface)

- XmtUWidth[1:0] = '10' (32-bit interface)
- XmtCellStruct = '1' (14-word cell data structure)
- XmtDRCnf = '1' (2 clock cycle decode-response time)
- XmtMPhyDevCnf = '0' (single PHY device)

Figure 49 shows an example where the transmit interface has been configured as a 32-bit multiple PHY device. This could be for a single OC-3/12/48 non-concatenated line side input or four OC-1/3/12 concatenated line side inputs. This example corresponds to the following configuration:

- XmtUQuad = '0' (single interface)
- XmtUWidth[1:0] = '10' (32-bit interface)
- XmtCellStruct = '1' (14-word cell data structure)
- XmtDRCnf = '1' (2 clock cycle decode-response time)
- XmtMPhyDevCnf = '1' (multiple PHY device)

Figure 51 shows an example where the transmit interface has been configured as a 16-bit single device. This could be for a single OC-3/12 non-concatenated line side input or four OC-1/3 concatenated line side inputs. This example corresponds to the following configuration:

- XmtUQuad = '0' (single interface)
- XmtUWidth[1:0] = '01' (16-bit interface)
- XmtCellStruct = '1' (27-word cell data structure)
- XmtDRCnf = '0' (1 clock cycle decode-response time)
- XmtMPhyDevCnf = '0' (single PHY device)

Figure 53 shows an example where the transmit interface has been configured in UTOPIA Level 2 mode. This could be for a single OC-3/12 non-concatenated line side input or four OC-1/3 concatenated line side inputs. This example corresponds to the following configuration:

- XmtUQuad = '0' (single interface)
- XmtUWidth[1:0] = '01' (16-bit interface)
- XmtCellStruct = '1' (27-word cell data structure)
- XmtDRCnf = '0' (1 clock cycle decode-response time)
- XmtMPhyDevCnf = '1' (multiple PHY device)

6.5 ATM-UTOPIA Level 3/Level 2 Compatibility

Intel IXF6048 operates according to the ATM Forum UTOPIA Level 3 specification by using the following settings:

- 32-bit data bus
- 52-byte or 56-byte ATM cell data structure
- 2 clock cycles decode-response configuration
- Single-device mode

Intel IXF6048 operates according to the UTOPIA Level 2 specification by using the following settings:

- 16-bit or 8-bit data bus
- 52-byte, 53-byte, or 54-byte ATM cell data structure
- 1 clock cycle decode-response configuration
- Multiple-device mode

Intel IXF6048 operates according to the UTOPIA (Level 1) specification by using the following settings:

- 8-bit data bus
- 52-byte or 53-byte ATM cell data structure
- 1 clock cycle decode-response configuration
- Single-device mode

Figure 44. Receive ATM-UTOPIA Interface as a Single PHY Device, 64-Bit Data Bus, and 56-Byte Cell Data Structure (ATM-UTOPIA Level 3)

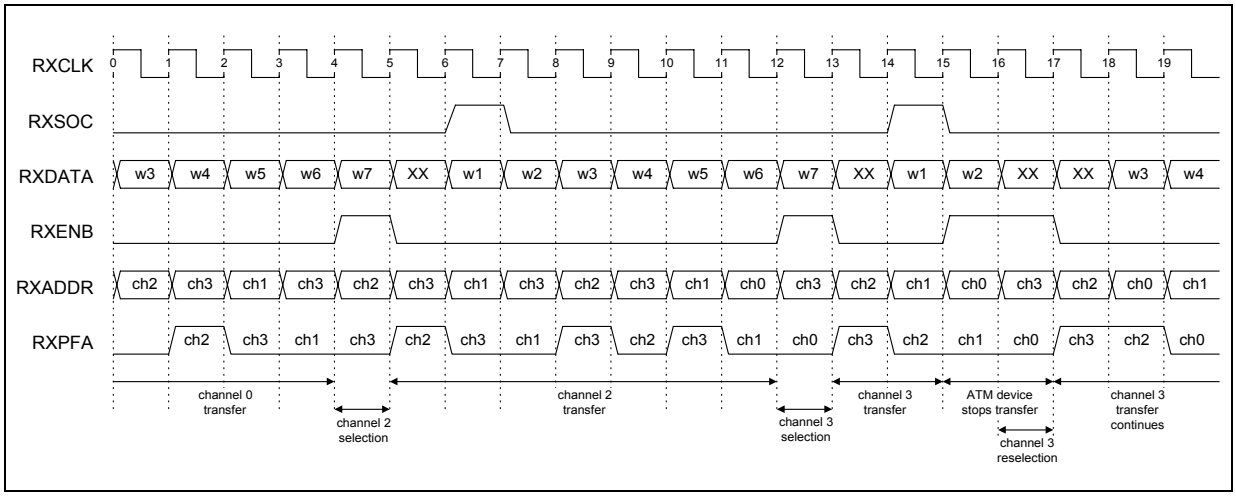


Figure 45. Transmit ATM-UTOPIA Interface as a Single PHY Device, 64-Bit Data Bus, and 56-Byte Cell Data Structure (ATM-UTOPIA Level 3)

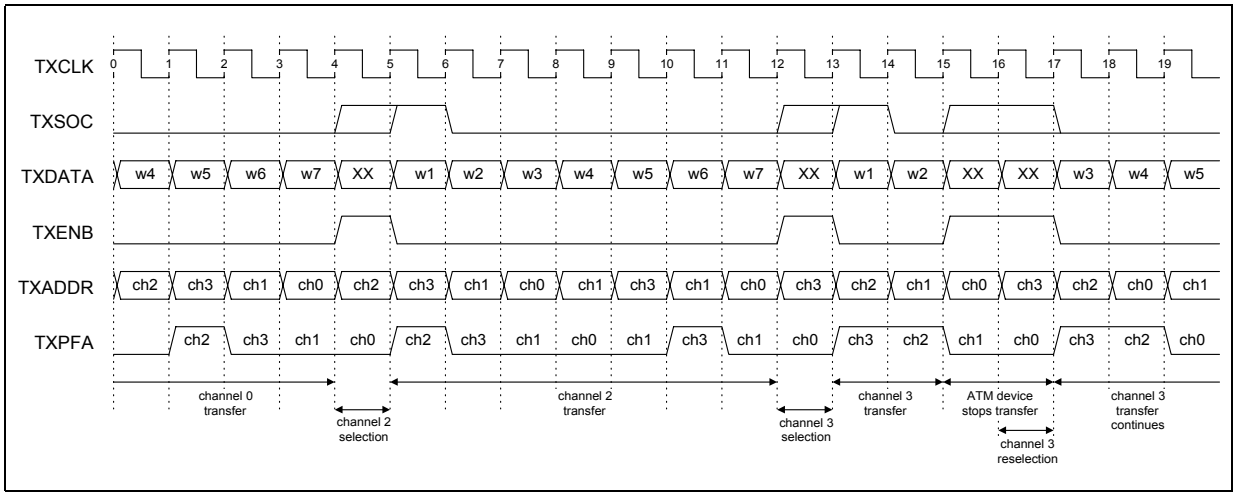


Figure 46. Receive ATM-UTOPIA Interface as a Single PHY Device, 32-Bit Data Bus, and 56-Byte Cell Data Structure (ATM-UTOPIA Level 3 Mode)

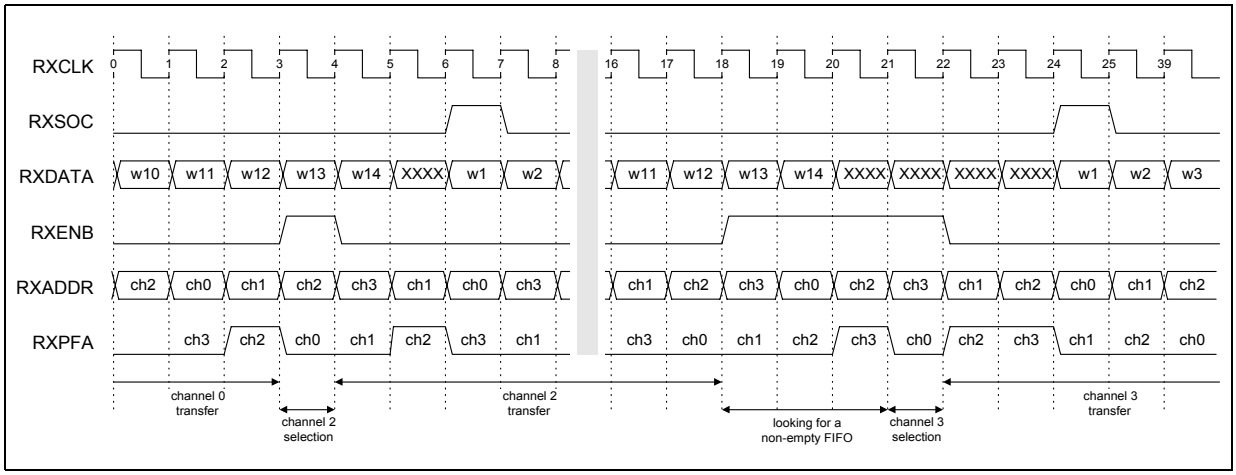


Figure 47. Transmit ATM-UTOPIA Interface as a Single PHY Device, 32-Bit Data Bus, and 56-Byte Cell Data Structure (ATM-UTOPIA Level 3 Mode)

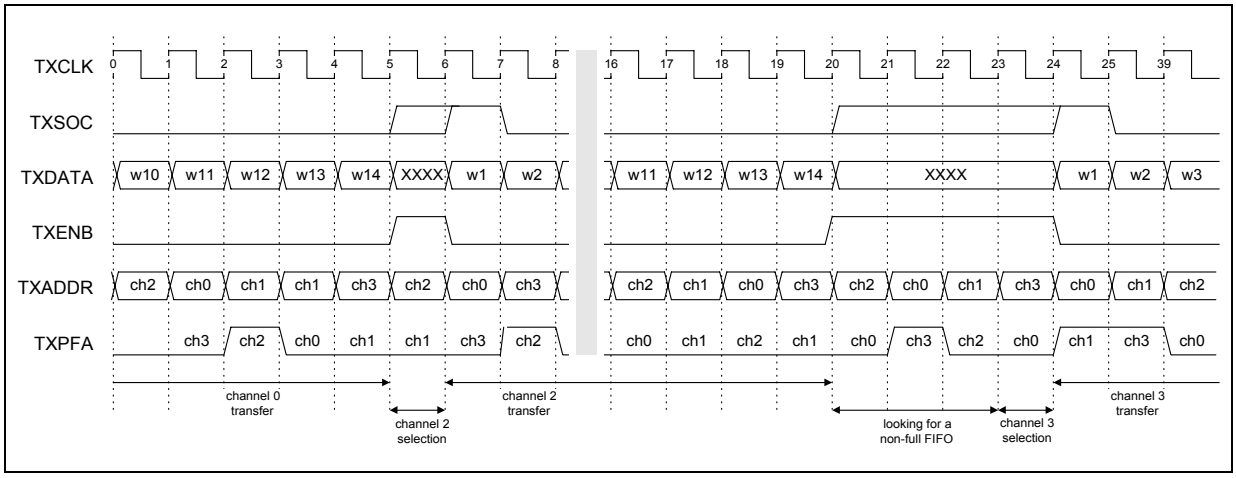


Figure 48. Receive ATM-UTOPIA Interface as a Multiple PHY Device, 32-Bit Data Bus, and 56-Byte Cell Data Structure

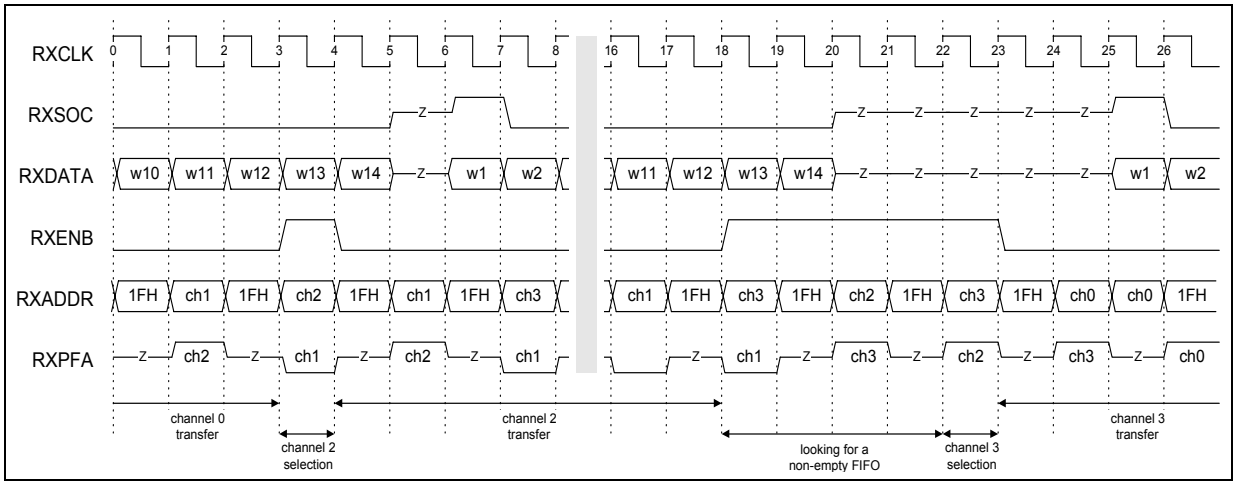


Figure 49. Transmit ATM-UTOPIA Interface as a Multiple PHY Device, 32-Bit Data Bus, and 56-Byte Cell Data Structure

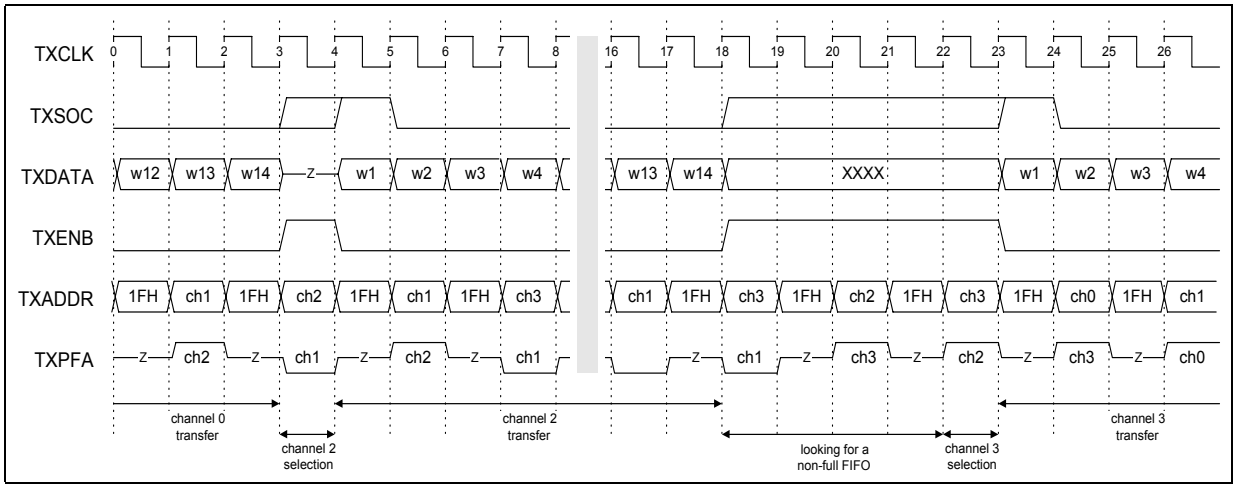


Figure 50. Receive ATM-UTOPIA Interface as a Single PHY Device, 16-Bit Data Bus, and 54-Byte Cell Data Structure

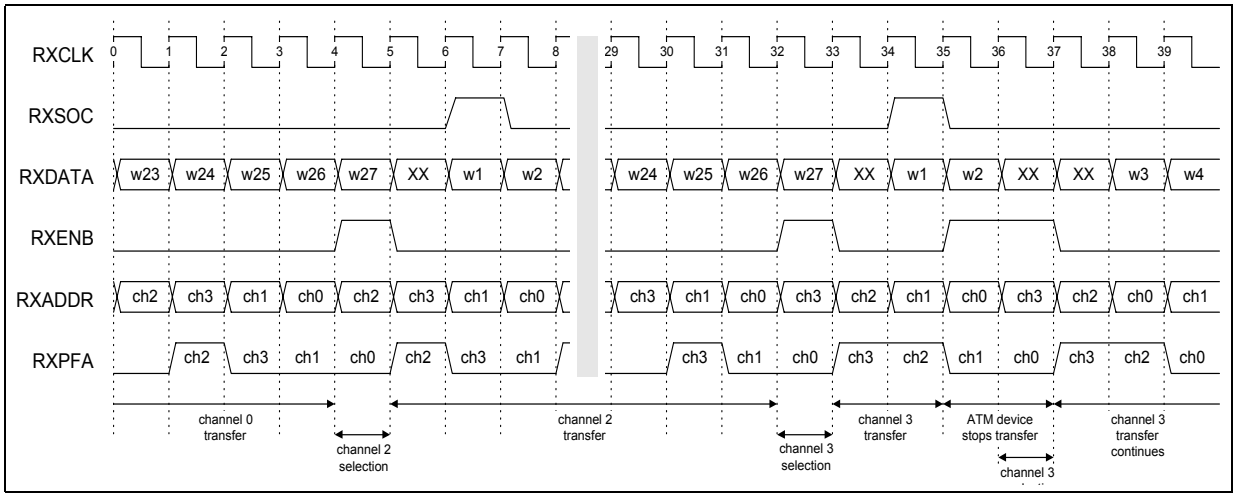


Figure 51. Transmit ATM-UTOPIA Interface as a Single PHY Device, 16-Bit Data Bus, and 54-Byte Cell Data Structure

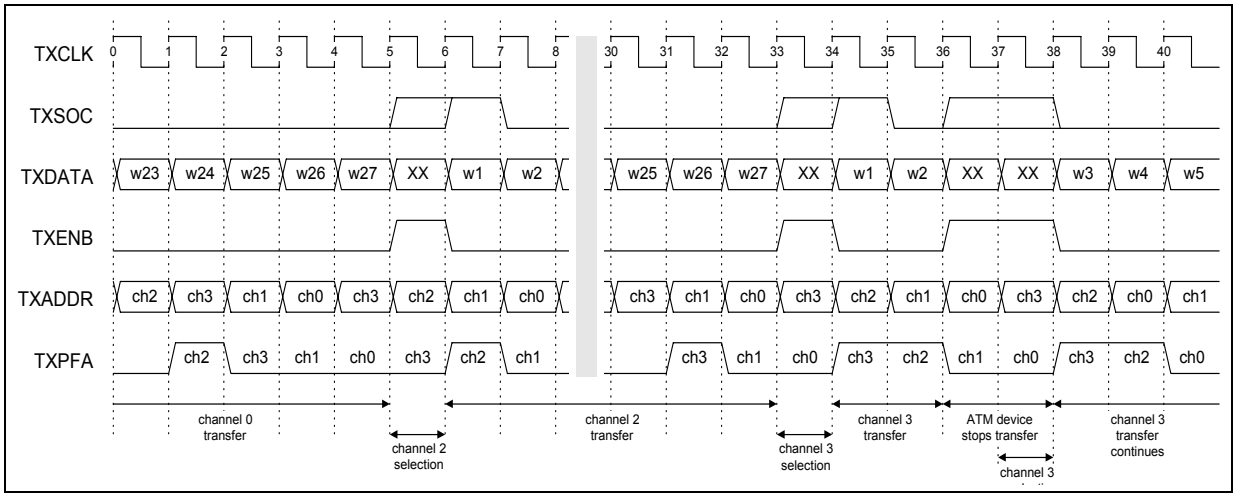


Figure 52. Receive ATM-UTOPIA Interface as a Multiple PHY Device, 16-Bit Data Bus, and 54-Byte Cell Data Structure (ATM-UTOPIA Level 2 Mode)

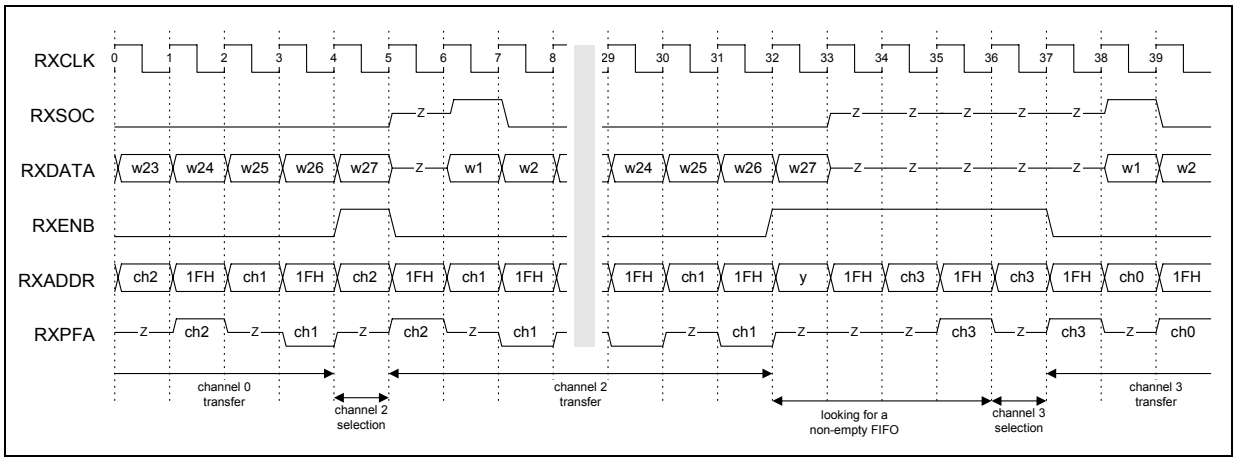
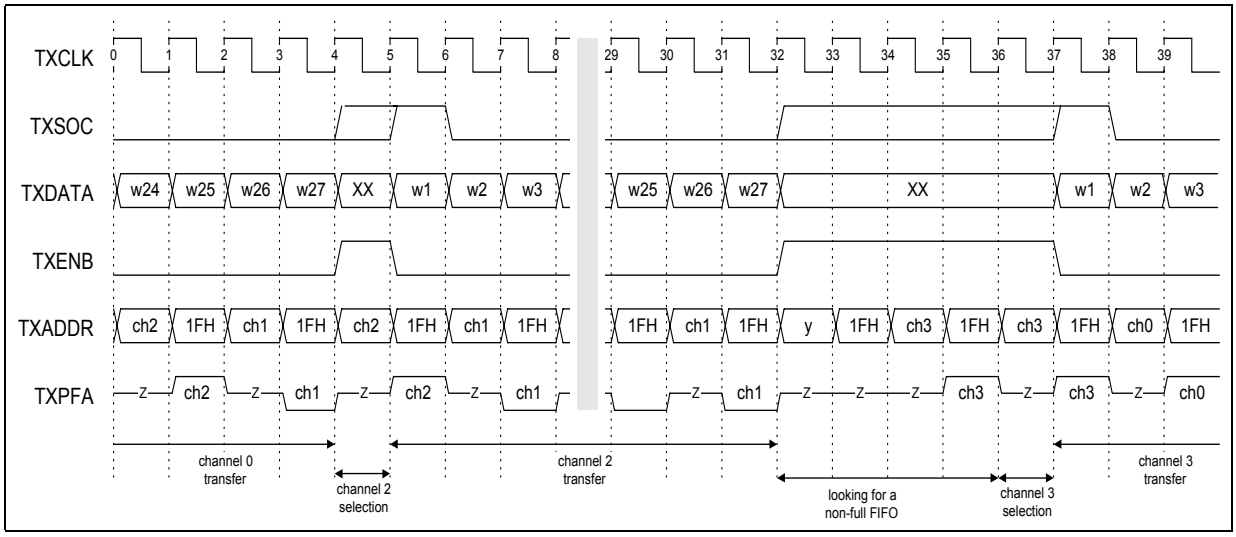


Figure 53. Transmit ATM-UTOPIA Interface as a Multiple PHY Device, 16-Bit Data Bus, and 54-Byte Cell Data Structure (ATM-UTOPIA Level 2 Mode)



7.0 POS HDLC Controller Functional Description

Intel IXF6048 maps HDLC frames into one or four SONET/SDH payloads complying with RFCs 2615 (formerly 1619) and 1662.

Each receive HDLC controller locates the HDLC frames (Flag detection), removes interframe time fill, removes control Escape stuffing (restoring the original byte stream), optionally checks/removes the HDLC Address-Control fields, checks the HDLC FCS field (32-bit, 16-bit, or none), detects Abort sequences, and transfers the "POS-packets" (and some status information) to the Link Layer device using the POS-UTOPIA interface. Each transmit HDLC controller reads POS-packets (coming from the transmit POS-UTOPIA interface), encapsulates each packet into an octet synchronous HDLC frame, and maps the HDLC frame into the SONET/SDH SPE.

Note: Due to the nature of the internal pathways, for specific sizes of POS packets, some bandwidth loss will occur in the transmit direction when sending a data stream consisting entirely of one size of POS packets. The bandwidth loss lessens as the specific packet size increases. The predicted loss rate is:

- For POS packet sizes (not including the flag byte) that equal 4N + 1 (in other words, 49, 53, 57, …, 65533, 65537, 65541), where N is an integer from 12 to 16385, the Intel IXF6048 will add two extra bytes internally and, therefore, reduce the overall throughput by up to (200 / (the POS packet size + 3))% which is 3.8% for a constant stream of 49-byte POS packets to 0.003% for a constant stream of 65541-byte POS packets.
- For POS packet sizes (not including the flag byte) that equal 4N + 2 (in other words, 50, 54, 58, …, 65534, 65538, 65542), where N is an integer from 12 to 16385, the Intel IXF6048 will add one extra byte internally and, therefore, reduce the overall throughput by up to (100 / (the POS packet size + 3))% which is 1.9% for a constant stream of 50-byte POS packets to 0.0015% for a constant stream of 65542-byte POS packets.
- All other sizes of POS packets experience no bandwidth loss and can attain 100% of theoretical throughput.

A POS-packet is the data structure transferred between the Intel IXF6048 and the Link Layer device using the FIFO-based POS-UTOPIA interface. Intel IXF6048 supports two different POS-packet formats. When using the first format, the POS-packet is the HDLC frame information field (the PPP frame). When using the second format, the POS-packet is the combination of the HDLC "Address + Control + Information" fields.

Figure 54 shows the mapping of HDLC frames into the SONET SPE while Figure 55 shows the HDLC frame and POS-packet formats.

Figure 54. HDLC Frame Mapping

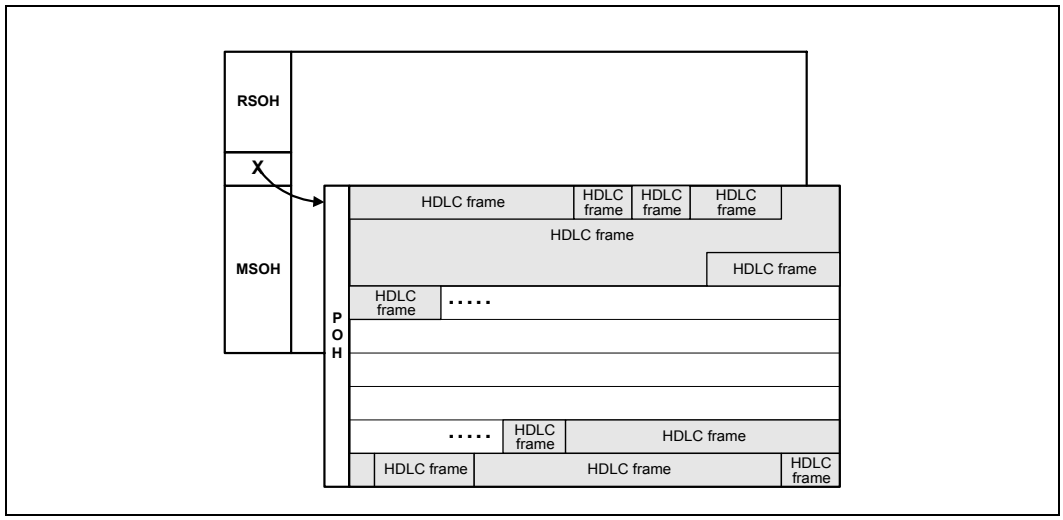
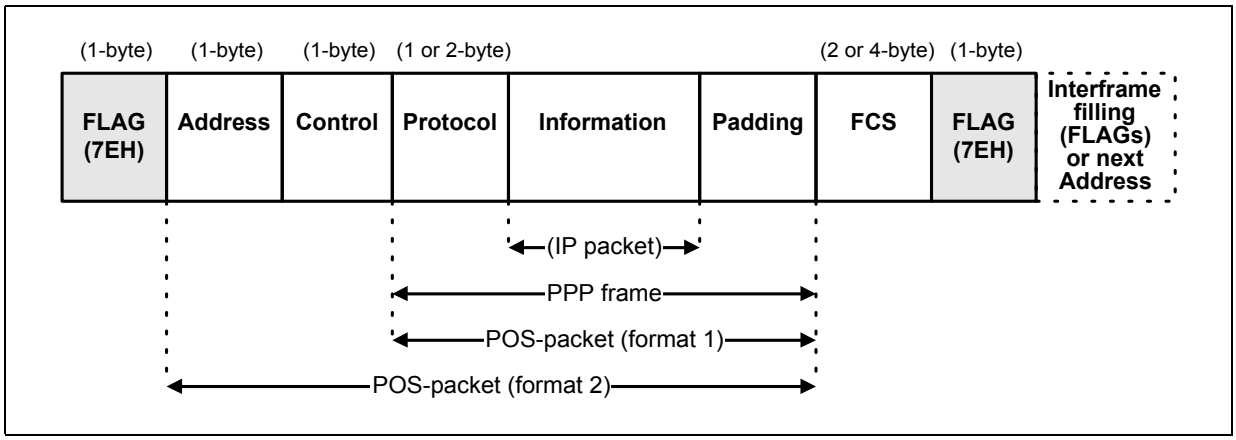


Figure 55. HDLC Frame Format



7.1 Receive HDLC Frame Processing

When Intel IXF6048 is configured as a Quad transceiver (STS-1/STS-3c/STM-1/STS-12c/STM-4c) or as a Single OC-48/STM-16/STM-4 (non-concatenated) transceiver, each of the four receive HDLC controllers extracts the incoming HDLC frames from the corresponding SPE, and writes the POS-packets into a FIFO memory. The FIFO memory is 16-Kbyte deep in the first channel and 2-Kbyte deep in the other three channels. When Intel IXF6048 is configured as a Single OC-48c/STM-12c (concatenated) transceiver, only one HDLC controller is active, extracting the incoming HDLC frames from the SPE and writing the POS-packets into a 16-Kbyte deep FIFO memory.

7.1.1 SPE Descrambling

Intel IXF6048 performs self-synchronous descrambling of the incoming HDLC frames (the incoming SPE bytes) using the polynomial $X^{43} + 1$. The descrambling is performed before the HDLC frames are processed (frame delineation, byte destuffing, etc.). The self-synchronous descrambling can be disabled by setting RcvDescrEn = '0' (register R_PHCCNF).

7.1.2 HDLC Frame Delineation

After SPE descrambling, the receive HDLC controller finds the HDLC frame boundaries by searching the Flag character (7EH). As minimum, one Flag character must be used to separate two consecutive frames. Flags are also used for interframe spacing (two or more consecutive Flag characters). All the Flag characters are eliminated (not written into the receive FIFO).

7.1.3 Frame Intrafilling Removal

Instead of aborting frames when the FIFO underflows in the transmit POS processor, pairs of Control Escape characters (7DH) can be used to fill the gap between valid user data. These Control Escape Characters are added to the frame, after byte stuffing. Frame intrafilling can also be used for flow control purposes.

When the frame intrafilling is enabled (RcvFifEn = '1' in the register R_PHCCNF), the receiver POS processor removes all the Control Escape character pairs found in the middle of a frame before performing byte destuffing. Control Escape pairs are not allowed at the beginning or end of a frame.

7.1.4 Control Escape Stuffing Removal (Byte Destuffing)

The byte destuffing block searches for the Control Escape character (7DH). The Control Escape characters are added for transparency in transmission and must be removed by the receiver to restore the user data. The byte destuffing block eliminates all the Control Escape characters and then XORs the next character with 20H, unless it is the Flag character (which aborts a frame). The byte stuffing/destuffing algorithm is performed over the Address, Control, Protocol, Information, Padding, and FCS fields (between Flags).

Table 22. Byte Destuffing

Character	Received	Destuffed
Flag	7D–5E	7E
Control Escape	7D–5D	7D

7.1.5 User Data Descrambling

In order to avoid frame extension by malicious users and allow data-transparent behavior, the POS frame can be scrambled in the POS transmit processor before going through byte stuffing. The POS receiver processor can optionally descramble received frames, after byte destuffing, recovering the original user data. The descrambling process is self-synchronous and uses the polynomial $X^{48} + X^{28} + X^{27} + 1$.

This descrambler can be disabled by setting RcvTrDescEn = '0' (register R_PHCCNF).

7.1.6 FCS Verification

The Frame Check Sequence (FCS) field is calculated over all bits of the Address, Control, Protocol, Information, and Padding fields, not including the Flag Sequences nor the FCS field itself. The FCS field is checked after Control Escape removal (after byte destuffing). The FCS is received least significant octet first, which contains the coefficient of the highest term. Two different generating polynomials are defined, the CRC-CCITT (CRC-16)

$$g(X) = 1 + X^5 + X^{12} + X^{16}$$

and the CRC-32:

$$g(X) = 1 + X + X^2 + X^4 + X^5 + X^7 + X^8 + X^{10} + X^{11} + X^{12} + X^{16} + X^{22} + X^{23} + X^{26} + X^{32}$$

RcvFCSCnf[1:0] (register R_PHCCNF) configures the use of CRC-CCITT, CRC-32, or no-FCS checking.

When an FCS error is detected, the POS-packet can optionally be marked in the receive FIFO as errored. RcvFCSErr (register R_PHCCNF) is used to configure whether the packet is marked as errored or not.

The FCS field can be eliminated (not written into the receive FIFO) or written into the receive FIFO, depending on the RcvFCSPass bit (register R_PHCCNF). The FCS is always eliminated if the Address and Control fields are passed to the user (see Section 7.1.7).

7.1.7 Address and Control Fields

RcvACPass (register R_PHCCNF) configures whether the Address and Control fields are eliminated or passed to the user (written into the receive FIFO) with the PPP frame. RcvACChk (register R_PHCCNF) enables the checking of the Address and Control fields. The Address field is compared with FFH and the All-Stations address while the Control field is compared with 03H and the Unnumbered Information (UI) command, with the Poll/Final (P/F) bit set to '0'. If RcvACChk = '1', the frames containing Address and Control fields with values different than FFH and 03H are discarded (not written into the FIFO). A maskable interrupt (RcvACI, register R_POSINT) is activated when a frame is discarded in this way.

7.1.8 Receive FIFO

The receive FIFO memory (a 2-Kbyte deep FIFO per channel or a 16-Kbyte deep FIFO in a single-channel application) stores the received POS-packets, providing for the separation of the transport timing from the system timing. It is then read by the receive POS-UTOPIA interface.

When the receive FIFO overflows (the Link Layer device fails to keep up with the incoming HDLC frame traffic), the packet being written into the FIFO is marked as errored. This incomplete POS-packet stored in the FIFO must be discarded by the user. A maskable interrupt (RcvFifoOFI, register R_POSINT) is activated when the FIFO overflows.

After a receive FIFO overflow condition, the receive HDLC controller stops writing data into the FIFO until the receive FIFO free available space is equal to or greater than the value specified by RcvIML[3:0] (register R_PUICNF). RcvIML[3:0] (receive initiation minimum level) is used only after a receive FIFO overflow and is used to avoid consecutive FIFO overflows (to recover after an

overflow condition). Once the receive FIFO contains a number of free words equal to or greater than RcvIML, the HDLC waits for the reception of a new HDLC frame before writing a new POS-packet into the FIFO.

The last byte of aborted packets (packets received with an abort sequence) is not written into the FIFO.

7.1.9 Packet Length Checking

The receive HDLC controller checks the length of the received HDLC frames and optionally marks as errored the frames smaller than a programmed minimum length (R_MINPL) or longer than a programmed maximum length (register R_MAXPL). Configuration bits RcvMixPLDEn and RcvMaxPLDEn (register R_PHCCNF) enable the discarding of the packets smaller or longer than the programmed values R_MINPL and R_MAXPL.

When receiving a packet shorter than the minimum legal packet length, the packet is discarded (not written into the FIFO), and a software maskable interrupt is set (bit RcvSFI in register R_POSINT). These are packets which cannot be processed by the HDLC controlled because they do not contain the minimum information required. For example, if the HDLC controller is configured to discard Address and Control fields and a 32-bit FCS field, any packet shorter than seven bytes is considered illegal and will be discarded.

7.1.10 Performance Monitoring Counters

The monitoring of received frames can be performed considering only the frames that are written into the FIFO (when RcvCntWrFr = '1' in the R_PHCCNF register) or considering all the received frames (RcvCntWrFr = '0').

- The number of received frames not marked as errored (“good frames”) are counted in a 27-bit counter (register R_FRMCNT).
- The number of bytes received are counted in a 29-bit counter (register R_BYTECNT). Intel IXF6048 can be configured to count all the bytes written into the FIFO (good frames + frames marked as errored) or only the bytes received within good frames.
- The number of received aborted frames (finishing with an Abort sequence) are counted in a 20-bit counter (register R_AFCNT).
- The number of received frames with an incorrect FCS field are counted in a 16-bit counter (register R_FCSECNT).
- The number of received frames that have been partially lost due to a FIFO overrun are counted in a 20-bit counter (register R_PFOCNT).
- The number of frames received with a packet length smaller than a programmable minimum packet length (registers R_MINPL) are counted in a 27-bit counter (register R_MINPLECNT)
- The number of frames received with a packet length longer than a programmable maximum packet length (registers R_MAXPL) are counted in a 16-bit counter (register R_MAXPLECNT).

7.2 Transmit HDLC Frame Processing

When Intel IXF6048 is configured as a Quad transceiver (STS-1/STS-3c/STM-1/STS-12c/STM-4c) or as a Single OC-48/STM-16/STM-4 (non-concatenated) transceiver, each of the four transmit HDLC controllers reads the POS-packets from a FIFO memory (16-Kbyte deep in the first channel and 2-Kbyte deep in the other three), encapsulates the data into the generated HDLC frames, and maps the HDLC frames into the corresponding SPE. When Intel IXF6048 is configured as a Single OC-48c/STM-12c (concatenated) transceiver, only one HDLC controller is active, reading the user packets from a 16-Kbyte deep FIFO memory and mapping the generated HDLC frames into the outgoing SPE.

7.2.1 Transmit FIFO

The transmit FIFO memory (a 16-Kbyte deep FIFO in the first channel and 2-Kbyte deep FIFO in the other three channels in a four-channel application or a 16-Kbyte deep FIFO in a single-channel application) stores the POS-packets to be transmitted, providing for the separation of the TCS timing from the system timing. The POS-packets are written into the transmit FIFO by the Link Layer device by using the transmit POS-UTOPIA interface.

After the transmit HDLC controller reads the last word of a POS-packet from the transmit FIFO, the FIFO can be empty. This is not a transmit FIFO underflow: after writing the last word of a POS-packet, the Link Layer device is not required to write a new POS-packet immediately.

A transmit FIFO underflow occurs when the HDLC controller tries to read an empty FIFO (when reading a POS-packet). A transmit FIFO underflow occurs when the Link Layer device fails to keep up with the outgoing HDLC frame traffic (i.e., the SPE rate). If frame intrafilling is not enabled (XmtFifEn = '0' in T_PHCCNF), when the transmit FIFO underflows, the HDLC controller aborts the current HDLC frame, finishing the frame with an Abort sequence.If frame intrafilling is enabled, the HDLC controller inserts pairs of Control Escape characters until new data is available.

While the transmit FIFO is empty, the HDLC controller maps Flag characters into the SPE (interframe filling) and waits for the Link Layer device to write a new POS-packet into the FIFO. The HDLC controller starts reading (and transmitting) the new POS-packet as soon as the transmit FIFO contains a number of words equal to or greater than XmtIML[3:0] (register T_PUICNF). XmtIML[3:0] (transmit initiation minimum level) is used to avoid consecutive FIFO underflows (to recover after an underflow condition).

7.2.2 Address and Control Fields

When the POS-packet is the HDLC information field (XmtACPass = '0', Register T_PHCCNF), the HDLC controller generates the following Address and Control fields:

- Address = FFH (All-stations address)
- Control = 03H (Unnumbered Information command with the Poll/Final bit set to '0')

When the POS-packet is the HDLC “Address + Control + information” fields (XmtACPass = '1', Register T_PHCCNF), the HDLC controller transmits the Address and Control fields read from the FIFO.

7.2.3 FCS Generation/Insertion

The Frame Check Sequence (FCS) field is calculated over all bits of the Address, Control, Protocol, Information, and Padding fields, not including the Flag Sequences nor the FCS field itself. The FCS field is calculated before Control Escape insertion (before byte stuffing). The FCS is transmitted least significant octet first, which contains the coefficient of the highest term. Two different generating polynomials are defined, the CRC-CCITT (CRC-16)

$$g(X) = 1 + X^5 + X^{12} + X^{16}$$

and the CRC-32:

$$g(X) = 1 + X + X^2 + X^4 + X^5 + X^7 + X^8 + X^{10} + X^{11} + X^{12} + X^{16} + X^{22} + X^{23} + X^{26} + X^{32}$$

XmtFCSCnf[1:0] (register T_PHCCNF) configures the use of CRC-CCITT, CRC-32, or no-FCS generation.

The transmit HDLC controller allows insertion of FCS errors by inverting the calculated FCS field before transmission. This can be done by software control (XmtFCSErrCnf and XmtFCSErr, register T_PHCCNF)

7.2.4 User Data Scrambling

In order to avoid frame extension by malicious users and allow data-transparent behavior, the POS frame can be scrambled in the POS transmit processor before going through byte stuffing. When XmtTrScrEn = ‘1’ (register T_PHCCNF), user data goes through a self-synchronous scrambler using the polynomial $X^{48} + X^{28} + X^{27} + 1$.

7.2.5 Control Escape Stuffing Insertion (Byte Stuffing)

Before mapping an HDLC frame into the outgoing SONET/SDH SPE, the transmit HDLC controller escapes all the Flag characters (7EH) and Control Escape characters (7DH) for transparency. The byte stuffing algorithm analyzes, byte by byte, all the characters between Flags (the Address, Control, Protocol, Information, Padding, and FCS fields). Every time a Flag or a Control Escape character is detected, the character is escaped by XORing it with 20H and inserting a Control Escape character before it.

Table 23. Byte Stuffing

Character	Original	Escaped
Flag	7E	7D–5E
Control Escape	7D	7D–5D

7.2.6 Transmit Flow Control

The transmit HDLC controller can perform transmission flow control, by inserting a number of Flag characters between consecutive HDLC frames (interframe filling) by using two different methods.

The first method (configuration bits XmtIPGRelEn, XmtIPGRelCnf, and XmtIPGRel[2:0] in register T_IPGCTRL) transmits, after each HDLC frame, a number of Flag characters proportional to the length of the transmitted frame. Added Control Escape characters due to the byte stuffing process are counted as extra bytes already added to the user's data and are subtracted from the number of flags to be inserted. This method reduces the POS-packet transmission rate.

The second method (configuration bits XmtIPGAbsEn, XmtIPGAbsCnf, and XmtIPGAbs[7:0] in register T_IPGCTRL) transmits, after each HDLC frame, a constant number of Flag characters. This method allows programming a minimum separation between consecutive HDLC frames.

Both methods can be used at the same time to ensure a maximum transmission rate and a minimum interpacket gap simultaneously.

7.2.7 SPE Scrambling

Intel IXF6048 performs self-synchronous scrambling of the outgoing HDLC frames (the outgoing SPE bytes) using the polynomial $X^{43} + 1$. The scrambling is performed after the HDLC frames have been mapped into SPE (after FCS checking, byte stuffing, etc.). The self-synchronous scrambling can be disabled by setting XmtScrEn = '0' (register T_PHCCNF).

7.2.8 Performance Monitoring Counters

- The number of packets read from the transmit FIFO and transmitted into HDLC frames are counted in a 27-bit counter (register T_FRMCNT). This counter only counts the non aborted frames, i.e., the frames aborted by the user or unsuccessfully transmitted due to a FIFO underflow error are not counted.
- The number of bytes read from the transmit FIFO and transmitted into the generated HDLC frames are counted in a 29-bit counter (register T_BYTECNT).
- The number of HDLC frames that have been aborted by the user are counted in a 20-bit counter (register T_AFCNT).
- The number of HDLC frames that have been aborted by the HDLC controller due to a transmit FIFO underflow are counted in a 16-bit counter (register T_PFUCNT).

8.0 POS-UTOPIA Interface Functional Description

The Intel IXF6048 UTOPIA interface is configured in either ATM mode (ATM-UTOPIA interface) or in POS mode (POS-UTOPIA), depending on the configuration of the channel being accessed through the interface. The configuration of the interface is totally independent in both the transmit and the receive directions. When a transmit (or receive) channel is configured in ATM mode (RcvChMode[1:0] = '11' in register R_COCNF or XmtChMode[1:0] = '11' in register T_COCNF), the transmit (or receive) UTOPIA interface operates in POS mode for this channel. It is possible to have a mixed configuration of channels working in ATM mode and channels in POS mode.

The POS-UTOPIA interface connects a Link Layer device to the Intel IXF6048 (a Physical Layer device). The POS-UTOPIA interface is an extension of the ATM industry standard UTOPIA, adapted to support the transfer of variable length packets.

The interface can operate using a port selection cycle (such as the ATM-UTOPIA interface) or with no port selection cycle.

- When the POS-UTOPIA interface is configured to use a port selection cycle, the interface operates in the same way as the ATM-UTOPIA interface: two processes (data transfer and FIFO status polling) are performed simultaneously.
- When the POS-UTOPIA interface is configured to **not** use a port selection cycle, the interface operates as a simple memory mapped device.

The interface can operate at up to 104 MHz in the single 32-bit, 16-bit, and 8-bit modes as well as in the quad 8-bit mode. The interface can operate at up to 52 MHz in the single 64-bit mode and the quad 16-bit mode.

The receive and transmit FIFO memories provide for the separation of the Physical Layer timing and the Data Link Layer timing. The FIFOs are also necessary to handle the rate differences caused by the insertion/removal of Control Escape characters:

- When Intel IXF6048 is configured as a Single concatenated transceiver (a single Physical port transporting a single HDLC frame stream), only one channel is enabled and connected to the interface using a 2 or 16-Kbyte FIFO memory (selectable).
- When Intel IXF6048 is configured as a Quad transceiver (four Physical ports) or as a Single non-concatenated transceiver (a single Physical port transporting four independent HDLC frame streams), channel #0 is connected to the interface using a 16-Kbyte FIFO memory while channels #1, #2, and #3 use a 2-Kbyte FIFO memory. Optionally, the size of the FIFO for channel #0 can be limited to 2-Kbytes by setting XmtSmallMem (transmission) in register T_UICNF and RcvSmallMem (reception) in register R_UICNF.

The interface can be configured as a single interface or as four independent 8-bit interfaces by setting RcvUMode[1:0] in register R_UICNF.

Figure 56. POS-UTOPIA Physical Layer/Link Layer Rate Decoupling FIFOs in Multi-Channel Configuration

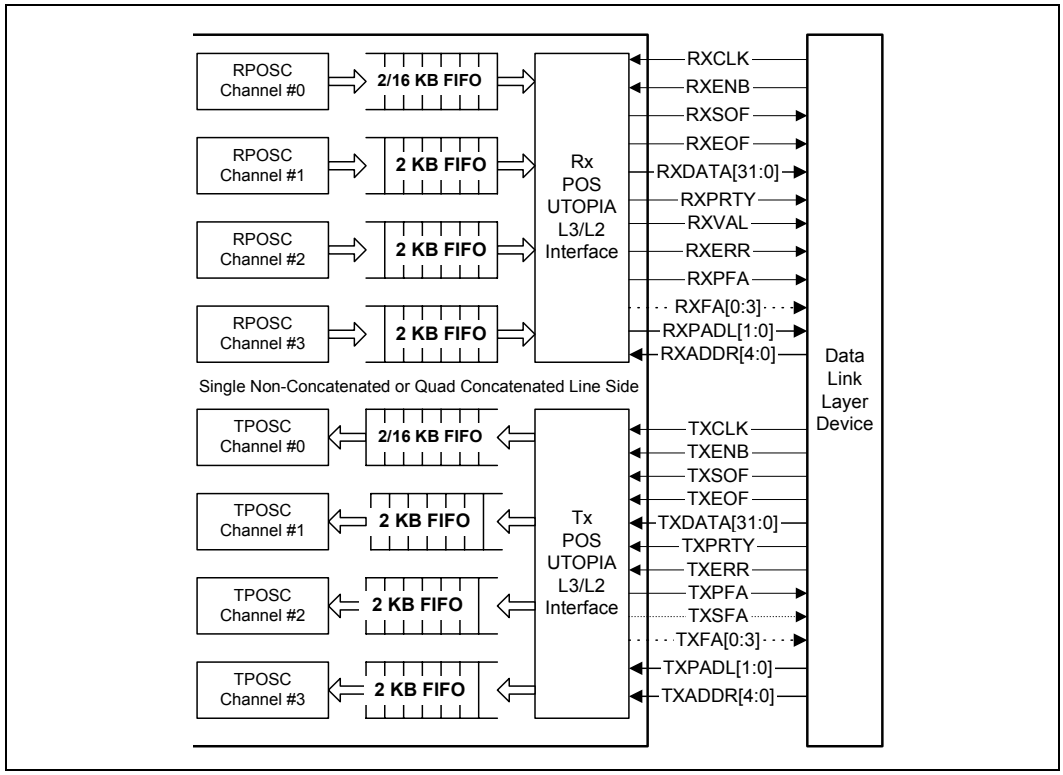


Figure 57. POS-UTOPIA Physical Layer/Link Layer Rate Decoupling FIFO in Single-Channel Configuration

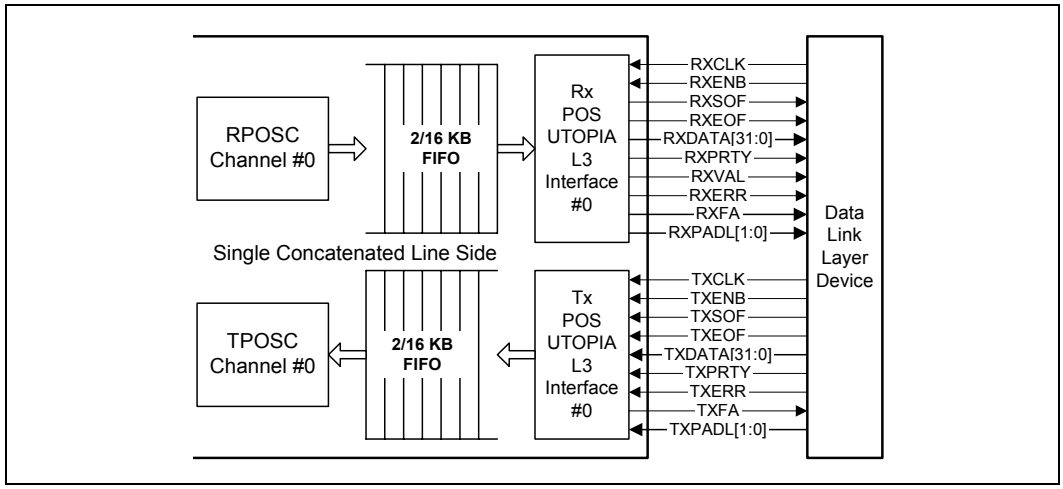
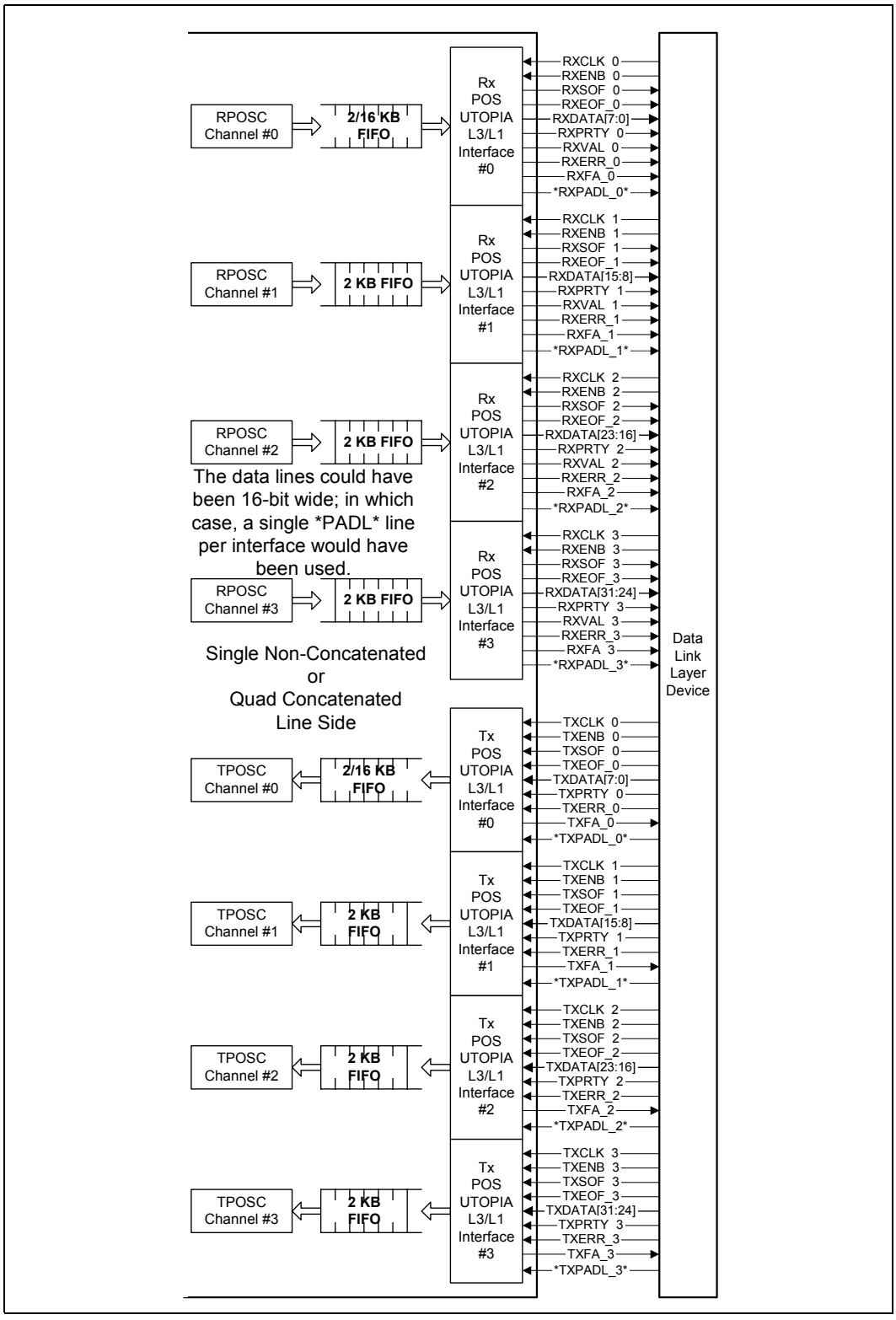


Figure 58. Four Independent POS-UTOPIA Interfaces



8.1 Data Bus Width and Packet Data Structure

The transmit data bus width and receive data bus width can be set independently.

The receive data bus width is configured by setting RcvUMode[1:0] in global register R_UICNF. Outputs RXDATA[31:0] are always part of the UTOPIA interface whereas RXDATA[63:32] use outputs from the TTL line side interface or from overhead ports (see the pinout description).

Table 24. UTOPIA Receive Data Bus Width

RcvUMode[1:0]	Data Bus Width	Line Status
'00'	8-bit	**Single Mode**: RXDATA[7:0] data bus. RXDATA [31:8] tristated. RXDATA[63:32] are not used in the UTOPIA interface. **Quad Mode**: RXDATA[7:0] ch 0 data. RXDATA[15:8] ch 1 data. RXDATA[23:16] ch 2 data. RXDATA[31:24] ch 3 data. RXDATA[63:32] are not used in the UTOPIA interface.
'01'	16-bit	**Single Mode**: RXDATA[15:0] data bus. RXDATA[31:16] tristated. RXDATA[63:32] are not used in the UTOPIA interface. **Quad Mode**: RXDATA[15:0] ch 0 data. RXDATA[31:16] ch 1 data. RXDATA[47:32] ch 2 data. RXDATA[63:48] ch 3 data.
'10'	32-bit	RXDATA[31:0] data bus. RXDATA[63:32] are not used in the UTOPIA interface.
'11'	64-bit	RXDATA[63:0] data bus.

The transmit data bus width is configured by setting XmtUMode[1:0] in global register T_UICNF. Inputs TXDATA[31:0] are always part of the UTOPIA interface whereas TXDATA[63:32] use inputs from the TTL line side interface or from overhead ports (see the pinout description).

For both transmit and receive interfaces, all three PADL lines would be used in the 64-bit wide UTOPIA data bus mode to indicate unused padding in the last UTOPIA interface clocking.

Table 25. UTOPIA Transmit Data Bus Width

XmtUMode[1:0]	Data Bus Width	Line Status
'00'	8-bit	**Single Mode**: TXDATA[7:0] data bus. TXDATA[31:8] tristated. TXDATA[63:32] are not used in the UTOPIA interface. **Quad Mode**: TXDATA[7:0] ch 0 data. TXDATA[15:8] ch 1 data. TXDATA[23:16] ch 2 data. TXDATA[31:24] ch 3 data. TXDATA[63:32] are not used in the UTOPIA interface.
'01'	16-bit	**Single Mode**: TXDATA[15:0] data bus. TXDATA[31:16] tristated. TXDATA[63:32] are not used in the UTOPIA interface. **Quad Mode**: TXDATA[15:0] ch 0 data. TXDATA[31:16] ch 1 data. TXDATA[47:32] ch 2 data. TXDATA[63:48] ch 3 data.
'10'	32-bit	TXDATA[31:0] data bus. TXDATA[63:32] are not used in the UTOPIA interface.
'11'	64-bit	TXDATA[63:0] data bus.

The POS-UTOPIA interface offers three different POS-packet formats.

The first format transports the Information field of the HDLC frame. This format is selected by setting RcvACPass = '0' and RcvFCSPass = '0' in register R_PHCCNF. In transmission, this format is selected by setting XmtACPass = '0' in register T_PHCCNF.

The second format transports the Address, Control and Information fields of the HDLC frame. In reception, this format is selected by setting RcvACPass = '1' and RcvFCSPass = '0' in register R_PHCCNF. In transmission, this format is selected by setting XmtACPass = '1' in register T_PHCCNF.

The third format transports the information and the FCS field of the HDLC frame. This format is selected by setting RcvACPass = '0' and RcvFCSPass = '1' in register R_PHCCNF. In transmission, this format is selected by setting XmfFCSCnf = '00' in register T_PHCCNF.

Figure 59. POS-Packet Format

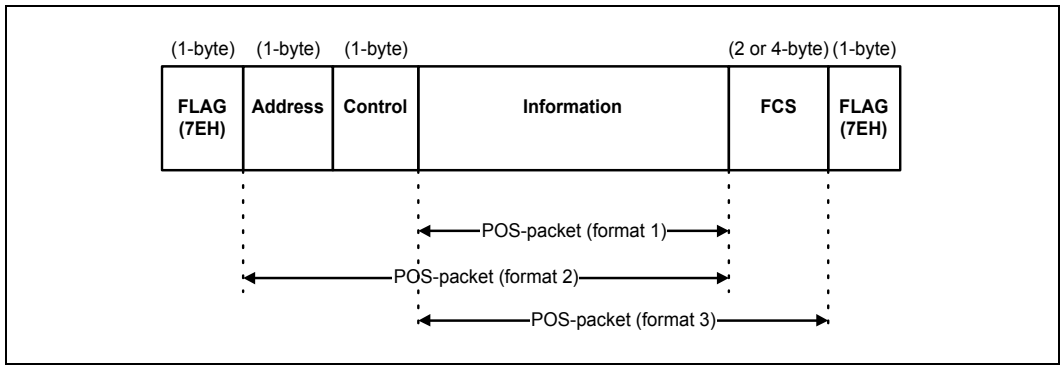


Figure 60, Figure 61, Figure 62, and Figure 63 show the POS-packet data structure transferred in the POS-UTOPIA interface (transmit and receive directions) for the different data bus widths.

The most significant bit of a word is the first received bit. The first word of the data structure (word one) in the RXDATA (TXDATA) bus is coincident with the RXSOF (TXSOF) indication. The last word of the data structure in RXDATA (TXDATA) is coincident with the RXEOF (TXEOF) indication.

The first byte of a packet is always transferred in the most-significant byte of the first word. POS-packets are transferred as a continuous stream; no padding bytes allowed between the first byte and the last byte of the packet. Only the last word can contain padding byte(s) in the less-significant byte(s).

In reception, output RXPADL (RXPADL[2:0] in 64-bit mode, RXPADL[1:0] in 32-bit mode, and RXPADL[0] in 16-bit mode) indicates the number of padding bytes contained in the last word; RXPADL is only valid when RXEOF is active.

In transmission, input TXPADL indicates the number of padding bytes contained in the last word (TXPADL[2:0] in 64-bit mode, TXPADL[1:0] in 32-bit mode, and TXPADL[0] in 16-bit mode); TXPADL is only valid when TXEOF is active.

Figure 60. POS-Packet Data Structure Using the 64-Bit UTOPIA Interface

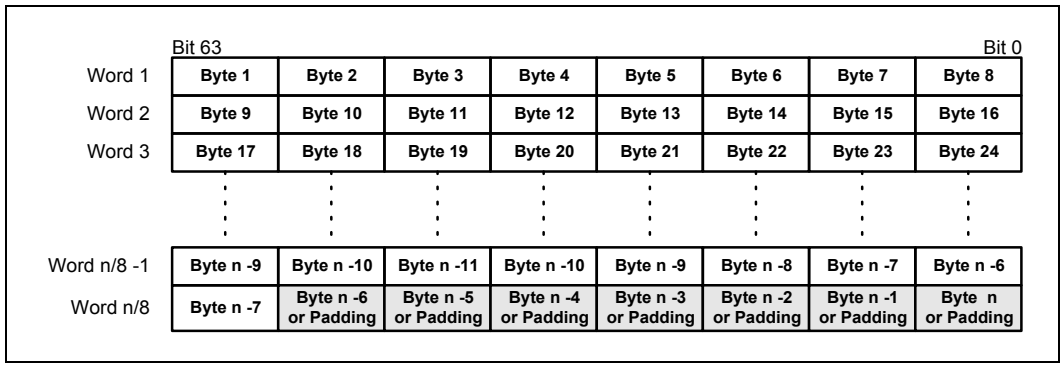


Figure 61. POS-Packet Data Structure Using the 32-Bit UTOPIA Interface

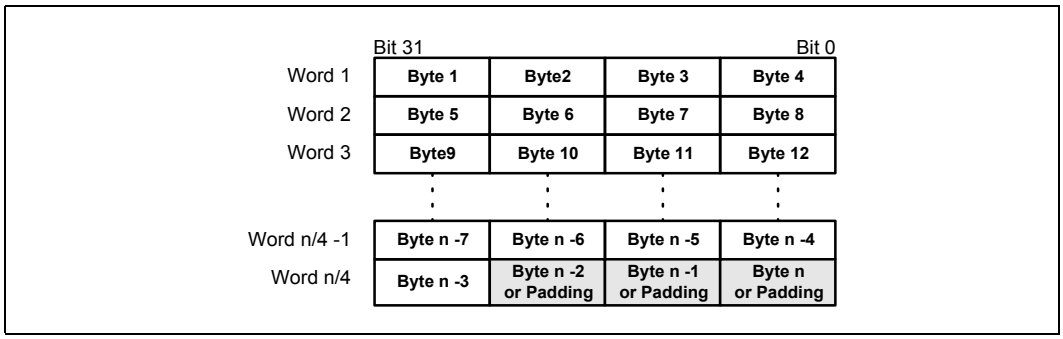


Figure 62. POS-Packet Data Structure Using the 16-Bit UTOPIA Interface

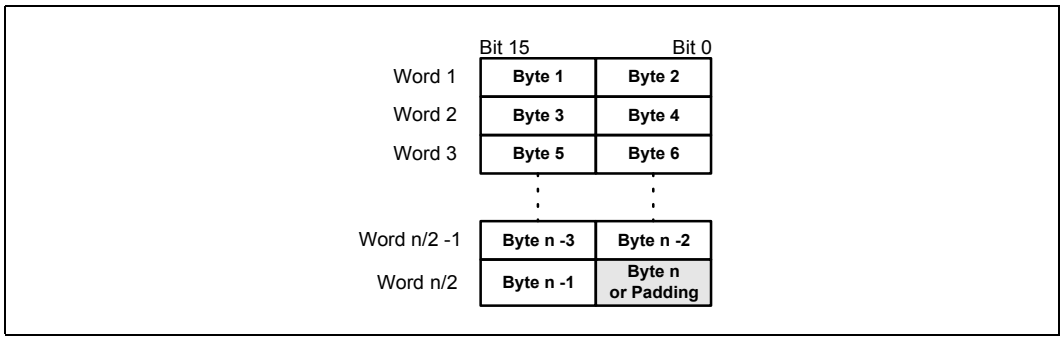
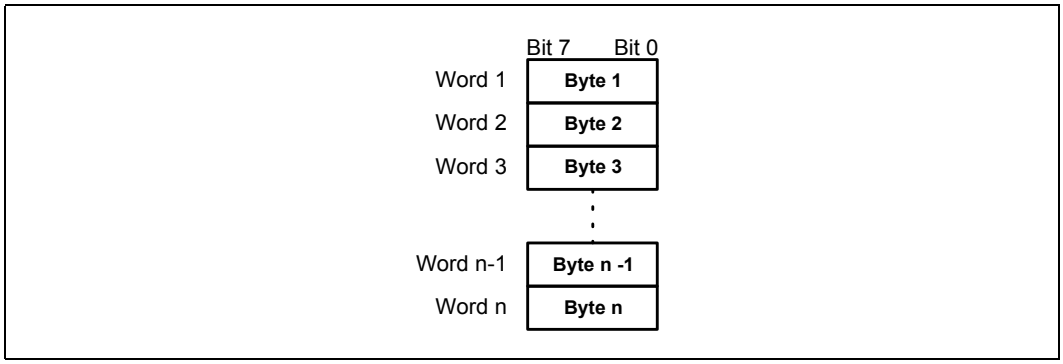


Figure 63. POS-Packet Data Structure Using the 8-Bit UTOPIA Interface



8.2 Receive POS-UTOPIA Interface

8.2.1 Port Selection Mode

The receive POS-UTOPIA interface can be configured to operate as the ATM-UTOPIA interface (using a port selection cycle) or as a simple memory mapped device.

- When configuration bit RcvSelMode = '0' (global register R_UICNF), the receive POS-UTOPIA interface operates in a similar way to the ATM-UTOPIA interface. Two independent processes run in parallel: the data transfer and the FIFO status polling. RXADDR[4:0] are used to poll the status of the FIFOs (using the output RXPFA) and to select a port when

RXENB changes from '1' to '0'. Once the port is selected (RXENB = '0'), the receive address RXADDR[4:0] can take any value (FIFO status polling using RXPFA).

- When configuration bit RcvSelMode = '1' (global register R_UICNF), the receive POS-UTOPIA interface is controlled as a memory mapped device. There is no selection cycle or FIFO status polling, just port addressing. The RXPFA output is not used and the status of each FIFO is indicated using the direct outputs RXFA_0, RXFA_1, RXFA_2, and RXFA_3. Nothing happens when RXENB = '1'. If RXENB = '0', the interface reads a word from the FIFO addressed by RXADDR[4:0].

Each of the previous configurations requires the use of the RXVAL output. The Link-Layer device MUST use RXVAL to validate/invalidate the data read from the FIFO. The RXVAL output can be used in two different modes:

- When the bit RcvValCnf (in register R_UICNF) is set to logic zero, RXVAL assertion and deassertion is based only on the status of the receive FIFO. RXVAL is deasserted when attempting to read an empty FIFO (receive FIFO underflow). When the Link Layer device tries to read an empty FIFO, the read command is disregarded and the FIFO is not modified. The receive FIFO underflow is not considered an error (no data is lost).
- When the bit RcvValCnf (in register R_UICNF) is set to logic one, RXVAL is used in the same way as for RcvValCnf = '0' (invalidation of the output the signals if the FIFO is empty). In addition, RXVAL is also deasserted after reading the last word of a packet, i.e. the next word (start of the next packet) is not read from the FIFO. When RXVAL is deasserted, the conditions FIFO-empty and end-of packet are differentiated using RXEOF. This configuration allows the Link Layer device to synchronize with the packet boundaries.

Asserting RXVALCTRL the Link-Layer device indicates that it wants to stop reading the FIFO after the end of the current packet.

8.2.2 Decode-Response Configuration

RcvDRCnf (global register R_UICNF) configures the decode-response delay for the receive interface:

When RcvDRCnf = '0', the decode-response delay in the receive UTOPIA interface is one clock cycle:

- The delay from the receive address (RXADDR) to the receive polled frame available signal (RXPFA) is one clock cycle.
- The delay from the receive enable (RXENA) to the receive data (RXDATA[31:0], RXSOF, RXEOF, RXPADL[1:0], RXERR, RXVAL, and RXPRTY) is one clock cycle.

When RcvDRCnf = '1', the decode-response delay in the receive UTOPIA interface is two clock cycles:

- The delay from the receive address (RXADDR) to the receive polled frame available signal (RXPFA) is two clock cycles.
- The delay from the receive enable (RXENA) to the receive data (RXDATA[31:0], RXSOF, RXEOF, RXPADL[1:0], RXERR, RXVAL, and RXPRTY) is two clock cycles.

8.2.3 Single-Device/Multiple-Device Configuration

Intel IXF6048 can be configured to operate as the only device in the interface (driving the outputs always) or sharing the interface with other PHY devices (driving the outputs only when it is selected). This feature can be configured independently in the receive and transmit directions.

RcvMPhyDevCnf in global register R_UICNF controls the receive interface:

- When RcvMPhyDevCnf = '1', the receive outputs RXDATA[31:0], RXSOF, RXEOF, RXPADL[1:0], RXERR, RXVAL, and RXPRTY are only driven when the device is selected for a receive cell transfer while RXPFA is only driven when RXADDR matches the programmed device address. This setting **must** be used when Intel IXF6048 shares the receive interface with **other PHY devices**.
- When RcvMPhyDevCnf = '0', the receive outputs RXDATA[31:0], RXSOF, RXEOF, RXPADL[1:0], RXERR, RXVAL, RXPRTY, and RXFA are always driven. This setting **can** be used when Intel IXF6048 is the **only PHY device** in the receive interface.

The direct indication outputs RXFA_i (i = 0, 1, 2, 3) can be also configured to be driven always or driven only when RXADDR[4:0] matches the programmed device address.

RcvDirStatCnf (global register R_UICNF) configures the RXFA_i outputs in two different ways:

- When RcvDirStatCnf = '1' (direct status indication mode), the RXFA_i (i = 0, 1, 2, 3) outputs are always driven.
- When RcvDirStatCnf = '0' (multiplexed status polling), the RXFA_i (i = 0, 1, 2, 3) outputs are driven when RXADDR bus matches the programmed base-address value (UAddrBase, register GOCNF).

8.2.4 Receive POS-UTOPIA Interface Functional Timing Examples

Figure 64 shows an example where the receive interface has been configured in POS-UTOPIA Level 3 mode and only channel 0 is used. This could be for a single OC-1/3/12/48 concatenated line side input. This example corresponds to the following configuration:

- RcvUQuad = '0' (single interface)
- RcvUWidth[1:0] = '10' (32-bit interface)
- RcvSelMode = '1' (memory mapped port selection)
- RcvDRCnf = '1' (2 clock cycle decode-response time)
- RcvMPhyDevCnf = '0' (single PHY device)

Figure 66 shows an example where the receive interface has been configured in POS-UTOPIA Level 3 mode. This could be for a single OC-3/12/48 non-concatenated line side input or four OC-1/3/12 concatenated line side inputs. This example corresponds to the following configuration:

- RcvUQuad = '0' (single interface)
- RcvUWidth[1:0] = '11' (64-bit interface)
- RcvSelMode = '0' (ATM-like port selection)
- RcvDRCnf = '0' (1 clock cycle decode-response time)
- RcvMPhyDevCnf = '0' (single PHY device)

Figure 68 shows an example where the receive interface has been configured in POS-UTOPIA Level 3 mode. This could be for a single OC-3/12/48 non-concatenated line side input or four OC-1/3/12 concatenated line side inputs. This example corresponds to the following configuration:

- RcvUQuad = '0' (single interface)
- RcvUWidth[1:0] = '11' (64-bit interface)
- RcvSelMode = '0' (ATM-like port selection)
- RcvDRCnf = '1' (2 clock cycle decode-response time)
- RcvMPhyDevCnf = '1' (multiple PHY device)

Figure 70 shows an example where the receive interface has been configured in POS-UTOPIA Level 3 mode. This could be for a single OC-3/12/48 non-concatenated line side input or four OC-1/3/12 concatenated line side inputs. This example corresponds to the following configuration:

- RcvUQuad = '0' (single interface)
- RcvUWidth[1:0] = '10' (32-bit interface)
- RcvSelMode = '0' (ATM-like port selection)
- RcvDRCnf = '1' (2 clock cycle decode-response time)
- RcvMPhyDevCnf = '0' (single PHY device)

Figure 72 shows an example where the receive interface has been configured as a 32-bit MPHY device. This could be for a single OC-3/12/48 non-concatenated line side input or four OC-1/3/12 concatenated line side inputs. This example corresponds to the following configuration:

- RcvUQuad = '0' (single interface)
- RcvUWidth[1:0] = '10' (32-bit interface)
- RcvSelMode = '0' (ATM-like port selection)
- RcvDRCnf = '1' (2 clock cycle decode-response time)
- RcvMPhyDevCnf = '1' (multiple PHY device)

Figure 74 shows an example where the receive interface has been configured in POS-UTOPIA Level 2 mode. This could be for a single OC-3/12 non-concatenated line side input or four OC-1/3 concatenated line side inputs. This example corresponds to the following configuration:

- RcvUQuad = '0' (single interface)
- RcvUWidth[1:0] = '01' (16-bit interface)
- RcvSelMode = '0' (ATM-like port selection)
- RcvDRCnf = '0' (1 clock cycle decode-response time)
- RcvMPhyDevCnf = '1' (multiple PHY device)

Figure 76 shows an example where the receive interface has been configured as a 16-bit single device. This could be for a single OC-3/12 non-concatenated line side input or four OC-1/3 concatenated line side inputs. This example corresponds to the following configuration:

- RcvUQuad = '0' (single interface)
- RcvUWidth[1:0] = '01' (16-bit interface)
- RcvSelMode = '0' (ATM-like port selection)

- RcvDRCnf = '0' (1 clock cycle decode-response time)
- RcvMPhyDevCnf = '0' (single PHY device)

8.3 Transmit POS-UTOPIA Interface

8.3.1 Port Selection Mode

The transmit POS-UTOPIA interface can be configured to operate as the ATM-UTOPIA interface (using a port selection cycle) or as a simple memory mapped device.

- When configuration bit XmtSelMode = '0' (global register T_UICNF), the transmit POS-UTOPIA interface operates in a similar way to the ATM-UTOPIA interface. Two independent processes run in parallel: the data transfer and the FIFO status polling. TXADDR[4:0] are used to poll the status of the FIFOs (using the output TXPFA) and to select a port when TXENB changes from '1' to '0'. Once the port is selected (TXENB = '0'), the transmit address TXADDR[4:0] can take any value (FIFO status polling using TXPFA).
- When configuration bit XmtSelMode = '1' (global register T_UICNF), the transmit POS-UTOPIA interface is controlled as a memory mapped device. There is no selection cycle or FIFO status polling, just port addressing. The TXPFA output is not used and the status of each FIFO is indicated using the direct outputs TXFA_0, TXFA_1, TXFA_2, and TXFA_3. Nothing happens when TXENB = '1'. If TXENB = '0', the interface writes the word transported on TXDATA into the FIFO addressed by TXADDR[4:0].

8.3.2 Decode-Response Configuration

XmtDRCnf (global register T_UICNF) configures the decode-response delay for the receive interface:

When XmtDRCnf = '0', the decode-response delay in the receive UTOPIA interface is one clock cycle:

- The delay from the transmit address (TXADDR) to the receive polled frame available signal (TXPFA) is one clock cycle.

When XmtDRCnf = '1', the decode-response delay in the receive UTOPIA interface is two clock cycles:

- The delay from the transmit address (RXADDR) to the receive polled frame available signal (RXPFA) is two clock cycles.

8.3.3 Single-Device/Multiple-Device Configuration

Intel IXF6048 can be configured to operate as the only device in the interface (driving the outputs always) or sharing the interface with other PHY devices (driving the outputs only when it is selected). This feature can be configured independently in the receive and transmit directions.

XmtMPhyDevCnf in global register T_UICNF controls the receive interface:

- When XmtMPhyDevCnf = '1', TXPFA is only driven when TXADDR matches the programmed device address. This setting **must** be used when Intel IXF6048 shares the transmit interface with **other PHY devices**.

- When XmtMPhyDevCnf = '0', TXPFA is always driven. This setting **can** be used when Intel IXF6048 is the **only PHY device** in the transmit interface.

The direct indication outputs TXFA_i (i = 0, 1, 2, 3) can be also configured to be driven always or driven only when RXADDR[4:0] matches the programmed device address.

XmtDirStatCnf (global register T_UICNF) configures the TXFA_i outputs in two different ways:

- When XmtDirStatCnf = '1' (direct status indication mode), the TXFA_i (i = 0, 1, 2, 3) outputs are always driven.
- When XmtDirStatCnf = '0' (multiplexed status polling), the TXFA_i (i = 0, 1, 2, 3) outputs are driven only when the TXADDR bus matches the programmed base-address value (UAddrBase, register GOCNF).

8.3.4 Transmit POS-UTOPIA Interface Functional Timing Examples

Figure 65 shows an example where the transmit interface has been configured in POS-UTOPIA Level 3 mode and only channel 0 is used. This could be for a single OC-1/3/12/48 concatenated line side input. This example corresponds to the following configuration:

- XmtUQuad = '0' (single interface)
- XmtUWidth[1:0] = '10' (32-bit interface)
- XmtSelMode = '1' (memory mapped port selection)
- XmtDRCnf = '1' (2 clock cycle decode-response time)
- XmtMPhyDevCnf = '0' (single PHY device)

Figure 67 shows an example where the transmit interface has been configured in POS-UTOPIA Level 3 mode. This could be for a single OC-3/12/48 non-concatenated line side input or four OC-1/3/12 concatenated line side inputs. This example corresponds to the following configuration:

- XmtUQuad = '0' (single interface)
- XmtUWidth[1:0] = '11' (64-bit interface)
- XmtSelMode = '0' (ATM-like port selection)
- XmtDRCnf = '0' (1 clock cycle decode-response time)
- XmtMPhyDevCnf = '0' (single PHY device)

Figure 69 shows an example where the transmit interface has been configured in POS-UTOPIA Level 3 mode. This could be for a single OC-3/12/48 non-concatenated line side input or four OC-1/3/12 concatenated line side inputs. This example corresponds to the following configuration:

- XmtUQuad = '0' (single interface)
- XmtUWidth[1:0] = '11' (64-bit interface)
- XmtSelMode = '0' (ATM-like port selection)
- XmtDRCnf = '1' (2 clock cycle decode-response time)
- XmtMPhyDevCnf = '1' (multiple PHY device)

Figure 71 shows an example where the transmit interface has been configured in POS-UTOPIA Level 3 mode. This could be for a single OC-3/12/48 non-concatenated line side input or four OC-1/3/12 concatenated line side inputs. This example corresponds to the following configuration:

- XmtUQuad = '0' (single interface)
- XmtUWidth[1:0] = '10' (32-bit interface)
- XmtSelMode = '0' (ATM-like port selection)
- XmtDRCnf = '1' (2 clock cycle decode-response time)
- XmtMPhyDevCnf = '0' (single PHY device)

Figure 73 shows an example where the transmit interface has been configured as a 32-bit MPHY device. This could be for a single OC-3/12/48 non-concatenated line side input or four OC-1/3/12 concatenated line side inputs. This example corresponds to the following configuration:

- XmtUQuad = '0' (single interface)
- XmtUWidth[1:0] = '10' (32-bit interface)
- XmtSelMode = '0' (ATM-like port selection)
- XmtDRCnf = '1' (2 clock cycle decode-response time)
- XmtMPhyDevCnf = '1' (multiple PHY device)

Figure 75 shows an example where the transmit interface has been configured in POS-UTOPIA Level 2 mode. This could be for a single OC-3/12 non-concatenated line side input or four OC-1/3 concatenated line side inputs. This example corresponds to the following configuration:

- XmtUQuad = '0' (single interface)
- XmtUWidth[1:0] = '01' (16-bit interface)
- XmtSelMode = '0' (ATM-like port selection)
- XmtDRCnf = '0' (1 clock cycle decode-response time)
- XmtMPhyDevCnf = '1' (multiple PHY device)

Figure 77 shows an example where the transmit interface has been configured as a 16-bit single device. This could be for a single OC-3/12 non-concatenated line side input or four OC-1/3 concatenated line side inputs. This example corresponds to the following configuration:

- XmtUQuad = '0' (single interface)
- XmtUWidth[1:0] = '01' (16-bit interface)
- XmtSelMode = '0' (ATM-like port selection)
- XmtDRCnf = '0' (1 clock cycle decode-response time)
- XmtMPhyDevCnf = '0' (single PHY device)

Figure 64. Receive POS-UTOPIA Interface as a Single PHY Device with 32-Bit Data Bus Using Port Selection (POS-UTOPIA Level 3 Mode and Only Channel 0 Is Used)

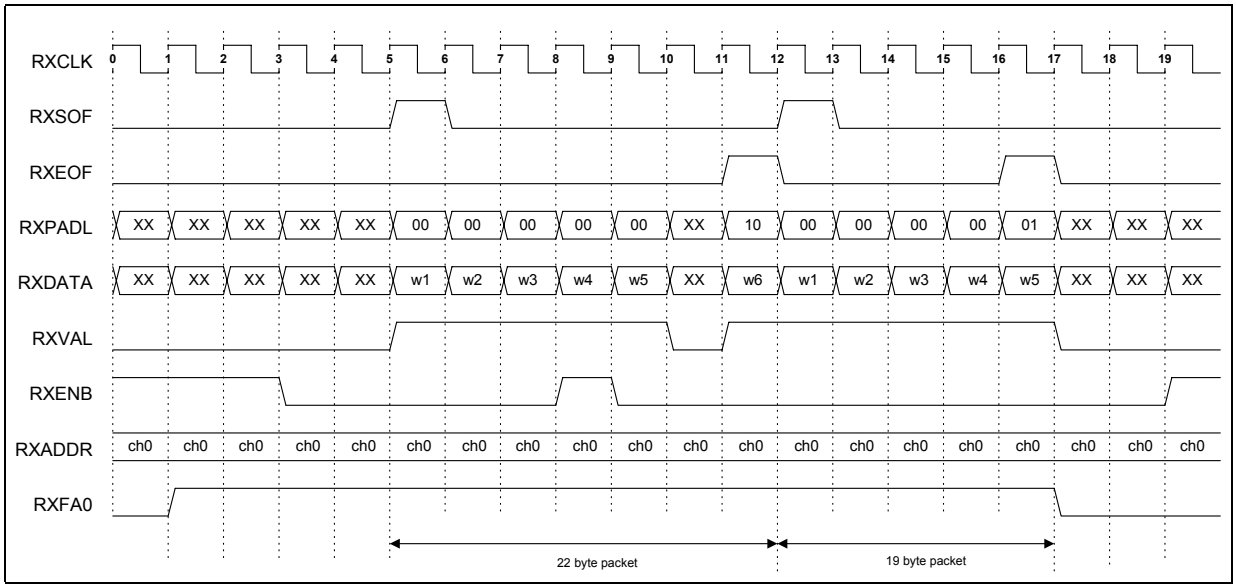


Figure 65. Transmit POS-UTOPIA Interface as a Single PHY Device with 32-Bit Data Bus Using Port Selection (POS-UTOPIA Level 3 Mode and Only Channel 0 Is Used)

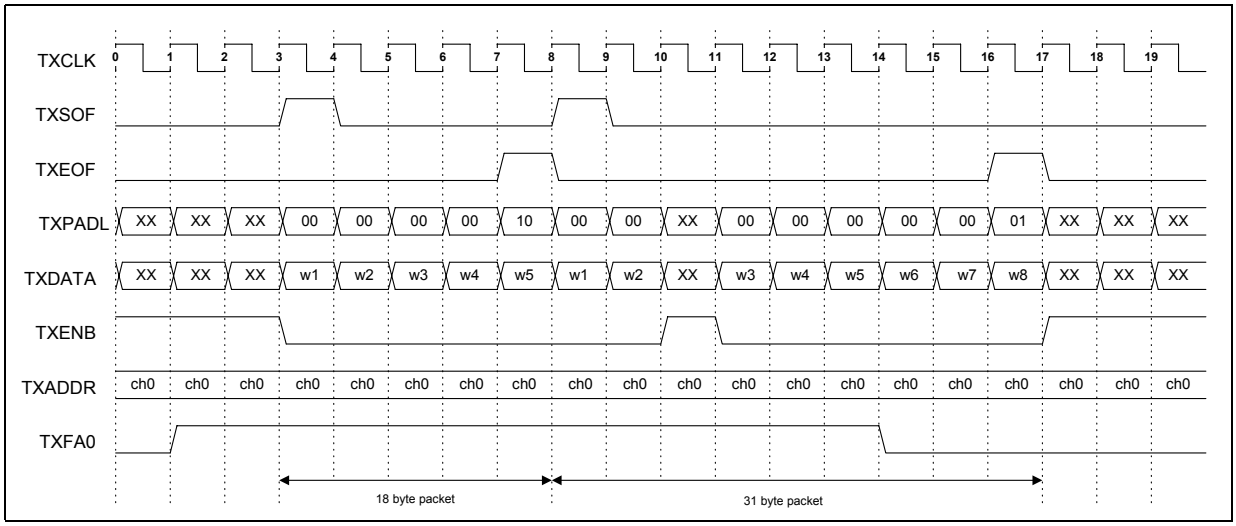


Figure 66. Receive POS-UTOPIA Interface as a Single PHY Device with 64-Bit Data Bus Using Port Selection (POS-UTOPIA Level 3 Mode)

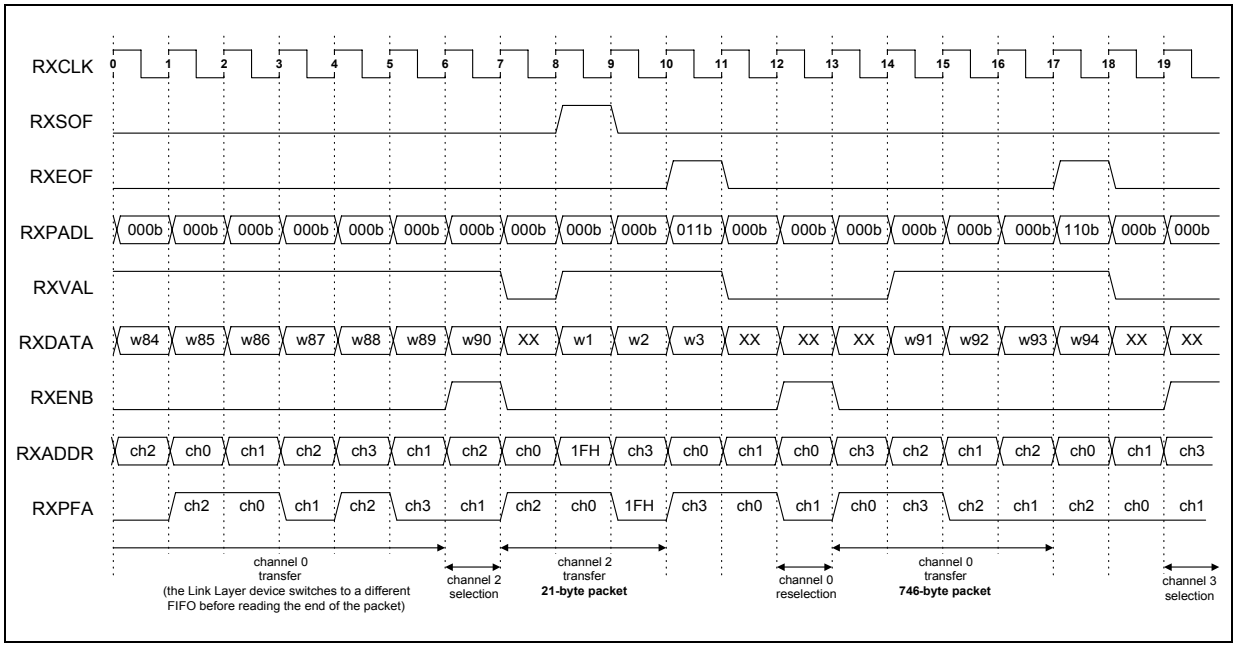


Figure 67. Transmit POS-UTOPIA Interface as a Single PHY Device with 64-Bit Data Bus Using Port Selection (POS-UTOPIA Level 3 Mode)

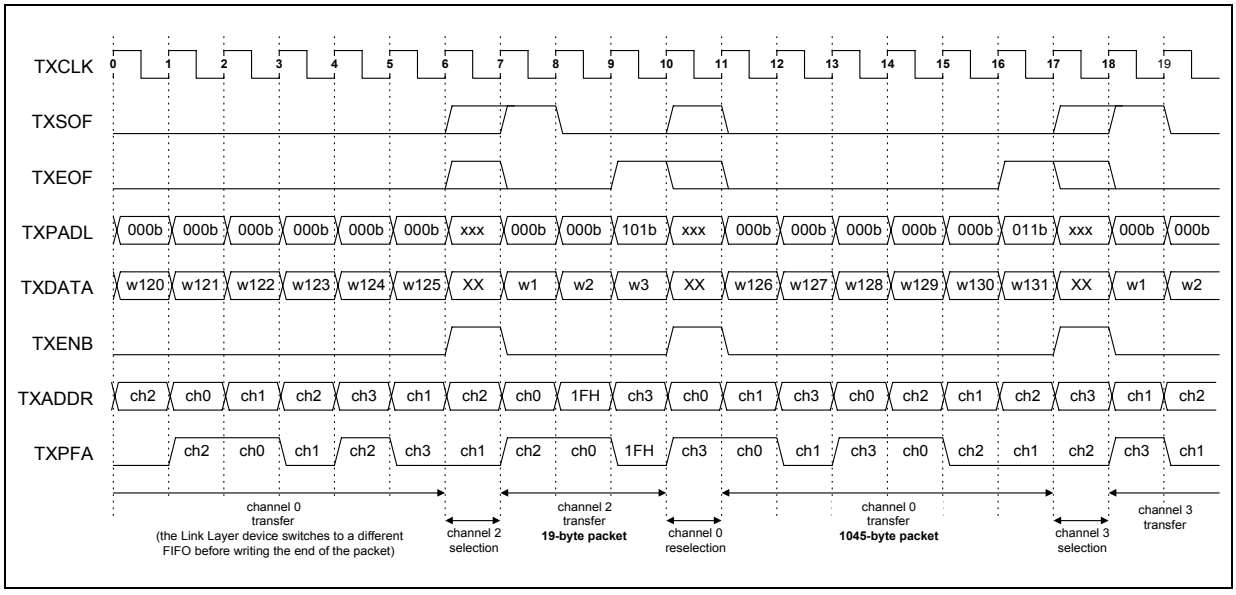


Figure 68. Receive POS-UTOPIA Interface as a Multiple PHY Device with 64-Bit Data Bus Using Port Selection (POS-UTOPIA Level 3 Mode)

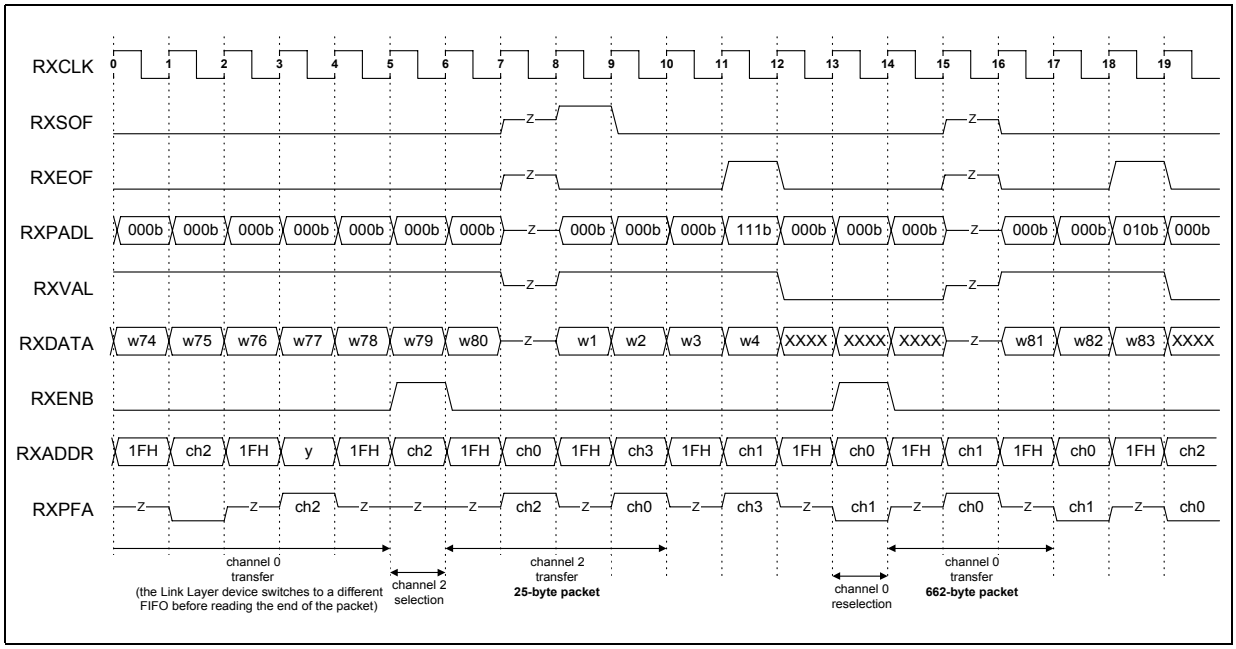


Figure 69. Transmit POS-UTOPIA Interface as a Multiple PHY Device with 64-Bit Data Bus Using Port Selection (POS-UTOPIA Level 3 Mode)

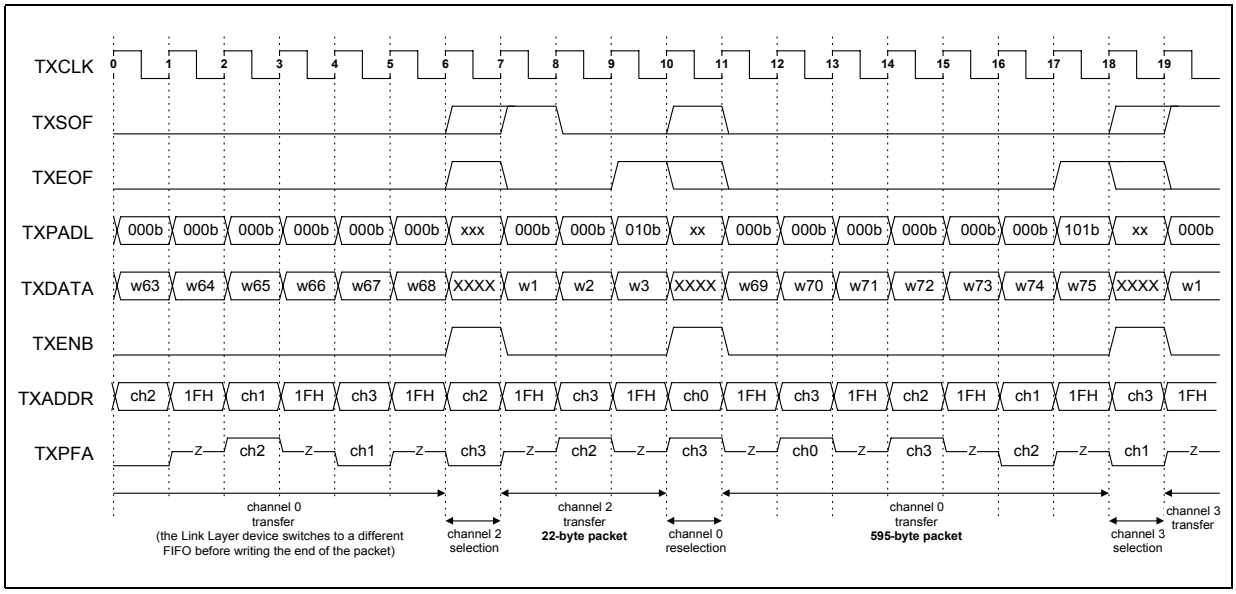


Figure 70. Receive POS-UTOPIA Interface as a Single PHY Device with 32-Bit Data Bus Using Port Selection (POS-UTOPIA Level 3 Mode)

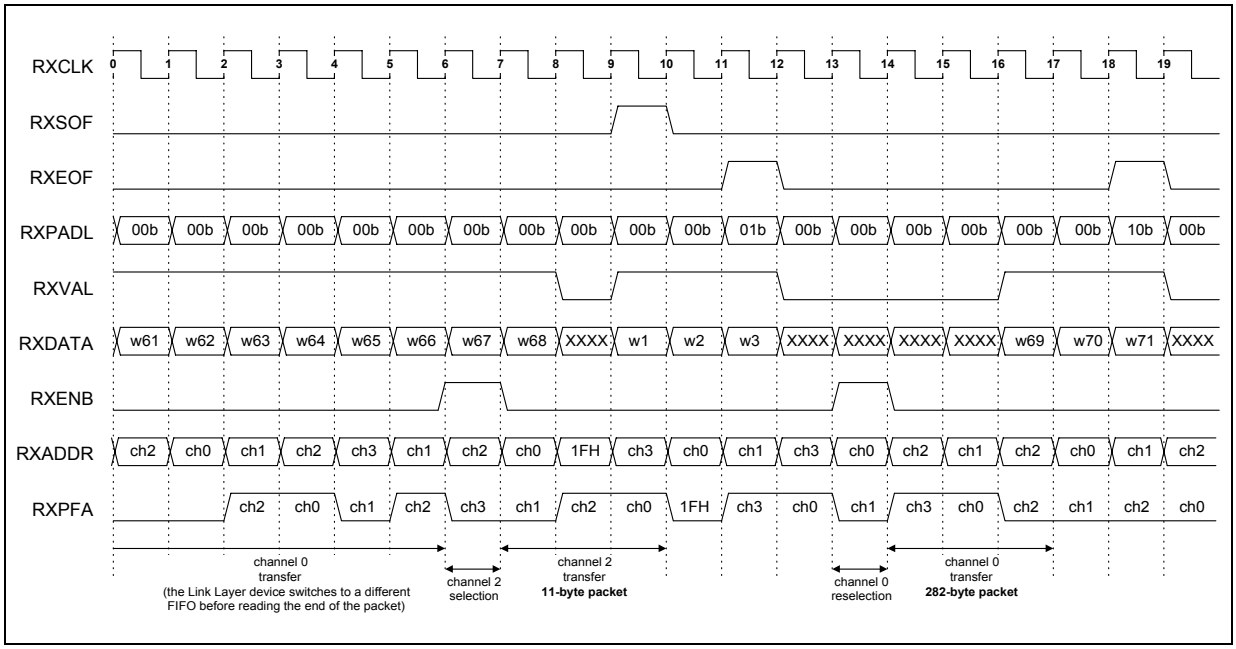


Figure 71. Transmit POS-UTOPIA Interface as a Single PHY Device with 32-Bit Data Bus Using Port Selection (POS-UTOPIA Level 3 Mode)

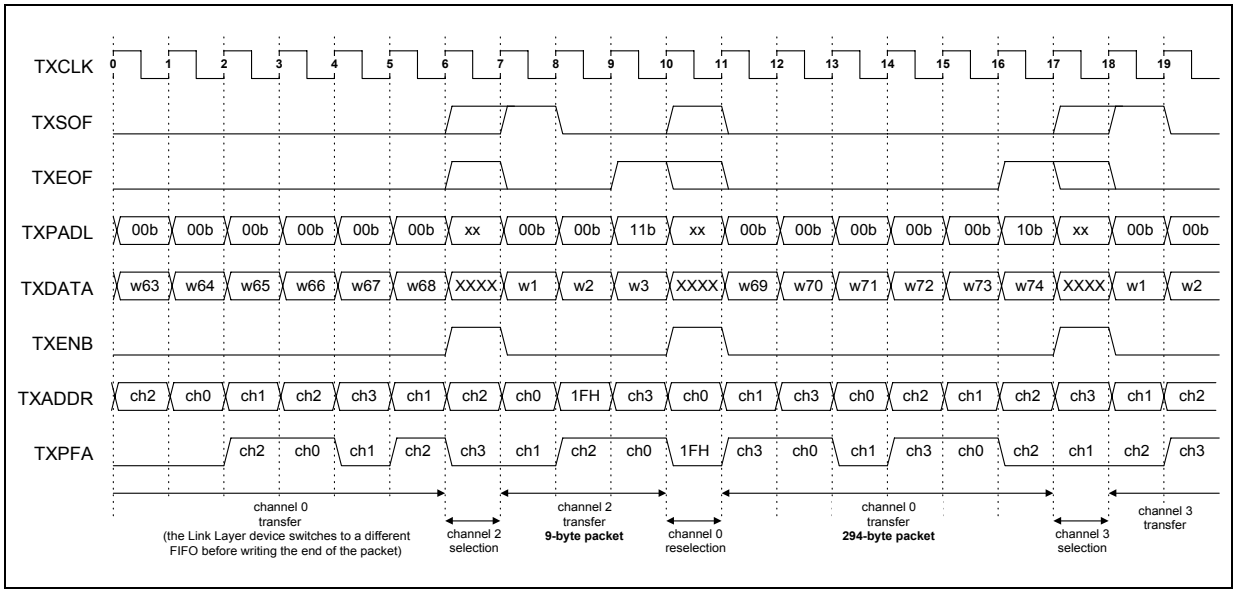


Figure 72. Receive POS-UTOPIA Interface as a Multiple PHY Device with 32-Bit Data Bus Using Port Selection

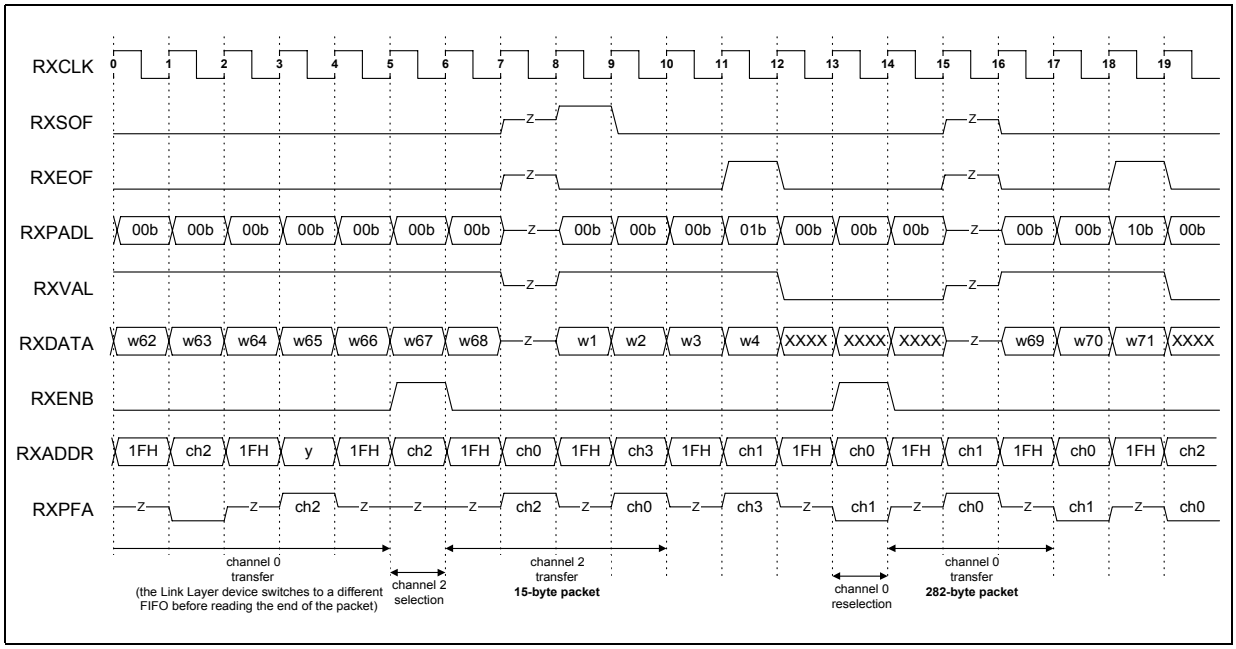


Figure 73. Transmit POS-UTOPIA Interface as a Multiple PHY Device with 32-Bit Data Bus Using Port Selection

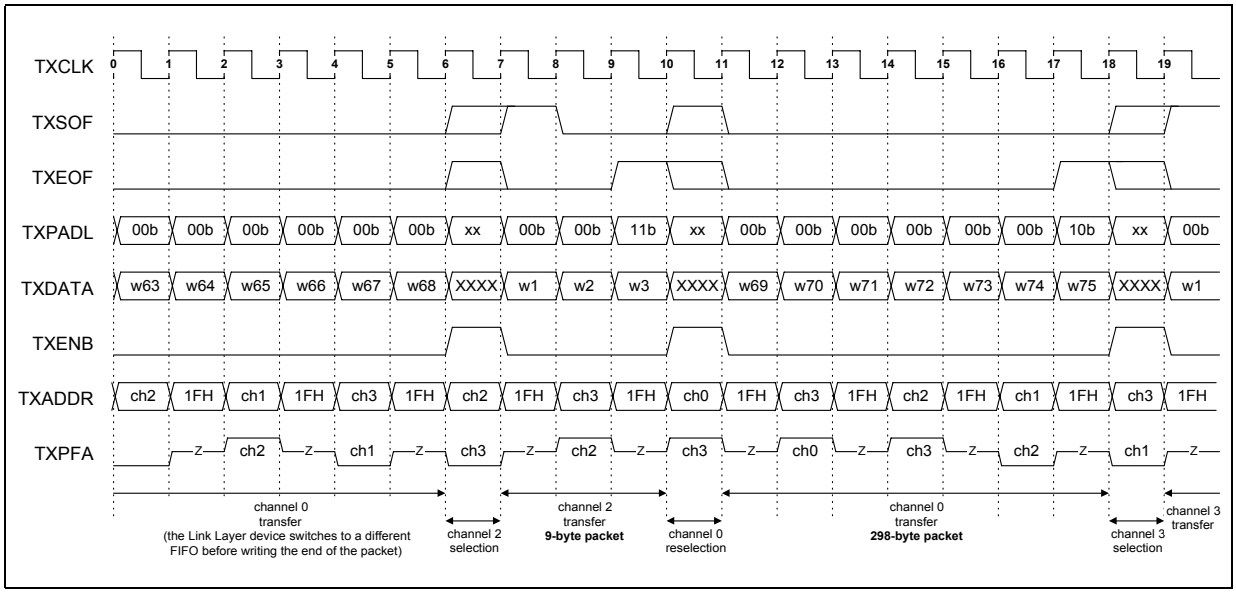


Figure 74. Receive POS-UTOPIA Interface as a Multiple PHY Device with 16-Bit Data Bus Using Port Selection (POS-UTOPIA Level 2 Mode)

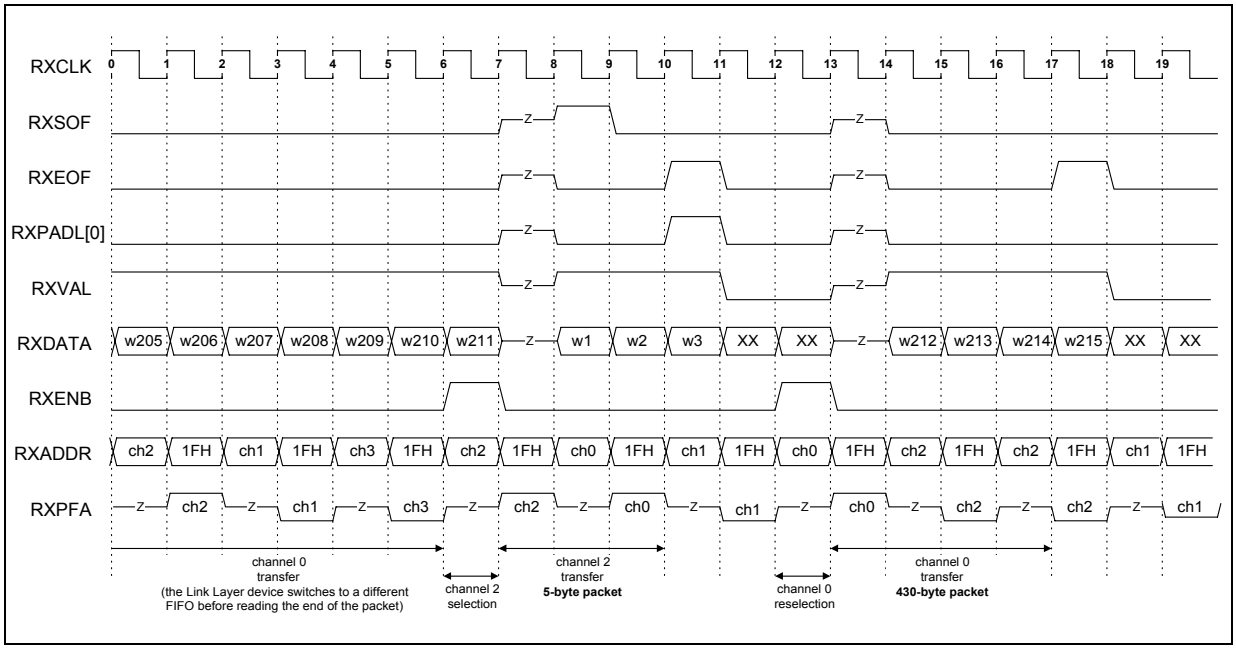


Figure 75. Transmit POS-UTOPIA Interface as a Multiple PHY Device with 16-Bit Data Bus Using Port Selection (POS-UTOPIA Level 2 Mode)

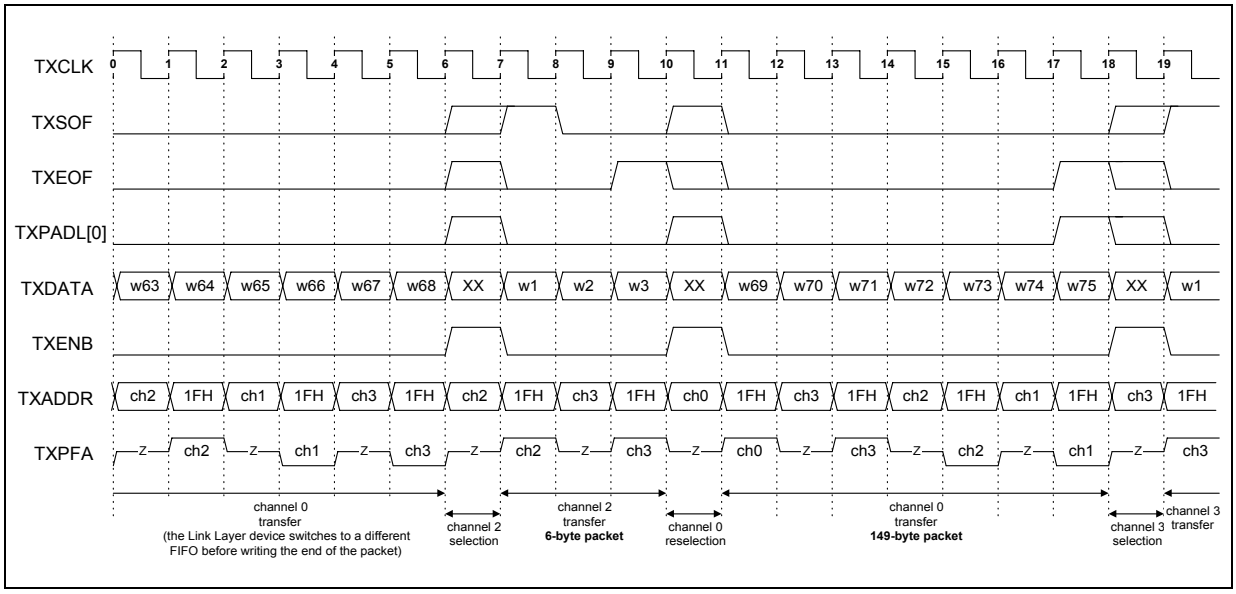


Figure 76. Receive POS-UTOPIA Interface as a Single PHY Device with 16-Bit Data Bus Using Port Selection

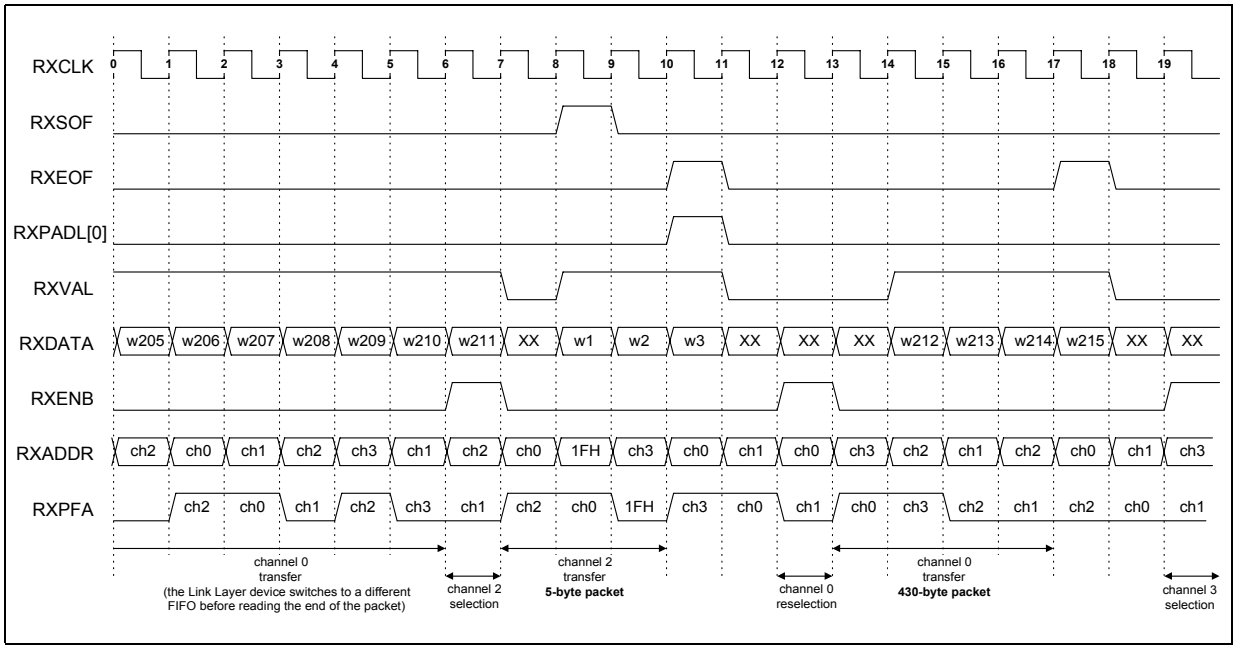
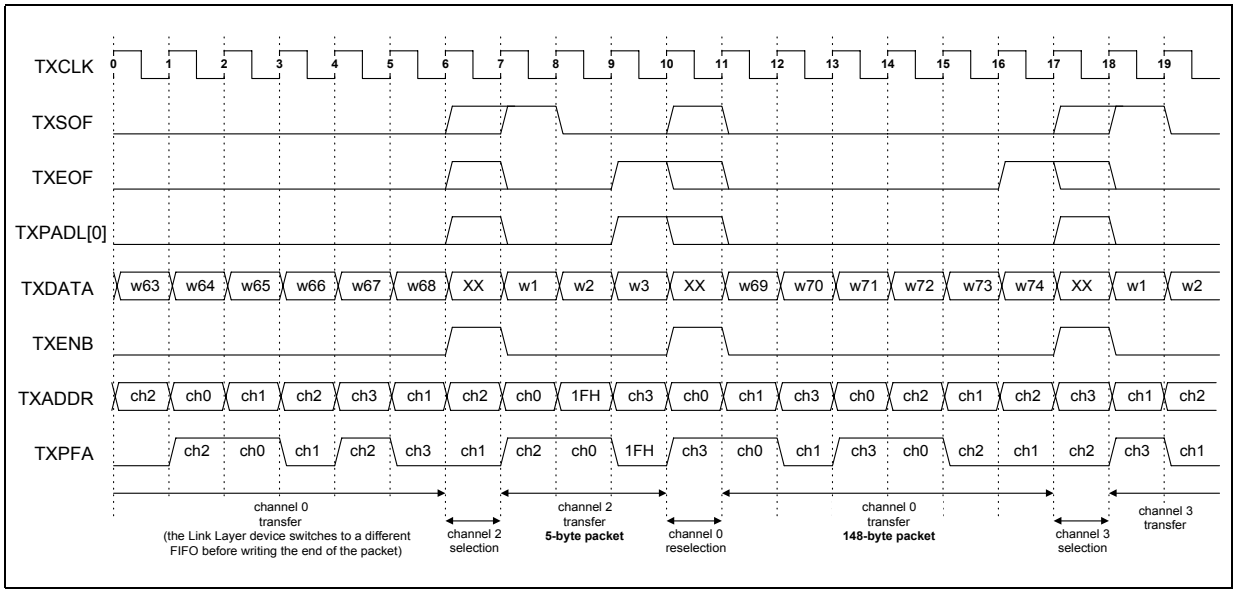


Figure 77. Transmit POS-UTOPIA Interface as a Single PHY Device with 16-Bit Data Bus Using Port Selection



9.0 Transparent Mode Functional Description

The Intel IXF6048 provides direct mapping from the system interface to the SONET/SDH SPE in the transmit direction and direct extraction of the SONET/SDH SPE through the system interface. This capability can be used to bypass the ATM and POS processors and map other protocols, like Ethernet, into SONET/SDH.

9.1 Receive Direction

Each Intel IXF6048 channel, when configured in transparent mode in the receive direction (RcvChMode in register R_COCNF), writes the full contents of the SPE to a FIFO buffer. The contents of the FIFO can be read through the UTOPIA interface.

The data coming from the SPE can be optionally descrambled (RcvTrDescrEn in register R_COCNF) before it is written into the FIFO using the self-synchronous scrambler $1 + X^{43}$.

When a channel is configured in transparent mode, the UTOPIA interface behaves as if the channel were configured in POS mode except for the fact that all the signals used to delineate frames are not used. Thus, RXSOF (start of frame), RXEOF (end of frame), RXPADL (padding length) and RXABORT should be ignored. FIFO size configuration, watermarks and status signals as well as the channel addressing and channel selection mechanisms work in the same way as when the interface is configure in POS-UTOPIA mode.

The external demapper should be able to read data fast and frequently enough to prevent the FIFO from overflowing. When a FIFO overflow occurs, an interrupt RcvFifoOFI in register R_UTOINT) is asserted.

9.2 Transmit Direction

Each Intel IXF6048 channel, when configured in transparent mode in the transmit direction (XmtChMode in register T_COCNF), reads the contents of the SPE from an external mapper. In this mode, the data written by an external mapper to a FIFO buffer through a UTOPIA-like interface is used to fill the SDH container for each channel.

The data read from the FIFO and mapped into the SPE can be optionally scrambled (XmtTrScrEn in register T_COCNF) using the self-synchronous scrambler $1 + X^{43}$.

When a channel is configured in transparent mode, the UTOPIA interface behaves as if the channel were configured in POS mode except for the fact that all the signals used to delineate frames are not used. Thus, TXSOF (start of frame), TXEOF (end of frame), TXPADL (padding length) and TXABORT are not used. FIFO size configuration, watermarks and status signals as well as the channel addressing and channel selection mechanisms work in the same way as when the interface is configure in POS-UTOPIA mode.

The external mapper should be able to write data fast and frequently enough to maintain a minimum level in the FIFO. If the FIFO is empty when data is needed for the SPE, an interrupt (XmtFifoUFI in register T_UTOINT) is asserted.

10.0 Microcontroller Interface

This section contains a description of the asynchronous microprocessor interface. The microprocessor interface is a generic asynchronous interface, including an address bus (A[10:0]), data bus (DATA[15:0]), and handshaking pins (WRB/RWB, RDB/E, CSB, and ALE). The MCUTYPE input pin indicates the type of microprocessor interface to be used—Intel or Motorola*. There is also an INT output pin that indicates status changes to the microprocessor.

10.1 Intel Interface

An Intel interface is selected by driving the MCUTYPE input pin low. It uses the WRB/RWB input pin as WRB and the RDB/E input pin as RDB.

A read cycle is indicated to the Intel IXF6048 by the microprocessor forcing a low on the RDB pin with the WRB pin held high.

A write cycle is indicated to the Intel IXF6048 by the microprocessor forcing a low on the WRB pin with the RDB pin held high.

Both cycles require the CSB pin to be low and the microprocessor to drive the A[10:0] address pins. In a write cycle, the microprocessor also drives the DATA[15:0] data pins. In a read cycle, the Intel IXF6048 drives the DATA[15:0] data pins.

When a multiplexed data/address bus is used, the falling edge of the ALE input, latches the address provided on the muxed bus (the muxed bus is connected to both A[10:0] and DATA[15:0]). If the address and data are not multiplexed, the ALE pin should be tied high.

10.2 Motorola* Interface

A Motorola* interface is selected by driving the MCUTYPE input pin high. It uses the WRB/RWB input pin as RWB and the RDB/E input pin as E.

A read cycle is indicated to the Intel IXF6048 by the microprocessor forcing a high on the RWB pin. A write cycle is indicated to the Intel IXF6048 by the microprocessor forcing a low on the RWR pin.

A low on the E input initiates both cycles. The E input is connected to the E output from the Motorola* microprocessor and is typically a 50% duty cycle waveform with a frequency derived from the microprocessor clock.

Both cycles require the CSB pin to be low and the microprocessor to drive the A[10:0] address pins. In a write cycle, the microprocessor also drives the DATA[15:0] data pins. In a read cycle, the Intel IXF6048 drives the DATA[15:0] data pins.

When a multiplexed data/address bus is used, the falling edge of the ALE input, latches the address provided on the muxed bus (the muxed bus is connected to both A[10:0] and DATA[15:0]). If the address and data are not multiplexed, the ALE pin should be tied high.

10.3 Interrupt Handling

10.3.1 Interrupt Sources

There are three types of interrupt sources:

1. Status change of a monitoring process: For example, the Intel IXF6048 monitors the incoming SONET/SDH frames for the correct framing word and updates the LosSt, LofSt, and OofSt status bits (register (1cc)D8H) indicating the presence or absence of Loss Of Signal, Loss Of Frame, and Out Of Frame conditions. When the value of these status bits change, an interrupt (LOS, LOF, and OOF in register (1cc)D0H) is generated, if enabled.
2. Event Occurrence: For example, the receive ATM FIFO overflow is considered an event and generates interrupts, if enabled.
3. Counter overflows: For example, the Intel IXF6048 monitors the SONET/SDH frame for BIP errors. These errors are recorded in a counter whose overflow causes an interrupt, if enabled.

10.3.2 Interrupt Enables

In order for an interrupt source to affect the state of the INT output pin, its associated interrupt enable bit must be set. The setting (whether it is '0' or '1') of the interrupt enables does not affect the updating of the status registers or counters.

Assuming the interrupt enable for a particular interrupt source is set and the interrupt source is active, its interrupt bit is set. The primary difference between each interrupt type is the way its respective interrupt bit is cleared.

10.3.3 Interrupt Clearing

In the discussion below, it is assumed that the example interrupt sources have their interrupt enable bits set.

Status change interrupt sources have their interrupt bits cleared when their status is read. For example, say the OofSt bit changes from '0' to '1' (in frame to out of frame). Its interrupt bit is set by this event. When the microprocessor reads the register containing the OofSt bit, its interrupt bit is cleared. If the OofSt bit subsequently changes from '1' to '0' (out of frame to in frame) again, its interrupt bit is set again by this event and then cleared when the status is read.

The interrupt register can be read again only after three internal clock cycles have been completed since it was last cleared by reading its associated status registers.

It should be noted that updates to status bits are not affected by the interrupt bit state. For example, the OofSt bit could change from '1' to '0' (generating an interrupt) and then before the microprocessor reads OofSt, it could change back to '1'. This would have no affect on its interrupt bit since it would already be set. When the microprocessor reads the OofSt bit, it would read '1'.

Both event interrupts and counter overflow interrupts are cleared when their interrupt registers are read, as event interrupts and counters do not have any associated status registers.

10.4 Counter Reading

Counters are read by first buffering their contents and then reading the buffer. They can be individually buffered or group buffered. They are group buffered by writing to register BfrAllCntrs (register MACNF). They are individually buffered by writing to the most significant byte of a particular buffer.

After buffering the counter, the contents of the buffer are read at the address specified in the register definition.

A counter can be read only after three internal clock cycles have completed since it has been buffered (previous write operation.

11.0 Microprocessor Register Description

11.1 Register Address Map

The following notations and definitions are used in the register descriptions.

R	Read Only. Unless otherwise stated in the register description, writes have no affect. Note that for some counter registers, a write to the MSByte resets the counter.
W	Write Only. Reading returns undefined values.
R/W	Read/Write. A register (or bit) with this attribute can be read from and written to.
Unused Bits	Some of the registers contain unused bits. When reading a register, the value of the unused bits is logic zero. The software **should** program the unused bit positions to logic zero to avoid incompatibilities with future versions of the device.
Reserved Bits	Some of the registers contain reserved bits. Software must deal correctly with reserved fields. For reads, software must use appropriate masks to extract the defined bits and not rely on reserved bits to be any particular value.The software **must** program the reserved bit positions to their default value.
Default	When the Intel IXF6048 is reset, it sets its registers to predetermined default states. The default state represents the minimum functionality feature set required to successfully bring up the system. Hence, it does not represent the optimal system configuration. It is the responsibility of software to properly determine the operating parameters, optional system features that are applicable, and to program the Intel IXF6048 registers accordingly.
Default = X	Undefined
AIS	Alarm Signal Indication
HPOH	High Order Path OverHead
MSOH	Multiplexer Section OverHead
OHT	OverHead Terminator
RSOH	Regenerator Section OverHead
RST	Regenerator Section Termination
cc	Channel number (00, 01, 10, 11)—this represents the four bits that make up this hexadecimal value in an address. This is used to select between registers that are for channels 0 (0X00b), 1 (0X01b), 2 (0X10b) and 3 (0X11b). X can be a 1 or 0 depending upon the register. The MSB is always 0.

Table 26. Register Address Map (Sheet 1 of 6)

Address	Mnemonic	Register Name	Type	Page #
Global Registers				
(000)01H	MACNF	Microprocessor Access Configuration Register	R/W	221
(000)02H	CHIP_ID	Chip ID and Version Numbers Register	R	221
(000)03H	SRESET	Software Reset Register	R/W	222
(000)04H	BUF_ACNTS	Buffer All Counters Global Register	W	223
(000)05H	SDH_GIS	SDH Global Interrupt Source Register	R	223

Table 26. Register Address Map (Sheet 2 of 6)

Address	Mnemonic	Register Name	Type	Page #
(000)06H	ATMPOS_GIS	ATM and POS Global Interrupt Source Register	R	224
(000)07H	S_AIS	SDH/SONET Receive AIS Register	R	224
(000)08H	GOCNF	Global Operational Configuration Register	R/W	225
(0cc)09H	COCNF	Channel Operational Configuration Register	R/W	227
(0cc)0AH	R_COCNF	Receive Channel Operational Configuration Register	R/W	229
(0cc)0BH	T_COCNF	Transmit Channel Operational Configuration Register	R/W	231
(000)0CH	OHPCNF	Overhead Ports Configuration Register	R/W	233
(000)0DH	R_FPCNF	Receive Frame Pulse Configuration Register	R/W	234
(000)0EH	T_FPCNF	Transmit Frame Pulse Configuration Register	R/W	235
(000)0FH	OCPCNF	Output Clock Polarity Configuration	R/W	236
(000)10H	ICPCNF1	Input Clock Polarity Configuration 1	R/W	237
(000)11H	ICPCNF2	Input Clock Polarity Configuration 2	R/W	238
(000)12H	ICMR1	Input Clock Monitoring Register 1	R	239
(000)13H	ICMR2	Input Clock Monitoring Register 2	R	240
(000)14H	NCMODECNF	Non-concatenated mode Configuration Register	R/W	241
(000)1AH	PRBSINT	PRBS Analyzer Interrupt Register	R	241
(000)1BH	PRBSINTEN	PRBS Analyzer Interrupt Enable Register	R/W	241
(000)1CH	TALBINT	Transmit Alarm Bus Interrupt Register	R	242
(000)1DH	TALBINTEN	Transmit Alarm Bus Interrupt Enable Register	R/W	242
(000)1EH	LSPCNF	Line Side Parity Configuration Register	R/W	242
(000)1FH	LSPINT	Line Side Parity Interrupt Register	R	243
(000)20H	LSPINTEN	Line Side Parity Interrupt Enable Register	R/W	243
(000)21H	MISC_GIS	Miscellaneous Global Interrupt Source Register	R/W	244
UTOPIA Interface Registers				
(000)70H	R_UICNF	Receive UTOPIA Interface Configuration	R/W	245
(000)71H	R_UIIML	Receive UTOPIA Interface Initiation Minimum Level	R/W	248
(0cc)60H	R_UICHCNF	Receive UTOPIA Interface Channel Configuration	R/W	249
(0cc)61H	R_PWM	Receive Programmable Watermark	R/W	251
(000)50H	T_UICNF	Transmit UTOPIA Interface Configuration	R/W	251
(000)51H	T_UIIML	Transmit UTOPIA Interface Initiation Minimum Level	R/W	253
(0cc)40H	T_UICHCNF	Transmit UTOPIA Interface Channel Configuration	R/W	254
(0cc)41H	T_UIFDP	Transmit UTOPIA Interface FIFO Depth	R/W	255
(0cc)42H	T_NFPWM	Transmit Near Full Programmable Watermark	R/W	256
(0cc)43H	T_NEPWM	Transmit Near Empty Programmable Watermark	R/W	256
(000)72H	R_UTOINT	Receive UTOPIA Interface Interrupt Register	R	257
(000)52H	T_UTOINT	Transmit UTOPIA Interface Interrupt Register	R	257
(000)73H	R_UTOINTEN	Receive UTOPIA Interface Interrupt Enable Register	R/W	258

Table 26. Register Address Map (Sheet 3 of 6)

Address	Mnemonic	Register Name	Type	Page #
(000)53H	T_UTOINTEN	Transmit UTOPIA Interface Interrupt Enable Register	R/W	258
SDH/SONET Receive Regenerator Section Termination Registers				
(1cc)80H	R_RSTC	Receive RST Configuration	R/W	258
(1cc)81H	LOF_LMN	Out Of Frame and Loss of Frame L, M, and N Configuration	R/W	261
(1cc)82H	OOF_ECNT	Out Of Frame Event Counter	R	261
(1cc)83H	B1_ERRCNT	B1 Error Counter	R	261
(1cc)85H	R_J0_ESTRA	J0 Receive Expected String Data Access	R/W	261
(1cc)86H	R_J0_ASTRA	J0 Received Accepted String Data Access	R/W	263
(1cc)87H	J0_RSTC	J0 Received Trace Configuration	R/W	265
(1cc)D0H	IS_RG	Receive Regenerator Section Interrupt Register	R	265
(1cc)D4H	IE_RG	Receive Regenerator Section Interrupt Enable	R/W	266
(1cc)D8H	S_RG	Receive Regenerator Section Status	R	266
SDH/SONET Receive Multiplexer Section Termination Registers				
(1cc)90H	R_MST_C	Receive MST Configuration	R/W	267
(1cc)96H-(1cc)95H	B2_BLKCNT	B2 Block Error Counter	R	269
(1cc)98H-(1cc)97H	B2_BIPCNT	B2 BIP Error Counter	R	269
(1cc)9AH-(1cc)99H	MR_BLKCNT	MST REI Block Error Counter	R	269
(1cc)9CH-(1cc)9BH	MR_BIPCNT	MST REI BIP Error Counter	R	270
(1cc)9DH	R_K2K1	Received K2 and K1 bytes/APS channel	R	271
(1cc)9FH	R_S1	Received S1 byte	R	271
(1cc)B0H	WINSZ_SB2	Window Size for Setting ExcB2ErrSt	R/W	271
(1cc)B1H	CWIN_SB2	Consecutive Windows for Setting ExcB2ErrSt	R/W	271
(1cc)B2H	E#_EXCWIN_SB2	Number of Errs/Win for Excessively Errored window	R/W	272
(1cc)B3H	WINSZ_CB2	Window Size for Clearing ExcB2ErrSt	R/W	272
(1cc)B4H	CWIN_CB2	Consecutive Windows for Clearing ExcB2ErrSt	R/W	272
(1cc)B5H	E#_NEXCWIN_CB2	Number of Errs/Win for Non-Excessively Errored Window	R/W	272
(1cc)B7H-(1cc)B6H	WINSZ_SDEGB2	Window Size for Setting DegB2ErrSt	R/W	273
(1cc)B8H	CWIN_SDEGB2	Consecutive Windows for Setting DegB2ErrSt	R/W	273
(1cc)B9H	E#_DEGWIN	Number of Errs/Win for Error Degraded window	R/W	273
(1cc)BBH-(1cc)BAH	WINSZ_CDEGB2	Window Size for Clearing DegB2ErrSt	R/W	273
(1cc)BCH	CWIN_CDEGB2	Consecutive Windows for Clearing DegB2ErrSt	R/W	274
(1cc)BDH	E#_NDEGWIN_CB2	Number of Errs/Win for Non-Degraded Error Rate Window	R/W	274
(1cc)D1H	IS_MUX	Receive Multiplexer Section Interrupt Register	R	274
(1cc)D5H	IE_MUX	Receive Multiplexer Section Interrupt Enable	R/W	275
(1cc)D9H	S_MUX	Receive Multiplexer Section Status	R	276
SDH/SONET Receive Multiplexer Section Adaptation Registers				
(1cc)A0H	R_MSA_C	Receive MSA Configuration	R/W	277

Table 26. Register Address Map (Sheet 4 of 6)

Address	Mnemonic	Register Name	Type	Page #
(1cc)A1H	R_AU_NCNT	Receive Negative AU Pointer Justification Event Counter	R	278
(1cc)A2H	R_AU_PCNT	Receive Positive AU Pointer Justification Event Counter	R	279
(1cc)D2H	IS_ADP	Receive Section Adaptation Interrupt Register	R	279
(1cc)D6H	IE_ADP	Receive Section Adaptation Interrupt Enable	R/W	279
(1cc)DAH	S_ADP	Receive Section Adaptation Status	R	280
SDH/SONET Receive High Order Path Termination Registers				
(1cc)A4H	R_HPT_C1	Receive HPT Configuration 1 Register	R/W	281
(1cc)A5H	R_HPT_C2	Receive HPT Configuration 2 Register	R/W	282
(1cc)A6H	EXP_C2	Expected C2 byte Register	R/W	283
(1cc)A7H	R_C2	Received C2 byte Register	R	284
(1cc)A8H	R_HPT_RDI	Received HPT RDI Bits Register	R	284
(1cc)A9H	B3_ECNT	B3 Error Event Counter	R	284
(1cc)AAH	HPTREI_CNT	HPT REI Counter	R	284
(1cc)ADH	R_J1_ASTRA	J1 Received Accepted String Data Access	R/W	285
(1cc)AFH	R_J1_ESTRA	J1 Receive Expected String Data Access	R/W	286
(1cc)D3H	IS_HPT	Receive Path (HPT) Interrupt Register	R	287
(1cc)D7H	IE_HPT	Receive Path (HPT) Interrupt Enable	R/W	287
(1cc)DBH	S_HPT	Receive Path (HPT) Status	R	288
SDH/SONET Transmit Regenerator and Multiplexer Section Termination Registers				
(1cc)E0H	T_RMST_OP	Transmit RMST Operational Register	R/W	289
(1cc)E1H	T_SC_RSOH	Transmit Source Configuration for RSOH bytes Register	R/W	291
(1cc)E2H	T_SC_MSOH	Transmit Source Configuration for MSOH bytes Register	R/W	293
(1cc)E4H	T_J0_STRA	J0 Transmit String Data Access Register	R/W	295
(1cc)E5H	MP_TK2K1	Microprocessor Provided Transmit K1 and K2 Bytes Register	R/W	295
(1cc)E6H	MP_TS1	Microprocessor Provided Transmit S1 Byte Register	R/W	296
SDH/SONET Transmit Multiplexer Section Adaptation Registers				
(1cc)E9H	T_AU_PTS	Transmit AU Pointer Operational Configuration	R/W	296
(1cc)EAH	T_CAU_PT	Transmit Current AU Pointer Value	R	297
SDH/SONET Transmit High Order Path Termination Registers				
(1cc)E8H	T_HPT_C	Transmit HPT Configuration	R/W	297
(1cc)EBH	MP_TC2	Microprocessor Provided Transmit C2 Byte	R/W	301
(1cc)ECH	MP_THPTRDI	Microprocessor Provided Transmit HPT RDI bits	R/W	301
(1cc)EEH	T_J1_STRA	J1 Transmit String Data Access Register	R/W	302
(1cc)EFH	T_HPT_OPC	Transmit HPT Operational Configuration	R/W	300
ATM Receive Channel Registers				
(1cc)20H	R_ACPCNF	Receive ATM Cell Processor Configuration	R/W	303

Table 26. Register Address Map (Sheet 5 of 6)

Address	Mnemonic	Register Name	Type	Page #
(1cc)21H	R_IUCFLTR	Receive Idle/Unassigned Cell Filter	R/W	305
(1cc)23H-(1cc)22H	R_LCDFLTR	Receive LCD Filter	R/W	306
(1cc)25H-(1cc)24H	R_ACELLCNT	Receive ATM Cell Counter	R	306
(1cc)27H-(1cc)26H	R_ICELLCNT	Receive Idle Cell Counter	R	307
(1cc)28H	R_CHECNT	Receive Correctable HEC Error Counter	R	307
(1cc)29H	R_UHECNT	Receive Uncorrectable HEC Error Counter	R	307
(1cc)2AH	R_CFOCNT	Receive Cell FIFO Overflow Counter	R	307
(1cc)2BH	R_ATMINT	Receive ATM Interrupt (and Status) Register	R	308
(1cc)2CH	R_ATMINTEN	Receive ATM Interrupt Enable	R/W	309
ATM Transmit Channel Registers				
(1cc)10H	T_ACPCNF	Transmit ATM Cell Processor Configuration	R/W	309
(1cc)11H	T_ICELLP	Transmit Idle Cell Pattern	R/W	311
(1cc)13H-(1cc)12H	T_ACELLCNT	Transmit ATM Cell Counter	R	311
(1cc)15H-(1cc)14H	T_ICELLCNT	Transmit Idle Cell Counter	R	312
(1cc)16H	T_ATMINT	Transmit ATM Interrupt Register	R	312
(1cc)17H	T_ATMINTEN	Transmit ATM Interrupt Enable	R/W	312
POS Receive Channel Registers				
(1cc)60H	R_PHCCNF	Receive POS HDLC Controller Configuration	R/W	313
(1cc)61H	R_MINPL	Receive Minimum Packet Length	R/W	314
(1cc)62H	R_MAXPL	Receive Maximum Packet Length	R/W	315
(1cc)64H-(1cc)63H	R_FRMCNT	Receive Frame Counter	R	315
(1cc)66H-(1cc)65H	R_BYTECNT	Receive Byte Counter	R	315
(1cc)68H-(1cc)67H	R_AFCNT	Receive Aborted Frame Counter	R	316
(1cc)6AH-(1cc)69H	R_FCSECNT	Receive FCS Error Counter	R	316
(1cc)6BH	R_PFOCNT	Receive Packet FIFO Overflow Counter	R	316
(1cc)6DH-(1cc)6CH	R_MINPLECNT	Receive Minimum Packet Length Error Counter	R	317
(1cc)6EH	R_MAXPLECNT	Receive Maximum Packet Length Error Counter	R	317
(1cc)6FH	R_POSINT	Receive POS Interrupt Register	R	317
(1cc)70H	R_POSINTEN	Receive POS Interrupt Enable	R/W	319
POS Transmit Channel Registers				
(1cc)40H	T_PHCCNF	Transmit POS HDLC Controller Configuration	R/W	319
(1cc)41H	T_IPGCTRL	Transmit Interpacket Gap Control (Tx Flow Control)	R/W	321
(1cc)43H-(1cc)42H	T_FRMCNT	Transmit Frame Counter	R	323
(1cc)45H-(1cc)44H	T_BYTECNT	Transmit Byte Counter	R	323
(1cc)47H-(1cc)46H	T_AFCNT	Transmit Aborted Frame Counter	R	324

Table 26. Register Address Map (Sheet 6 of 6)

Address	Mnemonic	Register Name	Type	Page #
(1cc)48H	T_PFUCNT	Transmit Packet FIFO Underflow Counter	R	324
(1cc)49H	T_POSINT	Transmit POS Interrupt Register	R	324
(1cc)4AH	T_POSINTEN	Transmit POS Interrupt Enable	R/W	325

11.2 Global Registers

11.2.1 MACNF—Microprocessor Access Configuration Register ((000)01H)

Bit	Name	Description	Type	Default
15:3	Unused			0
2	BytChgUpdDsbl	This bit controls received byte register updates when a register's byte change interrupt is active. This bit is generally used for diagnostics. For example, if the received K2 byte were rapidly toggling, the values that it is toggling between could be captured by setting this bit: '0' = Enable received byte register updates when byte change interrupt is active. '1' = Disable received byte register updates when byte change interrupt is active.	R/W	'0'
1	CntrTest	This bit **should always be set to '0'** during normal operation. It allows faster testing of the overflow interrupt functionality during simulation: '0' = Normal operation '1' = Set overflow count: B1 counter = 7 B2 bit counter = 31 B2 block counter = 3 M1 REI bit counter = 31 M1 REI block counter = 3 B3 bit/block counters = 7 G1 REI bit/block counters = 7	R/W	'0'
0	MasIntEn	This bit controls the chip interrupt pin: '0' = Disable interrupt pin. '1' = Activate interrupt pin when there are unmasked active interrupts.	R/W	'0'

11.2.2 CHIP_ID—Chip ID and Version Numbers Register ((000)02H)

This register can only be read. It is used to identify the version of the chip.

Bit	Name	Description	Type	Default
15:8	ChipVer[7:0]	**Chip Version:** This field contains the Intel IXF6048 version number.	R	02H
7:0	ChipID[7:0]	**Chip Identification:** This field contains the Intel IXF6048 Identification number.	R	01H

11.2.3 SRESET—Software Reset Register ((000)03H)

The SRESET register allows the software to asynchronously reset the entire Intel IXF6048 device or only a part of it. When a bit is set to logic one, the section of the device controlled by this bit is held in reset. None of these bits are self-clearing; a logic zero must be written to bring Intel IXF6048 out of reset.

Bit	Name	Description	Type	Default
15:9	Unused			0
8	Reset	Resets the entire Intel IXF6048 device (equivalent to the RESET input pin).	R/W	'0'
7:4	ResetXmtCh[3:0]	Transmit section reset: When Intel IXF6048 is configured as a single processor (single line side interface), ResetXmtCh[0] resets the entire transmit section of Intel IXF6048 including: • Transmit SDH processing • Transmit ATM/POS processing • UTOPIA interface ResetXmtCh[3:1] are unused bits. ResetXmtCh[0] does not reset the Global or the UTOPIA configuration registers. When Intel IXF6048 is configured as a quad processor (quad line side interface), ResetXmtCh[i] (i = 0, 1, 2, 3) resets the transmit section of channel #i including: • Transmit SDH processor • Transmit ATM/POS processors • Transmit UTOPIA interface ResetXmtCh[i] (i = 0, 1, 2, 3) does not reset the Global or the UTOPIA configuration registers.	R/W	0000
3:0	ResetRcvCh[3:0]	Receive section reset: When Intel IXF6048 is configured as a single processor (single line side interface), ResetRcvCh[0] resets the entire receive section of Intel IXF6048 including: • Receive SDH processing • Receive ATM/POS processing • UTOPIA interface ResetRcvCh[3:1] are unused bits. ResetRcvCh[0] does not reset the Global or the UTOPIA configuration registers. When Intel IXF6048 is configured as a quad processor (quad line side interface), ResetRcvCh[i] (i = 0, 1, 2, 3) resets the receive section of channel #i including: • Receive SDH processor • Receive ATM/POS processors • Receive UTOPIA interface ResetRcvCh[i] (i = 0, 1, 2, 3) does not reset the Global or the UTOPIA configuration registers.	R/W	0000

11.2.4 BUF_ACNTS—Buffer All Counters Global Register ((000)04H)

Writing a logic one in any of these bits causes all of the counters in the corresponding processor to be loaded into buffers and then cleared. The contents of an individual counter buffer can then be read at the addresses specified for the counters in this document. Counters can be individually buffered by writing to the specified MSByte of the desired counter. Writing a logic zero has no effect on the corresponding processor.

Bit	Name	Description	Type	Default
15:12	Unused			
11:8	BfrRcvSdh[3:0]	BfrRcvSdh[i] (i = 0, 1, 2, 3) loads into buffers and clears all the counters of the receive SDH processor on channel #i.	W	'XXXX'
7:4	BfrXmtAtmPos[3:0]	BfrXmtAtmPos[i] (i = 0, 1, 2, 3) loads into buffers and clears all the counters of the transmit ATM/POS processors on channel #i.	W	'XXXX'
3:0	BfrRcvAtmPos[3:0]	BfrRcvAtmPos[i] (i = 0, 1, 2, 3) loads into buffers and clears all the counters of the receive ATM/POS processors on channel #i.	W	'XXXX'

11.2.5 SDH_GIS—SDH Global Interrupt Source Register ((000)05H)

This register indicates that an SDH interrupt source register on channel #i (i = 0, 1, 2, 3) contains an active interrupt. Each bit in this register is active-high and represents the logic OR of all the interrupt bits in the associated channel interrupt source register. Each bit in this register clears upon reading the associated channel interrupt source register.

Bit	Name	Description	Type	Default
15:12	RcvHptInt[3:0]	RcvHptInt[i] (i = 0, 1, 2, 3) indicates that one or more interrupt bits are active in the IS_HPT register on channel #i.	R	'XXXX'
11:8	RcvAdpInt[3:0]	RcvAdpInt[i] (i = 0, 1, 2, 3) indicates that one or more interrupt bits are active in the IS_ADP register on channel #i.	R	'XXXX'
7:4	RcvMuxInt[3:0]	RcvMuxInt[i] (i = 0, 1, 2, 3) indicates that one or more interrupt bits are active in the IS_MUX register on channel #i.	R	'XXXX'
3:0	RcvRegInt[3:0]	RcvRegInt[i] (i = 0, 1, 2, 3) indicates that one or more interrupt bits are active in the IS_RG register on channel #i.	R	'XXXX'

11.2.6 ATMPOS_GIS—ATM and POS Global Interrupt Source Register ((000)06H)

This register indicates that an ATM or POS interrupt source register on channel #i (i = 0, 1, 2, 3) contains an active interrupt. Each bit in this register is active-high and represents the logic OR of all the interrupt bits in the associated channel interrupt source register. Each bit in this register clears upon reading the associated channel interrupt source register.

Bit	Name	Description	Type	Default
15:12	XmtATMInt[3:0]	XmtATMInt[i] (i = 0, 1, 2, 3) indicates that one or more interrupt bits are active in the T_ATMINT register on channel #i.	R	'XXXX'
11:8	RcvATMInt[3:0]	RcvATMInt[i] (i = 0, 1, 2, 3) indicates that one or more interrupt bits are active in the R_ATMINT register on channel #i.	R	'XXXX'
7:4	XmtPOSInt[3:0]	XmtPOSInt[i] (i = 0, 1, 2, 3) indicates that one or more interrupt bits are active in the T_POSINT register on channel #i.	R	'XXXX'
3:0	RcvPOSInt[3:0]	RcvPOSInt[i] (i = 0, 1, 2, 3) indicates that one or more interrupt bits are active in the R_POSINT register on channel #i.	R	'XXXX'

11.2.7 S_AIS—SDH/SONET Receive AIS Register ((000)07H)

This register is used primarily for testing purposes. It indicates the status of internal chip logic for AIS generation processes.

Bit	Name	Description	Type	Default
15:12	GenRstAisSt[3:0]	GenRstAisSt[i] (i = 0, 1, 2, 3) contains the present status of receive side RST AIS generator on channel #i: '0' = No AIS '1' = AIS ≡ see register ((1cc)80H), where cc = i = 0, 1, 2, 3.	R	'XXXX'
11:8	GenMstAisSt[3:0]	GenMstAisSt[i] (i = 0, 1, 2, 3) contains the present status of the receive side MST AIS generator on channel #i: '0' = No AIS '1' = AIS ≡ (RcvMstAisEn **AND** MspSFSt) **OR** RcvMstAisFrc	R	'XXXX'
7:4	GenMsaAisSt[3:0]	GenMsaAisSt[i] (i = 0, 1, 2, 3) contains the present status of the receive side MSA AIS generator on channel #i: '0' = No AIS '1' = AIS ≡ (RcvMsaAisEn **AND** (AuAisSt **OR** LopSt)) **OR** RcvMsaAisFrc.	R	'XXXX'
3:0	GenHptAisSt[3:0]	GenHptAisSt[i] (i = 0, 1, 2, 3) contains the present status of the receive side HPT AIS generator on channel #i: '0' = No AIS '1' = AIS ≡ (HptSlmSt **AND** RcvHptAisSlmEn) **OR** (HptUneqSt **AND** RcvHptAisUneqEn) **OR** (RcvHptAisTimEn **AND** J1MsMtchSt)) **OR** RcvHptAisFrc.	R	'XXXX'

11.2.8 GOCNF—Global Operational Configuration Register ((000)08H)

This register configures Intel IXF6048 global configuration features.

Bit	Name	Description	Type	Default
15:14	Unused			
13	GenIOVal	GenIOVal status/configuration bit allows the control of GENIO generic input/output ball. If GenIOMode = ‘0’ (GENIO is configured as an input), then GenIOVal is a “read only” bit. GenIOVal indicates the present status of GENIO input ball: '0' = GENIO input is low. '1' = GENIO input is high. If GenIOMode = ‘1’ (GENIO is configured as an output), then GenIOVal is a “read/write” configuration bit. It forces the value of GENIO output signal: '0' = GENIO output is set to low. '1' = GENIO output is set to high.	R/W	‘0’
12	GenIOMode	GenIOMode configures GENIO generic input/output ball (K31) as an input or as an output. '0' = GENIO is an input. The value of GENIO input can be read via GenIOVal status bit. '1' = GENIO is an output. The value of GENIO output can be set via GenIOVal configuration bit.	R/W	‘0’
11	RcvUOutEnCnf	When RcvUOutEnCnf = ‘0’, the receive UTOPIA interface outputs are tristated when the pin UOEN = ‘0’ or UOutEn = ‘0’ (bit 4 in this register) When RcvUOutEnCnf = ‘1’, the receive UTOPIA interface outputs are not disabled independently of the values of UOEN and UOutEn.	R/W	‘0’
10	XmtUOutEnCnf	When XmtUOutEnCnf = ‘0’, the transmit UTOPIA interface outputs are tristated when the pin UOEN = ‘0’ or UOutEn = ‘0’ (bit 4 in this register) When XmtUOutEnCnf = ‘1’, the transmit UTOPIA interface outputs are not disabled independently of the values of UOEN and UOutEn.	R/W	‘0’
9:8	Unused			
7	U64Mode	U64Mode is only used when the UTOPIA interface is configured in 64-bit mode: RcvUWidth = '11' (register R_UICNF) or XmtUWidth = '11' (register T_UICNF). U64Mode indicates what pins are used to expand the UTOPIA interface data buses (RXDATA and TXDATA) to 64-bits: '0' = The 32 additional lines (RXDATA[63:32] and TXDATA[63:32]) are located in the TTL line side interface: RPDI[31:0] and TPDO[31:0]. In this configuration, Intel IXF6048 can only use the PECL line side interface. '1' = The 32 additional lines (RXDATA[63:32] and TXDATA[63:32]) are located in the extraction and insertion overhead ports. In this configuration, Intel IXF6048 uses a simplified overhead insertion/ extraction interface i.e., insertion/extraction of SOH bytes only.	R/W	'0'

Bit	Name	Description	Type	Default
6	QMode	QMode configures Intel IXF6048 as a Single or Quad transceiver. QMode configures the Line Side Interface I/O as a Single Line Side Interface or as four independent Serial Line Side Interfaces: '0' = Single transceiver mode. Single OC-48c/48nc/12c/12nc/3c/3nc/1. '1' = Quad transceiver mode. Quad (in other words, more than one) OC-12c/3c/1. CMode must be set to '1'.	R/W	'0'
5	CMode	CMode configures Intel IXF6048 as a concatenated or non-concatenated processor. CMode is used only when the Intel IXF6048 is configured as a Single transceiver (QMode = '0'): '0' = Intel IXF6048 is configured as a non-concatenated processor (Single STS-48/STM-16, STS-12/STM-4, or STS-3). '1' = Intel IXF6048 is configured as a concatenated processor (Single STS-48c/STM-16c).	R/W	'1'
4	UOutEn	UOEn enables the UTOPIA interface: '0' = All the UTOPIA interface outputs (RXDATA, etc.) are held in high impedance. '1' = All the UTOPIA interface outputs operate in normal mode. In order to avoid collisions that could damage the device when several PHY devices are connected into the same UTOPIA interface, **the software MUST configure the UTOPIA interface (physical address of the device, decode-response delay, ATM/POS, etc.) before setting UOEn to logic one**. UOutEn is internally ORed with the UOEN input.	R/W	'0'
3	OutEn	This bit controls all the output pins of Intel IXF6048 except the microprocessor interface: '0' = All the Intel IXF6048 outputs (except microprocessor interface) are held in high impedance. '1' = All the Intel IXF6048 outputs operate in normal mode. In order to avoid collisions that could damage the device when several PHY devices are connected into the same UTOPIA interface, **the software must configure the UTOPIA interface (physical address of the device, decode-response delay, ATM/POS mode, etc.) before setting IOBusEn to logic one**. OutEn is internally ORed with the OEN input.	R/W	'0'
2:0	UAddrBase[2:0]	UAddrBase[2:0] are the device identification address and contains the address of the memory space that Intel IXF6048 occupies in the UTOPIA interface. UAddrBase[2:0] are compared with RXADDR[4:2] and TXADDR[4:2]. The least significant two bits of the address (RXADDR[1:0]) are hard-wired to select a specific channel ('00' = channel 0, '01' = channel 1, '10' = channel 2, '11' = channel 3). The address value 1FH is the null physical address and can not be assigned to any PHY port.	R/W	'000'

11.2.9 COCNF—Channel Operational Configuration Register ((0cc)09H)

This register configures global operational features, common to the receive and transmit directions, for each channel.

Bit	Name	Description	Type	Default
15:6	Unused			
5	RepeaterMode	RepeaterMode configures the channel in Repeater mode: '0' = The channel is configured in normal mode. '1' = The channel is configured in repeater mode. CMode (GOCNF register bit[5]) must be set to '1'.	R/W	'0'
4	SysLoopBack	SysLoopBack disables the system diagnostic loopback mode from the transmitter to the receiver. The transmit data and clock generated by the transmit Regenerator Section block (just after SONET/SDH frame scrambling) are looped back to the receive Regenerator Section block (just before SONET/SDH frame descrambling): '0' = System diagnostic loopback is disabled. The receiver operates normally '1' = System diagnostic loopback is enabled. The receive Regenerator Section block input clock and input data are a flowed-through versions of the transmit Regenerator Section clock and data outputs. **NOTE:** When Intel IXF6048 is configured in Single transceiver mode (one serial or parallel interface), the System Diagnostic Loopback feature is enabled/disabled using channel #0 register.	R/W	'0'

Bit	Name	Description	Type	Default
3	LineLoopBack	LineLoopBack disables the line loopback mode: '0' = Line loopback is disabled. The transmitter operates normally. '1' = Line loopback is enabled. The transmit line side interface output clock and output data are flowed-through versions of the receive line side interface inputs. **NOTE:** The Line Loopback mode can be used ONLY if the RcvIFMode[2:0] (register R_COCNF) and XmtIFMode[2:0] (register T_COCNF) values match. **NOTE:** When Intel IXF6048 is configured in Single transceiver mode (a single line side interface), the Line Loopback feature is enabled/disabled using channel #0 register. **NOTE:** In the line side loopback mode, the TPCO/TSCO is always sourced from the associated RPCI/RSCI no matter what source/reference is selected in (T_COCNF—Transmit Channel Operational Configuration Register ((0cc)0BH) bit 9:8 <XmtTimRef[1:0]>) but the transmit divider (T_COCNF—Transmit Channel Operational Configuration Register ((0cc)0BH) bit 7:5 <XmtCOCnf[2:0]>) needs to be changed if the TPCI/TSCI clock is different than the RPCI/RSCI clock.	R/W	'0'
2	ChEna	ChEna controls the channel operation (both receive and transmit directions): '0' = Channel is disabled. The channel operation is stopped and the channel output pins are tristated. '1' = Channel is enabled. The channel operates normally.	R/W	'1'
1:0	ChRate[1:0]	ChRate[1:0] configures the channel in one of the following modes: '11' = 2.48832 Gb/s (OC-48) '10' = 622.08 Mb/s (OC-12) '01' = 155.52 Mb/s (OC-3) '00' = 51.84 Mb/s (OC-1) **NOTE:** When Intel IXF6048 is configured in Quad transceiver mode (four line side interfaces), configuration value '11' (OC-48 mode) is invalid. **NOTE:** When Intel IXF6048 is configured in Single transceiver mode (single line side interface), Intel IXF6048's rate is configured by using channel #0 register.	R/W	'11'

11.2.10 R_COCNF—Receive Channel Operational Configuration Register ((0cc)0AH)

This register configures global operational features for each channel.

Bit	Name	Description	Type	Default
15:10	Unused			
9	RcvTrDescrEn	RcvTrDescrEn controls descrambling of data in “transparent” mode (the SONET/SDH SPE) by using the self-synchronous scrambler 1 + X^{43}: '0' = The scrambler is disabled. '1' = The scrambler is enabled.	R/W	'0'
8	RcvLockCnf	RcvLockCnf configures how the input pins RLOCK_i (i = 0, 1, 2, 3) are used by Intel IXF6048 to switch the internal receive clock reference to the selected transmit line (Blue) clock signal reference (TPCI/TCCI/TSCI). RLOCK_i (i = 0, 1, 2, 3) is active to indicate that the external PLL is locked. '0' = RLOCK_i (i = 0, 1, 2, 3) input pin is active-high. Intel IXF6048 receive channel #i switches to blue clock when RLOCK_i = '0'. '1' = RLOCK_i (i = 0, 1, 2, 3) input pin is active-low. Intel IXF6048 receive channel #i switches to blue clock when RLOCK_i = '1'.	R/W	'0'

Bit	Name	Description	Type	Default
7:5	RcvCOCnf[2:0]	RcvCOCnf[2:0] configures the TTL receive output clocks (RPCO, RPCO_i, and RSCO_i) as divided or flowed-through versions of the received input clocks (RPCI_P/N, RPCI_Pi/Ni, RPCI, RPCI_i, and RSCI_i): **2:0 TTL Receive Output Clock** '000' Receive input clock ÷ 1 (flow-through) '001' Receive input clock ÷ 2 '010' Receive input clock ÷ 4 '011' Receive input clock ÷ 8 '100' Receive input clock ÷ 16 '101' Receive input clock ÷ 32 '110' 8-KHz clock '111' tristated See the pin description for details.	R/W	'111'
4:2	RcvIFMode[2:0]	RcvIFMode configures the type of line side interface used by the receive channel: '000' = 32-bit TTL '001' = Reserved '010' = 8-bit TTL '011' = 1-bit TTL '100' = 16-bit PECL '101' = Reserved '110' = Reserved '111' = 1-bit PECL **NOTE:** In order to use the line loop back mode (LineLoopBack = '1', register COCNF) or to clock the transmit channel by using the receive channel timing reference (XmtTimRef[1:0] = '01', register T_COCNF), the configuration values RcvIFMode[2:0] and XmtIFMode[2:0] (register T_COCNF) must match. **NOTE:** The 32-bit TTL and 16-bit PECL configurations can be used only when Intel IXF6048 is configured as a single transceiver. In this mode (single transceiver configuration), the configuration values for channels 1, 2 and 3 are ignored.	R/W	'100'
1:0	RcvChMode[1:0]	RcvChMode[1:0] configures the receive channel in one of the following operational modes: '00' = Test mode. The receive channel analyzes the incoming SPE bytes using an $X^{15} + X^{14} + 1$ linear feedback shift register. Error detection is indicated using register PRBSINT. In this configuration, no data is written into the UTOPIA receive FIFO. '01' = Transparent mode. The receive channel does not perform any processing of the SPE bytes. The full SPE is written into the UTOPIA receive FIFO (allowing the use of an external SPE analyzer). '10' = ATM Mode (UTOPIA) '11' = POS Mode (UTOPIA like)	R/W	'10'

11.2.11 T_COCNF—Transmit Channel Operational Configuration Register ((0cc)0BH)

This register configures global operational features for each channel.

Bit	Name	Description	Type	Default
15:12	Unused			
11	XmtTrScrEn	XmtTrScrEn controls the scrambling of the data in “transparent” mode (the SONET/SDH SPE) by using the self-synchronous scrambler 1 + X^{43}: '0' = The scrambler is disabled. '1' = The scrambler is enabled	R/W	0
10	XmtPClkOut	XmtPClkOut enables the transmit PECL output clock: '0' = The PECL transmit output clock is enabled. '1' = The PECL transmit output clock is held in high impedance. See the pin description for details.	R/W	'0'
9:8	XmtTimRef[1:0]	XmtTimRef[1:0] selects the clock source used by the transmitter: '00' = Transmitter stopped (transmit clock internally tied low). '01' = Transmitter is clocked by the corresponding receive serial clock input (RPCI/RSCI). '10' = Transmitter is clocked by its own (per channel) input clock (TPCI_i/TSCI_i). '11' = Transmitter is clocked by the transmit common clock input (TCCI). **NOTE:** The transmit channel input timing reference depends on the configuration of XmtTimRef[1:0], XmtIFMode[2:0], and RcvIFMode[2:0]. See Table 4 for details. **NOTE:** A transmit channel can be configured to use the receive channel timing reference ONLY if the XmtIFMode[2:0] and RcvIFMode[2:0] values match. **NOTE:** When Intel IXF6048 is configured in Single transceiver mode, the configurations values for channels 1, 2 and 3 are ignored.	R/W	'11'

Bit	Name	Description	Type	Default
7:5	XmtCOCnf[2:0]	XmtCOCnf[2:0] configures the TTL transmit output clocks (TPCO, TPCO_i, and TSCO_i) as divided or flowed-through versions of the transmit source clock. Note that the transmit source clock depends on the configuration of XmtTimRef[1;0]. **2:0 TTL Transmit Output Clock** '000' Transmit source clock" ÷ 1 (flow-through) '001' Transmit input clock ÷ 2 '010' Transmit input clock ÷ 4 '011' Transmit input clock ÷ 8 '100' Transmit input clock ÷ 16 '101' Transmit input clock ÷ 32 '110' 8-KHz clock '111' tristated See the pin description for details.	R/W	'111'
4:2	XmtIFMode[2:0]	XmtIFMode[2:0] configures the type of line side interface used by the transmit channel: '000' = 32-bit TTL '001' = Reserved '010' = 8-bit TTL '011' = 1-bit TTL '100' = 16-bit PECL '101' = Reserved '110' = Reserved '111' = 1-bit PECL **NOTE:** In order to use the line loop back mode (LineLoopBack = '1', register COCNF) or to clock the transmit channel by using the receive channel timing reference (XmtTimRef[1:0] = '01'), the configuration values XmtIFMode[2:0] and RcvIFMode[2:0] must match. **NOTE:** The 32-bit TTL and 16-bit PECL configurations can be used when Intel IXF6048 is configured as a single transceiver. In this mode (single transceiver configuration), the configuration values for channels 1, 2 and 3 are ignored.	R/W	'100'
1:0	XmtChMode[1:0]	XmtChMode[1:0] configures the transmit channel in one of the following operational modes: '00' = Test mode. The transmit channel maps a PRBS sequence (generated using the polynomial $X^{15} + X^{14} + 1$) into the outgoing SPE. Error detection is indicated using register PRBSINT. In this configuration, no data is read from the UTOPIA transmit FIFO. '01' = Transparent mode. The transmit channel does not process the bytes read from the UTOPIA transmit FIFO. The bytes read from the FIFO are directly copied into the outgoing SPE (allowing the use of an external SPE generator). '10' = ATM Mode (UTOPIA) '11' = POS Mode (UTOPIA like)	R/W	'10'

11.2.12 OHPCNF—Overhead Ports Configuration Register ((000)0CH)

This register configures Intel IXF6048 overhead ports' features.

Bit	Name	Description	Type	Default
15:2	Unused			
1	OWPlsCnf	OWPlsCnf configures the location of the byte pulse used in the orderwire buses: ROWBYC, TOWBYC, RPOWBYC, and TPOWBYC pins. In transmission: '0' = The most significant data bit is expected in the same clock cycle as the pulse. '1' = The least significant data bit is expected in the same clock cycle as the pulse. In reception: '0' = The most significant data bit is output in the same clock cycle as the pulse. '1' = The least significant data bit is output in the same clock cycle as the pulse.	R/W	'0'
0	OHPortMode	OHPortMode configures the Overhead, Alarms, data communications channels, and orderwire Insertion/Extraction ports. When Intel IXF6048 is configured as a Single transceiver (QMode = '0'), the OH ports are automatically configured as the OH Ports Logical Interface #1 (OH, Alarm, DCC and Orderwire Insertion/ Extraction Single PHY Mode). See the pin description for details. When Intel IXF6048 is configured as a Quad transceiver (QMode = '1'), OHPortMode configures the OH ports in the following modes (see the pin description for details): '0' = OH Ports Logical Interface #2 (OH and Alarm Insertion/ Extraction Ports Quad PHY Mode. '1' = OH Ports Logical Interface #3 (DCC and Orderwire Insertion/ Extraction Ports Quad PHY Mode.	R/W	'0'

11.2.13 R_FPCNF—Receive Frame Pulse Configuration Register ((000)0DH)

This register configures the frame position of the receive frame pulse input: RFPI_P/N, RFPI, or RFPI_i (i = 0, 1, 2, 3) inputs.

Bit	Name	Description	Type	Default
15:0	unused			
7:0	RcvFPICnf[7:0]	RcvFPICnf[7:0] configures the receive input frame pulse, relative to the frameword received on the receive data input bus. RcvFPICnf[7:0] are used to configure all the different parallel receive interfaces: **Frame Pulse Input — Data Input Bus** RFPI_P/N — RPDI_P/N[15:0] RFPI — RPDI[31:0] RFPI_0 — RPDI_0[7:0] RFPI_1 — RPDI_1[7:0] RFPI_2 — RPDI_2[7:0] RFPI_3 — RPDI_3[7:0] The receive frame pulse input pin is set to logic one to denote that the receive data input bus is now carrying the byte indicated by RcvFPICnf[7:0]. The value of RcvFPICnf[7:0] selects a byte position in the first row of the SONET/SDH frame. RcvFPICnf[7:0] = '0' locates the first A1 byte, RcvFPICnf[7:0] = '1' locates the second A1 byte, etc. The following is an example of the RcvFPICnf[7:0] coding for OC-48c/OC-48: '0' = First A1 byte '1' = Second A1 byte …… 47 = Last A1 byte 48 = First A2 byte …… 144 = First SPE byte ……	R/W	30H

11.2.14 T_FPCNF—Transmit Frame Pulse Configuration Register ((000)0EH)

This register configures the frame position of the transmit frame pulse output and the transmit frame pulse input: TFPO_P/N, TFPO, or TFPO_i (i = 0, 1, 2, 3) outputs and TFPI_P/N, TFPI, or TFPI_i (i = 0, 1, 2, 3) inputs.

Bit	Name	Description	Type	Default
15:8	XmtFPOCnf [7:0]	XmtFPOCnf[7:0] configures the transmit output frame pulse, relative to the frameword transmitted on the transmit data output bus. XmtFPOCnf[7:0] are used to configure all the different parallel transmit interfaces: **Frame Pulse Output** — **Data Output Bus** TFPO_P/N — TPDO_P/N[15:0] TFPO — TPDO[31:0] TFPO_0 — TPDO_0[7:0] TFPO_1 — TPDO_1[7:0] TFPO_2 — TPDO_2[7:0] TFPO_3 — TPDO_3[7:0] The transmit frame pulse output pin is set to logic one to denote that the transmit data output bus is carrying (in the same clock cycle) the byte indicated by XmtFPOCnf[7:0]. The value of XmtFPOCnf[7:0] selects a byte position in the first row of the SONET/SDH frame. XmtFPOCnf[7:0] = '0' selects the first A1 byte, XmtFPOCnf[7:0] = '1' selects the second A1 byte, etc. The following is an example of the XmtFPOCnf[7:0] coding for OC-48c/OC-48: '0' = First A1 byte '1' = Second A1 byte …… 47 = Last A1 byte 48 = First A2 byte …… 144 = First SPE byte ……	R/W	30H

Bit	Name	Description	Type	Default
7:0	XmtFPICnf[7:0]	XmtFPICnf[7:0] configures the transmit input frame pulse, relative to the frameword transmitted on the transmit data output bus. XmtFPICnf[7:0] are used to configure all the different parallel transmit interfaces: **Frame Pulse Input Data Output Bus** TFPI_P/N TPDO_P/N[15:0] or TPDO_P/N[7:0] TFPI TPDO[31:0] TFPI_0 TPDO_0[7:0] TFPI_1 TPDO_1[7:0] TFPI_2 TPDO_2[7:0] TFPI_3 TPDO_3[7:0] The transmit frame pulse input pin is set to logic one to denote that the transmit data output bus MUST carry (in the same clock cycle) the byte indicated by XmtFPICnf[7:0]. The value of XmtFPICnf[7:0] selects a byte position in the first row of the SONET/SDH frame. XmtFPICnf[7:0] = '0' selects the first A1 byte, XmtFPICnf[7:0] = '1' selects the second A1 byte, etc. The next example shows the XmtFPICnf[7:0] coding for OC-48c/ OC-48: '0' = First A1 byte '1' = Second A1 byte …… 47 = Last A1 byte 48 = First A2 byte …… 144 = First SPE byte ……	R/W	30H

11.2.15 OCPCNF—Output Clock Polarity Configuration ((000)0FH)

This register allows inversion of each individual Intel IXF6048 output clock.

When the polarity configuration bit of an output clock is set to logic one, Intel IXF6048 inverts the clock before driving the output pin.

Bit	Name	Description	Type	Default
15	Pol_TCO_T3	'0' = TSCO_3 and TPCO_3 clocks are not inverted. '1' = TSCO_3 and TPCO_3 clocks are inverted.	R/W	'0'
14	Pol_TCO_T2	'0' = TSCO_2 and TPCO_2 clocks are not inverted. '1' = TSCO_2 and TPCO_2 clocks are inverted.	R/W	'0'
13	Pol_TCO_T1	'0' = TSCO_1 and TPCO_1 clocks are not inverted. '1' = TSCO_1 and TPCO_1 clocks are inverted.	R/W	'0'
12	Pol_TCO_T0	'0' = TSCO_0, TPCO_0, and TPCO clocks are not inverted. '1' = TSCO_0, TPCO_0, and TPCO clocks are inverted.	R/W	'0'
11	Pol_RCO_T3	'0' = RSCO_3 and RPCO_3 clocks are not inverted. '1' = RSCO_3 and RPCO_3 clocks are inverted.	R/W	'0'
10	Pol_RCO_T2	'0' = RSCO_2 and RPCO_2 clocks are not inverted. '1' = RSCO_2 and RPCO_2 clocks are inverted.	R/W	'0'

Bit	Name	Description	Type	Default
9	Pol_RCO_T1	'0' = RSCO_1 and RPCO_1 clocks are not inverted. '1' = RSCO_1 and RPCO_1 clocks are inverted.	R/W	'0'
8	Pol_RCO_T0	'0' = RSCO_0, RPCO_0, and RPCO clocks are not inverted. '1' = RSCO_0, RPCO_0, and RPCO clocks are inverted.	R/W	'0'
7	Pol_TSCO_P3	'0' = TSCO_P3/N3 is not inverted. '1' = TSCO_P3/N3 clock is inverted.	R/W	'0'
6	Pol_TSCO_P2	'0' = TSCO_P2/N2 clock is not inverted. '1' = TSCO_P2/N2 clock is inverted.	R/W	'0'
5	Pol_TSCO_P1	'0' = TSCO_P1/N1 clock is not inverted. '1' = TSCO_P1/N1 clock is inverted.	R/W	'0'
4	Pol_TSCO_P0	'0' = TSCO_P0/N0 clock is not inverted. '1' = TSCO_P0/N0 clock is inverted.	R/W	'0'
3	Pol_ROWC	'0' = ROWC_i and RPOWC clocks are not inverted. '1' = ROWC_i and RPOWC clocks are inverted.	R/W	'0'
2	Pol_TOWC	'0' = TOWC_i and TPOWC clocks are not inverted. '1' = TOWC_i and TPOWC clocks are inverted.	R/W	'0'
1	Unused			
0	Pol_TPCO_P	'0' = TPCO_P0/N0 clock is not inverted. '1' = TPCO_P0/N0 clock is inverted.	R/W	'0'

11.2.16 ICPCNF1—Input Clock Polarity Configuration 1 ((000)10H)

This register allows inversion of each individual Intel IXF6048 input clock.

By default, Intel IXF6048 uses the rising edge of each input clock to sample data. When the polarity configuration bit of an input clock is set to logic one, Intel IXF6048 inverts the clock before using it, i.e., Intel IXF6048 uses the falling edge of the clock.

Bit	Name	Description	Type	Default
15	Pol_TCI_T3	'0' = TSCI_3 and TPCI_3 clock is not inverted. '1' = TSCI_3 and TPCI_3 clock is inverted.	R/W	'0'
14	Pol_TCI_T2	'0' = TSCI_2 and TPCI_2 clock is not inverted. '1' = TSCI_2 and TPCI_2 clock is inverted.	R/W	'0'
13	Pol_TCI_T1	'0' = TSCI_1 and TPCI_1 clock is not inverted. '1' = TSCI_1 and TPCI_1 clock is inverted.	R/W	'0'
12	Pol_TCI_T0	'0' = TSCI_0 and TPCI_0 and TPCI clock is not inverted. '1' = TSCI_0 and TPCI_0 and TPCI clock is inverted.	R/W	'0'
11	Pol_RCI_T3	'0' = RSCI_3 and RPCI_3 clock is not inverted. '1' = RSCI_3 and RPCI_3 clock is inverted.	R/W	'0'
10	Pol_RCI_T2	'0' = RSCI_2 and RPCI_2 clock is not inverted. '1' = RSCI_2 and RPCI_2 clock is inverted.	R/W	'0'
9	Pol_RCI_T1	'0' = RSCI_1 and RPCI_1 clock is not inverted. '1' = RSCI_1 and RPCI_1 clock is inverted.	R/W	'0'

Bit	Name	Description	Type	Default
8	Pol_RCI_T0	'0' = RSCI_0, RPCI_0 and RPCI clock is not inverted. '1' = RSCI_0, RPCI_0 and RPCI clock is inverted.	R/W	'0'
7	Pol_TSCI_P3	'0' = TSCI_P3/N3 is not inverted. '1' = TSCI_P3/N3 clock is inverted.	R/W	'0'
6	Pol_TSCI_P2	'0' = TSCI_P2/N2 clock is not inverted. '1' = TSCI_P2/N2 clock is inverted.	R/W	'0'
5	Pol_TSCI_P1	'0' = TSCI_P1/N1 clock is not inverted. '1' = TSCI_P1/N1 clock is inverted.	R/W	'0'
4	Pol_TSCI_P0	'0' = TSCI_P0/N0 clock is not inverted. '1' = TSCI_P0/N0 clock is inverted.	R/W	'0'
3	Pol_RSCI_P3	'0' = RSCI_P3/N3 is not inverted. '1' = RSCI_P3/N3 clock is inverted.	R/W	'0'
2	Pol_RSCI_P2	'0' = RSCI_P2/N2 clock is not inverted. '1' = RSCI_P2/N2 clock is inverted.	R/W	'0'
1	Pol_RSCI_P1	'0' = RSCI_P1/N1 clock is not inverted. '1' = RSCI_P1/N1 clock is inverted.	R/W	'0'
0	Pol_RSCI_P0	'0' = RSCI_P0/N0 clock is not inverted. '1' = RSCI_P0/N0 clock is inverted.	R/W	'0'

11.2.17 ICPCNF2—Input Clock Polarity Configuration 2 ((000)11H)

This register allows inversion of each individual Intel IXF6048 input clock.

By default, Intel IXF6048 uses the rising edge of each input clock to sample data. When the polarity configuration bit of an input clock is set to logic one, Intel IXF6048 inverts the clock before using it, i.e., Intel IXF6048 uses the falling edge of the clock.

Bit	Name	Description	Type	Default
15:2	Unused			
1	Pol_TPCI_P	'0' = TPCI_P/N clock is not inverted. '1' = TPCI_P/N clock is inverted.	R/W	'0'
0	Pol_RPCI_P	'0' = RPCI_P/N clock is not inverted. '1' = RPCI_P/N clock is inverted.	R/W	'0'

11.2.18 ICMR1—Input Clock Monitoring Register 1 ((000)12H)

This register monitors any changes of the Intel IXF6048 input clocks. All the register's bits reset upon reading the register.

Bit	Name	Description	Type	Default
15	Chg_TCI_T3	'0' = TSCI_3 or TPCI_3 have not changed since last register access. '1' = TSCI_3 or TPCI_3 have changed.	R	'0'
14	Chg_TCI_T2	'0' = TSCI_2 or TPCI_2 have not changed since last register access. '1' = TSCI_2 or TPCI_2 have changed.	R	'0'
13	Chg_TCI_T1	'0' = TSCI_1 or TPCI_1 have not changed since last register access. '1' = TSCI_1 or TPCI_1 have changed.	R	'0'
12	Chg_TCI_T0	'0' = TSCI_0, TPCI_0, or TPCI have not changed since last register access. '1' = TSCI_0, TPCI_0, or TPCI have changed.	R	'0'
11	Chg_RCI_T3	'0' = RSCI_3 or RPCI_3 have not changed since last register access. '1' = RSCI_3 or RPCI_3 have changed.	R	'0'
10	Chg_RCI_T2	'0' = RSCI_2 or RPCI_2 have not changed since last register access. '1' = RSCI_2 or RPCI_2 have changed.	R	'0'
9	Chg_RCI_T1	'0' = RSCI_1 or RPCI_1 have not changed since last register access. '1' = RSCI_1 or RPCI_1 have changed.	R	'0'
8	Chg_RCI_T0	'0' = RSCI_0, RPCI_0, or RPCI have not changed since last register access. '1' = RSCI_0, RPCI_0, or RPCI have changed.	R	'0'
7	Chg_TSCI_P3	'0' = TSCI_P3/N3 have not changed since last register access. '1' = TSCI_P3/N3 have changed.	R	'0'
6	Chg_TSCI_P2	'0' = TSCI_P2/N2 have not changed since last register access. '1' = TSCI_P2/N2 have changed.	R	'0'
5	Chg_TSCI_P1	'0' = TSCI_P1/N1 have not changed since last register access. '1' = TSCI_P1/N1 have changed.	R	'0'
4	Chg_TSCI_P0	'0' = TSCI_P0/N0 have not changed since last register access. '1' = TSCI_P0/N0 have changed.	R	'0'
3	Chg_RSCI_P3	'0' = RSCI_P3/N3 have not changed since last register access. '1' = RSCI_P3/N3 have changed.	R	'0'
2	Chg_RSCI_P2	'0' = RSCI_P2/N2 have not changed since last register access. '1' = RSCI_P2/N2 have changed.	R	'0'
1	Chg_RSCI_P1	'0' = RSCI_P1/N1 have not changed since last register access. '1' = RSCI_P1/N1 have changed.	R	'0'
0	Chg_RSCI_P0	'0' = RSCI_P0/N0 have not changed since last register access. '1' = RSCI_P0/N0 have changed.	R/W	'0'

11.2.19 ICMR2—Input Clock Monitoring Register 2 ((000)13H)

This register monitors any changes of the Intel IXF6048 input clocks. All the register's bits reset upon reading the register.

Bit	Name	Description	Type	Default
15	Chg_TXCLK_3	'0' = TXCLK_3 has not changed since last register access. '1' = TXCLK_3 has changed.	R	'0'
14	Chg_TXCLK_2	'0' = TXCLK_2 has not changed since last register access. '1' = TXCLK_2 has changed.	R	'0'
13	Chgl_TXCLK_1	'0' = TXCLK_1 has not changed since last register access. '1' = TXCLK_1 has changed.	R	'0'
12	Chg_TXCLK_0	'0' = TXCLK_0 has not changed since last register access. '1' = TXCLK_0 has changed.	R	'0'
11	Chg_RXCLK_3	'0' = RXCLK_3 has not changed since last register access. '1' = RXCLK_3 has changed.	R	'0'
10	Chg_RXCLK_2	'0' = RXCLK_2 has not changed since last register access. '1' = RXCLK_2 has changed.	R	'0'
9	Chg_RXCLK_1	'0' = RXCLK_1 has not changed since last register access. '1' = RXCLK_1 has changed.	R	'0'
8	Chg_RXCLK_0	'0' = RXCLK_0 has not changed since last register access. '1' = RXCLK_0 has changed.	R	'0'
7:2	Unused			
1	Chg_TPCI_P	'0' = TPCI_P/N has not changed since last register access. '1' = TPCI_P/N has changed.	R	'0'
0	Chg_RPCI_P	'0' = RPCI_P/N has not changed since last register access. '1' = RPCI_P/N has changed.	R	'0'

11.2.20 NCMODECNF—Non-Concatenated Mode Configuration Register ((000)14H)

Bit	Name	Description	Type	Default
15:5	Unused			
4	J0Mux_Cnf	This bit configures how the Z0 (previously known as C0) bytes are generated by the SONET/SDH Multiplexer: '0' = The Z0 bytes are not overwritten by the SONET/SDH Multiplexer. The multiplexer transmits the Z0 bytes generated by the transmit channels (transparency). '1' = The Z0 bytes are overwritten by the SONET/SDH Multiplexer: 02, 03, 04, etc.	R/W	'1'
3	Unused			
2	BWMux_Cnf	This bit configures how the SONET/SDH Multiplexer interleaves the SONET/SDH frames generated by each transmit channel: '0' = Word (32-bit) interleaved multiplexing. '1' = Byte interleaved multiplexing.	R/W	'0'
1	Unused			
0	BWDmx_Cnf	This bit configures how the SONET/SDH Demultiplexer de-interleaves the received SONET/SDH frames: '0' = Word (32-bit) interleaved demultiplexing. '1' = Byte interleaved demultiplexing.	R/W	'0'

11.2.21 PRBSINT—PRBS Analyzer Interrupt Register ((000)1AH)

Bit	Name	Description	Type	Default
15:4	Unused			
3:0	PRBSI[3:0]	PRBSErr[i] (i = 0, 1, 2, 3) are set to logic one when the PRBS analyzer, in receive channel #i, detects an error in the incoming PRBS sequence. The PRBSErr[i] bits (i = 0, 1, 2, 3) are self-cleared upon reading this register.	R	0000

11.2.22 PRBSINTEN—PRBS Analyzer Interrupt Enable Register ((000)1BH)

Bit	Name	Description	Type	Default
15:4	Unused			
3:0	PRBSIEn[3:0]	Active-high enable for the PRBSI[3:0] interrupt bits.	R/W	0000

11.2.23 TALBINT—Transmit Alarm Bus Interrupt Register ((000)1CH)

Bit	Name	Description	Type	Default
15:12	TpalCrcI[3:0]	TpalCrcI[i] (i = 0, 1, 2, 3) are set to logic one when Intel IXF6048 detects a CRC-4 error in the transmit path alarm bus. The TpalBusI[i] bits (i = 0, 1, 2, 3) are self-cleared upon reading this register.	R	0000
11:8	TpalBusI[3:0]	TpalBusI[i] (i = 0, 1, 2, 3) are set to logic one when Intel IXF6048 detects the absence of clock or delineation pulse in the transmit path alarm bus. These interrupt bits are used only when the transmit path alarm bus are configured in codirectional mode. The TpalBusI[i] bits (i = 0, 1, 2, 3) are self-cleared upon reading this register.	R	0000
7:4	TsalCrcI[3:0]	TsalCrcI[i] (i = 0, 1, 2, 3) are set to logic one when Intel IXF6048 detects a CRC-4 error in the transmit section alarm bus. The TsalBusI[i] bits (i = 0, 1, 2, 3) are self-cleared upon reading this register.	R	0000
3:0	TsalBusI[3:0]	TsalBusI[i] (i = 0, 1, 2, 3) are set to logic one when Intel IXF6048 detects the absence of clock or delineation pulse in the transmit section alarm bus. These interrupt bits are used only when the transmit section alarm bus are configured in codirectional mode. The TsalBusI[i] bits (i = 0, 1, 2, 3) are self-cleared upon reading this register.	R	0000

11.2.24 TALBINTEN—Transmit Alarm Bus Interrupt Enable Register ((000)1DH)

Bit	Name	Description	Type	Default
15:12	TpalCrcIEn[3:0]	Active-high enable for the TpalCrcI[3:0] bits.	R/W	0000
11:8	TpalBusIEn[3:0]	Active-high enable for the TpalBusI[3:0] bits.	R/W	0000
7:4	TsalCrcIEn[3:0]	Active-high enable for the TsalCrcI[3:0] bits.	R/W	0000
3:0	TsalBusIEn[3:0]	Active-high enable for the TsalBusI[3:0] bits.	R/W	0000

11.2.25 LSPCNF—Line Side Parity Configuration Register ((000)1EH)

This register configures Intel IXF6048 line side parity signals.

Bit	Name	Description	Type	Default
15:3	Unused			

Bit	Name	Description	Type	Default
2	PrtyMode_Cnf	PrtyMode_Cnf configures how the parallel PECL line side interface parity signals (TPRTY_P/N and RPRTY_P/N) are used: '0' = The parity bit protects only the parallel data bus. TPRTY_P/N protects TPDO_P/N[15:0]. RPRTY_P/N protects RPDI_P/N[15:0]. '1' = The parity bit protects both the parallel data bus and the frame pulse: TPRTY_P/N protects TPDO_P/N[15:0] and TFPO_P/N. RPRTY_P/N protects RPDI_P/N[15:0] and RFPI_P/N.	R/W	'0'
1	RcvPrty_Cnf	RcvPrty_Cnf configures the type of parity used in the receive parallel PECL line side interface (RPRTY_P/N input): '0' = RPRTY_P/N serves as the odd parity over RPDI_P/N[15:0] (and optionally RFPI_P/N). '1' = RPRTY_P/N serves as the even parity over RPDI_P/N[15:0] (and optionally RFPI_P/N).	R/W	'0'
0	XmtPrty_Cnf	XmtPrty_Cnf configures the type of parity used in the transmit parallel PECL line side interface (TPRTY_P/N output): '0' = TPRTY_P/N serves as the odd parity over TPDO_P/N[15:0] (and optionally TFPO_P/N). '1' = TPRTY_P/N serves as the even parity over TPDO_P/N[15:0] (and optionally TFPO_P/N).	R/W	'0'

11.2.26 LSPINT—Line Side Parity Interrupt Register ((000)1FH)

Bit	Name	Description	Type	Default
15:1	Unused			
0	RcvPrtyI	RcvPrtyI is set to logic one when a parity error is detected in the receive parallel PECL line side interface. This interrupt bit clears automatically upon reading this register.	R	'0'

11.2.27 LSPINTEN—Line Side Parity Interrupt Enable Register ((000)20H)

Bit	Name	Description	Type	Default
15:1	Unused			
0	RcvPrtyIEn	Active-high enable for the RcvPrtyI interrupt bit.	R/W	'0'

11.2.28 MISC_GIS—Miscellaneous Global Interrupt Source Register ((000)21H)

This register indicates that a global interrupt source register contains an active interrupt. Each bit in this register is active-high and represents the logic OR of all the interrupt bits in the associated interrupt source register. Each bit in this register clears upon reading the associated interrupt source register.

Bit	Name	Description	Type	Default
14:5	Unused			
4	PRBSInt	PRBSInt indicates that one or more interrupt bits are active in the PRBSINT register (Global registers).	R	'X'
3	TAlbInt	TAlbInt indicates that one or more interrupt bits are active in the TALBINT register (Global registers).	R	'X'
2	LSPInt	LSPInt indicates that one or more interrupt bits are active in the LSPINT register (Global registers).	R	'X'
1	XmtUtoInt	XmtUtoInt indicates that one or more interrupt bits are active in the T_UTOINT register (UTOPIA interface registers).	R	'X'
0	RcvUtoInt	RcvUtoInt indicates that one or more interrupt bits are active in the R_UTOINT register (UTOPIA interface registers).	R	'X'

11.3 UTOPIA Interface Registers

11.3.1 R_UICNF—Receive UTOPIA Interface Configuration ((000)70H)

This register configures the receive UTOPIA interface features that are common to the four channels.

Bit	Name	Description	Type	Default
15:12	Unused			
11	RcvVal2Cnf	RcvVal2Cnf configures under which conditions the reading in the receive interface is blocked. When RcvValCnf = '0', reading is never blocked thus RcvVal2Cnf is only taken into account when RcvValCnf = '1'. In this case: if RcvVal2Cnf = '0' then reading is blocked after an EOF is read or the FIFO is empty if RcvVal2Cnf = '1' then reading is only blocked after an EOF is read	R/W	'0'
10	RcvATMHEC	RcvATMHEC is used in 8-bit mode (RcvUWidth = '00') to select the information stored in the extra byte, when an extra byte is passed through the UTOPIA interface (RcvCellStruct = '1' in register R_UICHCNF): '1' = The received HEC is passed as the extra byte. '0' = Two status bits are passed. Bit 0 indicates whether the header was error free. If bit 0 is a '1' (meaning that there were errors in the header), then bit 1 indicates whether the error is single (bit 1 = '0') or multiple (bit 1 = '1'). In 16- or 32-bit modes, both HEC and status are copied in the extra word (when RcvCellStruct = '1'). In these modes bits 15:8 contain the received HEC and bits 1:0 contain the status with the same meaning as explained for 8-bit mode.	R/W	'0'
9	RcvSmallMem	RcvSmallMem reduces the size of the receive UTOPIA interface FIFO memory used by channel #0: '0' = Channel #0's receive FIFO size is 16-Kbyte. '1' = Channel #0's receive FIFO size is 2-Kbyte. RcvSmallMem can be used to force identical behavior in all four channels.	R/W	'0'
8	RcvTestOEn	RcvTestOEn configures whether the unused signals, resulting from the interface configuration, are set to high impedance: '0' = Unused signals in the interface (POS signals when configured in ATM mode or signals used only in quad mode when configured in single mode) are held in high-impedance. '1' = Unused signals, determined by the interface configuration, are not held in high-impedance.	R/W	'0'
7	RcvValCnf	RcvValCnf configures how the RXVAL output is used. '0' = The reading is never blocked. RXVAL is deasserted when attempting to read an empty FIFO. In this case, the read command is disregarded. '1' = Apart from RXVAL being deasserted when attempting to read an empty FIFO, the reading is blocked under the conditions configured in RcvVal2Cnf. When the reading is blocked, RXVAL is also deasserted and all the read commands are disregarded until the port is deselected and reselected.	R/W	'0'

Bit	Name	Description	Type	Default
6	RcvFifEmptEOF	RcvFifEmptEOF configures the assertion condition of RXFA_i (i = 0, 1, 2, 3) in POS mode: '0' = RXFA_i is asserted if the FIFO contains one or more EOFs **or** if the FIFO contains a number of words equal to or greater than the receive programmable watermark (register R_PWM). '1' = RXFA_i is asserted if the FIFO contains a number of words equal to or greater than the receive programmable watermark (register R_PWM).	R/W	'0'
5	RcvDirStatCnf	RcvDirStatCnf use the RXFA_i (i = 0, 1, 2, 3) outputs in two different ways: '1' = Direct status indication mode. The RXFA_i (i = 0, 1, 2, 3) outputs are always driven. '0' = Multiplexed status polling. The RXFA_i (i = 0, 1, 2, 3) outputs are driven only after one (UTOPIA Level 2) or two (UTOPIA Level 3) clock cycles with an address in the RXADDR bus matching the programmed base-address value UaddrBase[2:0].	R/W	'1'
4	RcvMPhyDevCnf	RcvMPhyDevCnf configures the receive interface as follows: '1' = The receive used outputs are only driven when the device is selected for a receive cell transfer. RXPFA is only driven when RXADDR matches the programmed device address. This setting **must** be used when Intel IXF6048 shares the receive interface with **other PHY devices**. '0' = The receive outputs RXDATA, RXSOF, RXPRTY, and RXFA are always driven. This setting **can** be used when Intel IXF6048 is the **only PHY device** in the receive interface.	R/W	'0'

Bit	Name	Description	Type	Default
3	RcvUQuad	RcvUQuad sets the receive UTOPIA interface: '0' = Single receive UTOPIA interface. '1' = Quad receive UTOPIA interface.	R/W	'0'
2:1	RcvUWidth[1:0]	RcvUWidth[1:0] sets the width of the receive UTOPIA data bus (RXDATA): '00' = 8-bit data interface '01' = 16-bit data interface '10' = 32-bit data interface '11' = 64-bit data interface **NOTE:** When the receive UTOPIA interface is configured in Quad mode (RcvUQuad set to logic one), configuration values '10' (32-bit) and '11' (64-bit) are invalid.	R/W	'10'
0	RcvSelMode	RcvSelMode configures the receive POS-UTOPIA interface port selection mode: '0' = The receive POS-UTOPIA interface operates similar to the ATM-UTOPIA interface, with two independent processes running in parallel: the data transfer and the port selection. RXADDR[4:0] are used to select a port when RXENB changes from '1' to '0' and to poll the status of the FIFOs (using the output RXPFA). Once the port is selected (RXENB = '0'), RXADDR[4:0] can take any value (FIFO status polling using RXPFA). '1' = The POS-UTOPIA interface is controlled as a memory mapped device. There is no selection cycle or FIFO status polling, just port addressing. The RXPFA output is not used and the status of each FIFO is indicated using the direct outputs RXFA_0, RXFA_1, RXFA_2, and RXFA_3. Nothing happens when RXENB = '1'. If RXENB = '0', the interface reads the FIFO indicated by RXADDR[4:0]. In this mode, the decode-response is still indicated for each channel by RcvDRCnf (in register R_UICHCNF). Thus, independently of when the channel selection occurs, the outputs will switch one or two cycles (as indicated by RcvDRCnf) after RXENB is asserted.	R/W	'0'

11.3.2 R_UIIML—Receive UTOPIA Interface Initiation Minimum Level ((000)71H)

This register configures the receive UTOPIA interface features that are common to the four channels.

Bit	Name	Description	Type	Default
15:8	Unused			
7:0	RcvIML[7:0]	RcvIML[7:0] configures the minimum level of available space the receive FIFO must contain to initiate the reception (writing in the FIFO) of a new packet. RcvIML[7:0] are used to avoid consecutive FIFO overflows (to recover after an overflow condition). The contents of RcvIML[7:0] indicates the number of 16-word blocks (64-byte blocks). **Channels 1, 2 and 3:** The size of the FIFO is 512 words of 32 bits (2048 bytes) and only RcvIML[4:0] are used (RcvIML[7:5] are unused bits). RcvIML[4:0] sets one of 32 different minimum levels: 00000 = Initiate Rx if FIFO contains 1 or more free words. 00001 = Initiate Rx if FIFO contains 17 or more free words. 00010 = Initiate Rx if FIFO contains 33 or more free words. …… 11110 = Initiate Rx if FIFO contains 481 or more free words. 11111 = Initiate Rx if FIFO contains 497 or more free words. **Channel 0:** The size of the FIFO is 4096 words of 32 bits (16 Kbytes) and RcvIML[7:0] sets one of 256 different minimum levels: 00000000 = Initiate Rx if FIFO contains 1 or more free words. 00000001 = Initiate Rx if FIFO contains 17 or more free words. 00000010 = Initiate Rx if FIFO contains 33 or more free words. …… 11111110 = Initiate Rx if FIFO contains 4065 or more free words. 11111111 = Initiate Rx if FIFO contains 4081 or more free words.	R/W	02H

11.3.3 R_UICHCNF—Receive UTOPIA Interface Channel Configuration ((0cc)60H)

This register configures the receive UTOPIA interface features for every channel. When the UTOPIA interface is configured in single mode (RcvUQuad = '0'), the configuration for the interface (except for the bit RcvFIFORst) is the one indicated for channel 0. RcvFIFORst is independent for every channel, regardless of interface mode.

Bit	Name	Description	Type	Default
15:11	Unused			
10	RcvFACnf	RcvFACnf configures the outputs RXPFA (receive polled frame available output) and RXFA_i (i = 0, 1, 2, 3, receive direct frame available outputs) as active-high or active-low signals: '0' = Normal mode. RXPFA and RXFA_i (i = 0, 1, 2, 3) are active-high output signals i.e., a logic one means there is data in the FIFO. '1' = RXPFA and RXFA_i (i = 0, 1, 2, 3) are active-low output signals i.e., a logic zero means there is data in the FIFO.	R/W	'0'
9	RcvPrtyCnf	RcvPrtyCnf configures the type of parity used in the receive UTOPIA interface (RXPRTY output): '0' = RXPRTY serves as the odd parity over RXDATA. '1' = RXPRTY serves as the even parity over RXDATA.	R/W	'0'
8	RcvDRCnf	RcvDRCnf configures the decode-response delay for the receive interface: '0' = The decode-response delay in the receive UTOPIA interface is one clock cycle. '1' = The decode-response delay in the receive UTOPIA interface is two clock cycles.	R/W	'1'

Bit	Name	Description	Type	Default
7	RcvFIFORst	RcvFIFORst resets the receive FIFO: '0' = The receive FIFO operates normally. '1' = The FIFO is emptied and any further read command is disregarded. All the frames (in POS mode) or cells (in ATM mode) received while RcvFIFORst = '1' are lost but it are not considered a FIFO overflow.	R/W	'0'
6	RcvCellStruct	RcvCellStruct selects the cell data structure used in the receive ATM-UTOPIA interface: '0' = No extra words are used between the first four ATM cell header bytes (no HEC field) and the first ATM cell payload byte. Depending on the data bus width configuration, that corresponds to a cell data structure of 7 words (64-bit interface), 13 words (32-bit interface), 26 words (16-bit interface), or 52 words (8-bit interface). '1' = An extra word (unused word) is used between the first four ATM cell header bytes (no HEC field) and the first ATM cell payload byte. Depending on the data bus width configuration, that corresponds to a cell data structure of 8 words (64-bit interface), 14 words (32-bit interface), 27 words (16-bit interface), or 53 words (8-bit interface).	R/W	'0'
5:0	RcvCADeassert[5:0]	RcvCADeassert[5:0] configures when to deassert RXPFA (receive polled cell available output) and RXFA_i (i = 0, 1, 2, 3, receive direct cell available outputs) when the addressed channel works in ATM mode. When the ATM cell being read in the UTOPIA interface is the last complete cell in the FIFO, each of these outputs are deasserted when the word containing the cell byte indicated by RcvCADeassert[5:0]: 1, 2, 3,… n. (n = 52, 53, 54, or 56). The value of n (number of bytes of the cell) depends on the cell structure. RcvCADeassert **cannot be configured to zero**. Configuring RcvCADeassert[5:0] to an appropriate value ensures that the ATM Layer device can detect that the current ATM cell is the last cell in the FIFO, four clock cycles (or more) before reading the last word.	R/W	19H

11.3.4 R_PWM—Receive Programmable Watermark ((0cc)61H)

Bit	Name	Description	Type	Default
15:12	Unused			
11:0	RcvPWM[11:0]	The receive programmable watermark RcvPWM is used to control the assertion and deassertion of the receiver outputs RXPFA and RXFA_i (i = 0, 1, 2, 3) when the addressed channel works in POS mode. RXPFA and RXFA_i (i = 0, 1, 2, 3) are asserted when the FIFO contains an end-of-packet **or** contains a number of 32-bit words equal to or greater than RcvPWM. RXPFA and RXFA_i (i = 0, 1, 2, 3) are deasserted when the FIFO does not contain an end of packet (see RcvFifEmptEOF in the register R_UICNF) **and** contains a number of 32-bit words less than RcvPWM. **Channels 1, 2, and 3:** The size of the FIFO is 512 words of 32 bits (2048 bytes) and only RcvPWM[8:0] are used (9-bit watermark). RcvPWM[11:9] are unused bits. **Channel 0:** The size of the FIFO is 4096 words of 32 bits (16 Kbytes) and RcvPWM[11:0] are used as a 12-bit watermark.	R/W	00FH

11.3.5 T_UICNF—Transmit UTOPIA Interface Configuration ((000)50H)

This register configures the transmit UTOPIA interface features that are common to the four channels.

Bit	Name	Description	Type	Default
15:8	Unused			
7	XmtSmallMem	XmtSmallMem selects the size of the transmit UTOPIA interface FIFO memory used by channel #0: '0' = Channel #0's transmit FIFO size is 16-Kbyte. '1' = Channel #0's transmit FIFO size is 2-Kbyte. XmtSmallMem can be used to force identical behavior in all four channels.	R/W	'0'
6	XmtFifEmptEOF	XmtFifEmptEOF selects when the POS transmitter can start the transmission of a new packet: '0' = The POS transmitter starts the transmission of a new packet, if the FIFO contains an EOF **or** the FIFO contains a number of words equal to or greater than the Transmit Initiation Minimum Level (register T_UIIML). '1' = The POS transmitter starts the transmission of a new packet, if the FIFO contains a number of words equal to or greater than the Transmit Initiation Minimum Level (register T_UIIML).	R/W	'0'
5	XmtDirStatCnf	XmtDirStatCnf configures the TXFA_i (i = 0, 1, 2, 3) outputs in two different ways: '1' = Direct status indication mode. The TXFA_i (i = 0, 1, 2, 3) outputs are always driven. '0' = Multiplexed status polling. The TXFA_i (i = 0, 1, 2, 3) outputs are driven only after one (UTOPIA Level 2) or two (UTOPIA Level 3) clock cycles with an address in the TXADDR bus matching the programmed base-address value UaddrBase[2:0].	R/W	'1'

Bit	Name	Description	Type	Default
4	XmtMPhyDevCnf	XmtMPhyDevCnf configures the transmit interface as follows: '1' = The transmit output TXPFA is only driven when TXADDR matches the programmed device address (Level 2 mode). This setting **must** be used when Intel IXF6048 shares the transmit interface with **other PHY devices**. '0' = The transmit output TXPFA is always driven. This setting **can** be used when Intel IXF6048 is the **only PHY device** in the transmit interface.	R/W	'0'
3	XmtUQuad	XmtUQuad sets the transmit UTOPIA interface. '0' = Single transmit UTOPIA interface. '1' = Quad transmit UTOPIA interface.	R/W	'0'
2:1	XmtUWidth[1:0]	XmtUWidth[1:0] sets the width of the transmit UTOPIA data bus (TXDATA): '00' = 8-bit data interface '01' = 16-bit data interface '10' = 32-bit data interface '11' = 64-bit data interface **NOTE:** when the transmit UTOPIA interface is configured in Quad mode (XmtUQuad set to logic one), configuration values '10' (32-bit) and '11' (64-bit) are invalid.	R/W	'10'
0	XmtSelMode	XmtSelMode configures the transmit POS-UTOPIA interface port selection mode. '0' = The transmit POS-UTOPIA interface operates similar to the ATM-UTOPIA interface, with two independent processes running in parallel: the data transfer and the port selection. TXADDR[4:0] are used to select a port when TXENB changes from '1' to '0' and to poll the status of the FIFOs (using the output TXPFA). Once the port is selected (TXENB = '0'), TXADDR[4:0] can take any value (FIFO status polling using TXPFA). '1' = The POS-UTOPIA interface is controlled as a memory mapped device. There is no selection cycle or FIFO status polling, just port addressing. The TXPFA output is not used and the status of each FIFO is indicated using the direct outputs TXFA_0, TXFA_1, TXFA_2, and TXFA_3. Nothing happens when TXENB = '1'. If TXENB = '0', the value transferred in TXDATA is written in the FIFO indicated by TXADDR[4:0].	R/W	'0'

11.3.6 T_UIIML—Transmit UTOPIA Interface Initiation Minimum Level ((000)51H)

This register configures the transmit UTOPIA interface features that are common to the four channels.

Bit	Name	Description	Type	Default
15:8	Unused			
7:0	XmtIML[7:0]	XmtIML[7:0] configures the minimum level of data the transmit FIFO must contain to initiate the transmission of a new packet (to read the first word of a packet). XmtIML[7:0] are used to avoid consecutive FIFO underflows. They are only considered when a new packet is going to be transmitted and there is no complete packet in the FIFO, and XmtFifEmptEOF = '0'. If the FIFO contains an EOF, the transmission starts regardless of the IML value and the amount of data in the FIFO. The contents of XmtIML[7:0] indicates the number of 16-word blocks (64-byte blocks). **Channels 1, 2, and 3:** The size of the FIFO is 512 words of 32 bits (2048 bytes) and only XmtIML[4:0] are used (XmtIML[7:5] are unused bits). XmtIML[4:0] sets one of 32 different minimum levels: 0000 = Initiate Tx if FIFO contains 1 or more words. 0001 = Initiate Tx if FIFO contains 17 or more words. 0010 = Initiate Tx if FIFO contains 33 or more words. …… 1110 = Initiate Tx if FIFO contains 481 or more words. 1111 = Initiate Tx if FIFO contains 497 or more words. **Channel 0:** The size of the FIFO is 4096 words of 32 bits (16-Kbytes) and XmtIML[7:0] sets one of 256 different minimum levels: 00000000 = Initiate Tx if FIFO contains 1 or more words. 00000001 = Initiate Tx if FIFO contains 17 or more words. 00000010 = Initiate Tx if FIFO contains 33 or more words. …… 11111110 = Initiate Tx if FIFO contains 4065 or more words. 11111111 = Initiate Tx if FIFO contains 4081 or more words.	R/W	02H

11.3.7 T_UICHCNF—Transmit UTOPIA Interface Channel Configuration ((0cc)40H)

This register configures the transmit UTOPIA interface features for every channel. When UTOPIA interface is configured in single mode (XmtUQuad = '0'), the configuration for the interface (except for the bit XmtFIFORst) is the one indicated for channel 0. XmtFIFORst is independent for every channel regardless of interface mode.

Bit	Name	Description	Type	Default
15:11	Unused			
10	XmtFACnf	XmtFACnf configures the outputs TXPFA (transmit polled frame available output), TXSFA (transmit selected frame-available output), and TXFA_i (i = 0, 1, 2, 3, transmit direct frame available outputs) as active-high or active-low signals: '0' = Normal mode. TXPFA and TXFA_i (i = 0, 1, 2, 3) are active-high output signals i.e., a logic one means there is available space for a complete ATM cell. '1' = TXPFA and TXFA_i (i = 0, 1, 2, 3) are active-low output signals i.e., a logic zero means there is available space for a complete ATM cell.	R/W	'0'
9	XmtPrtyCnf	XmtPrtyCnf configures the type of parity used in the transmit UTOPIA interface (TXPRTY input): '0' = Input TXPRTY serves as the odd parity over TXDATA. '1' = Input TXPRTY serves as the even parity over TXDATA.	R/W	'0'
8	XmtDRCnf	XmtDRCnf configures the decode-response delay for the transmit interface: '0' = The decode-response delay in the transmit UTOPIA interface is one clock cycle. '1' = The decode-response delay in the transmit UTOPIA interface is two clock cycles.	R/W	'1'

Bit	Name	Description	Type	Default
7	XmtFIFORst	XmtFIFORst resets the transmit FIFO. '0' = The transmit FIFO operates normally. '1' = The FIFO is emptied and any following write commands are disregarded. As soon as a logic zero is written into XmtFIFORst, the UTOPIA interface accepts new writes, after receiving the first start of frame (TXSOF input).	R/W	'0'
6	XmtCellStruct	XmtCellStruct selects the cell data structure used in the transmit ATM-UTOPIA interface: '0' = No extra words are used between the first four ATM cell header bytes (no HEC field) and the first ATM cell payload byte. Depending on the data bus width configuration, that corresponds to a cell data structure of 7 words (64-bit interface), 13 words (32-bit interface), 26 words (16-bit interface), or 52 words (8-bit interface). '1' = An extra word (unused word) is used between the first four ATM cell header bytes (no HEC field) and the first ATM cell payload byte. Depending on the data bus width configuration, that corresponds to a cell data structure of 8 words (64-bit interface), 14 words (32-bit interface), 27 words (16-bit interface), or 53 words (8-bit interface).	R/W	'0'
5:0	XmtCADeassert [5:0]	XmtCADeassert[5:0] configures when to deasserted TXPFA (transmit polled cell available output), TXSFA (transmit selected frame-available output), and TXFA_i (i = 0, 1, 2, 3, transmit direct cell available outputs) in the transmit ATM-UTOPIA interface. When the ATM cell being written into the UTOPIA interface is stored in the last cell-slot available in the FIFO, each of these outputs is deasserted three clock cycles after the TXCLK rising edge that samples the word indicated by XmtCADeassert[5:0]: 1, 2, 3,… n-3 (n = 7, 13, 14, 52, 53). The value of n (number of words of the cell) depends on the bus width and the cell structure. Configuring XmtCADeassert[5:0] to an appropriate value ensures that the ATM Layer device can detect that the current ATM cell is going to fill up the transmit FIFO, four clock cycles (or more) before writing the last word.	R/W	19H

11.3.8 T_UIFDP—Transmit UTOPIA Interface FIFO Depth ((0cc)41H)

Bit	Name	Description	Type	Default
15:8	Unused			
7:0	XmfFDCnf[7:0]	XmtFDCnf[7:0] configures the depth of the transmit FIFO when the channel works in ATM mode. TXFA is deasserted when the number of cells in the FIFO is greater than indicated by XmfFDCnf[7:0]. If the configured FIFO depth is smaller than the real depth of the FIFO, additional cells, after the configured depth is reached, are written into the FIFO until the FIFO is full. For channels 1, 2, and 3, only XmtFDCnf[4:0] are used and XmtFDCnf[7:5] are unused bits.	R/W	FFH

11.3.9 T_NFPWM—Transmit Near Full Programmable Watermark ((0cc)42H)

Bit	Name	Description	Type	Default
15:12	Unused			
11:0	XmtNFPWM[11:0]	The transmit nearly full programmable watermark XmtNFPWM is used to control the deassertion of the transmitter outputs TXPFA, TXSFA, and TXFA_i (i = 0, 1, 2, 3) in POS and transparent (direct mapping) modes only. This value (XmtNFPWM) *must always be less than or equal to* the transmit near empty watermark value (XmtNEPWM). TXPFA, TXSFA, and TXFA_i (i = 0, 1, 2, 3) are deasserted when the transmit FIFO is full or the available space (in 32-bit words) is less than XmtNFPWM. **Channels 1, 2, and 3:** The size of the FIFO is 512 words of 32 bits (2048 bytes) and only XmtNFPWM[8:0] are used (9-bit watermark). XmtNFPWM[11:9] are unused bits. **Channel 0:** The size of the FIFO is 4096 words of 32 bits (16 Kbytes) and XmtNFPWM[11:0] are used as a 12-bit watermark.	R/W	1FH

11.3.10 T_NEPWM—Transmit Near Empty Programmable Watermark ((0cc)43H)

Bit	Name	Description	Type	Default
15:12	Unused			
11:0	XmtNEPWM [11:0]	The transmit near empty programmable watermark XmtNEPWM is used to control the assertion of the transmitter outputs TXPFA, TXSFA, and TXFA_i (i = 0, 1, 2, 3) in POS and transparent (direct mapping) modes only. This value (XmtNEPWM) *must always be greater* than the transmit near full watermark value (XmtNFPWM). TXPFA, TXSFA, and TXFA_i (i = 0, 1, 2, 3) are asserted when the FIFO's available space (in 32-bit words) is equal to or greater than XmtNEPWM. **NOTE:** There could be a dead space from when the transmit FIFO is emptied after a high watermark (near full) condition to a low watermark (near empty) condition where the TXFA will be equal to 0 - deasserted. This is because the TXFA is set to 0 when it passes the high watermark value (near full) and does not get reset to 1 (asserted) until it is emptied to at least the low watermark value (near empty). This could cause a see-saw like effect in the throughput. **Channels 1, 2, and 3:** The size of the FIFO is 512 words of 32 bits (2048 bytes) and only XmtNEPWM[8:0] are used (9-bit watermark). XmtNEPWM[11:9] are unused bits. **Channel 0:** The size of the FIFO is 4096 words of 32 bits (16 Kbytes) and XmtNEPWM[11:0] are used as a 12-bit watermark.	R/W	FFH

11.3.11 R_UTOINT—Receive UTOPIA Interface Interrupt Register ((000)72H)

Bit	Name	Description	Type	Default
15:8	Unused			
7:4	RcvFIFOOFI[3:0]	RcvFIFOOFI[i] (i = 0, 1, 2, 3) is set to logic one when a receive FIFO overflow occurs in channel i. This interrupt is meant to be used when the channel is configured in transparent mode. In ATM or POS modes, both ATM and POS processors monitor the FIFO overflow condition.	R	0000
3:0	RcvFifoUFI[3:0]	RcvFifoUFI[i] (i = 0, 1, 2, 3) is set to logic one when a receive FIFO underflow occurs in channel i, e.g., the Link Layer device attempts to read a new ATM cell from a FIFO that does not contain a complete ATM cell (in ATM mode) or attempts to read a word when the FIFO is empty (in POS mode). These interrupt bits clear upon reading this register.	R	0000

11.3.12 T_UTOINT—Transmit UTOPIA Interface Interrupt Register ((000)52H)

Bit	Name	Description	Type	Default
15:12	XmtFifoUFI[3:0]	XmtFifoUFI[i] (i = 0, 1, 2, 3) are set to logic one when a transmit FIFO underflow occurs in channel i. These interrupts are meant to be used in transparent mode. If data is needed from the FIFO to be mapped into the SPE and the FIFO is empty then the interrupt is asserted.	R	0000
11:8	XmtSOCI[3:0]	XmtSOCI set to logic one when a start of cell (TXSOF input) is sampled high in an incorrect position, which is any position different than the first word of an ATM cell. When TXSOF is sampled high during any position other than the first word of an ATM cell, XmtSOCI are activated and the FIFO write address is initialized so the previous incomplete cell is overwritten by the new cell. TXSOF is not required to be high when writing the first word of an ATM cell. If TXSOF is low, when writing the first word of a cell, it is not considered an error and XmtSOCI are not activated. These interrupt bits clear upon reading this register.	R	0000
7:4	XmtPrtyErrI[3:0]	When the interface is working in quad mode (XmtUMode = '00' in register T_UICNF), XmtPrtyErrI[i] are set to logic one if a parity error occurs in channel i. When working in single mode, the four bits take the same value and are asserted if a parity error occurs in the data bit. These interrupt bits clear upon reading this register.	R	0000
3:0	XmtFifoOFI[3:0]	XmtFifoOFI[i] (i = 0, 1, 2, 3) are set to logic one when a transmit FIFO overflow occurs in channel i, e.g.,the ATM Layer device attempts to write into a full FIFO. These interrupt bits are cleared automatically after this register is read.	R	0000

11.3.13 R_UTOINTEN—Receive UTOPIA Interface Interrupt Enable Register ((000)73H)

Bit	Name	Description	Type	Default
15:8	Unused			
7:4	RcvFifoOFIEn[3:0]	Active-high enable for the RcvFifoOFI[3:0] interrupt bits	R/W	0000
3:0	RcvFifoUFIEn[3:0]	Active-high enable for the RcvFifoUFI[3:0] interrupt bits.	R/W	0000

11.3.14 T_UTOINTEN—Receive UTOPIA Interface Interrupt Enable Register ((000)53H)

Bit	Name	Description	Type	Default
15:12	XmtFifoUFIEn[3:0]	Active-high enable for the XmtFifoUFI[3:0] interrupt bits.	R/W	0000
11:8	XmtSOCIEn[3:0]	Active-high enable for the XmtSOCI[3:0] interrupt bits.	R/W	0000
7:4	XmtPrtyErrIEn[3:0]	Active-high enable for the XmtPrtyErrI[3:0] interrupt bits.	R/W	0000
3:0	XmtFifoOFIEn[3:0]	Active-high enable for the XmtFifoOFI[3:0] interrupt bits.	R/W	0000

11.4 SONET/SDH Receive Regenerator Section Termination Channel Registers

11.4.1 R_RSTC—Receive RST Configuration ((1cc)80H)

Configures Regenerator Section Termination parameters of the chip (SDH/SONET block).

Bit	Name	Description	Type	Default
15	RcvScrmblCnfg	This bit controls the receive scrambler operation: '0' = Disables receive scrambler. '1' = Enables receive scrambler 2e7.	R/W	'1'
14	RcvFBaDsbl	Disables the receive byte and frame alignment when using an external frame pulse reference input (see input pin RFPI): '1' = disabled '0' = enabled	R/W	'0'

Bit	Name	Description	Type	Default
13	RcvFwdOofCnfg	Configures the frameword checking during frame desynchronization (from an In Frame condition to an Out Of Frame) in OC-12 and OC-48 modes of operation. It can be configured on all or on different subsets of the A1 and A2 framing bytes: '0' = In OC-12 mode, OOF is declared when 4 (or 5: see register LOF_LMN) consecutive erroneous frameworks not matching the entire framing pattern (12 A1 bytes followed by 12 A2 bytes) have been detected. '0' = In OC-48 mode, OOF is declared when 4 (or 5: see register LOF_LMN) consecutive erroneous frameworks not matching a 24 byte subset of the framing pattern (12 A1 bytes followed by 12 A2 bytes) have been detected. '1' = In either OC-12 or OC-48 modes, OOF is declared when 4 (or 5: see register LOF_LMN) consecutive erroneous frameworks not matching a 6-byte subset of the framing pattern (48 bits at the A1/A2 transition) have been detected. (SDH) **NOTE:** in the OC-1 or OC-3 modes of operation, this configuration bit is ignored as the frameword is checked on the entire pattern (3×A1 bytes followed by 3×A2 bytes in OC-3 and one A1 followed by one A2 byte in OC-1).	R/W	'0'
12	RcvFwdOnCnfg	Configures the frameword detection during frame acquisition (from an Out Of Frame to an In Frame condition) in OC-12 and OC-48 modes of operation. It can be used on all or on different subsets of the A1 and A2 framing bytes: '0' = In OC-12 mode, the frame is synchronized when two consecutive frameworks matching the entire framing pattern (12 A1 bytes followed by 12 A2 bytes) have been detected. '0' = In OC-48 mode, the frame is synchronized when two consecutive frameworks matching a 24-byte subset of the framing pattern (12 A1 bytes followed by 12 A2 bytes) have been detected. '1' = In either OC-12 or OC-48 modes, the frame is synchronized when two consecutive frameworks matching a 6-byte subset of the framing pattern (48 bits at the A1/A2 transition) have been detected. **NOTE:** In the OC-1 or OC-3 modes of operation, this configuration bit is ignored as the frameword is detected on the entire pattern (3×A1 bytes followed by 3×A2 bytes in OC-3 and one A1 followed by one A2 byte in OC-1).	R/W	'0'
11	CnfgB1Cntr	Configures the B1 error counter to update on bit errors or block errors: '0' = Bit errors. '1' = Block errors.	R/W	'0'
10:9	RcvLosCnfg [1:0]	Configures the internally generated LOS alarm: '11' = LOS alarm sets when no transition occurs in the incoming data for at least 25 µs and clears if two consecutive frameworks are detected with no LOS condition between them. (SDH) '10' = LOS alarm sets when all '0's occurs in the incoming data for at least 25 µs and clears if two consecutive frameworks are detected with no LOS condition between them. '01' = LOS alarm sets when no transition occurs in the incoming data for at least 20 µs and clears if two consecutive frameworks are detected with no LOS condition between them. (SDH) '00' = LOS alarm sets when all '0's occurs in the incoming data for at least 20 µs and clears if two consecutive frameworks are detected with no LOS condition between them.	R/W	'01'
8	RstClkLockEn	Allows automatic switching to selected transmit line (Blue) clock signal reference (TPCI/TCCI/TSCI) during Loss of Signal or Clock conditions. '0' = Disables automatic clock switch during RLOCK or LOS. '1' = Enables automatic clock switch during RLOCK or LOS.	R/W	'1'

Bit	Name	Description	Type	Default
7	RstAisLofEn	Allows automatic AIS generation from the RST section to the MST section because of a Loss of Frame condition: '0' = Disables AIS generation during LOF. '1' = Enables AIS generation during LOF. When in the system loopback mode (COCNF ((0cc)09H) bit [4]), an AIS will propagate out the system side also.	R/W	'0'
6	RstAisLosEn	Allows automatic AIS generation from the RST section to the MST section because of the internally generated Loss of Signal condition: '0' = Disables AIS generation during LOS. '1' = Enables AIS generation during LOS. (SDH) When in the system loopback mode (COCNF ((0cc)09H) bit [4]), an AIS will propagate out the system side also.	R/W	'0'
5	RstAisLockEn	Allows automatic AIS generation from the RST section to the MST section because of a Loss of Synchronization condition: '0' = Disables AIS generation during RLOCK. '1' = Enables AIS generation during RLOCK. When in the system loopback mode (COCNF ((0cc)09H) bit [4]), an AIS will propagate out the system side also.	R/W	'0'
4	RstAisFrc	Forces AIS generation from the RST section to the MST section via software: '0' = Disable. '1' = Enable. When in the system loopback mode (COCNF ((0cc)09H) bit [4]), an AIS will propagate out the system side also.	R/W	'0'
3	RstAisTimEn	Allows automatic AIS generation from the RST section to the MST section because of an active J0MsMtchSt. '0' = Disables AIS generation during active J0MsMtchSt. '1' = Enables AIS generation during active J0MsMtchSt. When in the system loopback mode (COCNF ((0cc)09H) bit [4]), an AIS will propagate out the system side also.	R/W	'0'
2:1	LockItg[1:0]	This field configures RLOCK alarm filtering: '0X' = No filtering. '10' = Weak RLOCK filtering. The RLOCK condition must be maintained for a total of 512 bits (OC-48/12) or 128 bits (OC-3/1) to be acknowledged. '11' = Strong RLOCK filtering. The RLOCK condition must be maintained for a total of 16384 bits (OC-48/12) or 4096 bits (OC-3/1) to be acknowledged.	R/W	'00'
0	CnfgFrmAcq	Modifies the frame acquisition algorithm as it relates to the NDF bits. Only relevant in STM-0/STS-1 (51.84 Mbit/s). Other framing modes and data rates, always use Normal Acquisition. '0' = Normal Acquisition. During acquisition, checks 2 consecutive frames for identical NDF and correct frameword. Desynchronization results from 4 consecutive incorrect frameworks. '1' = Robust Acquisition. During acquisition, checks 5 consecutive frames for identical NDF while also checking for 2 consecutive correct frameworks. Desynchronization results from 4 consecutive incorrect frameworks **OR** 8 consecutive frames not having identical NDF bits.	R/W	'0'

11.4.2 LOF_LMN—Out Of Frame and Loss of Frame L, M, and N Configuration ((1cc)81H)

This register sets the Loss Of Frame detection parameters.

Bit	Name	Description	Type	Default
15	RcvOofCnfg	This bit configures the number of consecutive erroneous framewords to detect before going to an Out Of Frame condition, after the frame has been synchronized. Also, see configuration bit RcvFwdOofCnfg, register R-RSTC: '0' = Requires **four** consecutive frames within 500 µs, having incorrect framewords to declare an OOF condition. '1' = Requires **five** consecutive frames within 500 µs, having incorrect framewords to declare an OOF condition. (SDH)	R/W	'0'
14:10	L[4:0]	After an OOF event is observed (indicated by OofSt = S_RG[0] = '1'), this represents the L parameter. L + 1 is the number of frames with OofSt = '1' needed to enter the LOF state (indicated by LofSt = (1cc)D8H[1] = '1').	R/W	00000
9:5	M[4:0]	After an OOF event is observed (indicated by OofSt = S_RG[0] = '1'), this represents the M parameter. M + 1 is the number of frames with OofSt = '0' needed to reenter the NORM state before entering the LOF state.	R/W	00000
4:0	N[4:0]	After an LOF event is observed (indicated by LofSt = S_RG[1] = '1'), this represents the N parameter. N + 1 is the number of frames with OofSt = '0' needed to reenter the NORM state from the LOF state (indicated by LofSt = S_RG[1] = '0').	R/W	00000

11.4.3 OOF_ECNT—Out Of Frame Event Counter ((1cc)82H)

This counter increments each time an OOF error event is detected. A write to the counter address((1cc)82H) causes the entire counter to be loaded into a buffer and then cleared. The contents of the buffer can then be read.

Bit	Name	Description	Type	Default
15:13	Unused		R	
12:0	OofCnt[12:0]	This field indicates the OOF error count value.	R	00H

11.4.4 B1_ERRCNT—B1 Error Counter ((1cc)83H)

This counter increments each time a B1 error event is detected. A write to the counter address ((1cc)83H) causes the entire counter to be loaded into a buffer and then cleared. The contents of the buffer can then be read.

Bit	Name	Description	Type	Default
15:0	B1Cnt[15:0]	This field indicates the B1 error count value.	R	00H

11.4.5 R_J0_ESTRA—J0 Receive Expected String Data Access ((1cc)85H)

The following registers (R_J0_ESTRA and R_J0_ASTRA) allow control and access of the expected and accepted Trace Identifier J0 string received in the incoming SOH. This is outlined below.

11.4.5.1 For the Expected Trace Identifier J0 String

11.4.5.1.1 Writing the Expected String Value

1. Initiate with a write to register (1cc)85H, ExpcJ0StrgWrite bit to '1', ExpcJ0StrgAddr[5:0] to the address (string pointer) of the byte which needs to be updated into the expected string RAM, and ExpcJ0StrgData[7:0] to the value of this byte. The write operation of the corresponding byte into the expected RAM is now initiated.
2. Read register (1cc)85H bit #15 (ExpcJ0StrgWrite). If ExpcJ0StrgWrite value is '1', then a write operation is still pending, and the microprocessor should wait before writing a new byte into this RAM. If ExpcJ0StrgWrite value is '0', then the write operation is complete and the microprocessor is allowed to write into the expected RAM. These two steps can be repeated, using different ExpcJ0StrgAddr[5:0] and ExpcJ0StrgData[7:0], until the entire 1-, 16-, 64-byte expected string is written into the RAM.

11.4.5.1.2 Reading the Expected String Value

1. Initiate with a write to register (1cc)85H, ExpcJ0StrgRead bit to '1' and ExpcJ0StrgAddr[5:0] to the address (string pointer) of the byte to be read from the expected string RAM. The read operation of the corresponding byte from the expected RAM is now initiated.
2. Read register (1cc)85H bit #14 (ExpcJ0StrgRead). If ExpcJ0StrgRead value is '1', then a read operation is still pending, and the microprocessor should initiate a new read to get the data byte value. If ExpcJ0StrgRead value is '0', then the read operation is complete and the microprocessor gets the corresponding data byte value on ExpcJ0StrgData[7:0] bits. These two steps can be repeated, using different ExpcJ0StrgAddr[5:0], until the entire 1-, 16-, 64-byte expected string is read from the RAM.

Bit	Name	Description	Type	Default
15	ExpcJ0StrgWrite	ExpcJ0StrgWrite is the Write Command operational bit for the expected J0 string internal RAM: When the microprocessor **writes** to this bit: '0' = No consequent action. '1' = Writes ExpcJ0StrgData[7:0] data byte into the expected string RAM at ExpcJ0StrgAddr[5:0] address location (string pointer). ExpcJ0StrgWrite bit clears automatically when this operation is complete. When the microprocessor **reads** this bit: '0' = The internal expected string RAM is ready for a new write operation. The previous write operation, if any, is complete. '1' = A write operation is pending; the internal expected string RAM is busy, and no new read/write operations to this RAM are allowed.	R/W	'0'

Bit	Name	Description	Type	Default
14	ExpcJ0StrgRead	ExpcJ0StrgRead is the Read Command operational bit for the expected J0 string internal RAM: When the microprocessor **writes** to this bit: '0' = No consequent action. '1' = Downloads ExpcJ0StrgData[7:0] data byte from the ExpcJ0StrgAddr[5:0] address location (string pointer) of the expected string RAM, into an internal register. ExpcJ0StrgRead bit clears automatically when this operation is complete. The microprocessor accesses this downloaded byte by reading the values at address (1cc)85H ExpcJ0StrgData[7:0], after reading that ExpcJ0StrgRead is '0'. When the microprocessor **reads** this bit: '0' = The internal expected string RAM is ready for a new read operation. The previous read operation, if any, is complete. '1' = A read operation is pending; the internal expected string RAM is busy, and no new read/write operations to this RAM are allowed.	R/W	'0'
13:8	ExpcJ0StrgAddr[5:0]	Bits [5:0] represent the string pointer value (RAM address)	R/W	000000
7:0	ExpcJ0StrgData[7:0]	Bits [7:0] represent the data value.	R/W	00H

11.4.6 R_J0_ASTRA—J0 Received Accepted String Data Access ((1cc)86H)

11.4.6.1 Reading the Accepted String Value

This operation is similar to the one described above for the expected string with access register R_J0_ESTRA.

11.4.6.1.1 Writing into the Accepted RAM from the Microprocessor

This operation is relevant only for testing and debugging purpose when the receive J0 string internal process is disabled.

Bit	Name	Description	Type	Default
15	TstJ0StrgWrite	**For testing purpose only:** TstJ0StrgWrite is the Write Command Test bit for the accepted J0 string internal RAM. It is only relevant when the J0 received trace processing is disabled (see register J0_RSTC, RcvJ0_Cnf[2:0] bits): When the microprocessor **writes** to this bit: '0' = No consequent action. '1' = Writes RcvJ0StrgData[7:0] data byte into the accepted string RAM at RcvJ0StrgAddr[5:0] address location (string pointer). TstJ0StrgWrite bit clears automatically when this operation is complete. When the microprocessor **reads** this bit: '0' = The internal expected string RAM is ready for a new write operation. The previous write operation, if any, is complete. '1' = A write operation is pending; the internal expected string RAM is busy, and no new read/write operations to this RAM are allowed.	R/W	'0'
14	RcvJ0StrgRead	RcvJ0StrgRead is the Read Command operational bit for the accepted J0 string internal RAM: When the microprocessor **writes** to this bit: '0' = No consequent action. '1' = Downloads RcvJ0StrgData[7:0] data byte from the RcvJ0StrgAddr[5:0] address location (string pointer) of the accepted string RAM, into an internal register. RcvJ0StrgRead bit clears automatically when this operation is complete. The microprocessor accesses this downloaded byte by reading the values at address (1cc)86H RcvJ0StrgData[7:0], after reading RcvJ0StrgRead as '0'. When the microprocessor **reads** this bit: '0' = The internal accepted string RAM is ready for a new read operation. The previous read operation, if any, is complete. '1' = A read operation is pending; the internal accepted string RAM is busy, and no new read/write operations to this RAM are allowed.	R/W	'0'
13:8	RcvJ0StrgAddr[5:0]	Bits [5:0] represent the string pointer value (RAM address).	R/W	000000
7:0	RcvJ0StrgData[7:0]	Bits [7:0] represent the data value of the received accepted Trace.	R/W	00H

11.4.7 J0_RSTC—J0 Received Trace Configuration ((1cc)87H)

Bit	Name	Description	Type	Default
15:6	Unused			
5	RsTimOnCRC7ErrDsb	This bit configures the setting of the Rs-Tim alarm i.e., J0MsMtchSt, when the CRC-7 is wrong: '1' = An active J0Crc7ErrSt alarm masks the J0MsMtchSt alarm (Rs-Tim), **if** (RsTimOnUnstableEn is low) **or** (RsTimOnUnstableEn is high **and** J0UnstableSt is low). '0' = J0MsMtchSt (Rs-Tim) alarm and J0CRC7ErrSt alarm are two independent processes.	R/W	'0'
4	RsTimOnUnstableEn	This bit configures the setting of the Rs-Tim alarm i.e., J0MsMtchSt, when the trace is unstable: '1' = An active J0UnstableSt alarm forces the J0MsMtchSt alarm (Rs-Tim) active. '0' = J0MsMtchSt (Rs-Tim) alarm and J0UnstableSt alarm are two independent processes.	R/W	'0'
3	RcvJ0_StableCnfg	This bit configures the number of consecutive identical received Section Traces needed for the J0UnstableSt (register S_RG bit #6) alarm to be cleared and for the received section trace to be declared stable and accepted: '1' = 5 consecutive identical messages. '0' = 3 consecutive identical messages.	R/W	'0'
2:0	RcvJ0_Cnf[2:0]	Configure J0 Receive Trace Identifier format: '111' = Trace Identifier is a framed 64-byte string with 2 special ASCII characters: linefeed and carriage return. '110' = Trace Identifier is a 64-byte string, free format. '10X' = Trace Identifier is a 16-byte string + CRC-7 (SDH). '01X' = Ignore J0 trace (no trace). '00X' = Trace Identifier is a 1-byte string. (SONET)	R/W	'010'

11.4.8 IS_RG—Receive Regenerator Section Interrupt Register ((1cc)D0H)

Each of these bits can cause the chip interrupt pin to become active if enabled via the bits in the Receive Interrupt Enable Register 1.

Bit	Name	Description	Type	Default
15:10	Reserved			
9	OofOvrFlw	This bit sets when the OOF_ECNT error counter rollover occurs. It clears when this register (IS_RG) is read.	R	'0'
8	B1OvrFlw	This bit sets when the B1_ERRCNT error counter rollover occurs. It clears when this register (IS_RG) is read.	R	'0'
7	Unused			
6	J0Unstable	This bit sets when there is a change in the J0UnstableSt bit (register S_RG[6]). It clears when this register (IS_RG) is read.	R	'0'
5	J0MsMtch	This bit sets when there is a change in the J0MsMtchSt bit (register S_RG[5]). It clears when this register (IS_RG) is read.	R	'0'
4	J0Crc7Err	This bit sets when there is a change in the J0Crc7ErrSt bit (register S_RG[4]). It clears when this register (IS_RG) is read.	R	'0'

Bit	Name	Description	Type	Default
3	Los	This bit sets when there is a change in the LosSt bit (register S_RG[3]). It clears when this register (IS_RG) is read	R	'0'
2	Lock	This bit sets when there is a change in the LockSt bit (register S_RG[2]). It clears when this register (IS_RG) is read.	R	'0'
1	Lof	This bit sets when there is a change in the LofSt bit (register S_RG[1]). It clears when this register (IS_RG) is read.	R	'0'
0	Oof	This bit sets when there is a change in the OofSt bit (register S_RG[0]). It clears when this register (IS_RG) is read.	R	'0'

11.4.9 IE_RG—Receive Regenerator Section Interrupt Enable ((1cc)D4H)

Bit	Name	Description	Type	Default
15:10	Unused			
9	OofOvrFlwEn	Active-high enable for the OofOvrFlw interrupt bit.	R/W	0
8	B1OvrFlwEn	Active-high enable for the B1OvrFlw interrupt bit.	R/W	0
7	Unused			
6	J0UnStableEn	Active-high enable for the J0Unstable interrupt bit.	R/W	0
5	J0MsMtchEn	Active-high enable for the J0MsMtch interrupt bit.	R/W	0
4	J0Crc7ErrEn	Active-high enable for the J0Crc7Err interrupt bit.	R/W	0
3	LosEn	Active-high enable for the LOS interrupt bit.	R/W	0
2	LockEn	Active-high enable for the Lock interrupt bit.	R/W	0
1	LofEn	Active-high enable for the LOF interrupt bit.	R/W	0
0	OofEn	Active-high enable for the OOF interrupt bit.	R/W	0

11.4.10 S_RG—Receive Regenerator Section Status ((1cc)D8H)

Bit	Name	Description	Type	Default
15:5	Unused			
6	J0UnStableSt	Present status of receive unstable/stable section trace detect (accepted trace when stable): '0' = Receive stable/accepted trace detected. '1' = Receive unstable trace.	R	'X'
5	J0MsMtchSt	Present status of comparison between received and expected J0 string (Trace Identifier Mismatch): '0' = OK comparison '1' = Bad comparison	R	'X'
4	J0Crc7ErrSt	Present status of comparison between received and calculated J0 string CRC-7 value (if 16-byte trace format): '0' = No CRC-7 error detected in the section trace '1' = CRC-7 error detected in the section trace	R	'X'

Bit	Name	Description	Type	Default
3	LosSt	Present status of the internal Loss of Signal (LOS) detect: '0' = No LOS '1' = LOS	R	'X'
2	LockSt	Present status of the external receive Loss of Clock Synchronization (RLOCK) input alarm: '0' = No RLOCK '1' = RLOCK	R	'X'
1	LofSt	Present status of Loss of Frame detect: '0' = No LOF '1' = LOF	R	'X'
0	OofSt	Present status of Out of Frame detect: '0' = No OOF '1' = OOF	R	'X'

11.5 SONET/SDH Receive Multiplexer Section Termination Channel Registers

11.5.1 R_MST_C—Receive MST Configuration ((1cc)90H)

Bit	Name	Description	Type	Default
15:14	Unused			
13	MstApsFiltCnfg	Configures the filtering of the receive K1 and K2 APS bytes (either a single APS channel or two independent channels): '1' = K1 and K2 APS bytes are filtered and updated together in register R_K2K1. If K1/K2 value is stable for 3 consecutive frames, K1 and K2 bits are updated in register R_K2K1. '0' = K1 and K2 APS bytes are independently filtered and updated in register R_K2K1. If K1 (resp. K2) value is stable for 3 consecutive frames, then K1 (resp K2) bits are updated in register R_K2K1.	R/W	'0'
12:11	Unused			
10	MstAisDetCnt	Configures the number of consecutive received K2 bytes that must have their RDI bits equal to or different from '111' for the MstAisSt alarm (register S_MUX bit[0]) to be updated: '1' = MstAisSt alarm sets when '111' is received in K2-RDI bits for 5 consecutive frames and clears if K2-RDI bits differ from '111' in 5 consecutive frames. '0' = MstAisSt alarm sets when '111' is received in K2-RDI bits for 3 consecutive frames, and clears if K2-RDI bits differ from '111' in 3 consecutive frames. (SDH)	R/W	'1'

Bit	Name	Description	Type	Default
9:8	MstRdiDetCnt[1:0]	Configures the number of consecutive received K2 bytes that must have their RDI bits equal to or different from '110' for the MstRdiSt alarm (register S_MUX bit[2]) to be updated: '11' = MstRdiSt alarm sets when '110' is received in K2-RDI bits for 16 consecutive frames, and clears if K2-RDI bits differ from '110' in 16 consecutive frames. '10' = MstRdiSt alarm sets when '110' is received in K2-RDI bits for 10 consecutive frames, and clears if K2-RDI bits differ from '110' in 10 consecutive frames. '01' = MstRdiSt alarm sets when '110' is received in K2-RDI bits for 5 consecutive frames, and clears if K2-RDI bits differ from '110' in 5 consecutive frames. (SDH) '00' = MstRdiSt alarm sets when '110' is received in K2-RDI bits for 3 consecutive frames, and clears if K2-RDI bits differ from '110' in 3 consecutive frames. (SDH)	R/W	'01'
7	AisOnExcB2En	Enables the insertion of AIS from the MST section to the MSA section and generation of SF when ExcB2ErrSt bit is set (register S_MUX[3]): '0' = Active ExcB2ErrSt does **not** cause AIS to be transmitted. '1' = Active ExcB2ErrSt causes AIS to be transmitted.	R/W	'1'
6	MstAisFrc	Forces AIS generation from the MST section to the MSA section via software: '0' = Disables. '1' = Enables.	R/W	'0'
5	MstAisEn	Controls automatic AIS generation from the MST section to the MSA section (see GenMstAisSt bit (global register S_AIS) for AIS generation logic): '0' = Disables. '1' = Enables. (SDH)	R/W	'0'
4	MstGenReiCnf	Configures generated REI (based on B2 BIP detected errors) to be inserted in M1 transmit Byte, as Block or BIP for STM-4c/STS-12c and STM-16c/STS-48c frame formats: '0' = Generated REI is coded as BIP Errors. '1' = Generated REI is coded as Block Errors.	R/W	'0'
3	MstRcvReiCnf	Configures interpretation of Receive REI (demultiplexed from M1 receive byte) as Block or BIP for STM-4c/STS-12c and STM-16c/STS-48c frame formats: '0' = Receive REI was coded as BIP Errors. '1' = Receive REI was coded as Block Errors (may be single or multiple blocks: see MstBlkErrCnfg bit).	R/W	'0'

Bit	Name	Description	Type	Default
2	MstRdiOnExcB2En	Enables the generation of MST RDI (to be inserted in transmit K2[2:0] = '110') during active ExcB2ErrSt (i0DH bit[3]): '0' = Active ExcB2ErrSt does **not** cause insertion. '1' = Active ExcB2ErrSt causes insertion.	R/W	'0'
1	MstRdiFrc	Forces Generation of MST RDI (to be inserted in transmit K2[2:0] = '110'): '0' = Disables forcing. '1' = Enables forcing.	R/W	'0'
0	MstBlkErrCnfg	Configures the block size of a concatenated frame for B2 detected errored blocks and REI generated errored block (see MstGenReiCnf bit): '1' = Multiple blocks per frame. The block size is 2430 bytes (equivalent to an STM-1). '0' = One single block per concatenated frame.	R/W	'0'

11.5.2 B2_BLKCNT—B2 Block Error Counter ((1cc)96H-(1cc)95H)

(1cc)96H = Bits[31:16], (1cc)95H = Bits[15:0], (16-bit access only).

This counter increments each time a B2 block error event is detected. A write to the MSByte of the counter (register (1cc)96H) causes the entire counter to be loaded into a buffer and then cleared. The contents of the buffer can then be read.

Bit	Name	Description	Type	Default
31:17	Unused			
16:0	B2BlkCnt[16:0]	B2 Block Error Count Value.	R	00H

11.5.3 B2_BIPCNT—B2 BIP Error Counter ((1cc)98H-(1cc)97H)

(1cc)98H = Bits[31:16], (1cc)97H = Bits[15:0], (16-bit access only).

This counter increments each time a B2 BIP error event is detected. A write to the MSByte of the counter (register (1cc)98H) causes the entire counter to be loaded into a buffer and then cleared. The contents of the buffer can then be read.

Bit	Name	Description	Type	Default
31:22	Unused			
21:0	B2BipCnt[21:0]	B2 BIP Error Count Value.	R	00H

11.5.4 MR_BLKCNT—MST REI Block Error Counter ((1cc)9AH-(1cc)99H)

(1cc)9AH = Bits[31:16], (1cc)99H = Bits[15:0], (16-bit access only).

This counter increments every frame in which the value of MST REI bits (M1[7:0]) is nonzero. A write to the MSByte of the counter (register (1cc)9AH) causes the entire counter to be loaded into a buffer and then cleared. The contents of the buffer can then be read.

Bit	Name	Description	Type	Default
31:17	Unused			
16:0	MstReiBlkCnt[16:0]		R	00H

11.5.5 MR_BIPCNT—MST REI BIP Error Counter ((1cc)9CH-(1cc)9BH)

(1cc)9CH = Bits[23:16], (1cc)9BH = Bits[15:0] (16-bit access only).

Every frame, the value of MST REI bits (M1[7:0]) is added to this counter. A write to the MSByte of the counter (register (1cc)9CH) causes the entire counter to be loaded into a buffer and then cleared. The contents of the buffer can then be read.

When operating in concatenated mode, the received M1 overhead values (in the third STS-1/STM-0) are accumulated in the specific port/channels M1 accumulation register—one MR_BIPCNT register per port/channel. For example, if you were using port/channel 0 then the MR_BIPCNT register to use would be at address 0x[0100b]9Ch~0x[0100b]9Bh or 0x49Ch~0x49Bh. If you were using port/channel 3 then you would use the MR_BIPCNT register at address 0x[0111b]9Ch~0x[0111b]9Bh or 0x79Ch~0x79Bh.

When operating in non-concatenated STS-3 and STS-12/STM-4 modes, the received M1 overhead values (in the third STS-1/STM-0) are accumulated in channel 2's MR_BIPCNT register (address 0x[0110b]9Ch~0x[0110b]9Bh or 0x69Ch~0x69Bh) only. Channel 0, 1 and 3's MR_BIPCNT registers would not be used. This applies when receiving 1xOC-3nc (which equates to three STS-1's and which can only use the line side port 0) or 1xOC-12nc (which equates to four STS-3c's and which can only use the line side port 0).

When operating in non-concatenated STS-48/STM-16 mode, the received M1 overhead values (in the third STS-1/STM-0) are accumulated in port/channel 0's M1 accumulation register. The MR_BIPCNT register to use would be at address 0x[0100b]9Ch~0x[0100b]9Bh or 0x49Ch~0x49Bh.

Bit	Name	Description	Type	Default
31:21	Unused			
20:0	MstReiBipCnt[20:0]		R	00H

11.5.6 R_K2K1—Received K1 and K2 Bytes/APS Channel ((1cc)9DH)

This register is the repository for filtered received K1 and K2 bytes. Depending on the setting of bit 13 in register R_MST_C, K1 and K2 are stored either independently as two 8-bit registers or together as one 16-bit register.

Bit	Name	Description	Type	Default
15:8	RcvK2[7:0]	When MstApsFiltCnfg (register R_MST_C, bit #13) is set to '0', these bits contain the value of the last 3 consecutively received K2 bytes having the same setting.	R	00H
7:0	RcvK1[7:0]	When MstApsFiltCnfg (register R_MST_C, bit #13) is set to '0', these bits contain the value of the last 3 consecutively received K1 bytes having the same setting.	R	00H
15:0	RcvK1K2_APS	When MstApsFiltCnfg (register R_MST_C, bit #13) is set to '1', these bits contain the value of the last 3 consecutively received K1/K2 APS channel bytes having the same setting	R	0000H

11.5.7 R_S1—Received S1 Byte ((1cc)9FH)

This register is the repository for filtered received S1 bytes.

Bit	Name	Description	Type	Default
15:8	Unused			
7:0	RcvS1[7:0]	Value of the last 3 consecutively received S1 bytes having the same setting.	R	00H

11.5.8 WINSZ_SB2—Window Size for Setting ExcB2ErrSt ((1cc)B0H)

Bit	Name	Description	Type	Default
15:11	Unused			
10:0	ExcB2SetWinSz[10:0]	Number of frames per window = 8*(ExcB2SetWinSz[10:0] + 1)	R/W	00H

11.5.9 CWIN_SB2—Consecutive Windows for Setting ExcB2ErrSt ((1cc)B1H)

Bit	Name	Description	Type	Default
15:7	Unused			
6:0	ExcB2SetWinNum[6:0]	Number of consecutive windows that must be excessively errored to set the ExcB2ErrSt bit (register S_MUX). **NOTE:** If ExcB2ErrSt is clear and this register is set to '0', ExcB2ErrSt will never be set.	R/W	00 0011

11.5.10 E#_EXCWIN_SB2—Number of Errs/Win for Excessively Errored Window ((1cc)B2H)

Bit	Name	Description	Type	Default
15:12	Unused			
11:0	ExcB2Min[11:0]	This value configures the minimum number of errors that a window must contain to be considered an excessively errored window. **NOTE:** Setting this value to '0' causes every window to be considered an excessively errored window.	R/W	2BH

11.5.11 WINSZ_CB2—Window Size for Clearing ExcB2ErrSt ((1cc)B3H)

Bit	Name	Description	Type	Default
15:11	Unused			
10:0	ExcB2ClrWinSz[10:0]	Number of frames per window = 8*(ExcB2ClrWinSz[10:0] + 1).	R/W	00H

11.5.12 CWIN_CB2—Consecutive Windows for Clearing ExcB2ErrSt ((1cc)B4H)

Bit	Name	Description	Type	Default
15:7	Unused			
6:0	ExcB2ClrWinNum[6:0]	Number of consecutive Non-Excessively Errored windows needed for the excessive error condition to be cleared. **NOTE:** If the ExcB2ErrSt bit (register S_MUX) is set and this register is set to '0', bit ExcB2ErrSt will never be cleared.	R/W	00 0011

11.5.13 E#_NEXCWIN_CB2—Number of Errs/Win for Non-Excessively Errored Window ((1cc)B5H)

Bit	Name	Description	Type	Default
15:12	Unused			
11:0	ExcB2Max[11:0]	This value configures the maximum number of errors that a window can contain and be considered a Non-Excessively Errored window. **NOTE:** Setting this value to '0' causes every window to be considered a non-excessively errored window	R/W	08H

11.5.14 WINSZ_SDEGB2—Window Size for Setting DegB2ErrSt ((1cc)B7H-(1cc)B6H)

(1cc)B7H = Bits[31:16], (1cc)B6H = Bits[15:0], (16-bit access only).

Bit	Name	Description	Type	Default
31:23	Unused			
22:0	DegB2SetWinSz[22:0]	Number of frames per window = 8*(DegB2SetWinSz[22:0] + 1)	R/W	00H

11.5.15 CWIN_SDEGB2—Consecutive Windows for Setting DegB2ErrSt ((1cc)B8H)

Bit	Name	Description	Type	Default
15:7	Unused			
6:0	DegB2SetWinNum[6:0]	Number of consecutive windows that must be error degraded (Degraded Signal Defect) to set the DegB2ErrSt bit (register S_MUX). **NOTE:** If DegB2ErrSt is clear and this register is set to '0', DegB2ErrSt will never be set.	R/W	00 0011

11.5.16 E#_DEGWIN_SB2—Number of Errs/Win for Error Degraded Window ((1cc)B9H)

Bit	Name	Description	Type	Default
15:12	Unused			
11:0	DegB2Min[11:0]	This value configures the minimum number of errors that a window must contain to be considered an error degraded window. **NOTE:** Setting this value to '0' causes every window to be considered an error degraded window.	R/W	2BH

11.5.17 WINSZ_CDEGB2—Window Size for Clearing DegB2ErrSt ((1cc)BBH-(1cc)BAH)

(1cc)BBH = Bits[31:16], (1cc)BAH = Bits[15:0], (16-bit access only).

Bit	Name	Description	Type	Default
31:23	Unused			
22:0	DegB2ClrWinSz[22:0]	Number of frames per window = 8*(DegB2ClrWinSz[22:0] + 1).	R/W	00H

11.5.18 CWIN_CDEGB2—Consecutive Windows for Clearing DegB2ErrSt ((1cc)BCH)

Bit	Name	Description	Type	Default
15:7	Unused			
6:0	DegB2ClrWinNum[6:0]	Number of consecutive non-degraded Error Rate windows needed for the Degraded error rate condition to be cleared. **NOTE:** If the DegB2ErrSt bit (register S_MUX) is set and this register is set to '0', bit DegB2ErrSt will never be cleared.	R/W	00 0011

11.5.19 E#_NDEGWIN_CB2—Number of Errs/Win for Non-Degraded Error Rate Window ((1cc)BDH)

Bit	Name	Description	Type	Default
15:12	Unused			
11:0	DegB2Max[11:0]	This value configures the maximum number of errors that a window can contain and be considered a NonDegraded Error Rate window. **NOTE:** Setting this value to '0' causes every window to be considered a non-degraded error rate window	R/W	08H

11.5.20 IS_MUX—Receive Multiplexer Section Interrupt Register ((1cc)D1H)

Each of these bits can cause the chip interrupt pin to become active if enabled in the Receive Interrupt Enable Register (IE_MUX).

Bit	Name	Description	Type	Default
15	Reserved			
14	RcvS1Chg	This bit sets when there is a change in the R_S1 register ((1cc)9FH). It clears when this register (IS_MUX) is read.	R	'0'
13	RcvK1Chg	This bit sets when there is a change in the R_K2K1 register ((1cc)9DH) register. It clears when this register (IS_MUX) is read.	R	'0'
12	RcvK2Chg	This bit sets when there is a change in the R_K2K1 register ((1cc)9DH) register. It clears when this register (IS_MUX) is read.	R	'0'
11	B2BitOvrFlw	This bit sets when a B2_BIPCNT error counter rollover occurs. It clears when this register (IS_MUX) is read.	R	'0'
10	B2BlkOvrFlw	This bit sets when a B2_BLKCNT error counter rollover occurs. It clears when this register (IS_MUX) is read.	R	'0'
9	MstReiBitOvrFlw	This bit sets when a MR_BIPCNT error counter rollover occurs. It clears when this register (IS_MUX) is read.	R	'0'
8	MstReiBlkOvrFlw	This bit sets when a MR_BLKCNT error counter rollover occurs. It clears when this register (IS_MUX) is read.	R	'0'

Bit	Name	Description	Type	Default
7	RcvS1Unstable	This bit sets when there is a change in the RcvS1UnstableSt bit (register S_MUX[7]). It clears when this register (IS_MUX) is read.	R	'0'
6	RcvK1Unstable	This bit sets when there is a change in the RcvK1UnstableSt bit (register S_MUX[6]). It clears when this register (IS_MUX) is read.	R	'0'
5	RcvK2Unstable	This bit sets when there is a change in the RcvK2UnstableSt bit (register S_MUX[5]). It clears when this register ((1cc)D1H) is read.	R	'0'
4	DegB2Err (MstSD)	This bit sets when there is a change in the DegB2ErrSt bit (register S_MUX[4]). It clears when this register ((1cc)D1H) is read	R	'0'
3	MstSF	This bit sets when there is a change in the MstSFSt bit (register S_MUX[3]). It clears when this register (IS_MUX) is read.	R	'0'
2	MstRdi	This bit sets when there is a change in the MstRdiSt bit (register S_MUX[2]). It clears when this register (IS_MUX) is read.	R	'0'
1	ExcB2Err	This bit sets when there is a change in the ExcB2ErrSt bit (register S_MUX[1]). It clears when this register (IS_MUX) is read.	R	'0'
0	MstAis	This bit sets when there is a change in the MstAisSt bit (register S_MUX[0]). It clears when this register (IS_MUX) is read.	R	'0'

11.5.21 IE_MUX—Receive Multiplexer Section Interrupt Enable ((1cc)D5H)

Bit	Name	Description	Type	Default
15	Unused			
14	RcvS1ChgEn	Active-high enable for the RcvS1Chg interrupt bit.	R/W	'0'
13	RcvK1ChgEn	Active-high enable for the RcvK1Chg interrupt bit.	R/W	'0'
12	RcvK2ChgEn	Active-high enable for the RcvK2Chg interrupt bit.	R/W	'0'
11	B2BitOvrFlwEn	Active-high enable for the B2BitOvrFlw interrupt bit.	R/W	'0'
10	B2BlkOvrFlwEn	Active-high enable for the B2BlkOvrFlw interrupt bit.	R/W	'0'
9	MstReiBitOvrFlwEn	Active-high enable for the MstReiBitOvrFlw interrupt bit.	R/W	'0'
8	MstReiBlkOvrFlwEn	Active-high enable for the MstReiBlkOvrFlw interrupt bit.	R/W	'0'
7	RcvS1UnstableEn	Active-high enable for the RcvS1Unstable interrupt bit.	R/W	'0'
6	RcvK1UnstableEn	Active-high enable for the RcvK1Unstable interrupt bit.	R/W	'0'
5	RcvK2UnstableEn	Active-high enable for the RcvK2Unstable interrupt bit.	R/W	'0'
4	DegB2ErrEn (SDEn)	Active-high enable for the DegB2Err interrupt bit (MstSD).	R/W	'0'
3	MstSFEn	Active-high enable for the MstSF interrupt bit.	R/W	'0'
2	MstRdiEn	Active-high enable for the MstRdi interrupt bit.	R/W	'0'
1	ExcB2ErrEn	Active-high enable for the ExcB2Err interrupt bit.	R/W	'0'
0	MstAisEn	Active-high enable for the MstAis interrupt bit	R/W	'0'

11.5.22 S_MUX—Receive Multiplexer Section Status ((1cc)D9H)

Bit	Name	Description	Type	Default
15:8	Unused			
7	RcvS1UnStableSt	Present status of receive unstable/stable S1 Synchronization Message detect.(accepted S1 when stable): '0' = Receive stable/accepted S1 byte detected. '1' = Receive unstable S1 byte.	R	'X'
6	RcvK1UnStableSt	Present status of receive unstable/stable K1 APS detect (accepted K1 when stable): '0' = Receive stable/accepted K1 byte detected. '1' = Receive unstable K1 byte.	R	'X'
5	RcvK2UnStableSt	Present status of receive unstable/stable K2 APS detect (accepted K2 when stable): '0' = Receive stable/accepted K2 byte detected. '1' = Receive unstable K2 byte.	R	'X'
4	DegB2ErrSt (MstSdSt)	This bit indicates the present status of the Degraded Signal Defect detection (Degraded BER detects): '0' = No Degraded Signal Defect (degraded BER). '1' = Degraded Signal Defect (degraded BER).	R	'X'
3	MstSfSt	This bit indicates the present status of the Signal Fail detection: '0' = No Signal Fail. '1' = Signal Fail ≡ MstAisSt **OR** (AisOnExcB2En **AND** ExcB2ErrSt).	R	'X'
2	MstRdiSt	Detection of '110' in RcvK2[2:0] bits (01H): '0' = No '110' detected. '1' = '110' detected.	R	'X'
1	ExcB2ErrSt	Present status of excessive BER detects: '0' = No excessive BER. '1' = Excessive BER.	R	'X'
0	MstAisSt	Detection of '111' in RcvK2[2:0] bits (01H): '0' = No '111' detect LOSed. '1' = '111' detected.	R	'X'

11.6 SONET/SDH Receive Multiplexer Section Adaptation Channel Registers

11.6.1 R_MSA_C—Receive MSA Configuration ((1cc)A0H)

Bit		Description	Type	Default
15:10	Unused			
9	DauaiscEn	If the receive concatenation indicator bytes are processed, DauaiscEn enables AuAisc detection. This means that an AuAis defect may be asserted only when both the pointer interpreter and concatenation verification state machines are in the AIS state—both receive pointer and configured pointer identification H1/H2 are all '1's: '1' = Enables AuAisc detection. '0' = Disables AuAisc detection.	R/W	'0'
8	LopcOnSvDefEn	If the receive concatenation indicator bytes are processed, LopcOnSvDfEn enables forcing a server Defect alarm (into the HptRdi) because of a concatenation identification verification defect (LopcSt: concatenated code not detected): '1' = Enables HP-RDI generation during LOPC. '0' = Disables HP-RDI generation during LOPC.	R/W	'0'
7	LopcOnMsaAisEn	If the receive concatenation indicator bytes are processed, LopcOnMsaAisEn enables automatic AIS insertion (DMSAAIS) based on the concatenation identification verification defect (LopcSt: concatenated code not detected): '1' = Enables AIS generation during LOPC. '0' = Disables AIS generation during LOPC.	R/W	'0'
6	RcvConcPtDetCnfg	Configures the detection of concatenation indication in all or some of the receive H1/H2 pairs not carrying the pointer value. The detection algorithm follows the configured frame and payload structure according to ITU-T rec. G.783 Annex C.2. The Loss Of Pointer Concatenation defect (LOPC alarm) is accessible via register IS_ADP. The AISC defect (detection of all '1's) is also processed on the configured concatenation indicator receive bytes, when enabled via DauaiscEn bit. '0' = Verify concatenated pointer and AU-AISC identification on all the H1/H2 pairs (except the ones carrying the pointer value). '1' = Verify concatenated pointer and AU-AISC identification on some H1/H2 pairs (per STM-1 equivalent): • AU-4: no concatenation indicators are considered. • AU-4-4c: only the 2nd, 3rd and 4th H1/H2 pairs are considered as the concatenation indicators. • AU-4-16c: only H1/H2 pairs from #2 to #16 are considered as the concatenation indicators.	R/W	'0'

Bit		Description	Type	Default
5	AuPntrJustCnfg	Configures the justification rule (pointer increments/ decrements): '1' = SONET Objective: When 8 of the 10 pointer bits are detected with the I bits inverted and not the D bits, Au pointer increments. If instead, the D bits are inverted and not the I bits, it decrements. '0' = SDH Objective: When 3 of the 5 pointer bits are detected with the I bits inverted and not the D bits, Au pointer increments. If instead, the D bits are inverted and not the I bits, it decrements.	R/W	'0'
4:3	ExpcAuPntrSS[1:0]	Bits [1:0] represent the expected value of the receive Au Pointer SS two bits when AuPntrSSEn is enabled. For SDH, set this to '10' which is the expected value of the receive Au Pointer SS two bits when AuPntrSSEn is enabled.	R/W	'00'
2	RcvMsaAisEn	Controls automatic AIS generation from the MSA section to the HPT section (see GenMsaAisSt bit (005H bit[5]) for AIS generation logic): '0' = Disables '1' = Enables (SDH)	R/W	'0'
1	RcvMsaAisFrc	Forces AIS generation from the MSA section to the HPT section via software: '0' = Normal operation. '1' = Forces AIS.	R/W	'0'
0	AuPntrSSEn	Enables consideration of AU pointer SS bits during pointer processing. If enabled, the SS bits must be set to the expected value ExpcAuPntrSS[1:0] or a LOP ((1cc)D2H[2]) alarm is generated. (SDH) '0' = Disables '1' = Enables	R/W	'0'

11.6.2 R_AU_NCNT—Receive Negative AU Pointer Justification Event Counter ((1cc)A1H)

This counter increments each time a positive pointer justification, on the receive side, is detected in the H1: H2 bytes of the administrative unit payload. A write to the counter (register (1cc)A1H) causes the entire counter to be loaded into a buffer and then cleared. The contents of the buffer can then be read.

Bit	Name	Description	Type	Default
15:11	Unused			
10:0	RcvAUNegCnt[10:0]	Bits [10:0] represent the count value.	R	00H

11.6.3 R_AU_PCNT—Receive Positive AU Pointer Justification Event Counter ((1cc)A2H)

This counter increments each time a positive pointer justification, on the receive side, is detected in the H1:H2 bytes of the administrative unit payload. A write to the counter (register (1cc)A2H) causes the entire counter to be loaded into a buffer and then cleared. The contents of the buffer can then be read.

Bit	Name	Description	Type	Default
15:11	Unused			
10:0	RcvAUPosCnt[10:0]	Bits [10:0] represent the count value.	R	00H

11.6.4 IS_ADP—Receive Section Adaptation Interrupt Register ((1cc)D2H)

Each of these bits can cause the interrupt pin to become active if enabled via the Receive Interrupt Enable Register 3.

Bit	Name	Description	Type	Default
15:6	Unused			
5	Lopc	This bit sets when there is a change in the LopcSt bit (register S_ADP[5]). It clears when this register (IS_ADP) is read.	R	'0'
4	RcvAuNegOvrFlw	This bit sets when a R_AU_NgNt error counter rollover occurs. It clears when this register (IS_ADP) is read.	R	'0'
3	RcvAuPosOvrFlw	This bit sets when a R_AU_PcNt error counter rollover occurs. It clears when this register (IS_ADP) is read.	R	'0'
2	Lop	This bit sets when there is a change in the LopSt bit (register S_ADP[2]). It clears when this register (IS_ADP) is read.	R	'0'
1	NewDataFlg	This bit sets when there is a change in the NewDataFlgSt bit (register S_ADP[1]). It clears when this register (IS_ADP) is read.	R	'0'
0	AuAis	This bit sets when there is a change in the AuAisSt bit (register S_ADP[0]). It clears when this register (IS_ADP) is read.	R	'0'

11.6.5 IE_ADP—Receive Section Adaptation Interrupt Enable ((1cc)D6H)

Bit	Name	Description	Type	Default
15:6	Unused			
5	LopcEn	Active-high enable for the Lopc interrupt bit.	R/W	'0'
4	RcvAuNegOvrFlwEn	Active-high enable for the RcvAuNegOvrFlw interrupt bit.	R/W	'0'
3	RcvAuPosOvrFlwEn	Active-high enable for the RcvAuPosOvrFlw interrupt bit.	R/W	'0'
2	LopEn	Active-high enable for the Lop interrupt bit.	R/W	'0'
1	NewDataFlgEn	Active-high enable for the NewDataFlg interrupt bit.	R/W	'0'
0	AuAisEn	Active-high enable for the AuAis interrupt bit.	R/W	'0'

11.6.6 S_ADP—Receive Section Adaptation Status ((1cc)DAH)

Bit	Name	Description	Type	Default
15:6	Unused			
5	LopcSt	Present status of Loss of Pointer Concatenation indication detects: '0' = No LOPC detected. '1' = LOPC detected ≡ Any of the H1/H2 pairs, so configured, (see RcvConcPtDetCnfg) having an invalid concatenation indicator value: ≠ ('1001' **and** ExpcAuPntrSS[1:0] (if enabled) **and** '1111111111') **or** ≠ FFFFH.	R	'X'
4:3	Unused		R	'X'
2	LopSt	Present status of Loss of Pointer detects: '0' = No LOP detected. '1' = LOP detected ≡ Invalid pointer value **OR** (SS bits ≠ ExpcAuPntrSS[1:0] **AND** AuPntrSSEn.)	R	'X'
1	NewDataFlgSt	Present status of New Data Flag: '0' = NDF value is '0'. '1' = NDF value is '1'.	R	'X'
0	AuAisSt	Present status of Pointer processing AIS detects: '0' = No AIS detected. '1' = AIS detected ≡ H1:H2 bytes (AU pointer) = '11111111 11111111'	R	'X'

11.7 SONET/SDH Receive High-Order Path Termination Channel Registers

11.7.1 R_HPT_C1—Receive HPT Configuration 1 Register ((1cc)A4H)

Bit	Name	Description	Type	Default
15:14	HptRdiDetCnt[1:0]	These bits configure the number of received G1 bytes that must have the same value in the RDI bit(s) for the HptRdiSt bit(s)/alarm (register R_HPT_RDI bit[3:1]) to be updated. The received G1 RDI bits + spare can be retrieved via register R_HPT_RDI bit[3:0]. Note that if received RDI is not enhanced (see RcvHptRdiDetEnh), only bit #3 of G1 is considered in the algorithm: '11' = 16 received G1 bytes '10' = 10 received G1 bytes (SDH) '01' = 5 received G1 bytes (SDH) '00' = 3 received G1 bytes (SDH)	R/W	'01'
13	HptRdiDetEnhCnfg	Configures the detection of received HPT RDI (considered enhanced or not): '0' = Non-enhanced Received G1 RDI bits. '1' = Enhanced Received G1 RDI bits.	R/W	'1'
12	C2MsMtchCnt	Configures the number of mismatches, between the RcvC2 byte (register R_C2) and the ExpcC2 byte ((1cc)A6H), needed for the HptSlmSt bit (register S_HPT bit[12]) to be updated (SDH): '0' = 3 mismatches. '1' = 5 mismatches.	R/W	'0'
11	HpSlmOnC2UnstableEn	This bit configures the setting of the Hp-Slm alarm i.e., HptSlmSt, when the receive C2 Signal Label is unstable: '1' = Active C2UnstableSt alarm forces the HptSlmSt alarm (Hp-Slm). '0' = HptSlmSt (Signal Label Mismatch) alarm and C2UnstableSt alarm are two independent processes.	R/W	'0'
10	B3CntrCnfg	Configures whether the B3 error counter updates using bit errors or block errors: '0' = Bit errors. '1' = Block errors.	R/W	'0'
9	HptReiCntrCnfg	Configures whether the HPT REI error counter (register HPTREI_CNT) updates using bit errors or block errors: '0' = Bit errors. '1' = Block errors.	R/W	'0'
8	RcvStuffCnfg	In STS-1/STM-0 mode, this bit configures whether the two fixed stuff columns (#30 and #59) are part of the payload: '1' = Columns #30 and #59 of the SPE are **not** part of the payload and considered as stuff columns. '0' = Columns #30 and #59 of the SPE are part of the payload and their contents are part of the B3 BIP calculation.	R/W	'0'
7	HptRdiOnLcdEn	Enables the insertion of HPT RDI on active AtmLcdSt (H[bit]) alarm (ATM Loss Of Cell Delineation): '0' = Active AtmlcdSt alarm does **not** cause insertion of RDI bits into the transmitted G1 byte. '1' = Active AtmlcdSt alarm causes insertion of RDI bits into the transmitted G1 byte (payload defect).	R/W	'1'

Bit	Name	Description	Type	Default
6:5	HptRdiOnSlmEn[1:0]	Enables and configures the insertion of HPT RDI on active HptSlmSt (i63H bit[12]) alarm: '0X' = Active HptSlmSt alarm does **not** cause insertion of RDI bits into the transmitted G1 byte. '10' = Active HptSlmSt alarm causes insertion of RDI bits into the transmitted G1 byte as a connectivity defect. '11' = Active HptSlmSt alarm causes insertion of RDI bits into the transmitted G1 byte as a payload defect.	R/W	'11'
4	HptRdiOnTimEn	Enables the insertion of HPT RDI on active HptTimSt (i63H bit[15]) alarm: '0' = Active J1MsMtchSt (TIM) alarm does **not** cause insertion of RDI bits into the transmitted G1 byte. '1' = Active J1MsMtchSt (TIM) alarm causes insertion of RDI bits into the transmitted G1 byte (connectivity defect).	R/W	'1'
3	HptRdiOnUnEqpEn	Enables the insertion of HPT RDI on active HptUnEqpSt (i63H bit[13]) alarm: '0' = Active HptUnEqpSt alarm does **not** cause update of transmitted G1 RDI bits '1' = Active HptUnEqpSt alarm causes update of transmitted G1 RDI bits (connectivity defect).	R/W	'1'
2:1	HptRdiGenEnhCnfg[1:0]	Configures the generation of HPT RDI (enhanced or not) at both the RPAL bus output and the internal feedback value to the transmitter: '00' = Non-enhanced generated G1 RDI bit. (RDI = '100'—no RDI = '000'). '01' = Non-enhanced generated G1 RDI bit. (RDI = '111'—no RDI = '011'). (SDH) '1X' = Enhanced generated G1 RDI bit (refer to Table 15 for the Enhanced RDI bit coding). (SDH)	R/W	'10'
0	G1SpOnRpalCnfg	Sets the value of G1 Spare Bit (G1[0]) at the RPAL output (Serial Receive Path Alarm Port): '0' = Value is set to '0'. (SDH) '1' = Value is set to '1'.	R/W	'0'

11.7.2 R_HPT_C2—Receive HPT Configuration 2 Register ((1cc)A5H)

Bit	Name	Description	Type	Default
15:14	Unused			
13	HpTimOnCRC7ErrDsb	This bit configures the setting of the Hp-Tim alarm i.e., J1MsMtchSt, when the CRC-7 is wrong: '1' = An active J1Crc7ErrSt alarm masks the J1MsMtchSt alarm (Hp-Tim), **if** (HpTimOnUnstableEn is low) **or** (HpTimOnUnstableEn is high **and** J1UnstableSt is low). '0' = J1MsMtchSt (Hp-Tim) alarm and J1CRC7ErrSt alarm are two independent processes.	R/W	'0'
12	HpTimOnUnstableEn	This bit configures the setting of the Hp-Tim alarm i.e., J1MsMtchSt, when the trace is unstable: '1' = An active J1UnstableSt alarm forces the J1MsMtchSt alarm (Hp-Tim). '0' = J1MsMtchSt (Hp-Tim) alarm and J1UnstableSt alarm are two independent processes.	R/W	'0'

Bit	Name	Description	Type	Default
11	RcvJ1_StableCnfg	This bit configures the number of consecutive identical received Section Traces needed for the J1UnstableSt (register S_RG bit #6) alarm to be cleared and for the received path trace to be declared stable and accepted: '1' = 5 consecutive identical messages. '0' = 3 consecutive identical messages.	R/W	'0'
10:8	RcvJ1_Cnf[2:0]	Configure J1 Receive Path Trace Identifier format: '111' = Trace Identifier is a framed 64-byte string with 2 special ASCII characters: line feed and carriage return. '110' = Trace Identifier is a 64-byte string, free format. (SDH) '10X' = Trace Identifier is a 16-byte string + CRC-7 (SDH). '01X' = Ignore J1 trace (no trace). '00X' = Trace Identifiers a 1-byte string.	R/W	'010'
7:6	Unused			
5	RcvHptAisFrc	Force AIS generation from the HPT section to the HPA section via software '0' = Normal Operation '1' = Force	R/W	'0'
4	RcvHptAisSlmEnbl	Controls automatic AIS insertion from the HPT section to the HPA section (See GenHptAisSt bit register S_AIS for AIS generation logic) because of HptSlmSt alarm (Path Signal Label Mismatch alarm detection status: receive C2 different from expected): '0' = Disables AIS generation during dSLM. '1' = Enables AIS generation during dSLM. (SDH)	R/W	'0'
3	RcvHptAisUneqEnbl	Controls automatic AIS insertion from the HPT section to the HPA section because of HptUnEqpSt alarm (Unequipped alarm detection status: C2 = all '0's) '0' = Disables AIS generation during dUneq. '1' = Enables AIS generation during dUneq. (SDH)	R/W	'0'
2	RcvHptAisTimEnbl	Controls automatic AIS insertion from the HPT section to the HPA section because of J1MsmtchSt alarm (J1 Trace Identifier Mismatch detection status): '0' = Disables AIS generation during dTIM. '1' = Enables AIS generation during dTIM. (SDH)	R/W	'0'
1:0	Unused			

11.7.3 EXP_C2—Expected C2 Byte Register ((1cc)A6H)

The contents of this register are the expected value of the received signal label (C2) byte.

Bit	Name	Description	Type	Default
15:8	Unused			
7:0	ExpcC2[7:0]	Bits [7:0] correspond to ExpcC2[7:0], respectively.	R/W	01H

11.7.4 R_C2—Received C2 Byte Register ((1cc)A7H)

The contents of this register are the received signal label (C2) byte.

Bit	Name	Description	Type	Default
15:8	Unused			
7:0	RcvC2[7:0]	Bits [7:0] correspond to RcvC2[7:0], respectively.	R	XXH

11.7.5 R_HPT_RDI—Received HPT RDI Bits Register ((1cc)A8H)

The contents of this register are the received RDI (G1[3:1]) and spare bits (G1 bit[0]) from the received G1 byte.

Bit	Name	Description	Type	Default
15:4	Unused			
3:1	HptRcvRdi[2:0]	Bits [3:1] correspond to G1[3:1], respectively.	R	'X'
0	HptRcvSpBit	G1 bit[0]	R	'X'

11.7.6 B3_ECNT—B3 Error Event Counter ((1cc)A9H)

This counter is configured via B3CntrCnfg (register R_HPT_C1) to count B3 error events. A write to the counter (register (1cc)A9H) causes the entire counter to be loaded into a buffer and then cleared. The contents of the buffer can then be read.

Bit	Name	Description	Type	Default
15:0	B3Cnt[15:0]	Bits [15:0] correspond to B3CNT[15:0], respectively.	R	0000H

11.7.7 HPTREI_CNT—HPT REI Counter ((1cc)AAH)

If counting HPT REI bit errors (HptReiCntrCnfg, register R_HPT_C1 bit[9] = '0'), each frame's HPT REI bits (G1[7:4]) are added to this counter. If counting HPT REI block errors (HptReiCntrCnfg, register R_HPT_C1 bit[9] = '1'), for each frame in which the value of the REI bits is nonzero, this counter is incremented. A write to the counter (register (1cc)AAH) causes the entire counter to be loaded into a buffer and then cleared. The contents of the buffer can then be read.

Bit	Name	Description	Type	Default
15:0	HptReiCnt[15:0]	Bits [15:0] correspond to HptReiCnt[15:0], respectively.	R	0000H

11.7.8 R_J1_ASTRA—J1 Received Accepted String Data Access ((1cc)ADH)

This register allows microprocessor access to the accepted J1 string (trace identifier) received in incoming HPOH. See the R_J0_ASTRA register description for the configuration procedure

Bit	Name	Description	Type	Default
15	TstJ1StrgWrite	**For testing purpose only:** TstJ1StrgWrite is the Write Command Test bit for the accepted J1 string internal RAM; it is only relevant when the J1 received trace processing is disabled (see register R_HPT_C2, RcvJ1_Cnf[2:0] bits): When the microprocessor **writes** to this bit: '0' = No consequent action. '1' = Writes RcvJ1StrgData[7:0] data byte into the accepted string RAM at RcvJ1StrgAddr[5:0] address location (string pointer). TstJ1StrgWrite bit clears automatically when this operation is complete. When the microprocessor **reads** this bit: '0' = The internal expected string RAM is ready for a new write operation. The previous write operation, if any, has been completed. '1' = A write operation is pending; the internal expected string RAM is busy, and no new read or write operation to this RAM is allowed.	R/W	'0'
14	RcvJ1StrgRead	RcvJ1StrgRead is the Read Command operational bit for the accepted J1 string internal RAM: When the microprocessor **writes** to this bit: '0' = No consequent action. '1' = Downloads RcvJ1StrgData[7:0] data byte from the RcvJ1StrgAddr[5:0] address location (string pointer) of the accepted string RAM, into an internal register. RcvJ1StrgRead bit clears automatically when this operation is complete. The microprocessor accesses the downloaded byte-value of the receive accepted trace by performing a read at address (1cc)ADH (RcvJ1StrgData[7:0] value) and reading RcvJ1StrgRead as '0'. When the microprocessor **reads** this bit: '0' = The internal accepted string RAM is ready for a new read operation. The previous read operation, if any, has been completed. '1' = A read operation is pending; the internal accepted string RAM is busy, and no new read or write operation to this RAM is allowed.	R/W	'0'
13:8	RcvJ1StrgAddr[5:0]	Bits [5:0] represents the string pointer value (RAM address)	R/W	000000
7:0	RcvJ1StrgData[7:0]	Bits [7:0] correspond to Data[7:0], respectively.	R/W	00H

11.7.9 R_J1_ESTRA—J1 Receive Expected String Data Access ((1cc)AFH)

This register allows configuring the expected J1 string (trace identifier) received in incoming HPOH. See the R_J0_ESTRA ((1cc)85H) register description for the configuration procedure.

Bit	Name	Description	Type	Default
15	ExpcJ1StrgWrite	ExpcJ1StrgWrite is the Write Command operational bit for the expected J1 string internal RAM: When the microprocessor **writes** to this bit: '0' = No consequent action. '1' = Writes ExpcJ1StrgData[7:0] data byte into the expected string RAM at ExpcJ1StrgAddr[5:0] address location (string pointer). ExpcJ1StrgWrite bit clears automatically when this operation is complete. When the microprocessor **reads** this bit: '0' = The internal expected string RAM is ready for a new write operation. The previous write operation, if any, has been completed. '1' = A write operation is pending; the internal expected string RAM is busy, and no new read or write operation to this RAM is allowed.	R/W	'0'
14	ExpcJ1StrgRead	ExpcJ1StrgRead is the Read Command operational bit for the expected J1 string internal RAM: When the microprocessor **writes** to this bit: '0' = No consequent action. '1' = Downloads ExpcJ1StrgData[7:0] data byte from the ExpcJ1StrgAddr[5:0] address location (string pointer) of the expected string RAM, into an internal register. ExpcJ1StrgRead bit clears automatically when this operation is complete. The microprocessor accesses the downloaded value by performing a read at address (1cc)AFH (ExpcJ1StrgData[7:0] value) and reading ExpcJ1StrgRead as '0'. When the microprocessor **reads** this bit: '0' = The internal expected string RAM is ready for a new read operation. The previous read operation, if any, has been completed. '1' = A read operation is pending; the internal expected string RAM is busy and no new read or write operation to this RAM is allowed.	R/W	'0'
13:8	ExpcJ1StrgAddr[5:0]	Bits [5:0] represents the string pointer value (RAM address).	R/W	000000
7:0	ExpcJ1StrgData[7:0]	Bits [7:0] correspond to Data[7:0], respectively.	R/W	00H

11.7.10 IS_HPT—Receive Path (HPT) Interrupt Register ((1cc)D3H)

Each of these bits can cause the chip's interrupt pin to become active if enabled via the bits in the Receive Interrupt Enable Register 3.

Bit	Name	Description	Type	Default
15:12	Unused			
11	HptRdi	This bit sets when the register R_HPT_RDI[3:1] bits (filtered received G1 RDI bits) change (see HptRdiDetCnt = register R_HPT_C1). It clears when register R_HPT_RDI is read.	R	'0'
10	RcvC2Chg	This bit sets when there is a change in the R_C2 register. It clears when that register is read.	R	'0'
9	HptReiOvrFlw	This bit sets when the value in the HPTREI_CNT counter rolls over. It clears when this register, IS_HPT, is read.	R	'0'
8	B3OvrFlw	This bit sets when the value in the B3_ECNT counter rolls over. It clears when this register, IS_HPT, is read.	R	'0'
7	C2Unstable	This bit sets when there is a change in the C2UnstableSt bit (register S_HPT[6]). It clears when this register, IS_HPT, is read.	R	'0'
6	J1allzero	This bit sets when there is a change in the J1allzeroSt bit (register S_HPT[6]). It clears when this register, IS_HPT, is read.	R	'0'
5	J1Unstable	This bit sets when there is a change in the J1UnstableSt bit (register S_HPT[5]). It clears when this register, IS_HPT, is read.	R	'0'
4	J1MsMtch	This bit sets when there is a change in the J1MsMtchSt bit (register S_HPT[4]). It clears when this register, IS_HPT, is read.	R	'0'
3	J1Crc7Err	This bit sets when there is a change in the J1Crc7St bit (register S_HPT[3]). It clears when this register, IS_HPT, is read.	R	'0'
2	HptUnEqp	This bit sets when there is a change in the HptUneqSt bit (register S_HPT[2]). It clears when this register, IS_HPT, is read.	R	'0'
1	HptSlm	This bit sets when there is a change in the HptSlmSt bit (register S_HPT[1]). It clears when this register, IS_HPT, is read.	R	'0'
0	VcAis	This bit sets when there is a change in the VcAisSt bit (register S_HPT[0]). It clears when this register, IS_HPT, is read.	R	'0'

11.7.11 IE_HPT—Receive Path (HPT) Interrupt Enable ((1cc)D7H)

Bit	Name	Description	Type	Default
15:12	Unused			
11	HptRdiEn	Active-high enable for the HptRdi interrupt bit.	R/W	'0'
10	RcvC2ChgEn	Active-high enable for the RcvC2Chg interrupt bit.	R/W	'0'
9	HptReiOvrFlwEn	Active-high enable for the HptReiOvrFlw interrupt bit.	R/W	'0'
8	B3OvrFlwEn	Active-high enable for the B3OvrFlw interrupt bit.	R/W	'0'
7	C2UnstableEn	Active-high enable for the C2Unstable interrupt bit.	R/W	'0'
6	J1allzeroEn	Active-high enable for the J1allzero interrupt bit.	R/W	'0'
5	J1UnstableEn	Active-high enable for the J1Unstable interrupt bit.	R/W	'0'
4	J1MsMtchEn	Active-high enable for the J1MsMtch interrupt bit.	R/W	'0'

Bit	Name	Description	Type	Default
3	J1Crc7ErrEn	Active-high enable for the J1Crc7Err interrupt bit.	R/W	'0'
2	HptUnEqpEn	Active-high enable for the HptUnEqp interrupt bit.	R/W	'0'
1	HptSlmEn	Active-high enable for the HptSlm interrupt bit.	R/W	'0'
0	VcAisEn	Active-high enable for the VcAis interrupt bit.	R/W	'0'

11.7.12 S_HPT—Receive Path (HPT) Status ((1cc)DBH)

Bit	Name	Description	Type	Default
15:8	Unused			
7	C2UnStableSt	Present status of receive unstable/stable path signal label detect: '0' = Receive stable/accepted signal label detected. '1' = Receive unstable signal label.	R	'X'
6	J1allzeroSt	Present status of the detection of an all '0's receive stable path trace (accepted trace = all '0's): '0' = Receive trace is either not stable or not all '0's (if stable). '1' = Receive stable trace is all '0's.	R	'X'
5	J1UnStableSt	Present status of receive unstable/stable path trace detect (accepted trace when stable): '0' = Receive stable/accepted trace detected. '1' = Receive unstable trace.	R	'X'
4	J1MsMtchSt	Present status of comparison between received and expected J1 string: '0' = Comparison matches. '1' = Comparison does not match.	R	'X'
3	J1Crc7ErrSt	Present status of comparison between received and calculated J1 string CRC-7 value (16-byte string format only): '0' = No detection of a CRC-7 error. '1' = Detected a CRC-7 error in the receive trace.	R	'X'
2	HptUnEqpSt:	Present status of unequipped status detects: '0' = Equipped. '1' = Unequipped ≡ RcvC2 = '00000000'	R	'X'
1	HptSlmSt	Present status of Signal Label Mismatch detection: '0' = No mismatch '1' = Mismatch ≡ (RcvC2 ≠ ExpC2) **AND** (RcvC2 ≠ 00H) **AND** (RcvC2 ≠ 01H)	R	'X'
0	VcAisSt	Present status of VC AIS detect: '0' = No AIS '1' = AIS ≡ RcvC2 (signal label) = '11111111'	R	'X'

11.8 SONET/SDH Transmit Regenerator and Multiplexer Section Termination Channel Registers

11.8.1 T_RMST_OP—Transmit RMST Operational Register ((1cc)E0H)

Bit	Name	Description	Type	Default
15	XmtScrmblCnfg	This bit indicates the transmit scrambler operation: '0' = Disable transmit scrambler. '1' = Enable transmit scrambler 2e7.	R/W	'1'
14	Unused			
13:12	XmtTZ0_Cnfg	Value for Z0 #31 to #47 (STS-48c/STM-16c) transmit. Value for Z0 #8, 9, 10 and 11 (STS-12c/STM-4c) transmit. Value for Z0 #2 (STS-3c) or NU1_8 (STM-1). '00' = Sets value to all '0's. (SONET) '01' = Sets value to 0xAAH. Some SerDes might not accept a large number of sequential 0s (generating false Loss of SIgnal or no link indications); this setting will insert a transitioning pattern of 1010 into the unused and unscrambled Z0 bytes and prevent these false indications. (SDH) '10' = (SDH) For OC-48c: Z0 #n = n + 1. For OC-12c: Z0 #8 = 09H, Z0 #9 = 0AH, Z0 #10 = 0BH, and Z0 #11 = 0CH. For OC-3c: Z0 #2 = 03H. 11 = Reserved.	R/W	'00'
11:10	XmtSZ0_Cnfg	Value for Z0 #16 to #31 (STS-48c/STM-16c) transmit. Value for Z0 #4, 5, 6, and 7 (STS-12c/STM-4c) transmit. Value for Z0 #1 (STS-3c) or NU1_8 (STM-1). '00' = Sets value to all '0's. (SONET) '01' = Sets value to 0xAAH. Some SerDes might not accept a large number of sequential 0s (generating false Loss of SIgnal or no link indications); this setting will insert a transitioning pattern of 1010 into the unused and unscrambled Z0 bytes and prevent these false indications. (SDH) '10' = (SDH) For OC-48c: Z0 #n = n + 1. For OC-12c: Z0 #4 = 05H, Z0 #5 = 06H, Z0 #6 = 07H, and Z0 #7 = 08H. For OC-3c: Z0 #'1' = 02H. '11' = Reserved.	R/W	'00'

Bit	Name	Description	Type	Default
9:8	XmtFZ0_Cnfg	Value for Z0 #1 to #15 (STS-48c/STM-16c) transmit. Value for Z0 #1, 2 and 3 (STS-12c/STM-4c) transmit. '00' = Sets value to all '0's - SONET/SDH standard. '01' = Sets value to 0xAAH. Some SerDes might not accept a large number of sequential 0s (generating false Loss of SIgnal or no link indications); this setting will insert a transitioning pattern of 1010 into the unused and unscrambled Z0 bytes and prevent these false indications. (SDH) '10' = (SDH) For OC-48c: Z0 #n = n + 1. For OC-12c: Z0 #'1' = 02H, Z0 #2 = 03H, and Z0 #3 = 04H. '11' = Reserved.	R/W	'00'
7:6	XmtJ0_Cnfg	Configures J0 transmit byte: '11' = Trace Identifier: 64-byte string format. '10' = Trace Identifier: 16-byte string length. (SDH) '01' = Default value: 01H (former C1 byte). '00' = Trace Identifier: 1-byte string length.	R/W	'01'
5:4	InvA1[1:0]	Inverts A1 framing bytes (used for testing). '0X' = No inversion. '10' = Invert forever. '11' = Invert for four frames.	R/W	'00'
3:2	InvB2[1:0]	Inverts B2 byte (used for testing). '0X' = No inversion. '10' = Invert forever. '11' = Invert for a frame.	R/W	'00'
1:0	InvB1[1:0]	Inverts B1 byte (used for testing). '0X' = No inversion. '10' = Invert forever. '11' = Invert for a frame.	R/W	'00'

11.8.2 T_SC_RSOH—Transmit Source Configuration for RSOH Bytes Register ((1cc)E1H)

Bit	Name	Description	Type	Default
15	TSOHINS_Ena	Active high enable for the TSOHINS[cc] insertion control input pin. ‘0' = disable the transmit SOH bytes insertion from the TSOH serial input bus in channel #(cc). This configuration bit takes precedence over the TSOHINS hardware control input pin. ‘1' = Enable the transmit SOH insertion from the TSOH serial input bus in channel #(cc). The SOH bytes insertion from TSOH bus is then controlled by TSOHINS input pin.	R/W	‘0’
14:11	Unused			
10	XmtUnRsohSrc	This bit is **not valid in STM-0/STS-1 mode**. It specifies the transmit source for the Undefined bytes of the RSOH (except National Use Bytes rows 1 and 2) when TSOHINS input pin is disabled (TSOHINS_Ena = ‘0’) or active-low on these bytes time slots in TSOH serial bus input. '0' = Unused bytes: set to internal Overhead default value (all '0') '1' = Source is Received byte (pass-through mode)	R/W	'0'
9:8	XmtD1D3Src[1:0]	This bit specifies the source of the transmitted D1-D3 bytes when TSOHINS input pin is disabled (TSOHINS_Ena = ‘0’) or active-low on these bytes time slots in TSOH serial bus input. '00' = Dedicated 192-Kbit/s TRD serial input, when used. '01' = Unused: internal Overhead default value (all '0') '1X' = Source is received byte (pass-through mode)	R/W	'01'
7	XmtNu2Src	This bit is **not valid in STM-0/STS-1 mode**. It specifies the transmit source for the National Use bytes in row 2 of the RSOH when TSOHINS input pin is disabled (TSOHINS_Ena = ‘0’) or active-low on these bytes time slots in TSOH serial bus input. '0' = Unused byte: set to internal Overhead default value (all '0') '1' = Source is Received byte (pass-through mode)	R/W	'0'
6:5	XmtF1Src[1:0]	This bit specifies the source of the transmitted F1 byte when TSOHINS input pin is disabled (TSOHINS_Ena = ‘0’) or active-low on F1 time slot in TSOH serial bus input: '00' = Dedicated 64-Kbit/s TDOW serial input, when used '01' = Unused: internal Overhead default value (all '0') '1X' = Source is received byte (pass-through mode)	R/W	'01'

Bit	Name	Description	Type	Default
4:2	XmtE1Src[2:0]	These bits specifies the source of the transmitted E1 byte when TSOHINS input pin is disabled (TSOHINS_Ena = ‘0’) or active-low on E1 time slot in TSOH serial bus input: '000' = Dedicated 64-Kbit/s TROW serial input, when used. '001' = “Quiet” PCM code. Internal default value = '01111111'. '01X' = Unused. Set to internal Overhead default value (all '0's). '1XX' = Source is received byte (pass-through mode).	R/W	'001'
1	XmtNu1Z0Src	This bit is **not valid in STM-0/STS-1 mode**. It specifies the transmit source for the National Use bytes/Z0 bytes in row 1 of the RSOH, when TSOHINS input pin is disabled (TSOHINS_Ena = ‘0’) or active-low on these bytes time slots in TSOH serial bus input. '0' = XmtFSTZ0Cnf ((1cc)E0H[13:8]): internal hardware processing. '1' = Source is Received byte (pass-through mode).	R/W	'0'
0	XmtJ0Src	This bit specifies the source of the transmitted J0 byte when TSOHINS input pin is disabled (TSOHINS_Ena = ‘0’) or active-low on J0 time slot in TSOH serial bus input. '0' = Microprocessor provides. '1' = Source is received byte (pass-through mode).	R/W	'0'

11.8.3 T_SC_MSOH—Transmit Source Configuration for MSOH Bytes Register ((1cc)E2H)

Bit	Name	Description	Type	Default
15:14	MstRdiOnHystCnfg[1:0]	Configure the hysteresis of MST RDI when inserted into the transmit K2 byte following either the detection of a receiver defect or its activation via either the TSAL input alarm bus or the microprocessor (see XmtMstRdiSrc configuration bit): '11' = Transmitted K2 RDI remains stable at least for 20 frames '10' = Transmitted K2 RDI remains stable at least for 10 frames '01' = Transmitted K2 RDI remains stable at least for 5 frames '00' = Transmitted K2 RDI remains stable at least for 1 frame.	R/W	'10'
13:12	XmtMstReiSrc [1:0]	These bits specify the source of the transmitted M1 REI bits when XmtPrcMsohSrc bit is set to '0' **AND** TSOHINS input pin is disabled (TSOHINS_Ena = '0' in register T_SC_RSOH[15]) or active-low on M1 time slot in TSOH serial bus input. It is **ignored in regenerator** configuration—**the received byte is passed through**. '00' = Hardware supplied REI (Feedback of received B2 errors as Bit or Block: see configuration register R_MST_C. '01' = Serial transmit Section Alarm bus, TSAL input pin. '1X' = REI bits are set to '0's (disabled).	R/W	'00'
11:10	XmtMstRdiSrc [1:0]	The source of the MST RDI bits (K2[2:0] = '110') are defined by these bits **when the transmit MstRdi default is active (a Remote Defect Indication has to be sent to the remote end), XmtPrcMsohSrc bit is set to '0' AND TSOHINS input pin is disabled (TSOHINS_Ena = '0'** in register T_SC_RSOH[15]) **or active-low** on K2 time slot in TSOH serial bus input. In any other case, the source of the K2[2:0] bits is specified by XmtK2ApsSrc configuration bit. It is **ignored in regenerator** configuration—**the received byte is passed through**. '00' = Hardware supplied MST RDI bits (internal feedback from the receiver major defects: see configuration register R_MST_C. It is also possible in this configuration to force a transmit RDI defect via the microprocessor (see register R_MST_C, bit #1). '01' = Serial Transmit Section Alarm bus, TSAL input pin. '1X' = Microprocessor supplied RDI (all K2 bits set to register (1cc)B5H value)	R/W	'00'
9	XmtK2ApsSrc	This bit specifies the source of the transmitted K2-APS byte when XmtPrcMsohSrc bit is set to '0', the transmit MstRdi default is not active (no Remote Defect Indication), **AND** TSOHINS input pin is disabled (TSOHINS_Ena = '0' in register T_SC_RSOH[15]) or active-low on K2 time slot in TSOH serial bus input. It is **ignored in regenerator** configuration—**the received byte is passed through**. '1' = Serial Transmit Section Alarm bus, TSAL input pin. '0' = Microprocessor (internal register MP_TK2K1). See also XmtMstRdiSrc configuration bit for the K2[2:0] bits	R/W	'0'
8	XmtK1Src	This bit specifies the source of the transmitted K1 byte when XmtPrcMsohSrc bit is set to '0' **and** TSOHINS input pin is disabled (TSOHINS_Ena = '0' in register T_SC_RSOH[15]) or active-low on K1 time slot in TSOH serial bus input. It is **ignored in regenerator** configuration—**the received byte is passed through**: '1' = Serial Transmit Section Alarm bus, TSAL input pin. '0' = Microprocessor (internal register MP_TK2K1).	R/W	'0'

Bit	Name	Description	Type	Default
7	TsalBusCnfg	Configure the Transmit input Section Alarm serial bus timings: '0' = Contradirectional bus '1' = Codirectional bus	R/W	'0'
6	XmtPrcMsohSrc	This bit specifies the passing through of all the Processed MSOH bytes (B2, K1, K2, S1 and M1) when TSOHINS input pin is disabled (TSOHINS_Ena = '0' in register T_SC_RSOH[15]) or active-low on these time slots in TSOH serial bus input. It is **ignored in regenerator** configuration—**the received bytes are passed through**: '0' = Internal hardware processed, serial accesses, or microprocessor provided (normal mode) (see MstReiSrc and MstRdiSrc) '1' = Source is Received byte from downstream (pass-through mode)	R/W	'0'
5:3	XmtE2Src[2:0]	This bit specifies the source of the transmitted E2 byte when TSOHINS input pin is disabled (TSOHINS_Ena = '0' in register T_SC_RSOH[15]) or active-low on E1 time slot in TSOH serial bus input. It is **ignored in regenerator** configuration—**the received byte is passed through**: '000' = Dedicated 64-Kbit/s TMOW serial input, when used '001' = "Quiet" PCM code. Internal default value '01111111'. '01X' = Unused. Set to internal Overhead default value (all '0's). '1XX' = Source is received byte from downstream (passed through).	R/W	'001'
2:1	XmtD4D12Src[1:0]	This bit specifies the source of the transmitted D4-D12 bytes when TSOHINS input pin is disabled (TSOHINS_Ena = '0' in register T_SC_RSOH[15]) or active-low on these bytes time slots in TSOH serial bus input. It is **ignored in regenerator** configuration—**the received bytes are passed through**: '00' = Dedicated 576-Kbit/s TMD serial input, when used '01' = Unused: internal Overhead default value (all '0') '1X' = Source is received byte from downstream (passed through)	R/W	'01'
0	XmtUnMsohSrc	This bit specifies the transmit source for the unused MSOH bytes (except B2, K1, K2, D4-D12, S1, M1, E2) when TSOHINS input pin is disabled (TSOHINS_Ena = '0' in register T_SC_RSOH[15]) or active-low on these bytes time slots in TSOH serial bus input. It is **ignored in regenerator** configuration—**the received bytes are passed through**: '0' = Unused bytes: set to internal Overhead default value (all '0') '1' = Source is Received byte from downstream (passed through)	R/W	'0'

11.8.4 T_J0_STRA—J0 Transmit String Data Access Register ((1cc)E4H)

This register allows the configuration of the J0 string to be transmitted in the outgoing SOH. See the R_J0_ESTRA register description for the configuration procedure.

Bit	Name	Description	Type	Default
15	XmtJ0StrgWrite	XmtJ0StrgWrite is the Write Command operational bit for the transmit J0 string internal RAM: When the microprocessor **writes** to this bit: '0' = No consequent action. '1' = Write XmtJ0StrgData[7:0] data byte into the expected string RAM at XmtJ0StrgAddr[5:0] address location (string pointer). XmtJ0StrgWrite bit clears automatically when this operation is completed. When the microprocessor **reads** this bit: '0' = The internal expected string RAM is ready for a new write operation. The previous write operation, if any, has been completed. '1' = A write operation is pending; the internal expected string RAM is busy and no new read or write operation to this RAM is allowed.	R/W	'0'
14	XmtJ0StrgRead	XmtJ0StrgRead is the Read Command operational bit for the transmit J0 string internal RAM: When the microprocessor **writes** to this bit: '0' = No consequent action. '1' = Download XmtJ0StrgData[7:0] data byte from the XmtJ0StrgAddr[5:0] address location (string pointer) of the expected string RAM into an internal register. XmtJ0StrgRead bit clears automatically when this operation is completed. The microprocessor accesses the downloaded value by performing a read at address (1cc)E4H (XmtJ0StrgData[7:0] value) and reading XmtJ0StrgRead as '0'. When the microprocessor **reads** this bit: '0' = The internal expected string RAM is ready for a new read operation. The previous read operation, if any, has been completed. '1' = A read operation is pending; the internal expected string RAM is busy and no new read/write operation to this RAM is allowed.	R/W	'0'
13:8	XmtJ0StrgAddr[5:0]	Bits [5:0] represents the string pointer value (RAM address)	R/W	000000
7:0	XmtJ0StrgData[7:0]	Bits [7:0] correspond to Data bits [7:0], respectively.	R/W	00H

11.8.5 MP_TK2K1—Microprocessor Provided Transmit K1 and K2 Bytes Register ((1cc)E5H)

Bit	Name	Description	Type	Default
15:8	XmtK2[7:0]	Bits [15:8] correspond to XmtK2[7:0], respectively.	R/W	00H
7:0	XmtK1[7:0]	Bits [7:0] correspond to XmtK1[7:0], respectively.	R/W	00H

11.8.6 MP_TS1—Microprocessor Provided Transmit S1 Byte Register ((1cc)E6H)

Bit	Name	Description	Type	Default
15:8	Unused			
7:0	XmtS1[7:0]	Bits [7:0] correspond to XmtS1[7:0], respectively.	R/W	00H

11.9 SONET/SDH Transmit Multiplexer Section Adaptation Channel Registers

11.9.1 T_AU_PTS—Transmit AU Pointer Operational Configuration ((1cc)E9H)

This register sets the transmit AU pointer value (including SS bits). It also allows positive and negative pointer movement, as well as NDF indication for testing purpose. The are following examples of its usage:

1. Setting XmtSetAuPtVal bit to '1' and both XmtAuPtSS[1:0] and XmtAuPtVal[9:0] to the expected transmit AU pointer value, the transmit pointer value and SS bits update as programmed.
2. Setting XmtSetNdf to '1', an NDF is generated.
3. Setting XmtSetAuPtVal and XmtSetNdf to '0' and XmtSetAuPos to '1', a positive pointer movement (positive justification) occurs and the transmit pointer value becomes XmtAuPtVal[9:0] + 1.
4. Setting XmtSetAuPos to '0' and XmtSetAuNeg to '1', a negative pointer movement (negative justification) occurs and the transmit pointer value becomes (XmtAuPtVal[9:0] - 1).

Bit	Name	Description	Type	Default
15	XmtSetAuPtVal	This bit allows the microprocessor to set a new pointer value. When writing to this register T_AU_PTS, if XmtSetAuPtVal = '1', then the current pointer value updates with the programmed value The internal hardware only allows consecXmtAuPtVal[9:0].	R/W	'0'
14	XmtSetAuPos	This bit allows the microprocessor to generate a positive pointer movement. When writing to this register T_AU_PTS, if XmtSetAuPos = '1', then a positive pointer movement occurs and the transmit pointer value increments by one. The internal hardware only allows consecutive pointer movements separated by 4 frames.	R/W	'0'
13	XmtSetAuNeg	This bit allows the microprocessor to generate a negative pointer movement. When writing to this register T_AU_PTS, if XmtSetAuNeg = '1', then a negative pointer movement occurs and the transmit pointer value decrements by one. The internal hardware only allows consecutive pointer movements separated by 4 frames.	R/W	'0'

Bit	Name	Description	Type	Default
12	XmtSetNdf	This bit allows the microprocessor to send an NDF. When writing to this register T_AU_PTS, if XmtSetNdf = '1', then an NDF ('1001') is inserted in transmit H1.	R/W	'0'
11:10	XmtAuPtSS[1:0]	Bits[1:0] correspond to the transmit SS bits value. For SDH, set this to '10'.	R/W	'00'
9:0	XmtAuPtVal[9:0]	Bits [9:0] correspond to the initial transmit Au pointer value, set by the microprocessor. A valid pointer value is between 0 and 782, but a value between 783 and 1023 can also be programmed for default testing.	R/W	00H

11.9.2 T_CAU_PT—Transmit Current AU Pointer Value ((1cc)EAH)

This register provides the current transmit AU Pointer Value. Since Positive and Negative justification may be set by the microprocessor (register T_AU_PTS), this value might differ from the programmed XmtAuPtVal[9:0] (register i39H).

Bit	Name	Description	Type	Default
15:10	Unused			
9:0	XmtCurAuPt[9:0]	Bits [9:0] correspond to the current transmit AU pointer value.	R	00H

11.10 SONET/SDH Transmit High-Order Path Termination Channel Registers

11.10.1 T_HPT_C—Transmit HPT Configuration ((1cc)E8H)

Bit	Name	Description	Type	Default
15	TPOHINS_Ena	Active high enable for the TPOHINS[cc] hardware insertion control input pin. '0' = disable the transmit POH bytes insertion from the TPOH serial input bus in channel #(cc). This configuration bit takes precedence over the TPOHINS hardware control input pin. '1' = Enable the transmit POH insertion from the TPOH serial input bus in channel #(cc). The POH bytes insertion from the TPOH bus is then controlled by TPOHINS input pin.	R/W	'0'
14	XmtStufCnfg	In STS-1/STM-0 mode, this bit configures whether the two fixed stuff columns (#30 and #59) are part of the payload. '0' = Columns #30 and #59 of the SPE **are** part of the payload and their content is part of the B3 BIP calculation. '1' = Columns #30 and 59 of the SPE **are not** part of the payload and considered as stuff columns. (SDH)	R/W	'0'
13	XmtAuPntrSrc	This bit forces all AU pointer bytes to be pass-through. It is **ignored in regenerator** configuration—**the received Pointer bytes are passed through**. '0' = Internal hardware and microprocessor registers generate the AU pointer bytes. (SDH) '1' = All AU pointer bytes are passed through (testing *only*).	R/W	'0'

Bit	Name	Description	Type	Default
12	XmtPOHSrc	This bit forces all POH bytes and fixed stuff columns to be pass-through. It is **ignored in regenerator** configuration—**the received POH bytes are passed through**. '0' = Source of all POH bytes are independently specified by other bits in this register. (SDH) '1' = All POH bytes are passed through (testing *only*).	R/W	'0'
11	Unused			
10	XmtH4Cnfg	Sets transmit value of H4 byte. It is **ignored in regenerator** configuration—**the received POH bytes are passed through**. '0' = All '0' (H4 transmit value is 00H). (SDH) '1' = All '1' (H4 transmit value is FFH).	R/W	'0'
9:8	XmtF2Src	These bits specify the source of the transmitted F2 byte when TPOHINS input pin is disabled (TPOHINS_Ena = '0' in register T_HPT_C[15]) or active-low on F2 time slot in TPOH serial bus input **AND** XmtPohSrc bit is set to '0'. It is **ignored in regenerator** configuration—**the received F2 byte is passed through**. '00' = Dedicated 64-Kbit/s TPOW1 serial input, when used. '01' = Unused. Internal Overhead default value (all '0's). '1X' = Source is received byte from downstream (testing *only*).	R/W	'01'
7:6	XmtF3Src	These bits specify the source of the transmitted Z3/F3 byte when TPOHINS input pin is disabled (TPOHINS_Ena = '0' in register T_HPT_C[15]) or active-low on Z3/F3 time slot in TPOH serial bus input **AND** XmtPohSrc bit is set to '0'. It is **ignored in regenerator** configuration—**the received Z3/F3 byte is passed through**. '00' = Dedicated 64-Kbit/s TPOW2 serial input, when used. '01' = Unused. Internal Overhead default value (all '0's) '1X' = Source is received byte from downstream (testing *only*).	R/W	'01'

Bit	Name	Description	Type	Default
5:4	Unused			
3:2	XmtHptReiSrc[1:0]	These bits specify the source of the transmitted G1 REI bits (G1[7:4]) when XmtPohSrc bit is set to '0' **AND** TPOHINS input pin is disabled (TPOHINS_Ena = '0' in register T_HPT_C[15]) or active-low on G1 time slot in TPOH serial bus input. It is **ignored in regenerator** configuration—**the received G1 byte is passed through**. '00' = Hardware supplied REI ≡ (feedback B3 errors). '01' = Serial transmit Path Alarm bus, TPAL input pin. '1X' = REI bits are set to '0's (disabled).	R/W	'00'

1:0	XmtHptRdiSrc[1:0]	The source of the G1 RDI bits (G1[3:1]) and Spare bit (G1[0]) is defined by these bits when XmtPohSrc bit is set to '0' **AND** TSOHINS input pin is disabled (TPOHINS_Ena = '0' in register T_HPT_C[15]) or active-low on G1 time slot in TPOH serial bus input. It is **ignored in regenerator** configuration—**the received G1 byte is passed through**.
		'00' = Hardware supplied RDI (G1[3:1]) = feedback receiver defects:
		If HptRdiEnhCnfg = '0' **Then** (Non Enhanced RDI).
		If (AuAisSt) = '1' **OR**
		(LopSt) = '1' **OR**
		(RdiOnUnEqpEn = '1' **AND** HptUnEqpSt = '1') **OR**
		(J1MsMtchSt = '1' **AND** RdiOnTimEn = '1') **OR**
		(RdiOnSlmEn = '1' **AND** HptSlmSt = '1') **OR**
		(AtmLcdSt = '1' **AND** RdiOnLcdEn = '1') **Then**
		G1[3][1] = '1'.
		End If;
		Elsif HptRdiEnhCnfg = '1' **Then** (Enhanced RDI)
		If (AuAisSt = '1' **OR** LopSt = '1') **Then**
		G1[3:1][2] = '101' (server defect).
		Elsif (RdiOnUnEqpEn = '1' **AND** HptUnEqpSt = '1') **OR**
		(J1MsMtchSt = '1' **AND** RdiOnTimEn = '1') **OR**
		(RdiOnSlmEn = '10' **AND** HptSlmSt ='1') **Then**
		G1[3:1][2] = '110' (connectivity defect).
		Elsif (RdiOnSlmEn = '11' **AND** HptSlmSt = '1') **OR**
		(AtmLcdSt = '1' **AND** RdiOnLcdEn = '1') **Then**
		G1[3:1][2] = '010' (payload defect).
		Else
		G1[3:1][2] = '001'.
		End If;
		End If;
		'01' = Serial transmit Path Alarm bus, TPAL input pin (for both G1 RDI and spare bits).
		'1X' = Microprocessor supplied RDI (register MP_THPTRDI)
		NOTES:
		1. G1[2:0] are set to the internal Overhead default value (all '0').
		2. The G1 Spare bit (G1[0]) is set to the internal Overhead default value ('0').
			R/W	'00'

11.10.2 T_HPT_OPC—Transmit HPT Operational Configuration ((1cc)EFH)

Bit	Name	Description	Type	Default
15	TpalBusCnfg	Configures the Transmit input Path Alarm serial bus timings: '0' = Contradirectional bus '1' = Codirectional bus	R/W	'0'
14:13	Unused			
12	InvH1ConcInd	Inverts the concatenation indication value for a concatenated payload. In OC-Nc, inverts the H1 byte #1 + p (p = 1…N). This configuration is used for testing: '0' = No inversion (concatenation indication is the standard value '1001SS11' on the unused H1 transmit byte). '1' = Invert forever (“false” concatenation indication is '0110 not (SS) 00' on the unused H1 transmit byte).	R/W	'0'
11:10	HptRdiXmtHystCnfg[1:0]	Configures the hysteresis of HPT RDI when inserted in the transmit frame: '11' = Transmitted G1 RDI remains stable for at least 20 frames following the detection of a specific defect. '10' = Transmitted G1 RDI remains stable for at least 10 frames following the detection of a specific defect. '01' = Transmitted G1 RDI remains stable for at least 5 frames following the detection of a specific defect. (SDH) '00' = Transmitted G1 RDI remains stable for at least 1 frame following the detection of a specific defect.	R/W	'01'
9	HptRdiXmtEnhCnfg	Configures the transmit HPT RDI-G1[3:1] (enhanced or not): '0' = Non-enhanced Transmit G1 RDI bits (1 bit). '1' = Enhanced Transmit G1 RDI bits (3 bits).	R/W	'1'
8	XmtUnEqp	Transmit unequipped VC-3 (STM-0) or VC-4 (STM-1) signal: '0' = Normal (Equipped). '1' = Unequipped ≡ C2 = 00H.(The transmitted B3 byte is valid and the N1 and J1 values are specified by the XmtUnEqpJ1Cnfg and XmtUnEqpN1Cnfg bits).	R/W	'0'
7	XmtUnEqpJ1Cnfg	Enables insertion of all '0's in the J1 bytes during active XmtUnEqp (register T_HPT_OPC, bit[8]) setting: '0' = During active XmtUnEqp, sends a J1 value defined by the J1 Ram if TPOHINS input pin is active-low on J1 time slot in TPOH serial bus input **AND** XmtPohSrc is set to '0'. '1' = During active XmtUnEqp, sends all '0's in the J1 byte.	R/W	'1'
6	XmtUnEqpN1Cnfg	Enables insertion of all '0's in the N1 bytes during active XmtUnEqp (register T_HPT_OPC, bit[8]) setting: '0' = During active XmtUnEqp, sends an N1 value defined by XmtPohSrc bit. '1' = During active XmtUnEqp, sends all '0's in the N1 byte if XmtPohSrc is set to '0'.	R/W	'1'
5:4	XmtJ1StrgLen [1:0]	Sets the transmitted J1 string length: '11' = Trace Identifier: 64-byte string length. '10' = Trace Identifier: 16-byte string length. (SDH) '01' = Default value: 01H. '00' = Trace Identifier: 1-byte string length. (SONET)	R/W	'00'

Bit	Name	Description	Type	Default
3	XmtMsaAisFrc	Forces AIS, at the pointer processing block level (MSA), toward the SDH network: '0' = Normal operation. '1' = Forces AIS.	R/W	'0'
2	XmtHptAisFrc	Forces AIS, at the HPT level, toward the SDH network: '0' = Normal operation. '1' = Forces AIS.	R/W	'0'
1:0	InvB3[1:0]	Inverts B3 byte (used for testing): '0X' = No inversion. '10' = Invert forever. '11' = Invert for a frame.	R/W	'00'

11.10.3 MP_TC2—Microprocessor Provided Transmit C2 Byte ((1cc)EBH)

Bit	Name	Description	Type	Default
15:8	Unused			
7:0	XmtC2[7:0]	Bits [7:0] correspond to XmtC2[7:0], respectively.	R/W	01H

11.10.4 MP_THPTRDI—Microprocessor Provided Transmit HPT-RDI Bits ((1cc)ECH)

Bit	Name	Description	Type	Default
15:4	Unused			
3:1	XmtHptRdi[2:0]	Microprocessor provided HPT RDI value. This value is transmitted in G1[3:1] when HptRdiSrc in register T_HPT_C[2] = '1'.	R/W	'000'
0	XmtG1SpBit	Microprocessor provided HPT RDI value. This value is transmitted in G1[0] when HptRdiSrc in register T_HPT_C[2] = '1'.	R/W	'0'

11.10.5 T_J1_STRA—J1 Transmit String Data Access Register ((1cc)EEH)

These registers allow the configuration of the J1 string to be transmitted in outgoing HPOH. See the R_J0_ESTRA ((1cc)85H) Register description for the configuration procedure.

Bit	Name	Description	Type	Default
15	XmtJ1StrgWrite	XmtJ1StrgWrite is the Write Command operational bit for the transmit J1 string internal RAM: When the microprocessor **writes** to this bit: '0' = No consequent action. '1' = Writes XmtJ1StrgData[7:0] data byte into the expected string RAM at XmtJ1StrgAddr[5:0] address location (string pointer). XmtJ1StrgWrite bit clears automatically when this operation is complete. When the microprocessor **reads** this bit: '0' = The internal expected string RAM is ready for a new write operation. The previous write operation, if any, has been completed. '1' = A write operation is pending; the internal expected string RAM is busy and no new read or write operation to this RAM is allowed.	R/W	'0'
14	XmtJ1StrgRead	XmtJ1StrgRead is the Read Command operational bit for the transmit J1 string internal RAM: When the microprocessor **writes** to this bit: '0' = No consequent action. '1' = Downloads XmtJ1StrgData[7:0] data byte from the XmtJ1StrgAddr[5:0] address location (string pointer) of the expected string RAM into an internal register. XmtJ1StrgRead bit clears automatically when this operation is complete. The microprocessor accesses the downloaded value by performing a read at address (1cc)EEH (XmtJ1StrgData[7:0] value) and reading XmtJ1StrgRead as '0'. When the microprocessor **reads** this bit: '0' = The internal expected string RAM is ready for a new read operation. The previous read operation, if any, has been completed. '1' = A read operation is pending; the internal expected string RAM is busy and no new read or write operation to this RAM is allowed.	R/W	'0'
13:8	XmtJ1StrgAddr[5:0]	Bits [5:0] represents the string pointer value (RAM address)	R/W	000000
7:0	XmtJ1StrgData[7:0]	Bits [7:0] correspond to data bits 7:0, respectively.	R/W	00H

11.11 ATM Receive Channel Registers

11.11.1 R_ACPCNF—Receive ATM Cell Processor Configuration ((1cc)20H)

Bit	Name	Description	Type	Default
15:11	Unused			
10	RcvGFCcontroller	RcvGFCcontroller allows the microprocessor to determine if the far-end device is a controller device, before configuring Intel IXF6048 as a controlled device. RcvGFCcontroller is set to logic one when receiving an ATM cell with GFC[3] (halt command), GFC[2] (SET_A command), or GFC[1] (SET_B command) set to logic one. RcvGFCcontroller automatically clears when this register is read.	R	'0'
9	RcvGFCcontrolled	RcvGFCcontrolled allows the microprocessor to determine if the far-end device is a controlled device, before configuring Intel IXF6048 as a controller device. RcvGFCcontrolled is set to logic one when receiving an ATM cell with the controlled-bit (GFC[0] in the GFC[3:0] field) set to logic one. RcvGFCcontrolled automatically clears when this register is read.	R	'0'
8	RcvIUFltrEn	RcvIUFltrEn enables the dropping of ATM cells based on the Idle/ Unassigned cell filter matching (register R_IUCFLTR): '0' = The ATM cells matching the programmable Idle/Unassigned cell filter are **not** discarded. '1' = The ATM cells matching the programmable Idle/Unassigned cell filter are discarded. The configuration of RcvIUFltrEn does not affect the incrementing of the idle cell counter (register R_ICELLCNT). This counter is incremented when the Idle/Unassigned cell filter matches a header, independently of RcvIUFltrEn.	R/W	'1'
7	RcvCorrectEn	RcvCorrectEn enables the HEC-based correction algorithm. '0' = The correction algorithm is disabled and any single or multiple bit error in the header of a cell is treated as an uncorrectable error. '1' = The correction algorithm is enabled and single-bit errors are corrected.	R/W	'1'
6:5	RcvCorrDetCnf [1:0]	RcvCorrDetCnf[1:0] configures the number of consecutive error-free cells required, while in Detection mode, to return to Correction mode: '00' = The receiver returns to Correction mode after receiving one ATM cell with no HEC errors. This cell is accepted. '01' = The receiver returns to Correction mode after receiving two consecutive ATM cells with no HEC errors. The last cell (the second cell) is accepted. '10' = The receiver returns to Correction mode after receiving four consecutive ATM cells with no HEC errors. The last cell is accepted. '11' = The receiver returns to Correction Mode after receiving eight consecutive ATM cells with no HEC errors. The last cell is accepted.	R/W	'00'

Bit	Name	Description	Type	Default
4	RcvLCDCnf	RcvLCDCnf configures the discarding of ATM cells while in the loss of cell delineation (LCD) state: '0' = The ATM cells are accepted whether the receiver is in the LCD state or not. '1' = The ATM cells are dropped while the receiver is in the LCD state.	R/W	'0'
3	RcvSYNCCnf	RcvSYNCCnf configures the discarding of ATM cells while in the SYNC state: '0' = The ATM cells with uncorrectable errors are discarded. '1' = The received ATM cells are accepted regardless of the errors detected in the HEC field.	R/W	'0'
2	RcvPRESYNCCnf	RcvPRESYNCCnf configures the discarding of ATM cells while in the PRESYNC state: '0' = No cells are accepted while in the PRESYNC state. '1' = All the ATM cells with correct HEC (up to DELTA = 6) are accepted.	R/W	'0'
1	RcvHECAdd	RcvHECAdd enables the addition (XOR) of the pattern '01010101' ($X^6 + X^4 + X^2 + 1$) to the received HEC sequence before comparison to the expected (calculated) value: '0' = The received HEC sequence is not modified before comparison. '1' = The received HEC sequence is modified (by adding the sequence '01010101') before comparison.	R/W	'1'
0	RcvDescrEn	RcvDescrEn controls the descrambling of the cell payload by using the self-synchronous scrambler $1 + X^{43}$: '0' = The scrambler is disabled. '1' = The scrambler is enabled.	R/W	'1'

11.11.2 R_IUCFLTR—Receive Idle/Unassigned Cell Filter ((1cc)21H)

This register provides a programmable filter used to detect (and optionally to discard) the received idle and/or unassigned ATM cells. The register contains the value of the ATM cell header fields GFC, PTI and CLP (register bits 7:0) used to compare the incoming GFC, PTI and CLP bits and a mask (register bits 15:8) enabling the comparison of each individual bit. An ATM cell is identified as idle/unassigned if the VPI and VCI fields contain the all '0's pattern **and** if the GFC, PTI and CLP fields match the programmable filter.

Bit	Name	Description	Type	Default
15:12	RcvGFCMask[3:0]	RcvGFC[3:0] contains the Generic Flow Control mask used by the idle/unassigned cell programmable filter. If a bit of RcvGFCMask[3:0] is set to logic one, then the corresponding bit of the received GFC field is compared. If a bit of RcvGFCMask[3:0] is set to logic zero, then the corresponding bit of the received GFC field is not compared.	R/W	FH
11:9	RcvPTIMask[2:0]	RcvPTIMask[2:0] contains the Payload Type Indicator mask used by the idle/unassigned cell programmable filter. If a bit of RcvPTIMask[2:0] is set to logic one, then the corresponding bit of the received PTI field is compared. If a bit of RcvPTIMask[2:0] is set to logic zero, then the corresponding bit of the received PTI field is not compared.	R/W	'111'
8	RcvCLPMask	RcvCLPMask contains the Cell Loss Priority mask used by the idle/unassigned cell programmable filter. If RcvCLPMask is set to logic one, then the incoming CLP field is compared with RcvCLPPatt. If RcvCLPMask is set to logic zero, then the incoming CLP field is not compared.	R/W	'1'
7:4	RcvGFCPatt[3:0]	RcvGFCPatt[3:0] contains the Generic Flow Control pattern used by the idle/unassigned cell programmable filter. The received GFC field is compared bit by bit with RcvGFCPatt[3:0].	R/W	0H
3:1	RcvPTIPatt[2:0]	RcvPTIPatt[2:0] contains the Payload Type Indicator pattern used by the idle/unassigned cell programmable filter. The received PTI field is compared bit by bit with RcvPTIPatt[2:0].	R/W	'000'
0	RcvCLPPatt	RcvCLPPatt contains the Cell Loss Priority pattern used by the idle/unassigned cell programmable filter. The received CLP field is compared with RcvCLPPatt.	R/W	'1'

11.11.3 R_LCDFLTR—Receive LCD Filter ((1cc)23H-(1cc)22H)

(1cc)23H = Bits[18:16], (1cc)22H = Bits[15:0]

Bit	Name	Description	Type	Default
31:18	Unused			
18:0	RcvLCDFltr[18:0]	RcvLCDFltr[18:0] contains the number of consecutive cell periods used to filter the LCD (loss of cell delineation) defect. The LCD defect is declared if an OCD (out of cell delineation) anomaly has persisted for more than RcvLCDFltr[18:0] cell periods. The LCD defect terminates when the cell delineation process enters and remains in the SYNC state for more than RcvLCDFltr[18:0] cell periods. The default value sets a delay of 1 ms for OC-48c. Table 27 shows configuration examples of setting delays of 1 ms, 2 ms, 3 ms and 4 ms for OC-1, OC-3, OC-12 and OC-48.	R/W	12FC0H

Table 27. LCD Filter Configuration Examples

	1 ms	2 ms	3 ms	4 ms
OC-1 (clock-period = 617.28 ns)	00654H	00CA8H	012FCH	01950H
OC-3 (clock-period = 205.76 ns)	012FCH	025F8H	038F4H	04BF0H
OC-12 (clock-period = 51.44 ns)	04BF0H	097E0H	0E3D0H	12FC0H
OC-48 (clock-period = 12.86 ns)	12FC0H	25F81H	38F41H	4BF02H

11.11.4 R_ACELLCNT—Receive ATM Cell Counter ((1cc)25H-(1cc)24H)

(1cc)25H = Bits[23:16], (1cc)24H = Bits[15:0]

Bit	Name	Description	Type	Default
31:24	Unused			
23:0	RcvACellCnt[23:0]	RcvACellCnt[23:0] counts the number of ATM cells accepted (written into the FIFO) during the last accumulation interval. A write to the counter (address (1cc)25H) causes the entire counter to be loaded into a buffer and then cleared. The contents of the buffer can then be read.	R	00H

11.11.5 R_ICELLCNT—Receive Idle Cell Counter ((1cc)27H-(1cc)26H)

(1cc)27H = Bits[23:16], (1cc)26H = Bits[15:0]

Bit	Name	Description	Type	Default
31:24	Unused			
23:0	RcvICellCnt[23:0]	RcvICellCnt[31:0] counts the number of idle/unassigned cells detected by the programmable Idle/Unassigned Cell Filter (register R_IUCFLTR). This counter is incremented independently of the configuration of RcvIUFltrEn (R_ACPCNF). A write to the counter (address (1cc)27H) causes the entire counter to be loaded into a buffer and then cleared. The contents of the buffer can then be read.	R	00H

11.11.6 R_CHECNT—Receive Correctable HEC Error Counter ((1cc)28H)

Bit	Name	Description	Type	Default
15:0	RcvCHECnt[15:0]	RcvCHECnt[15:0] counts the number of correctable HEC errors received during the last accumulation interval. This counter is incremented independently of the configuration of RcvCorrectEn (register R_ACPCNF). A write to the counter (address (1cc)28H) causes the entire counter to be loaded into a buffer and then cleared. The contents of the buffer can then be read.	R	00H

11.11.7 R_UHECNT—Receive Uncorrectable HEC Error Counter ((1cc)29H)

Bit	Name	Description	Type	Default
15:0	RcvUHECnt[15:0]	RcvUHECnt[15:0] counts the number of uncorrectable HEC errors received during the last accumulation interval. This counter is incremented independently of the configuration of RcvCorrectEn (register R_ACPCNF). A write to the counter (address (1cc)29H) causes the entire counter to be loaded into a buffer and then cleared. The contents of the buffer can then be read.	R	00H

11.11.8 R_CFOCNT—Receive Cell FIFO Overflow Counter ((1cc)2AH)

Bit	Name	Description	Type	Default
15:0	RcvFifoOFCnt[15:0]	RcvFifoOFCnt[15:0] counts the number of accepted cells that have been lost due to a FIFO overrun during the last accumulation interval. These cells have not been written into the FIFO. A write to the counter (address (1cc)2AH) causes the entire counter to be loaded into a buffer and then cleared. The contents of the buffer can then be read.	R	00H

11.11.9 R_ATMINT—Receive ATM Interrupt (and Status) Register ((1cc)2BH)

Bit	Name	Description	Type	Default
15:12	Unused			
11	RcvLCDSt	The RcvLCDSt status bit shows the state of the cell delineation process. When RcvLCDSt is high, the cell delineation process is in the LCD (loss of cell delineation) state. When RcvLCDSt is low, the cell delineation process is not in the LCD state. Register R_LCDFLTR contains a programmable threshold for configuring the transitions to/from the LCD state.	R	'0'
10	RcvOCDSt	The RcvOCDSt status bit shows the state of the cell delineation process. When RcvOCDSt is low, the cell delineation process is in the SYNC state. When RcvOCDtS is high, the cell delineation process is in the HUNT or PRESYNCH states.	R	'0'
9	RcvICellCntI	RcvICellCntI sets to logic one when the “receive idle cell counter” (register R_ICELLCNT) rolls over. This interrupt bit clears automatically when this register is read.	R	'0'
8	RcvACellCntI	RcvACellCntI sets to logic one when the “receive ATM cell counter” (register R_ACELLCNT) rolls over. This interrupt bit clears automatically when this register is read.	R	'0'
7	RcvUHECntI	RcvUHECntI sets to logic one when the “receive ATM uncorrectable HEC error counter” (register R_UHECNT) rolls over. This interrupt bit clears automatically when this register is read.	R	'0'
6	RcvCHECntI	RcvCHECntI sets to logic one when the “receive ATM correctable HEC error counter” (register R_CHECNT) rolls over. This interrupt bit clears automatically when this register is read.	R	'0'
5	RcvFifoOFCntI	RcvFifoOFCntI sets to logic one when the “receive ATM FIFO overflow counter” (register R_CFOCNT) rolls over. This interrupt bit clears automatically when this register is read.	R	'0'
4	RcvLCDI	RcvLCDI sets to logic one when the cell delineation process enters or exits the LCD (loss of cell delineation) state. This interrupt bit clears automatically when this register is read.	R	'0'
3	RcvOCDI	RcvOCDI sets to logic one when the cell delineation process enters or exits the SYNC state. This interrupt bit clears automatically when this register is read.	R	'0'
2	RcvUHEI	RcvUHEI sets to logic one when an ATM cell with an uncorrectable header error is received. This interrupt bit clears automatically when this register is read.	R	'0'
1	RcvCHEI	RcvCHEI sets to logic one when an ATM cell with a correctable header error is received. This interrupt is activated regardless of the configuration of RcvCorrectEn (register R_ACPCNF). This interrupt bit clears automatically when this register is read.	R	'0'
0	RcvFifoOFI	RcvFifoOFI sets to logic one when a receive ATM FIFO overflow occurs. This means the receive ATM cell processor can not write an ATM cell because the receive ATM FIFO does not have available space for a complete cell. This interrupt bit clears automatically when this register is read.	R	'0'

11.11.10 R_ATMINTEN—Receive ATM Interrupt Enable ((1cc)2CH)

Bit	Name	Description	Type	Default
15:10	Unused			
9	RcvICellCntIEn	Active-high enable for the RcvICellCntI interrupt bit.	R/W	'0'
8	RcvACellCntIEn	Active-high enable for the RcvACellCntI interrupt bit.	R/W	'0'
7	RcvUHECntIEn	Active-high enable for the RcvUHECntI interrupt bit.	R/W	'0'
6	RcvCHECntIEn	Active-high enable for the RcvCHECntI interrupt bit.	R/W	'0'
5	RcvFifoOFCntIEn	Active-high enable for the RcvOFCntI interrupt bit.	R/W	'0'
4	RcvLCDIEn	Active-high enable for the RcvLCDI interrupt bit.	R/W	'0'
3	RcvOCDIEn	Active-high enable for the RcvOCDI interrupt bit.	R/W	'0'
2	RcvUHEIEn	Active-high enable for the RcvUHEI interrupt bit.	R/W	'0'
1	RcvCHEIEn	Active-high enable for the RcvCHEI interrupt bit.	R/W	'0'
0	RcvFifoOFIEn	Active-high enable for the RcvFifoOFI interrupt bit.	R/W	'0'

11.12 ATM Transmit Channel Registers

11.12.1 T_ACPCNF—Transmit ATM Cell Processor Configuration ((1cc)10H)

Bit	Name	Description	Type	Default
15:14	Unused			
13	XmtTestVPI	For test and debug purpose only. When XmtTestVPI = 0 (normal mode) idle cells are sent with VPI = VCI = 0 and GFC,PT, CLP is taken from register T_ICELLP When XmtTestVPI = 1 (debug mode) instead of idle cells, cells with VPI = 32 (20H), VCI = 0 are sent. Fields GFC,PT and CLP are taken from register T_ICELLP.	R/W	'0'
12:11	XmtExtHEC	XmtExtHec configures HEC insertion: '00' = HEC is generated by the ATM processor. '01' = The HEC inserted in cells is the result of an XOR function between the HEC generated by the ATM processor and the extra byte passed through the UTOPIA interface (when XmtCellStruct = '1' in register T_UICHCNF). '10' = The extra byte passed through the UTOPIA interface is sent as the HEC.	R/W	'00'
10	XmtGFCcontroller	When XmtGFCcontroller is set to logic one, Intel IXF6048 is configured as a controller-device and the cyclic halt function is enabled. The cyclic halt function sets the halt-bit (GFC[3]) to logic one, in a fixed fraction of the transmitted ATM cells. This limits the ATM traffic of the network across the UNI to a fixed fraction of the interface. This fixed fraction is configured by XmtGFCCnt[2:0]. The XmtGFCcontroller and XmtGFCcontrolled bits **must not** be set to logic one simultaneously.	R/W	'0'

Bit	Name	Description	Type	Default
9	XmtGFCcontrolled	XmtGFCcontrolled configures Intel IXF6048 as a controlled device. When XmtGFCcontrolled is set to logic one, the transmit ATM cell processor will: 1. Set the controlled-bit (GFC[0]) to logic one in the GFC[3:0] field, in all the transmitted cells. 2. Enable the GFC halt monitoring function. Every time an ATM cell with the halt-bit (GFC[3]) set to logic one is received, an unassigned cell is inserted in the transmit stream. The XmtGFCcontrolled and XmtGFCcontroller bits **must not** be set to logic one simultaneously.	R/W	'0'
8:6	XmtGFCCnt[2:0]	XmtGFCCnt[2:0] are used only by the transmitter when Intel IXF6048 is configured as a controller device (XmtGFCcontroller = '1'). XmtGFCCnt[2:0] indicates how many ATM cells are sent with the halt bit set to logic one (GFC[3] = '1') for every ATM cell sent with the halt bit set to logic zero: XmtGFCCnt[2:0]: '000' = GFC[3] is never set to logic one '001' = GFC[3] is '1' in 50% of the transmitted cells. '010' = GFC[3] is '1' in 66% of the transmitted cells. …… '111' = GFC[3] is '1' in 87.5% of the transmitted cells.	R/W	'000'
5	XmtReadEn	XmtReadEn disables the reading of ATM Layer cells from the transmit ATM FIFO. '0' = The transmit ATM cell processor does not read cells from the transmit FIFO (even if the FIFO contains complete ATM cell(s)) and maps idle cells into the SPE. '1' = The transmit ATM cell processor operates normally, reading ATM cells from the transmit FIFO (if the FIFO contains complete ATM cell(s)). XmtReadEn should not be used for transmit Flow Control. Configuration bits XmtGFCcontrolled and XmtGFCCnt[2:0] offer a better way to do that.	R/W	'1'
4:3	XmtHErrCnf	XmtHErrCnf[1:0] configures the insertion of errors into the transmitted ATM cells: '00' = Reserved. '01' = Reserved. '10' = Correctable errors are inserted in the transmitted cells when XmtHErrEn is set to logic one. '11' = Multiple uncorrectable errors are inserted in the transmitted cells when XmtHErrEn is set to logic one. When a correctable error is inserted, the most significant bit (first transmitted bit) of the HEC sequence is inverted prior to transmission. When an uncorrectable error is inserted, the eight bits of the HEC sequence are inverted prior to transmission.	R/W	'00'

Bit	Name	Description	Type	Default
2	XmtHErrEn	XmtHErrEn controls the insertion of HEC errors into the transmitted ATM cells according to the configuration stored in XmtHErrCnf. Errors are inserted when XmtHErrEn is set to logic one.	R/W	'0'
1	XmtHECAdd	XmtHECAdd enables the addition (XOR) of the pattern '01010101' ($X^6 + X^4 + X^2 + 1$) to the calculated HEC sequence before mapping the ATM cell into the SPE: '0' = The calculated HEC sequence is not modified before transmission. '1' = The calculated HEC sequence is modified (by adding the sequence '01010101') before transmission.	R/W	'1'
0	XmtScrEn	XmtScrEn controls the scrambling of the cell payload by using the self-synchronous scrambler $1 + X^{43}$: '0' = The scrambler is disabled. '1' = The scrambler is enabled.	R/W	'1'

11.12.2 T_ICELLP—Transmit Idle Cell Pattern ((1cc)11H)

This register contains the value of the ATM cell header fields GFC, PTI and CLP and the payload pattern used in the generated Idle cells. An Idle cell is generated and transmitted when the TACP block detects that the transmit FIFO does not contain any complete ATM cell.

The VPI and VCI fields of the generated Idle cells contain the all '0's pattern.

Bit	Name	Description	Type	Default
15:8	XmtPyldPatt[7:0]	XmtPyldPatt[7:0] contains the pattern transmitted in the entire 48-byte payload of the idle cells.	R/W	6AH
7:4	XmtGFCPatt[3:0]	XmtGFCPatt[3:0] contains the Generic Flow Control (GFC) field transmitted on the first octet of the idle/unassigned cells (bits 1, 2, 3 and 4).	R/W	'0'
3:1	XmtPTIPatt[2:0]	XmtPTIPattPTI[2:0] contains the Payload Type Indicator (PTI) field transmitted on the fourth octet of the idle/unassigned cells (bits 5, 6 and 7).	R/W	'0'
0	XmtCLPPatt	XmtCLPPatt contains the Cell Loss Priority (CLP) field transmitted on the fourth octet of the idle/unassigned cells (bit 8).	R/W	'1'

11.12.3 T_ACELLCNT—Transmit ATM Cell Counter ((1cc)13H-(1cc)12H)

(1cc)13H = Bits[23:16], (1cc)12H = Bits[15:0]

Bit	Name	Description	Type	Default
31:24	Unused			
23:0	XmtACellCnt[23:0]	XmtACellCnt[23:0] counts the number of ATM cells read from the transmit FIFO (ATM Layer cells) and mapped into the transmitted SONET/SDH frames during the last accumulation interval. A write to the counter (address (1cc)13H) causes the entire counter to be loaded into a buffer and then cleared. The contents of the buffer can then be read.	R	00H

11.12.4 T_ICELLCNT—Transmit Idle Cell Counter ((1cc)15H-(1cc)14H)

(1cc)15H = Bits[23:16], (1cc)14H = Bits[15:0]

Bit	Name	Description	Type	Default
31:24	Unused			
23:0	XmtICellCnt[23:0]	XmtICellCnt[31:0] counts the number of idle cells generated and mapped into the transmitted SONET/SDH frames during the last accumulation interval. This counter only counts the idle cells generated by the cell rate decoupling process: the idle cells generated when the transmit FIFO does not contain a complete ATM cell. This counter does not count the null cells generated by the Generic Flow Control (GFC) Halt function. A write to the counter (address (1cc)15H) causes the entire counter to be loaded into a buffer and then cleared. The contents of the buffer can then be read.	R	00H

11.12.5 T_ATMINT—Transmit ATM Interrupt Register ((1cc)16H)

Bit	Name	Description	Type	Default
15:2	Unused			
1	XmtICellCntI	XmtICellCntI sets to logic one when the “transmit idle cell counter” (register T_ICELLCNT) rolls over. This interrupt bit clears automatically when this register is read.	R	'0'
0	XmtACellCntI	XmtACellCntI sets to logic one when the “transmit ATM cell counter” (register T_ACELLCNT) rolls over. This interrupt bit clears automatically when this register is read.	R	'0'

11.12.6 T_ATMINTEN—Transmit ATM Interrupt Enable ((1cc)17H)

Bit	Name	Description	Type	Default
15:2	Unused			
1	XmtICellCntIEn	Active-high enable for the XmtICellCntI interrupt bit	R/W	'0'
0	XmtACellCntIEn	Active-high enable for the XmtACellCntI interrupt bit	R/W	'0'

11.13 POS Receive Channel Registers

11.13.1 R_PHCCNF—Receive POS HDLC Controller Configuration ((1cc)60H)

Bit	Name	Description	Type	Default
15:13	Unused			
12	RcvCntWrFr	RcvCntWrFr configures how performance monitoring function are done: '0' = Performance monitoring functions are not affected by FIFO overflows. This mode is intended for line monitoring. '1' = Only frames written into the FIFO are considered for performance monitoring purposes.	R/W	'0'
11	RcvAByteCntEn	RcvAByteCntEn configures how byte counts are performed: '0' = R_BYTECNT counts all the bytes written into the FIFO. '1' = Only bytes in good frames (frames not aborted and without errors) are counted.	R/W	'0'
10	RcvFCSErr	Frames with FCS errors are marked as erroneous in the FIFO only if RcvFCSErr = '1'.	R/W	'0'
9	RcvFCSPass	RcvFCSPass configures the writing of the HDLC FCS field into the receive FIFO: '0' = The FCS field is eliminated and not written into the receive FIFO. '1' = The FCS field is written into the receive FIFO except when RcvACPass = '1'. If RcvACPass = '1', the FCS field must be eliminated and is not written into the FIFO regardless of RcvFCSPass.	R/W	'0'
8	RcvTrDescrEn	RcvTrDescrEn controls the descrambling of the HDLC frames, after byte destuffing, by using the self-synchronous scrambler $X^{48} + X^{28} + X^{27} + 1$: '0' = The scrambler is disabled. '1' = The scrambler is enabled.	R/W	'0'
7	RcvFifEn	RcvFifEn enables removal of frame intrafilling sequences (Control Escape character pairs) before the byte destuffing process: '0' = Frame intrafilling is disabled. If a pair of Control Escape characters are received (7DH-7DH), they are converted to the character 5DH, after destuffing. '1' = All Control Escape character pairs are discarded before going to the destuffing process.	R/W	'0'
6	RcvMaxPLDEn	RcvMaxPLDEn enables discarding of packets longer than the programmed maximum packet length (register R_MAXPL): '0' = The packet is **not** marked as errored in the receive FIFO. The rest of the packet is received and written into the FIFO normally. '1' = The packet is marked as errored in the receive FIFO (the user must discard it) and the rest of the FIFO is not stored into the receive FIFO. The HDLC controller stops writing and waits for a new HDLC frame. The counter which counts the number of received frames longer than the programmed maximum length (register R_MAXPLECNT) operates independently of the configuration of RcvMaxPLDEn.	R/W	'1'

Bit	Name	Description	Type	Default
5	RcvMinPLDEn	RcvMinPLDEn enables discarding of packets smaller than the programmed minimum packet length (register R_MINPL): '0' = The packet is **not** marked as errored in the receive FIFO. '1' = The packet is marked as errored in the receive FIFO (the user must discard it). Independent of the configuration of RcvMinPLDEn, packets smaller than R_MINPL are always entirely written into the receive FIFO. The counter which counts the number of received frames smaller than the programmed minimum length (register R_MINPLECNT) operates independently of the configuration of RcvMinPLDEn.	R/W	'1'
4	RcvACChk	RcvACChk enables checking the HDLC Address and Control fields: '0' = The Address and Control fields are **not** checked by the receiver. '1' = The Address field is compared with FFH (the All-Stations address) and the Control field is compared with 03H (the Unnumbered Information command with the Poll/Final bit set to '0'). If RcvACChk = '1', the frames containing Address and Control fields with values different than FFH and 03H are discarded (not written into the FIFO).	R/W	'0'
3:2	RcvFCSCnf[1:0]	RcvFCSCnf[1:0] selects the size of the Frame Check Sequence (FCS) in the received frames and whether it is checked or not: **RcvFCSCnf[1:0] — # Bytes and Action Performed** '00' — CRC-16 (CRC-CCITT), no checking. '01' — CRC-32, no checking. '10' — CRC-16 (CRC-CCITT), does check. '11 — CRC-32, does check.	R/W	'11'
1	RcvACPass	RcvACPass configures writing of the HDLC Address and Control fields into the receive FIFO: '0' = The HDLC controller writes only the HDLC Information field (PPP frames) of the received HDLC frames into the receive FIFO. '1' = The HDLC controller writes the HDLC Address and Control fields, as well as the Information field, into the receive FIFO, allowing optional processing of these two fields.	R/W	'1'
0	RcvDescrEn	RcvDescrEn controls descrambling of HDLC frames (the SONET/SDH SPE) by using the self-synchronous scrambler 1 + X^{43}: '0' = The scrambler is disabled. '1' = The scrambler is enabled.	R/W	'1'

11.13.2 R_MINPL—Receive Minimum Packet Length ((1cc)61H)

Bit	Name	Description	Type	Default
15:8	Unused			
7:0	RcvMinPL[7:0]	RcvMinPL sets the minimum packet length in bytes. The packet length is defined as the HDLC frame information field length, i.e., the bytes after the HDLC-Control field and before the HDLC-FCS field. Any packet smaller than Minimum Packet Length is optionally marked errored.	R/W	02H

11.13.3 R_MAXPL—Receive Maximum Packet Length ((1cc)62H)

Bit	Name	Description	Type	Default
15:0	RcvMaxPL[15:0]	RcvMaxPL sets the maximum packet length in bytes. The packet length is defined as the HDLC frame information field length, i.e., the bytes after the HDLC-Control field and before the HDLC-FCS field. Any packet longer than the Maximum Packet Length is optionally marked errored. MaxPL defaults to 1.5-Kbytes.	R/W	0600H

11.13.4 R_FRMCNT—Receive Frame Counter ((1cc)64H-(1cc)63H)

(1cc)64H = Bits[26:16], (1cc)63H = Bits[15:0]

Bit	Name	Description	Type	Default
31:27	Unused			
26:0	RcvFrmCnt[26:0]	RcvFrmCnt[26:0] counts the number of good received frames written into the FIFO (not marked as invalid) during the last accumulation interval. RcvFrmCnt[26:0] does not count the aborted HDLC frames. A write to the counter (address (1cc)64H) causes the entire counter to be loaded into a buffer and then cleared. The contents of the buffer may then be read.	R	00H

11.13.5 R_BYTECNT—Receive Byte Counter ((1cc)66H-(1cc)65H)

(1cc)66H = Bits[28:16], (1cc)65H = Bits[15:0]

Bit	Name	Description	Type	Default
31:29	Unused			
28:0	RcvByteCnt[28:0]	RcvByteCnt[28:0] counts the number of bytes received and written into the receive FIFO during the last accumulation interval. If RcvAByteCntEn = '0' (register R_PHCCNF), RcvByteCnt only counts the bytes received within good frames (not marked as errored). If RcvAByteCntEn = '1' (register R_PHCCNF), RcvByteCnt counts all the bytes written into the FIFO (good frames + frames with FCS error + frames with Abort sequence). A write to the counter (address (1cc)66H) causes the entire counter to be loaded into a buffer and then cleared. The contents of the buffer may then be read.	R	00H

11.13.6 R_AFCNT—Receive Aborted Frame Counter ((1cc)68H-(1cc)67H)

(1cc)68H = Bits[19:16], (1cc)67H = Bits[15:0]

Bit	Name	Description	Type	Default
31:20	Unused			
19:0	RcvAFrmCnt[19:0]	RcvAFrmCnt[19:0] counts the number of received aborted frames (finishing with an Abort sequence) during the last accumulation interval. These frames are written into the receive FIFO and marked as errored. A write to the counter (address (1cc)68H) causes the entire counter to be loaded into a buffer and then cleared. The contents of the buffer may then be read.	R	00H

11.13.7 R_FCSECNT—Receive FCS Error Counter ((1cc)6AH-(1cc)69H)

(1cc)6AH = Bits[19:16], (1cc)69H = Bits[15:0]

Bit	Name	Description	Type	Default
31:20	Unused			
19:0	RcvFCSECnt[19:0]	RcvFCSECnt[19:0] counts the number of received errored frames (with an incorrect FCS field) during the last accumulation interval. These frames are written into the receive FIFO and marked as errored. A write to the counter (address (1cc)6AH) causes the entire counter to be loaded into a buffer and then cleared. The contents of the buffer may then be read.	R	00H

11.13.8 R_PFOCNT—Receive Packet FIFO Overflow Counter ((1cc)6BH)

Bit	Name	Description	Type	Default
15:0	RcvFifoOFCnt[15:0]	RcvFifoOFCnt[15:0] counts the number of received frames that have been lost due to a FIFO overrun during the last accumulation interval. Some of these frames could have been partially written into the FIFO and marked as errored and some others could have been completely lost. A write to the counter (address (1cc)6BH) causes the entire counter to be loaded into a buffer and then cleared. The contents of the buffer may then be read.	R	00H

11.13.9 R_MINPLECNT—Receive Minimum Packet Length Error Counter ((1cc)6DH-(1cc)6CH)

(1cc)6DH = Bits[26:16], (1cc)6CH = Bits[15:0]

Bit	Name	Description	Type	Default
31:27	Unused			
26:0	RcvMinPLECnt[26:0]	RcvMinPLECnt[26:0] counts the number of HDLC frames received and written into the receive FIFO with a packet length shorter than the Minimum Packet Length (RcvMinPL). This counter works independent of the configuration of RcvMinPLDEn (register R_PHCCNF). A write to the counter (address (1cc)6DH) causes the entire counter to be loaded into a buffer and then cleared. The contents of the buffer may then be read.	R	00H

11.13.10 R_MAXPLECNT—Receive Maximum Packet Length Error Counter ((1cc)6EH)

Bit	Name	Description	Type	Default
15:0	RcvMaxPLECnt[15:0]	RcvMaxPLECnt[15:0] counts the number of HDLC frames received and written into the receive FIFO during the last accumulation interval with a packet length longer than the Maximum Packet Length (RcvMaxPL). This counter works independent of the configuration of RcvMaxPLDEn (register R_PHCCNF). A write to the counter (address (1cc)6EH) causes the entire counter to be loaded into a buffer and then cleared. The contents of the buffer may then be read.	R	00H

11.13.11 R_POSINT—Receive POS Interrupt Register ((1cc)6FH)

Bit	Name	Description	Type	Default
15	Unused			
14	RcvMaxPLCntI	RcvMaxPLCntI sets to logic one when the receive maximum packet length error counter (register R_MAXPLECNT) rolls over. This interrupt bit clears automatically when this register is read.	R	'0'
13	RcvMinPLCntI	RcvMinPLCntI sets to logic one when the receive minimum packet length error counter (register R_MINPLECNT) rolls over. This interrupt bit clears automatically when this register is read.	R	'0'
12	RcvByteCntI	RcvByteCntI sets to logic one when the receive byte counter (register R_BYTECNT) rolls over. This interrupt bit clears automatically when this register is read.	R	'0'
11	RcvFrmCntI	RcvFrmCntI sets to logic one when the receive frame counter (register R_FRMCNT) rolls over. This interrupt bit clears automatically when this register is read.	R	'0'

Bit	Name	Description	Type	Default
10	RcvAbortCntI	RcvAbortCntI sets to logic one when the receive aborted frame counter (register R_AFCNT) rolls over. This interrupt bit clears automatically when this register is read.	R	'0'
9	RcvFCSCntI	RcvFCSCntI sets to logic one when the receive FCS error counter (register R_FCSECNT) rolls over. This interrupt bit clears automatically when this register is read.	R	'0'
8	RcvFifoOFCntI	RcvFifoOFCntI sets to logic one when the receive POS FIFO overflow counter (register R_PFOCNT) rolls over. This interrupt bit clears automatically when this register is read.	R	'0'
7	RcvSFI	RcvSFI sets to one when a frame is discarded because it is too short according to the receiver POS processor configuration.	R	'0'
6	RcvMaxPLI	RcvMaxPLI sets to logic one when a packet exceeding the programmable maximum packet length (register R_MAXPL) is received. This interrupt bit clears automatically when this register is read.	R	'0'
5	RcvMinPLI	RcvMinPLI sets to logic one when a packet smaller than the programmable minimum packet length (register R_MINPL) is received. This interrupt bit clears automatically when this register is read.	R	'0'
4	RcvDblEscI	RcvDblEscI sets to one when a Control Escape character pair is received.	R	'0'
3	RcvACI	RcvACI sets to logic one when an HDLC frame with Address and Control fields different than FFH and 03H is received. This interrupt bit clears automatically when this register is read.	R	'0'
2	RcvAbortI	RcvAbortI sets to logic one when an HDLC frame finished with an Abort sequence is received. When a frame is aborted, the packet is marked in the FIFO as errored. This interrupt bit clears automatically when this register is read.	R	'0'
1	RcvFCSI	RcvFCSI sets to logic one when an HDLC frame with an FCS error is received. When a frame contains an FCS error, the packet is marked in the FIFO as errored. This interrupt bit clears automatically when this register is read.	R	'0'
0	RcvFifoOFI	RcvFifoOFI sets to logic one when a receive FIFO overflow occurs. If the overflow condition occurs when the receive HDLC controller attempted to write a word of a packet partially received (not the first word), the incomplete packet is marked in the FIFO as errored and the writings to the FIFO are stopped until a new start of packet is received. If the overflow condition occurs when the receive HDLC controller attempted to write the first word of a packet, then nothing is written into the FIFO i.e., the receive FIFO is not modified. This interrupt bit clears automatically when this register is read.	R	'0'

11.13.12 R_POSINTEN—Receive POS Interrupt Enable ((1cc)70H)

Bit	Name	Description	Type	Default
15	Unused			
14	RcvMaxPLCntlEn	Active-high enable for the RcvMaxPLCntl interrupt bit.	R/W	'0'
13	RcvMinPLCntlEn	Active-high enable for the RcvMinPLCntl interrupt bit.	R/W	'0'
12	RcvByteCntlEn	Active-high enable for the RcvByteCntl interrupt bit.	R/W	'0'
11	RcvFrmCntlEn	Active-high enable for the RcvFrmCntl interrupt bit.	R/W	'0'
10	RcvAbortCntlEn	Active-high enable for the RcvAbortCntl interrupt bit.	R/W	'0'
9	RcvFCSCntlEn	Active-high enable for the RcvFCSCntl interrupt bit.	R/W	'0'
8	RcvFifoOFCntlEn	Active-high enable for the RcvFifoOFCntl interrupt bit.	R/W	'0'
7	RcvSFIEn	Active-high enable for the RcvSFI interrupt bit.	R/W	'0'
6	RcvMaxPLIEn	Active-high enable for the RcvMaxPLI interrupt bit.	R/W	'0'
5	RcvMinPLIEn	Active-high enable for the RcvMinPLI interrupt bit.	R/W	'0'
4	RcvDblEscIEn	Active-high enable for the RcvDblEscI interrupt bit.	R/W	'0'
3	RcvACIEn	Active-high enable for the RcvACI interrupt bit.	R/W	'0'
2	RcvAbortIEn	Active-high enable for the RcvAbortI interrupt bit.	R/W	'0'
1	RcvFCSIEn	Active-high enable for the RcvFCSI interrupt bit.	R/W	'0'
0	RcvFifoOFIEn	Active-high enable for the RcvFifoOFI interrupt bit.	R/W	'0'

11.14 POS Transmit Channel Registers

11.14.1 T_PHCCNF—Transmit POS HDLC Controller Configuration ((1cc)40H)

Bit	Name	Description	Type	Default
15:9	Unused			
8	XmtTrScrEn	XmtTrScrEn enables the scrambling of user data before passing it through the byte stuffing process.The self-synchronous scrambler uses the polynomial $X^{48} + X^{28} + X^{27} + 1$: '0' = The scrambler is disabled. '1' = The scrambler is enabled.	R/W	'0'
7	XmtFifEn	XmtFifEn configures the behavior of the transmit POS processor when there is a FIFO underflow: '0' = The frame is aborted if there is a FIFO underflow. '1' = The frame is filled with Control Escape character pairs during FIFO underflows.	R/W	'0'

Bit	Name	Description	Type	Default
6	XmtReadEn	XmtReadEn disables the reading of POS-packets from the transmit FIFO: '0' = The transmit HDLC controller does not read packets from the transmit FIFO (even if the FIFO contains data) and maps Flag characters into the SPE. '1' = The transmit HDLC controller operates normally, reading packets from the transmit FIFO (if the FIFO contains data). XmtReadEn should not be used for transmit Flow Control. Register T_IPGCTRL offers a better way to do that.	R/W	'1'
5	XmtFCSErrCnf	XmtFCSErrCnf configures how XmtFCSErr is used (see below). '0' = If XmtFCSErr = 1, the next HDLC frame is transmitted with an error i.e., the FCS field (if used) is inverted prior to transmission. After inserting the FCS error, XmtFCSErr automatically resets. '1' = If XmtFCSErr = 1, **all** the HDLC frames are transmitted with an FCS error i.e., the FCS field (if used) is inverted prior to transmission. In this configuration, XmtFCSErr must be set to logic zero manually.	R/W	'0'
4	XmtFCSErr	XmtFCSErr controls the insertion of FCS errors into the transmitted HDLC frames. '0' = Normal Operation (default) XmtFCSErrCnf is Don't Care '1' = See the description in XmtFCSErrCnf.	R/W	'0'
3:2	XmtFCSCnf[1:0]	XmtFCSCnf[1:0] selects the type of Frame Check Sequence (FCS) inserted in the transmitted frames: **XmtFCSCnf[1:0] — # FLAGs** '00' — None '01' — Reserved '10' — CRC-16 (CRC-CCITT) '11' — CRC-32	R/W	'11'
1	XmtACPass	XmtACPass configures transmission of the HDLC Address and Control fields: '0' = The transmit HDLC controller generates the HDLC Address and Control fields. The Link Layer device writes into the transmit FIFO only the HDLC information field (PPP frames). '1' = The transmit HDLC does not generate the HDLC Address and Control fields. The Link Layer device writes into the transmit FIFO the HDLC Address, Control and Information field. The transmit HDLC controller transmits the HDLC Address and Control fields stored into the FIFO.	R/W	'1'
0	XmtScrEn	XmtScrEn controls the scrambling of the HDLC frames (the SONET/SDH SPE) by using the self-synchronous scrambler $1 + X^{43}$. '0' = The scrambler is disabled. '1' = The scrambler is enabled.	R/W	'1'

11.14.2 T_IPGCTRL—Transmit Interpacket Gap Control (Tx Flow Control) ((1cc)41H)

Bit	Name	Description	Type	Default
15	Unused			
14	XmtIPGRelEn	XmtIPGRelEn enables the insertion of interframe filling Flag characters to reduce the HDLC transmit rate: '0' = The transmit HDLC controller operates normally. '1' = The number of Flag characters inserted after an HDLC frame is proportional to the "length of the frame" (L), modified as indicated by XmtIPGRelCnf and XmtIPGRel[2:0] (see Table 28 and Table 29).	R/W	'0'
13	XmtIPGRelCnf	XmtIPGRelCnf configures how XmtIPGRel[2:0] are used to calculate the number of Flag characters. '0' = Divide length by XmtIPGRel[2:0] value. '1' = Multiply length by XmtIPGRel[2:0] value.	R/W	'0'
12:10	XmtIPGRel[2:0]	XmtIPGRel[2:0] configures the number of Flag characters to insert between consecutive HDLC frames as a function of the transmitted frame length (see Table 28 and Table 29).	R/W	'01'
9	XmtIPGAbsEn	XmtIPGAbsEn enables the insertion of interframe filling Flag characters to ensure a minimum number of Flag characters between consecutive HDLC frames: '0' = The transmit HDLC controller operates normally. '1' = The number of Flag characters inserted after an HDLC frame is a constant value indicated by XmtIPGAbsCnf and XmtIPGAbs[7:0] (see Table 30 and Table 31).	R/W	'0'
8	XmtIPGAbsCnf	This is the multiplier value used on the XmtIPGAbs[7:0] field: If 0, the value of XmtIPGAbs[7:0] is multiplied by 1. If 1, the value of XmtIPGAbs[7:0] is multiplied by 256.	R/W	'0'
7:0	XmtIPGAbs[7:0]	XmtIPGAbs[7:0] configures the number of Flag characters to insert between consecutive HDLC frames (see Table 30 and Table 31).	R/W	01H

Intel IXF6048 controls the interpacket gap (the number of Flag characters transmitted between consecutive HDLC frames) using two different methods. The interpacket gap is generated according to these rules:

- If any method is enabled, the minimum interpacket gap is one Flag.
- If one or both methods are enabled, the interpacket gap is max{1, m1, m2}, where m1 is the number of Flag characters calculated by the first method and m2 is the number of Flag characters calculated by the second method.

11.14.2.1 XmtIPGRelEn = '1' (Method 1)

XmtIPGRelEn = '1' enables the first method. This method limits the frame transmission rate by inserting a number of Flag characters (between two consecutive frames) proportional to the length of the transmitted frames. Every time a frame is transmitted, the HDLC controller transmits a number of Flag characters proportional to the length of the frame. The number of transmitted Flag characters is calculated by multiplying (XmtIPGRelCnf = '1') or by dividing (XmtIPGRelCnf = '0')

the frame length ‘L’ by 2 ** XmtIPGRel[2:0] (1, 2, 4, 8, 16, 32, 64, or 128). Table 28 and Table 29 show the number of transmitted Flag characters after a frame of size ‘L’ as a function of XmtIPGRel[2:0]

Table 28. HDLC Flow Control Using XmtIPGRelEn = '1' and XmtIPGRelCnf = '0'

XmtIPGRel[2:0]	Number of Flags
'000'	max{1, L}
'001'	max{1, L ÷ 2}
'010'	max{1, L ÷ 4}
'011'	max{1, L ÷ 8}
'100'	max{1, L ÷ 16}
'101'	max{1, L ÷ 32}
'110'	max{1, L ÷ 64}
'111'	max{1, L ÷ 128}

Table 29. HDLC Flow Control Using XmtIPGRelEn = '1' and XmtIPGRelCnf = '1'

XmtIPGRel[2:0]	Number of Flags
'000'	L
'001'	L × 2
'010'	L × 4
'011'	L × 8
'100'	L × 16
'101'	L × 32
'110'	L × 64
'111'	L × 128

Control Escape characters inserted during the byte stuffing process are considered to act as flags for flow control purposes. Thus, the number of Control Escape characters inserted is subtracted from the number of flags shown in Table 28–Table 29 in order to calculate the number of flags finally sent.

11.14.2.2 XmtIPGAbsEn = '1' (Method 2)

XmtIPGAbsEn = '1' enables the second method. This method limits the frame transmission rate by inserting a fixed number of Flag characters between consecutive frames.

- When XmtIPGAbsCnf = '0', XmtIPGAbs[7:0] controls the interpacket length in the range 1 to 256. XmtIPGAbs[7:0] contains the number of Flag characters to be inserted between consecutive frames. If XmtIPGap[7:0] = 00H, the HDLC controller inserts 256 FLAG characters between consecutive frames.
- When XmtIPGAbsCnf = '1', XmtIPGAbs[7:0] controls the interpacket length in the range 256 to 65536. The number of Flag characters inserted between consecutive frames is

XmtIPGAbs[7:0] multiplied by 256. If XmtIPGAbs[7:0] are set to 00H, the HDLC controller inserts 65536 Flag characters between consecutive frames.

Table 30. HDLC Flow Control Using XmtIPGAbsEn = '1' and XmtIPGAbsCnf = '0'

XmtIPGAbs[7:0]	0	1	2	3	4	…	255
Number of FLAGs	256	1	2	3	4	…	255

Table 31. HDLC Flow Control Using XmtIPGAbsEn = '1' and XmtIPGAbsCnf = '1'

XmtIPGAbs[7:0]	0	1	2	3	4	…	255
Number of FLAGs	65536	256	512	768	1024	…	65280

11.14.3 T_FRMCNT—Transmit Frame Counter ((1cc)43H-(1cc)42H)

(1cc)43H = Bits[26:16], (1cc)42H = Bits[15:0]

Bit	Name	Description	Type	Default
31:27	Unused			
26:0	XmtFrmCnt[26:0]	XmtFrmCnt[26:0] counts the number of packets read from the transmit FIFO and transmitted into HDLC frames during the last accumulation interval. XmtFrmCnt[26:0] does not count the aborted HDLC frames. A write to the counter (address (1cc)43H) causes the entire counter to be loaded into a buffer and then cleared. The contents of the buffer can then be read.	R	00H

11.14.4 T_BYTECNT—Transmit Byte Counter ((1cc)45H-(1cc)44H)

(1cc)45H = Bits[31:16], (1cc)44H = Bits[15:0]

Bit	Name	Description	Type	Default
31:29	Unused			
28:0	XmtByteCnt[28:0]	XmtByteCnt[28:0] counts the number of bytes read from the transmit FIFO and inserted into the transmitted HDLC frames during the last accumulation interval. A write to the counter (address (1cc)45H) causes the entire counter to be loaded into a buffer and then cleared. The contents of the buffer can then be read.	R	00H

11.14.5 T_AFCNT—Transmit Aborted Frame Counter ((1cc)47H-(1cc)46H)

(1cc)47H = Bits[19:16], (1cc)46H = Bits[15:0]

Bit	Name	Description	Type	Default
31:20	Unused			
19:0	XmtUAFrmCnt[19:0]	XmtAFrmCnt[19:0] counts the number of HDLC frames aborted by the Link Layer device (by asserting the TXERR input) during the last accumulation interval. These frames are mapped in the SONET/SDH SPE and are finished with an ABORT sequence. A write to the counter (address (1cc)47H) causes the entire counter to be loaded into a buffer and then cleared. The contents of the buffer can then be read.	R	00H

11.14.6 T_PFUCNT—Transmit Packet FIFO Underflow Counter ((1cc)48H)

Bit	Name	Description	Type	Default
15:0	XmtFifoUFCnt[15:0]	XmtFifoUFCnt[15:0] counts the number of HDLC frames that have been aborted by the transmit HDLC controller due to a FIFO under-run during the last accumulation interval. These frames are mapped in the SONET/SDH SPE and are finished with an ABORT sequence. A write to the counter (address (1cc)48H) causes the entire counter to be loaded into a buffer and then cleared. The contents of the buffer can then be read.	R	00H

11.14.7 T_POSINT—Transmit POS Interrupt Register ((1cc)49H)

Bit	Name	Description	Type	Default
15:7	Unused			
6	XmtByteCntI	XmtByteCntI sets to logic one when the “transmit byte counter” (register T_BYTECNT) rolls over. This interrupt bit clears automatically when this register is read.	R	'0'
5	XmtFrmCntI	XmtFrmCntI sets to logic one when the “transmit frame counter” (register T_FRMCNT) rolls over. This interrupt bit clears automatically when this register is read.	R	'0'
4	XmtAbortCntI	XmtAbortCntI sets to logic one when the “transmit aborted frame counter” (register T_AFCNT) rolls over. This interrupt bit clears automatically when this register is read.	R	'0'
3	XmtFifoUFCntI	XmtFifoUFCntI sets to logic one when the “transmit FIFO underflow counter” (register T_FUFCNT) rolls over. This interrupt bit clears automatically when this register is read.	R	'0'

Bit	Name	Description	Type	Default
2	XmtAbortI	XmtAbortI sets to logic one when a packet is aborted by the Link Layer device by using the TXERR input. This interrupt bit clears automatically when this register is read.	R	'0'
1	XmtFCSI	XmtFCSI sets to logic one when an FCS error is inserted into a packet This interrupt bit clears automatically when this register is read.	R	'0'
0	XmtFifoUFI	XmtFifoUFI sets to logic one when a transmit FIFO underflow occurs when reading a word of a partially transmitted packet (not the first word). When a FIFO underflow occurs, the incompletely transmitted packet is aborted (finished with an Abort sequence). Then the contents of the transmit FIFO is read and ignored until a new start of packet is read from the FIFO. This interrupt bit clears automatically when this register is read.	R	'0'

11.14.8 T_POSINTEN—Transmit POS Interrupt Enable ((1cc)4AH)

Bit	Name	Description	Type	Default
15:7	Unused			
6	XmtByteCntIEn	Active-high enable for the XmtByteCntI interrupt bit.	R/W	'0'
5	XmtFrmCntIEn	Active-high enable for the XmtFrmCntI interrupt bit.	R/W	'0'
4	XmtAbortCntIEn	Active-high enable for the XmtAbortCntI interrupt bit.	R/W	'0'
3	XmtFifoUFCntIEn	Active-high enable for the XmtFifoUFCntI interrupt bit.	R/W	'0'
2	XmtAbortIEn	Active-high enable for the XmtAbortI interrupt bit.	R/W	'0'
1	XmtFCSIEn	Active-high enable for the XmtFCSI interrupt bit.	R/W	'0'
0	XmtFifoUFIEn	Active-high enable for the XmtFifoUFI interrupt bit.	R/W	'0'

12.0 Test Specifications

Table 32. Absolute Maximum Ratings

Parameter	Symbol	Min	Max	Unit
Supply Voltage for Core (reference to ground[1])	VDD_CORE	-0.3	+4.0	V
Supply Voltage for TTL I/O (reference to ground[1])	VDD_TTL	-0.3	+4.0	V
Supply Voltage for PECL I/O (reference to ground[1])	VDD_PECL	-0.3	+4.0	V
Input Voltage on any pin (reference to ground[1])	-	-0.3	VDD_IO + 0.3	V
Storage temperature	TSTOR	-65	+150	°C
Junction Temperature	TJ	-65	+150	°C
NOTES: 1. GND_CORE = 0 V; GND_TTL = 0 V; GND_PECL = 0 V				
Caution: Exceeding these values may cause permanent damage. **Caution:** Functional operation under these conditions is not implied. **Caution:** Exposure to maximum rating conditions for extended periods may affect device reliability.				

Table 33. Recommended Operating Conditions

Parameter	Symbol	Min	Typ[1]	Max	Unit
Ambient Operating Temperature	TA	-40	25	+85	°C
Supply Voltage for Core (reference to ground[1])	VDD_CORE	2.25	2.5	2.75	V
Supply Voltage for TTL I/O (reference to ground[1])	VDD_TTL	2.97	3.3	3.63	V
Supply Voltage for PECL I/O (reference to ground[1])	VDD_PECL	2.97	3.3	3.63	V
NOTES: 1. GND_CORE = 0 V; GND_TTL = 0 V; GND_PECL = 0 V					

Table 34. DC Electrical Characteristics (Sheet 1 of 3)

Parameter	Symbol	Min	Typ	Max	Units	Test Conditions
Supply Current	ICC	-	TBD	TBD	mA	
TTL Input Low Voltage[1]	VIL_TTL	-	-	0.8	V	VDD_TTL = 3.3V ±10%
TTL Input High Voltage[1]	VIH_TTL	2.0	-	-	V	VDD_TTL = 3.3V ±10%
PECL Input Low Voltage	VIL_PECL	VDD_PECL-2.0	-	VDD_PECL-1.54	V	VDD_PECL = 3.3V ±10% 50Ω to VDD_PECL-2V
PECL Input High Voltage	VIH_PECL	VDD_PECL-1.1	-	VDD_PECL-0.7	V	VDD_PECL = 3.3V ±10% 50Ω to VDD_PECL-2V
NOTES: 1. The UTOPIA interface uses the TTL values. 2. Applies to pins when configured as inputs 3. Applies to pins when tristated 4. VDD_CORE = 2.75V; VDD_TTL = VDD_PECL = 3.63						

Table 34. DC Electrical Characteristics (Sheet 2 of 3)

Parameter	Symbol	Min	Typ	Max	Units	Test Conditions
PECL Input Differential Voltage	VID_PECL	0.2	-	-	V	VDD_PECL = 3.3V ±10% 50Ω to VDD_PECL-2V
TTL Output Low Voltage[1]	VOL_TTL	-	-	0.4	V	VDD_TTL = 3.3V ±10%
TTL Output High Voltage[1]	VOH_TTL	2.4	-	-	V	VDD_TTL = 3.3V ±10%
PECL Output Low Voltage	VOL_PECL	-	-	VDD_PECL-1.6	V	VDD_PECL = 3.3V ±10% 50Ω to VDD_PECL-2V
PECL Output High Voltage	VOH_PECL	VDD_PECL-1.1	-	-	V	VDD_PECL = 3.3V ±10% 50Ω to VDD_PECL-2V
PECL Output Differential Voltage	VOD_PECL	0.75	-	-	V	VDD_PECL = 3.3V ±10% 50Ω to VDD_PECL-2V
Input Leakage current[2]	IIL	-	-	±50	uA	VIN = VDD_TTL = 3.6V
Tristate Leakage current[3] (no pull up)	ITOL	-	-	±30	uA	VIN = VDD_TTL or GND_TTL, VDD_TTL = 3.6V, No pull up
Operating Current Core (ATM mode)	IDDOP_ATM1	-		325 (See Note 4)	mA	Single OC-48c ATM 16-bit PECL line and 32-bit UTOPIA @ 104 MHz
	IDDOP_ATM2	-		349 (See Note 4)	mA	Quad OC-12c ATM 4 x 8-bit TTL line and 32-bit UTOPIA @ 104 MHz
	IDDOP_ATM3	-		156 (See Note 4)	mA	Single OC-12c ATM 8-bit TTL line and 16-bit UTOPIA @ 50 MHz
Operating Current Core (POS mode)	IDDOP_POS1	-		357 (See Note 4)	mA	Single OC-48c POS 16-bit PECL line and 32-bit UTOPIA @ 104 MHz
	IDDOP_POS2	-		383 (See Note 4)	mA	Quad OC-12c POS 4 x 8-bit TTL line and 32-bit UTOPIA @ 104 MHz
	IDDOP_POS3	-		156 (See Note 4)	mA	Single OC-12c POS 8-bit TTL line and 16-bit UTOPIA @ 50 MHz

NOTES:
1. The UTOPIA interface uses the TTL values.
2. Applies to pins when configured as inputs
3. Applies to pins when tristated
4. VDD_CORE = 2.75V; VDD_TTL = VDD_PECL = 3.63

Table 34. DC Electrical Characteristics (Sheet 3 of 3)

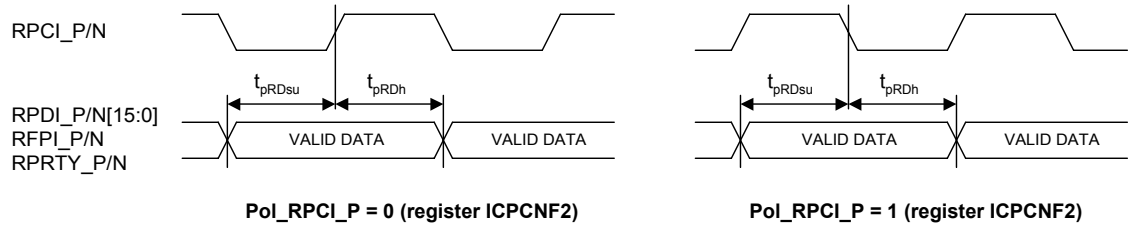
Parameter	Symbol	Min	Typ	Max	Units	Test Conditions
Operating Current I/O Outputs loaded	IDDIO_1	-		773 (See Note 4)	mA	Single OC-48c ATM/ POS 16-bit PECL line and 32-bit UTOPIA @ 104 MHz 50Ω PECL Line Termination to VDD_PECL-2V
	IDDIO_2	-		206 (See Note 4)	mA	Quad OC-12c ATM/ POS 4 x 8-bit TTL line and 32-bit UTOPIA @ 104 MHz
	IDDIO_3	-		73 (See Note 4)	mA	Single OC-12c ATM/ POS 8-bit TTL line and 16-bit UTOPIA @ 50 MHz

NOTES:
1. The UTOPIA interface uses the TTL values.
2. Applies to pins when configured as inputs
3. Applies to pins when tristated
4. VDD_CORE = 2.75V; VDD_TTL = VDD_PECL = 3.63

Note: Minimum and maximum timing values are guaranteed by design and other correlation methods and only a small subset of them are subject to production testing.

Note: All timing parameters assume that the LVTTL outputs for the POS-UTOPIA/UTOPIA interface have a 25 pF load (as per the ATM forum specification) and the rest of the LVTTL outputs have a 50 pF load unless otherwise noted. The minimum and maximum test load is 50 pF.

Figure 78. Receive 16-bit Differential PECL Line Side Interface Timings



PoI_RPCI_P = 0 (register ICPCNF2) **PoI_RPCI_P = 1 (register ICPCNF2)**

Figure 79. Transmit 16-Bit Differential PECL Line Side Interface Timings

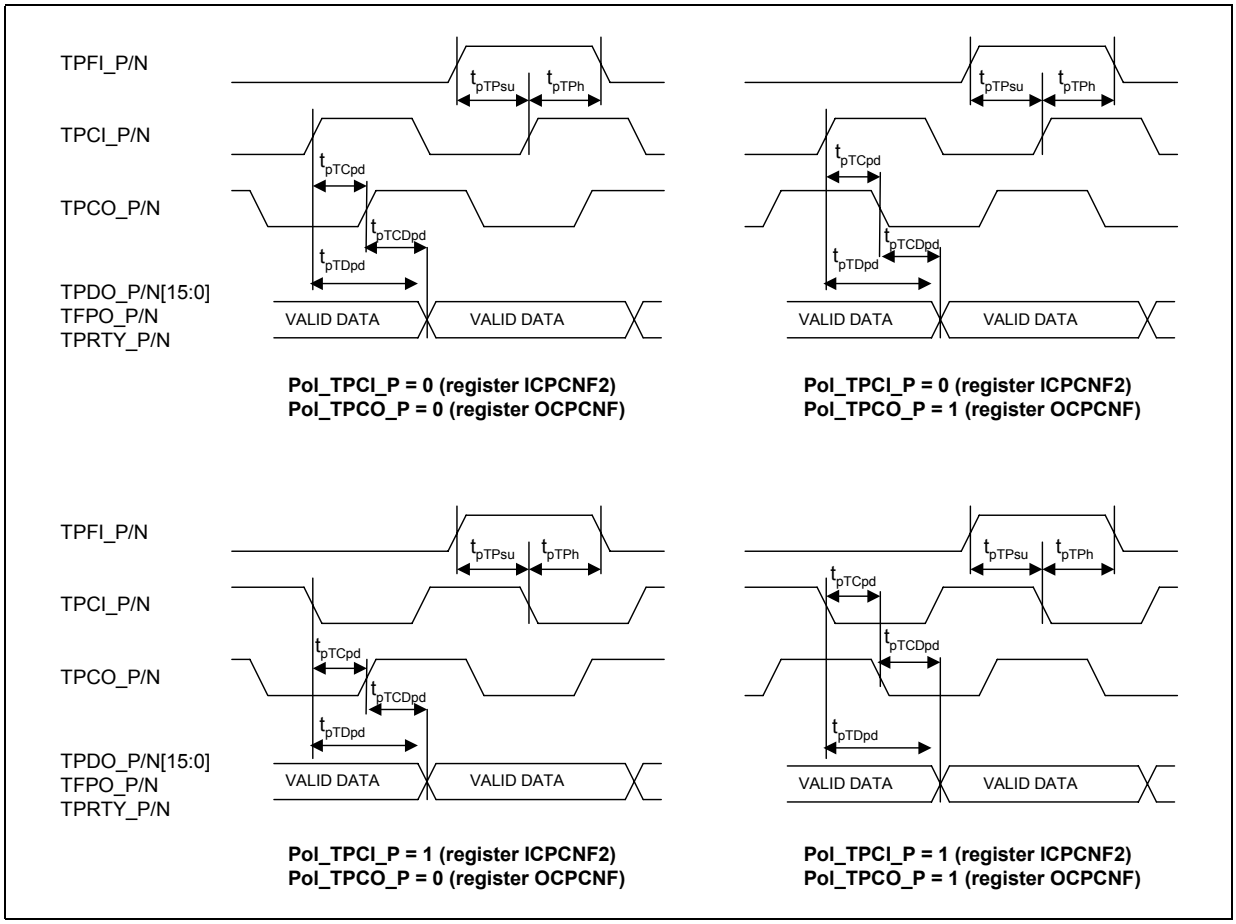


Table 35. Receive 16-Bit Differential PECL Line Side Interface Timings

Parameter	Symbol	Min	Typ	Max	Unit
RPDI_P/N[15:0], RFPI_P/N and RPRTY_P/N setup time to RPCI_P/N rising (falling)[1] edge.	t_{pRDsu}	1.25			ns
RPDI_P/N[15:0], RFPI_P/N and RPRTY_P/N hold time from RPCI_P/N rising (falling)[1] edge.	t_{pRDh}	1.25			ns
RPCI_P/N duty cycle.		40		60	%

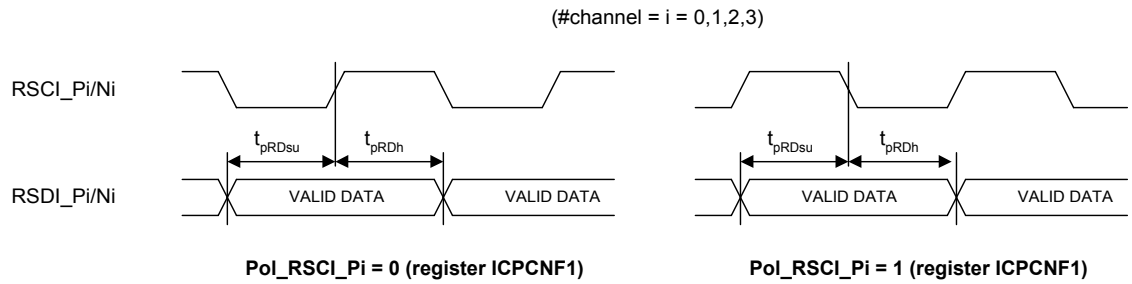
NOTES:
1. RPCI_P/N polarity is configured in global register ICPCNF2.

Table 36. Transmit 16-Bit Differential PECL Line Side Interface Timings

Parameter	Symbol	Min	Typ	Max	Unit
TPCI_P/N to TPCO_P/N propagation delay	t_{pTCpd}			12	ns
TPCI_P/N rising (falling)[1] edge to valid TPDO_P/N[15:0], TFPO_P/N and TPRTY_P/N propagation delay	t_{pTDpd}			12.5	ns
TPCO_P/N rising (falling)[1] edge to valid TPDO_P/N[15:0], TFPO_P/N and TPRTY_P/N propagation delay	t_{pTCDpd}	-1.5		1.5	ns
TFPI_P/N setup time to TPCI_P/N rising (falling)[1] edge.	t_{pTPsu}	1.25			ns
TFPI_P/N hold time to TPCI_P/N rising (falling)[1] edge.	t_{pTPh}	1.25			ns
TPCI_P/N duty cycle		40		60	%

NOTES:
1. TPCI_P/N polarity is configured in global register ICPCNF2.

Figure 80. Receive 1-Bit Differential PECL Line Side Interface Timings



PoI_RSCI_Pi = 0 (register ICPCNF1) **PoI_RSCI_Pi = 1 (register ICPCNF1)**

Figure 81. Transmit 1-bit Differential PECL Line Side Interface Timings

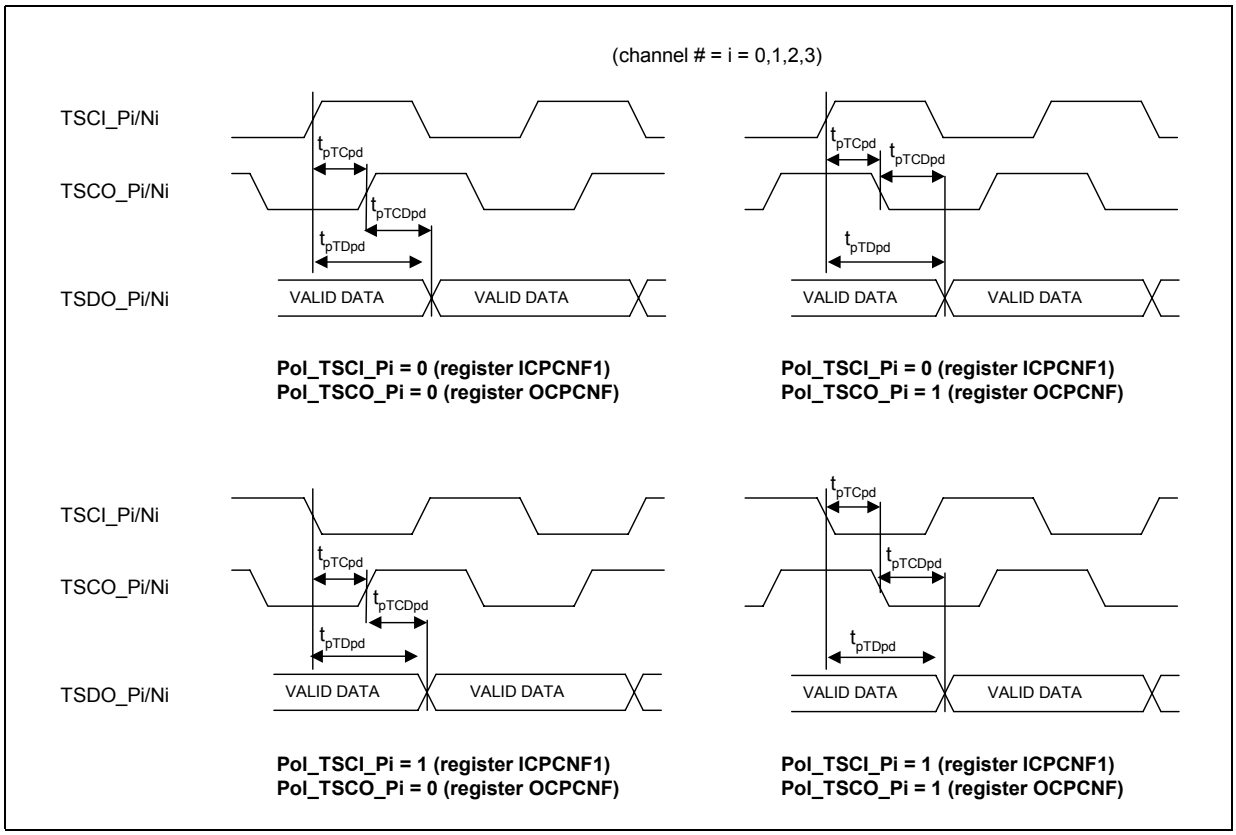


Table 37. Receive 1-Bit Differential PECL Line Side Interface Timings

Parameter	Symbol	Min	Typ	Max	Unit
RSDI_Pi/Ni setup time to RSCI_Pi/Ni rising (falling)[1] edge (i = 0, 1, 2, 3).	t_{pRDsu}	1.25			ns
RSDI_Pi/Ni setup time to RSCI_Pi/Ni rising (falling)[1] edge (i = 0, 1, 2, 3).	t_{pRDh}	1.25			ns
RSCI_Pi/Ni duty cycle (i = 0, 1, 2, 3).		40		60	%

NOTES:
1. RSCI_Pi/Ni (i = 0, 1, 2, 3) polarity is configured in global register ICPCNF1.

Table 38. Transmit 1-Bit Differential PECL Line Side Interface Timings

Parameter	Symbol	Min	Typ	Max	Unit
TSCI_Pi/Ni to TSCO_Pi/Ni propagation delay (i = 0, 1, 2, 3).	t_{pTCpd}			12	ns
TSCI_Pi/Ni rising (falling)[1] edge to valid TSDO_Pi/Ni propagation delay (i = 0, 1, 2, 3).	t_{pTDpd}			12.5	ns
TSCO_Pi/Ni rising (falling)[1] edge to valid TSDO_Pi/Ni propagation delay (i = 0, 1, 2, 3).	t_{pTDCpd}	-1.5		1.8	ns
TSCI_Pi/Ni duty cycle (i = 0, 1, 2, 3).		40		60	%

NOTES:
1. TSCI_Pi/Ni (i = 0, 1, 2, 3) polarity is configured in global register ICPCNF1.

Figure 82. Receive 32-Bit TTL Line Side Interface Timings

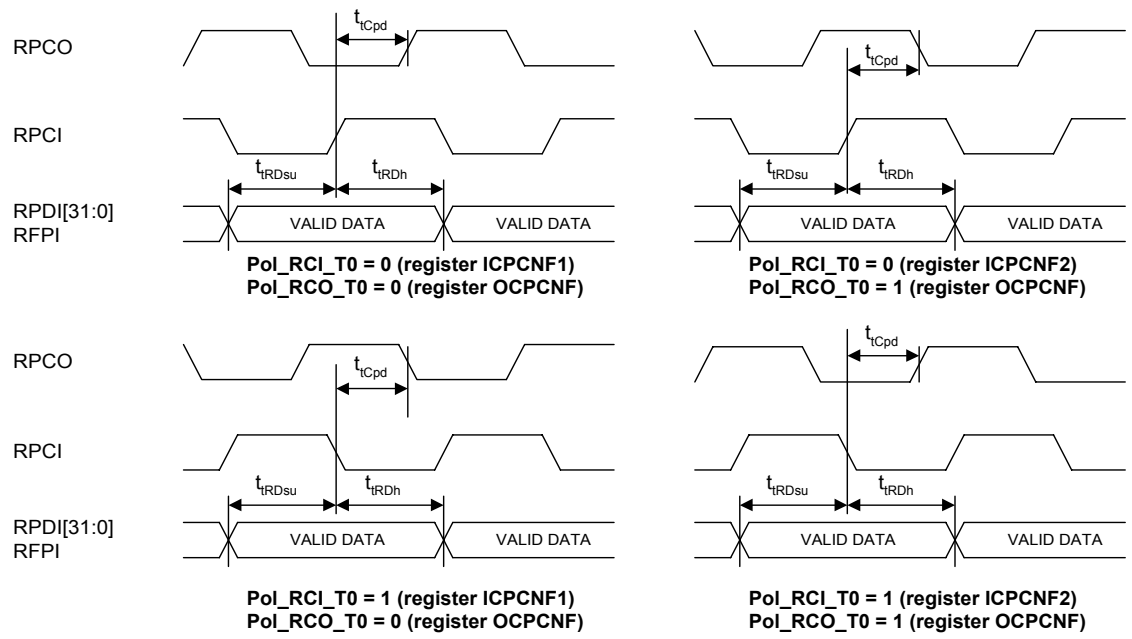


Figure 83. Transmit 32-Bit TTL Line Side Interface Timings

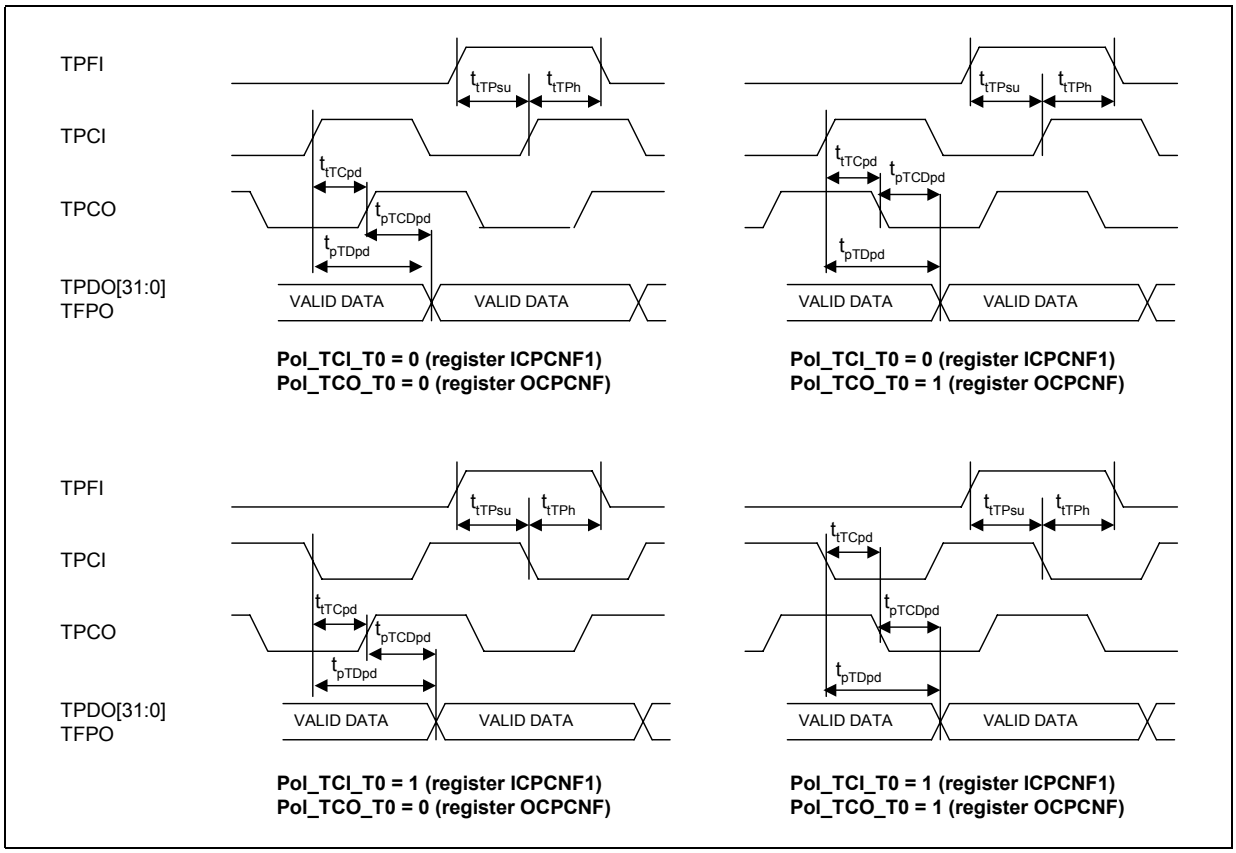


Table 39. Receive 32-Bit TTL Line Side Interface Timings

Parameter	Symbol	Min	Typ	Max	Unit
RPDI[31:0] and RFPI setup time to RPCI rising (falling)[1] edge	t_{tRDsu}	1.25			ns
RPDI[31:0] and RFPI hold time to RPCI rising (falling)[1] edge	t_{tRDh}	1.25			ns
RPCI to RPCO propagation delay	t_{tRCpd}			13.5	ns
RPCI duty cycle		40		60	%

NOTES:
1. RPCI polarity is configured in global register ICPCNF1.

Table 40. Transmit 32-Bit TTL Line Side Interface Timings

Parameter	Symbol	Min	Typ	Max	Unit
TPCI to TPCO propagation delay	t_{tTCpd}			13.5	ns
TPCI rising (falling)[1] edge to valid TPDO[31:0] and TFPO propagation delay	t_{pTDpd}			13.5	ns
TPCO rising (falling)[1] edge to valid TPDO[31:0] and TFPO propagation delay	t_{pTCDpd}	-1.5		1.5	ns
TFPI setup time to TPCI rising (falling)[1] edge	t_{tTPsu}	1.25			ns
TFPI hold time to TPCI_P/N rising (falling)[1] edge	t_{tTPh}	1.25			ns
TPCI duty cycle		40		60	%

NOTES:
1. TPCI polarity is configured in global register ICPCNF1.

Figure 84. Receive 8-Bit TTL Line Side Interface Timings

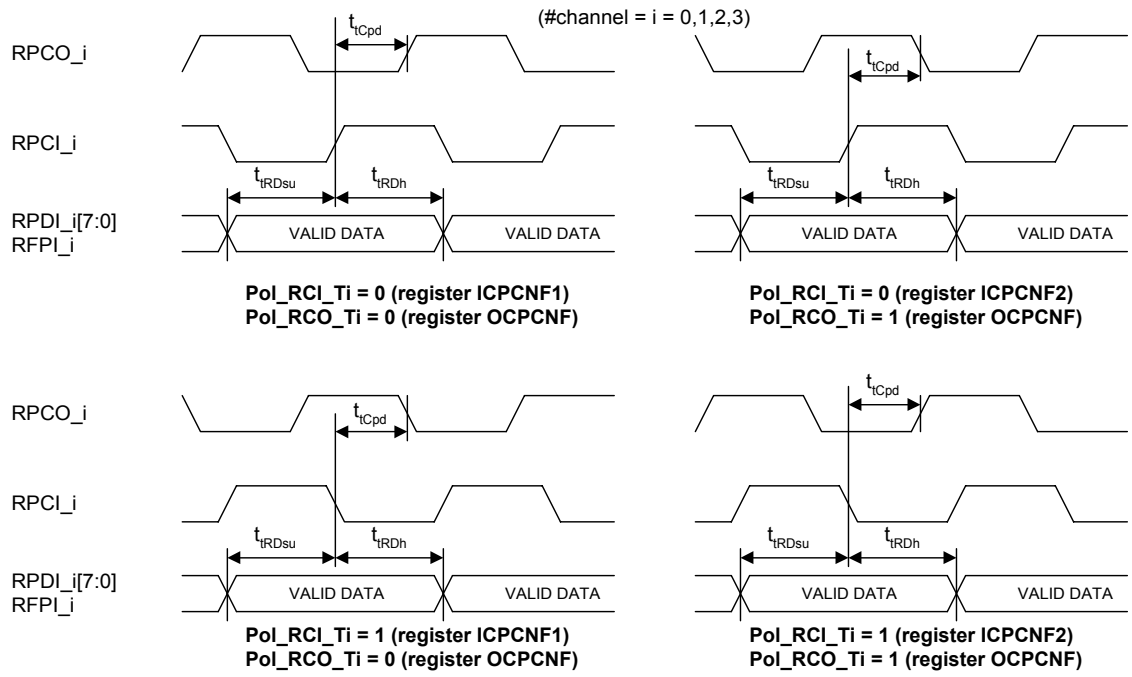


Figure 85. Transmit 8-Bit TTL Line Side Interface Timings

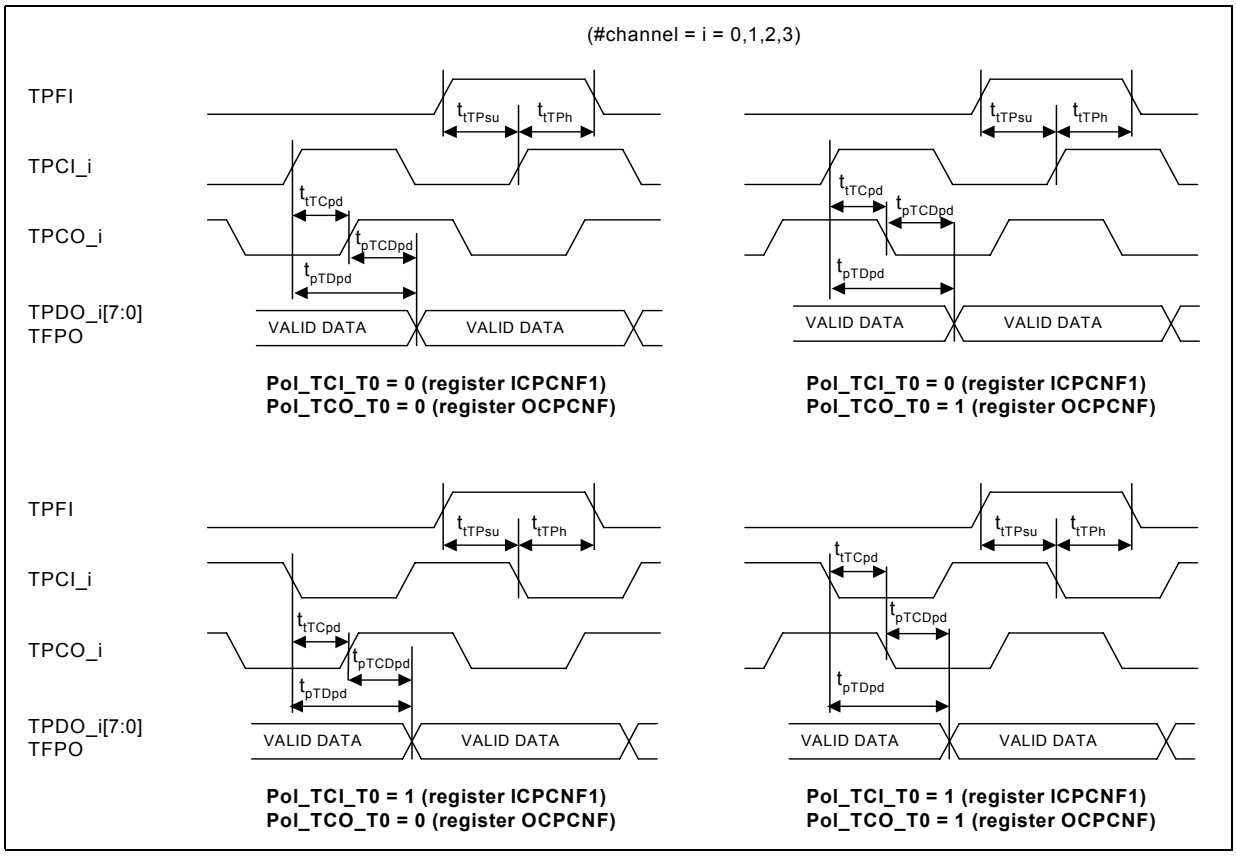


Table 41. Receive 8-Bit TTL Line Side Interface Timings

Parameter	Symbol	Min	Typ	Max	Unit
RPDI_i[7:0] and RFPI_i setup time to RPCI_i rising (falling)[1] edge (i = 0, 1, 2, 3)	t_{tRDsu}	1.25			ns
RPDI_i[7:0] and RFPI_i hold time to RPCI_i rising (falling)[1] edge (i = 0, 1, 2, 3)	t_{tRDh}	1.25			ns
RPCI_i to RPCO_i propagation delay (i = 0, 1, 2, 3)	t_{tRCpd}			13.5	ns
RPCI_i duty cycle (i = 0, 1, 2, 3)		40		60	%

NOTES:
1. RPCI_i (i = 0, 1, 2, 3) polarity is configured in global register ICPCNF1.

Table 42. Transmit 8-Bit TTL Line Side Interface Timings

Parameter	Symbol	Min	Typ	Max	Unit
TPCI_i to TPCO_i propagation delay (i = 0, 1, 2, 3)	t_{tTCpd}			13.5	ns
TPCI_i rising (falling)[1] edge to valid TPDO_i[7:0] (i = 0, 1, 2, 3) and TFPO propagation delay	t_{pTDpd}			13.5	ns
TPCO_i rising (falling)[2] edge to valid TPDO_i[7:0] (i = 0, 1, 2, 3) and TFPO propagation delay	t_{pTCDpd}	-1.5		1.5	ns
TFPI setup time to TPCI_i rising (falling)[1] edge (i = 0, 1, 2, 3)	t_{tTPsu}	1.25			ns
TFPI hold time to TPCI_i rising (falling)[1] edge (i = 0, 1, 2, 3)	t_{tTPh}	1.25			ns
TPCI_i duty cycle (i = 0, 1, 2, 3)		40		60	%

NOTES:
1. TPCI_i (i = 0, 1, 2, 3) polarity is configured in global register ICPCNF1.
2. TPCO_i (i = 0, 1, 2, 3) polarity is configured in global register OCPCNF.

Figure 86. Serial Overhead Timing Diagram

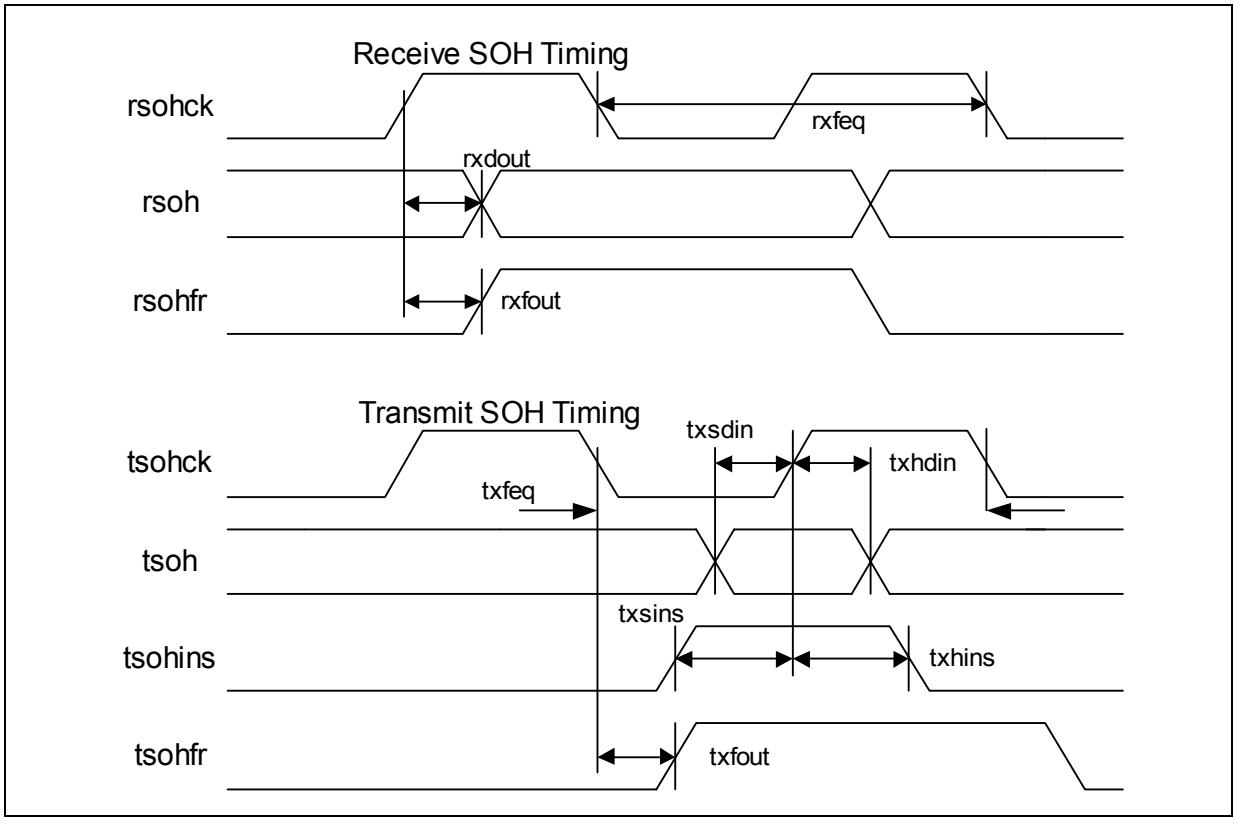


Table 43. Serial Overhead Timing Parameters

Parameter	Symbol	Min	Typ	Max	Unit
RSOHCK frequency	t_{RXFEQ}			21	MHz
RSOH delay time from rising RSOHCK	t_{RXDOUT}			5	ns
RSOHFR delay time from rising RSOHCK	t_{RXFOUT}			5	ns
TSOHCK frequency	t_{TXFEQ}			21	MHz
TSOH setup time required to rising TSOHCK	t_{TXSDIN}	12			ns
TSOH hold time required to rising TSOHCK	t_{TXHDIN}	1			ns
TSOHINS setup time required to rising TSOHCK	t_{TXSINS}	12			ns
TSOHINS hold time required to rising TSOHCK	t_{TXHINS}	1			ns
TSOHFR delay time from falling TSOHCK	t_{TXFOUT}			5	ns

Figure 87. Receive UTOPIA Single Interface Configured for 104 MHz Operation: 32/16/8-Bit Data Bus, Two Clock Cycle Decode-Response Delay and No High-Impedance Outputs

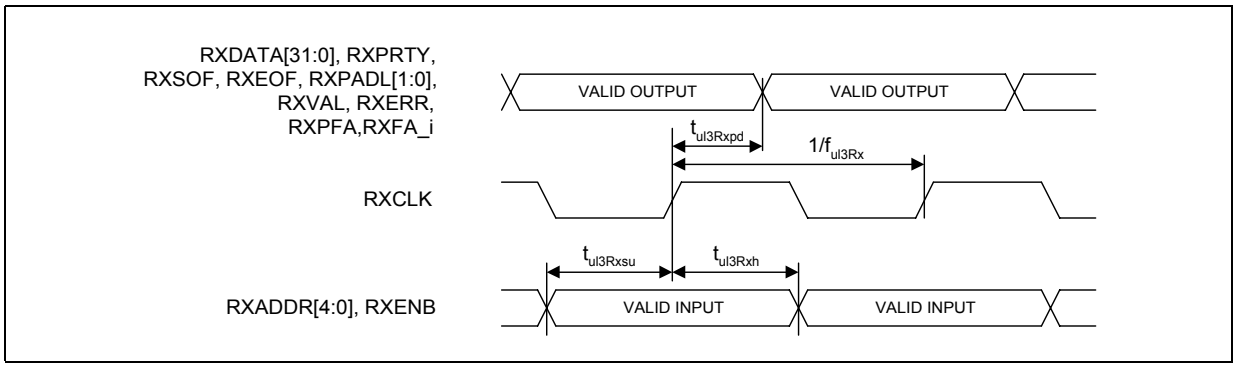


Figure 88. Transmit UTOPIA Single Interface Configured for 104 MHz Operation: 32/16/8-Bit Data Bus, Two Clock Cycle Decode-Response Delay and No High-Impedance Outputs

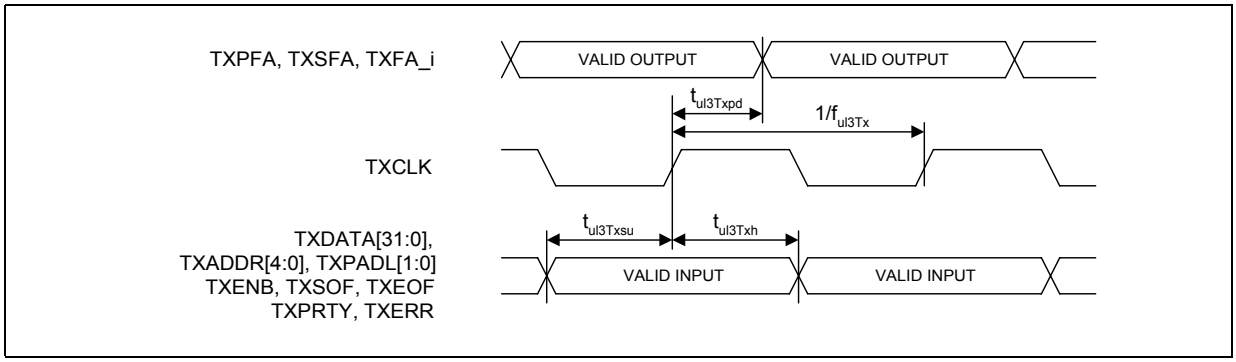


Table 44. Receive UTOPIA Single Interface Timings for the Configurations Supporting 104 MHz Operation: 32/16/8-Bit Wide Data Bus, Two Decode-Response Clock Cycles and No High-Impedance Outputs

Parameter	Symbol	Min	Typ	Max	Unit
RXCLK frequency	f_{ul3Rx}			104	MHz
RXCLK duty cycle	D_{ul3Rx}	30		70	%
RXADDR[4:0] and RXENB setup time to RXCLK	$t_{ul3Rxsu}$	2.0			ns
RXADDR[4:0] and RXENB hold time from RXCLK	t_{ul3Rxh}	0.5			ns
RXCLK rising edge to RXDATA[31:0], RXPRTY, RXSOF, RXEOF, RXPADL[1:0], RXVAL, RXERR, RXPFA, and RXFA_i (i = 0, 1, 2, 3) propagation delay	$t_{ul3Rxpd}$	1		6	ns

Table 45. Transmit UTOPIA Single Interface Timings for the Configurations Supporting 104 MHz Operation: 32/16/8-Bit Wide Data Bus, Two Decode-Response Clock Cycles and No High-Impedance Outputs

Parameter	Symbol	Min	Typ	Max	Unit
TXCLK frequency	f_{ul3Tx}			104	MHz
TXCLK duty cycle	D_{ul3Tx}	30		70	%
TXDATA[31:0], TXADDR[4:0], TXPADL[1:0], TXENB, TXSOF, TXEOF, TXPRTY, and TXERR setup time to TXCLK	$t_{ul3Txsu}$	2.0			ns
TXDATA[31:0], TXADDR[4:0], TXPADL[1:0], TXENB, TXSOF, TXEOF, TXPRTY, and TXERR hold time from TXCLK	t_{ul3Txh}	0.5			ns
TXCLK rising edge to TXPFA, TXSFA, and TXFA_i (i = 0, 1, 2, 3) propagation delay	$t_{ul3Txpd}$	1		6	ns

Figure 89. Receive UTOPIA Quad Interface Configured for 104 MHz Operation: 8-Bit Data Bus, Two Clock Cycle Decode-Response Delay and No High-Impedance Outputs

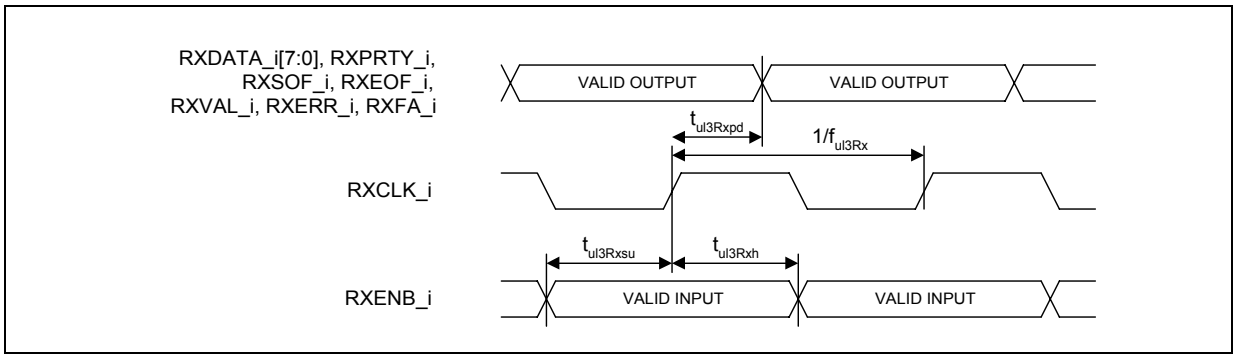


Figure 90. Transmit UTOPIA Quad Interface Configured for 104 MHz Operation: 8-Bit Data Bus, Two Clock Cycle Decode-Response Delay and No High-Impedance Outputs

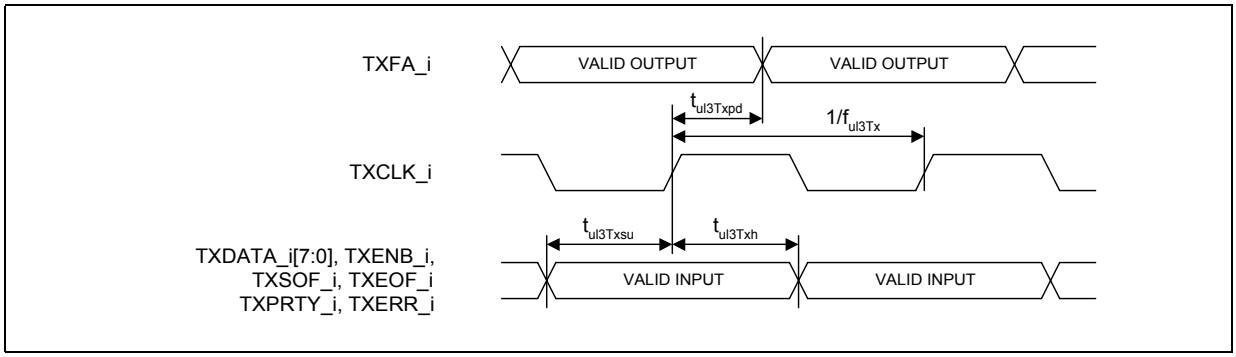


Table 46. Receive UTOPIA Quad Interface Timings for the Configurations Supporting 104 MHz Operation: 8-Bit Wide Data Bus, Two Decode-Response Clock Cycles and No High-Impedance Outputs

Parameter	Symbol	Min	Typ	Max	Unit
RXCLK_i frequency (i = 0, 1, 2, 3)	f_{ul3Rx}			104	MHz
RXCLK_i duty cycle (i = 0, 1, 2, 3)	D_{ul3Rx}	30		70	%
RXENB_i setup time to RXCLK_i (i = 0, 1, 2, 3)	$t_{ul3Rxsu}$	2.0			ns
RXENB_i hold time from RXCLK_i (i = 0, 1, 2, 3)	t_{ul3Rxh}	0.5			ns
RXCLK_i rising edge to RXDATA_i[7:0], RXPRTY_i, RXSOF_i, RXEOF_i, RXVAL_i, RXERR_i, and RXFA_i (i = 0, 1, 2, 3) propagation delay	$t_{ul3Rxpd}$	1		6	ns

Table 47. Transmit UTOPIA Quad Interface Timings for the Configurations Supporting 104 MHz Operation: 8-Bit Wide Data Bus, Two Decode-Response Clock Cycles and No High-Impedance Outputs

Parameter	Symbol	Min	Typ	Max	Unit
TXCLK_i frequency (i = 0, 1, 2, 3)	f_{ul3Tx}			104	MHz
TXCLK_i duty cycle (i = 0, 1, 2, 3)	D_{ul3Tx}	30		70	%
TXDATA_i[7:0], TXENB_i, TXSOF_i, TXEOF_i, TXPRTY_i, and TXERR_i setup time to TXCLK_i (i = 0, 1, 2, 3)	$t_{ul3Txsu}$	2.0			ns
TXDATA_i[7:0], TXENB_i, TXSOF_i, TXEOF_i, TXPRTY_i, and TXERR_i hold time from TXCLK_i (i = 0, 1, 2, 3)	t_{ul3Txh}	0.5			ns
TXCLK_i rising edge to TXFA_i (i = 0, 1, 2, 3) propagation delay	$t_{ul3Txpd}$	1		6	ns

Figure 91. Receive UTOPIA Single Interface Configured for 50 MHz Operation: 64/32/16/8-Bit Data Bus and One/Two Clock Cycle Decode-Response Delay Signals

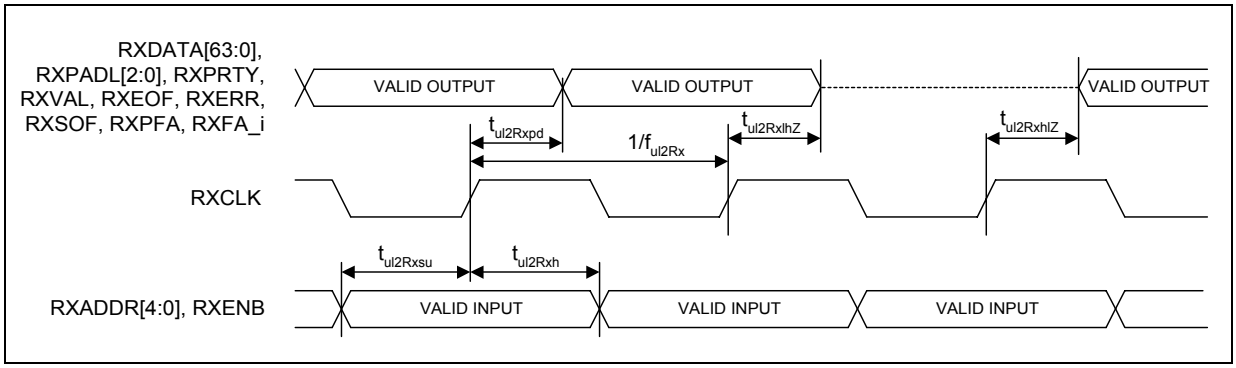


Figure 92. Transmit UTOPIA Single Interface Configured for 50 MHz Operation: 64/32/16/8-Bit Data Bus and One/Two Clock Cycle Decode-Response Delay Signals

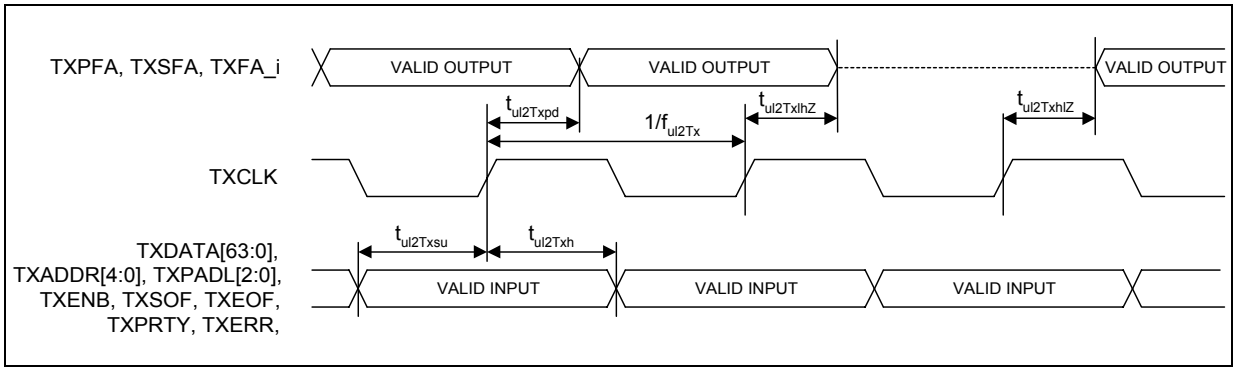


Table 48. Receive UTOPIA Single Interface Timings for the Configurations Supporting 50 MHz Operation: 64/32/16/8-Bit Wide Data Bus, One Decode-Response Clock Cycles or High-Impedance Outputs (Sheet 1 of 2)

Parameter	Symbol	Min	Typ	Max	Unit
RXCLK frequency	f_{ul2Rx}			50	MHz
RXCLK duty cycle	D_{ul2Rx}	30		70	%
RXADDR[4:0] and RXENB setup time to RXCLK	$t_{ul2Rxsu}$	4/5[1]			ns
RXADDR[4:0] and RXENB hold time from RXCLK	t_{ul2Rxh}	1			ns
RXCLK rising edge to RXDATA[63:0], RXPRTY, RXSOF, RXEOF, RXPADL[2:0], RXVAL, RXERR, RXPFA, and RXFA_i (i = 0, 1, 2, 3) propagation delay	$t_{ul2Rxpd}$	1		6	ns
RXCLK rising edge to RXDATA[63:32] propagation delay[2]	$t_{ul2Rxpd}$	1		14	ns

NOTES:
1. In memory mapped mode (RcvSelMode = 1 in register R_UICNF), $t_{ul2Rxsu}$ = 5 ns, otherwise $t_{ul2Rxsu}$ = 4 ns
2. Note that in 64-bit mode $t_{ul2Rxpd}$ is different for RXDATA[63:32]

Table 48. Receive UTOPIA Single Interface Timings for the Configurations Supporting 50 MHz Operation: 64/32/16/8-Bit Wide Data Bus, One Decode-Response Clock Cycles or High-Impedance Outputs (Sheet 2 of 2)

Parameter	Symbol	Min	Typ	Max	Unit
RXCLK rising edge to low-impedance RXDATA[63:0], RXPRTY, RXSOF, RXEOF, RXPADL[2:0], RXVAL, RXERR, RXPFA, and RXFA_i (i = 0, 1, 2, 3)	$t_{ul2RxhlZ}$	1			ns
RXCLK rising edge to high-impedance RXDATA[63:0], RXPRTY, RXSOF, RXEOF, RXPADL[2:0], RXVAL, RXERR, RXPFA, and RXFA_i (i = 0, 1, 2, 3)	$t_{ul2RxlhZ}$			11	ns
RXCLK rising edge to high-impedance RXDATA[63:32][2]	$t_{ul2RxlhZ}$			14	ns

NOTES:
1. In memory mapped mode (RcvSelMode = 1 in register R_UICNF), $t_{ul2Rxsu}$ = 5 ns, otherwise $t_{ul2Rxsu}$ = 4 ns
2. Note that in 64-bit mode $t_{ul2Rxpd}$ is different for RXDATA[63:32]

Table 49. Transmit UTOPIA Single Interface Timings for the Configurations Supporting 50 MHz Operation: 64/32/16/8-Bit Wide Data Bus, One Decode-Response Clock Cycles or High-Impedance Outputs

Parameter	Symbol	Min	Typ	Max	Unit
TXCLK frequency	f_{ul2Tx}			50	MHz
TXCLK duty cycle	D_{ul2Tx}	30		70	%
TXDATA[63:0], TXADDR[4:0], TXPADL[2:0], TXENB, TXSOF, TXEOF, TXPRTY, and TXERR setup time to TXCLK	$t_{ul2Txsu}$	4/5[1]			ns
TXDATA[63:0], TXADDR[4:0], TXPADL[2:0], TXENB, TXSOF, TXEOF, TXPRTY, and TXERR hold time from TXCLK	t_{ul2Txh}	1			ns
TXCLK rising edge to TXPFA, TXSFA, and TXFA_i (i = 0, 1, 2, 3) propagation delay	$t_{ul2Txpd}$	1		6	ns
TXCLK rising edge to low-impedance TXPFA, TXSFA, and TXFA_i (i = 0, 1, 2, 3)	$t_{ul2TxhlZ}$	1			ns
TXCLK rising edge to high-impedance TXPFA, TXSFA, and TXFA_i (i = 0, 1, 2, 3)	$t_{ul2TxlhZ}$			11	ns

NOTES:
1. In memory mapped mode (XmtSelMode = 1 in register T_UICNF), $t_{ul2Txsu}$ = 5 ns, otherwise $t_{ul2Txsu}$ = 4 ns

Figure 93. Receive UTOPIA Quad Interface Configured for 50 MHz Operation: 16/8-Bit Data Bus and One/Two Clock Cycle Decode-Response Delay

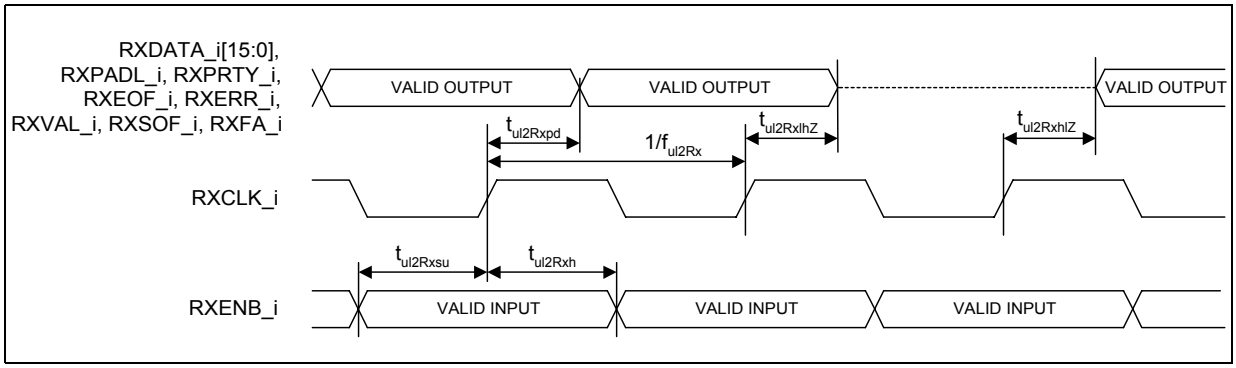


Figure 94. Transmit UTOPIA Quad Interface Configured for 50 MHz Operation: 16/8-Bit Data Bus and One/Two Clock Cycle Decode-Response Delay

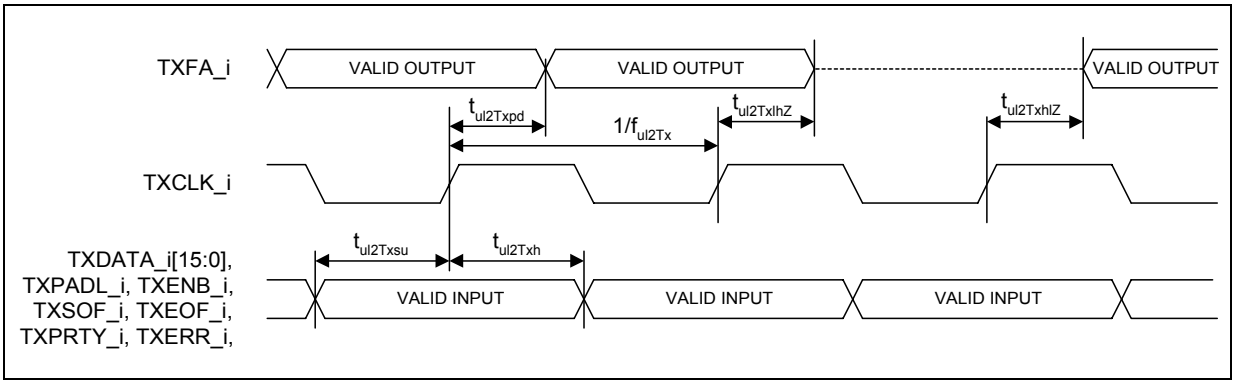


Table 50. Receive UTOPIA Quad Interface Configured for 50 MHz Operation: 16/8-Bit Data Bus and One/Two Clock Cycle Decode-Response Delay

Parameter	Symbol	Min	Typ	Max	Unit
RXCLK_i frequency (i = 0, 1, 2, 3)	f_{ul2Rx}			50	MHz
RXCLK_i duty cycle (i = 0, 1, 2, 3)	D_{ul2Rx}	30		70	%
RXENB_i setup time to RXCLK_i (i = 0, 1, 2, 3)	$t_{ul2Rxsu}$	4/5[1]			ns
RXENB_i hold time from RXCLK_i (i = 0, 1, 2, 3)	t_{ul2Rxh}	1			ns
RXCLK_i rising edge to RXDATA_i[7:0], RXPRTY_i, RXSOF_i, RXEOF_i, RXPADL_i, RXVAL_i, RXERR_i, and RXFA_i (i = 0, 1, 2, 3) propagation delay	$t_{ul2Rxpd}$	1		6	ns
RXCLK_i rising edge to RXDATA_i[15:0] (i = 0, 1, 2, 3)[2]	$t_{ul2Rxpd}$	1		14	ns
RXCLK_i rising edge to low-impedance RXDATA_i[15:0], RXPRTY_i, RXSOF_i, RXEOF_i, RXPADL_i, RXVAL_i, RXERR_i, and RXFA_i (i = 0, 1, 2, 3)	$t_{ul2RxhlZ}$	1			ns
RXCLK_i rising edge to high-impedance RXDATA_i[15:0], RXPRTY_i, RXSOF_i, RXEOF_i, RXPADL_i, RXVAL_i, RXERR_i, and RXFA_i (i = 0, 1, 2, 3)	$t_{ul2RxlhZ}$			11	ns
RXCLK_i rising edge to high-impedance RXDATA_i[15:0] (i = 0, 1, 2, 3)[2]	$t_{ul2RxlhZ}$			14	ns

NOTES:
1. In memory mapped mode (RcvSelMode = 1 in register R_UICNF), $t_{ul2Rxsu}$ = 5 ns, otherwise $t_{ul2Rxsu}$ = 4 ns
2. In quad 16-bit mode, $t_{ul2Rxpd}$ is different than in quad 8-bit mode

Table 51. Transmit UTOPIA Quad Interface Configured for 50 MHz Operation: 16/8-Bit Data Bus and One/Two Clock Cycle Decode-Response Delay

Parameter	Symbol	Min	Typ	Max	Unit
TXCLK_i frequency (i = 0, 1, 2, 3)	f_{ul2Tx}			50	MHz
TXCLK_i duty cycle (i = 0, 1, 2, 3)	D_{ul2Tx}	30		70	%
TXDATA_i[7:0], TXPADL_i, TXENB_i, TXSOF_i, TXEOF_i, TXPRTY_i, and TXERR_i setup time to TXCLK_i (i = 0, 1, 2, 3)	$t_{ul2Txsu}$	4/5[1]			ns
TXDATA_i[7:0], TXPADL_i, TXENB_i, TXSOF_i, TXEOF_i, TXPRTY_i, and TXERR_i hold time from TXCLK_i (i = 0, 1, 2, 3)	t_{ul2Txh}	1			ns
TXCLK_i rising edge to TXFA_i (i = 0, 1, 2, 3) propagation delay	$t_{ul2Txpd}$	1		6	ns
TXCLK_i rising edge to low-impedance TXFA_i (i = 0, 1, 2, 3)	$t_{ul2TxhlZ}$	1			ns
TXCLK_i rising edge to high-impedance TXFA_i (i = 0, 1, 2, 3)	$t_{ul2TxlhZ}$			11	ns

NOTES:
1. In memory mapped mode (XmtSelMode = 1 in register T_UICNF), $t_{ul2Txsu}$ = 5 ns, otherwise $t_{ul2Txsu}$ = 4 ns

Figure 95. Microprocessor Read Timing

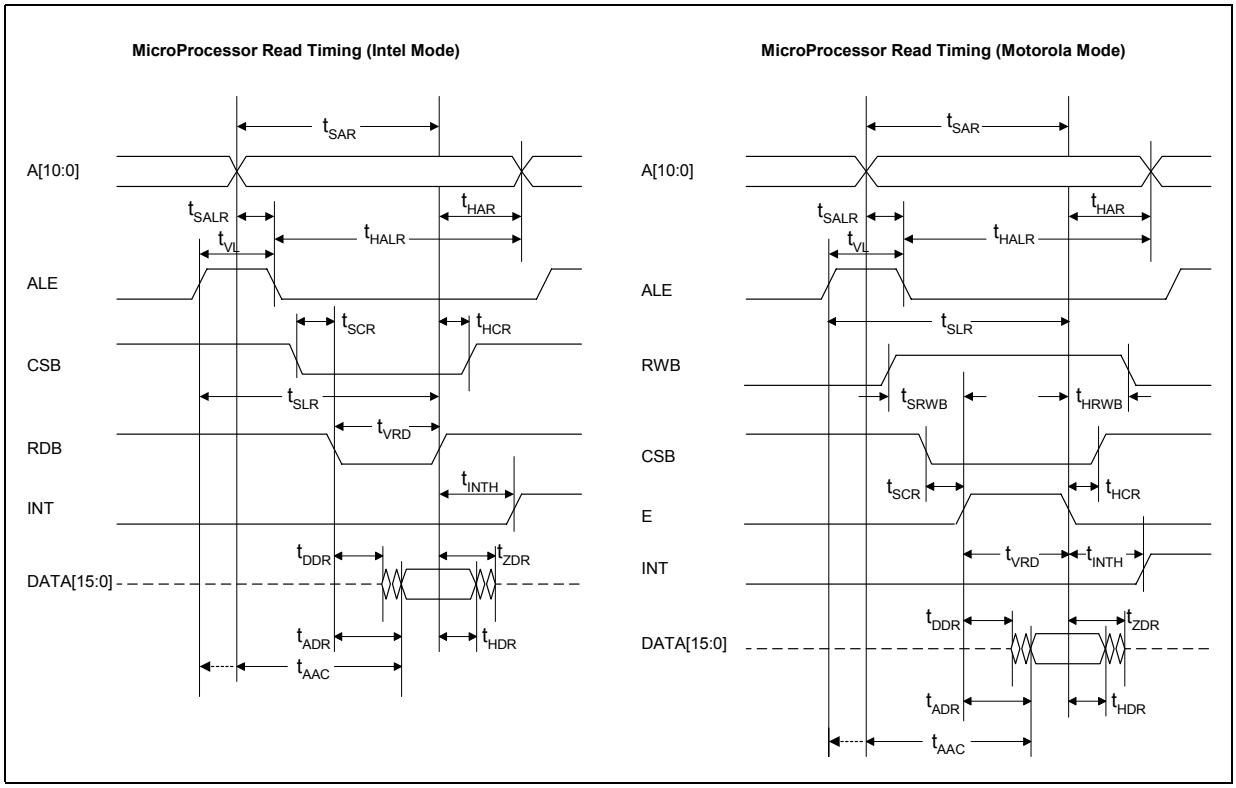


Figure 96. Microprocessor Write Timing

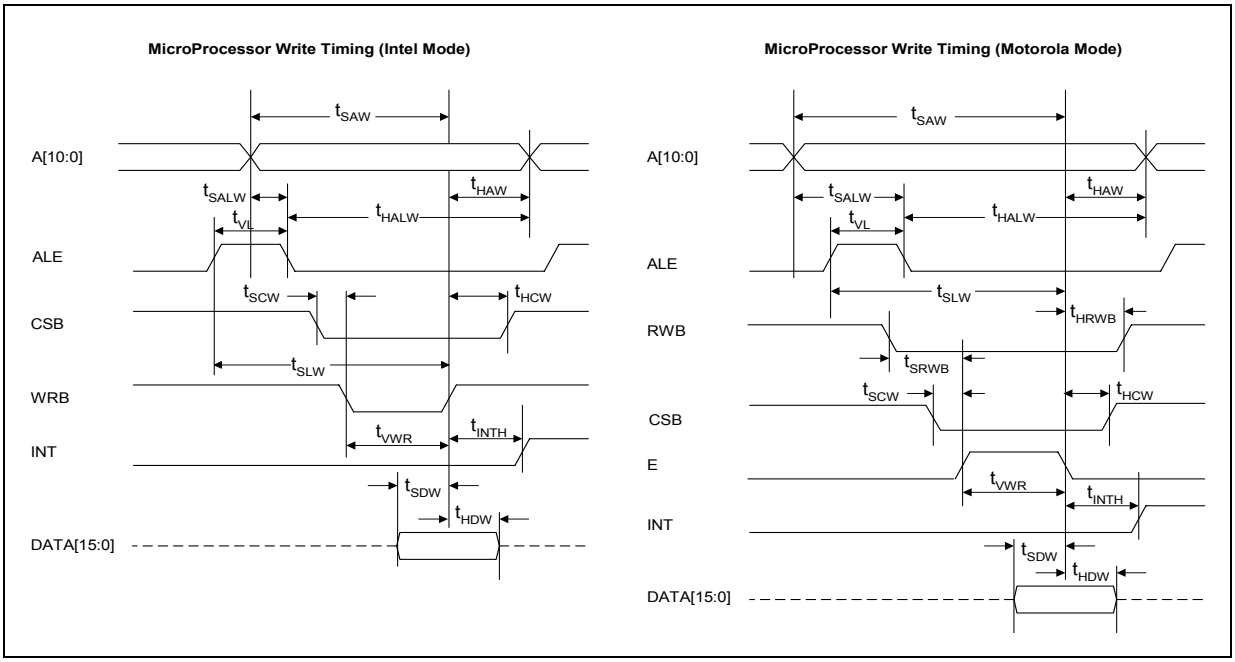


Table 52. Microprocessor Data Read Timing Parameters (Considering Outputs with a 50 pF Load) (Sheet 1 of 2)

Parameter	Symbol	Min	Typ	Max	Unit
A[10:0] setup time to read cycle end	t_{SAR}	8			ns
A[10:0] hold time from inactive read	t_{HAR}[1]	1			ns
A[10:0] setup time to latch	t_{SALR}[2]	1			ns
A[10:0] hold time from latch	t_{HALR}[2]	2			ns
Valid latch pulse width	t_{VL}[2]	8			ns
ALE rising edge to read cycle end setup	t_{SLR}[2]	8			ns
RWB setup to active read	t_{SRWB}[3]	1			ns
RWB hold from inactive read	t_{HRWB}[3]	1			ns
CSB setup to active read	t_{SCR}	2			ns
CSB hold from inactive read	t_{HCR}	1			ns
DATA[15:0] access time from valid address (or ALE whichever comes last for muxed AD bus)	t_{AAC}			31	ns
DATA[15:0] bus driven from active read	t_{DDR}	7			ns
DATA[15:0] access time from active read	t_{ADR}			16	ns
DATA[15:0] hold from inactive read	t_{HDR}	6			ns

NOTES:
1. For non-multiplexed Address and Data bus (ALE tied high).
2. For multiplexed Address and Data bus (ALE used as address latch enable).
3. Not used with an Intel microprocessor.
4. T is the internal clock cycle time.

Table 52. Microprocessor Data Read Timing Parameters (Considering Outputs with a 50 pF Load) (Sheet 2 of 2)

Parameter	Symbol	Min	Typ	Max	Unit
DATA[15:0] high impedance from inactive read	t_{ZDR}			14	ns
Valid read pulse width	t_{VRD}	20			ns
Inactive read to inactive INT (due to reset on read feature)	t_{INTH}[4]	7		19	ns

NOTES:
1. For non-multiplexed Address and Data bus (ALE tied high).
2. For multiplexed Address and Data bus (ALE used as address latch enable).
3. Not used with an Intel microprocessor.
4. T is the internal clock cycle time.

Table 53. Microprocessor Data Write Timing Parameters

Parameter	Symbol	Min	Typ	Max	Unit
A[10:0] setup time to write cycle end	t_{SAW}	9			ns
A[10:0] hold time from inactive write	t_{HAW}[1]	1			ns
A[10:0] setup time to latch	t_{SALW}[2]	1			ns
A[10:0] hold time from latch	t_{HALW}[2]	2			ns
Valid latch pulse width	t_{VL}[2]	9			ns
ALE rising edge to write cycle end setup	t_{SLW}[2]	9			ns
RWB setup to active write	t_{SRWB}[3]	1			ns
RWB hold from inactive write	t_{HRWB}[3]	1			ns
CSB setup to active write	t_{SCW}	2			ns
CSB hold from inactive write	t_{HCW}	1			ns
DATA[15:0] setup to inactive write	t_{SDW}	1			ns
DATA[15:0] hold from inactive write	t_{HDW}	1			ns
Valid write pulse width	t_{VWR}	20			ns
Inactive write to inactive INT (due to interrupt masking)	t_{INTHv}[4]	7		19	ns

NOTES:
1. For non-multiplexed Address and Data bus (ALE tied high).
2. For multiplexed Address and Data bus (ALE used as address latch enable).
3. Not used with an Intel microprocessor.
4. T is the internal clock cycle time

Figure 97. Asynchronous Reset (RESET) Timing

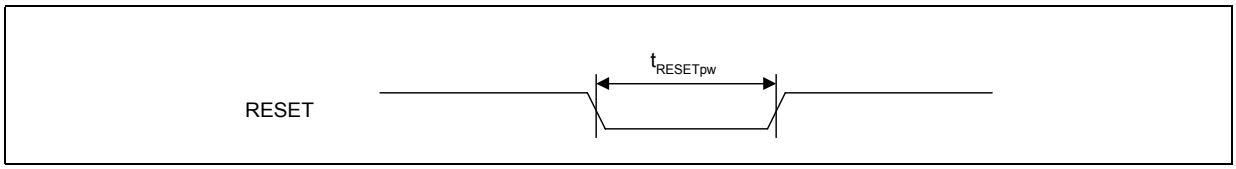


Table 54. Asynchronous Reset (RESET) Timing

Parameter	Symbol	Min	Typ	Max	Unit
Asynchronous Reset pulse width (RESET pin)	$t_{RESETpw}$	10			ns

13.0 Testability

IEEE* 1149.1 Boundary Scan (JTAG) is used for testing of the interconnect. The following provides an overview of IEEE 1149.1 as applied to the Intel IXF6048. [For more detailed information regarding JTAG, refer to "IEEE Standard Test Access Port and Boundary-Scan Architecture, IEEE Std 1149.1-1990" and "Supplement to IEEE Std 1149.1-1990, IEEE Std 1149.1b-1994", available through IEEE].

13.1 IEEE* 1149.1 Boundary Scan

The boundary scan circuitry allows the user to test the interconnection between the Intel IXF6048 and the circuit board.

The boundary scan port consists of 5 pins as shown in Table 55.

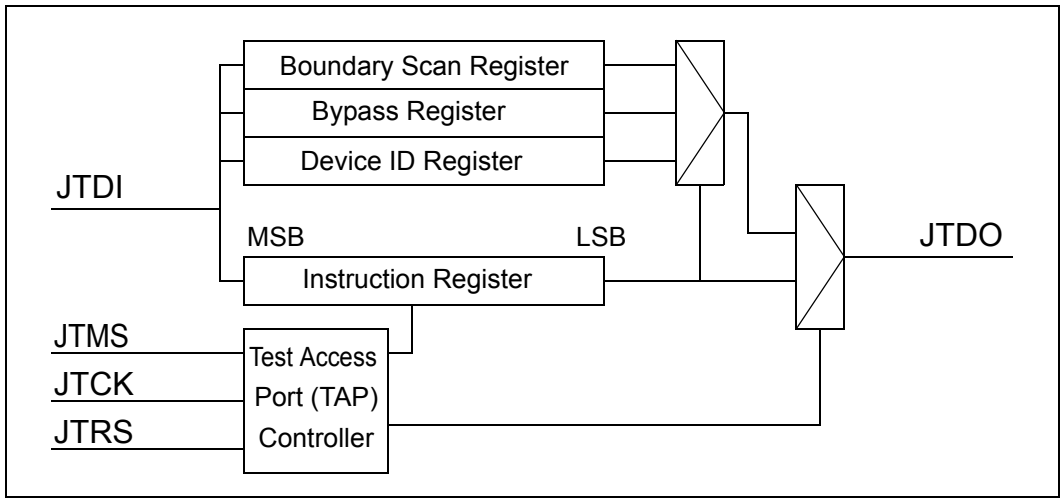
Table 55. Boundary Scan Port

Pin #	Name	I/O	Function
M26	JTMS	I	Test Mode Select: Determines state of TAP Controller. Internal pull-up resistor.
L28	JTCK	I	Test Clock: Clock for all boundary scan circuitry
L29	JTRS	I	Test Reset: Active-low asynchronous signal that causes the TAP controller to reset. Internal pull-up resistor. **Caution:** The VIH_TTL, for only this pin, needs to be increased from a minimum of 2.0 V to 2.4 V to work properly. If the VIH_TTL for this pin is left at 2.0 V, the JTAG could get stuck in reset.
L30	JTDI	I	Test Data In: input for instructions and data. Internal pull-up resistor.
L27	JTDO	O	Test Data Out: Output of instructions and data.

The JTAG circuitry, as shown in Figure 98, consists of a Test Access Port and Instruction Register for controlling the test output (JTDO) and the following Data Registers: Boundary Scan, Bypass, and Device ID.

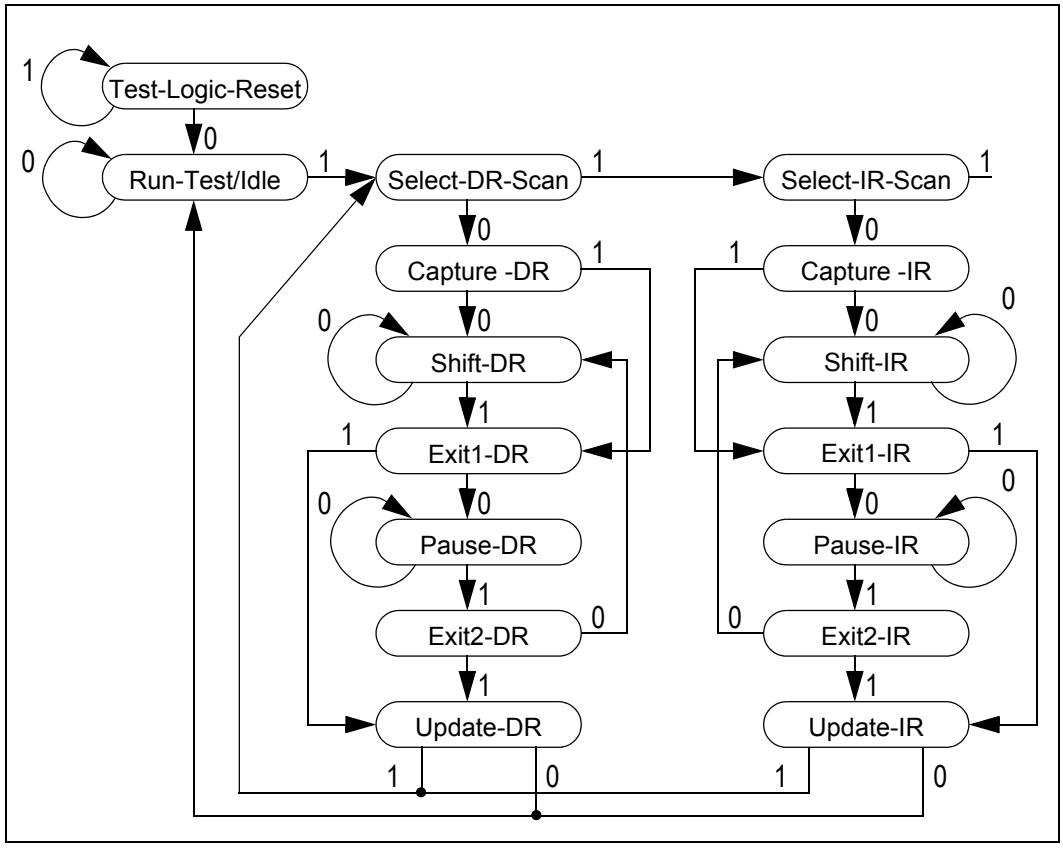
Data and instructions are shifted into the Intel IXF6048 through the Test Data In pin (JTDI), and then shifted out through the Test Data Out pin (JTDO). An asynchronous reset pin (JTRS) allows resetting of the boundary scan circuitry.

Figure 98. JTAG Test Circuitry



The TAP controller is a state machine that controls the function of the boundary scan circuitry. Inputs to the TAP controller are the Test Mode Select (JTMS) and the Test Clock (JTCK) signals. Figure 99 shows the state machine as defined by the 1149.1 Specification.

Figure 99. TAP State Machine



13.1.1 Instruction Register and Definitions

The Intel IXF6048 supports the following instructions identified by IEEE 1149.1: EXTEST, SAMPLE/PRELOAD, BYPASS, and IDCODE:

EXTEST (‘b00): Allows circuitry external to the package (typically the board interconnect) to be tested. While the instruction is active, the boundary scan register is connected between JTDI and JTDO. Signals present on input pins are loaded into the BSR inputs cells on the rising edge of JTCK during CAPTURE-DR state of the TAP controller. BSR input cell contents are shifted one bit location on each rising edge of JTCK during the TAP’s SHIFT-DR state. BSR output cell contents appear at output pins on the falling edge of JTCK during the TAP’s UPDATE-IR state.

SAMPLE/PRELOAD (‘b01): This instruction creates a snapshot of the normal operation of the Intel IXF6048. The boundary scan register is connected between JTDI and JTDO for any data shifts while this instruction is active. All BSR cells capture data present at their inputs on the rising edge of JTCK during the CAPTURE-DR state. No action is taken during the UPDATE-DR state.

BYPASS (‘b11): BYPASS allows a device to be removed from the scan chain by inserting a one-bit shift register stage between JTDI and JTDO during data shifts. When the instruction is active, the test logic has no impact upon the system logic performing its function. When selected, the shift-register is set to a logic zero on the rising edge of the JTCK during the CAPTURE-DR state.

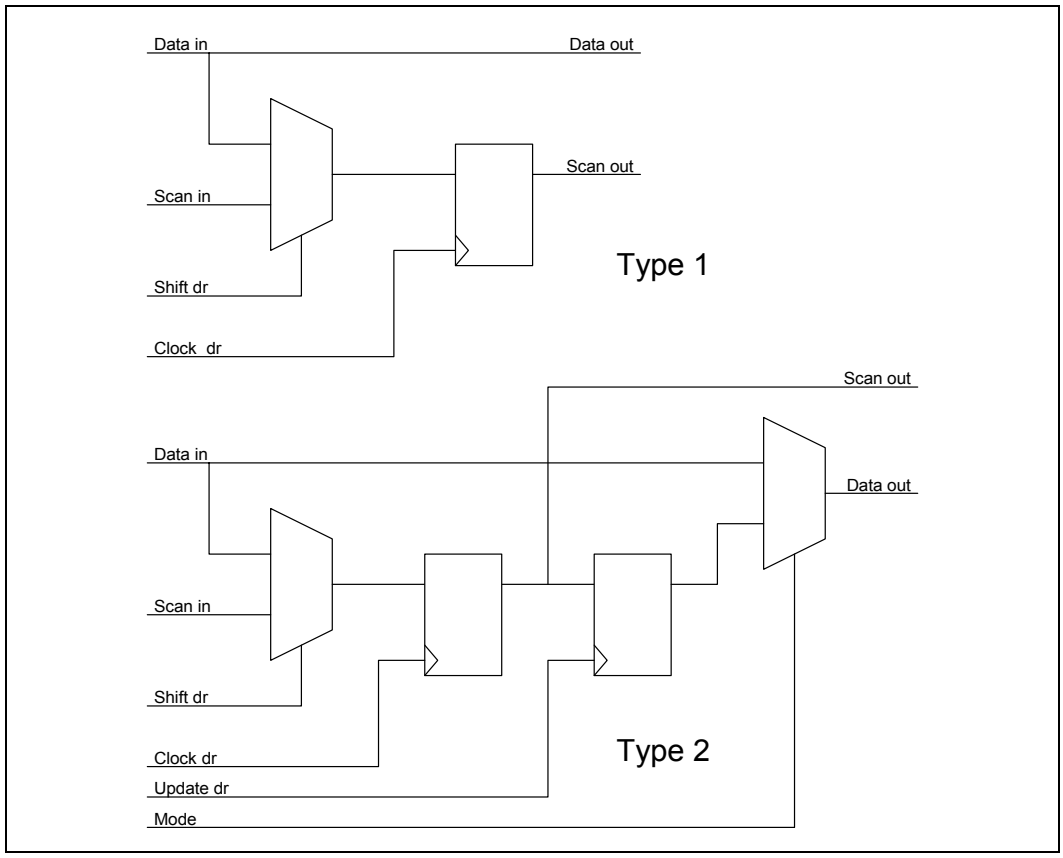
IDCODE (‘b10): IDCODE allows the reading of component types via the scan chain. During this instruction, the 32-bit Device Identification Register (ID-Register) is placed between JTDI and JTDO. The ID Register captures a fixed value on the rising edge of JTCK during the CAPTURE-DR state. The Device Identification Register contains the following information: Manufacturer ID: ‘d126; Design Part Number: ‘d 6048; Design Version Number: ‘d1.

The EXTEST, SAMPLE/PRELOAD, BYPASS, and IDCODE instructions are shifted into the instruction register during the SHIFT-IR state and become active upon exiting the UPDATE-IR state.

13.1.2 Boundary Scan Register

The Boundary Scan Register is a 614-bit shift register composed of 2 types of shift-register cells, as depicted in Figure 100. Type 1 is specifically for clock inputs; Type 2 is used for all other I/O and Control signals. More specific information regarding the Boundary Scan Register and individual Boundary Scan Cells may be obtained from the Boundary Scan Description Language (BSDL) file, which is available upon request.

Figure 100. Boundary Scan Cell Types



14.0 Package Information

Figure 101. Mechanical Information for the 600 TBGA (Top View)

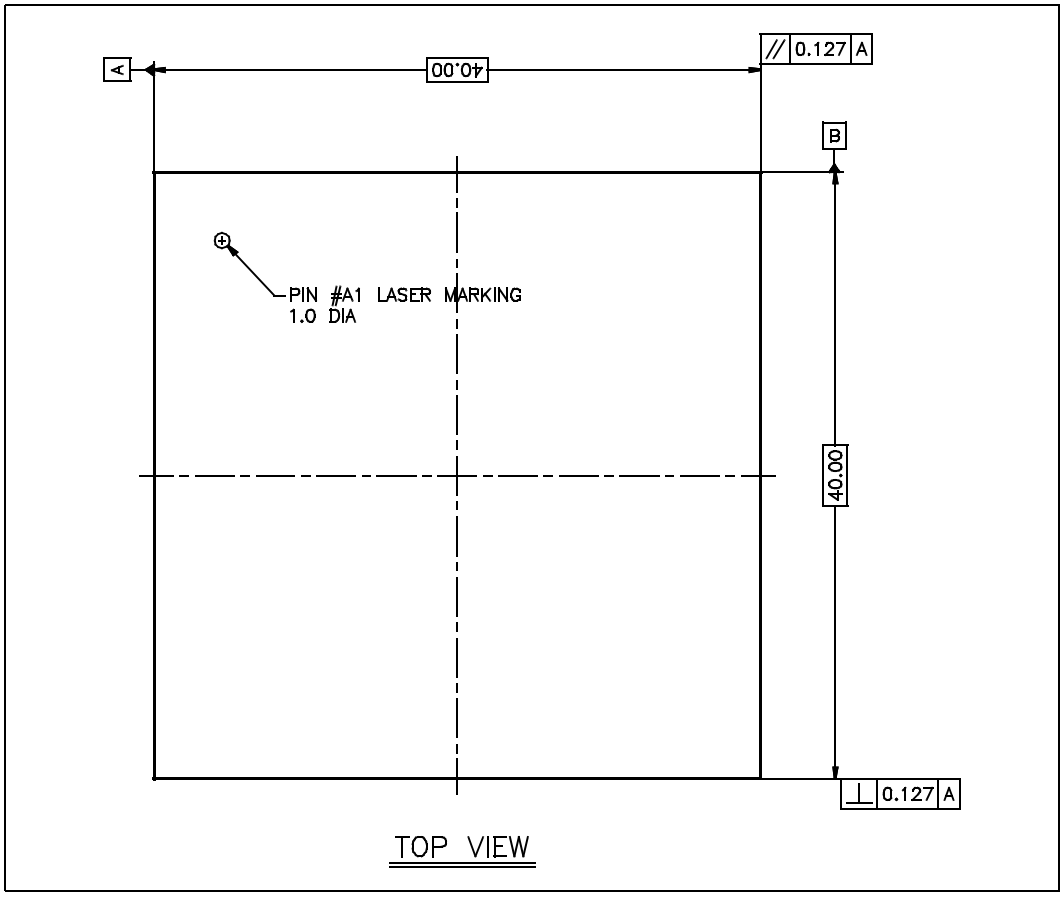


Figure 102. Mechanical Information for the 600 TBGA (Bottom View)

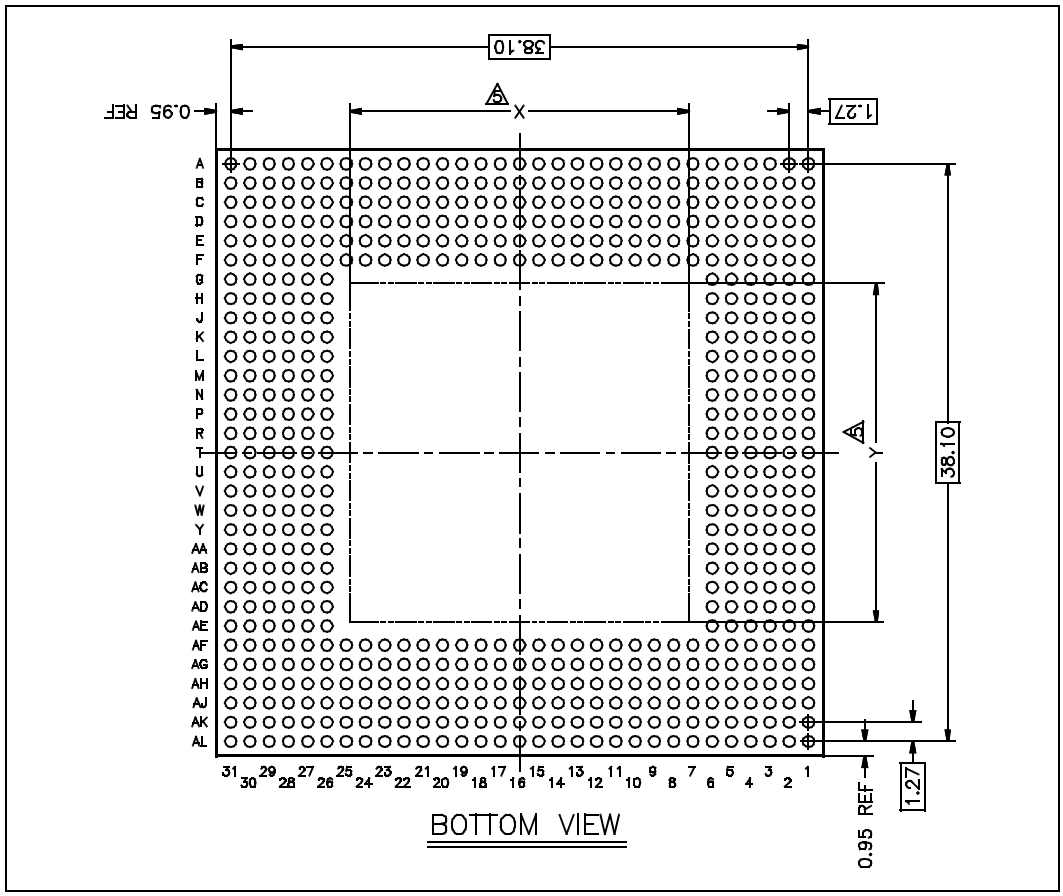
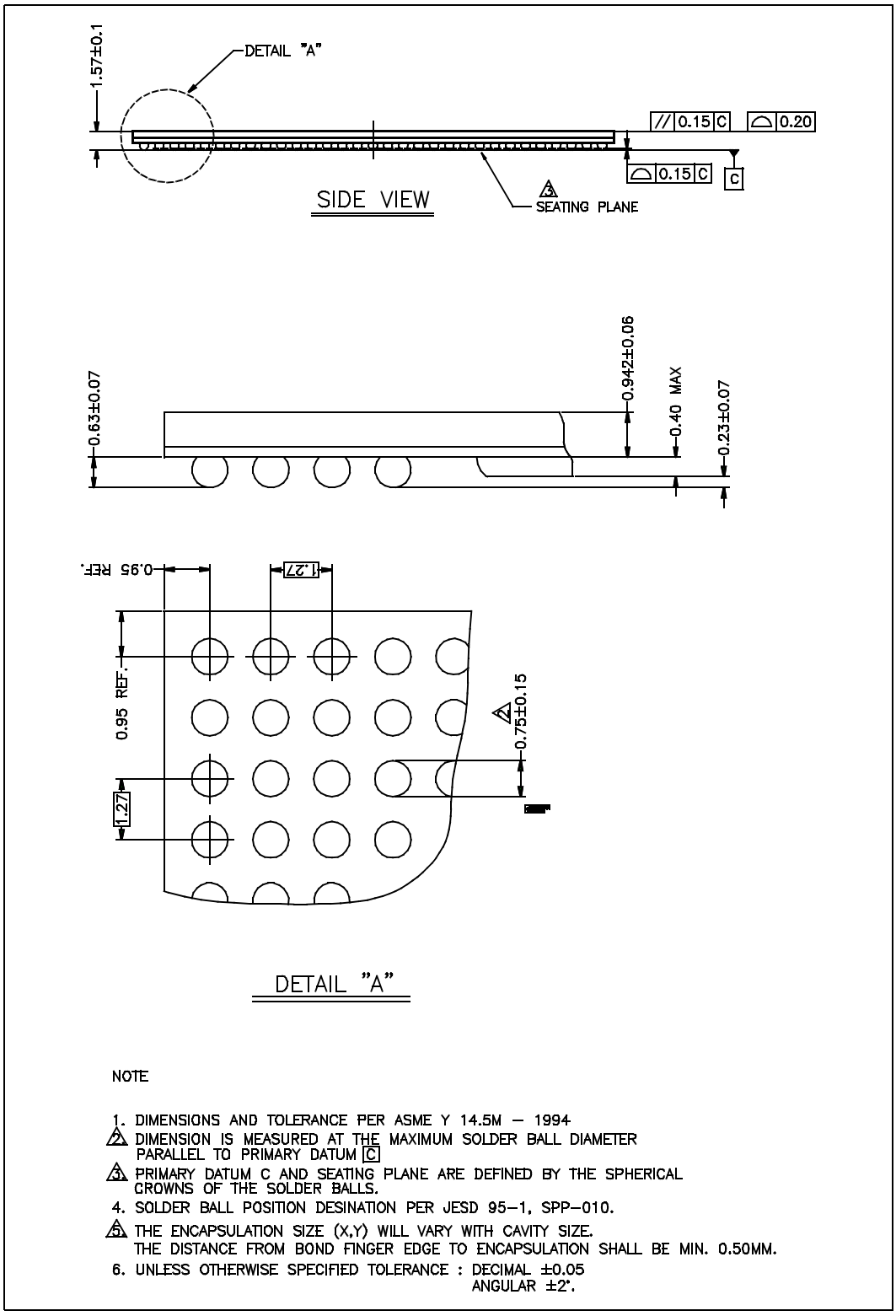


Figure 103. Mechanical Information for the 600 TBGA (Side and Detail View)



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