74HC3G06; 74HCT3G06

Triple inverter with open-drain outputs

Rev. 4 — 19 December 2013 Product data sheet

1. General description

The 74HC3G06; 74HCT3G06 is a triple inverter with open-drain outputs. Inputs include clamp diodes. This enables the use of current limiting resistors to interface inputs to voltages in excess of V_{CC}.

2. Features and benefits

- Wide supply voltage range from 2.0 V to 6.0 V
- Input levels:
  - For 74HC3G06: CMOS level
  - For 74HCT3G06: TTL level
- Complies with JEDEC standard no. 7A
- High noise immunity
- Low power dissipation
- Multiple package options
- ESD protection:
  - HBM JESD22-A114F exceeds 2000 V
  - MM JESD22-A115-A exceeds 200 V
- Specified from −40 °C to +85 °C and −40 °C to +125 °C

3. Ordering information

Table 1. Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
74HC3G06DP	−40 °C to +125 °C	TSSOP8	plastic thin shrink small outline package; 8 leads; body width 3 mm; lead length 0.5 mm	SOT505-2
74HCT3G06DP				
74HC3G06DC	−40 °C to +125 °C	VSSOP8	plastic very thin shrink small outline package; 8 leads; body width 2.3 mm	SOT765-1
74HCT3G06DC				
74HC3G06GD	−40 °C to +125 °C	XSON8	plastic extremely thin small outline package; no leads; 8 terminals; body 3 × 2 × 0.5 mm	SOT996-2
74HCT3G06GD				

4. Marking

Table 2. Marking code

Type number	Marking code[1]
74HC3G06DP	H06
74HCT3G06DP	T06
74HC3G06DC	H06
74HCT3G06DC	T06
74HC3G06GD	H06
74HCT3G06GD	T06

[1] The pin 1 indicator is located on the lower left corner of the device, below the marking code.

5. Functional diagram

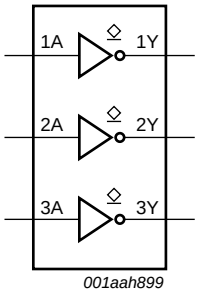


Fig 1. Logic symbol

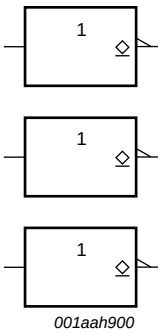


Fig 2. IEC logic symbol

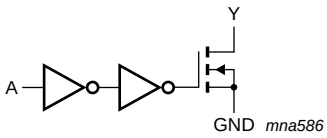


Fig 3. Logic diagram (one inverter)

6. Pinning information

6.1 Pinning

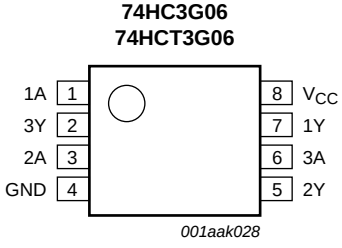
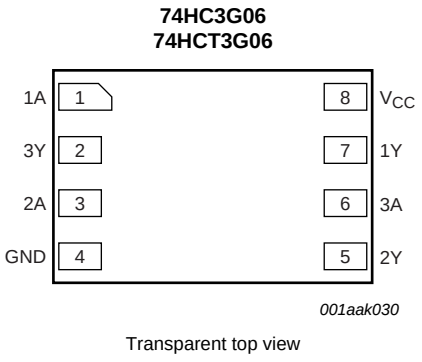


Fig 4. Pin configuration SOT505-2 (TSSOP8) and SOT765-1 (VSSOP8)



Transparent top view

Fig 5. Pin configuration SOT996-2 (XSON8)

6.2 Pin description

Table 3. Pin description

Symbol	Pin	Description
1A, 2A, 3A	1, 3, 6	data input
GND	4	ground (0 V)
1Y, 2Y, 3Y	7, 5, 2	data output
V_{CC}	8	supply voltage

7. Functional description

Table 4. Function table[1]

Input nA	Output nY
L	Z
H	L

[1] H = HIGH voltage level; L = LOW voltage level; Z = high-impedance OFF-state.

8. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions		Min	Max	Unit
V_{CC}	supply voltage			−0.5	7.0	V
I_{IK}	input clamping current	$V_I < -0.5$ V or $V_I > V_{CC} + 0.5$ V	[1]	-	±20	mA
I_{OK}	output clamping current	$V_O < -0.5$ V	[1]	−20	-	mA
V_O	output voltage	active mode	[1]	−0.5	$V_{CC} + 0.5$	V
		high-impedance mode	[1]	−0.5	7.0	V
I_O	output current	$V_O = -0.5$ V to 7.0 V	[1]	-	25	mA
I_{CC}	supply current		[1]	-	50	mA
I_{GND}	ground current		[1]	−50	-	mA
T_{stg}	storage temperature			−65	+150	°C
P_D	dynamic power dissipation	$T_{amb} = -40$ °C to +125 °C	[2]	-	300	mW

[1] The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

[2] For TSSOP8 package: above 55 °C the value of P_{tot} derates linearly with 2.5 mW/K.
For VSSOP8 package: above 110 °C the value of P_{tot} derates linearly with 8 mW/K.
For XSON8 package: above 118 °C the value of P_{tot} derates linearly with 7.8 mW/K.

9. Recommended operating conditions

Table 6. Recommended operating conditions

Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	74HC3G06			74HCT3G06			Unit
			Min	Typ	Max	Min	Typ	Max	
V_{CC}	supply voltage		2.0	5.0	6.0	4.5	5.0	5.5	V
V_I	input voltage		0	-	6.0	0	-	5.5	V
V_O	output voltage		0	-	V_{CC}	0	-	V_{CC}	V
T_{amb}	ambient temperature		–40	+25	+125	–40	+25	+125	°C
$\Delta t/\Delta V$	input transition rise and fall rate	V_{CC} = 2.0 V	-	-	625	-	-	-	ns/V
		V_{CC} = 4.5 V	-	1.67	139	-	1.67	139	ns/V
		V_{CC} = 6.0 V	-	-	83	-	-	-	ns/V

10. Static characteristics

Table 7. Static characteristics

Voltages are referenced to GND (ground = 0 V). All typical values are measured at T_{amb} = 25 °C.

Symbol	Parameter	Conditions	–40 °C to +85 °C			–40 °C to +125 °C		Unit
			Min	Typ[1]	Max	Min	Max	
74HC3G06								
V_{IH}	HIGH-level input voltage	V_{CC} = 2.0 V	1.5	1.2	-	1.5	-	V
		V_{CC} = 4.5 V	3.15	2.4	-	3.15	-	V
		V_{CC} = 6.0 V	4.2	3.2	-	4.2	-	V
V_{IL}	LOW-level input voltage	V_{CC} = 2.0 V	-	0.8	0.5	-	0.5	V
		V_{CC} = 4.5 V	-	2.1	1.35	-	1.35	V
		V_{CC} = 6.0 V	-	2.8	1.8	-	1.8	V
V_{OL}	LOW-level output voltage	V_I = V_{IH} or V_{IL}						
		I_O = 20 μA; V_{CC} = 2.0 V	-	0	0.1	-	0.1	V
		I_O = 20 μA; V_{CC} = 4.5 V	-	0	0.1	-	0.1	V
		I_O = 20 μA; V_{CC} = 6.0 V	-	0	0.1	-	0.1	V
		I_O = 4.0 mA; V_{CC} = 4.5 V	-	0.15	0.33	-	0.4	V
		I_O = 5.2 mA; V_{CC} = 6.0 V	-	0.16	0.33	-	0.4	V
I_I	input leakage current	V_I = V_{CC} or GND; V_{CC} = 6.0 V	-	-	±0.1	-	±1.0	μA
I_{LO}	output leakage current	V_I = V_{IL}; V_O = V_{CC} or GND	-	-	±5.0	-	±10	μA
I_{CC}	supply current	per input pin; V_{CC} = 6.0 V; V_I = V_{CC} or GND; I_O = 0 A;	-	-	10	-	20	μA
C_I	input capacitance		-	1.5	-	-	-	pF

Table 7. Static characteristics *...continued*

Voltages are referenced to GND (ground = 0 V). All typical values are measured at T_{amb} = 25 °C.

Symbol	Parameter	Conditions	–40 °C to +85 °C			–40 °C to +125 °C		Unit
			Min	Typ[1]	Max	Min	Max	
74HCT3G06								
V_{IH}	HIGH-level input voltage	V_{CC} = 4.5 V to 5.5 V	2.0	1.6	-	2.0	-	V
V_{IL}	LOW-level input voltage	V_{CC} = 4.5 V to 5.5 V	-	1.2	0.8	-	0.8	V
V_{OL}	LOW-level output voltage	V_I = V_{IH} or V_{IL}						
		I_O = 20 μA; V_{CC} = 4.5 V	-	0	0.1	-	0.1	V
		I_O = 4.0 mA; V_{CC} = 4.5 V	-	0.15	0.33	-	0.4	V
I_I	input leakage current	V_I = V_{CC} or GND; V_{CC} = 5.5 V	-	-	±1.0	-	±1.0	μA
I_{LO}	output leakage current	V_I = V_{IL}; V_O = V_{CC} or GND	-	-	±5.0	-	±10	μA
I_{CC}	supply current	per input pin; V_{CC} = 5.5 V; V_I = V_{CC} or GND; I_O = 0 A;	-	-	10	-	20	μA
ΔI_{CC}	additional supply current	per input; V_{CC} = 4.5 V to 5.5 V; V_I = V_{CC} – 2.1 V; I_O = 0 A	-	-	375	-	410	μA
C_I	input capacitance		-	1.5	-	-	-	pF

[1] Typical values are measured at T_{amb} = 25 °C.

11. Dynamic characteristics

Table 8. Dynamic characteristics

Voltages are referenced to GND (ground = 0 V); all typical values are measured at T_{amb} = 25 °C; for test circuit see Figure 7.

Symbol	Parameter	Conditions	–40 °C to +85 °C			–40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	
74HC3G06								
t_{PZL}	OFF-state to LOW propagation delay	nA to nY; see Figure 6						
		V_{CC} = 2.0 V	-	22	95	-	125	ns
		V_{CC} = 4.5 V	-	9	18	-	25	ns
		V_{CC} = 6.0 V	-	8	16	-	20	ns
t_{PLZ}	LOW to OFF-state propagation delay	nA to nY; see Figure 6						
		V_{CC} = 2.0 V	-	24	95	-	125	ns
		V_{CC} = 4.5 V	-	11	20	-	27	ns
		V_{CC} = 6.0 V	-	10	19	-	23	ns
t_{THL}	HIGH to LOW output transition time	nY; see Figure 6						
		V_{CC} = 2.0 V	-	18	95	-	125	ns
		V_{CC} = 4.5 V	-	6	19	-	25	ns
		V_{CC} = 6.0 V	-	5	16	-	20	ns
C_{PD}	power dissipation capacitance	V_I = GND to V_{CC} [1]	-	4	-	-	-	pF

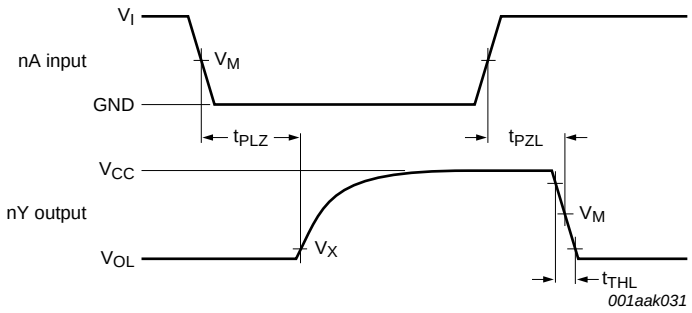
Table 8. Dynamic characteristics *...continued*

Voltages are referenced to GND (ground = 0 V); all typical values are measured at T_{amb} = 25 °C; for test circuit see Figure 7.

Symbol	Parameter	Conditions	–40 °C to +85 °C			–40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	
74HCT3G06								
t_{PZL}	OFF-state to LOW propagation delay	nA to nY; see Figure 6						
		V_{CC} = 4.5 V	-	9	24	-	29	ns
t_{PLZ}	LOW to OFF-state propagation delay	nA to nY; see Figure 6						
		V_{CC} = 4.5 V	-	12	27	-	32	ns
t_{THL}	HIGH to LOW output transition time	V_{CC} = 4.5 V; see Figure 6	-	6	19	-	22	ns
C_{PD}	power dissipation capacitance	V_I = GND to V_{CC} – 1.5 V [1]	-	4		-	-	pF

[1] C_{PD} is used to determine the dynamic power dissipation (P_D in μW).
$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma(C_L \times V_{CC}^2 \times f_o)$ where:
f_i = input frequency in MHz;
f_o = output frequency in MHz;
C_L = output load capacitance in pF;
V_{CC} = supply voltage in V;
N = number of inputs switching;
$\Sigma(C_L \times V_{CC}^2 \times f_o)$ = sum of outputs.

12. Waveforms



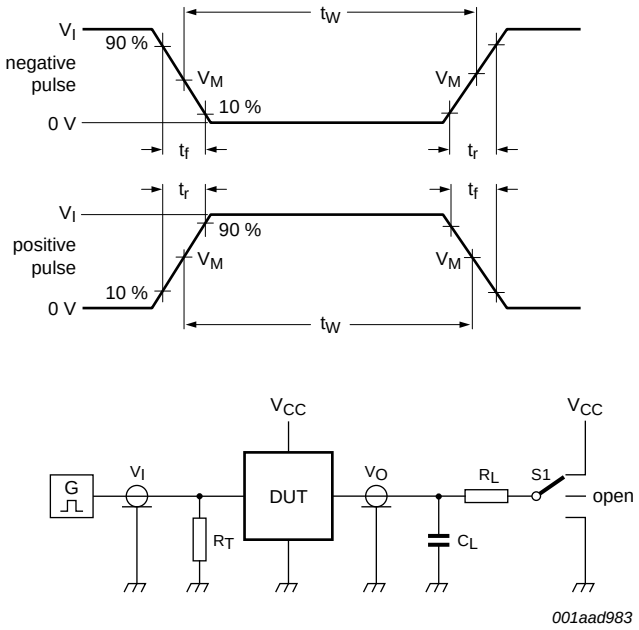
Measurement points are given in Table 9.

V_{OL} is the typical output voltage level that occurs with the output load.

Fig 6. The input (nA) to output (nY) propagation delays

Table 9. Measurement points

Type	Input	Output	
	V_M	V_M	V_X
74HC3G06	0.5 × V_{CC}	0.5 × V_{CC}	0.1 × V_{CC}
74HCT3G06	1.3 V	1.3 V	0.1 × V_{CC}



Test data is given in Table 10.

Definitions for test circuit:

R_T = Termination resistance should be equal to output impedance Z_o of the pulse generator.

C_L = Load capacitance including jig and probe capacitance.

R_L = Load resistance.

S1 = Test selection switch.

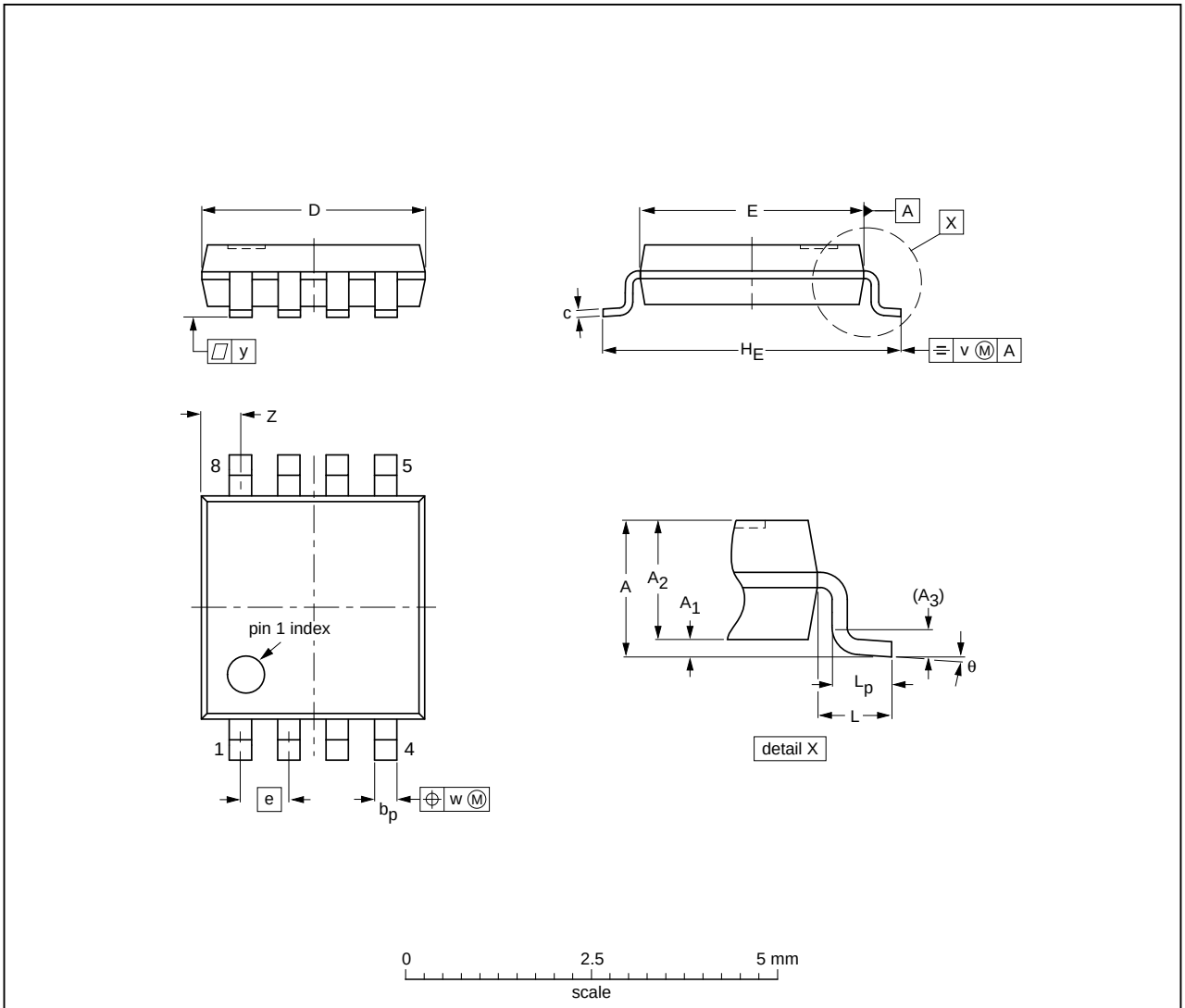
Fig 7. Test circuit for measuring switching times

Table 10. Test data

Type	Input		Load		S1 position
	V_I	t_r, t_f	C_L	R_L	t_{PZL}, t_{PLZ}
74HC3G06	GND to V_{CC}	≤ 6 ns	50 pF	1 kΩ	V_{CC}
74HCT3G06	GND to 3 V	≤ 6 ns	50 pF	1 kΩ	V_{CC}

13. Package outline

TSSOP8: plastic thin shrink small outline package; 8 leads; body width 3 mm; lead length 0.5 mm SOT505-2



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	v	w	y	$Z^{(1)}$	θ
mm	1.1	0.15 0.00	0.95 0.75	0.25	0.38 0.22	0.18 0.08	3.1 2.9	3.1 2.9	0.65	4.1 3.9	0.5	0.47 0.33	0.2	0.13	0.1	0.70 0.35	8° 0°

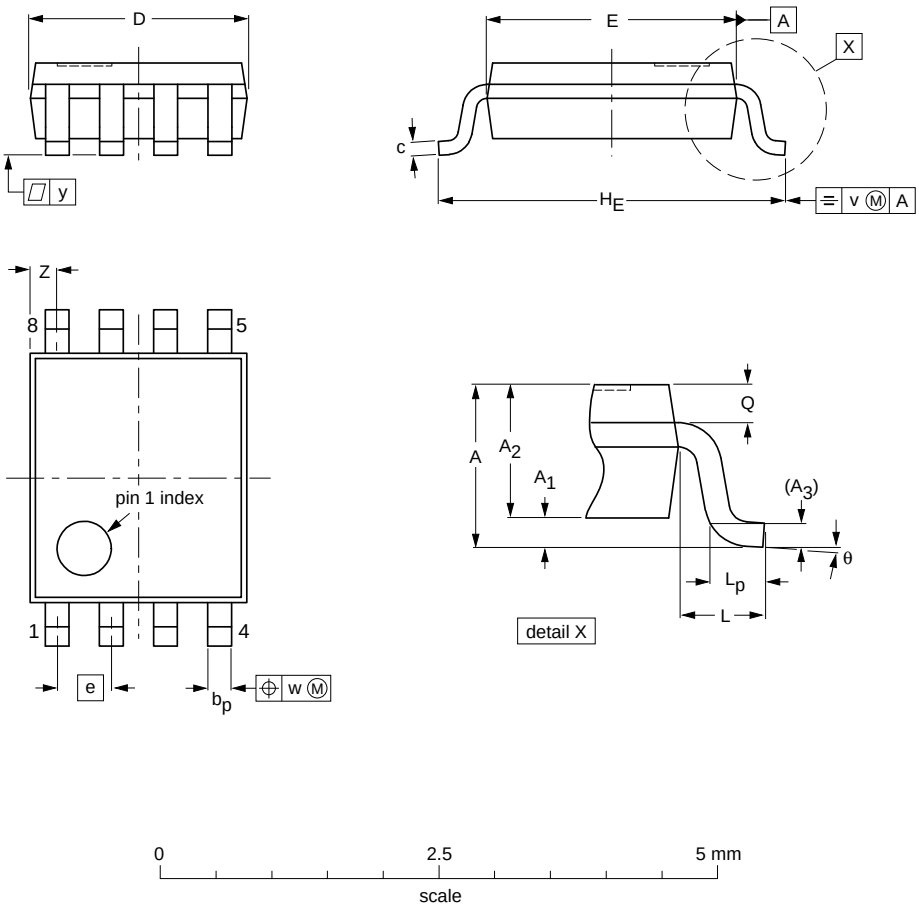
Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT505-2		- - -				02-01-16

Fig 8. Package outline SOT505-2 (TSSOP8)

VSSOP8: plastic very thin shrink small outline package; 8 leads; body width 2.3 mm **SOT765-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(2)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	1	0.15 0.00	0.85 0.60	0.12	0.27 0.17	0.23 0.08	2.1 1.9	2.4 2.2	0.5	3.2 3.0	0.4	0.40 0.15	0.21 0.19	0.2	0.13	0.1	0.4 0.1	8° 0°

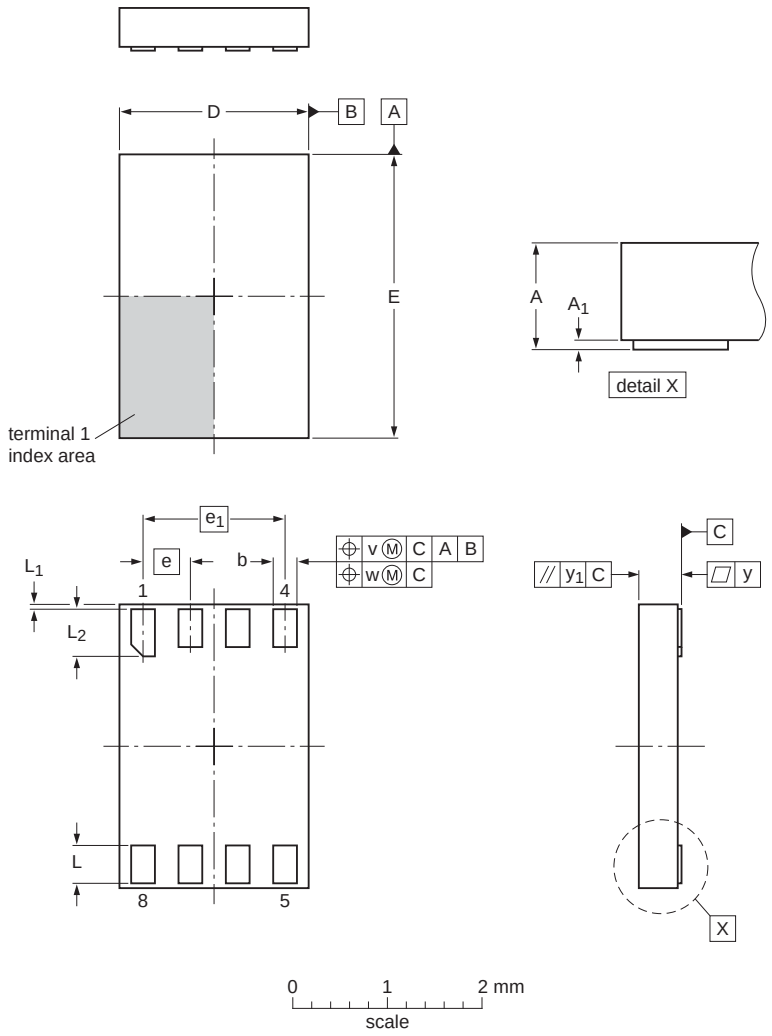
Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT765-1		MO-187				02-06-07

Fig 9. Package outline SOT765-1 (VSSOP8)

XSON8: plastic extremely thin small outline package; no leads; 8 terminals; body 3 x 2 x 0.5 mm **SOT996-2**



Dimensions (mm are the original dimensions)

Unit[1]		A	A_1	b	D	E	e	e_1	L	L_1	L_2	v	w	y	y_1
	max		0.05	0.35	2.1	3.1			0.5	0.15	0.6				
mm	nom	0.5					0.5	1.5				0.1	0.05	0.05	0.1
	min		0.00	0.15	1.9	2.9			0.3	0.05	0.4				

sot996-2_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT996-2						~~07-12-21~~ 12-11-20

Fig 10. Package outline SOT996-2 (XSON8)

14. Abbreviations

Table 11. Abbreviations

Acronym	Description
CMOS	Complementary Metal Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model
MM	Machine Model
TTL	Transistor-Transistor Logic

15. Revision history

Table 12. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74HC_HCT3G06 v.4	20131219	Product data sheet	-	74HC_HCT3G06 v.3
Modifications:	• For type numbers 74HC3G06GD and 74HCT3G06GD XSON8U has changed to XSON8.			
74HC_HCT3G06 v.3	20090511	Product data sheet	-	74HC_HCT3G06 v.2
74HC_HCT3G06 v.2	20031202	Product specification	-	74HC_HCT3G06 v.1
74HC_HCT3G06 v.1	20030515	Product specification	-	-

16. Legal information

16.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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