## SYNCHRONOUS SEPARATOR WITH AFC

## ■ GENERAL DESCRIPTION

The NJM2257 excutes Horizontal and Vertical synchronous signal separation, and odd / even field signal detection, from composit video signals.

Built-in $1 / 2 \mathrm{fH}$ Killer Function circuit can make stabilization of the Horizontal signal oscillation output during the vertical period.

## - FEATURES

- Operating Voltage (+4.5 to +5.3V)
- Internal AFC circuit (Horizontal sync. signal.)
- Internal 1 / 2 fH Killer Function
- AFC output Pulse Delay time is Adjustable
- Vertical synchronous pulse width is Adjustable
- Internal Field Discrlainat Function
- Package Outline DIP16, DMP16
- Bipolar Technology


## - APPLICATION

- VTR, TV, AV components etc.


## - BLOCK DIAGRAM

## NJM2257

$\square$ ABSOLUTE MAXIMUM RATINGS $\quad\left(T_{a}=25^{\circ} \mathrm{C}\right)$

| PARAMETER | SYMBOL | RATINGS | UNIT |
| :--- | :---: | :---: | :---: |
| Supply Voltage | $\mathrm{V}^{+}$ | +7 | V |
| Power Dissipation | $\mathrm{P}_{\mathrm{D}}$ | $(\mathrm{DIP16)500}$ |  |
|  |  | $(\mathrm{DMP16)} 350$ | mW |
| Operating Temperature Range | $\mathrm{T}_{\text {opr }}$ | -20 to +75 | mW |
| Storage Temperature Range | $\mathrm{T}_{\text {stg }}$ | -40 to +125 | ${ }^{\circ} \mathrm{C}$ |

- ELECTRICAL CHARACTERISTICS
$\left(\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}, \mathrm{~T}_{\mathrm{a}}=25^{\circ} \mathrm{C}\right)$

| PARAMETER |  | SYMBOL | TESTCONDITION | MIN. | TYP. | MAX. | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| Quiessent Current |  | $\mathrm{l}_{\mathrm{Q}}$ |  | - | 23.0 | 30.0 | mA |
| AFC Free Run Frequency |  | foH |  | 15.54 | 15.74 | 15.94 | KHz |
| AFC HD pulse width | none adiust | $\mathrm{T}_{\text {AHW1 }}$ | SW=a | 3.5 | 4.0 | 4.5 | $\mu \mathrm{S}$ |
|  | adjust | $\mathrm{T}_{\text {AHW2 }}$ | SW=b | 2.5 | 4.0 | 5.5 |  |
| AFC HD Delet Time |  | $\mathrm{T}_{\text {AHD }}$ |  | -1.0 | 0.5 | 2.0 | $\mu \mathrm{S}$ |
| AFC Lock Range |  | $\Delta \mathrm{ffL}_{\text {L }}$ |  | 500 | 700 | - | Hz |
| AFC Cap Charange |  | $\Delta \mathrm{f}_{\mathrm{HP}}$ |  | 400 | 600 | - | Hz |
| AFC Output Voltage | H | $\mathrm{V}_{\text {HAH }}$ |  | 4.0 | 4.2 | - | V |
|  | L | $\mathrm{V}_{\text {HAL }}$ |  | - | 0 | 0.1 |  |
| Sync Sepa Sync. Separation Level |  | $V_{\text {HSR }}$ |  | - | 0.16 | 0.18 | V |
| Sync Sepa Delay Time |  | THCD |  | 0.05 | 0.20 | 0.35 | $\mu \mathrm{S}$ |
| Sync Sepa Output Voltage | H | $\mathrm{V}_{\text {HCH }}$ |  | 4.0 | 4.2 | - | V |
|  | L | $\mathrm{V}_{\text {HCL }}$ |  | - | 0 | 0.1 |  |
| HD Output Palth Width |  | THPW |  | 4.0 | 5.5 | 7.0 | $\mu \mathrm{S}$ |
| HD Output Delay Time |  | THPD |  | 0.35 | 0.6 | 0.8 | $\mu \mathrm{S}$ |
| HD Output Voltage | H | $\mathrm{V}_{\text {HiH }}$ |  | 4.0 | 4.2 | - | V |
|  | L | $\mathrm{V}_{\text {Hil }}$ |  | - | 0 | 0.1 |  |
| $V$ Sync Palth Width |  | $\mathrm{V}_{\mathrm{Ww}}$ |  | 170 | 190 | 210 | $\mu \mathrm{S}$ |
| $\checkmark$ Sync Delay Time |  | TVD |  | 7.0 | 10.0 | 13.0 | $\mu \mathrm{S}$ |
| V Sync Output Voltage | H | TVH |  | 4.0 | 4.2 | - | V |
|  | L | $\mathrm{V}_{\mathrm{V}}$ |  | - | 0 | 0.1 |  |
| Field Distinction Delay Time | odd | T FOD |  | 246 | 256 | 266 | $\mu \mathrm{S}$ |
|  | even | T FED |  | 216 | 226 | 236 |  |
| Fideld Distinction Output Voltage | odd | Vfor |  | 4.0 | 4.2 | - | V |
|  | even | Vfer |  | - | 0 | 0.1 |  |

## - APPLICATION CIRCUIT



## - APPLICATION NOTES

It shows the characteristics by changing of the following resistor.

- The resistance between 9 Pin and GND

High resistance $\qquad$ AFC HD pulse is wide
Low resistance $\qquad$ AFC HD pulse is narrow

- The resistor between 9 Pin and $\mathrm{V}^{+}$

At the resistor is $100 \Omega$. AFC HD Delay adjustment is off, and AFC HD output width is $4 \mu \mathrm{~s}$ (typ.)

- The resistor between 9 Pin and GND is fundamentally $14.2 \mathrm{k} \Omega$, because the purpose of this resistor is pulse width adjusts $4 \mu \mathrm{~s}$.
- The resistor between 10 Pin and GND

High resistance $\qquad$ AFC HD Delay time gains
Low resistance - AFC HD Delay time loses

- The resistor between 13 Pin and GND

High resistance $\qquad$ Vsync pulse is wide
Low resistance

- Vsync pulse is narrow
- The resistor joind 2 Pin

Please adjust the wide of following W is from $33 \mu \mathrm{~s}$ to $37 \mu \mathrm{~s}(\mathrm{~W}=-(\mathrm{C} \cdot \mathrm{R}) \mathrm{ln} 0.5)$


Fig 1 I/ O PULSE


NOTE3


NOTE5


## - TERMINAL EXPLANATION

| PINNO. | PIN NAME | FUNCTION | INSIDE EQUIVALENT CIRCUIT |
| :---: | :---: | :---: | :---: |
| 1 | VIDEO-IN | Composit Video Signal Input |  |
| 2 | MM-HT | HD \& FD puse are Controlled by seting mono multi |  |
| 3 | HD-OUT | 1/2 $\mathrm{f}_{\mathrm{H}}$ Killer D Output |  |
| 4 | VCO-OUT | VCO Output is to be given to Ceramic Oscillator |  |
| 5 | VCO-FILTER 1 | Decide the Volume to be transfered shall by decided of Ceramic Oscillator. ( $90^{\circ}$ late) |  |

- TERMINAL EXPLANATION

| PIN NO. | PIN NAME | FUNCTION | INSIDE EQUIVALENT CIRCUIT |
| :---: | :---: | :---: | :---: |
| 6 | VCO-FILTER 2 | Decide the Volume to be transfered shall by decided of Cramic Oscillator. ( $90^{\circ}$ late) |  |
| 7 | L. P. F | L. P. F. of AFC |  |
| 8 | $\mathrm{V}^{+}$ | Supply Voltage |  |
| 9 | VR-1 | AFC-HD Output Can be adjusted by putting resistor between 9 to GND ( 9 to $\mathrm{V}_{\mathrm{cc}}$ no adjustment). The pulse width cam be adjusted by making changeable of resister (Adjusting mode) |  |
| 10 | VR-2 | AFC-HD Output delay adjustment by putting 10 pin resister changeable at 9 pin ajustment mode. |  |
| 11 | GND | Ground |  |

## - TERMINAL EXPLANATION

| PIN NO. | PIN NAME | FUNCTION | INSIDE EQUIVALENT CIRCUIT |
| :---: | :---: | :---: | :---: |
| 12 | AFC, HD-OUT | AFC-HD Output |  |
| 13 | MM-VT | Pulse Width of Vsync-OUT is adjusted by setting mono multi time constant. |  |
| 14 | Vsync-OUT | Vertical Synchronous Signal Output. |  |
| 15 | FD-OUT discrimination | Field Distiniction Signal Output. |  |
| 16 | Csyne-OUT | Synchronous Separation Output |  |

## - PIN FUNCTION

| PIN NO. | FUNCTION BLOCK | OPERATIONAL DESCRIPTION | NOTE |
| :---: | :---: | :---: | :---: |
| (1)Pin | Signal Input | Video Signal input | Sync tip clump |
| (2)Pin | HD pulse control | HD pulse and FD pulse control by time constant of CR |  |
| (3) Pin | HD pulse output | 1/2 f f killer HD pulse output | In a period of vertical synchronizing, a $\mathrm{f}_{\mathrm{H}}$ is converted to $\mathrm{f}_{\mathrm{H}}$ |
| $\begin{aligned} & \text { (4) Pin } \\ & \text { (5) Pin } \\ & \text { (6) Pin } \end{aligned}$ | AFC Oscillation | Oscillation of 503 KHz by a ceramic oscillator, and divided by 32 to get down to 15.74 KHz |  |
| (7) Pin | AFC control | Leg Lead filter for phase detection |  |
| (8)Pin | V Cc | Vcc |  |
| (9)Pin | AFC HD output Switch (AFC HD pulse width adjustment) | The case that $R$ is connected between 9pin and $V_{c c} \cdots$ Fixed output <br> The case that $R$ is connected between 9pin and GND $\cdots$ Adjustable AFC HD Delay Mode | High Resistance $\rightarrow$ Wide pulse width Low Resistance $\rightarrow$ Narrow pulse width |
| (10) Pin | AFC HD Delay adjustment | The case that $R$ is connected between 9pin and GND $\cdots$ Adjustable AFC HD Delay output | High Resistance $\rightarrow$ AFC HD Delay time gains Low Resistance $\rightarrow$ AFC HD Delay time loses |
| (11) Pin | GND | GND |  |
| (12) Pin | AFC HD output | AFC HD pulse output | Positive polarity |
| (13) Pin | VD pulse width adujstment | VD pulse width control by time constant of CR |  |
| (14) Pin | VD output | Vertical synchronizing signal output | Positive polarity |
| (15) Pin | FD output | Field discriminating signal output | odd field $\rightarrow$ High Output even field $\rightarrow$ Low Output |
| (16) Pin | C Sync. output | Composite Sync Signal output | Positive polarity |

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