High Voltage Multi-Topology LED Driver

General Description

The RT8463 is a current mode PWM regulator for LED driving applications. With a 2A power switch, wide input voltage (4.5V to 50V) and output voltage (up to 50V) ranges, the RT8463 can operate in any of the three common topologies : Buck, Boost or Buck-Boost.

With 470kHz operating frequency, the size of the external PWM inductor and input/output capacitors can be minimized. High efficiency is achieved by a 100mV current sensing control.

Brightness dimming can be controlled from either analog or PWM signal. A unique built-in clamping comparator and filtering resistor allow easy low noise analog dimming conversion from PWM signal with only one external capacitor.

The RT8463 is available in the TSSOP-14 (Exposed pad) and WDFN-12L 3x3 packages.

Ordering Information

RT8463□□

- Package Type
  - CP : TSSOP-14 (Exposed Pad)
  - QW : WDFN-12L 3x3 (W-Type)
- Lead Plating System
  - G : Green (Halogen Free and Pb Free)

Note :

Richtek products are :

- RoHS compliant and compatible with the current requirements of IPC/JEDEC J-STD-020.
- Suitable for use in SnPb or Pb-free soldering processes.

Features

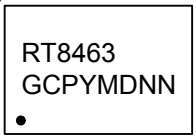
- **High Voltage : V_{IN} Up to 50V, V_{OUT} Up to 50V**
- **Buck, Boost or Buck-Boost Operation**
- **Built-In 2A Power Switch**
- **Current Mode PWM Control**
- **470kHz Fixed Switching Frequency**
- **Easy Dimming : Analog, PWM Digital or PWM Converting to Analog with One External Capacitor**
- **Adjustable Soft-Start to Avoid Inrush Current**
- **Adjustable Over Voltage Protection to Limit Output Voltage**
- **Thermal Shutdown**
- **Under Voltage Lockout**
- **RoHS Compliant and Halogen Free**

Applications

- GPS, Portable DVD Backlight
- Desk Lights and Room Lighting
- Industrial Display Backlight

Marking Information

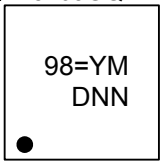
RT8463GCP



RT8463GCP : Product Number

YMDNN : Date Code

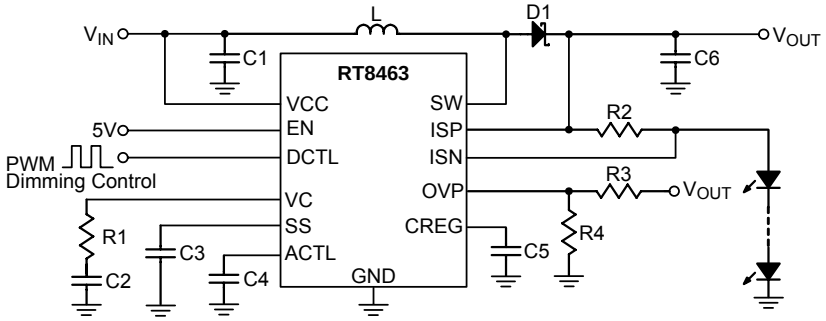
RT8463GQW



98 = : Product Code

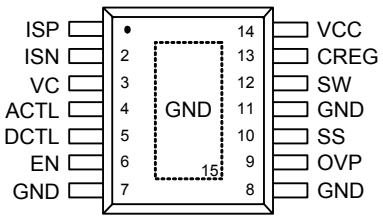
YMDNN : Date Code

Simplified Application Circuit

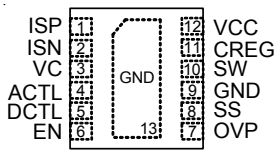


Pin Configurations

(TOP VIEW)



TSSOP-14 (Exposed Pad)

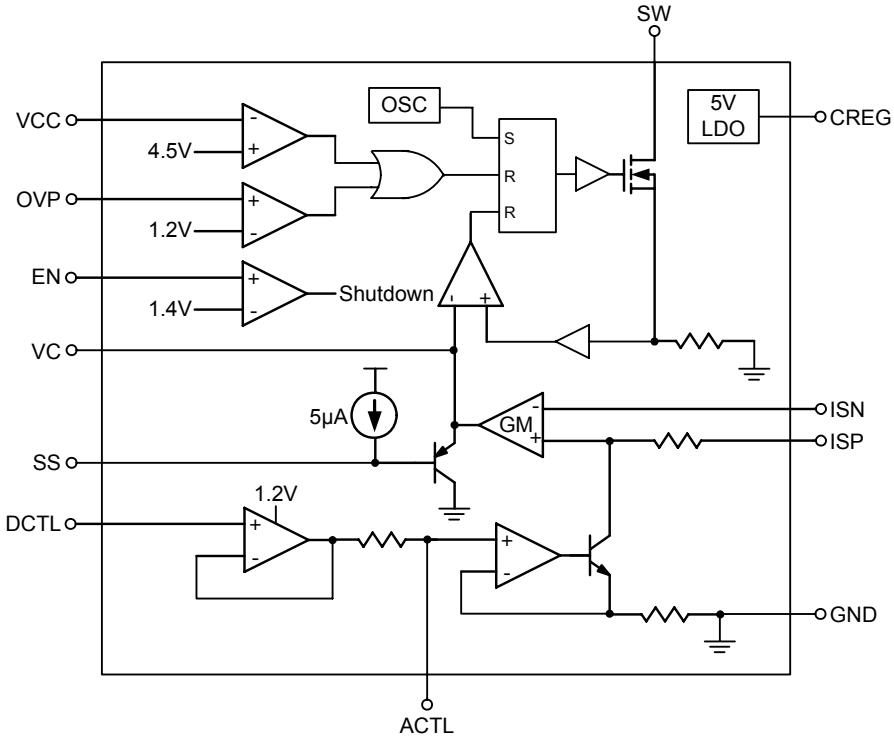


WDFN-12L 3x3

Functional Pin Description

Pin No.		Pin Name	Pin Function
TSSOP-14 (Exposed Pad)	WDFN-12L 3x3		
1	1	ISP	Positive Current Sense Input.
2	2	ISN	Negative Current Sense Input. Voltage threshold between ISP and ISN is 100mV.
3	3	VC	Compensation Node for PWM Boost Converter Loop.
4	4	ACTL	Analog Dimming Control Input. Effective programming range is between 0.2V and 1.2V.
5	5	DCTL	Digital Dimming Control Input. By adding a 0.47μF filtering capacitor on the ACTL pin, the PWM dimming signal on DCTL pin will be averaged and converted into analog dimming signal on the ACTL pin. V_{ACTL} = 1.2V x PWM dimming duty cycle.
6	6	EN	Enable Control Input (Active High). When this pin is low, the chip is in shutdown mode.
7, 8, 11, 15 (Exposed Pad)	9, 13 (Exposed Pad)	GND	Ground. The exposed pad must be soldered to a large PCB and connected to GND for maximum power dissipation.
9	7	OVP	Over Voltage Protection Sense Input. The PWM Boost converter turns off when V_{OVP} goes higher than 1.2V.
10	8	SS	Soft-Start Time Setting. A minimum 10nF capacitor is required for soft-start.
12	10	SW	Switch Node of PWM Boost Converter.
13	11	CREG	Regulator Output for Internal Circuit. Placed a 1μF capacitor to stabilize the 5V output regulator.
14	12	VCC	Power Supply Voltage Input. For good bypass, a low ESR capacitor is required.

Function Block Diagram



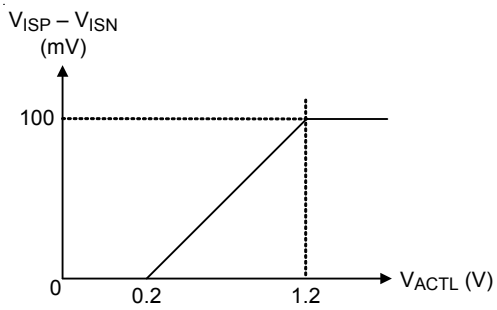


Figure 1

Operation

The RT8463 is specifically designed to be operated in Buck, Boost and Buck-Boost converter applications. This device uses a fixed frequency, current mode control scheme to provide excellent line and load regulations. The control loop has a current sense amplifier to sense the voltage between the ISP and ISN pins and provides an output voltage at the VC pin. A PWM comparator then turns off the internal power switch when the sensed power switch current exceeds the compensated VC pin voltage. The power switch will not reset by the oscillator clock in each cycle. If the comparator does not turn off the switch in a cycle, the power switch is on for more than a full switching period until the comparator is tripped. In this manner, the programmed voltage across the sense resistor is regulated by the control loop.

The current through the sense resistor is set by the programmed voltage and the sense resistance. The voltage across the sense resistor can be programmed by either the analog or PWM signals at the ACTL pin, or the PWM signal at the DCTL pin.

The RT8463 provides protection functions which include over temperature, input voltage under voltage, output voltage over voltage, and switch current limit.

Absolute Maximum Ratings (Note 1)

- Supply Input Voltage, VCC ---------- –0.3V to 60V
- SW Pin Voltage at Switching Off, ISP, ISN ---------- –0.3V to 60V
- DCTL, ACTL, CREG, OVP Pin Voltage ---------- –0.3V to 5.5V (Note 2)
- EN Pin Voltage ---------- –0.3V to 20V
- Power Dissipation, P_D @ T_A = 25°C
  - TSSOP-14 (Exposed Pad) ---------- 3.32W
  - WDFN-12L 3x3 ---------- 3.28W
- Package Thermal Resistance (Note 3)
  - TSSOP-14 (Exposed Pad), θ_{JA} ---------- 30.1°C/W
  - TSSOP-14 (Exposed Pad), θ_{JC} ---------- 7.5°C/W
  - WDFN-12L 3x3, θ_{JA} ---------- 30.5°C/W
  - WDFN-12L 3x3, θ_{JC} ---------- 7.5°C/W
- Junction Temperature ---------- 150°C
- Lead Temperature (Soldering, 10 sec.) ---------- 260°C
- Storage Temperature Range ---------- –65°C to 150°C
- ESD Susceptibility (Note 4)
  - HBM (Human Body Model) ---------- 2kV
  - MM (Machine Model) ---------- 200V

Recommended Operating Conditions (Note 5)

- Supply Input Voltage, VCC ---------- 4.5V to 50V
- Junction Temperature Range ---------- –40°C to 125°C
- Ambient Temperature Range ---------- –40°C to 85°C

Electrical Characteristics

(V_{CC} = 12V, No Load on any Output, T_A = 25°C, unless otherwise specified)

Parameter		Symbol	Test Conditions	Min	Typ	Max	Unit
Overall							
Regulator Output Voltage		V_{CREG}	I_{CREG} = 20mA	4.5	5	5.5	V
Supply Current		I_{VCC}	VC ≤ 0.2V (Not Switching)	--	--	5	mA
VIN Under Voltage Lockout Threshold		V_{UVLO}	V_{IN} Rising	--	4.2	--	V
			V_{IN} Falling	--	3.8	--	
Shutdown Current		I_{SHDN}	V_{EN} < 0.5V	--	--	15	μA
EN Input Voltage	Logic-High	V_{EN_H}		2	--	--	V
	Logic-Low	V_{EN_L}		--	--	0.5	
EN Input Current			V_{EN} > 2V	--	--	1	μA
Current Sense Amplifier							
Input Threshold (V_{ISP} – V_{ISN})			V_{ACTL} ≥ 1.25V	96	100	102	mV
			V_{ACTL} = 1.2V	95	98	101	

Parameter		Symbol	Test Conditions	Min	Typ	Max	Unit
Input Current		I_{ISP}	V_{ISP} = 24V	--	200	--	μA
Input Current		I_{ISN}	V_{ISN} = 24V	--	20	--	μA
Output Current		I_{VC}	2V > VC > 0.2V	--	±10	--	μA
VC Threshold for PWM Switch Off				--	0.2	--	V
LED Dimming							
Analog Dimming ACTL Pin Input Current		I_{ACTL}	$0 \le V_{ACTL} \le 3V$, DCTL Floating	--	--	2	μA
LED Current On Threshold at ACTL		V_{ACTL_ON}	$(V_{ISP} - V_{ISN})$ = 100mV	--	1.2	1.33	V
LED Current Off Threshold at ACTL		V_{ACTL_OFF}		--	0.2	0.25	V
DCTL Input Current		I_{DCTL}	$0.3V \le V_{DCTL} \le 5V$	--	0.5	2	μA
DCTL Input Voltage	Logic-High	V_{DCTL_H}		2	--	--	V
	Logic-Low	V_{DCTL_L}		--	--	0.1	
PWM Boost Converter							
Switching Frequency		f_{SW}		420	470	520	kHz
Maximum Duty Cycle		D_{MAX}		--	--	100	%
Minimum On-Time (Note 6)				--	150	250	ns
SW $R_{DS(ON)}$				--	0.3	0.5	Ω
SW Current Limit		I_{LIM_SW}		2	2.5	--	A
OVP and Soft-Start							
OVP Threshold		V_{OVP}		1.15	1.2	1.25	V
OVP Input Current		I_{OVP}	$V_{OVP} \le 1.5V$	--	--	50	nA
Soft-Start SS Pin Current		I_{SS}	$V_{SS} \le 2.5V$	--	5	8	μA
Temperature Protection							
Thermal Shutdown Temperature		T_{SD}		--	150	--	°C
Thermal Shutdown Hysteresis		ΔT_{SD}		--	20	--	°C

Note 1. Stresses beyond those listed "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

Note 2. If connected with a 20kΩ serial resistor, ACTL and DCTL can go up to 40V.

Note 3. θ_{JA} is measured at T_A = 25°C on a high effective thermal conductivity four-layer test board per JEDEC 51-7. θ_{JC} is measured at the exposed pad of the package.

Note 4. Devices are ESD sensitive. Handling precaution is recommended.

Note 5. The device is not guaranteed to function outside its operating conditions.

Note 6. Guaranteed by design, not subjected to production test.

Typical Application Circuit

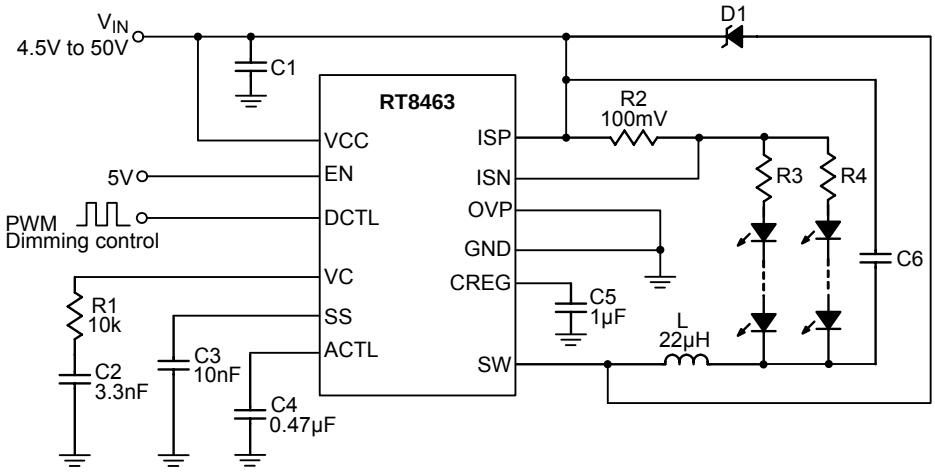


Figure 2. PWM to Analog Dimming Buck Configuration

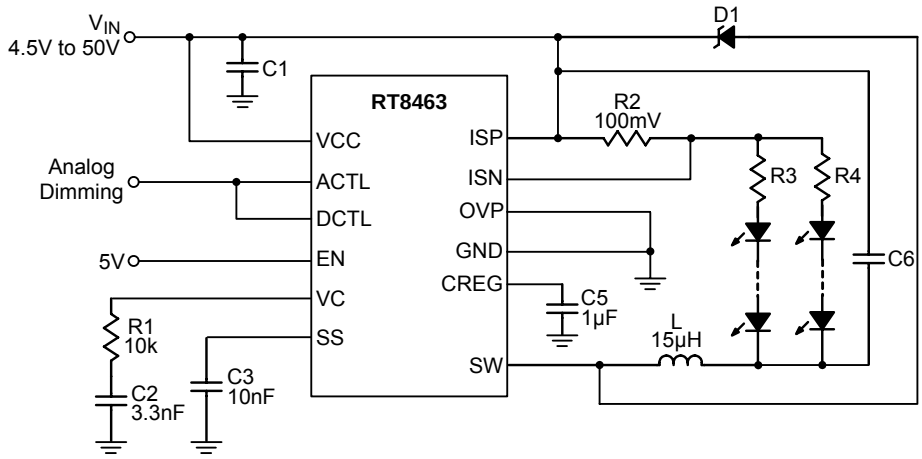


Figure 3. Analog Dimming Buck Configuration

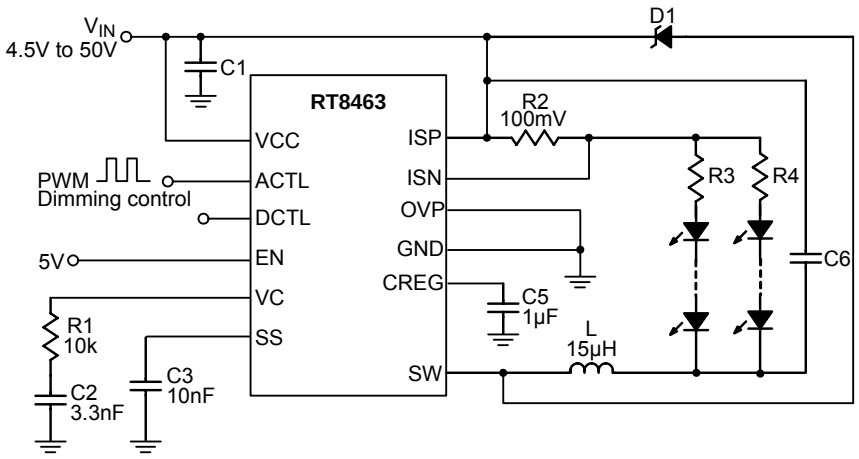


Figure 4. PWM Dimming Buck Configuration Through ACTL Pin

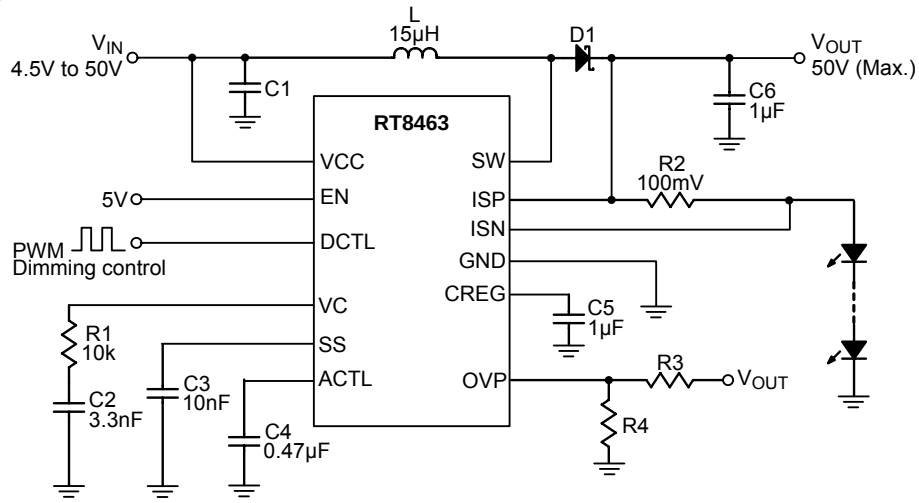


Figure 5. PWM to Analog Dimming Boost Configuration

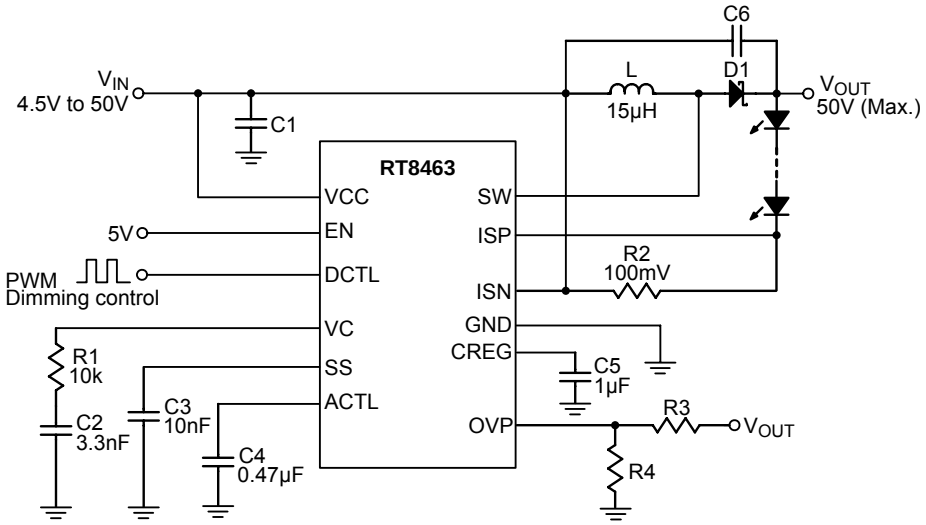
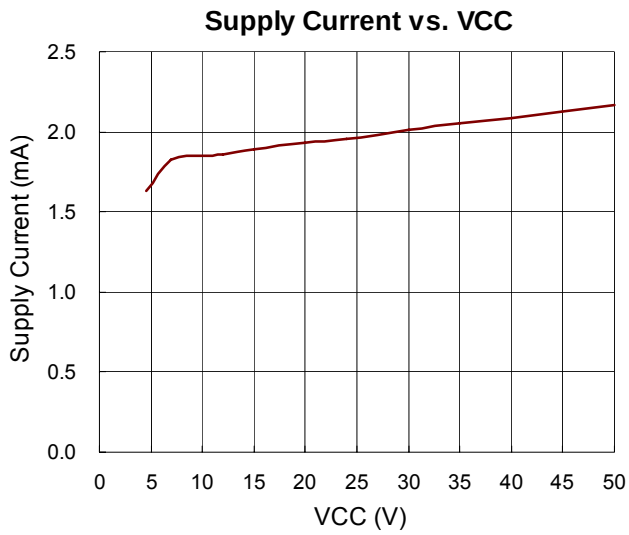
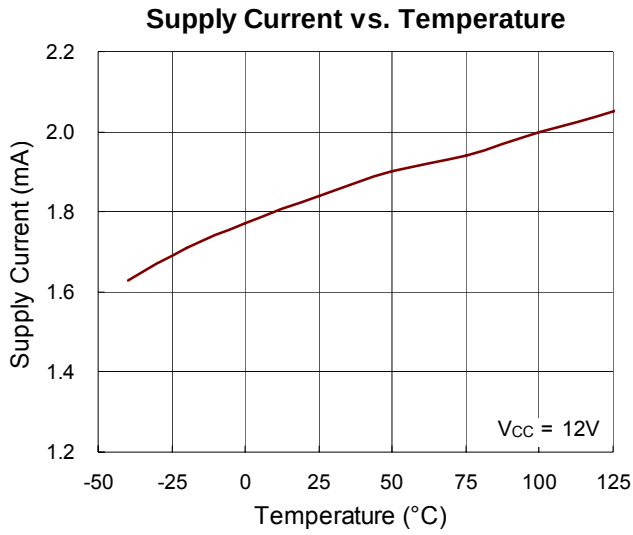
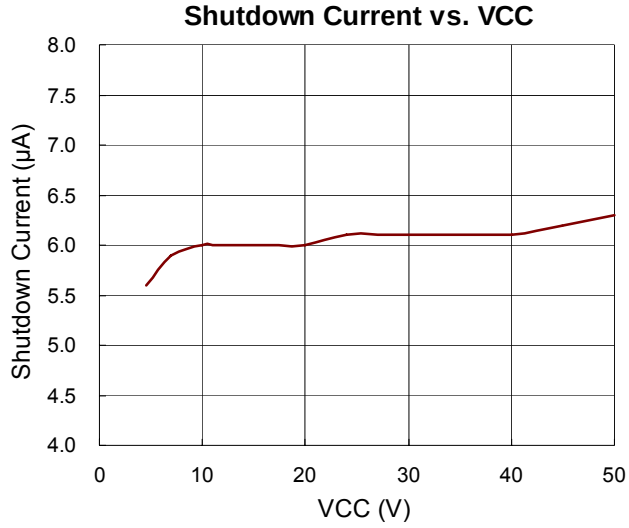


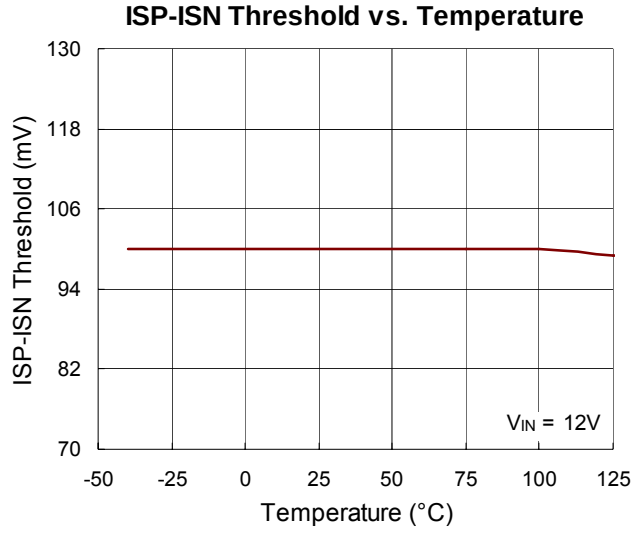
Figure 6. PWM to Analog Dimming Buck-Boost Configuration

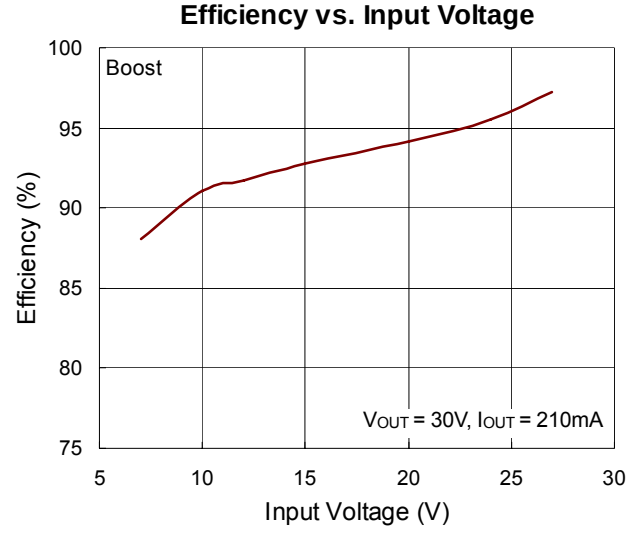
Typical Operating Characteristics

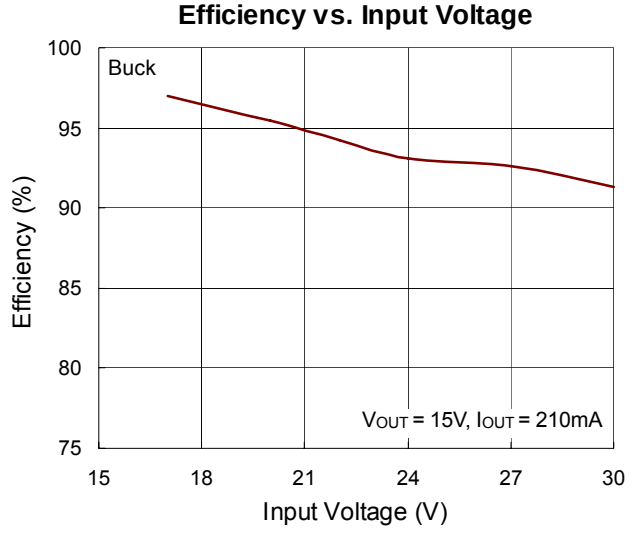




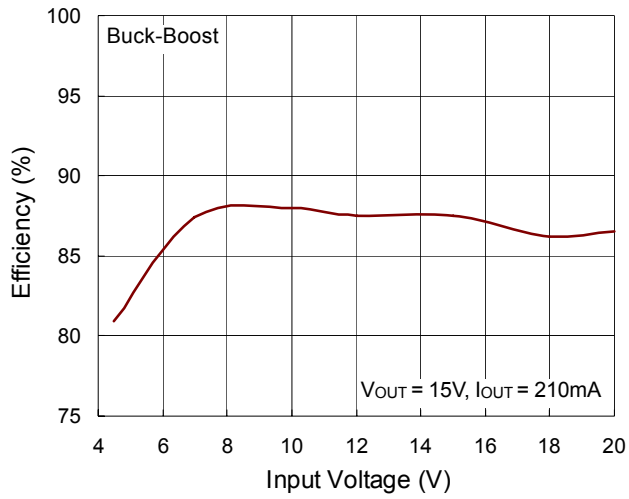




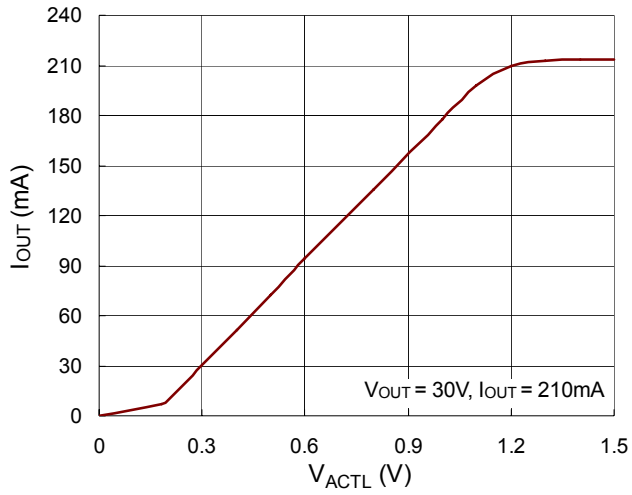




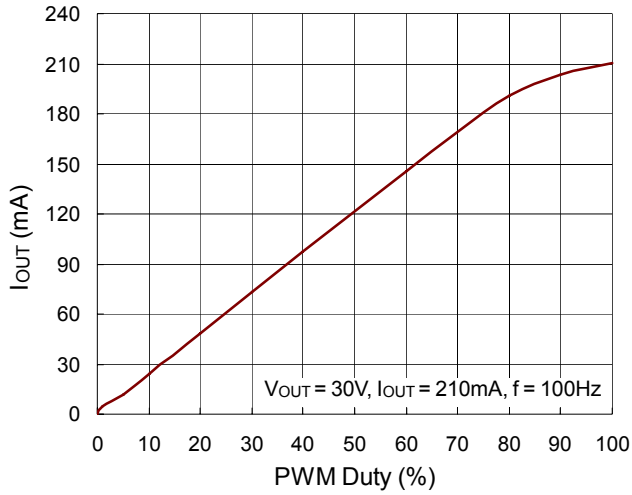
Efficiency vs. Input Voltage



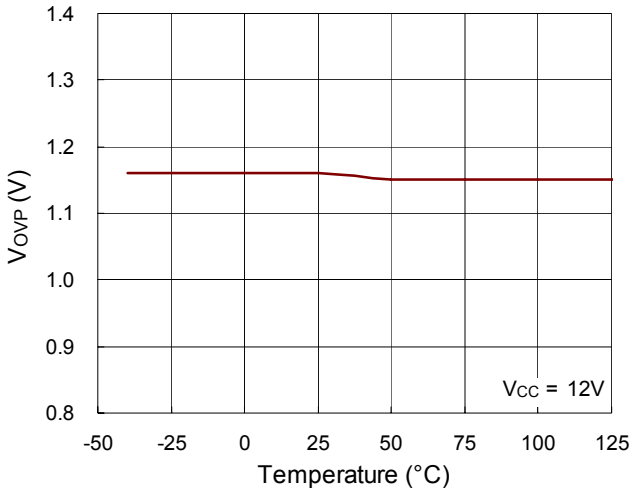
IOUT vs. VACTL



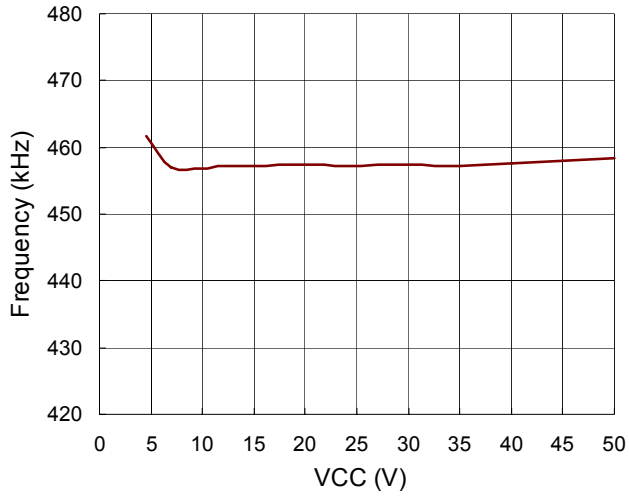
IOUT vs. VDCTL



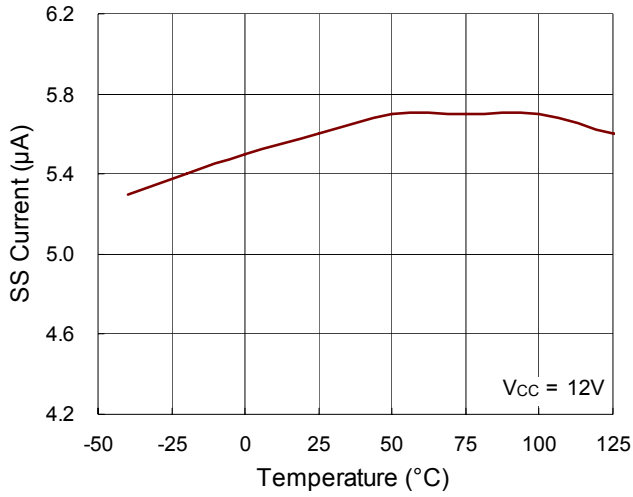
VOVP vs. Temperature



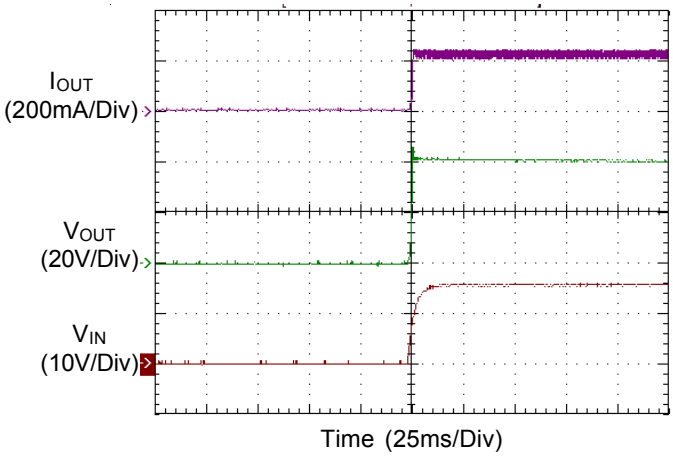
Frequency vs. VCC



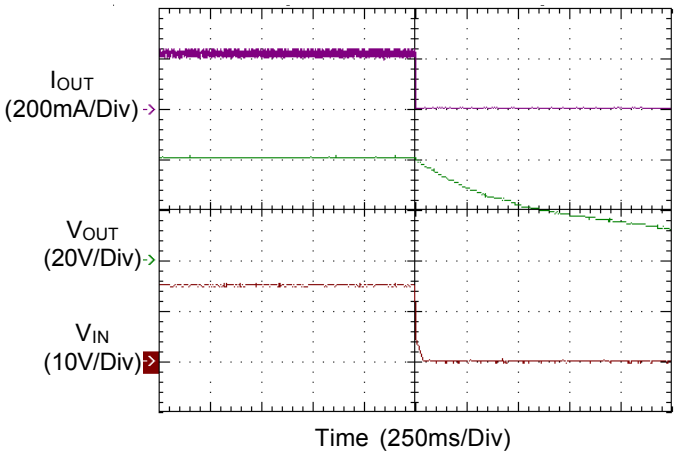
SS Current vs. Temperature



Power On from VIN



Power Off from VIN



Application Information

Loop Compensation

The RT8463 has an external compensation pin (VC) allowing the loop response optimized for specific application. An external resistor in series with a capacitor is connected from the VC pin to GND to provide a pole and a zero for proper loop compensation. The recommended compensation resistance and capacitance for the RT8463 are 10kΩ and 3.3nF.

Soft-Start

The soft-start can be achieved by connecting a capacitor from the SS pin to GND. The built-in soft-start circuit reduces the start-up current spike and output voltage overshoot. The soft-start time is determined by the external capacitor charged by an internal 5μA constant charging current. The SS pin directly limits the slew rate of voltage on the VC pin, which in turn limits the peak switch current. The value of the soft-start capacitor is user defined to satisfy the designer's requirements.

LED Current Setting

The LED current could be calculated by the following equation :

$$I_{LED(MAX)} = \frac{V\,(ISP - ISN)}{R2}$$

where V (ISP – ISN) is the voltage between ISP and ISN (100mV typ. if ACTL or DCTL dimming is not applied) and the R2 is the resister between ISP and ISN.

Brightness / Dimming Control

The RT8463 features both analog and digital dimming control. Analog dimming is linearly controlled by an external voltage (0.2V < V_{ACTL} < 1.2V). With an on-chip output clamping amplifier and a resistor, PWM dimming signal fed at DCTL pin can be easily filtered to an analog dimming signal with an external capacitor from the ACTL pin to GND for noise-free PWM dimming. A very high contrast ratio true digital PWM dimming can be achieved by driving the ACTL pin with a PWM signal from 100Hz to 10kHz.

Output Over Voltage Setting

The RT8463 is equipped with Over Voltage Protection (OVP) function. When the voltage at OVP pin exceeds a threshold of approximately1.2V, the power switch is turned off. The power switch can be turned on again once the voltage at OVP pin drops below 1.2V.

For the Boost application, the output voltage could be clamped at a certain voltage level. The OVP voltage can be set by the following equation :

$$V_{OUT\_OVP} = 1.2 \times (1 + \frac{R3}{R4})$$

where R3 and R4 are the voltage divider from V_{OUT} to GND with the divider center node connected to the OVP pin.

Current Limit Protection

The RT8463 can limit the peak switch current by the internal over current protection feature. In normal operation, the power switch is turned off when the switch current reaches the loop-set value. The maximum peak-current limit of the switch is 2.5A (typ.).

Over Temperature Protection

The RT8463 provides Over Temperature Protection (OTP) function to prevent the excessive power dissipation from overheating. The OTP function will shut down switching operation when the die junction temperature exceeds 150°C. The chip will automatically start to switch again when the die junction temperature cools off.

Inductor Selection

Choose an inductor that can handle the necessary peak current without saturating, and ensure that the inductor has a low DCR (copper wire resistance) to minimize I^2R power losses. Inductor manufacturers specify the maximum current rating as the current where the inductance falls to certain percentage of its nominal value (65% typ.).

Table 1. Relevant Parameters for Buck, Boost, and Buck – Boost Topologies

	Buck	Boost	Buck – Boost
Duty Cycle : D	$\frac{V_{OUT}}{V_{IN}+V_F}$	$\frac{V_{OUT}-V_{IN}+V_F}{V_{OUT}+V_F}$	$\frac{V_{OUT}+V_F}{V_{IN}+V_{OUT}+V_F}$
Average Inductor Current : I_L	I_{OUT}	$\frac{I_{OUT}}{1-D}$	$\frac{I_{OUT}}{1-D}$
ΔI (A)	$\frac{V_{OUT}+V_F}{L\times f_{SW}}\times(1-D)$	$\frac{V_{OUT}+V_F}{L\times f_{SW}}\times D\,(1-D)$	$\frac{V_{OUT}+V_F}{L\times f_{SW}}\times(1-D)$
$\gamma=\frac{\Delta I\,(A)}{I_L}$	$\frac{V_{OUT}+V_F}{I_{OUT}\times L\times f_{SW}}\times(1-D)$	$\frac{V_{OUT}+V_F}{I_{OUT}\times L\times f_{SW}}\times D\,(1-D)^2$	$\frac{V_{OUT}+V_F}{I_{OUT}\times L\times f_{SW}}\times(1-D)^2$
$I_{PK}\ (A)=I_L\times(1+\frac{\gamma}{2})$	$I_{OUT}\times(1+\frac{\gamma}{2})$	$\frac{I_{OUT}}{1-D}\times(1+\frac{\gamma}{2})$	$\frac{I_{OUT}}{1-D}\times(1+\frac{\gamma}{2})$
L (H)	$\frac{V_{OUT}+V_F}{I_{OUT}\times\gamma\times f_{SW}}\times(1-D)$	$\frac{V_{OUT}+V_F}{I_{OUT}\times\gamma\times f_{SW}}\times D\,(1-D)^2$	$\frac{V_{OUT}+V_F}{I_{OUT}\times\gamma\times f_{SW}}\times(1-D)^2$

γ : Current ripple ratio, set γ = 1 for typical peak current disign.

f_{SW} : Switch Frequency

V_F : Forward voltage drop of the output rectifier.

V_{IN} : Nominal input voltage.

V_{OUT} : Desired output voltage.

I_{OUT} : Desired output current.

I_{PK} : Peak current of Inductor.

L : Minimum Desired Inductor value.

Table1, shows the relevant parameters for Buck, Boost and Buck – Boost topologies. The first column is for the basic definition of the terms.

The peak inductor current depends on the different topologies. For a Buck converter the average value of the inductor current equals the load current, irrespective of the input voltage. When as the input increases, the peak current increases.

The inductor must be selected with a saturation current rating greater than the peak current limit.

Schottky Diode Selection

The Schottky diode, with low forward voltage drop and fast switching speed, is necessary for the RT8463 applications. In addition, power dissipation, reverse voltage rating and pulsating peak current are the important parameters of the Schottky diode that must be considered. Choose a suitable Schottky diode whose reverse voltage rating is greater than the maximum output voltage. The diode's average current rating must exceed the average output current. The diode conducts current only when the power switch is turned off (typically less than 50% duty cycle).

Capacitor Selection

The input capacitor reduces current spikes from the input supply and minimizes noise injection to the converter. For most RT8463 applications, a 4.7μF ceramic capacitor is sufficient. A higher or lower value may be used depending on the noise level from the input supply and the input current to the converter.

In Boost application, the output capacitor is typically a ceramic capacitor and is selected based on the output voltage ripple requirements. The minimum value of the output capacitor, C_{OUT}, is approximately given by the following equation :

$$C_{OUT} = \frac{I_{LED}\times D\times T}{V_{RIPPLE}}$$

Thermal Considerations

For continuous operation, do not exceed absolute maximum junction temperature. The maximum power dissipation depends on the thermal resistance of the IC package, PCB layout, rate of surrounding airflow, and difference between junction and ambient temperature. The maximum power dissipation can be calculated by the following formula :

$P_{D(MAX)} = (T_{J(MAX)} - T_A) / \theta_{JA}$

where $T_{J(MAX)}$ is the maximum junction temperature, T_A is the ambient temperature, and θ_{JA} is the junction to ambient thermal resistance.

For recommended operating condition specifications, the maximum junction temperature is 125°C. The junction to ambient thermal resistance, θ_{JA}, is layout dependent. For TSSOP-14 (Exposed Pad) package, the thermal resistance, θ_{JA}, is 30.1°C/W on a standard JEDEC 51-7 four-layer thermal test board. For WDFN-12L 3x3 package, the thermal resistance, θ_{JA}, is 30.5°C/W on a standard JEDEC 51-7 four-layer thermal test board. The maximum power dissipation at T_A = 25°C can be calculated by the following formula :

$P_{D(MAX)}$ = (125°C – 25°C) / (30.1°C/W) = 3.32W for TSSOP-14 (Exposed Pad) package

$P_{D(MAX)}$ = (125°C – 25°C) / (30.5°C/W) = 3.28W for WDFN-12L 3x3 package

The maximum power dissipation depends on the operating ambient temperature for fixed $T_{J(MAX)}$ and thermal resistance, θ_{JA}. The derating curve in Figure 7 allows the designer to see the effect of rising ambient temperature on the maximum power dissipation.

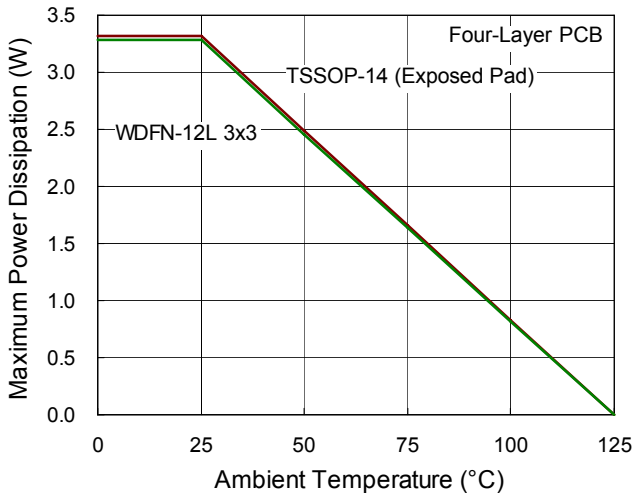


Figure 7. Derating Curve of Maximum Power Dissipation

Layout Consideration

PCB layout is very important to design power switching converter circuits. The recommended layout guidelines are listed as follows :

- The power components L1, D1, C_{VIN}, and C_{OUT} must be placed as close to each other as possible to reduce the ac current loop area. The PCB trace between power components must be as short and wide as possible due to large current flow through these traces during operation.
- Place L1 and D1 connected to SW pin as close as possible. The trace should be as short and wide as possible.
- The input capacitors C1 must be placed as close to VCC pin as possible.
- Place the compensation components to the VC pin as close as possible to avoid noise pick up.

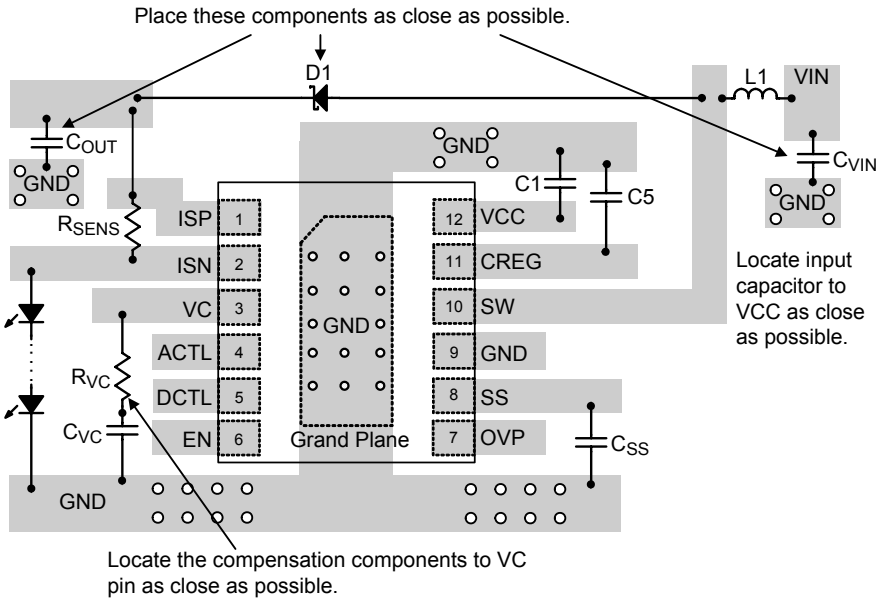
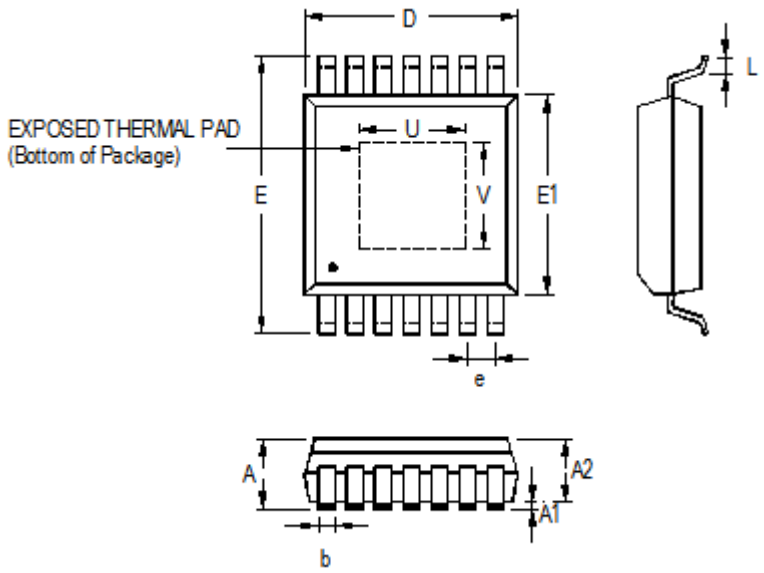


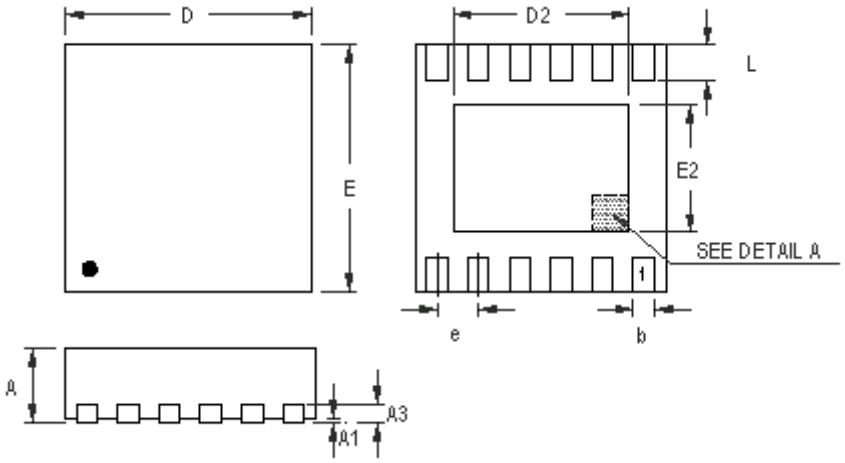
Figure 8. PCB Layout Guide for WDFN-12L 3x3

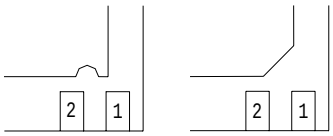
Outline Dimension



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	1.000	1.200	0.039	0.047
A1	0.000	0.150	0.000	0.006
A2	0.800	1.050	0.031	0.041
b	0.190	0.300	0.007	0.012
D	4.900	5.100	0.193	0.201
e	0.650		0.026	
E	6.300	6.500	0.248	0.256
E1	4.300	4.500	0.169	0.177
L	0.450	0.750	0.018	0.030
U	1.900	2.900	0.075	0.114
V	1.600	2.600	0.063	0.102

14-Lead TSSOP (Exposed Pad) Plastic Package





DETAIL A

Pin #1 ID and Tie Bar Mark Options

Note : The configuration of the Pin #1 identifier is optional, but must be located within the zone indicated.

Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.700	0.800	0.028	0.031
A1	0.000	0.050	0.000	0.002
A3	0.175	0.250	0.007	0.010
b	0.150	0.250	0.006	0.010
D	2.950	3.050	0.116	0.120
D2	2.300	2.650	0.091	0.104
E	2.950	3.050	0.116	0.120
E2	1.400	1.750	0.055	0.069
e	0.450		0.018	
L	0.350	0.450	0.014	0.018

W-Type 12L DFN 3x3 Package

Richtek Technology Corporation

5F, No. 20, Taiyuen Street, Chupei City

Hsinchu, Taiwan, R.O.C.

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