OXFORD SEMICONDUCTOR

Data Sheet

OXU200
USB High-Speed Peripheral Controller

Features

- High-speed USB peripheral controller
- Compatible with the *Universal Serial Bus Specification, Revision 2.0*
- Single 3.3 V power supply, flexible I/O voltage of 1.65 V to 3.6 V (LVCMOS/TTL) to interface to a wide range of CPUs and DSPs
- 16-bit memory mapped interface can gluelessly interface to most popular microprocessors and DSPs
- 8 Kbytes of on-chip SRAM buffer, optimized for performance and cost
- DMA slave channel lowers CPU utilization
- Allows up to 8 bi-directional endpoints for support of multi-function systems
- Transfer-oriented control model handles all USB signaling and packetization, minimizes CPU loading
- Low power operation, suitable for mobile applications
- Ultra-low-power sleep mode and power-saving suspend state
- Integrated PLL supports 12 MHz external crystal or crystal oscillator
- Small package and footprint saves board space
  - 12×12 mm LQFP, 100-pin, RoHS compliant
  - 6×6 mm BGA, 64-ball, RoHS compliant
- Fast microprocessor access cycle and multi-buffering support for all four types of USB transfers
- Operating temperature range: -40° to 85° C

Device Overview

The Oxford Semiconductor OXU200 is a low-cost, single-port USB high-speed peripheral controller. It is designed for high performance and enables embedded systems to perform high-speed USB data transfers for peripheral connectivity when connected to a USB host.

The low-power, high-performance design and small package size make the OXU200 ideal for adding high-speed USB into a broad range of mobile consumer electronics, including cell phones, portable GPS devices, and PDAs.

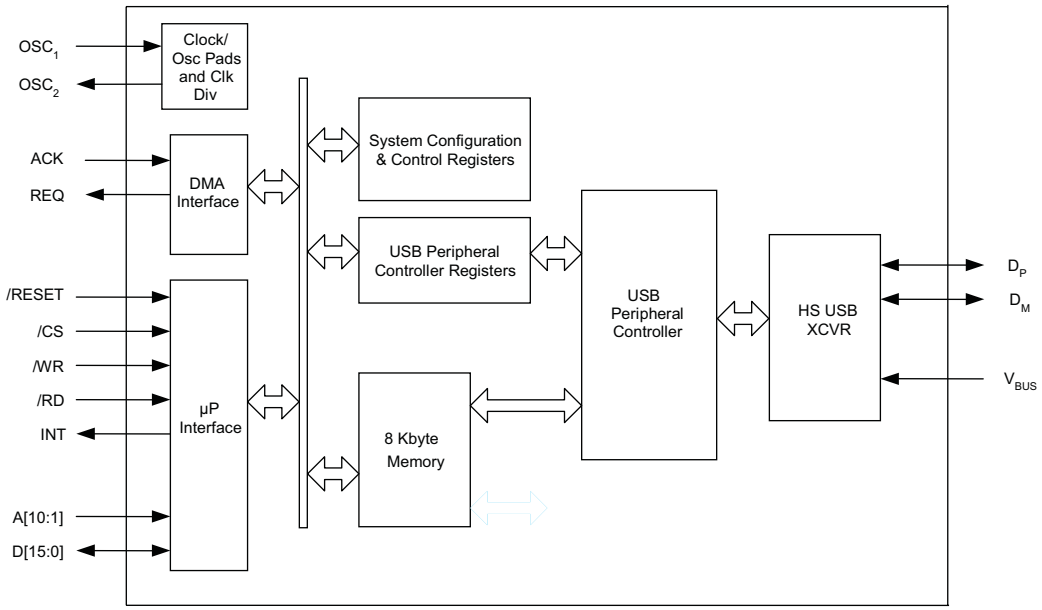
The OXU200 has a 16-bit SRAM-like memory-mapped interface and flexible I/O voltage that can connect gluelessly to most popular CPUs and DSPs. The 8 Kbytes of on-chip SRAM buffer is cost and performance optimized to reduce system interrupts and minimize processor overhead.

Software solutions for the OXU200 include USB device drivers and the Oxford Semiconductor USBLink™ product suite. USBLink Peripheral has been ported to a wide variety of real time operating systems including VxWorks®, ThreadX®, and Nucleus®.

In addition, Oxford Semiconductor also makes available low-level controller drivers for other native USB stacks such as those included with Windows® CE 5.0 and Linux® 2.6.x.

Figure 1 shows the OXU200 architectural diagram.

Figure 1 OXU200 Architectural Diagram



Development Support

The OXU200 product suite includes the USB controller as well as the protocol stacks and the driver software that enable a wide variety of USB applications. This unique ability to deliver a total hardware and software solution sets Oxford Semiconductor apart from other semiconductor companies and benefits customers by:

- Shortening time to market
- Reducing risk
- Offering a single source for hardware and software, thereby reducing the number of suppliers the customer has to deal with

Oxford Semiconductor is a Microsoft® Windows® Embedded Partner and has developed peripheral controller drivers for Windows CE 5.0. Similar software support is also available for Linux® 2.6.x.

For customers using a real time operating system (RTOS) such as VxWorks®, ThreadX®, Nucleus®, OSE, LynxOS® and AMX™ among others, Oxford Semiconductor offers its USBLink peripheral software solution.

The USBLink Product Suite is a modularized approach to providing USB connectivity for a wide variety of embedded products. Due to its flexible architecture and broad based support for USB host, peripheral and OTG applications, Oxford Semiconductor can tailor the USBLink software deliverables to meet each customer's USB requirements.

The USBLink solutions are configurable and can support systems with:

- Big or little endian processors
- DMA or non-DMA USB controllers
- A wide variety of USB controllers, including the OXU200
- A broad range of operating systems

Oxford Semiconductor has over eight years of experience developing embedded USB technology. Its USBLink software has been ported to over twenty different operating systems and a wide variety of embedded architectures. USBLink is shipping in many millions of units.

Sample Applications

- Cell phones
- Personal Digital Assistants (PDA)
- Portable media players
- Portable GPS systems

Electrical Characteristics

Table 1 to Table 6 detail the required operating conditions for the device and the DC and AC electrical characteristics.

Table 1 Absolute Maximum Device Ratings

Symbol	Parameter	Condition	Min	Max	Unit
$V_{DD3.3}$	3.3 V power supply		-0.3	4.0	V
$V_{DD1.8}$	1.8 V power supply		-0.3	2.16	V
V_{DDW}	Wide-range I/O power supply		-0.3	4.0	V
V_I	DC input voltage		-0.3	4.0	V
T_S	Storage temperature		-40	+150	°C

Note: Permanent device damage may occur if absolute maximum ratings are exceeded. Functional operation should be restricted to the normal operating conditions specified in the following section. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 2 Recommended Operating Conditions

Symbol	Parameter	Condition	Min	Max	Unit
$V_{DD3.3}$	3.3 V power supply		2.97	3.63	V
$V_{DD1.8}$	1.8 V power supply		1.62	1.98	V
V_{DDW}	Wide-range I/O power supply		1.62	3.63	V
$V_{I3.3}$	DC input voltage of 3.3 V pins		0	3.6	V
V_{IW}	DC input voltage of wide-range pins		0	$1.1*V_{DDW}$	V
T_O	Operating temperature		-40	+85	°C

Table 3 DC Characteristics, High-Speed USB I/O Signals: D_P and D_M Only

Symbol	Parameter	Condition	Min	Max	Unit
V_{HSDIFF}	High-speed differential input sensitivity	$\lvert V_{I(DP)} - V_{I(DM)} \rvert$	300		mV
V_{HSCM}	High-speed data signaling common mode range		-50	500	mV
V_{HSSQ}	High-speed squelch detection threshold	Squelch detected		100	mV
		No squelch detected	150		mV
V_{HSIO}	High-speed idle output voltage (differential)		-10	10	mV
V_{HSOL}	High-speed low-level output voltage (differential)		-10	10	mV
V_{HSOH}	High-speed high-level output voltage (differential)		-360	400	mV
V_{CHIRPK}	Chirp-K output voltage (differential)		-900	-500	mV

Table 4 DC Characteristics, Logic Signals

Symbol	Parameter	Condition	Min	Max	Unit
V_{OL}	Low-level output voltage			0.4	V
V_{OH}	High-level output voltage	V_{DDW} = 3.3 V	2.4		V
		V_{DDW} = 1.8 V	0.75*V_{DDW}		V
V_{IL}	Low-level input voltage	V_{DDW} = 3.3 V		0.8	V
		V_{DDW} = 1.8 V		0.3*V_{DDW}	V
V_{IH}	High-level input voltage	V_{DDW} = 3.3 V	2.0		V
		V_{DDW} = 1.8 V	0.7*V_{DDW}		V
C_{IN}	Input capacitance		2.2 (typical)		pF
C_{OUT}	Output capacitance		2.2 (typical)		pF
C_{BI}	Bi-directional capacitance		2.2 (typical)		pF
I_{IN}	Input leakage current	No pull up or pull down	-10	10	µA

Note: The capacitances listed above do not include pad capacitance and package capacitance. One can estimate pin capacitance by adding pad capacitance of about 0.5 pF and the package capacitance, which is about 0.86 pF max for LQFP.

Table 5 DC Characteristics, Regulator

Symbol	Parameter	Condition	Min	Max	Unit
V_{rout}	Output voltage	Driving current <= 100 mA	1.8 (typical)		V
I_{rdrive}	Driving current	$V_{DD3.3A}$ = 3.3 V Output voltage = 1.8 V		150	mA
t_{rst}	Start-up time when enabled	$V_{DD3.3A}$ = 3.3 V V_{REGOUT} = 1.62 V (90%)	25 (typical)		µs

Note: The $V_{DD3.3A}$ pin that corresponds to the regulator supply is QFP pin 81.

Table 6 AC Characteristics, High-Speed D_P and D_M Driver Characteristics

Symbol	Parameter	Condition	Min	Max	Unit
t_{HSR}	High-speed differential rise time		500		ps
t_{HSF}	High-speed differential fall time		500		ps
R_{DRV}	Driver output impedance	Equivalent resistance used as internal chip	40.5	49.5	Ω

Power Consumption

Table 7 gives typical power consumption figures for the OXU200.

Table 7 OXU200 Power Consumption

	Min	Max	Unit
Peripheral operational current, High Speed		75	mA
Peripheral operational current, Full Speed		50	mA
Peripheral suspend state current	400 (typical)		µA
Power save state current	150 (typical)		µA

The above measurements are at typical process corner and room temperature and do not account for process and temperature variations.

Peripheral operational current is measured with a 5 m cable with maximum switching and BULK OUT transfer at 400 Mbps with 92.6% bus utilization during one microframe. The actual average current in customer applications will be lower.

Pin Layout

The OXU200 is supplied as a 100-pin LQFP package and as a 64-ball BGA package. Figure 2 shows the pin layout of the 100-pin OXU200-LQAG package.

Figure 2 OXU200 100-Pin LQFP Package (Top View)

Table 8 lists the LQFP pin allocations.

*Table 8 OXU200 **100-Pin LQFP** Pin Allocations (Sheet 1 of 2)*

Pin	No. Bits	Type[(1)]	Name	Description
Processor Interface (33 pins)				
2, 3, 4, 5, 8, 9, 10, 11, 13, 14, 15, 16, 96, 97, 98, 99	16	MSBCT	D_0 - D_{15}	16-bit data bus. Pull-up/pull-down can be controlled through register 0x034, bits 2:1. Default is none
22, 23, 24, 25, 28, 29, 30 32, 33, 35	10	MSID	A_1 - A_{10}	Address bus for direct address space of 2 Kbytes. Default is pull-down
20	1	MSIU	/WR	Write strobe. Pull-up can be disabled through register 0x034, bit 13. Default is pull-up
21	1	MSIU	/RD	Read strobe. Pull-up can be disabled through register 0x034, bit 13. Default is pull-up
39	1	MSIU	/CS	Chip select. Pull-up can be disabled through register 0x034, bit 13. Default is pull-up
19	1	MOCT	/INT	Interrupt to the MCU.This pin can be software configured as a driven output or open drain. Open drain is the default
86	1	MSIU	/RESET	Hardware reset. Pull-up is always enabled
89	1	MOCT	DRQ	DMA request output
90	1	MSI	ACK	DMA acknowledge. Pull-up/pull-down can be controlled through register 0x03A, bits 1:0. Default is none
General Purpose I/O (1 pin)				
88	1	BC	GPIO	General purpose I/O
Power & Ground (34 pins)				
1, 12, 27, 41, 51, 65, 75, 83	8		V_{SS}	Digital/wide-range ground
42, 47, 69, 74, 82	5		V_{SSA}	Analog ground
6, 18, 40, 53, 57, 66, 84, 100	8		$V_{DD1.8}$	1.8 V core power. V_{REGOUT} must be used for the supplies
43, 48, 70, 73, 81	5		$V_{DD3.3A}$	Analog +3.3 V power
56, 78	2		$V_{DD3.3}$	Digital +3.3 V power
7, 17, 26, 31, 85, 95	6		V_{DDW}	Wide-range I/O +1.8 V to +3.3 V. If using +1.8 V, V_{REGOUT} may be used for these supplies
USB Interface (4 pins)				
44, 45	2	B	D_P, D_M	Data lines for USB peripheral port
46	1	B	R_{REF}	Connect external reference resistor (12 KΩ +/- 1%) to V_{SSA}
72	1	5I	V_{BUS}	V_{BUS} input used by the voltage comparators of the peripheral port for connection

Table 8 OXU200 ***100-Pin LQFP*** *Pin Allocations (Sheet 2 of 2)*

Pin	No. Bits	Type[1]	Name	Description
Clock Interface (2 pins)				
50	1	I	OSC_1	Input. A 12 MHz passive crystal should be connected across the two pins (OSC_1 and OSC_2). Optionally, a 12 MHz oscillator can be connected to OSC_1 while keeping OSC_2 unconnected
49	1	O	OSC_2	Output
Internal Voltage Regulator (1 pin)				
80	1	O	V_{REGOUT}	Internal voltage regulator output of 1.8 V. This output must be connected to the $V_{DD1.8}$ supply of the chip (and may be connected to V_{DDW} if wide-range IO is at 1.8 V)
Test (2 pins)				
87	1	ID	TEST	Factory test mode. This pin should be grounded or left floating (has an internal pull-down) for normal operation. Pull-down is always enabled
64	1	I	XMODE	This pin must be grounded for normal operation
Miscellaneous (23 pins)				
91, 94, 93	3	-	$RSVD_0$, $RSVD_1$, $RSVD_2$	Reserved. These pins must be grounded
34, 36, 37, 38, 52, 54, 55, 58, 59, 60, 61, 62, 63, 67, 68, 71, 76, 77, 79, 92	20	-	NC	No connection. These pins should be left floating

Note to Table 8:

1 Type key: format is [(L)(W_)X(Y)(_Z(A))] where the following conventions apply:

L—Logic Level		W—Tolerance		X—Type		Y—Pull		Z—Drive	T—Tristate	
M[2]	Multi-voltage: 3.3 V CMOS 2.5 V CMOS 1.8 V CMOS	5	5 V	I	Input	U	Pull up	C[3]	T	Tristate
			3.3 V	O	Output	D	Pull down			Normal
S	Schmitt Trigger			B	Bidirectional		None			

2 Program to 3.3, 2.5, or 1.8 V by setting the V_{IO} voltage level.

3 Program to 2 mA, 4 mA, 6 mA, 8 mA, 10 mA, 12 mA, 14, mA, or 16 mA via the I/O Configuration Register (0x034).

Figure 3 shows the ball layout of the 64-ball OXU200-TBAG package.

Figure 3 OXU200 64-ball BGA Package (Top View)

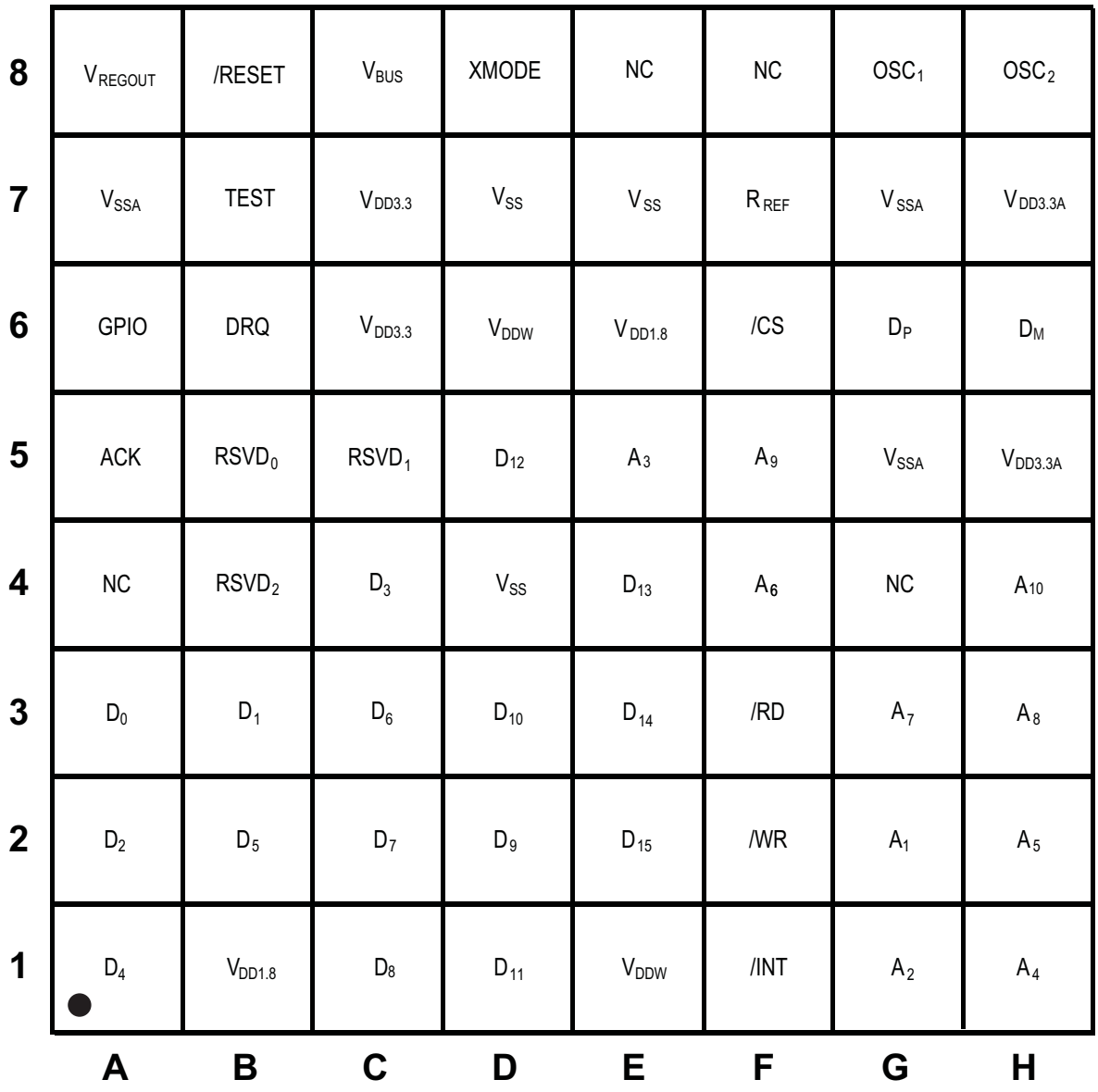


Table 9 lists the BGA ball allocations.

Table 9 OXU200 64-Ball BGA Ball Allocations (Sheet 1 of 2)

Pin	No. Bits	Type(1)	Name	Description
Processor Interface (33 pins)				
A3, B3, A2, C4, A1, B2, C3, C2, C1, D2, D3, D1, D5, E4, E3, E2	16	MSBCT	D_0 - D_{15}	16-bit data bus. Pull-up/pull-down can be controlled through register 0x034, bits 2:1. Default is none
G2, G1, E5, H1, H2, F4, G3, H3, F5, H4	10	MSID	A_1 - A_{10}	Address bus for direct address space of 2 Kbytes. Default is pull-down
F2	1	MSIU	/WR	Write strobe. Pull-up can be disabled through register 0x034, bit 13. Default is pull-up
F3	1	MSIU	/RD	Read strobe. Pull-up can be disabled through register 0x034, bit 13. Default is pull-up
F6	1	MSIU	/CS	Chip select. Pull-up can be disabled through register 0x034, bit 13. Default is pull-up
F1	1	MOCT	/INT	Interrupt to the MCU.This pin can be software configured as a driven output or open drain. Open drain is the default
B8	1	MSIU	/RESET	Hardware reset. Pull-up is always enabled
B6	1	MOCT	DRQ	DMA request output to support one channel
A5	1	MSI	ACK	DMA acknowledge. Pull-up/pull-down can be controlled through register 0x03A, bits 1:0. Default is none
General Purpose I/O (1 pin)				
A6	1	B	GPIO	General purpose I/O
Power & Ground (14 pins)				
D4, D7, E7	3		V_{SS}	Digital ground
A7, G5, G7	3		V_{SSA}	Analog ground
B1, E6	2		$V_{DD1.8}$	1.8 V core power. V_{REGOUT} must be used for the supplies
H5, H7	2		$V_{DD3.3A}$	Analog +3.3 V power
C6, C7	2		$V_{DD3.3}$	Digital +3.3 V power
D6, E1	2		V_{DDW}	Wide-range I/O +1.8 V to +3.3 V. If using +1.8 V, V_{REGOUT} may be used for the supplies
USB Interface (4 pins)				
G6, H6	2	B	D_P, D_M	Data lines for USB peripheral port
C8	1	5I	V_{BUS}	V_{BUS} input is used to detect connection to a host
F7	1	B	R_{REF}	Connect external reference resistor (12 KΩ ± 1%) to V_{SSA}

Table 9 OXU200 64-Ball BGA Ball Allocations (Sheet 2 of 2)

Pin	No. Bits	Type(1)	Name	Description
Clock Interface (2 pins)				
G8	1	I	OSC_1	Input. A 12 MHz passive crystal should be connected across the two pins (OSC_1 and OSC_2). Optionally, a 12 MHz oscillator can be connected to OSC_1 while keeping OSC_2 unconnected
H8	1	O	OSC_2	Output
Internal Voltage Regulator (1 pin)				
A8	1	O	V_{REGOUT}	Internal voltage regulator output of 1.8 V. This output must be connected to the $V_{DD1.8}$ supply of the chip (and may be connected to V_{DDW} if wide-range IO is at 1.8 V)
Test (2 pins)				
B7	1	ID	TEST	Factory test mode. This pin should be grounded or left floating (has an internal pull-down) for normal operation. Pull-down is always enabled
D8	1	I	XMODE	This pin must be grounded for normal operation
Miscellaneous (7 pins)				
B5, C5, B4	3	-	$RSVD_0$, $RSVD_1$, $RSVD_2$	Reserved. These pins must be grounded
A4, E8, F8, G4	4	-	NC	No connect. These pins should be left floating

Note to Table 9:

1 Type key: format is [(L)(W_)X(Y)(_Z(T))] where the following conventions apply:

L—Logic Level		W—Tolerance		X—Type		Y—Pull		Z—Drive	T—Tristate	
M(2)	Multi-voltage: 3.3 V CMOS 2.5 V CMOS 1.8 V CMOS	5	5 V	I	Input	U	Pull up	C(3)	T	Tristate
			3.3 V	O	Output	D	Pull down			Normal
S	Schmitt Trigger			B	Bidirectional		None			

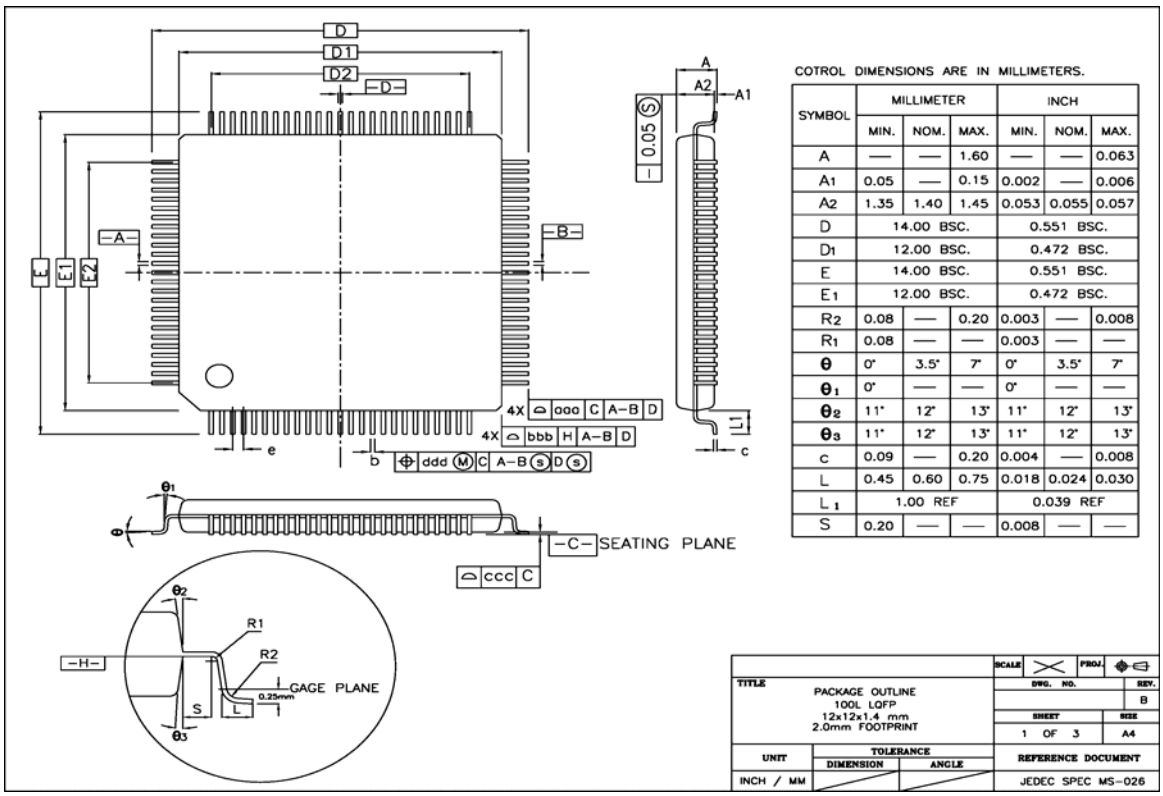
2 Program to 3.3, 2.5, or 1.8 V by setting the V_{IO} voltage level.

3 Program to 2 mA, 4 mA, 6 mA, 8 mA, 10 mA, 12 mA, 14, mA, or 16 mA via the I/O Configuration Register (0x034).

Package Layout

Figure 4 shows the package layout for the 100-pin LQFP package.

Figure 4 100-Pin LQFP



COTROL DIMENSIONS ARE IN MILLIMETERS.

SYMBOL	MILLIMETER			INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	—	—	1.60	—	—	0.063
A1	0.05	—	0.15	0.002	—	0.006
A2	1.35	1.40	1.45	0.053	0.055	0.057
D	14.00 BSC.			0.551 BSC.		
D1	12.00 BSC.			0.472 BSC.		
E	14.00 BSC.			0.551 BSC.		
E1	12.00 BSC.			0.472 BSC.		
R2	0.08	—	0.20	0.003	—	0.008
R1	0.08	—	—	0.003	—	—
θ	0°	3.5°	7°	0°	3.5°	7°
θ1	0°	—	—	0°	—	—
θ2	11°	12°	13°	11°	12°	13°
θ3	11°	12°	13°	11°	12°	13°
c	0.09	—	0.20	0.004	—	0.008
L	0.45	0.60	0.75	0.018	0.024	0.030
L1	1.00 REF			0.039 REF		
S	0.20	—	—	0.008	—	—

TITLE: PACKAGE OUTLINE 100L LQFP 12x12x1.4 mm 2.0mm FOOTPRINT	SCALE:	PROJ.	
	DWG. NO.		REV. B
	SHEET 1 OF 3		SIZE A4
UNIT: INCH / MM	TOLERANCE: DIMENSION / ANGLE		REFERENCE DOCUMENT: JEDEC SPEC MS-026

SYMBOL	100L					
	MILLIMETER			INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
b	0.13	0.16	0.23	0.005	0.006	0.009
e	0.40 BSC.			0.016 BSC.		
D2	9.60			0.378		
E2	9.60			0.378		
TOLERANCES OF FORM AND POSITION						
aaa	0.20			0.008		
bbb	0.20			0.008		
ccc	0.08			0.003		
ddd	0.07			0.003		

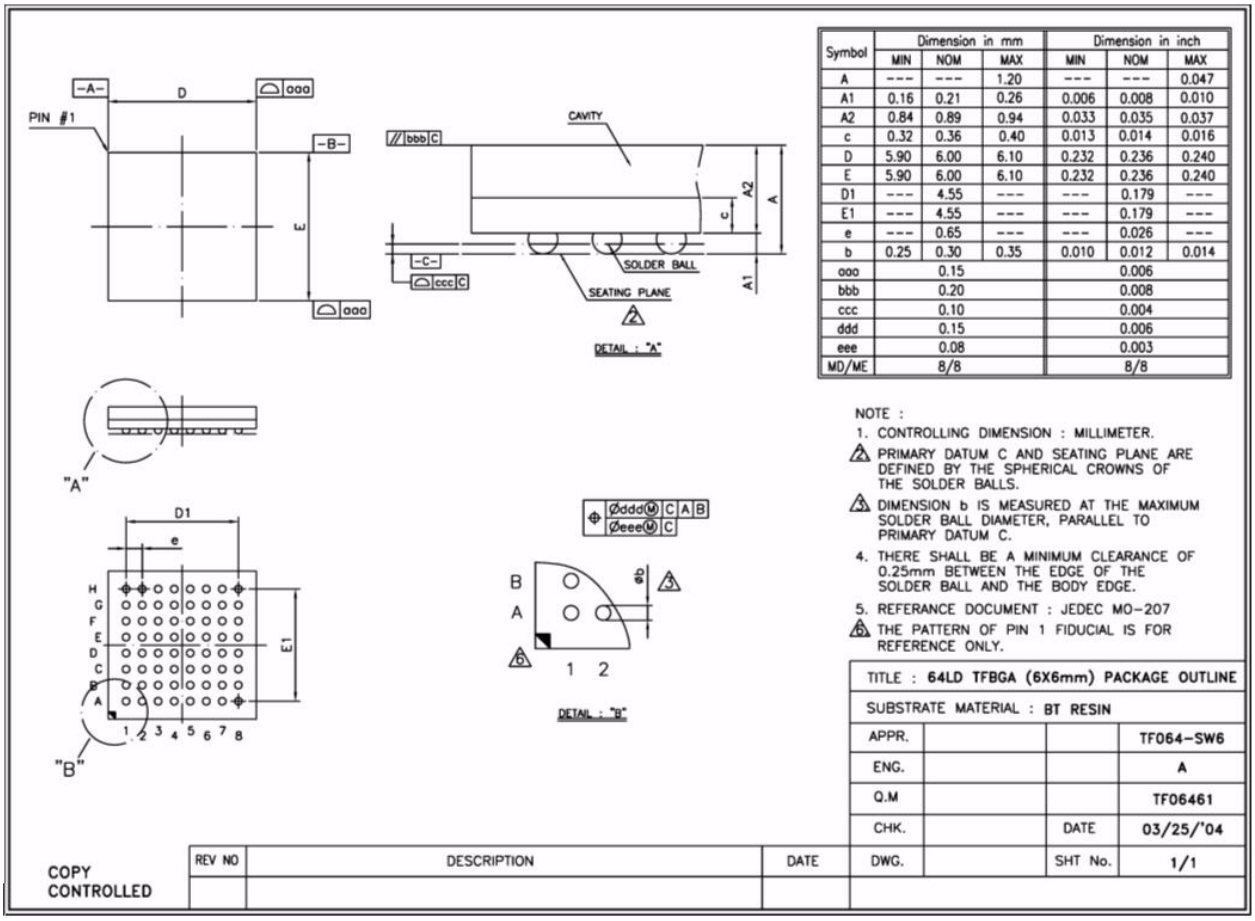
NOTES :

1. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25mm PER SIDE. D1 AND E1 ARE MAXIMUN PLASTIC BODY SIZE DIMENSIONS INCLUDING MOLD MISMATCH.
2. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED THE MAXIMUM b DIMENSION BY MORE THAN 0.08mm. DAMBAR CAN NOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSION AND AN ADJACENT LEAD IS 0.07mm FOR 0.4mm and 0.5mm PITCH PACKAGES.

TITLE: PACKAGE OUTLINE 100L LQFP 12x12x1.4 mm 2.0mm FOOTPRINT	SCALE:	PROJ.	
	DWG. NO.		REV. B
	SHEET 2 OF 3		SIZE A4
UNIT: INCH / MM	TOLERANCE: DIMENSION / ANGLE		REFERENCE DOCUMENT: JEDEC SPEC MS-026

Figure 5 shows the package layout for the 64-ball BGA.

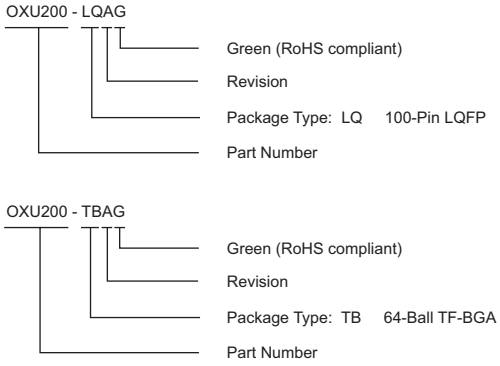
Figure 5 64-Ball TFBGA Package



Symbol	Dimension in mm			Dimension in inch		
	MIN	NOM	MAX	MIN	NOM	MAX
A	---	---	1.20	---	---	0.047
A1	0.16	0.21	0.26	0.006	0.008	0.010
A2	0.84	0.89	0.94	0.033	0.035	0.037
c	0.32	0.36	0.40	0.013	0.014	0.016
D	5.90	6.00	6.10	0.232	0.236	0.240
E	5.90	6.00	6.10	0.232	0.236	0.240
D1	---	4.55	---	---	0.179	---
E1	---	4.55	---	---	0.179	---
e	---	0.65	---	---	0.026	---
b	0.25	0.30	0.35	0.010	0.012	0.014
aaa		0.15			0.006	
bbb		0.20			0.008	
ccc		0.10			0.004	
ddd		0.15			0.006	
eee		0.08			0.003	
MD/ME		8/8			8/8	

Ordering Information

The following conventions are used to identify Oxford Semiconductor products.



Contacting Oxford Semiconductor

See the Oxford Semiconductor website (http://www.oxsemi.com) for further detail about Oxford Semiconductor devices, or email sales@oxsemi.com.

Revision Information

Table 10 documents the revisions of this guide.

Table 10 Revision Information

Revision	Modification
Dec 06	First publication
Jan 07	Added BGA chip layout, BGA pin allocations, and BGA package information
Feb 07	Miscellaneous editorial changes
Mar 07	Added the Certified USB logo to the title page

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