

# 74LVC74A-Q100

Dual D-type flip-flop with set and reset; positive-edge trigger

Rev. 2 — 5 April 2013

Product data sheet

## 1. General description

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The 74LVC74A-Q100 is a dual edge triggered D-type flip-flop. It has individual data ( $nD$ ) inputs, clock ( $nCP$ ) inputs, set ( $n\overline{SD}$ ) and ( $n\overline{RD}$ ) inputs, and complementary  $nQ$  and  $n\overline{Q}$  outputs.

The set and reset are asynchronous active LOW inputs and operate independently of the clock input. Information on the data input is transferred to the  $nQ$  output on the LOW-to-HIGH transition of the clock pulse. The  $nD$  inputs must be stable one set-up time prior to the LOW-to-HIGH clock transition, for predictable operation.

Schmitt trigger action at all inputs makes the circuit highly tolerant of slower input rise and fall times.

This product has been qualified to the Automotive Electronics Council (AEC) standard Q100 (Grade 1) and is suitable for use in automotive applications.

## 2. Features and benefits

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- Automotive product qualification in accordance with AEC-Q100 (Grade 1)
  - ◆ Specified from  $-40\text{ }^{\circ}\text{C}$  to  $+85\text{ }^{\circ}\text{C}$  and from  $-40\text{ }^{\circ}\text{C}$  to  $+125\text{ }^{\circ}\text{C}$
- 5 V tolerant inputs for interlacing with 5 V logic
- Wide supply voltage range from 1.2 V to 3.6 V
- CMOS low power consumption
- Direct interface with TTL levels
- ESD protection:
  - ◆ MIL-STD-883, method 3015 exceeds 2000 V
  - ◆ HBM JESD22-A114F exceeds 2000 V
  - ◆ MM JESD22-A115-A exceeds 200 V ( $C = 200\text{ pF}$ ,  $R = 0\ \Omega$ )
- Multiple package options

### 3. Ordering information

Table 1. Ordering information

Type number	Package			Version
	Temperature range	Name	Description	
74LVC74AD-Q100	-40 °C to +125 °C	SO14	plastic small outline package; 14 leads; body width 3.9 mm	SOT108-1
74LVC74APW-Q100	-40 °C to +125 °C	TSSOP14	plastic thin shrink small outline package; 14 leads; body width 4.4 mm	SOT402-1
74LVC74ABQ-Q100	-40 °C to +125 °C	DHVQFN14	plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 14 terminals; body 2.5 × 3 × 0.85 mm	SOT762-1

### 4. Functional diagram

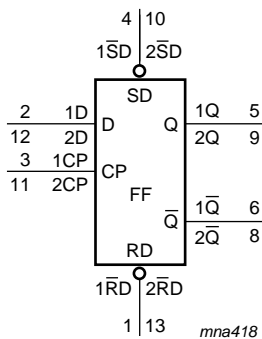


Fig 1. Logic symbol

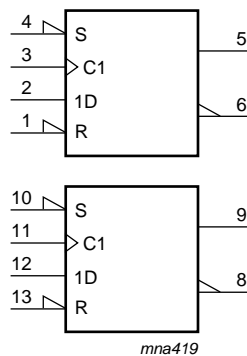


Fig 2. IEC logic symbol

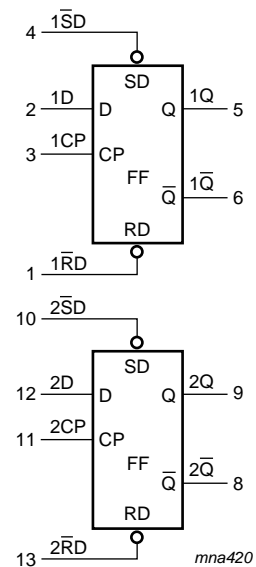


Fig 3. Functional diagram

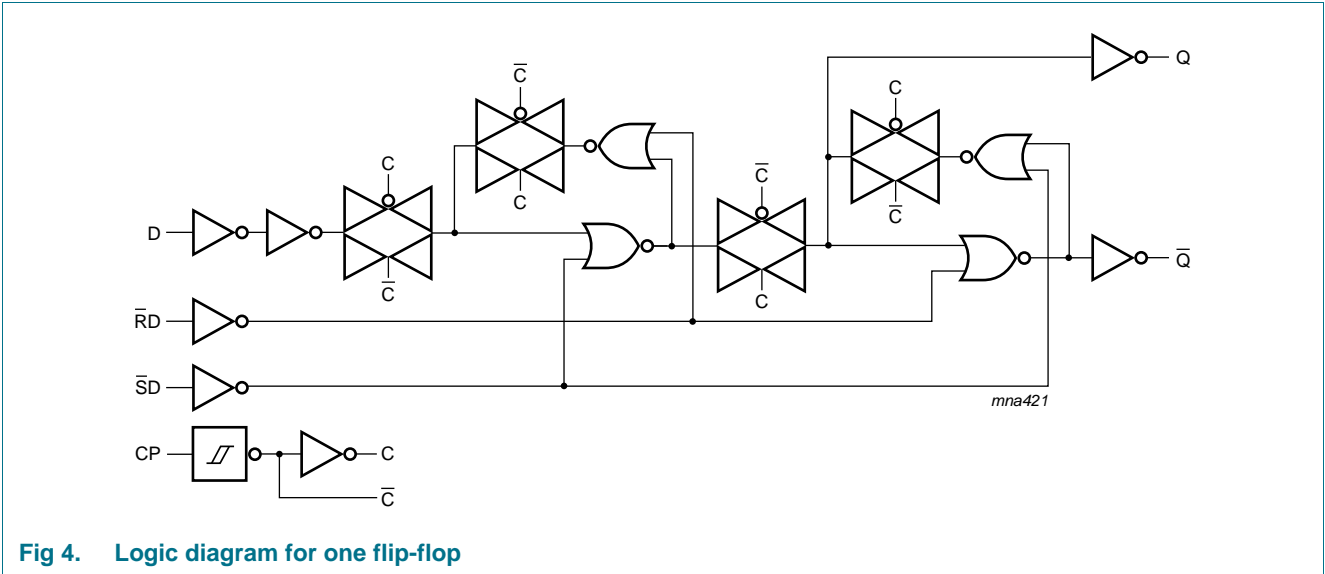


Fig 4. Logic diagram for one flip-flop

## 5. Pinning information

### 5.1 Pinning

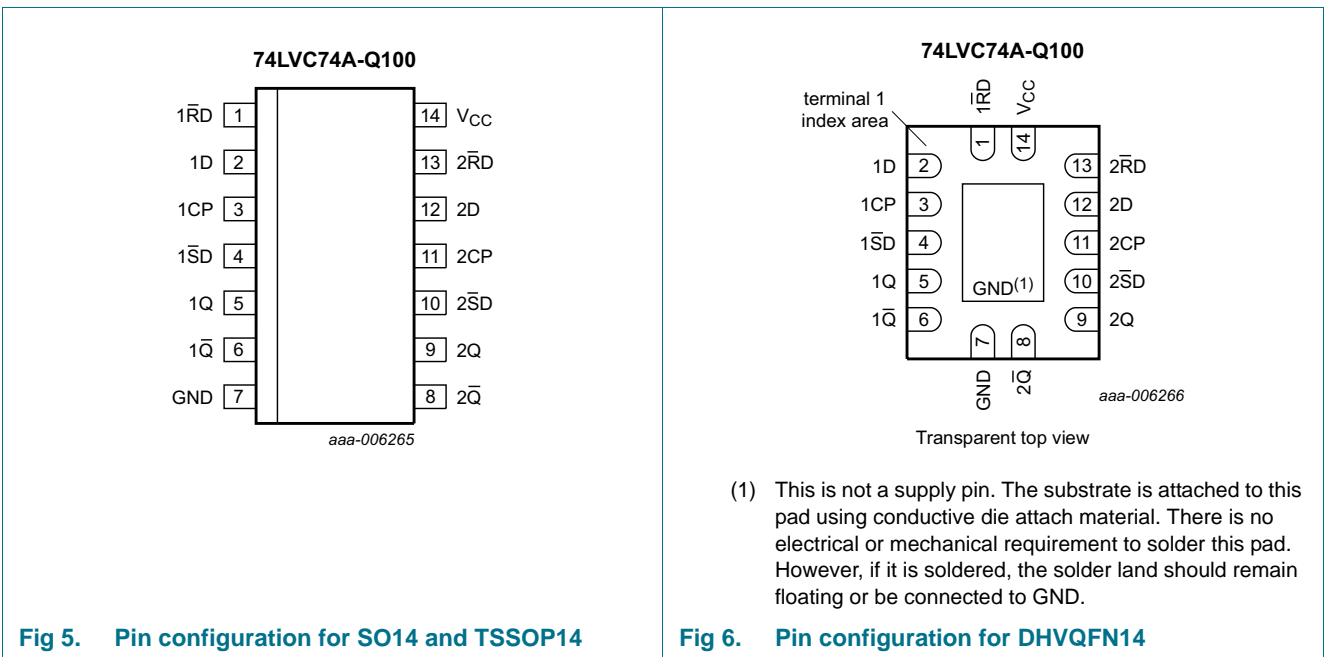


Fig 5. Pin configuration for SO14 and TSSOP14

Fig 6. Pin configuration for DHVQFN14

## 5.2 Pin description

Table 2. Pin description

Symbol	Pin	Description
$1\overline{RD}$ , $2\overline{RD}$	1, 13	asynchronous reset-direct input (active LOW)
1D, 2D	2, 12	data input
1CP, 2CP	3, 11	clock input (LOW-to-HIGH, edge-triggered)
$1\overline{SD}$ , $2\overline{SD}$	4, 10	asynchronous set-direct input (active LOW)
1Q, 2Q	5, 9	true output
$1\overline{Q}$ , $2\overline{Q}$	6, 8	complement output
GND	7	ground (0 V)
$V_{CC}$	14	supply voltage

## 6. Functional description

Table 3. Function table<sup>[1]</sup>

Input				Output	
$n\overline{SD}$	$n\overline{RD}$	nCP	nD	nQ	$n\overline{Q}$
L	H	X	X	H	L
H	L	X	X	L	H
L	L	X	X	H	H

[1] H = HIGH voltage level; L = LOW voltage level; X = don't care

Table 4. Function table<sup>[1]</sup>

Input				Output	
$n\overline{SD}$	$n\overline{RD}$	nCP	nD	$nQ_{n+1}$	$n\overline{Q}_{n+1}$
H	H	↑	L	L	H
H	H	↑	H	H	L

[1] H = HIGH voltage level; L = LOW voltage level; ↑ = LOW-to-HIGH transition;  $Q_{n+1}$  = state after the next LOW-to-HIGH CP transition; X = don't care

## 7. Limiting values

**Table 5. Limiting values**

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{CC}$	supply voltage		-0.5	+6.5	V
$I_{IK}$	input clamping current	$V_I < 0$ V	-50	-	mA
$V_I$	input voltage		[1] -0.5	+6.5	V
$I_{OK}$	output clamping current	$V_O > V_{CC}$ or $V_O < 0$ V	-	$\pm 50$	mA
$V_O$	output voltage		[2] -0.5	$V_{CC} + 0.5$	V
$I_O$	output current	$V_O = 0$ V to $V_{CC}$	-	$\pm 50$	mA
$I_{CC}$	supply current		-	100	mA
$I_{GND}$	ground current		-100	-	mA
$T_{stg}$	storage temperature		-65	+150	°C
$P_{tot}$	total power dissipation	$T_{amb} = -40$ °C to +125 °C	[3] -	500	mW

[1] The minimum input voltage ratings may be exceeded if the input current ratings are observed.

[2] The output voltage ratings may be exceeded if the output current ratings are observed.

[3] For SO14 packages: above 70 °C the value of  $P_{tot}$  derates linearly with 8 mW/K.  
 For TSSOP14 packages: above 60 °C the value of  $P_{tot}$  derates linearly with 5.5 mW/K.  
 For DHVQFN14 packages: above 60 °C the value of  $P_{tot}$  derates linearly with 4.5 mW/K.

## 8. Recommended operating conditions

**Table 6. Recommended operating conditions**

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{CC}$	supply voltage	for maximum speed performance	1.65	-	3.6	V
		for low-voltage applications	1.2	-	3.6	V
$V_I$	input voltage		0	-	5.5	V
$V_O$	output voltage		0	-	$V_{CC}$	V
$T_{amb}$	ambient temperature		-40	-	+125	°C
$\Delta t/\Delta V$	input transition rise and fall rate	$V_{CC} = 1.65$ V to 2.7 V	0	-	20	ns/V
		$V_{CC} = 2.7$ V to 3.6 V	0	-	10	ns/V

## 9. Static characteristics

**Table 7. Static characteristics**

At recommended operating conditions. Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	-40 °C to +85 °C			-40 °C to +125 °C		Unit
			Min	Typ <sup>[1]</sup>	Max	Min	Max	
V <sub>IH</sub>	HIGH-level input voltage	V <sub>CC</sub> = 1.2 V	1.08	-	-	1.08	-	V
		V <sub>CC</sub> = 1.65 V to 1.95 V	0.65 × V <sub>CC</sub>	-	-	0.65 × V <sub>CC</sub>	-	V
		V <sub>CC</sub> = 2.3 V to 2.7 V	1.7	-	-	1.7	-	V
		V <sub>CC</sub> = 2.7 V to 3.6 V	2.0	-	-	2.0	-	V
V <sub>IL</sub>	LOW-level input voltage	V <sub>CC</sub> = 1.2 V	-	-	0.12	-	0.12	V
		V <sub>CC</sub> = 1.65 V to 1.95 V	-	-	0.35 × V <sub>CC</sub>	-	0.35 × V <sub>CC</sub>	V
		V <sub>CC</sub> = 2.3 V to 2.7 V	-	-	0.7	-	0.7	V
		V <sub>CC</sub> = 2.7 V to 3.6 V	-	-	0.8	-	0.8	V
V <sub>OH</sub>	HIGH-level output voltage	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>						
		I <sub>O</sub> = -100 μA; V <sub>CC</sub> = 1.65 V to 3.6 V	V <sub>CC</sub> - 0.2	-	-	V <sub>CC</sub> - 0.3	-	V
		I <sub>O</sub> = -4 mA; V <sub>CC</sub> = 1.65 V	1.2	-	-	1.05	-	V
		I <sub>O</sub> = -8 mA; V <sub>CC</sub> = 2.3 V	1.8	-	-	1.65	-	V
		I <sub>O</sub> = -12 mA; V <sub>CC</sub> = 2.7 V	2.2	-	-	2.05	-	V
		I <sub>O</sub> = -18 mA; V <sub>CC</sub> = 3.0 V	2.4	-	-	2.25	-	V
		I <sub>O</sub> = -24 mA; V <sub>CC</sub> = 3.0 V	2.2	-	-	2.0	-	V
V <sub>OL</sub>	LOW-level output voltage	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>						
		I <sub>O</sub> = 100 μA; V <sub>CC</sub> = 1.65 V to 3.6 V	-	-	0.2	-	0.3	V
		I <sub>O</sub> = 4 mA; V <sub>CC</sub> = 1.65 V	-	-	0.45	-	0.65	V
		I <sub>O</sub> = 8 mA; V <sub>CC</sub> = 2.3 V	-	-	0.6	-	0.8	V
		I <sub>O</sub> = 12 mA; V <sub>CC</sub> = 2.7 V	-	-	0.4	-	0.6	V
		I <sub>O</sub> = 24 mA; V <sub>CC</sub> = 3.0 V	-	-	0.55	-	0.8	V
I <sub>I</sub>	input leakage current	V <sub>CC</sub> = 3.6 V; V <sub>I</sub> = 5.5 V or GND	-	±0.1	±5	-	±20	μA
I <sub>CC</sub>	supply current	V <sub>CC</sub> = 3.6 V; V <sub>I</sub> = V <sub>CC</sub> or GND; I <sub>O</sub> = 0 A	-	0.1	10	-	40	μA
ΔI <sub>CC</sub>	additional supply current	per input pin; V <sub>CC</sub> = 2.7 V to 3.6 V; V <sub>I</sub> = V <sub>CC</sub> - 0.6 V; I <sub>O</sub> = 0 A	-	5	500	-	5000	μA
C <sub>I</sub>	input capacitance	V <sub>CC</sub> = 0 V to 3.6 V; V <sub>I</sub> = GND to V <sub>CC</sub>	-	4.0	-	-	-	pF

[1] All typical values are measured at V<sub>CC</sub> = 3.3 V (unless stated otherwise) and T<sub>amb</sub> = 25 °C.

## 10. Dynamic characteristics

**Table 8. Dynamic characteristics**

Voltages are referenced to GND (ground = 0 V). For test circuit see [Figure 9](#).

Symbol	Parameter	Conditions	-40 °C to +85 °C			-40 °C to +125 °C		Unit
			Min	Typ <sup>[1]</sup>	Max	Min	Max	
t <sub>pd</sub>	propagation delay	nCP to nQ, nQ̄; see <a href="#">Figure 7</a> <sup>[2]</sup>						
		V <sub>CC</sub> = 1.2 V	-	15	-	-	-	ns
		V <sub>CC</sub> = 1.65 V to 1.95 V	1.0	5.0	10.3	1.0	11.9	ns
		V <sub>CC</sub> = 2.3 V to 2.7 V	1.8	2.9	5.8	1.8	6.7	ns
		V <sub>CC</sub> = 2.7 V	1.0	2.7	6.0	1.0	7.5	ns
		V <sub>CC</sub> = 3.0 V to 3.6 V	1.0	2.6	5.2	1.0	6.5	ns
		nSD to nQ, nQ̄; see <a href="#">Figure 8</a>						
		V <sub>CC</sub> = 1.2 V	-	15	-	-	-	ns
		V <sub>CC</sub> = 1.65 V to 1.95 V	0.5	4.0	10.6	0.5	12.2	ns
		V <sub>CC</sub> = 2.3 V to 2.7 V	1.0	2.4	6.1	1.0	7.1	ns
		V <sub>CC</sub> = 2.7 V	1.0	2.9	6.4	1.0	8.0	ns
		V <sub>CC</sub> = 3.0 V to 3.6 V	1.0	2.2	5.4	1.0	7.0	ns
		nRD to nQ, nQ̄; see <a href="#">Figure 8</a>						
		V <sub>CC</sub> = 1.2 V	-	15	-	-	-	ns
		V <sub>CC</sub> = 1.65 V to 1.95 V	0.5	4.1	10.7	0.5	12.4	ns
		V <sub>CC</sub> = 2.3 V to 2.7 V	1.0	2.4	6.1	1.0	7.1	ns
		V <sub>CC</sub> = 2.7 V	1.0	3.0	6.4	1.0	8.0	ns
		V <sub>CC</sub> = 3.0 V to 3.6 V	1.0	2.2	5.4	1.0	7.0	ns
t <sub>w</sub>	pulse width	clock HIGH or LOW; see <a href="#">Figure 7</a>						
		V <sub>CC</sub> = 1.65 V to 1.95 V	5.0	-	-	5.0	-	ns
		V <sub>CC</sub> = 2.3 V to 2.7 V	4.0	-	-	4.0	-	ns
		V <sub>CC</sub> = 2.7 V	3.3	-	-	4.5	-	ns
		V <sub>CC</sub> = 3.0 V to 3.6 V	3.3	1.3	-	4.5	-	ns
		set or reset LOW; see <a href="#">Figure 8</a>						
		V <sub>CC</sub> = 1.65 V to 1.95 V	5.0	-	-	5.0	-	ns
		V <sub>CC</sub> = 2.3 V to 2.7 V	4.0	-	-	4.0	-	ns
		V <sub>CC</sub> = 2.7 V	3.3	-	-	4.5	-	ns
		V <sub>CC</sub> = 3.0 V to 3.6 V	3.3	1.7	-	4.5	-	ns
t <sub>rec</sub>	recovery time	set or reset; see <a href="#">Figure 8</a>						
		V <sub>CC</sub> = 1.65 V to 1.95 V	1.5	-	-	1.5	-	ns
		V <sub>CC</sub> = 2.3 V to 2.7 V	1.5	-	-	1.5	-	ns
		V <sub>CC</sub> = 2.7 V	1.5	-	-	1.0	-	ns
		V <sub>CC</sub> = 3.0 V to 3.6 V	+1.0	-3.0	-	1.0	-	ns

**Table 8. Dynamic characteristics ...continued**Voltages are referenced to GND (ground = 0 V). For test circuit see [Figure 9](#).

Symbol	Parameter	Conditions	-40 °C to +85 °C			-40 °C to +125 °C		Unit		
			Min	Typ <sup>[1]</sup>	Max	Min	Max			
t <sub>su</sub>	set-up time	nD to nCP; see <a href="#">Figure 7</a>								
		V <sub>CC</sub> = 1.65 V to 1.95 V	3.0	-	-	3.0	-	ns		
		V <sub>CC</sub> = 2.3 V to 2.7 V	2.5	-	-	2.5	-	ns		
		V <sub>CC</sub> = 2.7 V	2.2	-	-	2.2	-	ns		
t <sub>h</sub>	hold time	nD to nCP; see <a href="#">Figure 7</a>								
		V <sub>CC</sub> = 1.65 V to 1.95 V	2.0	-	-	2.0	-	ns		
		V <sub>CC</sub> = 2.3 V to 2.7 V	1.5	-	-	1.5	-	ns		
		V <sub>CC</sub> = 2.7 V	1.0	-	-	1.0	-	ns		
f <sub>max</sub>	maximum frequency	nCP; see <a href="#">Figure 7</a>								
		V <sub>CC</sub> = 1.65 V to 1.95 V	100	-	-	80	-	MHz		
		V <sub>CC</sub> = 2.3 V to 2.7 V	125	-	-	100	-	MHz		
		V <sub>CC</sub> = 2.7 V	150	-	-	120	-	MHz		
t <sub>sk(o)</sub>	output skew time	V <sub>CC</sub> = 3.0 V to 3.6 V	[3]	-	-	1.0	-	1.5	ns	
		C <sub>PD</sub>	power dissipation capacitance	per flip-flop; V <sub>I</sub> = GND to V <sub>CC</sub>	[4]					
		V <sub>CC</sub> = 1.65 V to 1.95 V	-	12.4	-	-	-	pF		
		V <sub>CC</sub> = 2.3 V to 2.7 V	-	16.0	-	-	-	pF		
C <sub>PD</sub>	power dissipation capacitance	V <sub>CC</sub> = 3.0 V to 3.6 V	-	19.1	-	-	-	pF		

[1] Typical values are measured at T<sub>amb</sub> = 25 °C and V<sub>CC</sub> = 1.2 V, 1.8 V, 2.5 V, 2.7 V and 3.3 V respectively.

[2] t<sub>pd</sub> is the same as t<sub>PLH</sub> and t<sub>PHL</sub>.

[3] Skew between any two outputs of the same package switching in the same direction. This parameter is guaranteed by design.

[4] C<sub>PD</sub> is used to determine the dynamic power dissipation (P<sub>D</sub> in μW).

$$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma(C_L \times V_{CC}^2 \times f_o) \text{ where:}$$

f<sub>i</sub> = input frequency in MHz; f<sub>o</sub> = output frequency in MHz

C<sub>L</sub> = output load capacitance in pF

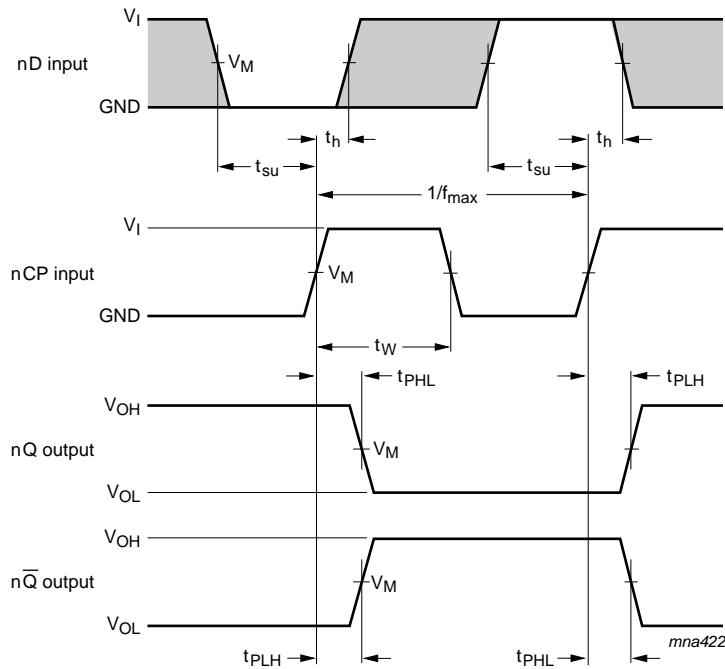
V<sub>CC</sub> = supply voltage in Volts

N = number of inputs switching

Σ(C<sub>L</sub> × V<sub>CC</sub><sup>2</sup> × f<sub>o</sub>) = sum of the outputs



11. AC waveforms

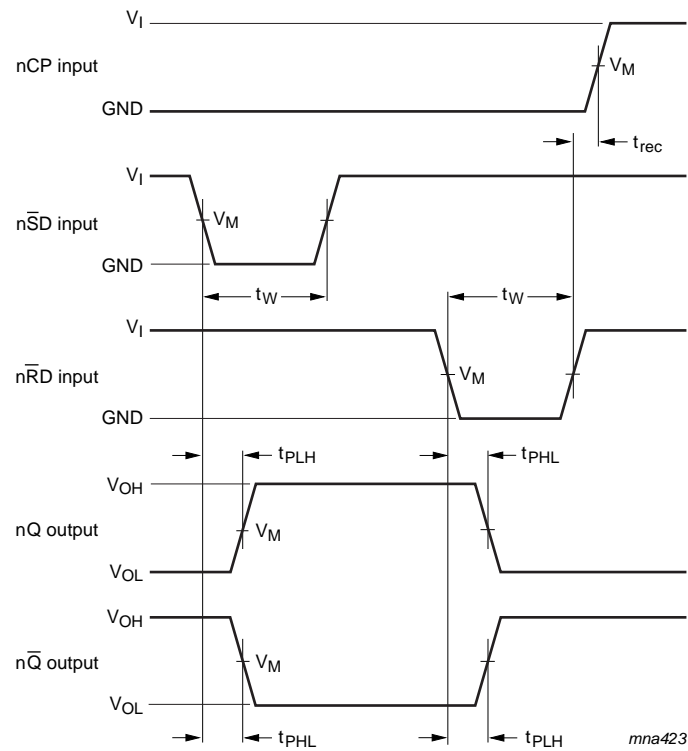


The shaded areas indicate when the input is permitted to change for predictable output performance.

Measurement points are given in [Table 9](#).

$V_{OL}$  and  $V_{OH}$  are typical output voltage levels that occur with the output load.

**Fig 7. Clock propagation delays, pulse widths, set-up, hold times and maximum frequency**



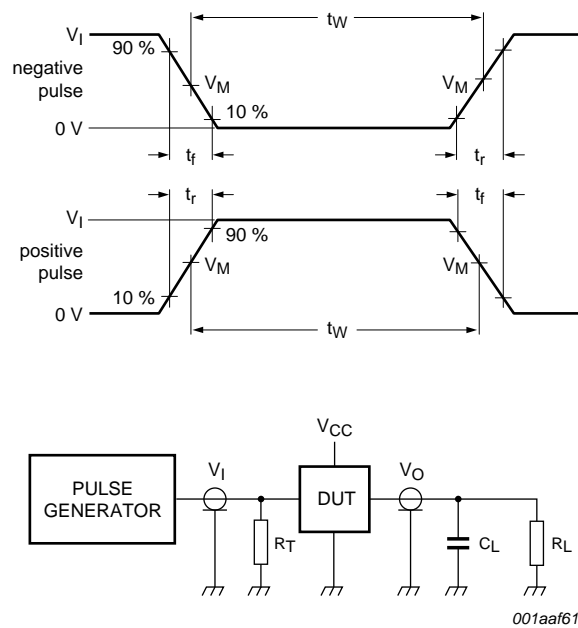
Measurement points are given in [Table 9](#).

$V_{OL}$  and  $V_{OH}$  are typical output voltage levels that occur with the output load.

**Fig 8. Set and reset propagation delays, pulse widths and recovery time**

**Table 9. Measurement points**

Supply voltage	Input		Output
$V_{CC}$	$V_I$	$V_M$	$V_M$
1.2 V	$V_{CC}$	$0.5 \times V_{CC}$	$0.5 \times V_{CC}$
1.65 V to 1.95 V	$V_{CC}$	$0.5 \times V_{CC}$	$0.5 \times V_{CC}$
2.3 V to 2.7 V	$V_{CC}$	$0.5 \times V_{CC}$	$0.5 \times V_{CC}$
2.7 V	2.7 V	1.5 V	1.5 V
3.0 V to 3.6 V	2.7 V	1.5 V	1.5 V



001aa615

Test data is given in [Table 10](#).

Definitions for test circuit:

$R_L$  = Load resistance.

$C_L$  = Load capacitance including jig and probe capacitance.

$R_T$  = Termination resistance should be equal to output impedance  $Z_o$  of the pulse generator.

**Fig 9. Load circuitry for switching times**

**Table 10. Test data**

Supply voltage	Input		Load		$V_{EXT}$		
$V_{CC}$	$V_I$	$t_r, t_f$	$C_L$	$R_L$	$t_{PLH}, t_{PHL}$	$t_{PLZ}, t_{PZL}$	$t_{PHZ}, t_{PZH}$
1.2 V	$V_{CC}$	$\leq 2$ ns	30 pF	1 k $\Omega$	open	$2 \times V_{CC}$	GND
1.65 V to 1.95 V	$V_{CC}$	$\leq 2$ ns	30 pF	1 k $\Omega$	open	$2 \times V_{CC}$	GND
2.3 V to 2.7 V	$V_{CC}$	$\leq 2$ ns	30 pF	500 $\Omega$	open	$2 \times V_{CC}$	GND
2.7 V	2.7 V	$\leq 2.5$ ns	50 pF	500 $\Omega$	open	$2 \times V_{CC}$	GND
3.0 V to 3.6 V	2.7 V	$\leq 2.5$ ns	50 pF	500 $\Omega$	open	$2 \times V_{CC}$	GND

12. Package outline

SO14: plastic small outline package; 14 leads; body width 3.9 mm

SOT108-1

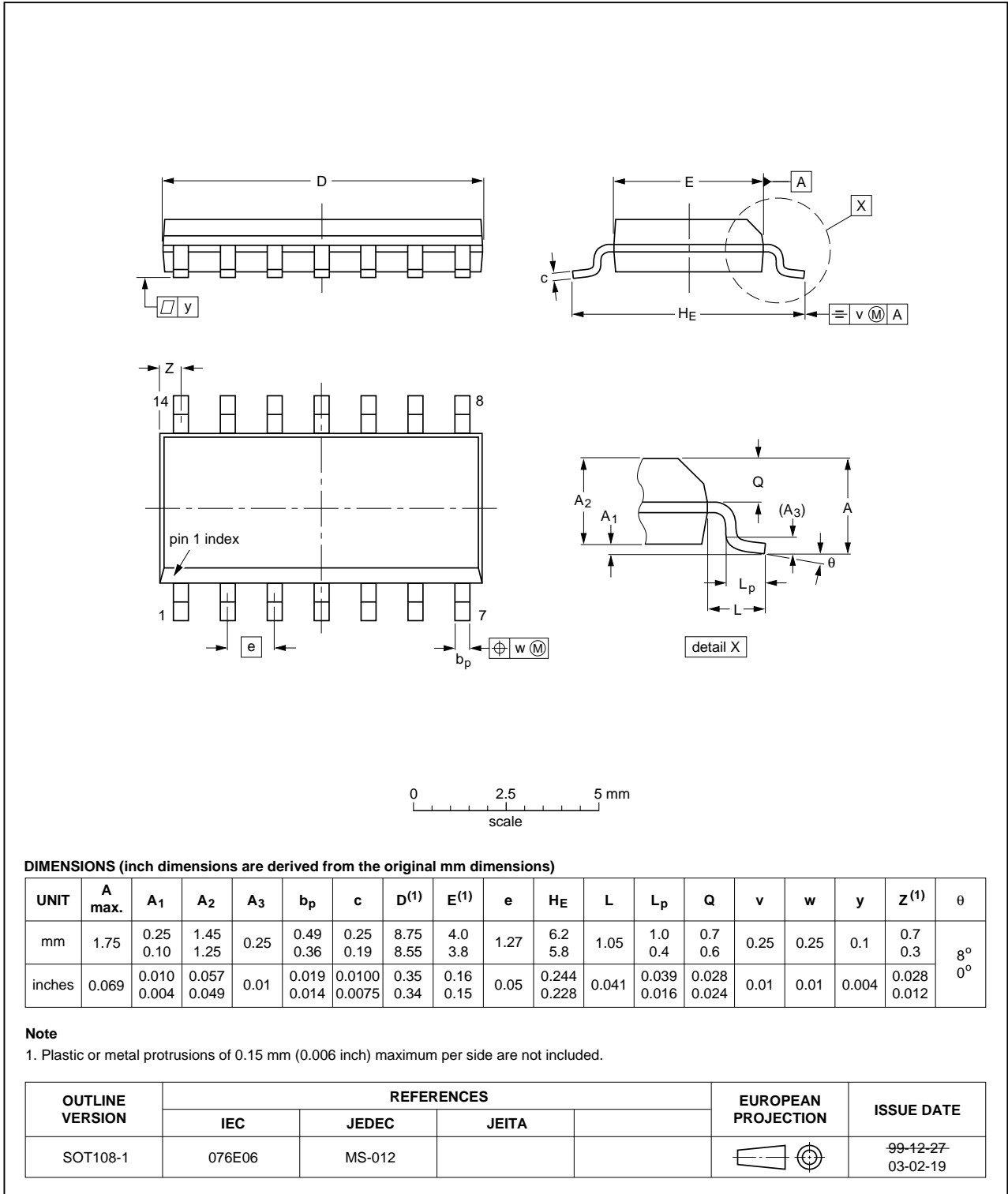


Fig 10. Package outline SOT108-1 (SO14)

TSSOP14: plastic thin shrink small outline package; 14 leads; body width 4.4 mm

SOT402-1

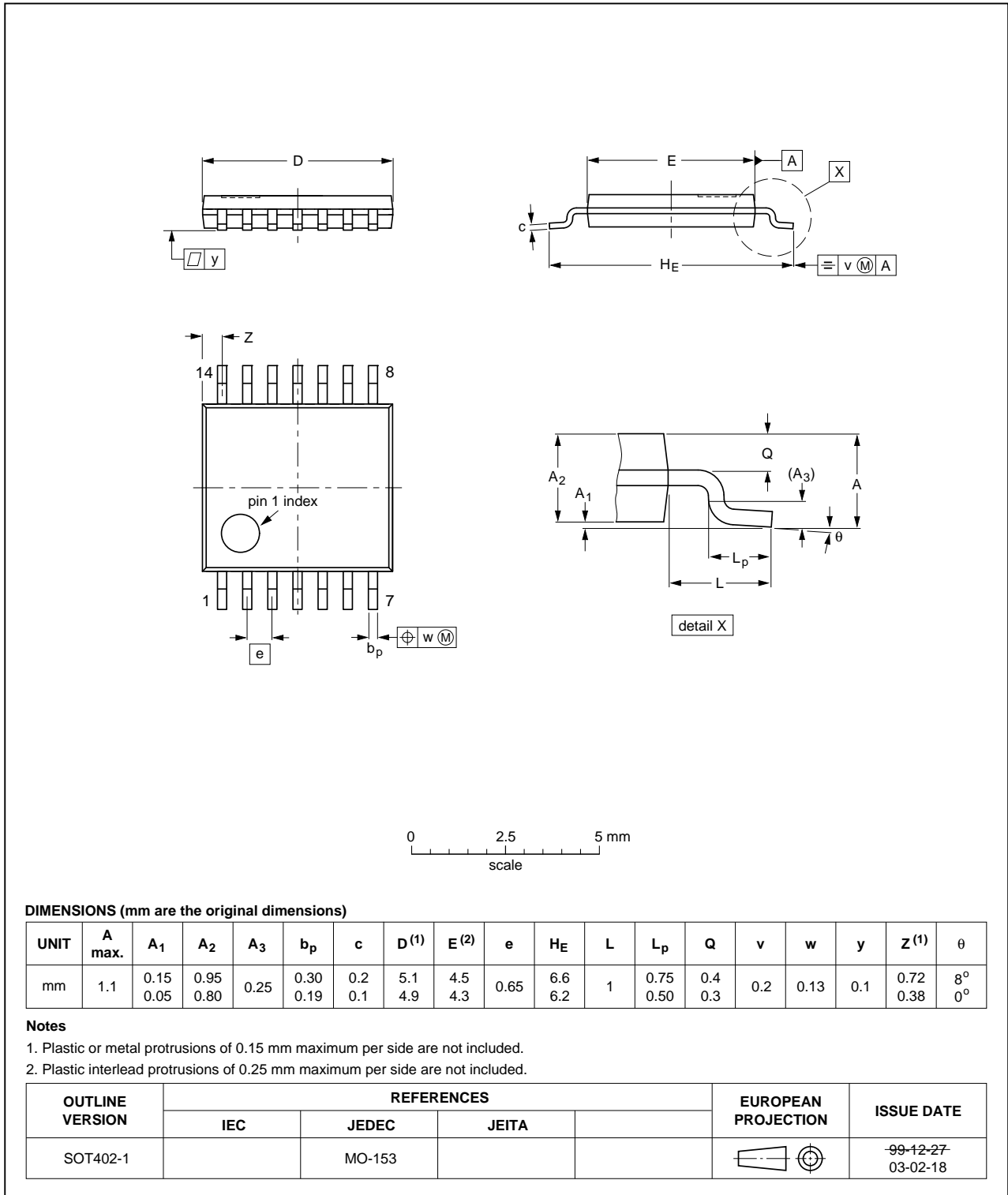


Fig 11. Package outline SOT402-1 (TSSOP14)

DHVQFN14: plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 14 terminals; body 2.5 x 3 x 0.85 mm

SOT762-1

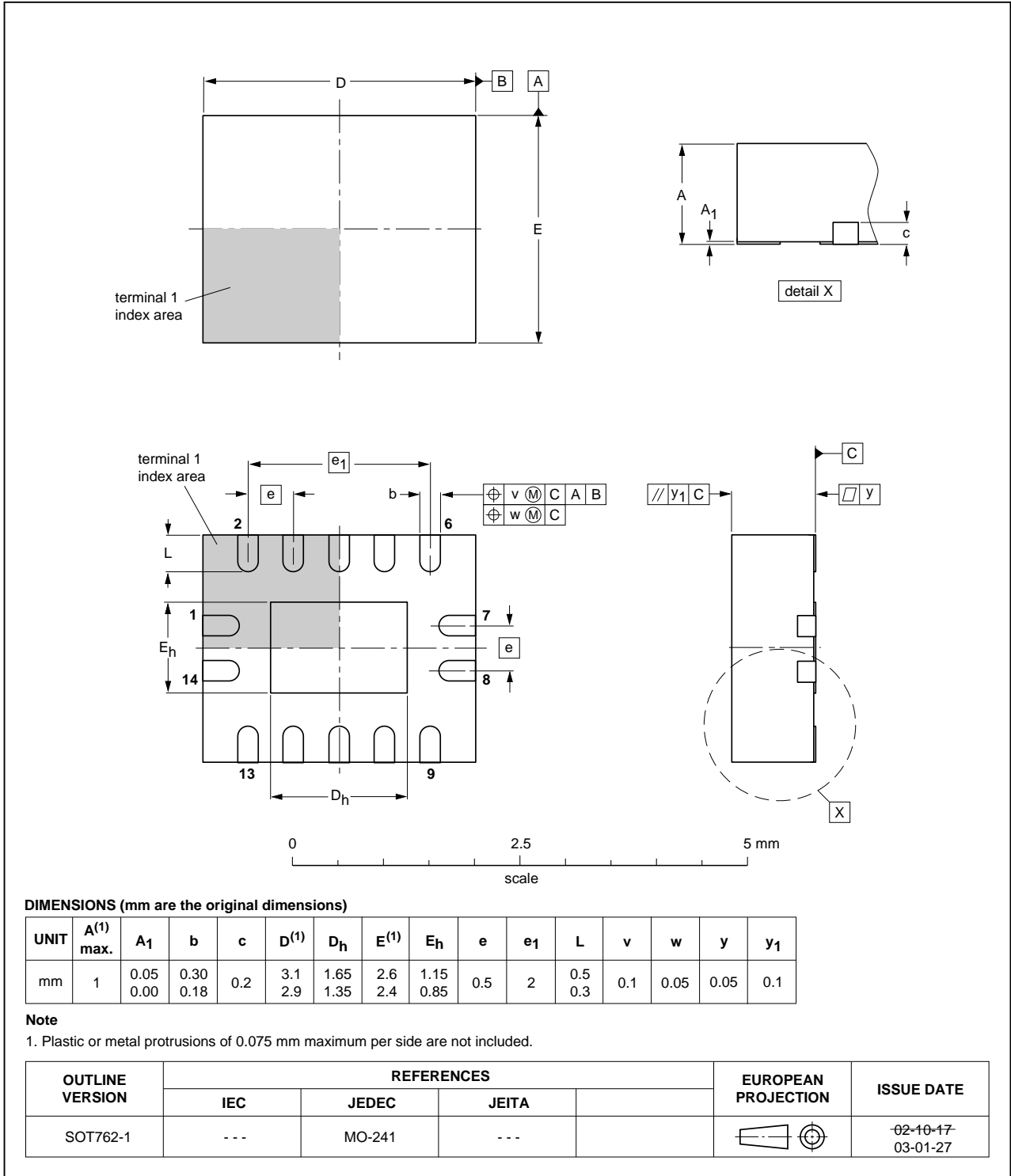


Fig 12. Package outline SOT762-1 (DHVQFN14)

## 13. Abbreviations

Table 11. Abbreviations

Acronym	Description
CDM	Charged Device Model
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model
MM	Machine Model
MIL	Military
TTL	Transistor-Transistor Logic

## 14. Revision history

Table 12. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74LVC74A_Q100 v.2	20130405	Product data sheet	-	74LVC74A_Q100 v.1
Modifications:	• <a href="#">Section 2 “Features and benefits”</a> removed redundant temperature range			
74LVC74A_Q100 v.1	20130326	Product data sheet	-	-

## 15. Legal information

### 15.1 Data sheet status

Document status <sup>[1][2]</sup>	Product status <sup>[3]</sup>	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL <http://www.nexperia.com>.

### 15.2 Definitions

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For more information, please visit: <http://www.nexperia.com>

For sales office addresses, please send an email to: [salesaddresses@nexperia.com](mailto:salesaddresses@nexperia.com)

## 17. Contents

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<b>1</b>	<b>General description</b> .....	<b>1</b>
<b>2</b>	<b>Features and benefits</b> .....	<b>1</b>
<b>3</b>	<b>Ordering information</b> .....	<b>2</b>
<b>4</b>	<b>Functional diagram</b> .....	<b>2</b>
<b>5</b>	<b>Pinning information</b> .....	<b>3</b>
5.1	Pinning .....	3
5.2	Pin description .....	4
<b>6</b>	<b>Functional description</b> .....	<b>4</b>
<b>7</b>	<b>Limiting values</b> .....	<b>5</b>
<b>8</b>	<b>Recommended operating conditions</b> .....	<b>5</b>
<b>9</b>	<b>Static characteristics</b> .....	<b>6</b>
<b>10</b>	<b>Dynamic characteristics</b> .....	<b>7</b>
<b>11</b>	<b>AC waveforms</b> .....	<b>9</b>
<b>12</b>	<b>Package outline</b> .....	<b>12</b>
<b>13</b>	<b>Abbreviations</b> .....	<b>15</b>
<b>14</b>	<b>Revision history</b> .....	<b>15</b>
<b>15</b>	<b>Legal information</b> .....	<b>16</b>
15.1	Data sheet status .....	16
15.2	Definitions .....	16
15.3	Disclaimers .....	16
15.4	Trademarks .....	17
<b>16</b>	<b>Contact information</b> .....	<b>17</b>
<b>17</b>	<b>Contents</b> .....	<b>18</b>

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