

8-BIT SINGLE-CHIP MICROCONTROLLER

DESCRIPTION

The μ PD78F9026A is a μ PD789026 Subseries product (compact general-purpose devices) of the 78K/0S Series.

The μ PD78F9026A has flash memory in place of the internal ROM of the μ PD789022, 789024, 789025, and 789026.

Since the data can be written to or erased from the flash memory of the μ PD78F9026A with the microcontroller mounted on a printed circuit board, it is ideal for applications involving the evaluation of the systems in the development stage, small-scale production of many different products, and rapid development and time-to-market of a new product.

Detailed function descriptions are provided in the following user's manuals. Be sure to read them before designing.

μ PD789026 Subseries User's Manual: U11919E
78K/0S Series User's Manual — Instruction: U11047E

FEATURES

- Pin compatible with mask ROM version (except V_{PP} pin)
- Flash memory: 16 Kbytes
- Internal high-speed RAM: 512 bytes
- Minimum instruction execution time can be changed from high-speed (0.4 μ s) to low-speed (1.6 μ s) (@ 5.0-MHz operation with system clock)
- I/O ports: 34
- Serial interface: 1 channel
3-wire serial I/O mode/UART mode can be selected
- Timer: 3 channels
 - 16-bit timer: 1 channel
 - 8-bit timer/event counter: 1 channel
 - Watchdog timer: 1 channel
- Power supply voltage: V_{DD} = 1.8 to 5.5 V

APPLICATIONS

Compact household appliances, car accessories, air conditioners, games, etc.

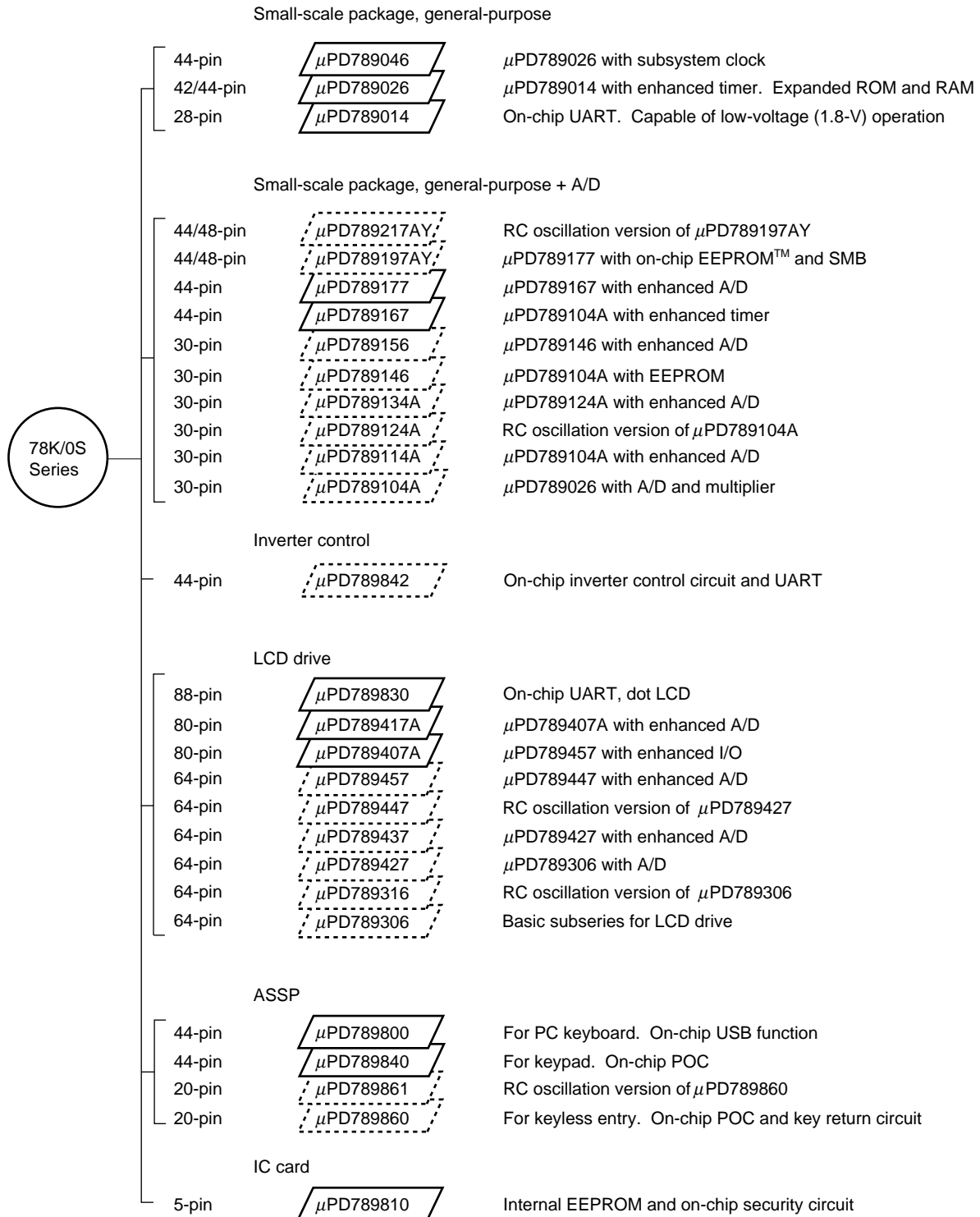
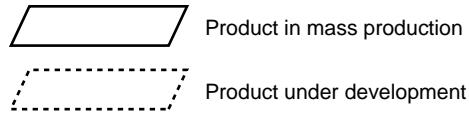
ORDERING INFORMATION

Part Number	Package
μ PD78F9026ACU	42-pin plastic shrink DIP (600 mils)
μ PD78F9026AGB-3BS-MTX	44-pin plastic QFP (10 × 10 mm, resin thickness: 2.7 mm)
μ PD78F9026AGB-8ES	44-pin plastic LQFP (10 × 10 mm, resin thickness: 1.4 mm)

The information in this document is subject to change without notice. Before using this document, please confirm that this is the latest version.
Not all devices/types available in every country. Please check with local NEC representative for availability and additional information.

78K/0S SERIES LINEUP

The products in the 78K/0S Series are listed below. The names enclosed in boxes are subseries names.



The major functional differences among the subseries are listed below.

Function Subseries Name		ROM Capacity	Timer				8-Bit A/D	10-Bit A/D	Serial Interface	I/O	V _{DD} MIN Value	Remark	
			8-bit	16-bit	Watch	WDT							
Small-scale package, general- purpose	μPD789046	16 K	1 ch	1 ch	1 ch	1 ch	—	—	1 ch (UART: 1 ch)	34	1.8 V	—	
	μPD789026	4 K to 16 K			—								
	μPD789014	2 K to 4 K	2 ch	—						22			
Small-scale package, general- purpose + A/D	μPD789217AY	16 K to 24 K	3 ch	1 ch	1 ch	1 ch	—	8 ch	2 ch (UART: 1 ch) SMB: 1 ch	31	1.8 V	RC oscillation version, internal EEPROM	
	μPD789197AY											Internal EEPROM	
	μPD789177											—	
	μPD789167					8 ch	—	1 ch (UART: 1 ch)					
	μPD789156	8 K to 16 K	1 ch	—	—	4 ch	—	4 ch	20			Internal EEPROM	
	μPD789146											4 ch	—
	μPD789134A	2 K to 8 K						4 ch				RC oscillation version	
	μPD789124A											4 ch	—
	μPD789114A											—	4 ch
μPD789104A	4 ch											—	
Inverter control	μPD789842	8 K to 16 K	3 ch	Note	1 ch	1 ch	8 ch	—	1 ch (UART: 1 ch)	30	4.0 V	—	
LCD drive	μPD789830	24 K	1 ch	1 ch	1 ch	1 ch	—	—	1 ch (UART: 1 ch)	30	2.7 V	—	
	μPD789417A	12 K to 24 K	3 ch					7 ch		43	1.8 V		
	μPD789407A				7 ch	—	25						
	μPD789457	16 K to 24 K	2 ch					4 ch	2 ch (UART: 1 ch)			RC oscillation version	
	μPD789447											4 ch	—
	μPD789437											—	4 ch
	μPD789427											4 ch	—
	μPD789316	8 K to 16 K								23		RC oscillation version	
μPD789306	—											—	
ASSP	μPD789800	8 K	2 ch	1 ch	—	1 ch	—	—	2 ch (USB: 1 ch)	31	4.0 V	—	
	μPD789840							4 ch		1 ch	29		2.8 V
	μPD789861	4 K		—					—	14	1.8 V	RC oscillation version	
	μPD789860											—	—
IC card	μPD789810	6 K	—	—	—	1 ch	—	—	—	1	2.7 V	Internal EEPROM	

Note 10-bit timer: 1 channel

OVERVIEW OF FUNCTIONS

Item		Function
Internal memory	Flash memory	16 Kbytes
	High-speed RAM	512 bytes
Minimum instruction execution time		0.4 μs/1.6 μs (@ 5.0-MHz operation with system clock)
General-purpose registers		8 bits × 8 registers
Instruction set		<ul style="list-style-type: none"> • 16-bit operation • Bit manipulation (set, reset, test), etc.
I/O ports		Total: 34 <ul style="list-style-type: none"> • CMOS input/output: 34
Serial interface		<ul style="list-style-type: none"> • 3-wire serial I/O mode/UART mode selectable: 1 channel
Timer		<ul style="list-style-type: none"> • 16-bit timer: 1 channel • 8-bit timer/event counter: 1 channel • Watchdog timer: 1 channel
Timer outputs		2
Vectored interrupt sources	Maskable	Internal: 5, External: 4
	Non-maskable	Internal: 1
Power supply voltage		V _{DD} = 1.8 to 5.5 V
Operating ambient temperature		T _A = -40 to +85°C
Packages		<ul style="list-style-type: none"> • 42-pin plastic shrink DIP (600 mils) • 44-pin plastic QFP (10 × 10 mm, resin thickness 2.7 mm) • 44-pin plastic LQFP (10 × 10 mm, resin thickness 1.4 mm)

CONTENTS

1. PIN CONFIGURATION (TOP VIEW)..... 6

2. BLOCK DIAGRAM 8

3. PIN FUNCTIONS 9

 3.1 Port Pins 9

 3.2 Non-Port Pins 10

 3.3 Pin I/O Circuits and Recommended Connection of Unused Pins..... 11

4. MEMORY SPACE 13

5. PROGRAMMING FLASH MEMORY 14

 5.1 Selecting Communication Mode..... 14

 5.2 Function of Flash Memory Programming 15

 5.3 Connecting Flashpro III 15

 5.4 Example of Settings for Flashpro III (PG-FP3)..... 17

6. INSTRUCTION SET OVERVIEW 18

 6.1 Conventions 18

 6.2 Operations 20

7. ELECTRICAL SPECIFICATIONS 25

8. PACKAGE DRAWINGS 35

9. RECOMMENDED SOLDERING CONDITIONS 38

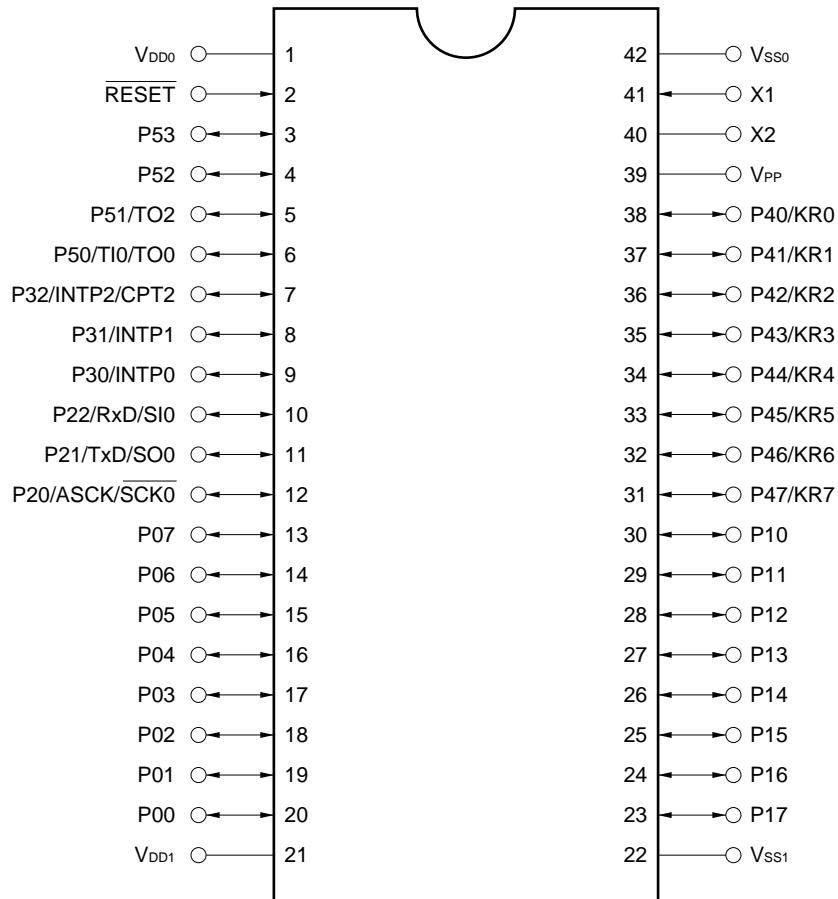
APPENDIX A DIFFERENCES BETWEEN μPD78F9026A AND MASK ROM VERSIONS 39

APPENDIX B DEVELOPMENT TOOLS 40

APPENDIX C RELATED DOCUMENTS..... 42

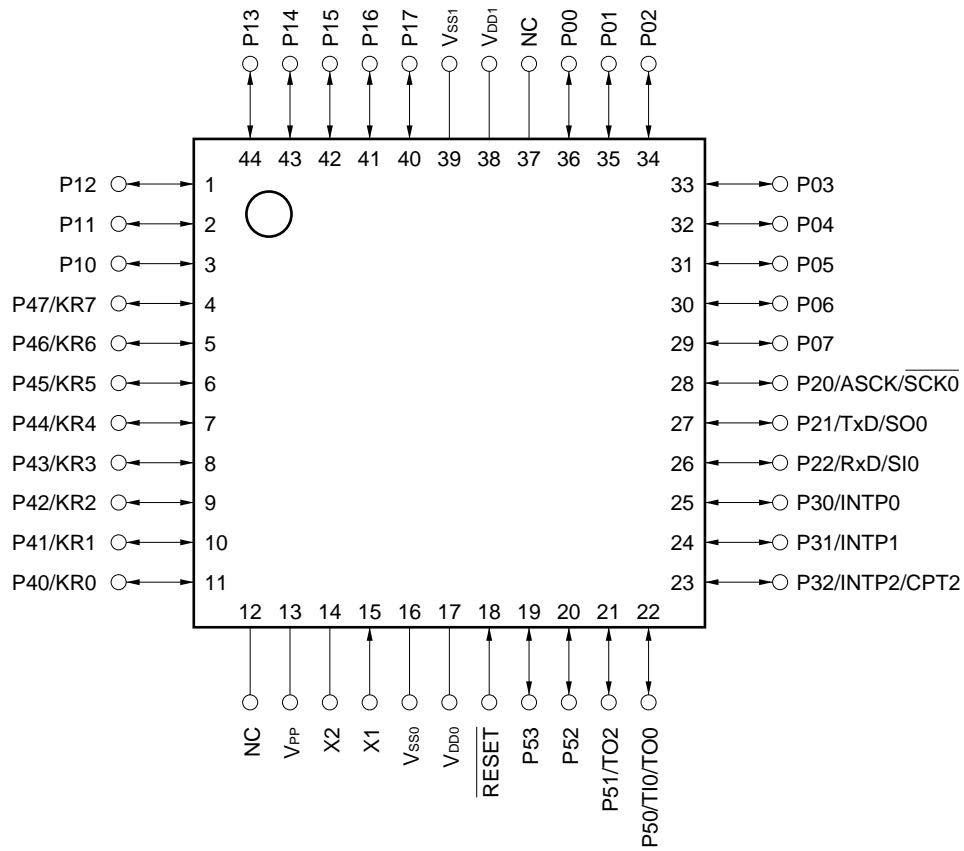
1. PIN CONFIGURATION (TOP VIEW)

- 42-pin plastic shrink DIP (600 mils)
μPD78F9026ACU



Caution Connect the V_{PP} pin directly to V_{SS} in normal operation mode.

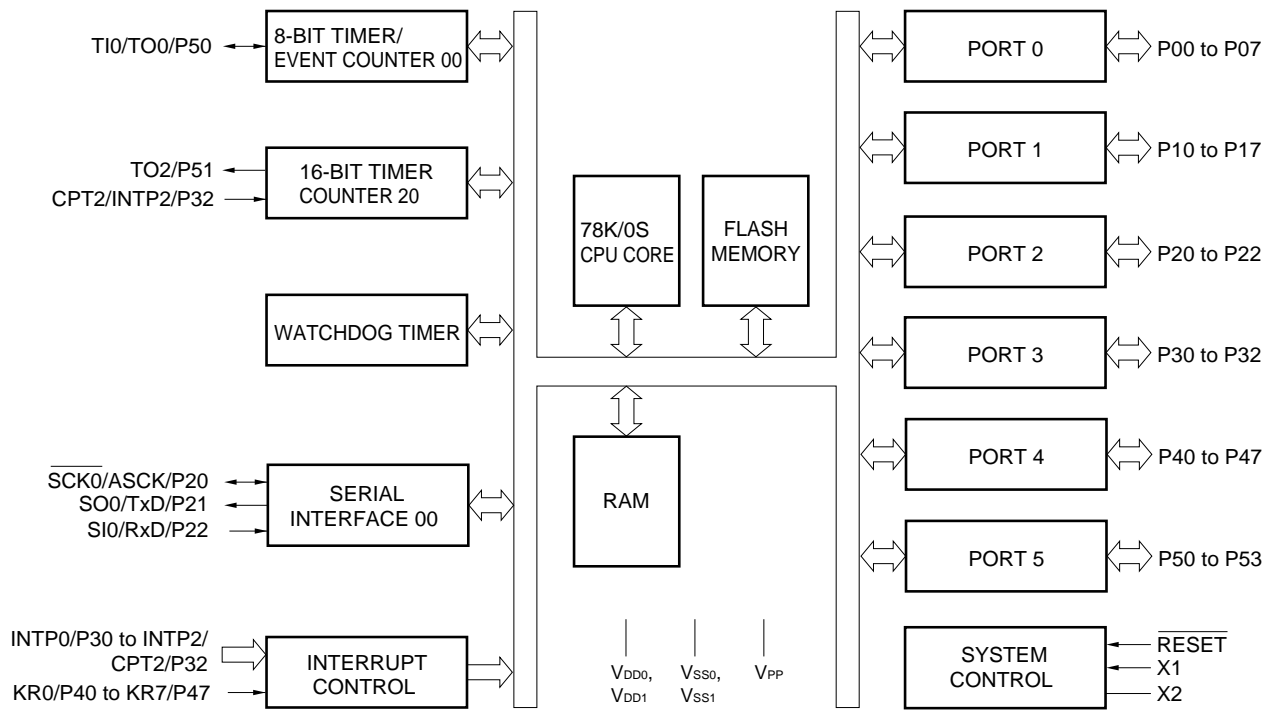
- 44-pin plastic QFP (10 × 10 mm, resin thickness 2.7 mm)
μPD78F9026AGB-3BS-MTX
- 44-pin plastic LQFP (10 × 10 mm, resin thickness 1.4 mm)
μPD78F9026AGB-8ES



Caution Connect the V_{PP} pin directly to V_{SS0} or V_{SS1} in normal operation mode.

ASCK:	Asynchronous Serial Clock	RxD:	Receive Data
CPT2:	Capture Trigger Input	SCK0 :	Serial Clock
INTP0 to INTP2:	Interrupt from Peripherals	SI0:	Serial Input
KR0 to KR7:	Key Return	SO0:	Serial Output
NC:	Non-connection	TI0:	Timer Input
P00 to P07:	Port 0	TO0, TO2:	Timer Output
P10 to P17:	Port 1	TxD:	Transmit Data
P20 to P22:	Port 2	V _{DD0} , V _{DD1} :	Power Supply
P30 to P32:	Port 3	V _{PP} :	Programming Power Supply
P40 to P47:	Port 4	V _{SS0} , V _{SS1} :	Ground
P50 to P53:	Port 5	X1, X2:	Crystal
RESET :	Reset		

2. BLOCK DIAGRAM



3. PIN FUNCTIONS

3.1 Port Pins

Pin Name	I/O	Function	After Reset	Alternate Function
P00 to P07	I/O	Port 0 8-bit input/output port Input/output can be specified in 1-bit units. When used as an input port, an on-chip pull-up resistor can be specified by means of software. LEDs can be driven directly.	Input	—
P10 to P17	I/O	Port 1 8-bit input/output port Input/output can be specified in 1-bit units. When used as an input port, an on-chip pull-up resistor can be specified by means of software. LEDs can be driven directly.	Input	—
P20	I/O	Port 2 3-bit input/output port Input/output can be specified in 1-bit units. When used as an input port, an on-chip pull-up resistor can be specified by means of software. LEDs can be driven directly.	Input	ASCK/ $\overline{\text{SCK0}}$
P21				TxD/SO0
P22				RxD/SI0
P30	I/O	Port 3 3-bit input/output port Input/output can be specified in 1-bit units. When used as an input port, an on-chip pull-up resistor can be specified by means of software. LEDs can be driven directly.	Input	INTP0
P31				INTP1
P32				INTP2/CPT2
P40 to P47	I/O	Port 4 8-bit input/output port Input/output can be specified in 1-bit units. When used as an input port, an on-chip pull-up resistor can be specified by means of software. LEDs can be driven directly.	Input	KR0 to KR7
P50	I/O	Port 5 4-bit input/output port Input/output can be specified in 1-bit units. When used as an input port, an on-chip pull-up resistor can be specified by means of software. LEDs can be driven directly.	Input	TI0/TO0
P51				TO2
P52, P53				—

3.2 Non-Port Pins

Pin Name	I/O	Function	After Reset	Alternate Function
INTP0	Input	External interrupt input for which the valid edge (rising edge, falling edge, or both rising and falling edges) can be specified	Input	P30
INTP1				P31
INTP2				P32/CPT2
SI0	Input	Serial interface serial data input	Input	P22/RxD
SO0	Output	Serial interface serial data output	Input	P21/TxD
SCK0	I/O	Serial interface serial clock input/output	Input	P20/ASCK
RxD	Input	Asynchronous serial interface serial data input	Input	P22/SI0
TxD	Output	Asynchronous serial interface serial data output	Input	P21/SO0
ASCK	Input	Asynchronous serial interface serial clock input	Input	P20/SCK0
TI0	Input	External count clock input to 8-bit timer (TM00)	Input	P50/TO0
TO0	Output	8-bit timer (TM00) output	Input	P50/TI0
TO2	Output	16-bit timer (TM20) output	Input	P51
CPT2	Input	Capture edge input pin	Input	P32/INTP2
KR0 to KR7	Input	Key return signal detection pin	Input	P40 to P47
RESET	Input	System reset input	Input	—
X1	Input	Connecting crystal resonator for system clock oscillation	—	—
X2	—		—	—
V _{DD0}	—	Positive power supply of ports	—	—
V _{DD1}	—	Positive power supply (except ports)	—	—
V _{PP}	—	Flash memory programming mode setting. High-voltage application for program write/verify. Connect directly to V _{SS0} or V _{SS1} in normal operation mode.	—	—
NC	—	Not internally connected. Leave open.	—	—
V _{SS0}	—	Ground potential of ports	—	—
V _{SS1}	—	Ground potential (except ports)	—	—

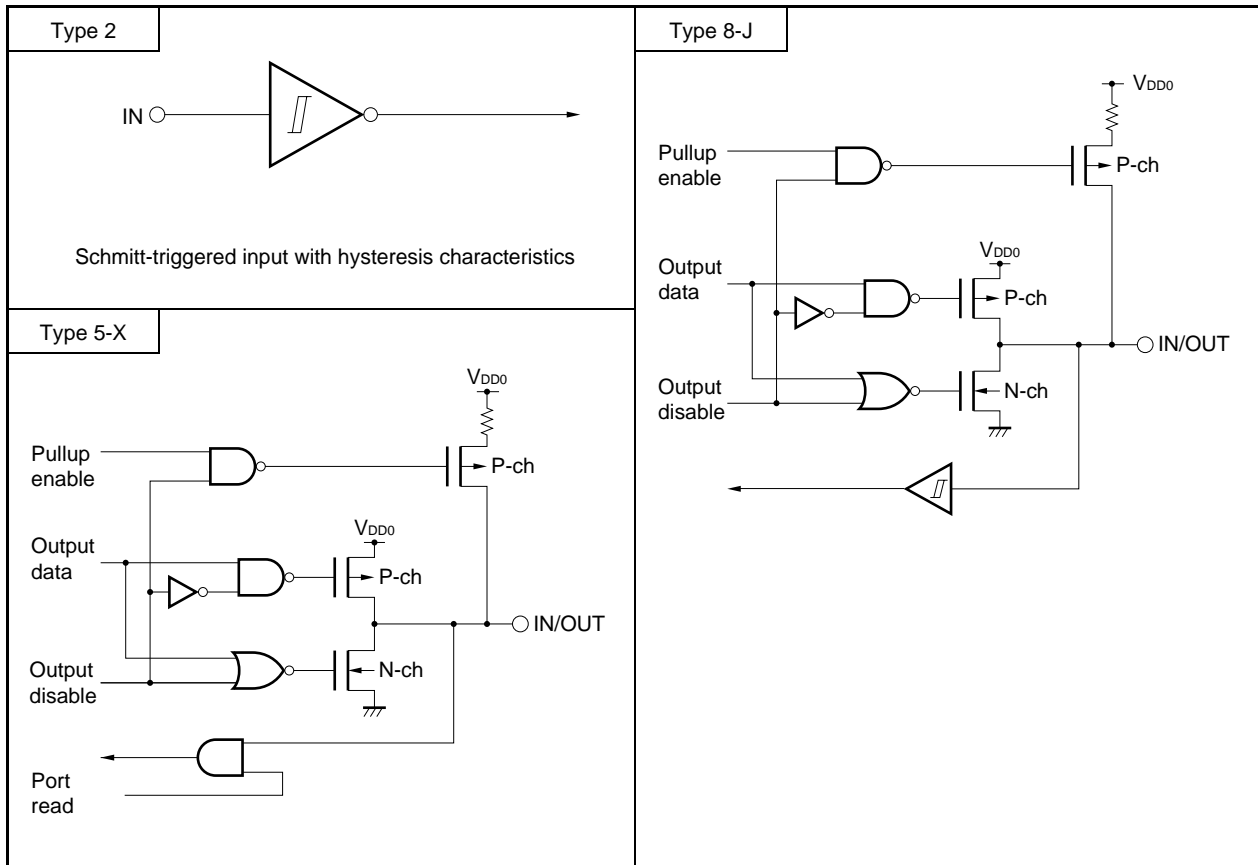
3.3 Pin I/O Circuits and Recommended Connection of Unused Pins

The input/output circuit type of each pin and recommended connection of unused pins are shown in Table 3-1. For the input/output circuit configuration of each type, refer to Figure 3-1.

Table 3-1. Types of Input/Output Circuits and Recommended Connection of Unused Pins

Pin Name	I/O Circuit Type	I/O	Recommended Connection of Unused Pins
P00 to P07	5-X	I/O	Input: Independently connect to V _{DD0} or V _{DD1} , or V _{SS0} or V _{SS1} via a resistor. Output: Leave open.
P10 to P17			
P20/ASCK/ $\overline{\text{SCK0}}$	8-J		
P21/TxD/SO0	5-X		
P22/RxD/SI0	8-J		
P30/INTP0			
P31/INTP1			
P32/INTP2/CPT2			
P40/KR0 to P47/KR7			
P50/TI0/TO0			
P51/TO2			
P52, P53			
$\overline{\text{RESET}}$	2		
NC	—	—	Leave open.
V _{PP}			Connect directly to V _{SS0} or V _{SS1} .

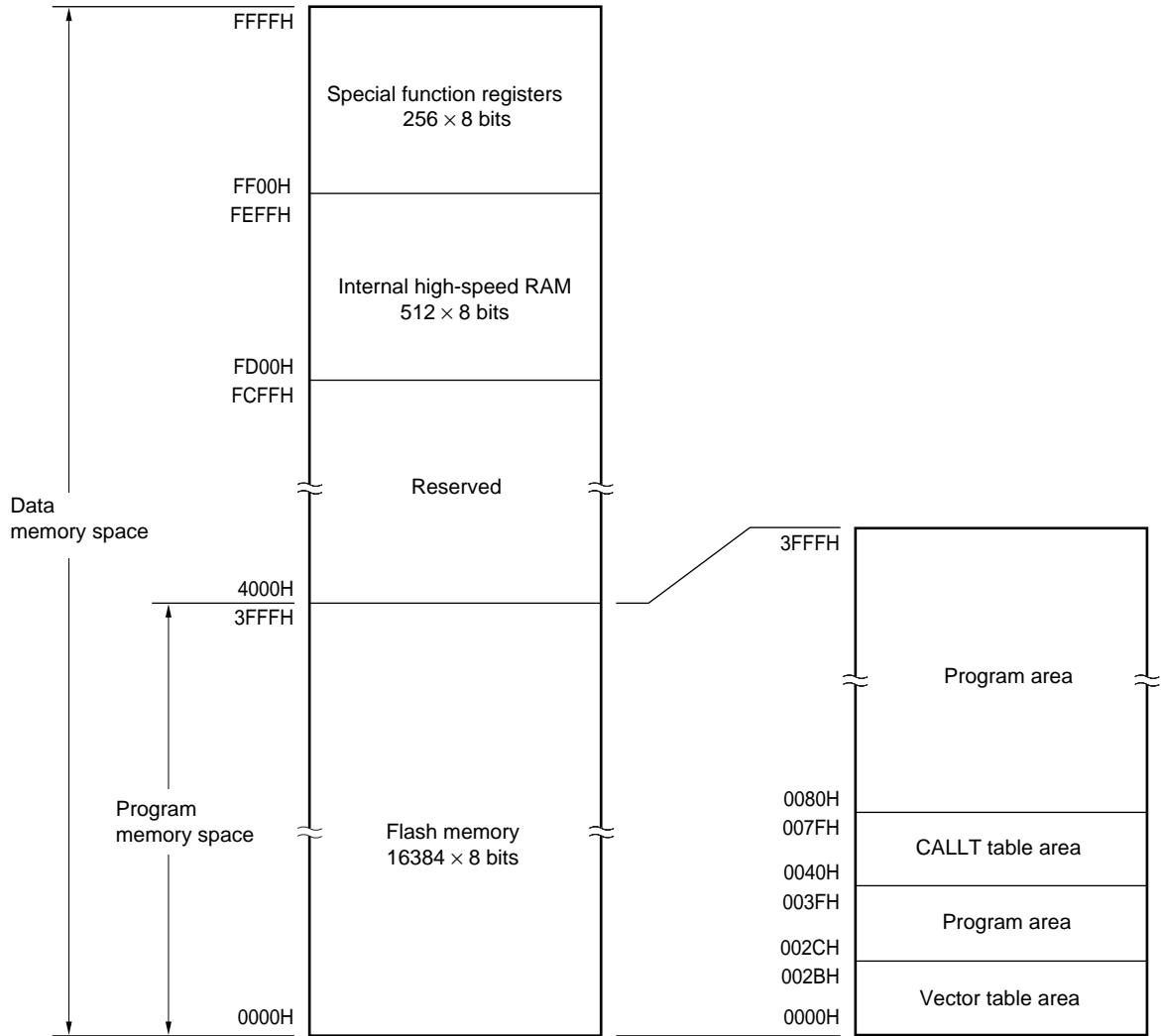
Figure 3-1. Pin Input/Output Circuits



4. MEMORY SPACE

The μPD78F9026A can access up to 64 Kbytes of memory space. Figure 4-1 shows the memory map.

Figure 4-1. Memory Map



5. PROGRAMMING FLASH MEMORY

The program memory that is incorporated in the μPD78F9026A is flash memory.

With flash memory, it is possible to write programs on-board. Writing is performed by connecting a dedicated flash programmer (Flashpro III, (Part No. FL-PR3, PG-FP3)) to the host machine and the target system.

Remark FL-PR3 is a product of Naito Densai Machida Mfg. Co., Ltd.

5.1 Selecting Communication Mode

Writing to flash memory is performed using the Flashpro III in a serial communication mode. Select one of the communication modes in Table 5-1. The selection of the communication mode is made by using the format shown in Figure 5-1. Each communication mode is selected using the number of V_{PP} pulses shown in Table 5-1.

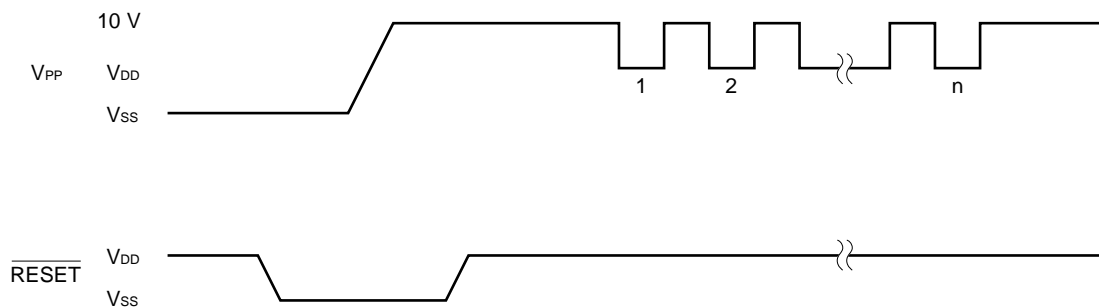
Table 5-1. List of Communication Mode

Communication Mode	Pins	V _{PP} Pulses
3-wire serial I/O	SCK0/ASCK/P20 SO0/TxD/P21 SI0/RxD/P22	0
UART	TxD/SO0/P21 RxD/SI0/P22	8
Pseudo 3-wire serial I/O ^{Note}	P00 (Serial clock input) P01 (Serial data output) P02 (Serial data input)	12
	P40/KR0 (Serial clock input) P41/KR1 (Serial data output) P42/KR2 (Serial data input)	13

Note Serial transfer is carried out by controlling ports with software.

Caution Be sure to select a communication mode using the number of V_{PP} pulses shown in Table 5-1.

Figure 5-1. Format of Communication Mode Selection



5.2 Function of Flash Memory Programming

Operations such as writing to flash memory are performed by various command/data transmission and reception operations according to the selected communication mode. Table 5-2 shows the major functions of flash memory programming.

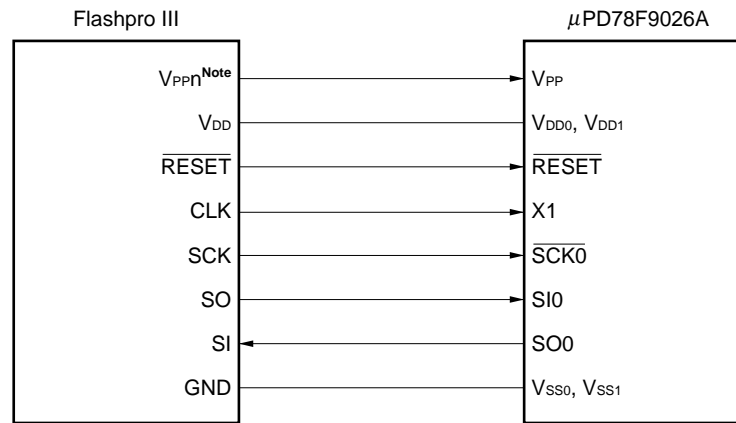
Table 5-2. Major Function of Flash Memory Programming

Function	Description
Batch delete	Deletes the entire memory contents
Batch blank check	Checks the deletion status of the entire memory
Data write	Performs a write operation to the flash memory based on the write start address and the number of data to be written (number of bytes).
Batch verify	Compares the entire memory contents with the input data.

5.3 Connecting Flashpro III

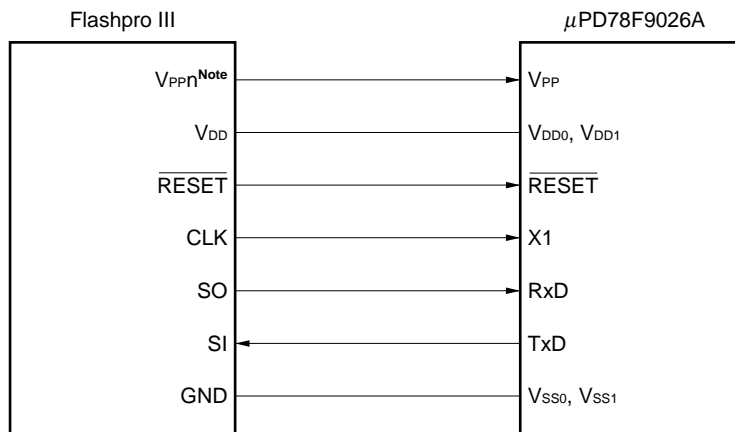
The connection of the Flashpro III and the μPD78F9026A differs according to the communication mode (3-wire serial I/O, UART, and pseudo 3-wire serial I/O). The connections for each communication mode are shown in Figures 5-2, 5-3, and 5-4, respectively.

Figure 5-2. Connection of Flashpro III when Using 3-Wire Serial I/O Mode



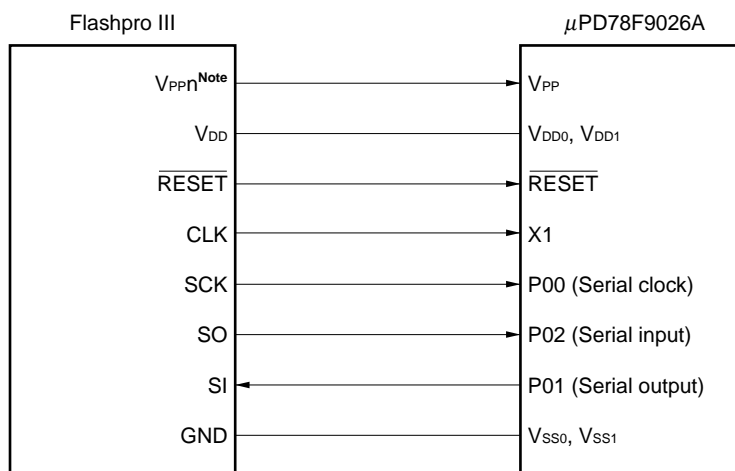
Note n = 0, 1

Figure 5-3. Connection of Flashpro III when Using UART Mode



Note n = 0, 1

Figure 5-4. Connection of Flashpro III When Using Pseudo 3-Wire Serial I/O Mode



Note n = 0, 1

5.4 Example of Settings for Flashpro III (PG-FP3)

When writing to flash memory using Flashpro III (PG-FP3), make the following settings.

1. Load a parameter file.
2. Select the mode of serial communication and serial clock with a type command.
3. Make the settings according to the example of settings for PG-FP3 shown below.

Table 5-3. Example of Settings for PG-FP3

Communication Mode	Example of Settings for PG-FP3		V _{PP} Pulse Number ^{Note 1}
3-wire serial I/O	COMM PORT	SIO-ch0	0
	CPU CLK	On Target Board	
		In Flashpro	
	On Target Board	4.1943 MHz	
	SIO CLK	1.0 MHz	
	In Flashpro	4.0 MHz	
SIO CLK	1.0 MHz		
UART	COMM PORT	UART-ch0	8
	CPU CLK	On Target Board	
	On Target Board	4.1943 MHz	
	UART BPS	9600 bps ^{Note 2}	
Pseudo 3-wire serial I/O	COMM PORT	Port A	12
	CPU CLK	On Target Board	
		In Flashpro	
	On Target Board	4.1943 MHz	
	SIO CLK	1.0 MHz	
	In Flashpro	4.0 MHz	
	SIO CLK	1.0 MHz	
	COMM PORT	Port B	13
	CPU CLK	On Target Board	
		In Flashpro	
On Target Board	4.1943 MHz		
SIO CLK	1.0 MHz		
In Flashpro	4.0 MHz		
SIO CLK	1.0 MHz		

- Notes**
1. This is the number of V_{PP} pulses that are supplied by the Flashpro III at serial communication initialization. The pins that will be used for communication are determined according to this number.
 2. Select one of 9600 bps, 19200 bps, 38400 bps, or 76800 bps.

Remark COMM PORT: Serial port selection
 SIO CLK: Serial clock frequency selection
 CPU CLK: Input CPU clock source selection

6. INSTRUCTION SET OVERVIEW

The instruction set for the μPD78F9026A is listed later in this section.

6.1 Conventions

6.1.1 Operand identifiers and descriptions

The description made in the operand field of each instruction conforms to the operand identifier for the instructions listed below (the details conform to the assembly specifications). If more than one operand identifier is listed for an instruction, one is selected. Uppercase letters, #, !, \$, and [] are used to specify keywords, which must be written exactly as they appear. The meanings of these special characters are as follows:

- #: Immediate data specification
- \$: Relative address specification
- !: Absolute address specification
- []: Indirect address specification

Immediate data should be described using appropriate values or labels. The specification of values and labels must be accompanied by #, !, \$, or [].

Operand registers, expressed by the identifiers r or rp, can be described using both functional names (X, A, C, etc.) and absolute names (R0, R1, R2, and other names listed inside the parentheses in Table 6-1).

Table 6-1. Operand Formats and Descriptions

Identifier	Description
r rp sfr	X (R0), A (R1), C (R2), B (R3), E (R4), D (R5), L (R6), H (R7) AX (RP0), BC (RP1), DE (RP2), HL (RP3) Special function register symbol
saddr saddrp	FE20H to FF1FH: Immediate data or label FE20H to FF1FH: Immediate data or label (even addresses only)
addr16 addr5	0000H to FFFFH: Immediate data or label (only even address for 16-bit data transfer instructions) 0040H to 007FH: Immediate data or label (even addresses only)
word byte bit	16-bit immediate data or label 8-bit immediate data or label 3-bit immediate data or label

6.1.2 Descriptions of the operation field

A:	A register (8-bit accumulator)
X:	X register
B:	B register
C:	C register
D:	D register
E:	E register
H:	H register
L:	L register
AX:	AX register pair (16-bit accumulator)
BC:	BC register pair
DE:	DE register pair
HL:	HL register pair
PC:	Program counter
SP:	Stack pointer
PSW:	Program status word
CY:	Carry flag
AC:	Auxiliary carry flag
Z:	Zero flag
IE:	Interrupt request enable flag
NMIS:	Flag to indicate that a non-maskable interrupt is being handled
():	Contents of a memory location indicated by a parenthesized address or register name
X _H , X _L :	Upper and lower 8 bits of a 16-bit register
∧:	Logical product (AND)
∨:	Logical sum (OR)
⊕:	Exclusive OR
—:	Inverted data
addr16:	16-bit immediate data or label
jdsp8:	Signed 8-bit data (displacement value)

6.1.3 Description of the flag operation field

(blank):	No change
0:	To be cleared to 0
1:	To be set to 1
x:	To be set or cleared according to the result
R:	To be restored to the previous value

6.2 Operations

Mnemonic	Operand	Byte	Clock	Operation	Flag		
					Z	AC	CY
MOV	r, #byte	3	6	$r \leftarrow \text{byte}$			
	saddr, #byte	3	6	$(\text{saddr}) \leftarrow \text{byte}$			
	sfr, #byte	3	6	$\text{sfr} \leftarrow \text{byte}$			
	A, r <small>Note 1</small>	2	4	$A \leftarrow r$			
	r, A <small>Note 1</small>	2	4	$r \leftarrow A$			
	A, saddr	2	4	$A \leftarrow (\text{saddr})$			
	saddr, A	2	4	$(\text{saddr}) \leftarrow A$			
	A, sfr	2	4	$A \leftarrow \text{sfr}$			
	sfr, A	2	4	$\text{sfr} \leftarrow A$			
	A, !addr16	3	8	$A \leftarrow (\text{addr16})$			
	!addr16, A	3	8	$(\text{addr16}) \leftarrow A$			
	PSW, #byte	3	6	$\text{PSW} \leftarrow \text{byte}$	x	x	x
	A, PSW	2	4	$A \leftarrow \text{PSW}$			
	PSW, A	2	4	$\text{PSW} \leftarrow A$	x	x	x
	A, [DE]	1	6	$A \leftarrow (\text{DE})$			
	[DE], A	1	6	$(\text{DE}) \leftarrow A$			
	A, [HL]	1	6	$A \leftarrow (\text{HL})$			
	[HL], A	1	6	$(\text{HL}) \leftarrow A$			
	A, [HL + byte]	2	6	$A \leftarrow (\text{HL} + \text{byte})$			
	[HL + byte], A	2	6	$(\text{HL} + \text{byte}) \leftarrow A$			
XCH	A, X	1	4	$A \leftrightarrow X$			
	A, r <small>Note 2</small>	2	6	$A \leftrightarrow r$			
	A, saddr	2	6	$A \leftrightarrow (\text{saddr})$			
	A, sfr	2	6	$A \leftrightarrow (\text{sfr})$			
	A, [DE]	1	8	$A \leftrightarrow (\text{DE})$			
	A, [HL]	1	8	$A \leftrightarrow (\text{HL})$			
	A, [HL + byte]	2	8	$A \leftrightarrow (\text{HL} + \text{byte})$			
MOVW	rp, #word	3	6	$\text{rp} \leftarrow \text{word}$			
	AX, saddrp	2	6	$\text{AX} \leftarrow (\text{saddrp})$			
	saddrp, AX	2	8	$(\text{saddrp}) \leftarrow \text{AX}$			
	AX, rp <small>Note 3</small>	1	4	$\text{AX} \leftarrow \text{rp}$			
	rp, AX <small>Note 3</small>	1	4	$\text{rp} \leftarrow \text{AX}$			

- Notes**
1. Except when $r = A$.
 2. Except when $r = A$ or X .
 3. Only when $\text{rp} = \text{BC}, \text{DE},$ or HL .

Remark The instruction clock cycle is based on the CPU clock (f_{CPU}), specified by the processor clock control register (PCC).

Mnemonic	Operand	Byte	Clock	Operation	Flag		
					Z	AC	CY
XCHW	AX, rp ^{Note}	1	8	AX ↔ rp			
ADD	A, #byte	2	4	A, CY ← A + byte	x	x	x
	saddr, #byte	3	6	(saddr), CY ← (saddr) + byte	x	x	x
	A, r	2	4	A, CY ← A + r	x	x	x
	A, saddr	2	4	A, CY ← A + (saddr)	x	x	x
	A, !addr16	3	8	A, CY ← A + (addr16)	x	x	x
	A, [HL]	1	6	A, CY ← A + (HL)	x	x	x
	A, [HL + byte]	2	6	A, CY ← A + (HL + byte)	x	x	x
ADDC	A, #byte	2	4	A, CY ← A + byte + CY	x	x	x
	saddr, #byte	3	6	(saddr), CY ← (saddr) + byte + CY	x	x	x
	A, r	2	4	A, CY ← A + r + CY	x	x	x
	A, saddr	2	4	A, CY ← A + (saddr) + CY	x	x	x
	A, !addr16	3	8	A, CY ← A + (addr16) + CY	x	x	x
	A, [HL]	1	6	A, CY ← A + (HL) + CY	x	x	x
	A, [HL + byte]	2	6	A, CY ← A + (HL + byte) + CY	x	x	x
SUB	A, #byte	2	4	A, CY ← A - byte	x	x	x
	saddr, #byte	3	6	(saddr), CY ← (saddr) - byte	x	x	x
	A, r	2	4	A, CY ← A - r	x	x	x
	A, saddr	2	4	A, CY ← A - (saddr)	x	x	x
	A, !addr16	3	8	A, CY ← A - (addr16)	x	x	x
	A, [HL]	1	6	A, CY ← A - (HL)	x	x	x
	A, [HL + byte]	2	6	A, CY ← A - (HL + byte)	x	x	x
SUBC	A, #byte	2	4	A, CY ← A - byte - CY	x	x	x
	saddr, #byte	3	6	(saddr), CY ← (saddr) - byte - CY	x	x	x
	A, r	2	4	A, CY ← A - r - CY	x	x	x
	A, saddr	2	4	A, CY ← A - (saddr) - CY	x	x	x
	A, !addr16	3	8	A, CY ← A - (addr16) - CY	x	x	x
	A, [HL]	1	6	A, CY ← A - (HL) - CY	x	x	x
	A, [HL + byte]	2	6	A, CY ← A - (HL + byte) - CY	x	x	x
AND	A, #byte	2	4	A ← A ∧ byte	x		
	saddr, #byte	3	6	(saddr) ← (saddr) ∧ byte	x		
	A, r	2	4	A ← A ∧ r	x		
	A, saddr	2	4	A ← A ∧ (saddr)	x		
	A, !addr16	3	8	A ← A ∧ (addr16)	x		
	A, [HL]	1	6	A ← A ∧ (HL)	x		
	A, [HL + byte]	2	6	A ← A ∧ (HL + byte)	x		

Note Only when rp = BC, DE, or HL.

Remark The instruction clock cycle is based on the CPU clock (f_{cpu}), specified by the processor clock control register (PCC).

Mnemonic	Operand	Byte	Clock	Operation	Flag		
					Z	AC	CY
OR	A, #byte	2	4	$A \leftarrow A \vee \text{byte}$	×		
	saddr, #byte	3	6	$(\text{saddr}) \leftarrow (\text{saddr}) \vee \text{byte}$	×		
	A, r	2	4	$A \leftarrow A \vee r$	×		
	A, saddr	2	4	$A \leftarrow A \vee (\text{saddr})$	×		
	A, !addr16	3	8	$A \leftarrow A \vee (\text{addr16})$	×		
	A, [HL]	1	6	$A \leftarrow A \vee (\text{HL})$	×		
	A, [HL + byte]	2	6	$A \leftarrow A \vee (\text{HL} + \text{byte})$	×		
XOR	A, #byte	2	4	$A \leftarrow A \nabla \text{byte}$	×		
	saddr, #byte	3	6	$(\text{saddr}) \leftarrow (\text{saddr}) \nabla \text{byte}$	×		
	A, r	2	4	$A \leftarrow A \nabla r$	×		
	A, saddr	2	4	$A \leftarrow A \nabla (\text{saddr})$	×		
	A, !addr16	3	8	$A \leftarrow A \nabla (\text{addr16})$	×		
	A, [HL]	1	6	$A \leftarrow A \nabla (\text{HL})$	×		
	A, [HL + byte]	2	6	$A \leftarrow A \nabla (\text{HL} + \text{byte})$	×		
CMP	A, #byte	2	4	$A - \text{byte}$	×	×	×
	saddr, #byte	3	6	$(\text{saddr}) - \text{byte}$	×	×	×
	A, r	2	4	$A - r$	×	×	×
	A, saddr	2	4	$A - (\text{saddr})$	×	×	×
	A, !addr16	3	8	$A - (\text{addr16})$	×	×	×
	A, [HL]	1	6	$A - (\text{HL})$	×	×	×
	A, [HL + byte]	2	6	$A - (\text{HL} + \text{byte})$	×	×	×
ADDW	AX, #word	3	6	$\text{AX}, \text{CY} \leftarrow \text{AX} + \text{word}$	×	×	×
SUBW	AX, #word	3	6	$\text{AX}, \text{CY} \leftarrow \text{AX} - \text{word}$	×	×	×
CMPW	AX, #word	3	6	$\text{AX} - \text{word}$	×	×	×
INC	r	2	4	$r \leftarrow r + 1$	×	×	
	saddr	2	4	$(\text{saddr}) \leftarrow (\text{saddr}) + 1$	×	×	
DEC	r	2	4	$r \leftarrow r - 1$	×	×	
	saddr	2	4	$(\text{saddr}) \leftarrow (\text{saddr}) - 1$	×	×	
INCW	rp	1	4	$\text{rp} \leftarrow \text{rp} + 1$			
DECW	rp	1	4	$\text{rp} \leftarrow \text{rp} - 1$			
ROR	A, 1	1	2	$(\text{CY}, \text{A}_7 \leftarrow \text{A}_0, \text{A}_{m-1} \leftarrow \text{A}_m) \times 1$			×
ROL	A, 1	1	2	$(\text{CY}, \text{A}_0 \leftarrow \text{A}_7, \text{A}_{m+1} \leftarrow \text{A}_m) \times 1$			×
RORC	A, 1	1	2	$(\text{CY} \leftarrow \text{A}_0, \text{A}_7 \leftarrow \text{CY}, \text{A}_{m-1} \leftarrow \text{A}_m) \times 1$			×
ROLC	A, 1	1	2	$(\text{CY} \leftarrow \text{A}_7, \text{A}_0 \leftarrow \text{CY}, \text{A}_{m+1} \leftarrow \text{A}_m) \times 1$			×

Remark The instruction clock cycle is based on the CPU clock (f_{CPU}), specified by the processor clock control register (PCC).

Mnemonic	Operand	Byte	Clock	Operation	Flag		
					Z	AC	CY
SET1	saddr. bit	3	6	(saddr. bit) ← 1			
	sfr. bit	3	6	sfr. bit ← 1			
	A. bit	2	4	A. bit ← 1			
	PSW. bit	3	6	PSW. bit ← 1	x	x	x
	[HL]. bit	2	10	(HL). bit ← 1			
CLR1	saddr. bit	3	6	(saddr. bit) ← 0			
	sfr. bit	3	6	sfr. bit ← 0			
	A. bit	2	4	A. bit ← 0			
	PSW. bit	3	6	PSW. bit ← 0	x	x	x
	[HL]. bit	2	10	(HL). bit ← 0			
SET1	CY	1	2	CY ← 1			1
CLR1	CY	1	2	CY ← 0			0
NOT1	CY	1	2	CY ← \overline{CY}			x
CALL	!addr16	3	6	(SP - 1) ← (PC + 3) _H , (SP - 2) ← (PC + 3) _L , PC ← addr16, SP ← SP - 2			
CALLT	[addr5]	1	8	(SP - 1) ← (PC + 1) _H , (SP - 2) ← (PC + 1) _L , PC _H ← (00000000, addr5 + 1), PC _L ← (00000000, addr5), SP ← SP - 2			
RET		1	6	PC _H ← (SP + 1), PC _L ← (SP), SP ← SP + 2			
RETI		1	8	PC _H ← (SP + 1), PC _L ← (SP), PSW ← (SP + 2), SP ← SP + 3, NMIS ← 0	R	R	R
PUSH	PSW	1	2	(SP - 1) ← PSW, SP ← SP - 1			
	rp	1	4	(SP - 1) ← rp _H , (SP - 2) ← rp _L , SP ← SP - 2			
POP	PSW	1	4	PSW ← (SP), SP ← SP + 1	R	R	R
	rp	1	6	rp _H ← (SP + 1), rp _L ← (SP), SP ← SP + 2			
MOVW	SP, AX	2	8	SP ← AX			
	AX, SP	2	6	AX ← SP			
BR	!addr16	3	6	PC ← addr16			
	\$addr16	2	6	PC ← PC + 2 + jdisp8			
	AX	1	6	PC _H ← A, PC _L ← X			

Remark The instruction clock cycle is based on the CPU clock (f_{CPU}), specified by the processor clock control register (PCC).

Mnemonic	Operand	Byte	Clock	Operation	Flag		
					Z	AC	CY
BC	\$addr16	2	6	$PC \leftarrow PC + 2 + jdisp8$ if $CY = 1$			
BNC	\$addr16	2	6	$PC \leftarrow PC + 2 + jdisp8$ if $CY = 0$			
BZ	\$addr16	2	6	$PC \leftarrow PC + 2 + jdisp8$ if $Z = 1$			
BNZ	\$addr16	2	6	$PC \leftarrow PC + 2 + jdisp8$ if $Z = 0$			
BT	saddr. bit, \$addr16	4	10	$PC \leftarrow PC + 4 + jdisp8$ if (saddr. bit) = 1			
	sfr. bit, \$addr16	4	10	$PC \leftarrow PC + 4 + jdisp8$ if sfr. bit = 1			
	A. bit, \$addr16	3	8	$PC \leftarrow PC + 3 + jdisp8$ if A. bit = 1			
	PSW. bit, \$addr16	4	10	$PC \leftarrow PC + 4 + jdisp8$ if PSW. bit = 1			
BF	saddr. bit, \$addr16	4	10	$PC \leftarrow PC + 4 + jdisp8$ if (saddr. bit) = 0			
	sfr. bit, \$addr16	4	10	$PC \leftarrow PC + 4 + jdisp8$ if sfr. bit = 0			
	A. bit, \$addr16	3	8	$PC \leftarrow PC + 3 + jdisp8$ if A. bit = 0			
	PSW. bit, \$addr16	4	10	$PC \leftarrow PC + 4 + jdisp8$ if PSW. bit = 0			
DBNZ	B, \$addr16	2	6	$B \leftarrow B - 1$, then $PC \leftarrow PC + 2 + jdisp8$ if $B \neq 0$			
	C, \$addr16	2	6	$C \leftarrow C - 1$, then $PC \leftarrow PC + 2 + jdisp8$ if $C \neq 0$			
	saddr, \$addr16	3	8	(saddr) \leftarrow (saddr) - 1, then $PC \leftarrow PC + 3 + jdisp8$ if (saddr) $\neq 0$			
NOP		1	2	No Operation			
EI		3	6	$IE \leftarrow 1$ (Enable Interrupt)			
DI		3	6	$IE \leftarrow 0$ (Disable Interrupt)			
HALT		1	2	Set HALT Mode			
STOP		1	2	Set STOP Mode			

Remark The instruction clock cycle is based on the CPU clock (f_{cpu}), specified by the processor clock control register (PCC).

7. ELECTRICAL SPECIFICATIONS

Absolute Maximum Ratings (T_A = 25°C)

Parameter	Symbol	Conditions	Ratings	Unit
Supply voltage	V _{DD}		-0.3 to +6.5	V
	V _{PP}		-0.3 to +10.5	V
Input voltage	V _I		-0.3 to V _{DD} + 0.3	V
Output voltage	V _O		-0.3 to V _{DD} + 0.3	V
Output current, high	I _{OH}	Per pin	-10	mA
		Total for all pins	-30	mA
Output current, low	I _{OL}	Per pin	30	mA
		Total for all pins	160	mA
Operating ambient temperature	T _A	In normal operation mode	-40 to +85	°C
		During flash memory programming	10 to 40	°C
Storage temperature	T _{stg}		-40 to +125	°C

Caution Product quality may suffer if the maximum absolute ratings exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of port pins.

Capacitance (T_A = 25°C, V_{DD} = V_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Input capacitance	C _{IN}	f = 1 MHz			15	pF
Output capacitance	C _{OUT}	Unmeasured pins returned to 0 V			15	pF
Input/output capacitance	C _{IO}				15	pF

System Clock Oscillator Characteristics (T_A = -40°C to +85°C, V_{DD} = 1.8 to 5.5 V)

Resonator	Recommended Circuit	Parameter	Conditions	MIN.	TYP.	MAX.	Unit
Ceramic resonator		Oscillation frequency (f _x) ^{Note 1}	V _{DD} = Oscillation voltage range	1.0		5.0	MHz
		Oscillation stabilization time ^{Note 2}	After V _{DD} reaches the oscillation voltage range MIN.			4	ms
Crystal resonator		Oscillation frequency (f _x) ^{Note 1}		1.0		5.0	MHz
		Oscillation stabilization time ^{Note 2}	V _{DD} = 4.5 to 5.5 V			10	ms
						30	
External clock		X1 input frequency (f _x) ^{Note 1}		1.0		5.0	MHz
		X1 input high-/low-level width (t _{xH} , t _{xL})		85		500	ns
		X1 input frequency (f _x) ^{Note 1}	V _{DD} = 2.7 to 5.5 V	1.0		5.0	MHz
		X1 input high-/low-level width (t _{xH} , t _{xL})	V _{DD} = 2.7 to 5.5 V	85		500	ns

- Notes**
1. Indicates only oscillator characteristics. Refer to AC Characteristics for instruction execution time.
 2. Time required to stabilize oscillation after reset or STOP mode release. Use a resonator whose oscillation is stabilized within the oscillation stabilization wait time.

Caution When using the system clock oscillator, wire as follows in the area enclosed by the broken lines in the above figures to avoid an adverse effect from wiring capacitance.

- Keep the wiring length as short as possible.
- Do not cross the wiring with the other signal lines.
- Do not route the wiring near a signal line through which a high fluctuating current flows.
- Always make the ground point of the oscillator capacitor the same potential as V_{SS0}.
- Do not ground the capacitor to a ground pattern through which a high current flows.
- Do not fetch signals from the oscillator.

DC Characteristics (T_A = -40°C to +85°C, V_{DD} = 1.8 to 5.5 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Output current, high	I _{OH}	Per pin				-1	mA
		Total for all pins				-15	mA
Output current, low	I _{OL}	Per pin				10	mA
		Total for all pins				80	mA
Input voltage, high	V _{IH1}	P00 to P07, P10 to P17, P21, P51 to 53	V _{DD} = 2.7 to 5.5 V	0.7V _{DD}		V _{DD}	V
				0.9V _{DD}		V _{DD}	V
	V _{IH2}	P20, P22, P30 to P32, P40 to P47, P50, RESET	V _{DD} = 2.7 to 5.5 V	0.8V _{DD}		V _{DD}	V
				0.9V _{DD}		V _{DD}	V
	V _{IH3}	X1, X2	V _{DD} = 5.0±10%	V _{DD} - 0.5		V _{DD}	V
				V _{DD} - 0.1		V _{DD}	V
Input voltage, low	V _{IL1}	P00 to P07, P10 to P17, P21, P51 to P53	V _{DD} = 2.7 to 5.5 V	0		0.3V _{DD}	V
				0		0.1V _{DD}	V
	V _{IL2}	P20, P22, P30 to P32, P40 to P47, P50, RESET	V _{DD} = 2.7 to 5.5 V	0		0.2V _{DD}	V
				0		0.1V _{DD}	V
	V _{IL3}	X1, X2	V _{DD} = 5.0±10%	0		0.4	V
				0		0.1	V
Output voltage, high	V _{OH}	V _{DD} = 4.5 to 5.5 V, I _{OH} = -1 mA		V _{DD} - 1.0			V
		V _{DD} = 1.8 to 5.5 V, I _{OH} = -100 μA		V _{DD} - 0.5			V
Output voltage, low	V _{OL}	V _{DD} = 4.5 to 5.5 V, I _{OL} = 10 mA				1.0	V
		V _{DD} = 1.8 to 5.5 V, I _{OL} = 400 μA				0.5	V
Input leakage current, high	I _{LIH1}	V _{IN} = V _{DD}	Pins other than X1 and X2			3	μA
	I _{LIH2}		X1, X2			20	μA
Input leakage current, low	I _{LIL1}	V _{IN} = 0 V	Pins other than X1 and X2			-3	μA
	I _{LIL2}		X1, X2			-20	μA
Output leakage current, high	I _{LOH}	V _{OUT} = V _{DD}				3	μA
Output leakage current, low	I _{LOL}	V _{OUT} = 0 V				-3	μA
Software pull-up resistor	R	V _{IN} = 0 V		50	100	200	kΩ
Supply current ^{Note 1}	I _{DD1}	5.0-MHz crystal oscillation operating mode (C1 = C2 = 22 pF)	V _{DD} = 5.0 V±10% ^{Note 2}		4.0	15.0	mA
			V _{DD} = 3.0 V±10% ^{Note 3}		1.0	5.0	mA
			V _{DD} = 2.0 V±10% ^{Note 3}		0.8	3.0	mA
	I _{DD2}	5.0-MHz crystal oscillation HALT mode (C1 = C2 = 22 pF)	V _{DD} = 5.0 V±10% ^{Note 2}		0.8	5.0	mA
			V _{DD} = 3.0 V±10% ^{Note 3}		0.5	2.5	mA
			V _{DD} = 2.0 V±10% ^{Note 3}		0.3	1.0	mA
	I _{DD3}	STOP mode	V _{DD} = 5.0 V±10%		0.1	30	μA
			V _{DD} = 3.0 V±10%		0.05	10	μA
			V _{DD} = 2.0 V±10%		0.05	10	μA

Notes 1. The current flowing to the ports (including the current flowing through the on-chip pull-up resistors) is not included.

2. High-speed mode operation (when the processor clock control register (PCC) is set to 00H)

3. Low-speed mode operation (when PCC is set to 02H)

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of port pins.

Flash Memory Write/Delete Characteristics

($T_A = 10$ to 40°C , $V_{DD} = 1.8$ to 5.5 V, in 5.0-MHz crystal oscillation operation mode)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Write current ^{Note} (V_{DD} pin)	I_{DDW}	When V_{PP} supply voltage = V_{PP1}			18	mA
Write current ^{Note} (V_{PP} pin)	I_{PPW}	When V_{PP} supply voltage = V_{PP1}			22.5	mA
Delete current ^{Note} (V_{DD} pin)	I_{DDE}	When V_{PP} supply voltage = V_{PP1}			18	mA
Delete current ^{Note} (V_{PP} pin)	I_{PPE}	When V_{PP} supply voltage = V_{PP1}			115	mA
Unit delete time	t_{er}		0.5	1	1	s
Total delete time	t_{era}				20	s
Write count		Delete/write are regarded as 1 cycle	20	20	20	Times
V_{PP} supply voltage	V_{PP0}	In normal operation	0		$0.2V_{DD}$	V
	V_{PP1}	During flash memory programming	9.7	10.0	10.3	V

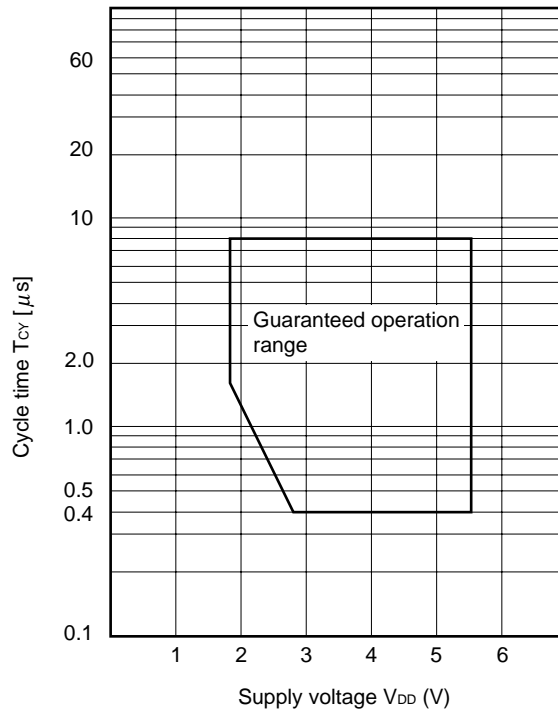
Note The current flowing to the ports (including the current flowing through the on-chip pull-up resistors) is not included.

AC Characteristics

(1) Basic operation (T_A = -40°C to +85°C, V_{DD} = 1.8 to 5.5 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Cycle time (minimum instruction execution time)	T _{CY}	V _{DD} = 2.7 to 5.5 V	0.4		8	μs
			1.6		8	μs
TIO input high-/low- level width	t _{TIH} , t _{TIL}	V _{DD} = 2.7 to 5.5 V	0.1			μs
			1.8			μs
TIO input frequency	f _{TI}	V _{DD} = 2.7 to 5.5 V	0		4	MHz
			0		275	kHz
Interrupt input high-/low-level width	t _{INTH} , t _{INTL}	INTP0 to INTP2	10			μs
RESET low-level width	t _{RSL}		10			μs

T_{CY} vs V_{DD} (system clock)



(2) Serial interface 00 (T_A = -40°C to +85°C, V_{DD} = 1.8 to 5.5 V)

(i) 3-wire serial I/O mode ($\overline{\text{SCK0}}$...Internal clock output)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit	
$\overline{\text{SCK0}}$ cycle time	t _{KCY1}	V _{DD} = 2.7 to 5.5 V	800			ns	
			3200			ns	
$\overline{\text{SCK0}}$ high-/low-level width	t _{KH1} , t _{KL1}	V _{DD} = 2.7 to 5.5 V	t _{KCY1} /2 - 50			ns	
			t _{KCY1} /2 - 150			ns	
SI0 setup time (to $\overline{\text{SCK0}}$ ↑)	t _{SIK1}	V _{DD} = 2.7 to 5.5 V	150			ns	
			500			ns	
SI0 hold time (from $\overline{\text{SCK0}}$ ↑)	t _{KS1}	V _{DD} = 2.7 to 5.5 V	400			ns	
			600			ns	
SO0 output delay time from $\overline{\text{SCK0}}$ ↓	t _{KSO1}	R = 1 kΩ, C = 100 pF ^{Note}	V _{DD} = 2.7 to 5.5 V	0		250	ns
				0		1000	ns

Note R and C are the load resistance and load capacitance of the SO0 output line, respectively.

(ii) 3-wire serial I/O mode ($\overline{\text{SCK0}}$...External clock input)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit	
$\overline{\text{SCK0}}$ cycle time	t _{KCY2}	V _{DD} = 2.7 to 5.5 V	900			ns	
			3500			ns	
$\overline{\text{SCK0}}$ high-/low-level width	t _{KH2} , t _{KL2}	V _{DD} = 2.7 to 5.5 V	400			ns	
			1600			ns	
SI0 setup time (to $\overline{\text{SCK0}}$ ↑)	t _{SIK2}	V _{DD} = 2.7 to 5.5 V	100			ns	
			150			ns	
SI0 hold time (from $\overline{\text{SCK0}}$ ↑)	t _{KS2}	V _{DD} = 2.7 to 5.5 V	400			ns	
			600			ns	
SO0 output delay time from $\overline{\text{SCK0}}$ ↓	t _{KSO2}	R = 1 kΩ, C = 100 pF ^{Note}	V _{DD} = 2.7 to 5.5 V	0		300	ns
				0		1000	ns

Note R and C are the load resistance and load capacitance of the SO0 output line, respectively.

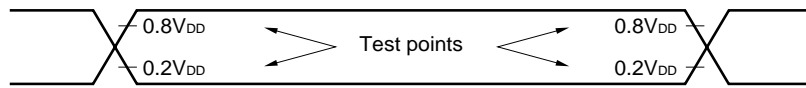
(iii) UART mode (Dedicated baud rate generator output)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Transfer rate		V _{DD} = 2.7 to 5.5 V			78125	bps
					19531	bps

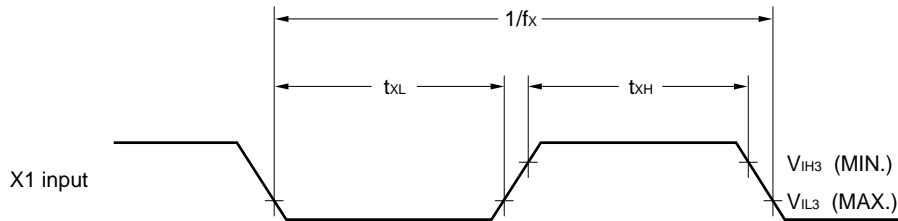
(iv) UART mode (External clock input)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
ASCK cycle time	t _{KCY3}	V _{DD} = 2.7 to 5.5 V	900			ns
			3500			ns
ASCK high-/low-level width	t _{KH3} , t _{KL3}	V _{DD} = 2.7 to 5.5 V	400			ns
			1600			ns
Transfer rate		V _{DD} = 2.7 to 5.5 V			39063	bps
					9766	bps
ASCK rise/fall time	t _R , t _F				1	μs

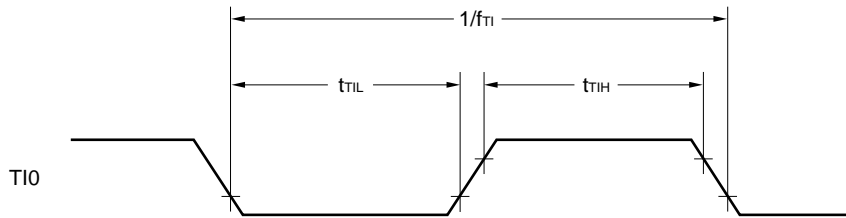
AC Timing Test Points (Except the X1 input)



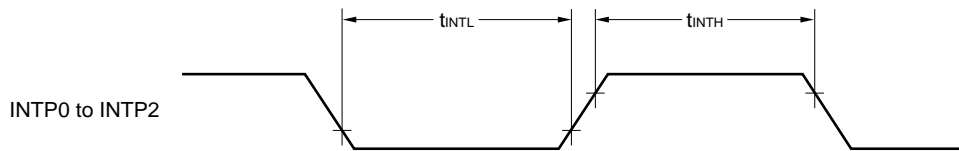
Clock Timing



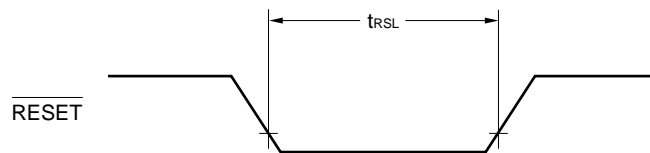
TI Timing



Interrupt Input Timing

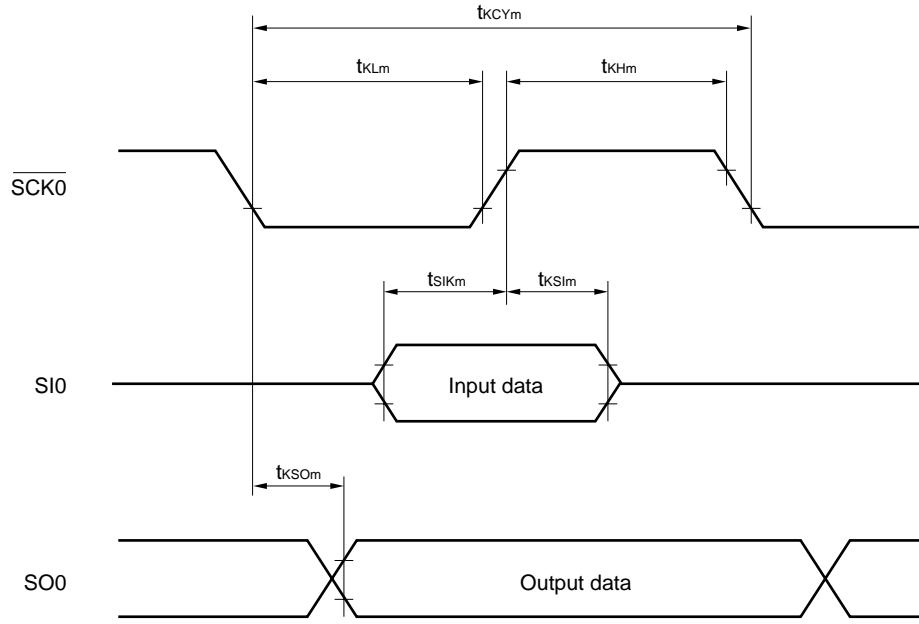


RESET Input Timing



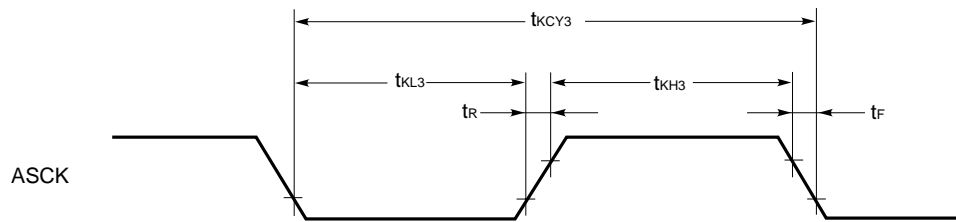
Serial Transfer Timing

3-wire serial I/O mode:



$m = 1, 2$

UART mode (External clock input):



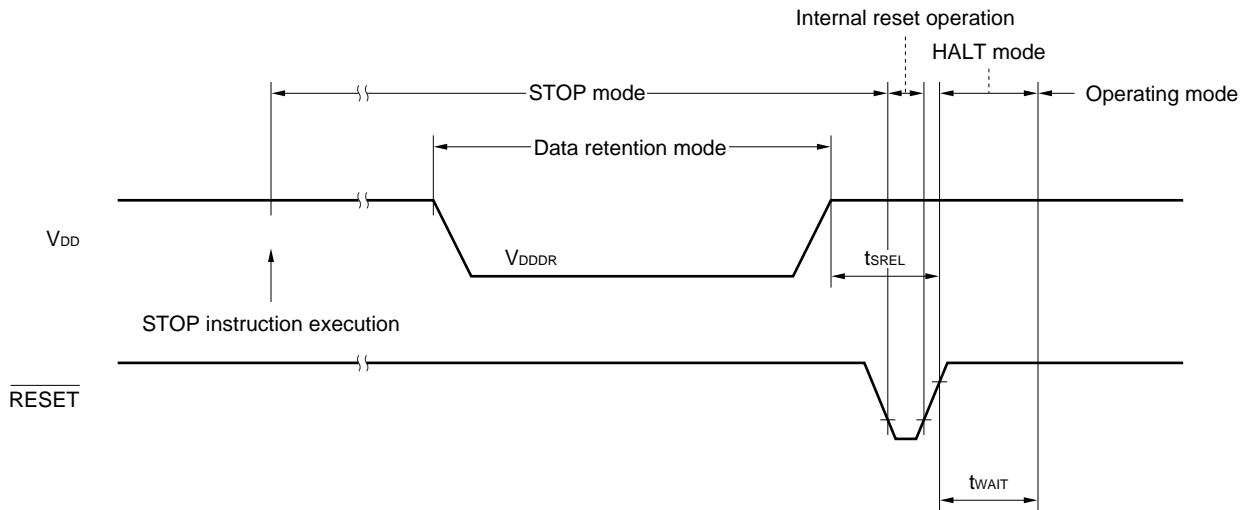
Data Memory Stop Mode Low Supply Voltage Data Retention Characteristics (T_A = -40°C to +85°C)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Data retention supply voltage	V _{DDDR}		1.8		5.5	V
Release signal set time	t _{SREL}		0			μs
Oscillation stabilization wait time	t _{WAIT}	Release by $\overline{\text{RESET}}$		2 ¹⁵ /f _x		ms
		Release by interrupt		Note		ms

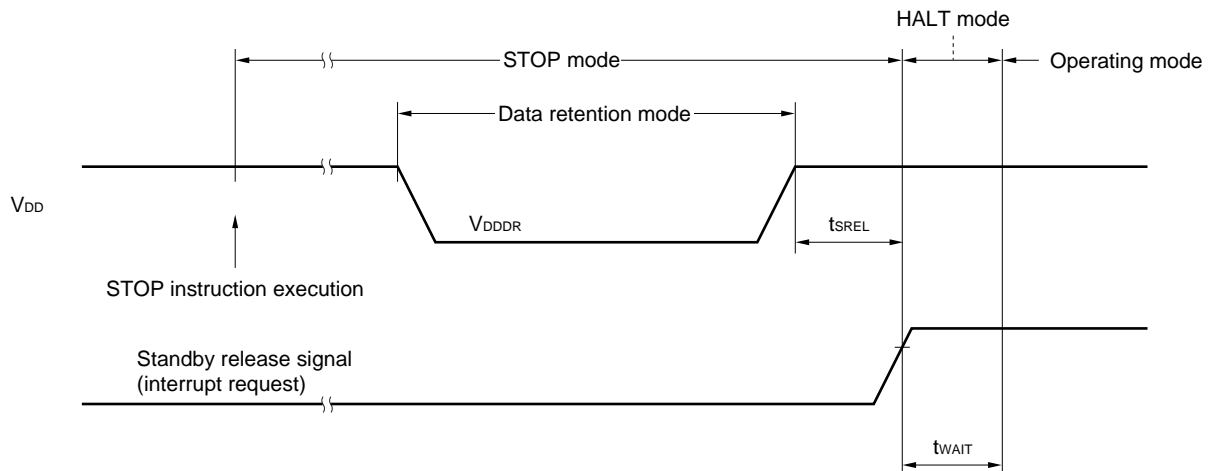
Note 2¹²/f_x, 2¹⁵/f_x, or 2¹⁷/f_x can be selected according to the setting of bits 0 to 2 (OSTS0 to OSTS2) of the oscillation stabilization time selection register.

Remark f_x: System clock oscillation frequency

Data Retention Timing (STOP mode release by $\overline{\text{RESET}}$)

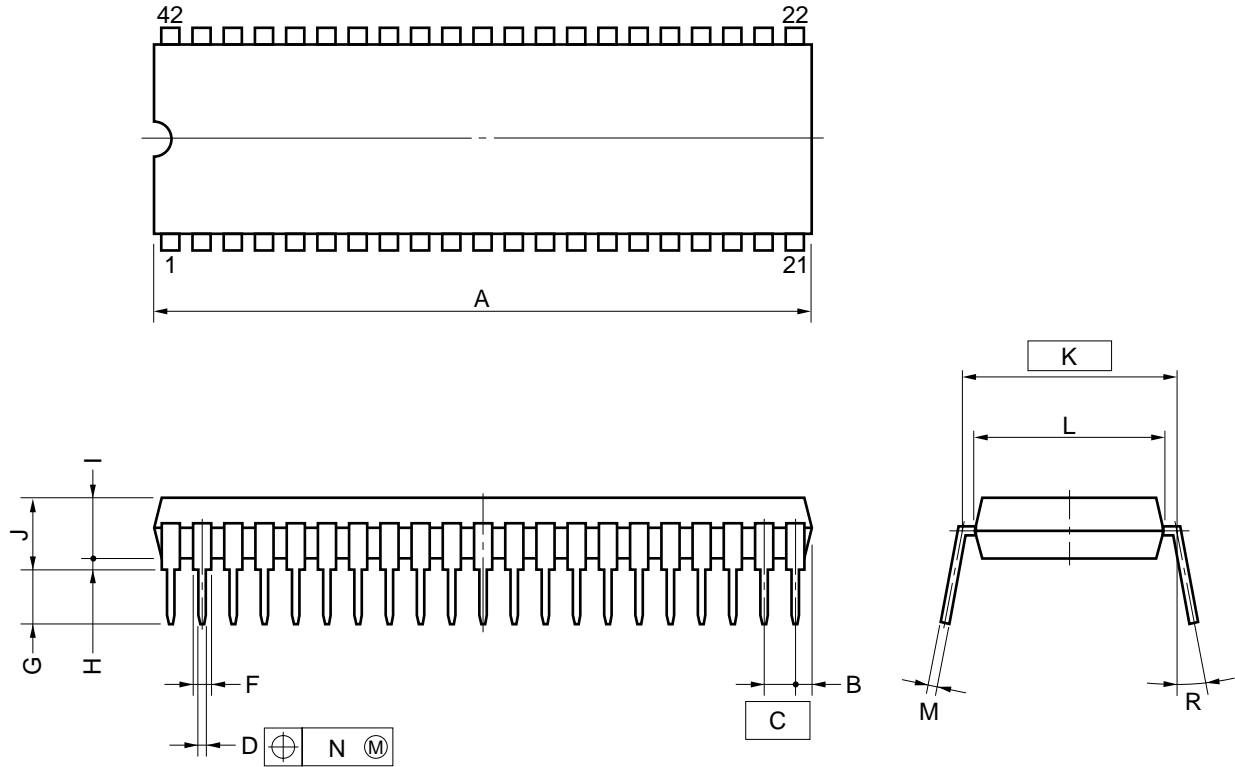


Data Retention Timing (Standby release signal: STOP mode release by interrupt signal)



8. PACKAGE DRAWINGS

42PIN PLASTIC SHRINK DIP (600 mil)



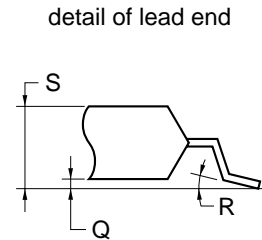
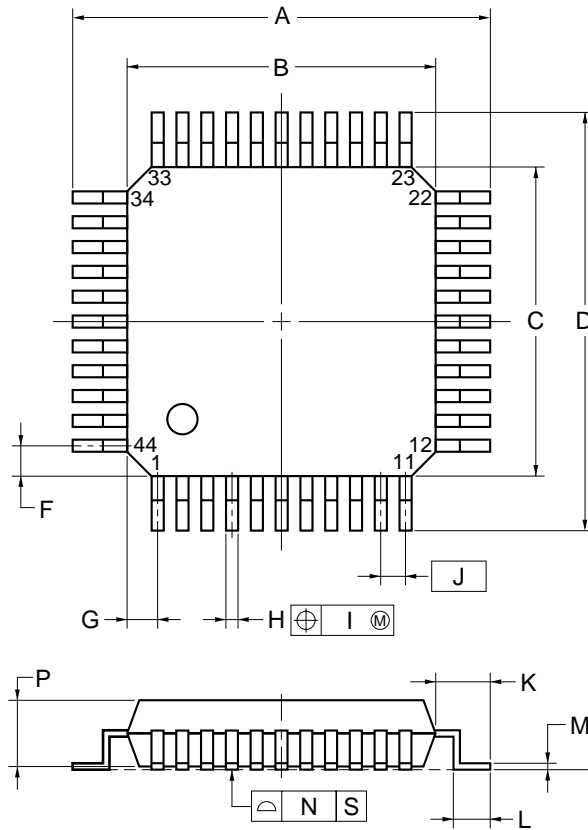
NOTES

- 1) Each lead centerline is located within 0.17 mm (0.007 inch) of its true position (T.P.) at maximum material condition.
- 2) Item "K" to center of leads when formed parallel.

ITEM	MILLIMETERS	INCHES
A	39.13 MAX.	1.541 MAX.
B	1.78 MAX.	0.070 MAX.
C	1.778 (T.P.)	0.070 (T.P.)
D	0.50±0.10	0.020 ^{+0.004} _{-0.005}
F	0.9 MIN.	0.035 MIN.
G	3.2±0.3	0.126±0.012
H	0.51 MIN.	0.020 MIN.
I	4.31 MAX.	0.170 MAX.
J	5.08 MAX.	0.200 MAX.
K	15.24 (T.P.)	0.600 (T.P.)
L	13.2	0.520
M	0.25 ^{+0.10} _{-0.05}	0.010 ^{+0.004} _{-0.003}
N	0.17	0.007
R	0~15°	0~15°

P42C-70-600A-1

44 PIN PLASTIC QFP (□10)



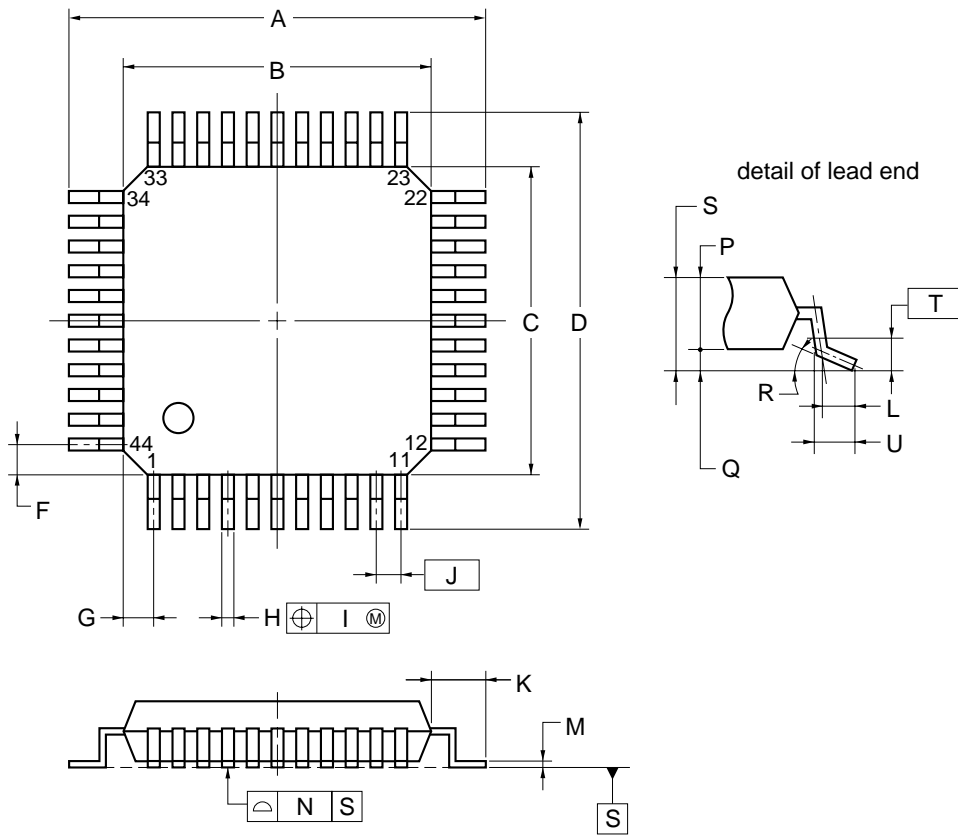
ITEM	MILLIMETERS	INCHES
A	13.2±0.2	0.520 ^{+0.008} _{-0.009}
B	10.0±0.2	0.394 ^{+0.008} _{-0.009}
C	10.0±0.2	0.394 ^{+0.008} _{-0.009}
D	13.2±0.2	0.520 ^{+0.008} _{-0.009}
F	1.0	0.039
G	1.0	0.039
H	0.37 ^{+0.08} _{-0.07}	0.015 ^{+0.003} _{-0.004}
I	0.16	0.007
J	0.8 (T.P.)	0.031 (T.P.)
K	1.6±0.2	0.063±0.008
L	0.8±0.2	0.031 ^{+0.009} _{-0.008}
M	0.17 ^{+0.06} _{-0.05}	0.007 ^{+0.002} _{-0.003}
N	0.10	0.004
P	2.7±0.1	0.106 ^{+0.005} _{-0.004}
Q	0.125±0.075	0.005±0.003
R	3° ^{+7°} _{-3°}	3° ^{+7°} _{-3°}
S	3.0 MAX.	0.119 MAX.

S44GB-80-3BS-1

NOTE

- Controlling dimension — millimeter.
- Each lead centerline is located within 0.16 mm (0.007 inch) of its true position (T.P.) at maximum material condition.

44 PIN PLASTIC LQFP (10x10)



NOTE

Each lead centerline is located within 0.16 mm of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS
A	12.0±0.2
B	10.0±0.2
C	10.0±0.2
D	12.0±0.2
F	1.0
G	1.0
H	0.37 ^{+0.08} _{-0.07}
I	0.2
J	0.8 (T.P.)
K	1.0±0.2
L	0.5
M	0.17 ^{+0.03} _{-0.06}
N	0.10
P	1.4±0.05
Q	0.1±0.05
R	3°+4° -3°
S	1.6 MAX.
U	0.6±0.15

S44GB-80-8ES-1

9. RECOMMENDED SOLDERING CONDITIONS

The μPD78F9026A should be soldered and mounted under the following recommended conditions.

For the details of the recommended soldering conditions, refer to the document **Semiconductor Device Mounting Technology Manual (C10535E)**.

For soldering methods and conditions other than those recommended below, contact your NEC sales representative.

Table 9-1. Surface Mounting Type Soldering Conditions

μPD78F9026AGB-3BS-MTX: 44-pin plastic QFP (10 × 10 mm, resin thickness 2.7 mm)

Soldering Method	Soldering Conditions	Recommended Condition Symbol
Infrared reflow	Package peak temperature: 235°C, Time: 30 sec. Max. (at 210°C or higher), Count: three times or less	IR35-00-3
VPS	Package peak temperature: 215°C, Time: 40 sec. Max. (at 200°C or higher), Count: three times or less	VP15-00-3
Wave soldering	Solder bath temperature: 260°C Max., Time: 10 sec. Max., Count: Once, Preheating temperature: 120°C Max. (package surface temperature)	WS60-00-1
Partial heating	Pin temperature: 300°C Max. Time: 3 sec. Max. (per pin row)	—

Caution Do not use different soldering methods together (except for partial heating).

μPD78F9026AGB-8ES: 44-pin plastic LQFP (10 × 10 mm, resin thickness 1.4 mm)

Soldering Method	Soldering Conditions	Recommended Condition Symbol
Infrared reflow	Package peak temperature: 235°C, Time: 30 sec. Max. (at 210°C or higher), Count: twice or less	IR35-00-2
VPS	Package peak temperature: 215°C, Time: 40 sec. Max. (at 200°C or higher), Count: twice or less	VP15-00-2
Wave soldering	Solder bath temperature: 260°C Max., Time: 10 sec. Max., Count: Once, Preheating temperature: 120°C Max. (package surface temperature)	WS60-00-1
Partial heating	Pin temperature: 300°C Max. Time: 3 sec. Max. (per pin row)	—

Caution Do not use different soldering methods together (except for partial heating).

Table 9-2. Insertion Type Soldering Conditions

μPD78F9026ACU: 42-pin plastic shrink DIP (600 mils)

Soldering Method	Soldering Conditions
Wave soldering (pin only)	Solder bath temperature: 260°C Max., Time: 10 sec. Max.
Partial heating	Pin temperature: 300°C Max., Time: 3 sec. Max. (for each pin)

Caution Apply wave soldering only to the pins and be careful not to bring solder into direct contact with the package.

APPENDIX A DIFFERENCES BETWEEN μPD78F9026A AND MASK ROM VERSIONS

The μPD78F9026A has flash memory in place of the internal ROM of the mask ROM versions (μPD789022, 789024, 789025, and 789026). Differences between the μPD78F9026A and mask ROM versions are shown in Table A-1.

Table A-1. Differences between μPD78F9026A and Mask ROM Versions

Parameter		Flash Memory Version	Mask ROM Versions			
		μPD78F9026A	μPD789022	μPD789024	μPD789025	μPD789026
Internal memory	ROM structure	Flash memory	Mask ROM			
	ROM capacity	16 Kbytes	4 Kbytes	8 Kbytes	12 Kbytes	16 Kbytes
	High-speed RAM capacity	512 bytes	256 bytes		512 bytes	
V _{PP} pin		Available	Not available			
IC pin		Not available	Available			
Electrical specifications		See the relevant data sheet				

Caution There are differences in noise immunity and noise radiation between the flash memory and mask ROM versions. When pre-producing an application set with the flash memory version and then mass-producing it with the mask ROM version, be sure to conduct sufficient evaluations for the consumer samples (not engineering samples) of the mask ROM version.

APPENDIX B DEVELOPMENT TOOLS

The following development tools are available for system development using the μPD78F9026A.

Language Processing Software

RA78K0S ^{Notes 1, 2, 3}	Assembler package common to 78K/0S Series
CC78K0S ^{Notes 1, 2, 3}	C compiler package common to 78K/0S Series
DF789026 ^{Note 6}	Device file for the μPD789026 Subseries
CC78K0S-L ^{Notes 1, 2, 3}	C compiler library source file common to 78K/0S Series

Flash Memory Writing Tools

Flashpro III (FL-PR3 ^{Note 4} , PG-FP3)	Dedicated flash programmer for microcontrollers incorporating flash memory
FA-42CU ^{Note 4}	Flash memory writing adapter for 42-pin plastic shrink DIP (CU type)
FA-44GB ^{Note 4}	Flash memory writing adapter for 44-pin plastic QFP (GB-3BS type)
FA-44GB-8ES ^{Note 4}	Flash memory writing adapter for 44-pin plastic LQFP (GB-8ES type)

Debugging Tools

IE-78K0S-NS In-circuit emulator	In-circuit emulator for debugging the hardware and software of the application system using the 78K/0S series. Supports the integrated debugger (ID78K0S-NS). Used with an AC adapter, emulation probe, and interface adapter that connects the host machine.
IE-70000-MC-PS-B AC adapter	Adapter that distributes power supply from an AC100 to 240-V outlet.
IE-70000-98-IF-C Interface adapter	Adapter when using a PC-9800 series PC (except notebook type) as the host machine of the IE-78K0S-NS (C bus supported).
IE-70000-CD-IF-A PC card interface	PC card and interface cable when using a notebook type PC as the host machine of the IE-78K0S-NS (PCMCIA socket supported).
IE-70000-PC-IF-C Interface adapter	Adapter when using an IBM PC/AT™ or compatible as the host machine of the IE-78K0S-NS (ISA bus supported).
IE-70000-PCI-IF Interface adapter	Adapter when using a PC with PCI bus as the host machine of the IE-78K0S-NS.
IE-789026-NS-EM1 Emulation board	Board for emulating device-specific peripheral hardware. Used with an in-circuit emulator.
NP-42CU ^{Note 4}	Board connecting an in-circuit emulator and target system. For 42-pin plastic shrink DIP (CU type).
NP-44GB ^{Note 4} NP-44GB-TQ ^{Note 4}	Board connecting an in-circuit emulator and target system. For 44-pin plastic QFP (GB-3BS type) and 44-pin plastic LQFP (GB-8ES type).
SM78K0S ^{Notes 1,2}	System simulator common to 78K/0S Series
ID78K0S-NS ^{Notes 1,2}	Integrated debugger common to 78K/0S Series
DF789026 ^{Notes 1,2}	Device file for μPD789026 Subseries

Real-Time OS

MX78K0S ^{Notes 1, 2}	OS for 78K/0S Series
-------------------------------	----------------------

- Notes**
1. Based on the PC-9800 series (MS-DOS™ + Windows™)
 2. Based on the IBM PC/AT and compatibles (Japanese/English Windows)
 3. Based on the HP9000 series 700™ (HP-UX™), SPARCstation™ (SunOS™, Solaris™), and NEWS™ (NEWS-OS™)
 4. Products manufactured by Naito Densetsu Machida Mfg. Co., Ltd. (+81-44-822-3813).

Remark The RA78K0S, CC78K0S, and SM78K0S can be used in combination with the DF789026.

APPENDIX C RELATED DOCUMENTS

Documents Related to Devices

Document Name	Document No.	
	English	Japanese
μPD789022, 789024, 789025, 789026 Data Sheet	U11715E	U11715J
μPD78F9026A Data Sheet	This manual	U14356J
μPD789026 Subseries User's Manual	U11919E	U11919J
78K/0S Series User's Manual — Instruction	U11047E	U11047J

Documents Related to Development Tools (User's Manuals)

Document Name		Document No.	
		English	Japanese
RA78K0S Assembler Package	Operation	U11622E	U11622J
	Assembly Language	U11599E	U11599J
	Structured Assembly Language	U11623E	U11623J
CC78K/0S C Compiler	Operation	U11816E	U11816J
	Language	U11817E	U11817J
SM78K0S System Simulator Windows Based	Reference	U11489E	U11489J
SM78K Series System Simulator	External Parts User Open Interface Specifications	U10092E	U10092J
ID78K0S-NS Integrated Debugger Windows Based	Reference	U12901E	U12901J
IE-78K0S-NS In-Circuit Emulator		U13549E	U13549J
IE-789026-NS-EM1 Emulation Board		To be prepared	To be prepared

Documents Related to Embedded Software (User's Manual)

Document Name	Document No.	
	English	Japanese
78K/0S Series OS MX78K0S	U12938E	U12938J

Caution The related documents listed above are subject to change without notice. Be sure to use the latest version of each document for designing.

Other Related Documents

Document Name	Document No.	
	English	Japanese
SEMICONDUCTOR SELECTION GUIDE Products & Packages (CD-ROM)	X13769X	
Semiconductor Device Mounting Technology Manual	C10535E	C10535J
Quality Grades on NEC Semiconductor Device	C11531E	C11531J
NEC Semiconductor Device Reliability/Quality Control System	C10983E	C10983J
Guide to Prevent Damage for Semiconductor Devices by Electrostatic Discharge (ESD)	C11892E	C11892J
Guide to Microcomputer-Related Products by Third Party	—	U11416J

Caution The related documents listed above are subject to change without notice. Be sure to use the latest version of each document for designing.

[MEMO]

NOTES FOR CMOS DEVICES**① PRECAUTION AGAINST ESD FOR SEMICONDUCTORS**

Note:

Strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor devices on it.

② HANDLING OF UNUSED INPUT PINS FOR CMOS

Note:

No connection for CMOS device inputs can be cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND with a resistor, if it is considered to have a possibility of being an output pin. All handling related to the unused pins must be judged device by device and related specifications governing the devices.

③ STATUS BEFORE INITIALIZATION OF MOS DEVICES

Note:

Power-on does not necessarily define initial status of MOS device. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the devices with reset function have not yet been initialized. Hence, power-on does not guarantee out-pin levels, I/O settings or contents of registers. Device is not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for devices having reset function.

EEPROM is a trademark of NEC Corporation.

MS-DOS and Windows are either registered trademarks or trademarks of Microsoft Corporation in the United States and/or other countries.

PC/AT is a trademark of International Business Machines Corporation.

HP9000 series 700 and HP-UX are trademarks of Hewlett-Packard Company.

SPARCstation is a trademark of SPARC International, Inc.

Solaris and SunOS are trademarks of Sun Microsystems, Inc.

NEWS and NEWS-OS are trademarks of Sony Corporation.

Regional Information

Some information contained in this document may vary from country to country. Before using any NEC product in your application, please contact the NEC office in your country to obtain a list of authorized representatives and distributors. They will verify:

- Device availability
- Ordering information
- Product release schedule
- Availability of related technical literature
- Development environment specifications (for example, specifications for third-party tools and components, host computers, power plugs, AC supply voltages, and so forth)
- Network requirements

In addition, trademarks, registered trademarks, export restrictions, and other legal issues may also vary from country to country.

NEC Electronics Inc. (U.S.)

Santa Clara, California
Tel: 408-588-6000
800-366-9782
Fax: 408-588-6130
800-729-9288

NEC Electronics (Germany) GmbH

Duesseldorf, Germany
Tel: 0211-65 03 02
Fax: 0211-65 03 490

NEC Electronics (UK) Ltd.

Milton Keynes, UK
Tel: 01908-691-133
Fax: 01908-670-290

NEC Electronics Italiana s.r.l.

Milano, Italy
Tel: 02-66 75 41
Fax: 02-66 75 42 99

NEC Electronics (Germany) GmbH

Benelux Office
Eindhoven, The Netherlands
Tel: 040-2445845
Fax: 040-2444580

NEC Electronics (France) S.A.

Velizy-Villacoublay, France
Tel: 01-30-67 58 00
Fax: 01-30-67 58 99

NEC Electronics (France) S.A.

Madrid Office
Madrid, Spain
Tel: 91-504-2787
Fax: 91-504-2860

NEC Electronics (Germany) GmbH

Scandinavia Office
Taeby, Sweden
Tel: 08-63 80 820
Fax: 08-63 80 388

NEC Electronics Hong Kong Ltd.

Hong Kong
Tel: 2886-9318
Fax: 2886-9022/9044

NEC Electronics Hong Kong Ltd.

Seoul Branch
Seoul, Korea
Tel: 02-528-0303
Fax: 02-528-4411

NEC Electronics Singapore Pte. Ltd.

United Square, Singapore
Tel: 65-253-8311
Fax: 65-250-3583

NEC Electronics Taiwan Ltd.

Taipei, Taiwan
Tel: 02-2719-2377
Fax: 02-2719-5951

NEC do Brasil S.A.

Electron Devices Division
Guarulhos-SP Brasil
Tel: 55-11-6462-6810
Fax: 55-11-6462-6829

J00.7

The related documents indicated in this publication may include preliminary versions. However, preliminary versions are not marked as such.

- **The information in this document is current as of September, 1999. The information is subject to change without notice. For actual design-in, refer to the latest publications of NEC's data sheets or data books, etc., for the most up-to-date specifications of NEC semiconductor products. Not all products and/or types are available in every country. Please check with an NEC sales representative for availability and additional information.**
 - No part of this document may be copied or reproduced in any form or by any means without prior written consent of NEC. NEC assumes no responsibility for any errors that may appear in this document.
 - NEC does not assume any liability for infringement of patents, copyrights or other intellectual property rights of third parties by or arising from the use of NEC semiconductor products listed in this document or any other liability arising from the use of such products. No license, express, implied or otherwise, is granted under any patents, copyrights or other intellectual property rights of NEC or others.
 - Descriptions of circuits, software and other related information in this document are provided for illustrative purposes in semiconductor product operation and application examples. The incorporation of these circuits, software and information in the design of customer's equipment shall be done under the full responsibility of customer. NEC assumes no responsibility for any losses incurred by customers or third parties arising from the use of these circuits, software and information.
 - While NEC endeavours to enhance the quality, reliability and safety of NEC semiconductor products, customers agree and acknowledge that the possibility of defects thereof cannot be eliminated entirely. To minimize risks of damage to property or injury (including death) to persons arising from defects in NEC semiconductor products, customers must incorporate sufficient safety measures in their design, such as redundancy, fire-containment, and anti-failure features.
 - NEC semiconductor products are classified into the following three quality grades:
"Standard", "Special" and "Specific". The "Specific" quality grade applies only to semiconductor products developed based on a customer-designated "quality assurance program" for a specific application. The recommended applications of a semiconductor product depend on its quality grade, as indicated below. Customers must check the quality grade of each semiconductor product before using it in a particular application.
"Standard": Computers, office equipment, communications equipment, test and measurement equipment, audio and visual equipment, home electronic appliances, machine tools, personal electronic equipment and industrial robots
"Special": Transportation equipment (automobiles, trains, ships, etc.), traffic control systems, anti-disaster systems, anti-crime systems, safety equipment and medical equipment (not specifically designed for life support)
"Specific": Aircraft, aerospace equipment, submersible repeaters, nuclear reactor control systems, life support systems and medical equipment for life support, etc.
- The quality grade of NEC semiconductor products is "Standard" unless otherwise expressly specified in NEC's data sheets or data books, etc. If customers wish to use NEC semiconductor products in applications not intended by NEC, they must contact an NEC sales representative in advance to determine NEC's willingness to support a given application.
- (Note)
- (1) "NEC" as used in this statement means NEC Corporation and also includes its majority-owned subsidiaries.
 - (2) "NEC semiconductor products" means any semiconductor product developed or manufactured by or for NEC (as defined above).

X-ON Electronics

Largest Supplier of Electrical and Electronic Components

Click to view similar products for [Microprocessors - MPU category](#):

Click to view products by [Renesas manufacturer](#):

Other Similar products are found below :

[MC68302EH20C](#) [MC7457RX1000LC](#) [MC7457RX1267LC](#) [MC7457VG1267LC](#) [A2C00010998 A](#) [A2C52004004](#) [R5F117BCGNA#20](#)
[R5F52106BDLA#U0](#) [R5S72690W266BG#U0](#) [ADJ3400IAA5DOE](#) [MPC8245TVV266D](#) [MPC8245TZU300D](#) [MPC8260ACVVMHBB](#)
[MPC8323ECVRAFDCA](#) [MPC8536ECVJAVLA](#) [BOXNUC5PGYH0AJ](#) [20-668-0024](#) [P1010NSN5DFB](#) [P2010NSN2MHC](#) [P2020NXE2HHC](#)
[P5020NSE7QMB](#) [P5020NSE7TNB](#) [P5020NSE7VNB](#) [LS1020ASN7KQB](#) [LS1020AXN7HNB](#) [LS1020AXN7KQB](#) [A2C00010729 A](#)
[A2C00039344](#) [T1022NSE7MQB](#) [T1022NXN7PQB](#) [T1023NSE7MQA](#) [T1024NXE7PQA](#) [T1042NSE7MQB](#) [T1042NSN7MQB](#)
[T1042NXN7WQB](#) [T2080NSE8TTB](#) [T2080NSN8PTB](#) [T2080NXE8TTB](#) [T2081NXN8TTB](#) [R5F101AFASP#V0](#) [MC68302CEH20C](#)
[TS68040MF33A](#) [MPC8260ACVVMIBB](#) [MPC8280CZUPEA](#) [MPC8313ECVRAFFC](#) [MPC8313ECVRAGDC](#) [MPC8313EVRADDC](#)
[MPC8313EVRAFFC](#) [MPC8313VRADDC](#) [MPC8314CVRAGDA](#)