NEC

MOS INTEGRATED CIRCUITS

# μPD78F9116B, 78F9116B(A)

## 8-BIT SINGLE-CHIP MICROCONTROLLERS

### DESCRIPTION

The μPD78F9116B is a μPD789114A Subseries product of the 78K/0S Series.

The μPD78F9116B replaces the internal ROM of the μPD789111A,789112A and 789114A with flash memory, which enables the writing/erasing of a program while the device is mounted on the board.

A stricter quality assurance program (called special grade in NEC's grade classification) is applied to the μPD78F9116B(A), compared to the μPD78F9116B, which are classified as standard grade.

Because flash memory allows the program to be written and erased electrically with the device mounted on the board, this product is ideal for the evaluation stages of system development, small-scale production, and rapid development of new products.

**Detailed function descriptions are provided in the following user's manuals. Be sure to read them before designing.**

**μPD789104A, 789114A, 789124A, 789134A Subseries User's Manual: U14643E**
**78K/0S Series User's Manual Instruction: U11047E**

### FEATURES

- Pin-compatible with mask ROM version (excluding $V_{PP}$ pin)
- Flash memory: 16 KB
- Internal high-speed RAM: 256 bytes
- On-chip multiplier: 8 bits × 8 bits = 16 bits
- Minimum instruction execution time can be changed from high-speed (0.2 μs) to low-speed (0.8 μs) (@ 10.0 MHz operation with system clock, $V_{DD}$ = 4.5 to 5.5 V)
- I/O ports: 20
- Serial interface: 1 channel: Switchable between 3-wire serial I/O and UART modes
- 10-bit resolution A/D converter: 4 channels
- Timers: 3 channels
  - 16-bit timer: 1 channel
  - 8-bit timer/event counter: 1 channel
  - Watchdog timer: 1 channel
- Power supply voltage: $V_{DD}$ = 1.8 to 5.5 V

### APPLICATIONS

Cleaners, washing machines, refrigerators and battery-charger



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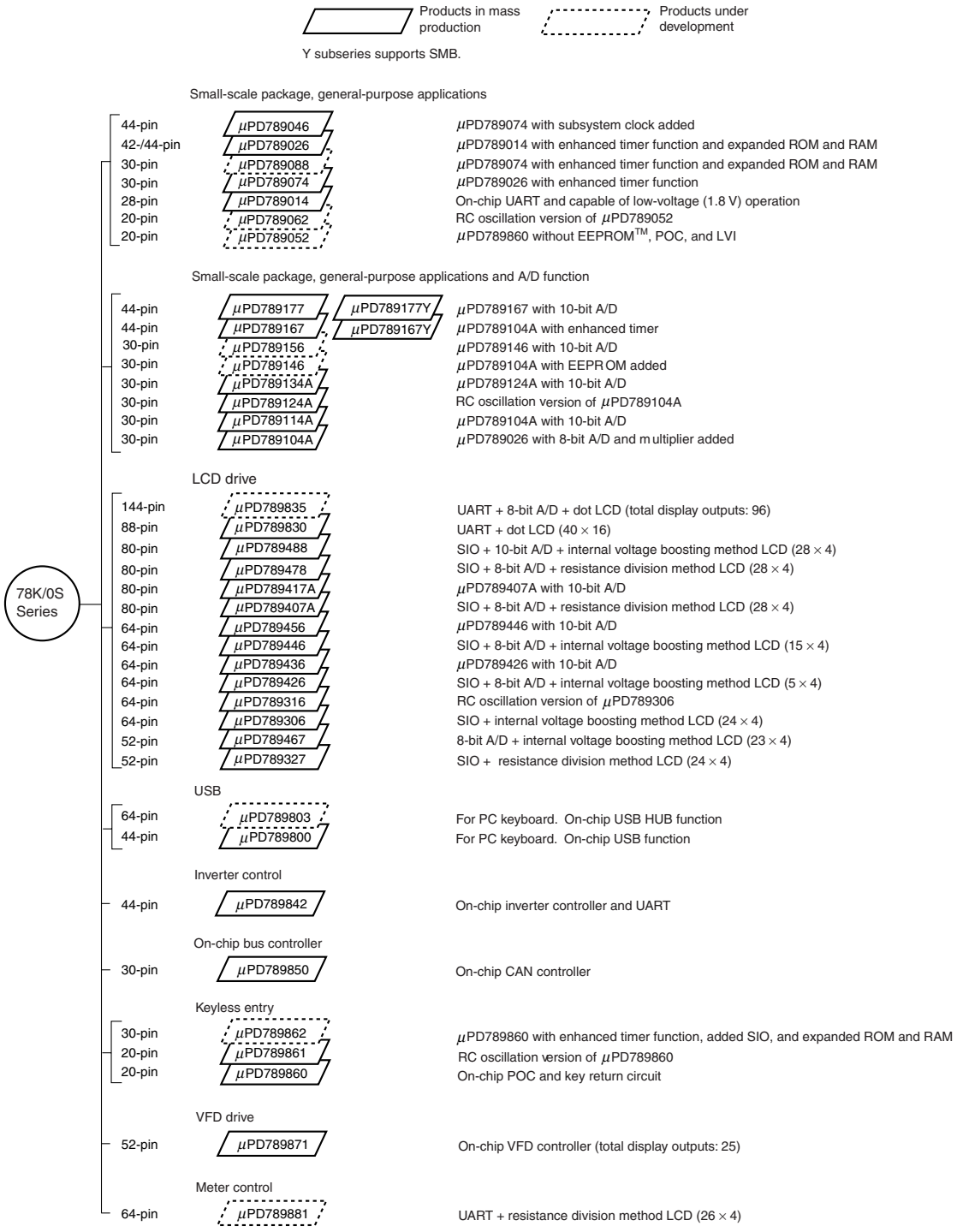
## ORDERING INFORMATION

| Part number | Package | Quality grade |
|---|---|---|
| μPD78F9116BMC-5A4 | 30-pin plastic SSOP (7.62 mm (300)) | Standard |
| μPD78F9116BMC(A)-5A4 | 30-pin plastic SSOP (7.62 mm (300)) | Special |

Please refer to "Quality Grades on NEC Semiconductor Devices" (Document No. C11531E) published by NEC Corporation to know the specification of quality grade on the devices and its recommended applications.

## 78K/0S SERIES LINEUP

The products in the 78K/0S Series are listed below. The names enclosed in boxes are subseries names.




**Remark** VFD (Vacuum Fluorescent Display) is referred to as FIP™ (Fluorescent Indicator Panel) in some documents, but the functions of the two are the same.

The major functional differences among the subseries are listed below.

**Series for General-Purpose and LCD Drive**

| Subseries Name \ Function | | ROM Capacity (Bytes) | Timer | | | | 8-Bit A/D | 10-Bit A/D | Serial Interface | I/O | $V_{DD}$ MIN. Value | Remarks |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | 8-Bit | 16-Bit | Watch | WDT | | | | | | |
| Small-scale package, general-purpose applications | μPD789046 | 16 K | 1 ch | 1 ch | 1 ch | 1 ch | – | – | 1 ch (UART: 1ch) | 34 | 1.8 V | – |
| | μPD789026 | 4 K to 16 K | | | – | | | | | | | |
| | μPD789088 | 16 K to 32 K | 3 ch | | | | | | | 24 | | |
| | μPD789074 | 2 K to 8 K | 1 ch | | | | | | | | | |
| | μPD789014 | 2 K to 4 K | 2 ch | – | | | | | | 22 | | |
| | μPD789062 | 4 K | | | | | | | – | 14 | | RC-oscillation version |
| | μPD789052 | | | | | | | | | | | – |
| Small-scale package, general-purpose applications + A/D converter | μPD789177 | 16 K to 24 K | 3 ch | 1 ch | 1 ch | 1ch | – | 8 ch | 1 ch (UART: 1ch) | 31 | 1.8 V | – |
| | μPD789167 | | | | | | 8 ch | – | | | | |
| | μPD789156 | 8 K to 16 K | 1 ch | | – | | – | 4 ch | | 20 | | On-chip EEPROM |
| | μPD789146 | | | | | | 4 ch | – | | | | |
| | μPD789134A | 2 K to 8 K | | | | | – | 4 ch | | | | RC-oscillation version |
| | μPD789124A | | | | | | 4 ch | – | | | | |
| | μPD789114A | | | | | | – | 4 ch | | | | – |
| | μPD789104A | | | | | | 4 ch | – | | | | |
| LCD drive | μPD789835 | 24 K to 60 K | 6 ch | – | 1 ch | 1 ch | 3 ch | – | 1 ch (UART: 1ch) | 37 | 1.8 V[Note] | Dot LCD supported |
| | μPD789830 | 24 K | 1 ch | 1 ch | | | – | | | 30 | 2.7 V | |
| | μPD789488 | 32 K | 3 ch | | | | | 8 ch | 2 ch (UART: 1ch) | 45 | 1.8 V | – |
| | μPD789478 | 24 K to 32 K | | | | | 8 ch | – | | | | |
| | μPD789417A | 12 K to 24 K | | | | | – | 7 ch | 1 ch (UART: 1ch) | 43 | | |
| | μPD789407A | | | | | | 7 ch | – | | | | |
| | μPD789456 | 12 K to 16 K | 2 ch | | | | – | 6 ch | | 30 | | |
| | μPD789446 | | | | | | 6 ch | – | | | | |
| | μPD789436 | | | | | | – | 6 ch | | 40 | | |
| | μPD789426 | | | | | | 6 ch | – | | | | |
| | μPD789316 | 8 K to 16 K | | | | | – | | 2 ch (UART: 1ch) | 23 | | RC-oscillation version |
| | μPD789306 | | | | | | | | | | | – |
| | μPD789467 | 4 K to 24 K | | – | | | 1 ch | | – | 18 | | |
| | μPD789327 | | | | | | – | | 1 ch | 21 | | |

**Note** Flash memory version: 3.0 V

**Series for ASSP**

| Subseries Name \ Function | | ROM Capacity (Bytes) | Timer | | | | 8-Bit A/D | 10-Bit A/D | Serial Interface | I/O | $V_{DD}$ MIN.Value | Remarks |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | 8-Bit | 16-Bit | Watch | WDT | | | | | | |
| USB | μPD789803 | 8 K to 16 K | 2 ch | – | – | 1 ch | – | – | 2 ch (USB: 1 ch) | 41 | 3.6 V | – |
| | μPD789800 | 8 K | | | | | | | | 31 | 4.0 V | |
| Inverter control | μPD789842 | 8 K to 16 K | 3 ch | **Note 1** | 1 ch | 1 ch | 8 ch | – | 1 ch (UART: 1 ch) | 30 | 4.0 V | – |
| On-chip bus controller | μPD789850 | 16 K | 1 ch | 1 ch | – | 1 ch | 4 ch | – | 2 ch (UART: 1 ch) | 18 | 4.0 V | – |
| Keyless entry | μPD789861 | 4 K | 2 ch | – | – | 1 ch | – | – | – | 14 | 1.8 V | RC-oscillation version, on-chip EEPROM |
| | μPD789860 | | | | | | | | | | | On-chip EEPROM |
| | μPD789862 | 16 K | 1 ch | 2 ch | | | | | 1 ch (UART: 1 ch) | 22 | | |
| VFD drive | μPD789871 | 4 K to 8 K | 3 ch | – | 1 ch | 1 ch | – | – | 1 ch | 33 | 2.7 V | – |
| Meter control | μPD789881 | 16 K | 2 ch | 1 ch | – | 1 ch | – | – | 1 ch (UART: 1 ch) | 28 | 2.7 V[Note 2] | – |

**Notes 1.** 10-bit timer: 1 channel

**2.** Flash memory version: 3.0 V

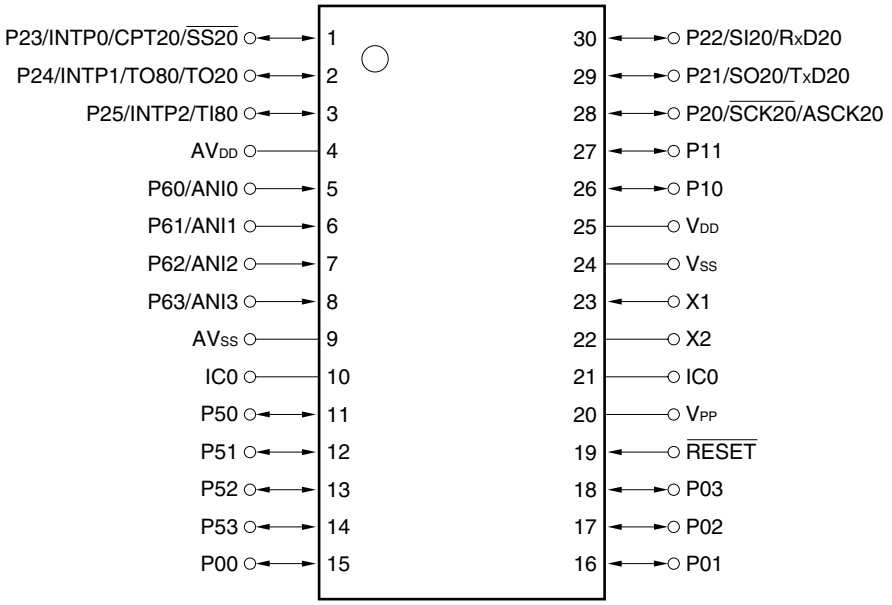
## OVERVIEW OF FUNCTIONS

| Item | | function |
|---|---|---|
| Internal memory | Flash memory | 16 KB |
| | High-speed RAM | 256 bytes |
| Minimum instruction execution time | | 0.2/0.8 μs (@ 10.0 MHz operation with system clock, $V_{DD}$ = 4.5 to 5.5 V) |
| General-purpose registers | | 8 bits × 8 registers |
| Instruction set | | • 16-bit operations<br>• Bit manipulations (set, reset, and test) |
| Multiplier | | 8 bits × 8 bits = 16 bits |
| I/O ports | | Total: 20<br>• CMOS input: 4<br>• CMOS I/O: 12<br>• N-ch open-drain (12 V withstand voltage): 4 |
| A/D converters | | 10-bit resolution × 4 channels |
| Serial interface | | Switchable between 3-wire serial I/O and UART modes |
| Timer | | • 16-bit timer: 1 channel<br>• 8-bit timer/event counter: 1 channel<br>• Watchdog timer: 1 channel |
| Timer output | | 1 output (16-bit/8-bit timer alternate function) |
| Vectored interrupt sources | Maskable | Internal: 6, External: 3 |
| | Non-maskable | Internal: 1 |
| Power supply voltage | | $V_{DD}$ = 1.8 to 5.5 V |
| Operating ambient temperature | | $T_A$ = –40 to +85°C |
| Package | | 30-pin plastic SSOP (7.62 mm (300)) |

CONTENTS

## 1. PIN CONFIGURATION (TOP VIEW)

- 30-pin plastic SSOP (7.62 mm (300))
  μPD78F9116BMC-5A4
  μPD78F9116BMC(A)-5A4




**Cautions 1. Connect the IC0 (Internally Connected) pin directly to $V_{SS}$.**

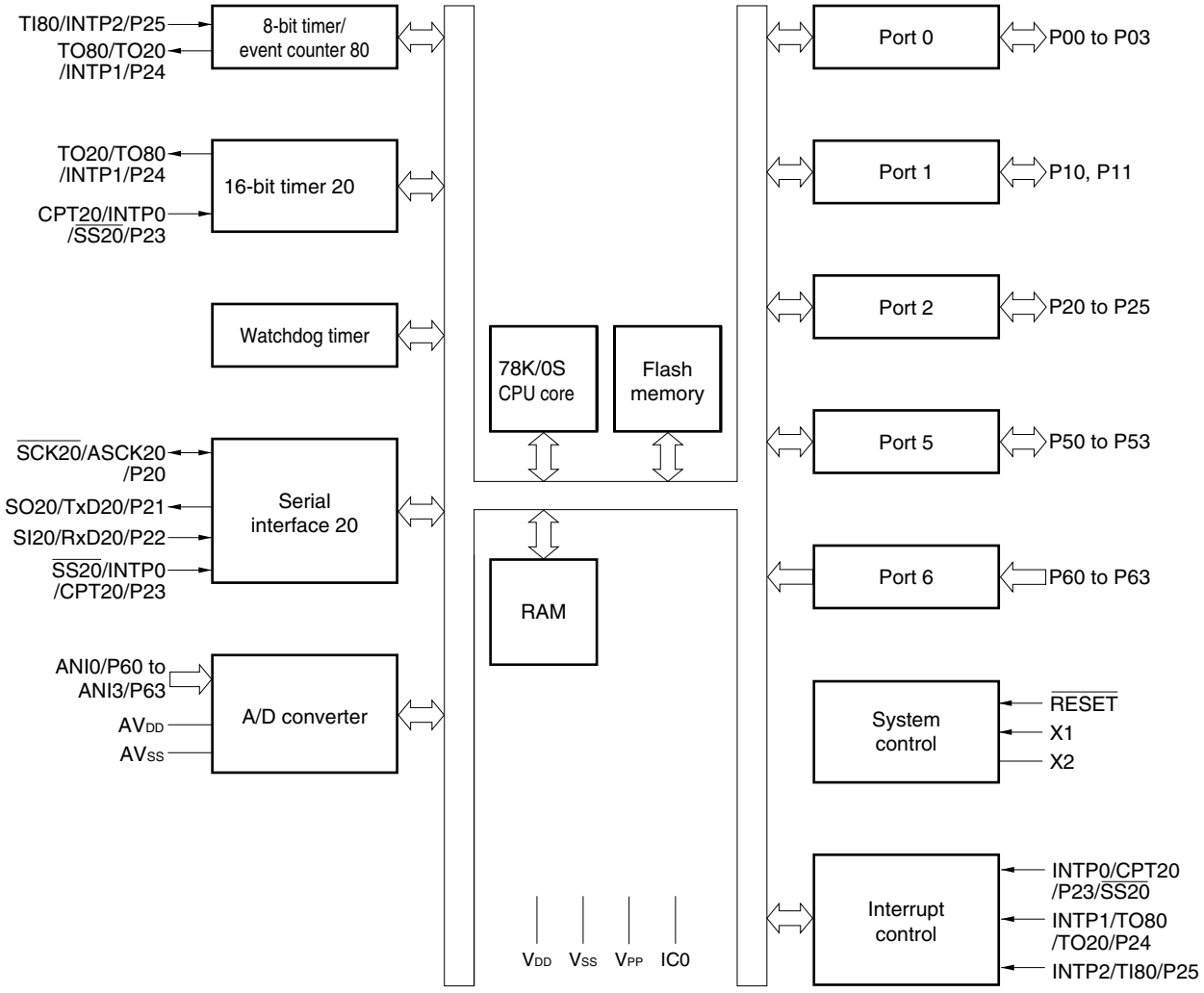
**2. Connect the $V_{PP}$ pin directly to $V_{SS}$ in normal operation mode.**

**3. Connect the $AV_{DD}$ pin to $V_{DD}$.**

**4. Connect the $AV_{SS}$ pin to $V_{SS}$.**

| | | | |
|---|---|---|---|
| ANI0 to ANI3: | Analog input | $\overline{RESET}$: | Reset |
| ASCK20: | Asynchronous serial input | RxD20: | Receive data |
| $AV_{DD}$: | Analog power supply | $\overline{SCK20}$: | Serial clock input/output |
| $AV_{SS}$: | Analog ground | SI20: | Serial data input |
| CPT20: | Capture trigger input | SO20: | Serial data output |
| IC0: | Internally connected | $\overline{SS20}$: | Chip select input |
| INTP0 to INTP2: | Interrupt from peripherals | TI80: | Timer input |
| P00 to P03: | Port0 | TO20, TO80: | Timer output |
| P10, P11: | Port1 | TxD20: | Transmit data |
| P20 to P25: | Port2 | $V_{DD}$: | Power supply |
| P50 to P53: | Port5 | $V_{PP}$: | Programming power supply |
| P60 to P63: | Port6 | $V_{SS}$: | Ground |
| | | X1, X2: | Crystal 1, 2 |

## 2. BLOCK DIAGRAM



## 3. DIFFERENCES BETWEEN μPD78F9116B, 78F9116B(A), AND MASK ROM VERSIONS

The μPD78F9116B and 78F9116B(A) are products in which flash memory is substituted for the internal ROM of the mask ROM version. The differences between the μPD78F9116B, 78F9116B(A), and the mask ROM versions are shown in Table 3-1.

**Table 3-1. Differences Between μPD78F9116B, 78F9116B(A), and Mask ROM Versions**

| Item | | Flash Memory Version | Mask ROM Version | | |
|---|---|---|---|---|---|
| | | μPD78F9116B<br>μPD78F9116B(A) | μPD789111A<br>μPD789111A(A) | μPD789112A<br>μPD789112A(A) | μPD789114A<br>μPD789114A(A) |
| Internal memory | ROM | 16 KB (Flash memory) | 2 KB | 4 KB | 8 KB |
| | High-speed RAM | 256 bytes | | | |
| Pull-up resistor | | 12 (software control only) | 16 (software control: 12, mask option specification: 4) | | |
| $V_{PP}$ pin | | Provided | Not provided | | |
| Electric characteristics | | See the relevant data sheet | | | |

**Caution There are differences in noise immunity and noise radiation between the flash memory and mask ROM versions. When pre-producing an application set with the flash memory version and then mass-producing it with the mask ROM version, be sure to conduct sufficient evaluations for the commercial samples (not engineering samples) of the mask ROM version.**

# 4. PIN FUNCTIONS

## 4.1 Port Pins

| Pin Name | I/O | Function | After Reset | Alternate Function |
|---|---|---|---|---|
| P00 to P03 | I/O | Port 0<br>4-bit I/O port<br>Input/output can be specified in 1-bit units<br>When used as an input port, connection of an on-chip pull-up resistor can be specified by software. | Input | – |
| P10, P11 | I/O | Port 1<br>2-bit I/O port<br>Input/output can be specified in 1-bit units<br>When used as an input port, an connection of on-chip pull-up resistor can be specified by software. | Input | – |
| P20 | I/O | Port 2<br>6-bit I/O port<br>Input/output can be specified in 1-bit units<br>When used as an input port, an connection of on-chip pull-up resistor can be specified by software. | Input | $\overline{\text{SCK20}}$/ASCK20 |
| P21 | | | | SO20/TxD20 |
| P22 | | | | SI20/RxD20 |
| P23 | | | | INTP0/CPT20<br>/$\overline{\text{SS20}}$ |
| P24 | | | | INTP1/TO80/TO20 |
| P25 | | | | INTP2/TI80 |
| P50 to P53 | I/O | Port 5<br>4-bit N-ch open-drain input/output port Input/output can be specified in 1-bit units. | Input | – |
| P60 to P63 | Input | Port 6<br>4-bit input-only port | Input | ANI0 to ANI3 |

### 4.2 Non-Port Pins

| Pin Name | I/O | Function | After Reset | Alternate Function |
|---|---|---|---|---|
| INTP0 | Input | External interrupt request input for which the valid edge (rising edge, falling edge, or both rising and falling edges) can be specified | Input | P23/CPT20/$\overline{SS20}$ |
| INTP1 | | | | P24/TO80/TO20 |
| INTP2 | | | | P25/TI80 |
| SI20 | Input | Serial interface serial data input | Input | P22/RxD20 |
| SO20 | Output | Serial interface serial data output | Input | P21/TxD20 |
| $\overline{SCK20}$ | I/O | Serial interface serial clock input/output | Input | P20/ASCK20 |
| ASCK20 | Input | Serial clock input for asynchronous serial interface | Input | P20/$\overline{SCK20}$ |
| $\overline{SS20}$ | Input | Chip select input for serial interface | Input | P23/CPT20/INTP0 |
| RxD20 | Input | Serial data input for asynchronous serial interface | Input | P22/SI20 |
| TxD20 | Output | Serial data output for asynchronous serial interface | Input | P21/SO20 |
| TI80 | Input | External count clock input to 8-bit timer/event counter 80 | Input | P25/INTP2 |
| TO80 | Output | 8-bit timer/event counter 80 output | Input | P24/INTP1/TO20 |
| TO20 | Output | 16-bit timer 20 output | Input | P24/INTP1/TO80 |
| CPT20 | Input | Capture edge input | Input | P23/INTP0/$\overline{SS20}$ |
| ANI0 to ANI3 | Input | A/D converter analog input | Input | P60 to P63 |
| $AV_{DD}$ | - | A/D converter analog power supply | – | – |
| $AV_{SS}$ | - | A/D converter ground potential | – | – |
| X1 | Input | Connecting crystal resonator for main system clock oscillation | – | – |
| X2 | - | | – | – |
| $\overline{RESET}$ | Input | System reset input | Input | – |
| $V_{DD}$ | - | Positive power supply | – | – |
| $V_{SS}$ | - | Ground potential | – | – |
| $V_{PP}$ | - | Sets flash memory programming mode.<br>Applies high voltage when a program is written or verified. | – | – |
| IC0 | - | Internally connected. Connect directly to $V_{SS}$. | – | – |

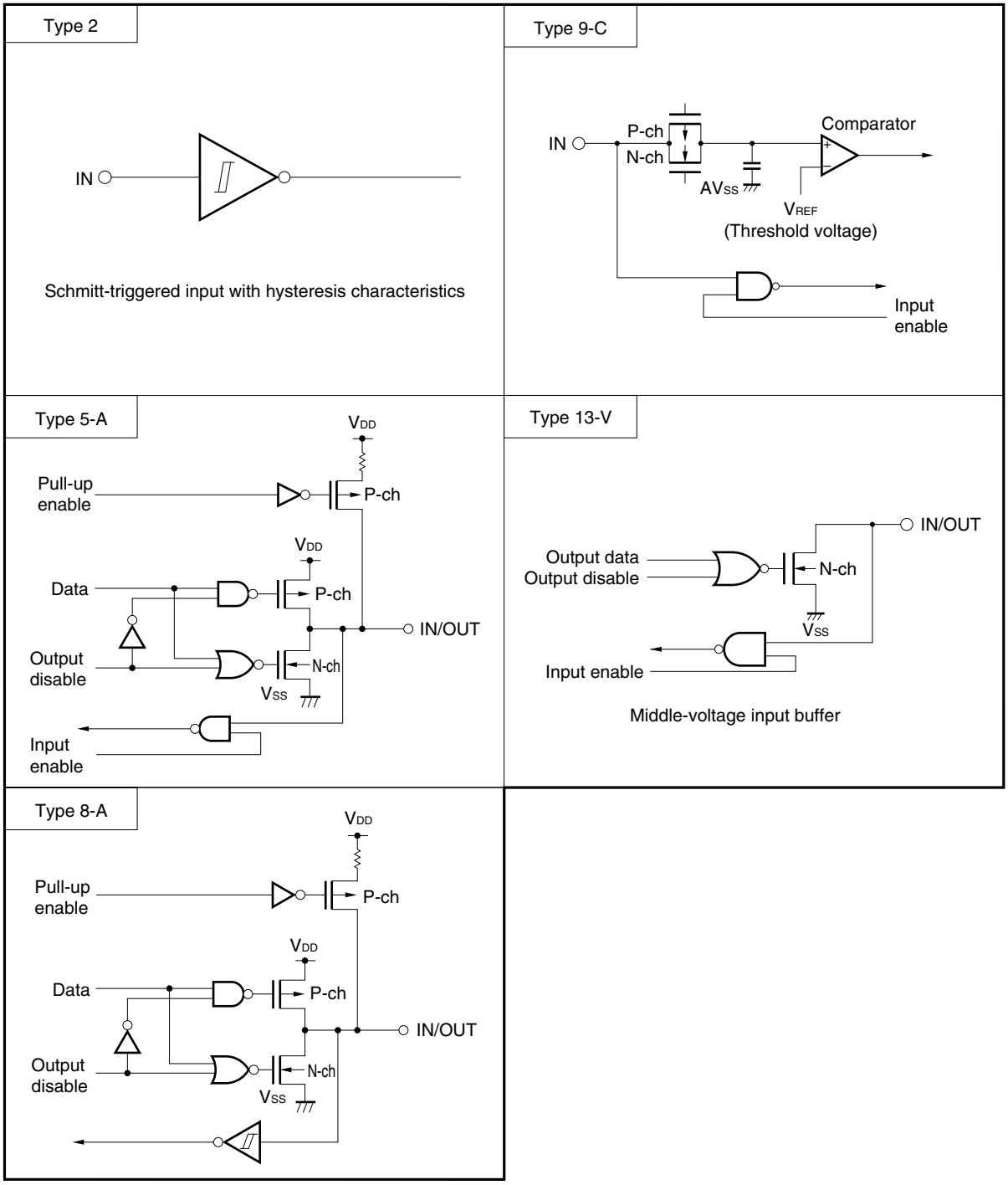
### 4.3 Pin I/O Circuits and Recommended Connection of Unused Pins

The input/output circuit type of each pin and recommended connection of unused pins are shown in Table 4-1. For the input/output circuit configuration of each type, refer to Figure 4-1.

**Table 4-1. Types of Pin Input/Output Circuits**

| Pin Name | Input/Output Circuit Type | I/O | Recommended Connection of Unused Pins |
|---|---|---|---|
| P00 to P03 | 5-A | I/O | Input: Independently connect to $V_{DD}$ or $V_{SS}$ via a resistor.<br>Output: Leave open |
| P10, P11 | | | |
| P20/$\overline{SCK20}$/ASCK20 | 8-A | | |
| P21/SO20/TxD20 | | | |
| P22/SI20/RxD20 | | | |
| P23/INTP0/CPT20/$\overline{SS20}$ | | | Input: Independently connect to $V_{SS}$ via a resistor.<br>Output: Leave open |
| P24/INTP1/TO80/TO20 | | | |
| P25/INTP2/TI80 | | | |
| P50 to P53 | 13-V | | Input: Independently connect to $V_{DD}$ via a resistor.<br>Output: Leave open |
| P60/ANI0 to P63/ANI3 | 9-C | Input | Connect directly to $V_{DD}$ or $V_{SS}$. |
| $AV_{DD}$ | – | – | Connect directly to $V_{DD}$. |
| $AV_{SS}$ | | | Connect directly to $V_{SS}$. |
| $\overline{RESET}$ | 2 | Input | – |
| IC0 | – | – | Connect directly to $V_{SS}$. |
| $V_{PP}$ | | | Connect a 10 kΩ pull-down resistor or connect directly to $V_{SS}$. |

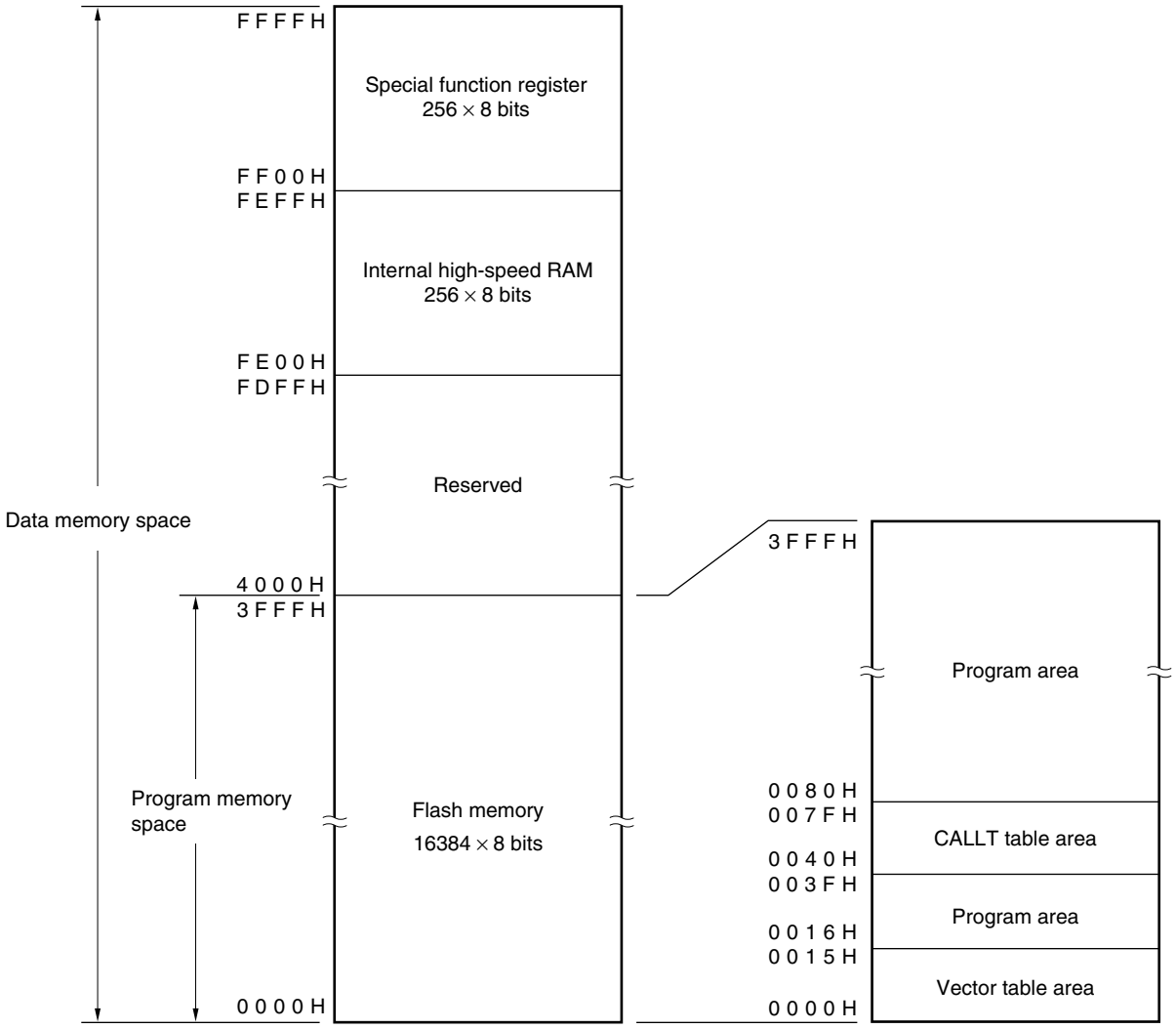
**Figure 4-1. Pin I/O Circuits**



## 5. MEMORY SPACE

Figure 5-1 shows the memory map of the μPD78F9116B and 78F9116B(A).

**Figure 5-1. Memory Map**



## 6. FLASH MEMORY CHARACTERISTICS

Flash memory programming is performed by connecting a dedicated flash programmer (Flashpro III (part no. FL-PR3, PG-FP3)/Flashpro IV[Note] (part no. FL-PR4, PG-FP4)) to the target system with the flash memory mounted on the target system (on-board). A flash memory writing adapter (program adapter), which is a target board used exclusively for programming, is also provided.

**Note** Under development

**Remark** FL-PR3, FL-PR4, and the program adapter are the products made by Naito Densei Machida Mfg. Co., Ltd. (TEL +81-45-475-4191).

Programming using flash memory has the following advantages.

- Software can be modified after the microcontroller is solder-mounted on the target system.
- Distinguishing software facilities low-quantity, varied model production
- Easy data adjustment when starting mass production

### 6.1 Programming Environment

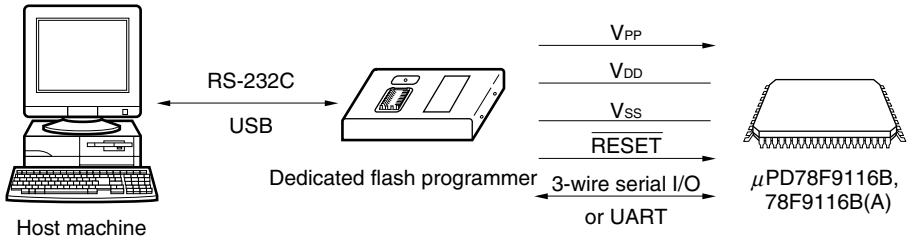
The following shows the environment required for μPD78F9116B and 78F9116B(A) flash memory programming.

When Flashpro III (part no. FL-PR3, PG-FP3) or Flashpro IV (Part no. FL-PR4, PG-FP4) is used as a dedicated flash programmer, a host machine is required to control the dedicated flash programmer. Communication between the host machine and flash programmer is performed via RS-232C/USB (Rev. 1.1).

For details, refer the manuals for Flashpro III/Flashpro IV.

**Remark** USB is supported by Flashpro IV only.

**Figure 6-1. Environment for Writing Program to Flash Memory**



## 6.2 Communication Mode

Use the communication mode shown in Table 6-1 to perform communication between the dedicated flash programmer and the μPD78F9116B or 78F9116B(A).

**Table 6-1. Communication Mode List**

| Communication Mode | TYPE Setting[Note 1] | | | | | Pins used | Number of $V_{PP}$ pulses |
|---|---|---|---|---|---|---|---|
| | COMM PORT | SIO clock | CPU clock | Flash clock | Multiple rate | | |
| 3-wire serial I/O (SIO3) | SIO ch-0 (3-wire, sync.) | 100 Hz to 1.25 MHz[Note 2] | Optional | 1 to 10 MHz[Note 2] | 1.0 | $\overline{SCK20}$/ASCK20/P20<br>SO20/TxD20/P21<br>SI20/RxD20/P22 | 0 |
| | SIO ch-1 (3-wire, sync.) | | | | | P00<br>P01<br>P02 | 1 |
| UART (UART0) | UART ch-0 | 4800 to 76800 bps[Note 2, 3] | Optional | 1 to 10 MHz[Note 2] | | TxD20/SO20/P21<br>RxD20/SI20/P22 | 8 |

**Notes 1.** Selection items for TYPE settings on the dedicated flash programmer (Flashpro III (part no. FL-PR3, PG-FP3)/Flashpro IV (Part no. FL-PR4, PG-FP4)).

**2.** The possible setting range differs depending on the voltage. For details, refer to **8. ELECTRICAL SPECIFICATIONS**.

**Caution Be sure to select a communication mode depending on the number of $V_{PP}$ pulses shown in Table 6-1.**

**Figure 6-2. Communication Mode Selection Format**

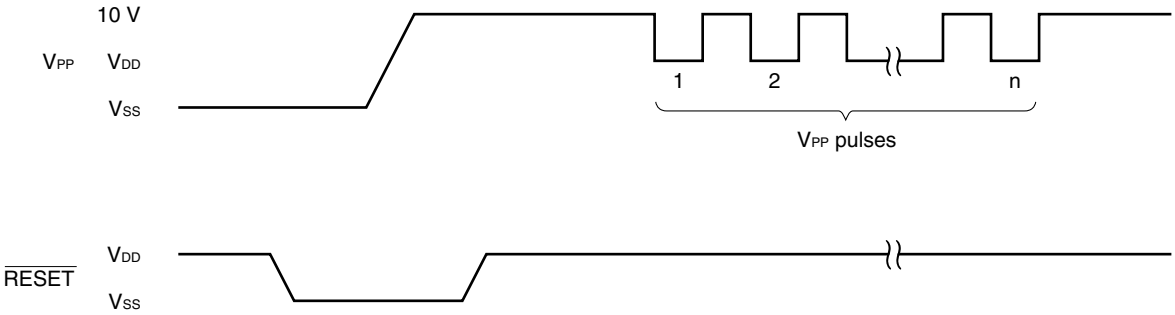
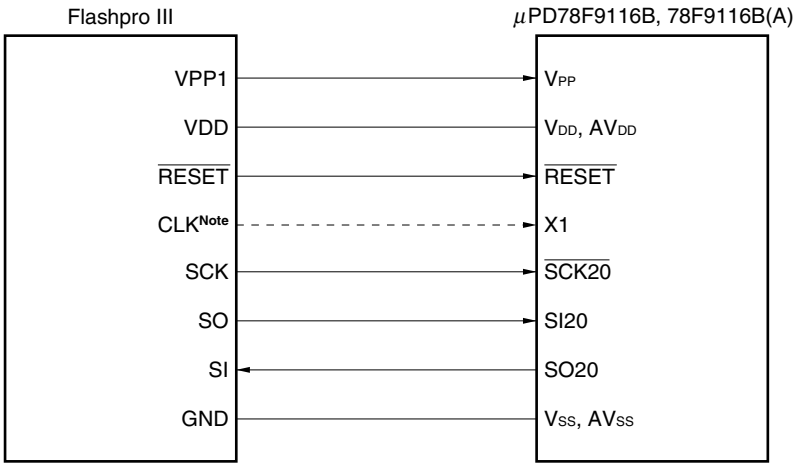
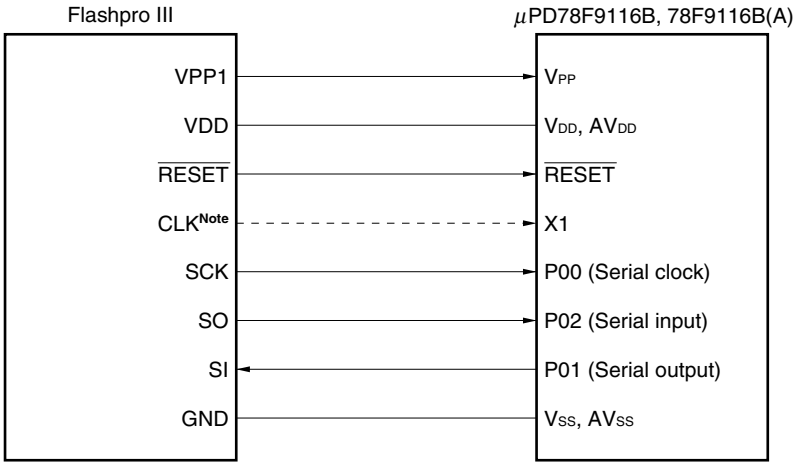


**Figure 6-3. Example of Connection with Dedicated Flash Programmer**

**(a) 3-Wired Serial I/O Mode (SIO ch-0)**



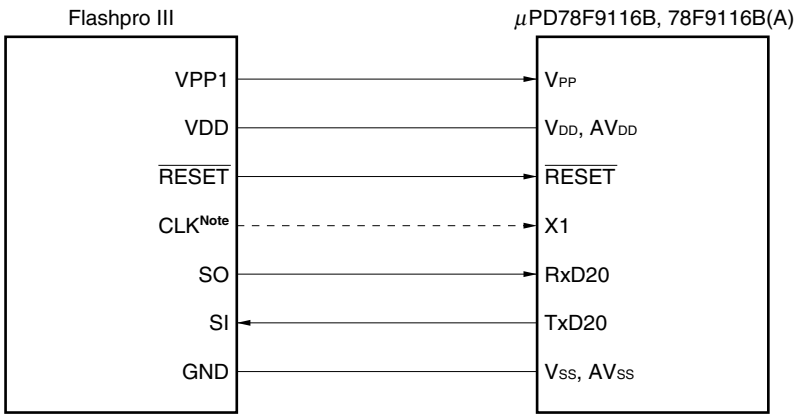

**(b) 3-Wired Serial I/O Mode (SIO ch-1)**




**Note** Connect this pin when the system clock is supplied by Flashpro III. When a resonator has already been connected to the X1 pin, the CLK pin does not need to be connected.

**Caution The $V_{DD}$ pin, if already connected to the power supply, must be connected to the VDD pin of the dedicated flash programmer. Before using the power supply connected to the $V_{DD}$ pin, supply voltage before starting programming.**

**(c) UART Mode**




**Note** Connect this pin when the system clock is supplied by Flashpro III. When a resonator has already been connected to the X1 pin, the CLK pin does not need to be connected.

**Caution The $V_{DD}$ pin, if already connected to the power supply, must be connected to the VDD pin of the dedicated flash programmer. Before using the power supply connected to the $V_{DD}$ pin, supply voltage before starting programming.**

If Flashpro III (part no. FL-PR3, PG-FP3)/Flashpro IV is used as a dedicated flash programmer, the following signals are generated for the μPD78F9116B and 78F9116B(A). For details, refer to the manual of Flashpro III/Flashpro IV.

**Table 6-2. Pin Connection List**

| Signal Name | I/O | Pin Function | Pin Name | 3-Wire Serial I/O | UART |
|---|---|---|---|---|---|
| VPP1 | Output | Write voltage | $V_{PP}$ | ◎ | ◎ |
| VPP2 | – | – | | × | × |
| VDD | I/O | $V_{DD}$ voltage generation/voltage monitoring | $V_{DD}$/$AV_{DD}$ | ◎Note | ◎Note |
| GND | – | Ground | $V_{SS}$/$AV_{SS}$ | ◎ | ◎ |
| CLK | Output | Clock output | X1 | ○ | ○ |
| RESET | Output | Reset signal | $\overline{RESET}$ | ◎ | ◎ |
| SI | Input | Reception signal | SO20/P01/TxD20 | ◎ | ◎ |
| SO | Output | Transmit signal | SI20/P02/RxD20 | ◎ | ◎ |
| SCK | Output | Transfer clock | SCK20/P00 | ◎ | × |
| HS | – | – | – | × | × |

**Note** $V_{DD}$ voltage must be supplied before programming is started.

**Remark** ◎: Pin must be connected.
○: If the signal is supplied on the target board, pin need not be connected.
×: Pin need not be connected.

### 6.3 On-Board Pin Processing

When performing programming on the target system, provide a connector on the target system to connect the dedicated flash programmer.

An on-board function that allows switching between normal operation mode and flash memory programming mode may be required in some cases.

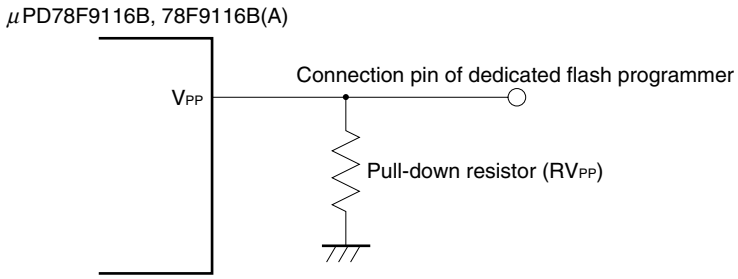
<$V_{PP}$ pin>

In normal operation mode, input 0 V to the $V_{PP}$ pin. In flash memory programming mode, a write voltage of 10.0 V (TYP.) is supplied to the $V_{PP}$ pin, so perform the following.

(1) Connect a pull-down resistor ($RV_{PP}$ = 10 kΩ) to the $V_{PP}$ pin.
(2) Use the jumper on the board to switch the $V_{PP}$ pin input to either the writer or directly to GND.

A $V_{PP}$ pin connection example is shown below.

**Figure 6-4. $V_{PP}$ Pin Connection Example**




<Serial interface pin>

The following shows the pins used by the serial interface.

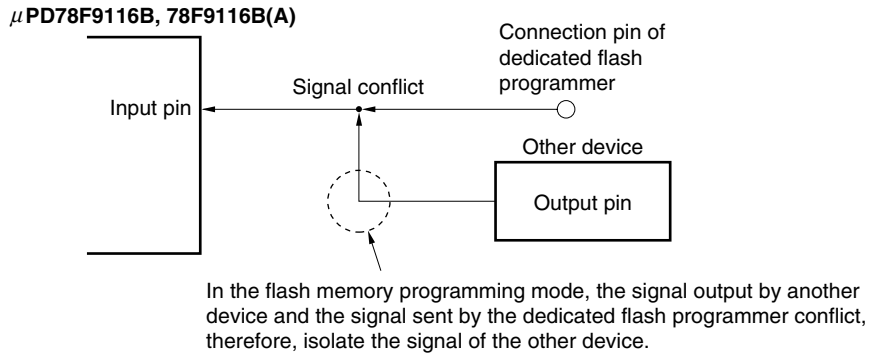
| Serial Interface | Pins Used |
|---|---|
| 3-wire serial I/O (SIO3) | $\overline{SCK20}$, SO20, SI20 |
| | P00, P01, P02 |
| UART | TxD20, RxD20 |

When connecting the dedicated flash programmer a serial interface pin that is connected to another device on-board, signal conflict or abnormal operation of the other devices may occur. Care must therefore be taken with such connections.

**(1) Signal conflict**

If the dedicated flash programmer (output) is connected to a serial interface pin (input) that is connected to another device (output), a signal conflict occurs. To prevent this, isolate the connection with the other device or set the other device to the output high impedance status.

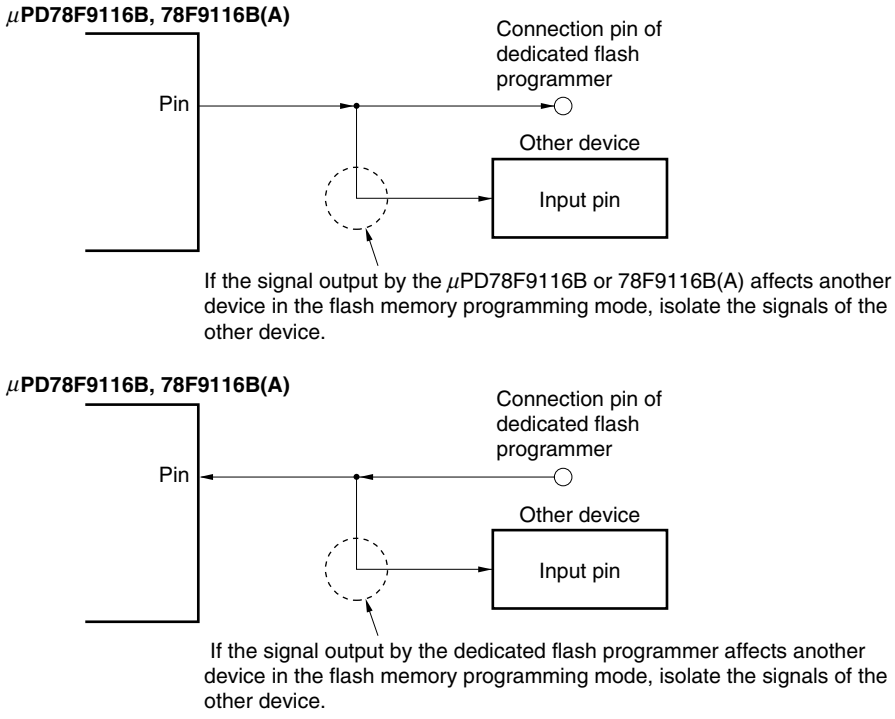
**Figure 6-5. Signal Conflict (Input Pin of Serial Interface)**




**(2) Abnormal operation of other device**

If the dedicated flash programmer (output or input) is connected to a serial interface pin (input or output) that is connected to another device (input), a signal is output to the device, and this may cause an abnormal operation. To prevent this abnormal operation, isolate the connection with the other device or set so that the input signals to the other device are ignored.

**Figure 6-6. Abnormal Operation of Other Device**

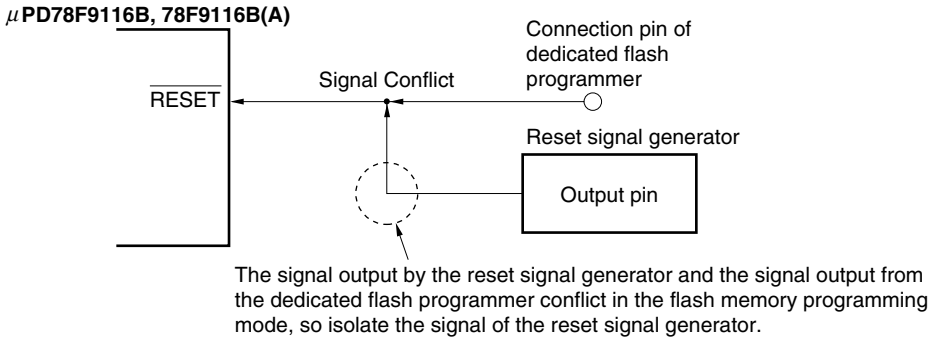


<$\overline{\text{RESET}}$ pin>

If the reset signal of the dedicated flash programmer is connected to the $\overline{\text{RESET}}$ pin connected to the reset signal generator on-board, a signal conflict occurs. To prevent this, isolate the connection with the reset signal generator.

If the reset signal is input from the user system in the flash memory programming mode, a normal programming operation cannot be performed. Therefore, do not input reset signals from other than the dedicated flash programmer.

**Figure 6-7. Signal Conflict ($\overline{\text{RESET}}$ Pin)**




<Port pins>

When the μPD78F9116B or 78F9116B(A) enters the flash memory programming mode, all the pins other than those that communicate in flash memory programming are in the same status as immediately after reset.

If the external device does not recognize initial statuses such as the output high impedance status, therefore, connect the external device to $V_{DD}$ or $V_{SS}$.

<Oscillation pins>

When using the on-board clock, connect X1 and X2 as required in the normal operation mode.

When using the clock output of the flash programmer, connect it directly to X1, disconnecting the main resonator on-board, and leave the X2 pin open.

<Power supply>

When using the power supply output of the flash programmer, connect the $V_{DD}$ and $V_{SS}$ pins to VDD and GND of the flash programmer, respectively.

When using the on-board power supply, connect it as required in the normal operation mode. Because the flash programmer monitors the voltage, however, VDD of the flash programmer must be connected.

For the other power pins ($AV_{DD}$ and $A_{SS}$), supply the same power supply as in the normal operation mode.

### 6.4 Connection When Using Flash Memory Writing Adapter

The following shows an example of the recommended connection when using the flash memory writing adapter.

**Figure 6-8. Example of Flash Memory Writing Adapter Connection When Using 3-Wire Serial I/O Mode (SIO-ch0)**

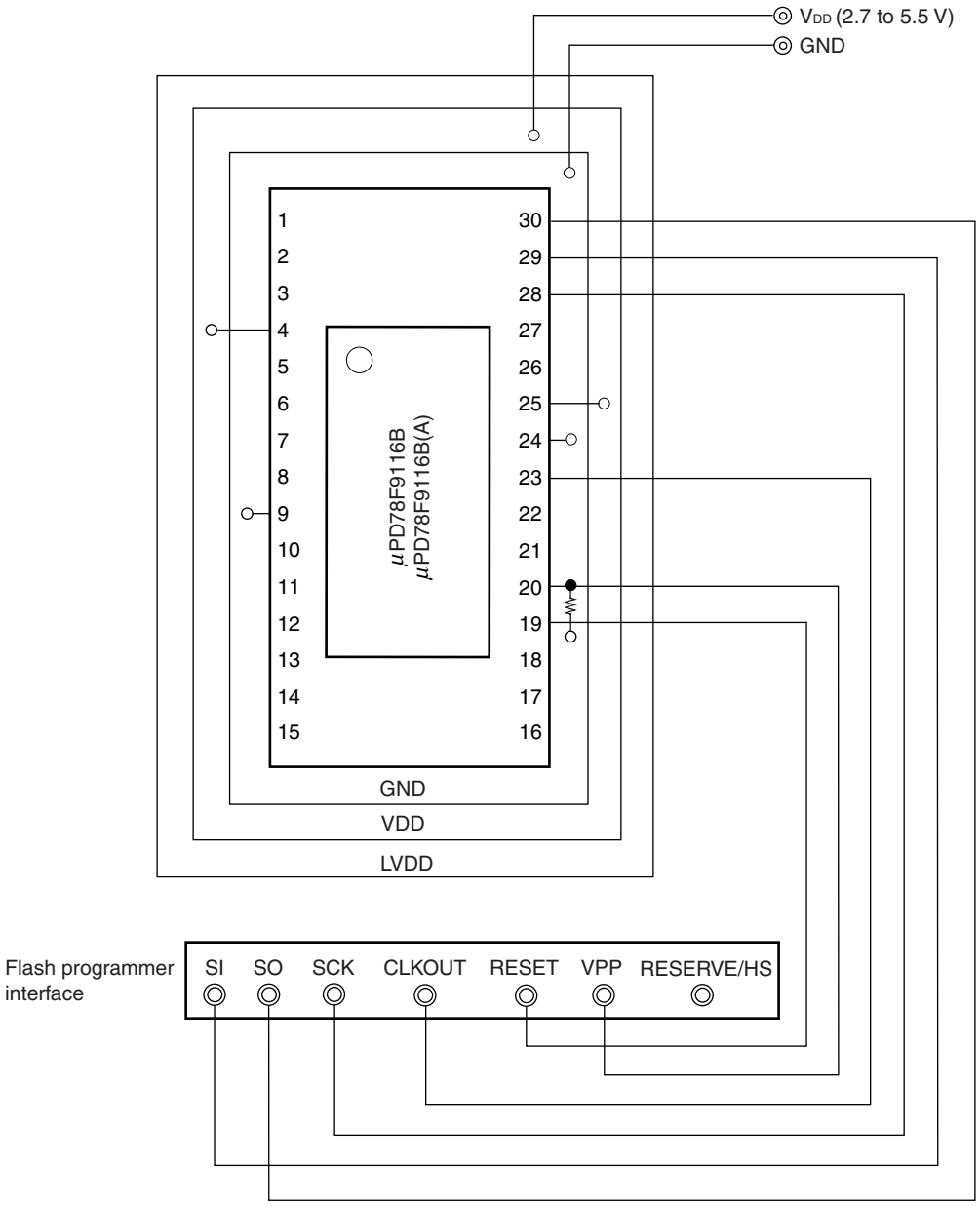


**Figure 6-9. Example of Flash Memory Writing Adapter Connection When Using 3-Wire Serial I/O Mode (SIO-ch1)**

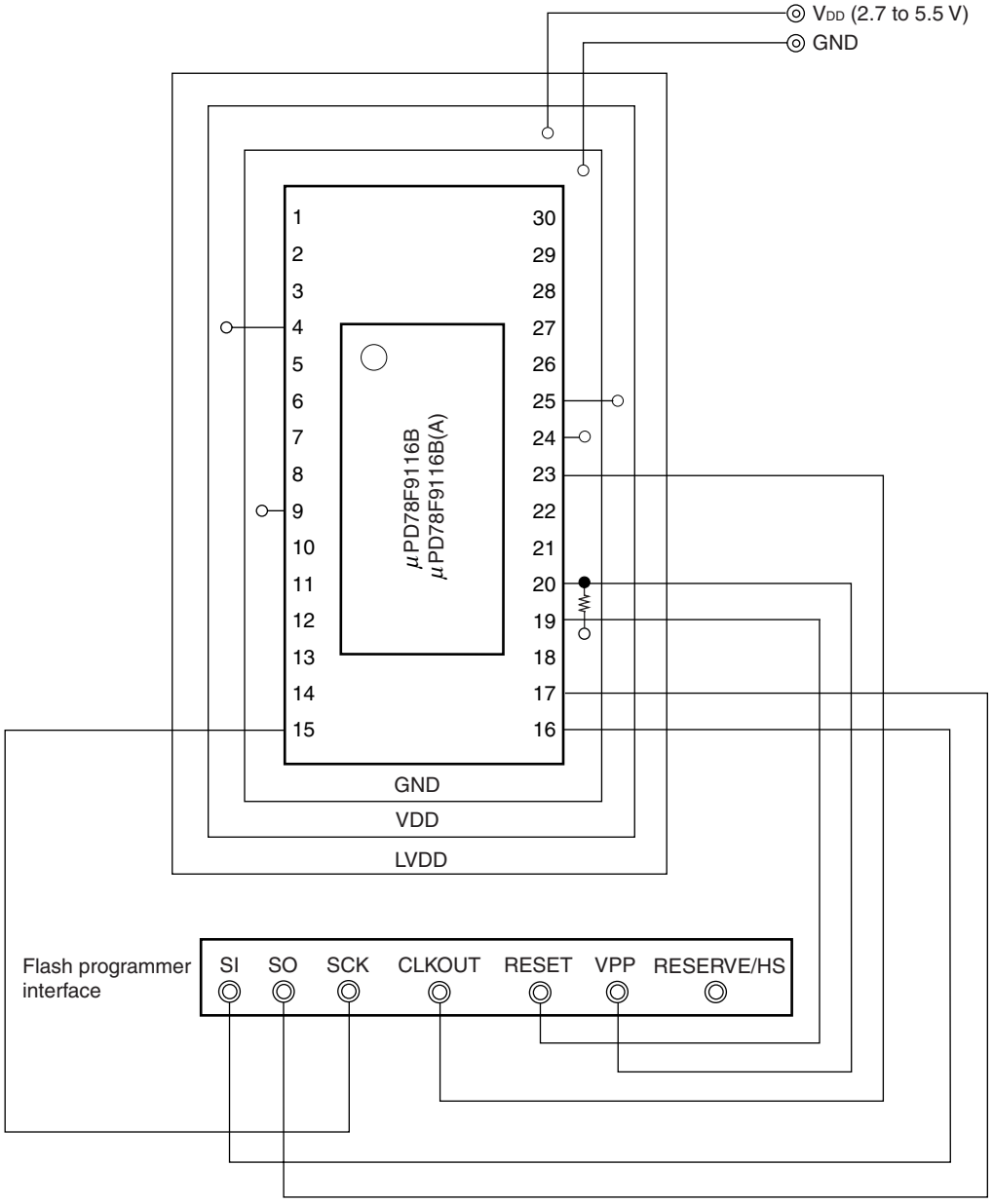
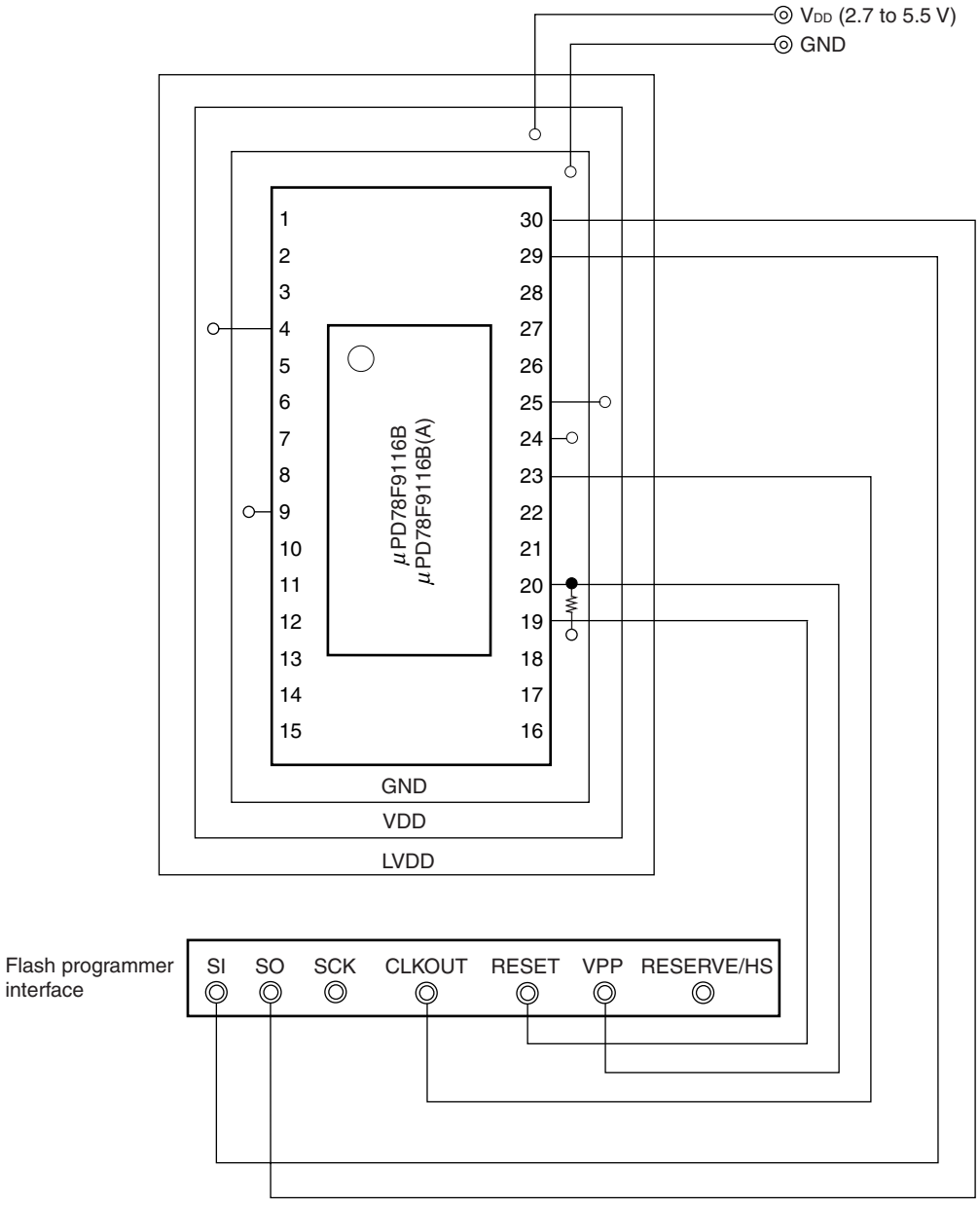


**Figure 6-10. Example of Flash Memory Writing Adapter Connection When Using UART Mode**



# 7. INSTRUCTION SET OVERVIEW

This section shows a list of the instruction set for the μPD78F9116B and 78F9116B(A).

## 7.1 Conventions

### 7.1.1 Operand identifiers and description methods

Operands are described in the "Operand" column of each instruction in accordance with the description method of the instruction operand identifier (refer to the assembler specifications for detail). When there are two or more description methods, select one of them. Alphabetic letters in capitals and the symbols, #, !, $, and [ ], are keywords and must be described as they are. Each symbol has the following meaning.

- #: Immediate data specification
- !: Absolute address specification
- $: Relative address specification
- [ ]: Indirect address specification

In the case of immediate data, describe an appropriate numeric value or a label. When using a label, be sure to describe the #,!, $, or [ ] symbols.

For operand register identifiers, r and rp, either function names (X, A, C, etc.) or absolute names (names in parentheses in the table below, R0, R1, R2, etc.) can be used for description.

**Table 7-1. Operand Identifiers and Description Methods**

| Identifier | Description Method |
|---|---|
| r<br>rp<br>sfr | X (R0), A (R1), C (R2), B (R3), E (R4), D (R5), L (R6), H (R7),<br>AX (RP0), BC (RP1), DE (RP2), HL (RP3)<br>Special function register symbol |
| saddr<br>saddrp | FE20H to FF1FH immediate data or label<br>FE20H to FF1FH immediate data or label (even address only) |
| addr16<br><br>addr5 | 0000H to FFFFH immediate data or label<br>(Only even addresses for 16-bit data transfer instructions)<br>0040H to 007FH immediate data or label (even address only) |
| word<br>byte<br>bit | 16-bit immediate data or label<br>8-bit immediate data or label<br>3-bit immediate data or label |

### 7.1.2 Descriptions of the operation field

A: A register; 8-bit accumulator
X: X register
B: B register
C: C register
D: D register
E: E register
H: H register
L: L register
AX: AX register pair; 16-bit accumulator
BC: BC register pair
DE: DE register pair
HL: HL register pair
PC: Program counter
SP: Stack pointer
PSW: Program status word
CY: Carry flag
AC: Auxiliary carry flag
Z: Zero flag
IE: Interrupt request enable flag
NMIS: Non-maskable interrupt servicing flag
( ): Memory contents indicated by address or register contents in parentheses
$X_H$, $X_L$: Higher 8 bits and lower 8 bits of 16-bit register
∧: Logical product (AND)
∨: Logical sum (OR)
∨: Exclusive OR
—— : Inverted data
addr16: 16-bit immediate data or label
jdisp8: Signed 8-bit data (displacement value)

### 7.1.3 Description of the flag operation field

(Blank): Not affected
0: Cleared to 0
1: Set to 1
×: Set/cleared according to the result
R: Previously saved value is restored

## 7.2 Operations

| Mnemonic | Operand | Byte | Clock | Operation | Flag |
|---|---|---|---|---|---|
| | | | | | Z AC CY |
| MOV | r, #byte | 3 | 6 | r ← byte | |
| | saddr , #byte | 3 | 6 | (addr) ← byte | |
| | sfr, #byte | 3 | 6 | sfr ← byte | |
| | A, r Note 1 | 2 | 4 | A ← r | |
| | r, A Note 1 | 2 | 4 | r ← A | |
| | A, saddr | 2 | 4 | A ← (saddr) | |
| | saddr, A | 2 | 4 | (saddr) ← A | |
| | A, sfr | 2 | 4 | A ← sfr | |
| | sfr, A | 2 | 4 | sfr ← A | |
| | A, !addr16 | 3 | 8 | A ← (addr16) | |
| | !addr16, A | 3 | 8 | (addr16) ← A | |
| | PSW, #byte | 3 | 6 | PSW ← byte | × × × |
| | A, PSW | 2 | 4 | A ← PSW | |
| | PSW, A | 2 | 4 | PSW ← A | × × × |
| | A, [DE] | 1 | 6 | A ← (DE) | |
| | [DE], A | 1 | 6 | (DE) ← A | |
| | A, [HL] | 1 | 6 | A ← (HL) | |
| | [HL], A | 1 | 6 | (HL) ← A | |
| | A, [HL + byte] | 2 | 6 | A ← (HL + byte) | |
| | [HL + byte], A | 2 | 6 | (HL + byte) ← A | |
| XCH | A, X | 1 | 4 | A ↔ X | |
| | A, r Note 2 | 2 | 6 | A ↔ r | |
| | A, saddr | 2 | 6 | A ↔ (saddr) | |
| | A, sfr | 2 | 6 | A ↔ sfr | |
| | A, [DE] | 1 | 8 | A ↔ (DE) | |
| | A, [HL] | 1 | 8 | A ↔ (HL) | |
| | A, [HL + byte] | 2 | 8 | A ↔ (HL + byte) | |
| MOVW | rp, #word | 3 | 6 | rp ← word | |
| | AX, saddrp | 2 | 6 | AX ← (saddrp) | |
| | saddrp, AX | 2 | 8 | (saddrp) ← AX | |
| | AX, rp Note 3 | 1 | 4 | AX ← rp | |
| | rp, AX Note 3 | 1 | 4 | rp ← AX | |
| XCHW | AX, rp Note 3 | 1 | 8 | AX ↔ rp | |

**Notes 1.** Except r = A

**2.** Except r = A or X

**3.** Only when rp = BC, DE, HL

**Remark** One instruction clock cycle is one cycle of the CPU clock ($f_{CPU}$), selected by the processor clock control register (PCC).

| Mnemonic | Operand | Byte | Clock | Operation | Flag |
|---|---|---|---|---|---|
| | | | | | Z AC CY |
| ADD | A, #byte | 2 | 4 | A, CY ← A + byte | × × × |
| | saddr, #byte | 3 | 6 | (saddr), CY ← (saddr) + byte | × × × |
| | A, r | 2 | 4 | A ,CY ← A + r | × × × |
| | A, saddr | 2 | 4 | A, CY ← A + (saddr) | × × × |
| | A, !addr16 | 3 | 8 | A, CY ← A + (addr16) | × × × |
| | A, [HL] | 1 | 6 | A, CY ← A + (HL) | × × × |
| | A, [HL + byte] | 2 | 6 | A, CY ← A + (HL + byte) | × × × |
| ADDC | A, #byte | 2 | 4 | A, CY ← A + byte + CY | × × × |
| | saddr, #byte | 3 | 6 | (saddr), CY ← (saddr) + byte + CY | × × × |
| | A, r | 2 | 4 | A, CY ← A + r + CY | × × × |
| | A, saddr | 2 | 4 | A, CY ← A + (saddr) + CY | × × × |
| | A, !addr16 | 3 | 8 | A, CY ← A + (addr16) + CY | × × × |
| | A, [HL] | 1 | 6 | A, CY ← A + (HL) + CY | × × × |
| | A, [HL + byte] | 2 | 6 | A, CY ← A + (HL + byte) + CY | × × × |
| SUB | A, #byte | 2 | 4 | A, CY ← A – byte | × × × |
| | saddr, #byte | 3 | 6 | (saddr), CY ← (saddr) – byte | × × × |
| | A, r | 2 | 4 | A, CY ← A – r | × × × |
| | A, saddr | 2 | 4 | A, CY ← A – (saddr) | × × × |
| | A, !addr16 | 3 | 8 | A, CY ← A – (addr16) | × × × |
| | A, [HL] | 1 | 6 | A, CY ← A – (HL) | × × × |
| | A, [HL + byte] | 2 | 6 | A, CY ← A – (HL + byte) | × × × |
| SUBC | A, #byte | 2 | 4 | A, CY ← A – byte – CY | × × × |
| | saddr, #byte | 3 | 6 | (saddr), CY ← (saddr) – byte – CY | × × × |
| | A, r | 2 | 4 | A, CY ← A – r – CY | × × × |
| | A, saddr | 2 | 4 | A, CY ← A – (saddr) – CY | × × × |
| | A, !addr16 | 3 | 8 | A, CY ← A – (addr16) – CY | × × × |
| | A, [HL] | 1 | 6 | A, CY ← A – (HL) – CY | × × × |
| | A, [HL + byte] | 2 | 6 | A, CY ← A – (HL + byte) – CY | × × × |
| AND | A, #byte | 2 | 4 | A ← A ∧ byte | × |
| | saddr, #byte | 3 | 6 | (saddr) ← (saddr) ∧ byte | × |
| | A, r | 2 | 4 | A ← A ∧ r | × |
| | A, saddr | 2 | 4 | A ← A ∧ (saddr) | × |
| | A, !addr16 | 3 | 8 | A ← A ∧ (addr16) | × |
| | A, [HL] | 1 | 6 | A ← A ∧ (HL) | × |
| | A, [HL + byte] | 2 | 6 | A ← A ∧ (HL + byte) | × |

**Remark** One instruction clock cycle is one cycle of the CPU clock ($f_{CPU}$), selected by the processor clock control register (PCC).

| Mnemonic | Operand | Byte | Clock | Operation | Flag |
|---|---|---|---|---|---|
| | | | | | Z AC CY |
| OR | A, #byte | 2 | 4 | A ← A ∨ byte | × |
| | saddr, #byte | 3 | 6 | (saddr) ← (saddr) ∨ byte | × |
| | A, r | 2 | 4 | A ← A ∨ r | × |
| | A, saddr | 2 | 4 | A ← A ∨ (saddr) | × |
| | A, !addr16 | 3 | 8 | A ← A ∨ (addr16) | × |
| | A, [HL] | 1 | 6 | A ← A ∨ (HL) | × |
| | A, [HL + byte] | 2 | 6 | A ← A ∨ (HL + byte) | × |
| XOR | A, #byte | 2 | 4 | A ← A ▽ byte | × |
| | saddr, #byte | 3 | 6 | (saddr) ← (saddr) ▽ byte | × |
| | A, r | 2 | 4 | A ← A ▽ r | × |
| | A, saddr | 2 | 4 | A ← A ▽ (saddr) | × |
| | A, !addr16 | 3 | 8 | A ← A ▽ (addr16) | × |
| | A, [HL] | 1 | 6 | A ← A ▽ (HL) | × |
| | A, [HL + byte] | 2 | 6 | A ← A ▽ (HL + byte) | × |
| CMP | A, #byte | 2 | 4 | A – byte | × × × |
| | saddr, #byte | 3 | 6 | (saddr) – byte | × × × |
| | A, r | 2 | 4 | A – r | × × × |
| | A, saddr | 2 | 4 | A – (saddr) | × × × |
| | A, !addr16 | 3 | 8 | A – (addr16) | × × × |
| | A, [HL] | 1 | 6 | A – (HL) | × × × |
| | A, [HL + byte] | 2 | 6 | A – (HL + byte) | × × × |
| ADDW | AX, #word | 3 | 6 | AX, CY ← AX + word | × × × |
| SUBW | AX, #word | 3 | 6 | AX, CY ← AX – word | × × × |
| CMPW | AX, #word | 3 | 6 | AX – word | × × × |
| INC | r | 2 | 4 | r ← r + 1 | × × |
| | saddr | 2 | 4 | (saddr) ← (saddr) + 1 | × × |
| DEC | r | 2 | 4 | r ← r – 1 | × × |
| | saddr | 2 | 4 | (saddr) ← (saddr) – 1 | × × |
| INCW | rp | 1 | 4 | rp ← rp + 1 | |
| DECW | rp | 1 | 4 | rp ← rp – 1 | |
| ROR | A, 1 | 1 | 2 | (CY, $A_7$ ← $A_0$, $A_{m-1}$ ← $A_m$) × 1 | × |
| ROL | A, 1 | 1 | 2 | (CY, $A_0$ ← $A_7$, $A_{m+1}$ ← $A_m$) × 1 | × |
| RORC | A, 1 | 1 | 2 | (CY ← $A_0$, $A_7$ ← CY, $A_{m-1}$ ← $A_m$) × 1 | × |
| ROLC | A, 1 | 1 | 2 | (CY ← $A_7$, $A_0$ ← CY, $A_{m+1}$ ← $A_m$) × 1 | × |

**Remark** One instruction clock cycle is one cycle of the CPU clock ($f_{CPU}$), selected by the processor clock control register (PCC).

| Mnemonic | Operand | Byte | Clock | Operation | Flag |
|---|---|---|---|---|---|
| | | | | | Z AC CY |
| SET1 | saddr. bit | 3 | 6 | (saddr. bit) ← 1 | |
| | sfr. bit | 3 | 6 | sfr. bit ← 1 | |
| | A. bit | 2 | 4 | A. bit ← 1 | |
| | PSW. bit | 3 | 6 | PSW. bit ← 1 | × × × |
| | [HL]. bit | 2 | 10 | (HL) . bit ← 1 | |
| CLR1 | saddr. bit | 3 | 6 | (saddr. bit) ← 0 | |
| | sfr. bit | 3 | 6 | sfr. bit ← 0 | |
| | A. bit | 2 | 4 | A. bit ← 0 | |
| | PSW. bit | 3 | 6 | PSW. bit ← 0 | × × × |
| | [HL]. bit | 2 | 10 | (HL) . bit ← 0 | |
| SET1 | CY | 1 | 2 | CY ← 1 | 1 |
| CLR1 | CY | 1 | 2 | CY ← 0 | 0 |
| NOT1 | CY | 1 | 2 | CY ← $\overline{CY}$ | × |
| CALL | !addr16 | 3 | 6 | (SP – 1) ← (PC + 3)$_H$,(SP – 2) ← (PC + 3)$_L$,<br>PC ← addr16, SP ← SP – 2 | |
| CALLT | [addr5] | 1 | 8 | (SP – 1) ← (PC + 1)$_H$,(SP – 2) ← (PC + 1)$_L$,<br>PC$_H$ ← (00000000, addr5 + 1),<br>PC$_L$ ← (00000000, addr5),<br>SP ← SP – 2 | |
| RET | | 1 | 6 | PC$_H$ ← (SP + 1), PC$_L$ ← (SP),<br>SP ← SP + 2 | |
| RETI | | 1 | 8 | PC$_H$ ← (SP + 1), PC$_L$ ← (SP),<br>PSW ← (SP + 2), SP ← SP + 3,<br>NMIS ← 0 | R R R |
| PUSH | PSW | 1 | 2 | (SP – 1) ← PSW, SP ← SP – 1 | |
| | rp | 1 | 4 | (SP – 1) ← rp$_H$, (SP – 2) ← rp$_L$,<br>SP ← SP – 2 | |
| POP | PSW | 1 | 4 | PSW ← (SP), SP ← SP + 1 | R R R |
| | rp | 1 | 6 | rp$_H$ ← (SP + 1), rp$_L$ ← (SP),<br>SP ← SP + 2 | |
| MOVW | SP, AX | 2 | 8 | SP ← AX | |
| | AX, SP | 2 | 6 | AX ← SP | |
| BR | !addr16 | 3 | 6 | PC ← addr16 | |
| | $addr16 | 2 | 6 | PC ← PC + 2 + jdisp8 | |
| | AX | 1 | 6 | PC$_H$ ← A, PC$_L$ ← X | |

**Remark** One instruction clock cycle is one cycle of the CPU clock ($f_{CPU}$), selected by the processor clock control register (PCC).

| Mnemonic | Operand | Byte | Clock | Operation | Flag |
|---|---|---|---|---|---|
| | | | | | Z AC CY |
| BC | $addr16 | 2 | 6 | PC ← PC + 2 + jdisp8 if CY = 1 | |
| BNC | $addr16 | 2 | 6 | PC ← PC + 2 + jdisp8 if CY = 0 | |
| BZ | $addr16 | 2 | 6 | PC ← PC + 2 + jdisp8 if Z = 1 | |
| BNZ | $addr16 | 2 | 6 | PC ← PC + 2 + jdisp8 if Z = 0 | |
| BT | saddr. bit, $addr16 | 4 | 10 | PC ← PC + 4 + jdisp8<br>if (saddr. bit) = 1 | |
| | sfr. bit, $addr16 | 4 | 10 | PC ← PC + 4 + jdisp8 if sfr. bit = 1 | |
| | A. bit , $addr16 | 3 | 8 | PC ← PC + 3 + jdisp8 if A. bit = 1 | |
| | PSW. bit, $addr16 | 4 | 10 | PC ← PC + 4 + jdisp8 if PSW. bit = 1 | |
| BF | saddr. bit, $addr16 | 4 | 10 | PC ← PC + 4 + jdisp8<br>if (saddr. bit) = 0 | |
| | sfr. bit, $addr16 | 4 | 10 | PC ← PC + 4 + jdisp8 if sfr. bit = 0 | |
| | A. bit, $addr16 | 3 | 8 | PC ← PC + 3 + jdisp8 if A. bit = 0 | |
| | PSW. bit, $addr16 | 4 | 10 | PC ← PC + 4 + jdisp8 if PSW. bit = 0 | |
| DBNZ | B, $addr16 | 2 | 6 | B ← B – 1, then<br>PC ← PC + 2 + jdisp8 if B ≠ 0 | |
| | C, $addr16 | 2 | 6 | C ← C – 1, then<br>PC ← PC + 2 + jdisp8 if C ≠ 0 | |
| | saddr, $addr16 | 3 | 8 | (saddr) ← (saddr) – 1, then<br>PC ← PC + 3 + jdisp8 if(saddr) ≠ 0 | |
| NOP | | 1 | 2 | No Operation | |
| EI | | 3 | 6 | IE ← 1(Enable Interrupt) | |
| DI | | 3 | 6 | IE ← 0(Disable Interrupt) | |
| HALT | | 1 | 2 | Set HALT Mode | |
| STOP | | 1 | 2 | Set STOP Mode | |

**Remark** One instruction clock cycle is one cycle of the CPU clock ($f_{CPU}$), selected by the processor clock control register (PCC).

## 8. ELECTRICAL SPECIFICATIONS

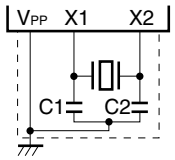
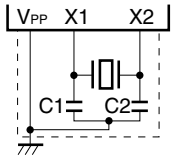
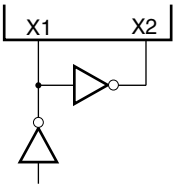
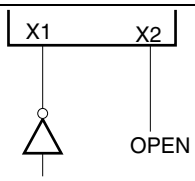
**Absolute Maximum Ratings ($T_A$ = 25°C)**

| Parameter | Symbol | Conditions | | Ratings | Unit |
|---|---|---|---|---|---|
| Supply voltage | $V_{DD}$, $AV_{DD}$ | $V_{DD}$ = $AV_{DD}$ | | –0.3 to +6.5 | V |
| | $V_{PP}$ | | | –0.3 to +10.5 | V |
| Input voltage | $V_{I1}$ | Pins other than P50 to P53 | | –0.3 to $V_{DD}$ + 0.3 | V |
| | $V_{I2}$ | P50 to P53 | With N-ch open drain | –0.3 to +13 | V |
| Output voltage | $V_O$ | | | –0.3 to $V_{DD}$ + 0.3 | V |
| Output current, high | $I_{OH}$ | Per pin | μPD78F9116B | –10 | mA |
| | | Total for all pins | | –30 | mA |
| | | Per pin | μPD78F9116B(A) | 10 | mA |
| | | Total for all pins | | 120 | mA |
| Output current, low | $I_{OL}$ | Per pin | μPD78F9116B | 30 | mA |
| | | Total for all pins | | 160 | mA |
| | | Per pin | μPD78F9116B(A) | –7 | mA |
| | | Total for all pins | | –22 | mA |
| Operating ambient temperature | $T_A$ | In normal operation mode | | –40 to +85 | °C |
| | | During flash memory programming | | 10 to 40 | °C |
| Storage temperature | $T_{stg}$ | | | –40 to +125 | °C |

**Caution Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.**

**Remark** Unless specified otherwise, the characteristics of alternate-function pins are the same as those of port pins.

**System Clock Oscillator Characteristics ($T_A$ = –40 to +85°C, $V_{DD}$ = 1.8 to 5.5 V)**

| Resonator | Recommended Circuit | Parameter | Conditions | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|---|
| Ceramic resonator |  | Oscillation frequency ($f_X$)[Note 1] | $V_{DD}$ = 4.5 to 5.5 V | 1.0 | | 10.0 | MHz |
| | | | $V_{DD}$ = 3.0 to 5.5 V | 1.0 | | 6.0 | MHz |
| | | | $V_{DD}$ = 1.8 to 5.5 V | 1.0 | | 5.0 | MHz |
| | | Oscillation stabilization time[Note 2] | After $V_{DD}$ reaches oscillation voltage range MIN. | | | 4 | ms |
| Crystal resonator |  | Oscillation frequency ($f_X$)[Note 1] | $V_{DD}$ = 4.5 to 5.5 V | 1.0 | | 10.0 | MHz |
| | | | $V_{DD}$ = 3.0 to 5.5 V | 1.0 | | 6.0 | MHz |
| | | | $V_{DD}$ = 1.8 to 5.5 V | 1.0 | | 5.0 | MHz |
| | | Oscillation stabilization time[Note 2] | $V_{DD}$ = 4.5 to 5.5 V | | | 10 | ms |
| | | | $V_{DD}$ = 1.8 to 5.5 V | | | 30 | |
| External clock |  | X1 input frequency ($f_X$)[Note 1] | $V_{DD}$ = 4.5 to 5.5 V | 1.0 | | 10.0 | MHz |
| | | | $V_{DD}$ = 3.0 to 5.5 V | 1.0 | | 6.0 | MHz |
| | | | $V_{DD}$ = 1.8 to 5.5 V | 1.0 | | 5.0 | MHz |
| | | X1 input high-/low-level width ($t_{XH}$, $t_{XL}$) | $V_{DD}$ = 4.5 to 5.5 V | 45 | | 500 | ns |
| | | | $V_{DD}$ = 3.0 to 5.5 V | 75 | | 500 | ns |
| | | | $V_{DD}$ = 1.8 to 5.5 V | 85 | | 500 | ns |
| |  | X1 input frequency ($f_X$)[Note 1] | $V_{DD}$ = 2.7 to 5.5 V | 1.0 | | 5.0 | MHz |
| | | X1 input high-/low-level width ($t_{XH}$, $t_{XL}$) | | 85 | | 500 | ns |

**Notes 1.** Indicates only oscillator characteristics. Refer to **AC characteristics** for instruction execution time.

**2.** Time required to stabilize oscillation after a reset or STOP mode release. Use the resonator that stabilizes oscillation during the oscillation wait time.

**Caution When using the system clock oscillator, wire as follows in the area enclosed by the broken lines in the above figures to avoid an adverse effect from wiring capacitance.**

- **Keep the wiring length as short as possible.**
- **Do not cross the wiring with the other signal lines.**
- **Do not route the wiring near a signal line through which a high fluctuating current flows.**
- **Always make the ground point of the oscillator capacitor the same potential as $V_{SS}$.**
- **Do not ground the capacitor to a ground pattern through which a high current flows.**
- **Do not fetch signals from the oscillator.**

**Remark** For the resonator selection and oscillator constant, customers are requested to either evaluate the oscillation themselves or apply to the resonator manufacturer for evaluation.

**DC Characteristics ($T_A$ = –40 to +85°C, $V_{DD}$ = 1.8 to 5.5 V) (1/2)**

| Parameter | Symbol | Conditions | | | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|---|---|
| Output current, high | $I_{OH}$ | Per pin | μPD78F9116B | | | | –1 | mA |
| | | Total for all pins | | | | | –15 | mA |
| | | Per pin | μPD78F9116B(A) | | | | –1 | mA |
| | | Total for all pins | | | | | –11 | mA |
| Output current, low | $I_{OL}$ | Per pin | μPD78F9116B | | | | 10 | mA |
| | | Total for all pins | | | | | 80 | mA |
| | | Per pin | μPD78F9116B(A) | | | | 3 | mA |
| | | Total for all pins | | | | | 60 | mA |
| Input voltage, high | $V_{IH1}$ | Pins other than described below | | $V_{DD}$ = 2.7 to 5.5 V | 0.7 $V_{DD}$ | | $V_{DD}$ | V |
| | | | | $V_{DD}$ = 1.8 to 5.5 V | 0.9 $V_{DD}$ | | $V_{DD}$ | V |
| | $V_{IH2}$ | P50 to P53 | N-ch open drain | $V_{DD}$ = 2.7 to 5.5 V | 0.7 $V_{DD}$ | | 12 | V |
| | | | | $V_{DD}$ = 1.8 to 5.5 V, $T_A$ = 25 to 85 °C | 0.9 $V_{DD}$ | | 12 | V |
| | $V_{IH3}$ | $\overline{\text{RESET}}$, P20 to P25 | | $V_{DD}$ = 2.7 to 5.5 V | 0.8 $V_{DD}$ | | $V_{DD}$ | V |
| | | | | $V_{DD}$ = 1.8 to 5.5 V | 0.9 $V_{DD}$ | | $V_{DD}$ | V |
| | $V_{IH4}$ | X1, X2 | | $V_{DD}$ = 4.5 to 5.5 V | $V_{DD}$ – 0.5 | | $V_{DD}$ | V |
| | | | | $V_{DD}$ = 1.8 to 5.5 V | $V_{DD}$ – 0.1 | | $V_{DD}$ | V |
| Input voltage, low | $V_{IL1}$ | Pins other than described below | | $V_{DD}$ = 2.7 to 5.5 V | 0 | | 0.3 $V_{DD}$ | V |
| | | | | $V_{DD}$ = 1.8 to 5.5 V | 0 | | 0.1 $V_{DD}$ | V |
| | $V_{IL2}$ | P50 to P53 | N-ch open drain | $V_{DD}$ = 2.7 to 5.5 V | 0 | | 0.3 $V_{DD}$ | V |
| | | | | $V_{DD}$ = 1.8 to 5.5 V, $T_A$ = 25 to 85 °C | 0 | | 0.1 $V_{DD}$ | V |
| | $V_{IL3}$ | $\overline{\text{RESET}}$, P20 to P25 | | $V_{DD}$ = 2.7 to 5.5 V | 0 | | 0.2 $V_{DD}$ | V |
| | | | | $V_{DD}$ = 1.8 to 5.5 V | 0 | | 0.1 $V_{DD}$ | V |
| | $V_{IL4}$ | X1, X2 | | $V_{DD}$ = 4.5 to 5.5 V | 0 | | 0.4 | V |
| | | | | $V_{DD}$ = 1.8 to 5.5 V | 0 | | 0.1 | V |
| Output voltage, high | $V_{OH1}$ | $V_{DD}$ = 4.5 to 5.5 V, $I_{OH}$ = –1 mA | | | $V_{DD}$ – 1.0 | | | V |
| | $V_{OH2}$ | $V_{DD}$ = 1.8 to 5.5 V, $I_{OH}$ = –100 μA | | | $V_{DD}$ – 0.5 | | | V |
| Output voltage, low | $V_{OL1}$ | Pins other than P50 to P53 | $V_{DD}$ = 4.5 to 5.5 V, $I_{OL}$ = 10 mA (μPD78F9116B) | | | | 1.0 | V |
| | | | $V_{DD}$ = 4.5 to 5.5 V, $I_{OL}$ = 3 mA (μPD78F9116B(A)) | | | | 1.0 | V |
| | | | $V_{DD}$ = 1.8 to 5.5 V, $I_{OL}$ = 400 μA | | | | 0.5 | V |
| | $V_{OL2}$ | P50 to P53 | $V_{DD}$ = 4.5 to 5.5 V, $I_{OL}$ = 10 mA (μPD78F9116B) | | | | 1.0 | V |
| | | | $V_{DD}$ = 4.5 to 5.5 V, $I_{OL}$ = 3 mA (μPD78F9116B(A)) | | | | 1.0 | V |
| | | | $V_{DD}$ = 1.8 to 5.5 V, $I_{OL}$ = 1.6 mA | | | | 0.4 | V |

**Remark** Unless specified otherwise, the characteristics of alternate-function pins are the same as those of port pins.

**DC Characteristics ($T_A$ = –40 to +85°C, $V_{DD}$ = 1.8 to 5.5 V) (2/2)**

| Parameter | Symbol | Conditions | | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|---|
| Input leakage current, high | $I_{LIH1}$ | Pins other than X1, X2, or P50 to P53 | $V_{IN} = V_{DD}$ | | | 3 | μA |
| | $I_{LIH2}$ | X1, X2 | | | | 20 | μA |
| | $I_{LIH3}$ | P50 to P53 (N-ch open drain) | $V_{IN}$ = 12 V | | | 20 | μA |
| Input leakage current, low | $I_{LIL1}$ | Pins other than X1, X2, or P50 to P53 | $V_{IN}$ = 0 V | | | –3 | μA |
| | $I_{LIL2}$ | X1, X2 | | | | –20 | μA |
| | $I_{LIL3}$ | P50 to P53 (N-ch open drain) | | | | –3 Note 1 | μA |
| Output leakage current, high | $I_{LOH}$ | $V_{OUT} = V_{DD}$ | | | | 3 | μA |
| Output leakage current, low | $I_{LOL}$ | $V_{OUT}$ = 0 V | | | | –3 | μA |
| Software pull-up resistor | $R_1$ | $V_{IN}$ = 0 V, for pins other than P50 to P53 | | 50 | 100 | 200 | kΩ |
| Power supply current | $I_{DD1}$ Note 2 | 10.0 MHz crystal oscillation operating mode | $V_{DD}$ = 5.0 V±10% Note 4 | | 10.0 | 20.0 | mA |
| | | 6.0 MHz crystal oscillation operating mode | $V_{DD}$ = 5.0 V±10% Note 4 | | 6.0 | 12.0 | mA |
| | | 5.0 MHz crystal oscillation operating mode (C1 = C2 = 22 pF) | $V_{DD}$ = 5.0 V±10% Note 4 | | 4.0 | 10.0 | mA |
| | | | $V_{DD}$ = 3.0 V±10% Note 5 | | 1.0 | 2.5 | mA |
| | | | $V_{DD}$ = 2.0 V±10% Note 5 | | 0.8 | 2.0 | mA |
| | $I_{DD2}$ Note 2 | 10.0 MHz crystal oscillation HALT mode | $V_{DD}$ = 5.0 V±10% Note 4 | | 1.2 | 6.0 | mA |
| | | 6.0 MHz crystal oscillation HALT mode | $V_{DD}$ = 5.0 V±10% Note 4 | | 0.9 | 2.8 | mA |
| | | 5.0 MHz crystal oscillation HALT mode (C1 = C2 = 22 pF) | $V_{DD}$ = 5.0 V±10% Note 4 | | 0.6 | 2.5 | mA |
| | | | $V_{DD}$ = 3.0 V±10% Note 5 | | 0.3 | 2.0 | mA |
| | | | $V_{DD}$ = 2.0 V±10% Note 5 | | 0.2 | 1.5 | mA |
| | $I_{DD3}$ Note 2 | STOP mode | $V_{DD}$ = 5.0 V±10% | | 0.1 | 30 | μA |
| | | | $V_{DD}$ = 3.0 V±10% | | 0.05 | 10 | μA |
| | | | $V_{DD}$ = 2.0 V±10% | | 0.05 | 10 | μA |
| | $I_{DD4}$ Note 3 | 10.0 MHz crystal oscillation A/D operating mode | $V_{DD}$ = 5.0 V±10% Note 4 | | 11.0 | 22.5 | mA |
| | | 6.0 MHz crystal oscillation A/D operating mode | $V_{DD}$ = 5.0 V±10% Note 4 | | 7.0 | 14.5 | mA |
| | | 5.0 MHz crystal oscillation A/D operating mode (C1 = C2 = 22 pF) | $V_{DD}$ = 5.0 V±10% Note 4 | | 5.0 | 12.5 | mA |
| | | | $V_{DD}$ = 3.0 V±10% Note 5 | | 2.0 | 5.0 | mA |
| | | | $V_{DD}$ = 2.0 V±10% Note 5 | | 1.8 | 4.5 | mA |

**Notes 1.** When port 5 is in input mode, a low-level input leakage current of –60 μA (MAX.) flows only for 1 cycle time after a read instruction has been executed to port 5.

**2.** The current flowing to the ports (including the current flowing through an on-chip pull-up resistor) and $AV_{DD}$ current are not included.

**3.** The current flowing to the ports (including the current flowing through an on-chip pull-up resistor) is not included.

**4.** High-speed mode operation (when processor clock control register (PCC) is set to 00H.)

**5.** Low-speed mode operation (when PCC is set to 02H).

**Remark** Unless specified otherwise, the characteristics of alternate-function pins are the same as those of port pins.

**Flash Memory Write/Erase Characteristics ($T_A$ = 10 to 40°C, $V_{DD}$ = 1.8 to 5.5 V)**

| Parameter | Symbol | Conditions | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|
| Operating frequency | $f_X$ | $V_{DD}$ = 4.5 to 5.5 V | 1.0 | | 10.0 | MHz |
| | | $V_{DD}$ = 3.0 to 5.5 V | 1.0 | | 6.0 | MHz |
| | | $V_{DD}$ = 2.7 to 5.5 V | 1.0 | | 5.0 | MHz |
| | | $V_{DD}$ = 1.8 to 5.5 V | 1.0 | | 1.25 | MHz |
| Write current ($V_{DD}$ pin) Note | $I_{DDW}$ | When $V_{PP}$ supply voltage = $V_{PP1}$ ( 5.0 MHz crystal oscillation operating mode ) | | | 21 | mA |
| Write current ($V_{PP}$ pin) Note | $I_{PPW}$ | When $V_{PP}$ supply voltage = $V_{PP1}$ | | | 22.5 | mA |
| Erase current ($V_{DD}$ pin) Note | $I_{DDE}$ | When $V_{PP}$ supply voltage = $V_{PP1}$ ( 5.0 MHz crystal oscillation operating mode ) | | | 3 | mA |
| Erase current ($V_{PP}$ pin) Note | $I_{PPE}$ | When $V_{PP}$ supply voltage = $V_{PP1}$ | | | 115 | mA |
| Unit erase time | $t_{er}$ | | 0.2 | 0.2 | 0.2 | s |
| Total erase time | $t_{era}$ | | | | 20 | s |
| Write count | | Erase/write are regarded as 1 cycle | | | 20 | Times |
| $V_{PP}$ supply voltage | $V_{PP0}$ | In normal operation | 0 | | $0.2V_{DD}$ | V |
| | $V_{PP1}$ | During flash memory programming | 9.7 | 10.0 | 10.3 | V |

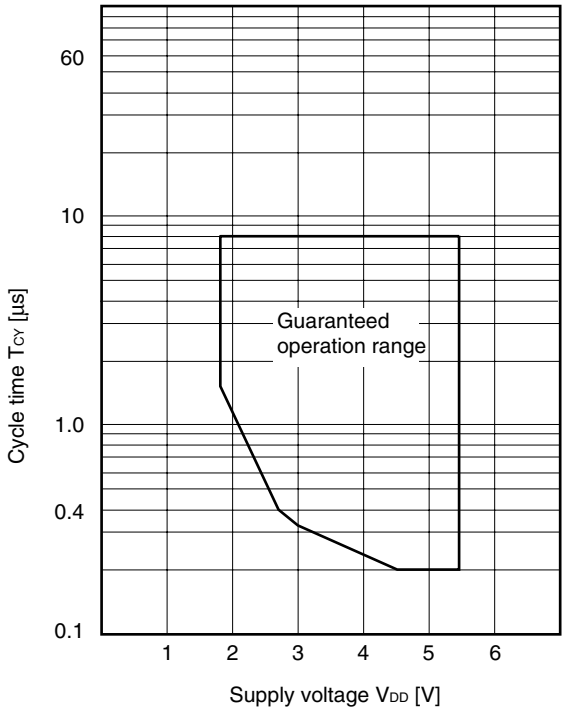
**Note** The current flowing to the ports (including the current flowing through an on-chip pull-up resistor) and $AV_{DD}$ current are not included.

**AC Characteristics**

**(1) Basic operation ($T_A$ = –40 to +85°C, $V_{DD}$ = 1.8 to 5.5 V)**

| Parameter | Symbol | Conditions | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|
| Cycle time (minimum instruction execution time) | $T_{CY}$ | $V_{DD}$ = 4.5 to 5.5 V | 0.2 | | 8 | μs |
| | | $V_{DD}$ = 3.0 to 5.5 V | 0.33 | | 8 | μs |
| | | $V_{DD}$ = 2.7 to 5.5 V | 0.4 | | 8 | μs |
| | | $V_{DD}$ = 1.8 to 5.5 V | 1.6 | | 8 | μs |
| TI80 input high-/low-level width | $t_{TIH}$, $t_{TIL}$ | $V_{DD}$ = 2.7 to 5.5 V | 0.1 | | | μs |
| | | $V_{DD}$ = 1.8 to 5.5 V | 1.8 | | | μs |
| TI80 input frequency | $f_{TI}$ | $V_{DD}$ = 2.7 to 5.5 V | 0 | | 4 | MHz |
| | | $V_{DD}$ = 1.8 to 5.5 V | 0 | | 275 | kHz |
| Interrupt input high-/low-level width | $t_{INTH}$, $t_{INTL}$ | INTP0 to INTP2 | 10 | | | μs |
| $\overline{\text{RESET}}$ low-level width | $t_{RSL}$ | | 10 | | | μs |
| CPT20 input high-/low-level width | $t_{CPH}$, $t_{CPL}$ | | 10 | | | μs |

**$T_{CY}$ vs $V_{DD}$**



**(2) Serial interface ($T_A$ = –40 to +85°C, $V_{DD}$ = 1.8 to 5.5 V)**

**(i) 3-wire serial I/O mode ($\overline{SCK20}$...Internal clock output)**

| Parameter | Symbol | Conditions | | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|---|
| $\overline{SCK20}$ cycle time | $t_{KCY1}$ | $V_{DD}$ = 2.7 to 5.5 V | | 800 | | | ns |
| | | $V_{DD}$ = 1.8 to 5.5 V | | 3200 | | | ns |
| $\overline{SCK20}$ high-/low-level width | $t_{KH1}$, $t_{KL1}$ | $V_{DD}$ = 2.7 to 5.5 V | | $t_{KCY1}/2 - 50$ | | | ns |
| | | $V_{DD}$ = 1.8 to 5.5 V | | $t_{KCY1}/2 - 150$ | | | ns |
| SI20 setup time (to $\overline{SCK20}\uparrow$) | $t_{SIK1}$ | $V_{DD}$ = 2.7 to 5.5 V | | 150 | | | ns |
| | | $V_{DD}$ = 1.8 to 5.5 V | | 500 | | | ns |
| SI20 hold time (from $\overline{SCK20}\uparrow$) | $t_{KSI1}$ | $V_{DD}$ = 2.7 to 5.5 V | | 400 | | | ns |
| | | | | 600 | | | ns |
| SO20 output delay time from $\overline{SCK20}\downarrow$ | $t_{KSO1}$ | R = 1 kΩ, C = 100 pF[Note] | $V_{DD}$ = 2.7 to 5.5 V | 0 | | 250 | ns |
| | | | $V_{DD}$ = 1.8 to 5.5 V | 0 | | 1000 | ns |

**Note** R and C are the load resistance and load capacitance of the SO output line.

**(ii) 3-wire serial I/O mode ($\overline{SCK20}$...External clock input)**

| Parameter | Symbol | Conditions | | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|---|
| $\overline{SCK20}$ cycle time | $t_{KCY2}$ | $V_{DD}$ = 2.7 to 5.5 V | | 800 | | | ns |
| | | $V_{DD}$ = 1.8 to 5.5 V | | 3200 | | | ns |
| $\overline{SCK20}$ high-/low-level width | $t_{KH2}$, $t_{KL2}$ | $V_{DD}$ = 2.7 to 5.5 V | | 400 | | | ns |
| | | $V_{DD}$ = 1.8 to 5.5 V | | 1600 | | | ns |
| SI20 setup time (to $\overline{SCK20}\uparrow$) | $t_{SIK2}$ | $V_{DD}$ = 2.7 to 5.5 V | | 100 | | | ns |
| | | $V_{DD}$ = 1.8 to 5.5 V | | 150 | | | ns |
| SI20 hold time (from $\overline{SCK20}\uparrow$) | $t_{KSI2}$ | $V_{DD}$ = 2.7 to 5.5 V | | 400 | | | ns |
| | | $V_{DD}$ = 1.8 to 5.5 V | | 600 | | | ns |
| SO20 output delay time from $\overline{SCK20}\downarrow$ | $t_{KSO2}$ | R = 1 kΩ, C = 100 pF[Note] | $V_{DD}$ = 2.7 to 5.5 V | 0 | | 300 | ns |
| | | | $V_{DD}$ = 1.8 to 5.5 V | 0 | | 1000 | ns |
| SO20 setup time (for $\overline{SS20}\downarrow$ when $\overline{SS20}$ is used) | $t_{KAS2}$ | $V_{DD}$ = 2.7 to 5.5 V | | | | 120 | ns |
| | | $V_{DD}$ = 1.8 to 5.5 V | | | | 400 | ns |
| SO20 disable time (for $\overline{SS20}\uparrow$ when $\overline{SS20}$ is used) | $t_{KDS2}$ | $V_{DD}$ = 2.7 to 5.5 V | | | | 240 | ns |
| | | $V_{DD}$ = 1.8 to 5.5 V | | | | 800 | ns |

**Note** R and C are the load resistance and load capacitance of the SO output line.

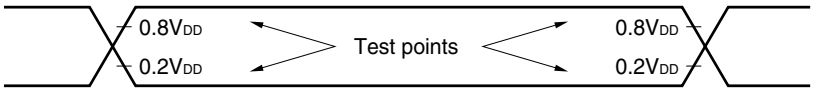
**(iii) UART mode (Dedicated baud rate generator output)**

| Parameter | Symbol | Conditions | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|
| Transfer rate | | $V_{DD}$ = 2.7 to 5.5 V | | | 78125 | bps |
| | | $V_{DD}$ = 1.8 to 5.5 V | | | 19531 | bps |

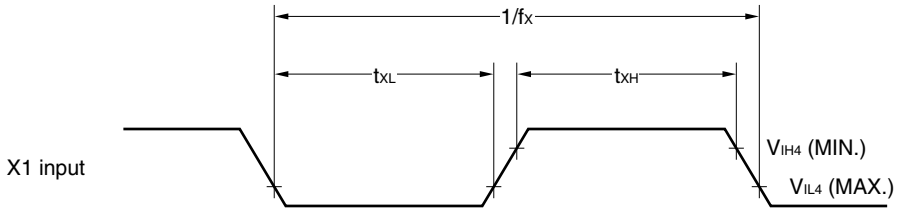
**(iv) UART mode (external clock input)**

| Parameter | Symbol | Conditions | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|
| ASCK20 cycle time | $t_{KCY3}$ | $V_{DD}$ = 2.7 to 5.5 V | 800 | | | ns |
| | | $V_{DD}$ = 1.8 to 5.5 V | 3200 | | | ns |
| ASCK20 high-/low-level width | $t_{KH3}$, $t_{KL3}$ | $V_{DD}$ = 2.7 to 5.5 V | 400 | | | ns |
| | | $V_{DD}$ = 1.8 to 5.5 V | 1600 | | | ns |
| Transfer rate | | $V_{DD}$ = 2.7 to 5.5 V | | | 39063 | bps |
| | | $V_{DD}$ = 1.8 to 5.5 V | | | 9766 | bps |
| ASCK20 rise/fall time | $t_R$, $t_F$ | | | | 1 | μs |

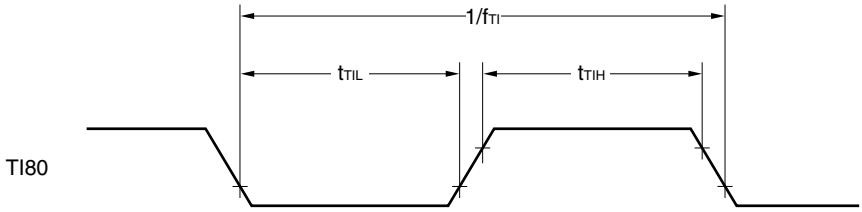
**AC Timing Test Points (excluding X1 input)**



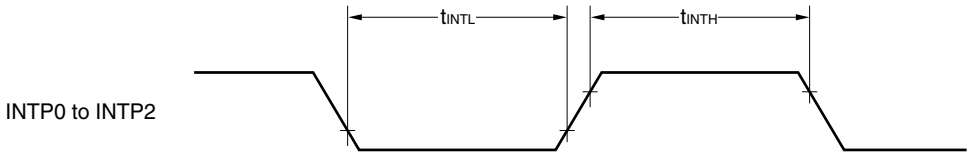

**Clock Timing**



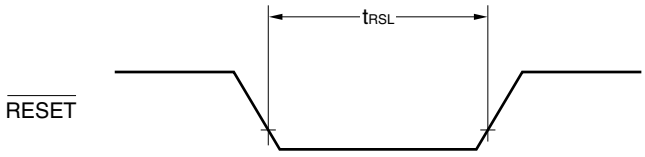

**TI Timing**




**Interrupt Input Timing**

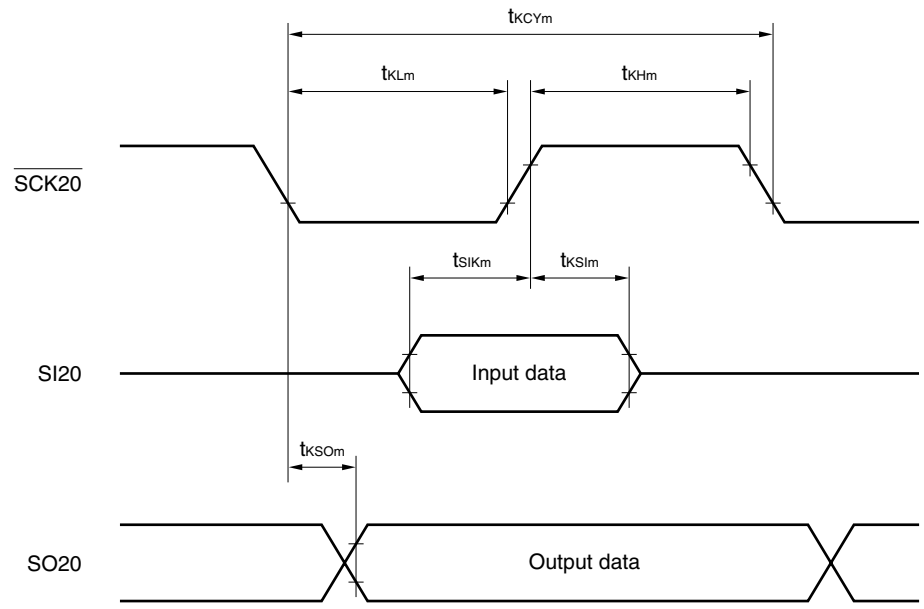



**$\overline{\text{RESET}}$ Input Timing**



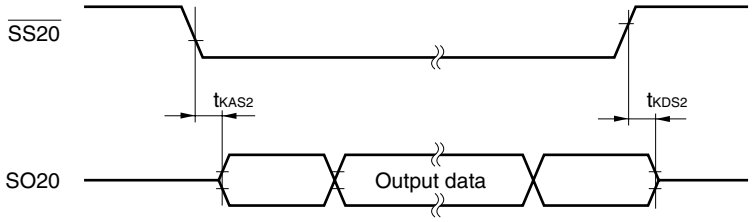
**Serial Transfer Timing**

**3-wire serial I/O mode:**

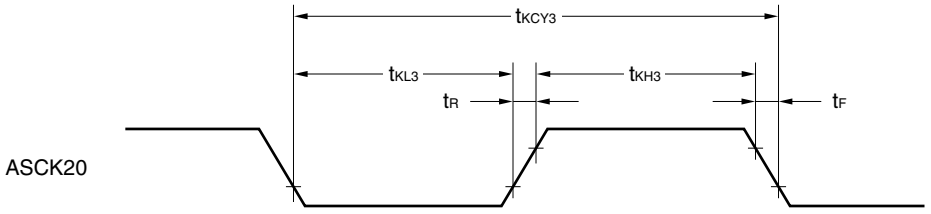



m = 1, 2

**3-wire serial I/O mode (when SS20 is used):**




**UART mode (external clock input):**



**10-Bit A/D Converter Characteristics ($T_A$ = –40 to +85°C, $AV_{DD}$ = $V_{DD}$ = 1.8 to 5.5 V, $AV_{SS}$ = $V_{SS}$ = 0 V)**

| Parameter | Symbol | Conditions | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|
| Resolution | | | 10 | 10 | 10 | bit |
| Overall error[Note1,2] | | 4.5 V ≤ $V_{DD}$ ≤ 5.5 V | | ±0.2 | ±0.4 | %FSR |
| | | 2.7 V ≤ $V_{DD}$ < 4.5 V | | ±0.4 | ±0.6 | %FSR |
| | | 1.8 V ≤ $V_{DD}$ < 2.7 V | | ±0.8 | ±1.2 | %FSR |
| Conversion time | $t_{CONV}$ | 4.5 V ≤ $V_{DD}$ ≤ 5.5 V | 12 | | 100 | μs |
| | | 2.7 V ≤ $V_{DD}$ < 4.5 V | 14 | | 100 | μs |
| | | 1.8 V ≤ $V_{DD}$ < 2.7 V | 28 | | 100 | μs |
| Zero-scale error[Note1,2] | | 4.5 V ≤ $V_{DD}$ ≤ 5.5 V | | | ±0.4 | %FSR |
| | | 2.7 V ≤ $V_{DD}$ < 4.5 V | | | ±0.6 | %FSR |
| | | 1.8 V ≤ $V_{DD}$ < 2.7 V | | | ±1.2 | %FSR |
| Full-scale error[Note1,2] | | 4.5 V ≤ $V_{DD}$ ≤ 5.5 V | | | ±0.4 | %FSR |
| | | 2.7 V ≤ $V_{DD}$ < 4.5 V | | | ±0.6 | %FSR |
| | | 1.8 V ≤ $V_{DD}$ < 2.7 V | | | ±1.2 | %FSR |
| Integral linearity error[Note1] | ILE | 4.5 V ≤ $V_{DD}$ ≤ 5.5 V | | | ±2.5 | LSB |
| | | 2.7 V ≤ $V_{DD}$ < 4.5 V | | | ±4.5 | LSB |
| | | 1.8 V ≤ $V_{DD}$ < 2.7 V | | | ±8.5 | LSB |
| Differential linearity error[Note1] | DLE | 4.5 V ≤ $V_{DD}$ ≤ 5.5 V | | | ±1.5 | LSB |
| | | 2.7 V ≤ $V_{DD}$ < 4.5 V | | | ±2.0 | LSB |
| | | 1.8 V ≤ $V_{DD}$ < 2.7 V | | | ±3.5 | LSB |
| Analog input voltage | $V_{IAN}$ | | 0 | | $AV_{DD}$ | V |

**Notes 1.** Excludes quantization error (±0.05%FSR).

**2.** It is indicated as a ratio to the full-scale value (%FSR).

**Data Memory STOP Mode Low Supply Voltage Data Retention Characteristics ($T_A$ = –40 to +85°C)**

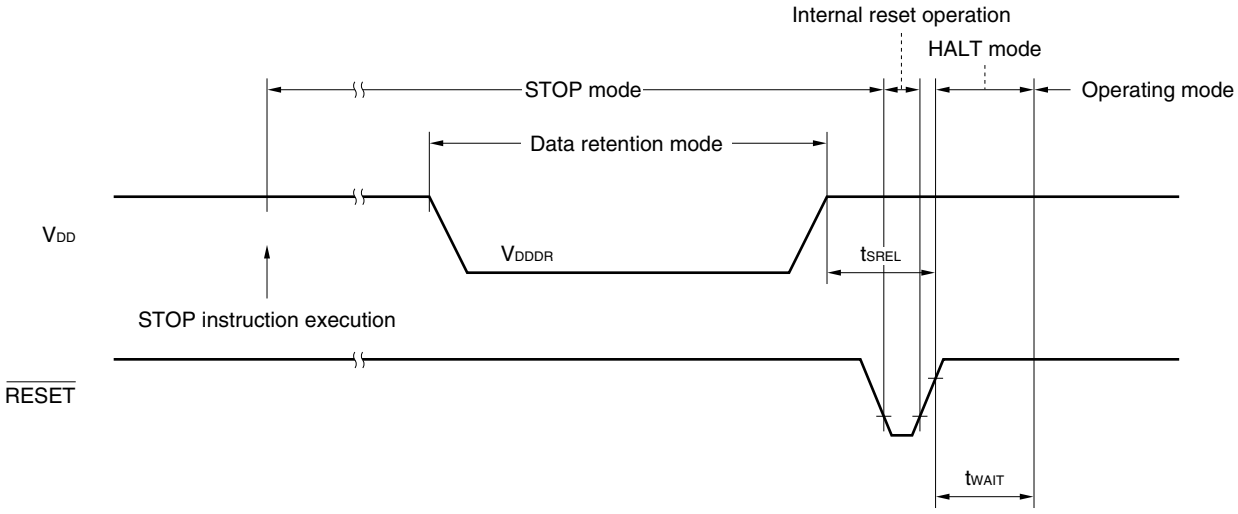
| Parameter | Symbol | Conditions | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|
| Data retention supply voltage | $V_{DDDR}$ | | 1.8 | | 5.5 | V |
| Release signal set time | $t_{SREL}$ | | 0 | | | μs |
| Oscillation stabilization wait time[Note 1] | $t_{WAIT}$ | Release by $\overline{RESET}$ | | $2^{15}/f_X$ | | ms |
| | | Release by interrupt request | | **Note 2** | | ms |

**Notes 1.** The oscillation stabilization wait time is the period during which the CPU operation is stopped to avoid unstable operation at the beginning of oscillation.

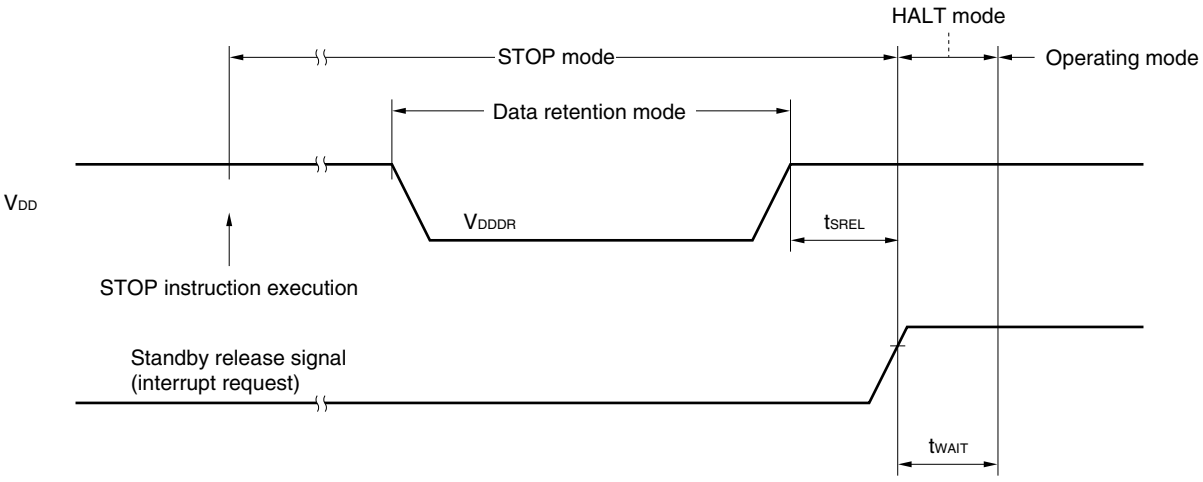
**2.** Selection of $2^{12}/f_X$, $2^{15}/f_X$, or $2^{17}/f_X$ is possible with bits 0 to 2 (OSTS0 to OSTS2) of the oscillation stabilization time select register.

**Remark** fx: System clock oscillation frequency

**Data Retention Timing (STOP mode release by $\overline{RESET}$)**

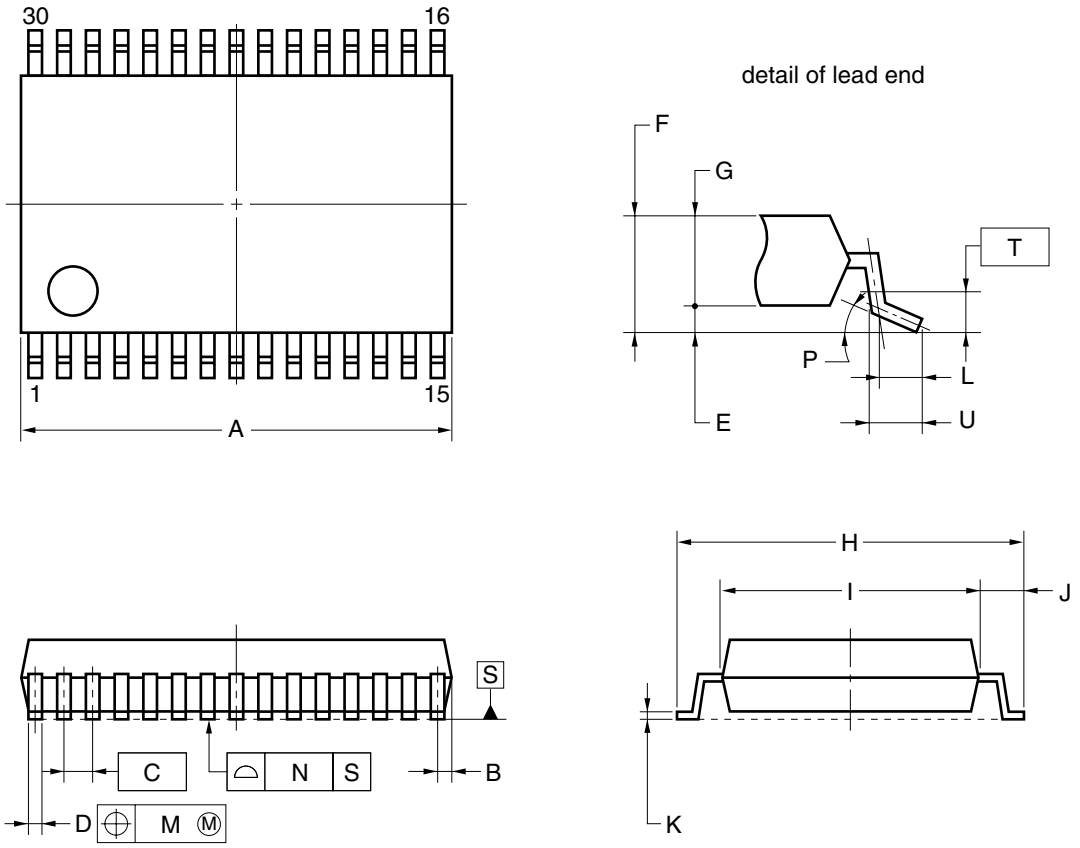



**Data Retention Timing (Standby release signal: STOP mode release by interrupt signal)**



## 9. PACKAGE DRAWING

### 30-PIN PLASTIC SSOP (7.62 mm (300))




**NOTE**

Each lead centerline is located within 0.13 mm of its true position (T.P.) at maximum material condition.

| ITEM | MILLIMETERS |
|---|---|
| A | 9.85±0.15 |
| B | 0.45 MAX. |
| C | 0.65 (T.P.) |
| D | $0.24^{+0.08}_{-0.07}$ |
| E | 0.1±0.05 |
| F | 1.3±0.1 |
| G | 1.2 |
| H | 8.1±0.2 |
| I | 6.1±0.2 |
| J | 1.0±0.2 |
| K | 0.17±0.03 |
| L | 0.5 |
| M | 0.13 |
| N | 0.10 |
| P | $3^{\circ}{}^{+5^{\circ}}_{-3^{\circ}}$ |
| T | 0.25 |
| U | 0.6±0.15 |

S30MC-65-5A4-2

## 10. RECOMMENDED SOLDERING CONDITIONS

The μPD78F9116B and 78F9116B(A) should be soldered and mounted under the following recommended conditions.

For the details of the recommended soldering conditions, refer to the document **Semiconductor Device Mounting Technology Manual (C10535E)**. For soldering methods and conditions other than those recommended below, contact your NEC sales representative.

**Table 10-1. Surface Mounting Type Soldering Conditions**

μPD78F9116BMC-5A4: 30-pin plastic SSOP (7.62 mm (300))
μPD78F9116BMC(A)-5A4: 30-pin plastic SSOP (7.62 mm (300))

| Soldering Method | Soldering Conditions | Recommended Condition Symbol |
|---|---|---|
| Infrared reflow | Package peak temperature: 235°C, Time: 30 seconds max. (at 210°C or higher), Count: Three times or less: 3 max., Exposure limit: 7days[Note] (after that, prebake at 125°C for 10 hours) | IR35-107-3 |
| VPS | Package peak temperature: 215°C, Time: 40 seconds max. (at 200°C or higher), Count: Three time or less, Exposure limit: 7days[Note] (after that, prebake at 125°C for 10 hours) | VP15-107-3 |
| Wave soldering | Solder bath temperature: 260°C max., Time: 10 seconds max., Count: Once Preheating temperature: 120°C or below (package surface temperature), Exposure limit : 7days[Note] (after that, prebake at 125°C for 10 hours) | WS60-107-1 |
| Partial heating | Pin temperature: 300°C max., Time: 3 sec. max. (per pin row) | – |

**Note** After opening the dry pack, store it at 25°C or less and 65% RH or less for the allowable storage period.

**Caution Do not use different soldering methods together (except for partial heating).**

## APPENDIX A. DEVELOPMENT TOOLS

The following development tools are available for system development using the μPD78F9116B and 78F9116B(A).

**Software package**

| | |
|---|---|
| SP78K0S[Notes 1, 2] | CD-ROM in which the development tools (software) common to the 78K/0S Series are included as a package |

**Language Processing Software**

| | |
|---|---|
| RA78K0S[Notes 1, 2, 3] | Assembler package common to 78K/0S Series |
| CC78K0S[Notes 1, 2, 3] | C compiler package common to 78K/0S Series |
| DF789136[Notes 1, 2, 3] | Device file for μPD78F9116B |

**Flash Memory Writing Tools**

| | |
|---|---|
| Flashpro III (Model number: FL-PR3[Note 4], PG-FP3) | Dedicated flash programmer for on-chip flash memory |
| FA-30MC[Note 4] | Flash memory writing adapter |

**Debugging Tools (1/2)**

| | |
|---|---|
| IE-78K0S-NS<br>In-circuit emulator | In-circuit emulator serves to debug hardware and software when developing application systems using a 78K/0S Series product. It supports the ID78K0S-NS integrated debugger. Used in combination with an AC adapter, emulation probe, and interface adapter connecting to the host machine. |
| IE-78K0S-NS-A<br>In-circuit emulator | The IE-78K0S-NS-A provides a coverage function in addition to the IE-78K0S-NS functions, thus enhancing the debug functions, including the tracer and timer functions. |
| IE-70000-MC-PS-B<br>AC adapter | Adapter used to supply power from a power outlet of 100 V AC to 240 V AC. |
| IE-70000-98-IF-C<br>Interface adapter | Adapter when PC-9800 series PC (except notebook type) is used as the host machine (C bus supported). |
| IE-70000-CD-IF-A<br>PC card interface | PC card and interface cable when notebook PC is used as the host machine (PCMCIA socket supported). |
| IE-70000-PC-IF-C<br>Interface adapter | Adapter when using an IBM PC/AT™ or compatible as the host machine. |
| IE-70000-PCI-IF-A<br>Interface adapter | Adapter when using PC that includes a PCI bus as the IE-78K0S-NS host machine. |
| IE-789136-NS-EM1<br>Emulation board | Board for emulation of the peripheral hardware peculiar to a device. Used in combination with an in-circuit emulator. |
| NP-36GS[Note 4] | Board used to connect the in-circuit emulator to the target system. For a 30-pin plastic SSOP (MC-5A4 type), used in combination with NGS-30. |
| NGS-30[Note 4]<br>Conversion socket | Conversion socket used to connect the NP-36GS to the target system board designed to mount a 30-pin plastic SSOP (MC-5A4 type). |

**Notes 1.** PC-9800 series (Japanese Windows™) based

**2.** IBM PC/AT or compatibles (Japanese/English Windows) based

**3.** HP9000 series 700™ (HP-UX™) based, SPARCstation™ (SunOS™, Solaris™) based.

**4.** Products made by Naito Densei Machida Mfg. Co., Ltd. (Phone: +81-45-475-4191)

**Remark** RA78K0S, CC78K0S, SM78K0S, and ID78K0S-NS are used in combination with the DF789136.

**Debugging Tools (2/2)**

| | |
|---|---|
| SM78K0S[Notes 1, 2] | System simulator common to 78K/0S Series |
| ID78K0S-NS[Notes 1, 2] | Integrated debugger common to 78K/0S Series |
| DF789136[Notes 1, 2] | Device file for μPD78F9116B |

**Notes 1.** PC-9800 series (Japanese Windows) based

**2.** IBM PC/AT or compatibles (Japanese/English Windows) based

**Remark** RA78K0S, CC78K0S, SM78K0S, and ID78K0S-NS are used in combination with the DF789136.

## APPENDIX B. RELATED DOCUMENTS

The related documents listed above are subject to change without notice. Be sure to use the latest version of each document for designing.

**Documents Related to Devices**

| Document Name | Document No. |
|---|---|
| μPD789101A, 102A, 104A, 111A, 112A, 114A, 101A(A), 102A(A), 104A(A), 111A(A), 112A(A), 114A(A) Data Sheet | U14590E |
| μPD78F9116B, 78F9116B(A) Data Sheet | This manual |
| μPD789104A, 789114A, 789124A, 789134A Subseries User's Manual | U14643E |
| 78K/0S Series User's Manual Instructions | U11047E |

**Documents Related to Development Software Tools (User's Manuals)**

| Document Name | | Document No. |
|---|---|---|
| RA78K0S Assembler Package | Operation | U14876E |
| | Language | U14877E |
| | Structured Assembly Language | U11623E |
| CC78K0S C Compiler | Operation | U14871E |
| | Language | U14872E |
| SM78K0S, SM78K0 System Simulator Ver. 2.10 or Later | Operation (Windows Based) | U14611E |
| SM78K Series System Simulator Ver. 2.10 or Later | External Part User Open Interface Specification | U15006E |
| ID78K0-NS, ID78K0S-NS Integrated Debugger Ver. 2.20 or Later | Operation (Windows Based) | U14910E |
| Project Manager Ver. 3.12 or Later (Windows Based) | | U14610E |

**Documents Related to Development Hardware Tools (User's Manuals)**

| Document Name | Document No. |
|---|---|
| IE-78K0S-NS In-Circuit Emulator | U13549E |
| IE-78K0S-NS-A In-Circuit Emulator | U15207E |
| IE-789136-NS-EM1 Emulation Board | U14363E |

**Documents Related to Flash Memory Writing**

| Document Name | Document No. |
|---|---|
| PG-FP3 Flash Memory Programmer User's Manual | U13502E |

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**Other Related Documents**

| Document Name | Document No. |
|---|---|
| SEMICONDUCTOR SELECTION GUIDE - Products & Packages - | X13769E |
| Semiconductor Device Mounting Technology Manual | C10535E |
| Quality Grades on NEC Semiconductor Devices | C11531E |
| NEC Semiconductor Device Reliability/Quality Control System | C10983E |
| Guide to Prevent Damage for Semiconductor Devices by Electrostatic Discharge (ESD) | C11892E |

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**[MEMO]**

**[MEMO]**

**[MEMO]**

## NOTES FOR CMOS DEVICES

### ① PRECAUTION AGAINST ESD FOR SEMICONDUCTORS

Note:

Strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor devices on it.

### ② HANDLING OF UNUSED INPUT PINS FOR CMOS

Note:

No connection for CMOS device inputs can be cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to $V_{DD}$ or GND with a resistor, if it is considered to have a possibility of being an output pin. All handling related to the unused pins must be judged device by device and related specifications governing the devices.

### ③ STATUS BEFORE INITIALIZATION OF MOS DEVICES

Note:

Power-on does not necessarily define initial status of MOS device. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the devices with reset function have not yet been initialized. Hence, power-on does not guarantee out-pin levels, I/O settings or contents of registers. Device is not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for devices having reset function.

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