

8-Channel, Dual 4-Channel, Triple 2-Channel (Triple SPDT) Multiplexers

DESCRIPTION

The DG4051A, DG4052A and DG4053A are high precision CMOS analog multiplexers. The DG4051A is an 8-channel multiplexer, the DG4052A is a dual 4-channel multiplexer and the DG4053A is a triple 2-channel multiplexer or triple SPDT.

Designed to operate from a + 2.7 V to + 12 V single supply or from a ± 2.5 V to ± 5 V dual supplies, the DG4051A, DG4052A and DG4053A are fully specified at + 3 V, + 5 V and ± 5 V. All control logic inputs have guaranteed 2.0 V logic high limit when operating from + 5 V or ± 5 V supplies and 1.4 V when operating from a + 3 V supply.

Channel leakage is typically in the range of 10 pA, and switch charge injection is less than 0.5 pC. Coupled with very low switch capacitance, these devices are ideal for high precision signal switching and multiplexing.

All switches conduct equally well in both directions, offering rail to rail analog signal switching and can be used both as multiplexers as well as de-multiplexers.

The DG4051A, DG4052A and DG4053A operating temperature is specified from - 40 °C to + 125 °C and are available in 16 pin TSSOP and the ultra compact 1.8 mm x 2.6 mm miniQFN16 packages.

FEATURES

- + 2.7 V to + 12 V single supply operation
- ± 2.5 V to ± 5 V dual supply operation
- Fully specified at + 3 V, + 5 V, ± 5 V
- 100 Ω maximum on-resistance
- Low voltage, 2.5 V CMOS/TTL compatible
- Low charge injection (< 0.5 pC typ.)
- High - 3 dB bandwidth: 330 MHz to 700 MHz
- Low switch capacitance ($C_{S(off)}$ 3 pF typ.)
- Excellent isolation and crosstalk performance (typ. 47 dB at 100 MHz)
- 16 pin SOIC, TSSOP and miniQFN package (1.8 mm x 2.6 mm)
- Fully specified from - 40 °C to + 85 °C and - 40 °C to + 125 °C
- Compliant to RoHS directive 2002/95/EC

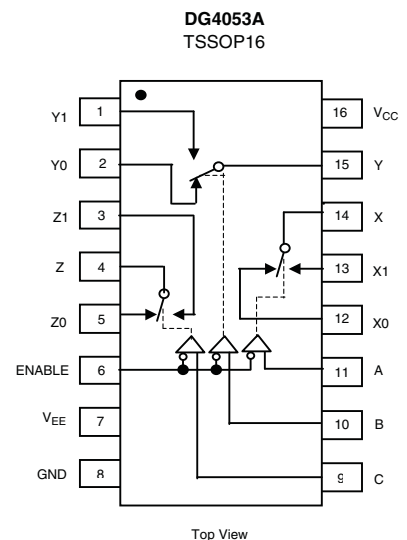
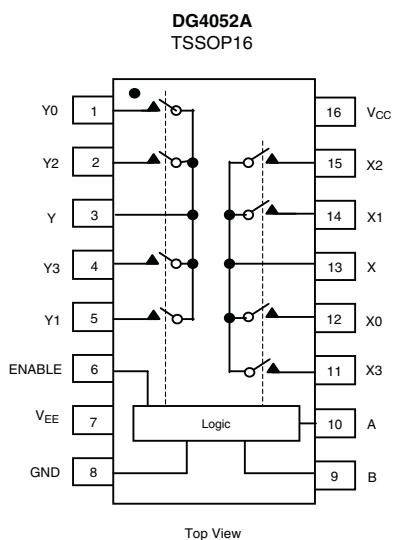
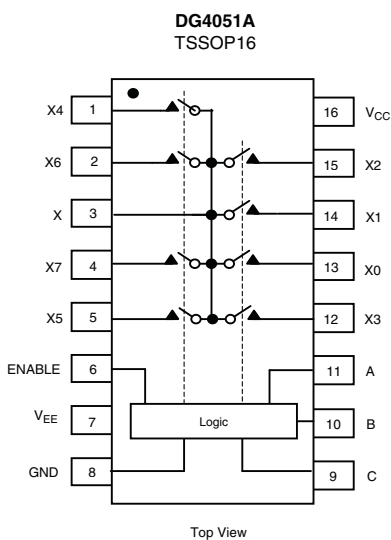


RoHS
COMPLIANT

APPLICATIONS

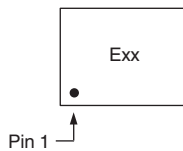
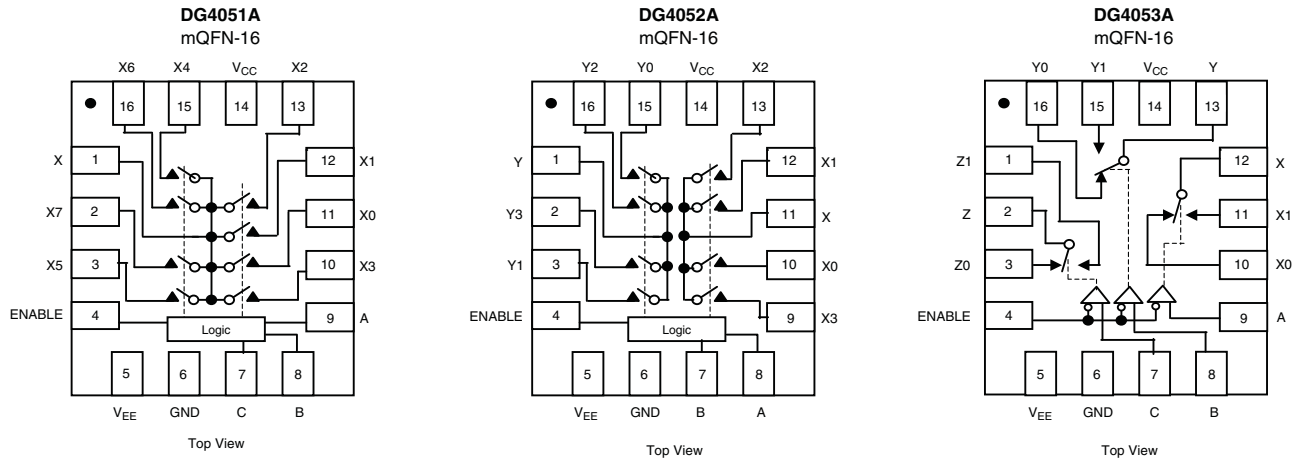
- Instruments
- Healthcare and medical equipments
- Touch panel
- Automated test equipment
- Automation and control
- High precision data acquisition
- Communication system

FUNCTIONAL BLOCK DIAGRAM AND PIN CONFIGURATION



ENABLE = LO, all switches are controlled by addr pins.
ENABLE = HI, all switches are off.

FUNCTIONAL BLOCK DIAGRAM AND PIN CONFIGURATION



Device Marking: Exx for DG4051A (miniQFN16) Fxx for DG4052A Gxx for DG4053A
xx = Date/Lot Traceability Code

| TRUTH TABLE | | | | | | |
|--------------|---------------|---|---|-------------------|-------------------|---------------------------|
| Enable Input | Select Inputs | | | On Switches | | |
| | C | B | A | DG4051A | DG4052A | DG4053A |
| H | X | X | X | All Switches Open | All Switches Open | All Switches Open |
| L | L | L | L | X to X0 | X to X0, Y to Y0 | X to X0, Y to Y0, Z to Z0 |
| L | L | L | H | X to X1 | X to X1, Y to Y1 | X to X1, Y to Y0, Z to Z0 |
| L | L | H | L | X to X2 | X to X2, Y to Y2 | X to X0, Y to Y1, Z to Z0 |
| L | L | H | H | X to X3 | X to X3, Y to Y3 | X to X1, Y to Y1, Z to Z0 |
| L | H | L | L | X to X4 | X to X0, Y to Y0 | X to X0, Y to Y0, Z to Z1 |
| L | H | L | H | X to X5 | X to X1, Y to Y1 | X to X1, Y to Y0, Z to Z1 |
| L | H | H | L | X to X6 | X to X2, Y to Y2 | X to X0, Y to Y1, Z to Z1 |
| L | H | H | H | X to X7 | X to X3, Y to Y3 | X to X1, Y to Y1, Z to Z1 |

| ORDERING INFORMATION | | |
|--------------------------------|----------------|---|
| Temp Range | Package | Part Number |
| DG4051A, DG4052A, DG4053A | | |
| - 40 °C to 125 °C ^a | 16-Pin TSSOP | DG4051AEQ-T1-E3 DG4052AEQ-T1-E3 DG4053AEQ-T1-E3 |
| | 16-Pin miniQFN | DG4051AEN-T1-E4 DG4052AEN-T1-E4 DG4053AEN-T1-E4 |

Notes:

a. - 40 °C to 85 °C datasheet limits apply.



| ABSOLUTE MAXIMUM RATINGS $T_A = 25^\circ\text{C}$, unless otherwise noted | | | |
|--|--|------------------|---------------------------|
| Parameter | Limit | Unit | |
| V+ to V- | 14 | V | |
| GND to V- | 7 | | |
| Digital Inputs ^a , V_S , V_D | (V-) - 0.3 to (V+) + 0.3 or 30 mA, whichever occurs first | | |
| Continuous Current (Any terminal) | 30 | mA | |
| Peak Current, S or D (Pulsed 1 ms, 10 % duty cycle) | 100 | | |
| Storage Temperature | - 65 to 150 | $^\circ\text{C}$ | |
| Power Dissipation ^b | 16-Pin TSSOP ^c | 450 | mW |
| | 16-Pin miniQFN ^{d, e} | 525 | |
| Thermal Resistance ^b | 16-Pin TSSOP | 178 | $^\circ\text{C}/\text{W}$ |
| | 16-Pin miniQFN ^e | 152 | |

Notes:

- a. Signals on SX, DX, or INX exceeding V+ or V- will be clamped by internal diodes. Limit forward diode current to maximum current ratings.
- b. All leads welded or soldered to PC board.
- c. Derate 5.6 mW/ $^\circ\text{C}$ above 70 $^\circ\text{C}$.
- d. Derate 6.6 mW/ $^\circ\text{C}$ above 70 $^\circ\text{C}$.
- e. Manual soldering with iron is not recommended for leadless components. The miniQFN-16 is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper lip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection.

| SPECIFICATIONS FOR DUAL SUPPLIES | | | | | | | | | |
|----------------------------------|-----------------|---|--------------------|-------------------|---|-------------------|--|-------------------|---------------|
| Parameter | Symbol | Test Conditions Unless Otherwise Specified $V_{CC} = +5\text{ V}$, $V_{EE} = -5\text{ V}$ $V_{IN(A, B, C \text{ and } ENABLE)} = 2.0\text{ V}$, 0.8 V^a | Temp. ^b | Typ. ^c | - 40 $^\circ\text{C}$ to 125 $^\circ\text{C}$ | | - 40 $^\circ\text{C}$ to 85 $^\circ\text{C}$ | | Unit |
| | | | | | Min. ^d | Max. ^d | Min. ^d | Max. ^d | |
| Analog Switch | | | | | | | | | |
| Analog Signal Range ^e | V_{ANALOG} | | Full | | - 5 | 5 | - 5 | 5 | V |
| On-Resistance | R_{ON} | $I_S = 1\text{ mA}$, $V_D = -3\text{ V}$, 0 V , $+3\text{ V}$ | Room Full | 66 | | 100 125 | | 100 118 | Ω |
| On-Resistance Match | ΔR_{ON} | $I_S = 1\text{ mA}$, $V_D = \pm 3\text{ V}$ | Room Full | 3 | | 6 10 | | 6 8 | |
| On-Resistance Flatness | $R_{FLATNESS}$ | $I_S = 1\text{ mA}$, $V_D = -3\text{ V}$, 0 V , $+3\text{ V}$ | Room Full | 12 | | 16 20 | | 16 18 | |
| Switch Off Leakage Current | $I_{S(off)}$ | $V_+ = 5.5\text{ V}$, $V_- = -5.5\text{ V}$, $V_D = \pm 4.5\text{ V}$, $V_S = \mp 4.5\text{ V}$ | Room Full | ± 0.02 | - 1 - 50 | 1 50 | - 1 - 5 | 1 5 | nA |
| | $I_{D(off)}$ | | Room Full | ± 0.02 | - 1 - 50 | 1 50 | - 1 - 5 | 1 5 | |
| Channel On Leakage Current | $I_{D(on)}$ | $V_+ = 5.5\text{ V}$, $V_- = -5.5\text{ V}$, $V_S = V_D = \pm 4.5\text{ V}$ | Room Full | ± 0.02 | - 1 - 50 | 1 50 | - 1 - 5 | 1 5 | |
| Digital Control | | | | | | | | | |
| Input Current, V_{IN} Low | I_{IL} | $V_{IN(A, B, C \text{ and } ENABLE)}$ under test = 0.8 V | Full | 0.01 | - 1 | 1 | - 1 | 1 | μA |
| Input Current, V_{IN} High | I_{IH} | $V_{IN(A, B, C \text{ and } ENABLE)}$ under test = 2.0 V | Full | 0.01 | - 1 | 1 | - 1 | 1 | |
| Input Capacitance ^e | C_{IN} | $f = 1\text{ MHz}$ | Room | 3.4 | | | | | pF |
| Dynamic Characteristics | | | | | | | | | |
| Off Isolation | OIRR | $R_L = 50\ \Omega$, $C_L = 1\text{ pF}$ | Room | f = 10 MHz | 67 | | | | dB |
| | | | | f = 100 MHz | 46 | | | | |
| Channel-to-Channel Crosstalk | X_{TALK} | | f = 10 MHz | Room | 67 | | | | |
| | | | f = 100 MHz | Room | 47 | | | | |
| Bandwidth, 3 dB | BW | $R_L = 50\ \Omega$ | DG4051A | Room | 330 | | | | MHz |
| | | | DG4052A | Room | 450 | | | | |
| | | | DG4053A | Room | 730 | | | | |

| SPECIFICATIONS FOR DUAL SUPPLIES | | | | | | | | | |
|---|--------------|---|--------------------|-------------------|-------------------|-------------------|-------------------|-------------------|---------------|
| Parameter | Symbol | Test Conditions Unless Otherwise Specified $V_{CC} = +5\text{ V}$, $V_{EE} = -5\text{ V}$ $V_{IN(A, B, C \text{ and } ENABLE)} = 2.0\text{ V}$, 0.8 V^a | Temp. ^b | Typ. ^c | - 40 °C to 125 °C | | - 40 °C to 85 °C | | Unit |
| | | | | | Min. ^d | Max. ^d | Min. ^d | Max. ^d | |
| Dynamic Characteristics | | | | | | | | | |
| Transition Time | t_{TRANS} | $R_L = 300\ \Omega$, $C_L = 35\text{ pF}$ see figure 1, 2, 3 | Room Full | 36 | | 110 127 | | 110 117 | ns |
| Enable Turn-On Time | t_{ON} | | Room Full | 31 | | 108 119 | | 108 114 | |
| Enable Turn-Off Time | t_{OFF} | | Room Full | 29 | | 92 103 | | 92 98 | |
| Break-Before-Make Time Delay | t_D | | Room Full | | 1 | | 1 | | |
| Charge Injection ^e | Q | $V_g = 0\text{ V}$, $R_g = 0\ \Omega$, $C_L = 1\text{ nF}$ | Room | 0.25 | | | | | pC |
| Off Isolation ^e | OIRR | $R_L = 50\ \Omega$, $C_L = 1\text{ pF}$ $f = 100\text{ kHz}$ | Room | < - 90 | | | | | dB |
| Channel-to-Channel Crosstalk ^e | X_{TALK} | | Room | < - 90 | | | | | |
| Source Off Capacitance ^e | $C_{S(off)}$ | $f = 1\text{ MHz}$ | DG4051A | Room | 3 | | | | pF |
| | | | DG4052A | Room | 3 | | | | |
| | | | DG4053A | Room | 3 | | | | |
| Drain Off Capacitance ^e | $C_{D(off)}$ | $f = 1\text{ MHz}$ | DG4051A | Room | 12 | | | | |
| | | | DG4052A | Room | 7 | | | | |
| | | | DG4053A | Room | 4 | | | | |
| Channel On Capacitance ^e | $C_{D(on)}$ | $f = 1\text{ MHz}$ | DG4051A | Room | 17 | | | | |
| | | | DG4052A | Room | 13 | | | | |
| | | | DG4053A | Room | 11 | | | | |
| Total Harmonic Distortion ^e | THD | Signal = 5 V_{RMS} , 20 Hz to 20 kHz, $R_L = 600\ \Omega$ | Room | 0.28 | | | | | % |
| Power Supplies | | | | | | | | | |
| Power Supply Current | I+ | $V_{CC} = +5\text{ V}$, $V_{EE} = -5\text{ V}$ $V_{IN(A, B, C \text{ and } ENABLE)} = 0\text{ or }5\text{ V}$ | Room Full | 0.05 | | 1 10 | | 1 10 | μA |
| Negative Supply Current | I- | | Room Full | - 0.05 | - 1 - 10 | | - 1 - 10 | | |
| Ground Current | I_{GND} | | Room Full | - 0.05 | - 1 - 10 | | - 1 - 10 | | |



| SPECIFICATIONS FOR UNIPOLAR SUPPLIES | | | | | | | | | |
|---|-----------------|--|--------------------|-------------------|-------------------|-------------------|-------------------|-------------------|------|
| Parameter | Symbol | Test Conditions Unless Otherwise Specified $V_{CC} = +5\text{ V}$, $V_{EE} = 0\text{ V}$ $V_{IN(A, B, C \text{ and } ENABLE)} = 2.0\text{ V}$, 0.8 V^a | Temp. ^b | Typ. ^c | - 40 °C to 125 °C | | - 40 °C to 85 °C | | Unit |
| | | | | | Min. ^d | Max. ^d | Min. ^d | Max. ^d | |
| Analog Switch | | | | | | | | | |
| Analog Signal Range ^e | V_{ANALOG} | | Full | | 0 | 5 | 0 | 5 | V |
| On-Resistance | R_{ON} | $I_S = 1\text{ mA}$, $V_D = 0\text{ V}$, $+3.5\text{ V}$ | Room Full | 107 | | 165 205 | | 165 194 | Ω |
| On-Resistance Match | ΔR_{ON} | $I_S = 1\text{ mA}$, $V_D = +3.5\text{ V}$ | Room Full | 3.2 | | 8 13 | | 8 11 | |
| On-Resistance Flatness | $R_{FLATNESS}$ | $I_S = 1\text{ mA}$, $V_D = 0\text{ V}$, $+3\text{ V}$ | Room Full | 19 | | 26 30 | | 26 28 | |
| Switch Off Leakage Current | $I_{S(off)}$ | $V_+ = +5.5\text{ V}$, $V_- = 0\text{ V}$ $V_D = 1\text{ V}/4.5\text{ V}$, $V_S = 4.5\text{ V}/1\text{ V}$ | Room Full | ± 0.02 | - 1 - 50 | 1 50 | - 1 - 5 | 1 5 | nA |
| | $I_{D(off)}$ | | Room Full | ± 0.02 | - 1 - 50 | 1 50 | - 1 - 5 | 1 5 | |
| Channel On Leakage Current | $I_{D(on)}$ | $V_+ = +5.5\text{ V}$, $V_- = 0\text{ V}$ $V_D = V_S = 1\text{ V}/4.5\text{ V}$ | Room Full | ± 0.02 | - 1 - 50 | 1 50 | - 1 - 5 | 1 5 | |
| Digital Control | | | | | | | | | |
| Input Current, V_{IN} Low | I_L | $V_{IN(A, B, C \text{ and } ENABLE)}$ under test = 0.8 V | Full | 0.01 | - 1 | 1 | - 1 | 1 | μA |
| Input Current, V_{IN} High | I_H | $V_{IN(A, B, C \text{ and } ENABLE)}$ under test = 2.0 V | Full | 0.01 | - 1 | 1 | - 1 | 1 | |
| Dynamic Characteristics | | | | | | | | | |
| Transition Time | t_{TRANS} | $R_L = 300\ \Omega$, $C_L = 35\text{ pF}$ See Figure 1, 2, 3 | Room Full | 38 | | 121 143 | | 121 134 | ns |
| Enable Turn-On Time | t_{ON} | | Room Full | 38 | | 110 126 | | 110 119 | |
| Enable Turn-Off Time | t_{OFF} | | Room Full | 38 | | 103 118 | | 103 111 | |
| Break-Before-Make Time Delay | t_D | | Room Full | | 1 | | 1 | | |
| Charge Injection ^e | Q | $V_g = 0\text{ V}$, $R_g = 0\ \Omega$, $C_L = 1\text{ nF}$ | Full | 0.5 | | | | | pC |
| Off Isolation ^e | OIRR | $R_L = 50\ \Omega$, $C_L = 1\text{ pF}$ $f = 100\text{ kHz}$ | Room | < - 90 | | | | | dB |
| Channel-to-Channel Crosstalk ^e | X_{TALK} | | Room | < - 90 | | | | | |
| Source Off Capacitance ^e | $C_{S(off)}$ | $f = 1\text{ MHz}$ | DG4051A | Room | 3 | | | | pF |
| | | | DG4052A | Room | 3 | | | | |
| | | | DG4053A | Room | 4 | | | | |
| Drain Off Capacitance ^e | $C_{D(off)}$ | $f = 1\text{ MHz}$ | DG4051A | Room | 13 | | | | |
| | | | DG4052A | Room | 8 | | | | |
| | | | DG4053A | Room | 5 | | | | |
| Channel On Capacitance ^e | $C_{D(on)}$ | $f = 1\text{ MHz}$ | DG4051A | Room | 18 | | | | |
| | | | DG4052A | Room | 14 | | | | |
| | | | DG4053A | Room | 11 | | | | |
| Power Supplies | | | | | | | | | |
| Power Supply Current | I_+ | $V_{IN(A, B, C \text{ and } ENABLE)} = 0\text{ V}$ or 5 V | Room Full | 0.05 | | 1 10 | | 1 10 | μA |
| Negative Supply Current | I_- | | Room Full | - 0.05 | - 1 - 10 | | - 1 - 10 | | |
| Ground Current | I_{GND} | | Room Full | - 0.05 | - 1 - 10 | | - 1 - 10 | | |

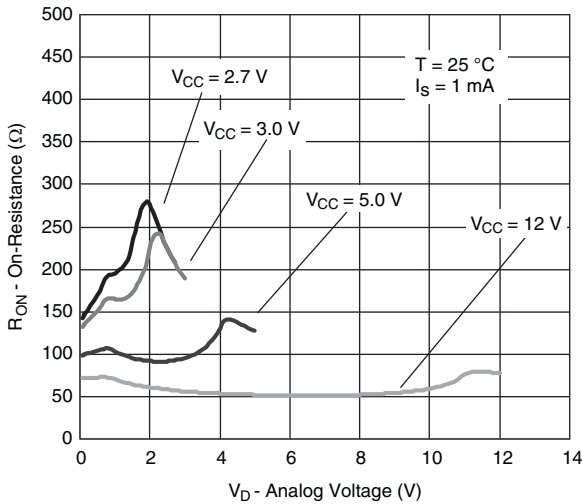
| SPECIFICATIONS FOR UNIPOLAR SUPPLIES | | | | | | | | | | |
|---|--------------|--|--------------|--------------------|-------------------|-------------------|-------------------|-------------------|-------------------|------|
| Parameter | Symbol | Test Conditions Unless Otherwise Specified $V_{CC} = +3\text{ V}$, $V_{EE} = 0\text{ V}$ $V_{IN(A, B, C \text{ and } ENABLE)} = 1.4\text{ V}$, 0.6 V^a | | Temp. ^b | Typ. ^c | - 40 °C to 125 °C | | - 40 °C to 85 °C | | Unit |
| | | | | | | Min. ^d | Max. ^d | Min. ^d | Max. ^d | |
| Analog Switch | | | | | | | | | | |
| Analog Signal Range ^e | V_{ANALOG} | | Full | | 0 | 3 | 0 | 3 | V | |
| On-Resistance | R_{ON} | $I_S = 1\text{ mA}$, $V_D = 1.5\text{ V}$ | Room Full | 175 | | 265 310 | | 265 298 | Ω | |
| Switch Off Leakage Current | $I_{S(off)}$ | $V_+ = +3.3\text{ V}$, $V_- = 0\text{ V}$ $V_D = 0.3\text{ V}/3.0\text{ V}$, $V_S = 3.0\text{ V}/0.3\text{ V}$ | Room Full | ± 0.02 | - 1 - 50 | 1 50 | - 1 - 5 | 1 5 | nA | |
| | $I_{D(off)}$ | | Room Full | ± 0.02 | - 1 - 50 | 1 50 | - 1 - 5 | 1 5 | | |
| Channel On Leakage Current | $I_{D(on)}$ | $V_+ = +3.3\text{ V}$, $V_- = 0\text{ V}$ $V_D = V_S = 0.3\text{ V}/3.0\text{ V}$ | Room Full | ± 0.02 | - 1 - 50 | 1 50 | - 1 - 5 | 1 5 | | |
| Digital Control | | | | | | | | | | |
| Input Current, V_{IN} Low | I_L | $V_{IN(A, B, C \text{ and } ENABLE)}$ under test = 0.6 V | Full | 0.01 | - 1 | 1 | - 1 | 1 | μA | |
| Input Current, V_{IN} High | I_H | $V_{IN(A, B, C \text{ and } ENABLE)}$ under test = 1.4 V | Full | 0.01 | - 1 | 1 | - 1 | 1 | | |
| Dynamic Characteristics | | | | | | | | | | |
| Transition Time | t_{TRANS} | $R_L = 300\ \Omega$, $C_L = 35\text{ pF}$ see figure 1, 2, 3 | Room Full | 81 | | 172 218 | | 172 194 | ns | |
| Enable Turn-On Time | t_{ON} | | Room Full | 71 | | 151 183 | | 151 167 | | |
| Enable Turn-Off Time | t_{OFF} | | Room Full | 69 | | 138 161 | | 138 151 | | |
| Break-Before-Make Time Delay | t_D | | Room Full | | 1 | | 1 | | | |
| Charge Injection ^e | Q | $V_g = 0\text{ V}$, $R_g = 0\ \Omega$, $C_L = 1\text{ nF}$ | Room | 0.5 | | | | | pC | |
| Off Isolation ^e | OIRR | $R_L = 50\ \Omega$, $C_L = 1\text{ pF}$ $f = 100\text{ kHz}$ | Room | < - 90 | | | | | dB | |
| Channel-to-Channel Crosstalk ^e | X_{TALK} | | Room | < - 90 | | | | | | |
| Source Off Capacitance ^e | $C_{S(off)}$ | $f = 1\text{ MHz}$ | DG4051A | Room | 4 | | | | pF | |
| | | | DG4052A | Room | 3 | | | | | |
| | | | DG4053A | Room | 4 | | | | | |
| Drain Off Capacitance ^e | $C_{D(off)}$ | $f = 1\text{ MHz}$ | DG4051A | Room | 14 | | | | | |
| | | | DG4052A | Room | 8 | | | | | |
| | | | DG4053A | Room | 5 | | | | | |
| Channel On Capacitance ^e | $C_{D(on)}$ | $f = 1\text{ MHz}$ | DG4051A | Room | 19 | | | | | |
| | | | DG4052A | Room | 14 | | | | | |
| | | | DG4053A | Room | 11 | | | | | |
| Power Supplies | | | | | | | | | | |
| Power Supply Current | I_+ | $V_{IN(A, B, C \text{ and } ENABLE)} = 0\text{ V}$ or 3 V | Room Full | 0.05 | | 1 10 | | 1 10 | μA | |
| Negative Supply Current | I_- | | Room Full | - 0.05 | - 1 - 10 | | - 1 - 10 | | | |
| Ground Current | I_{GND} | | Room Full | - 0.05 | - 1 - 10 | | - 1 - 10 | | | |

Notes:

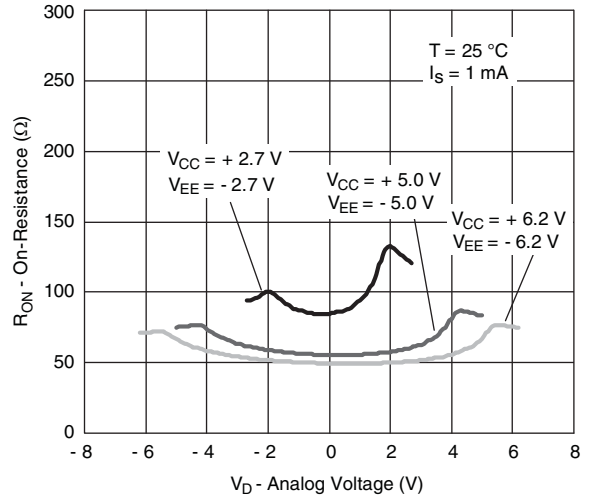
- a. V_{IN} = input voltage to perform proper function.
- b. Room = 25 °C, Full = as determined by the operating temperature suffix.
- c. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
- d. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
- e. Guaranteed by design, not subject to production test.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

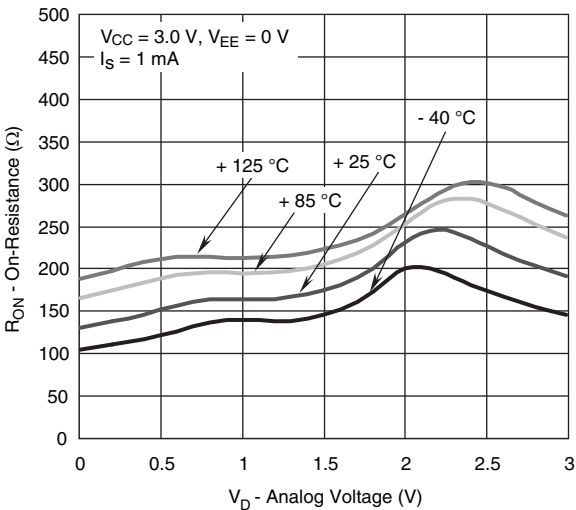
TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



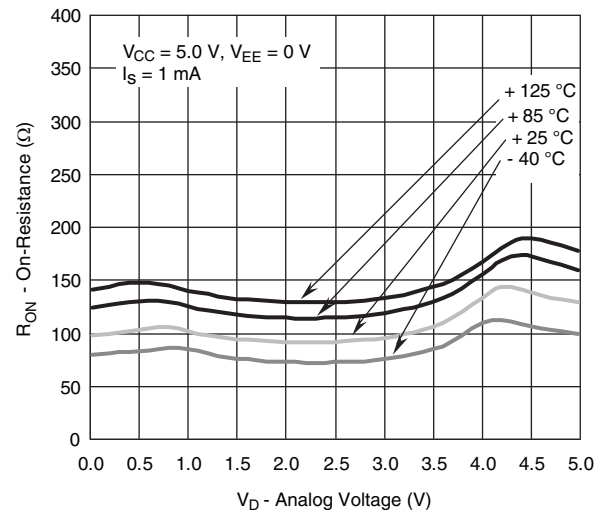
On-Resistance vs. V_D and Single Supply Voltage



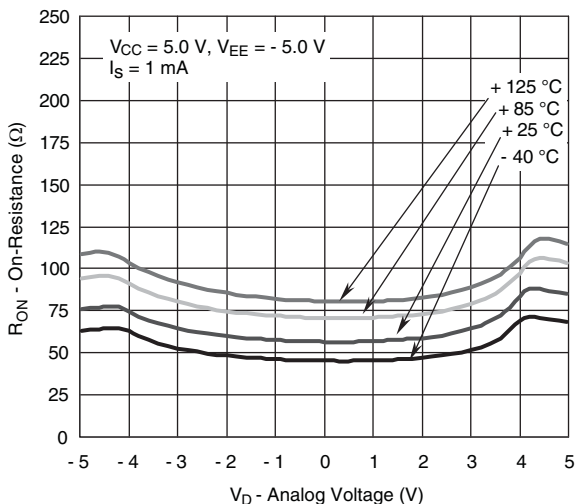
On-Resistance vs. V_D and Dual Supply Voltage



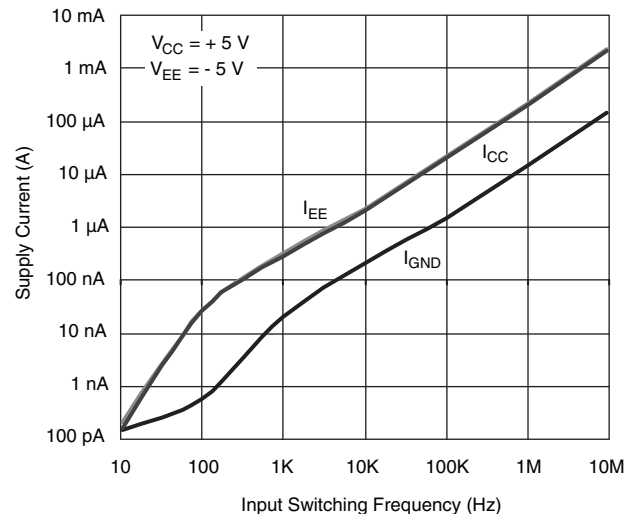
On-Resistance vs. Analog Voltage and Temperature at $V_{CC} = +3$ V, $V_{EE} = 0$ V



On-Resistance vs. Analog Voltage and Temperature at $V_{CC} = +5$ V, $V_{EE} = 0$ V

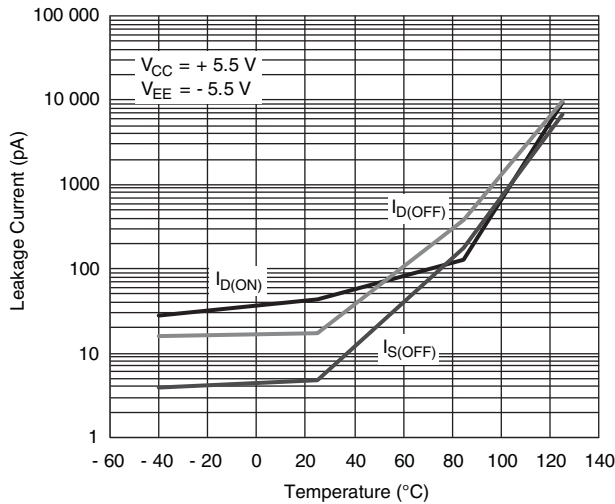


On-Resistance vs. Analog Voltage and Temperature at $V_{CC} = +5$ V, $V_{EE} = -5$ V

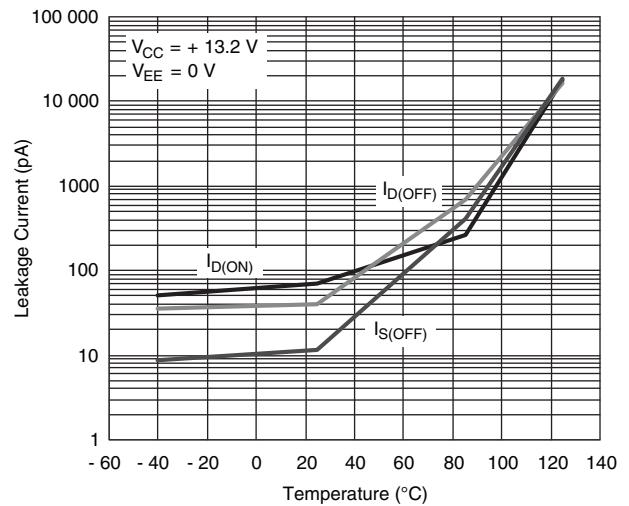


Supply Current vs. Input Switching Frequency

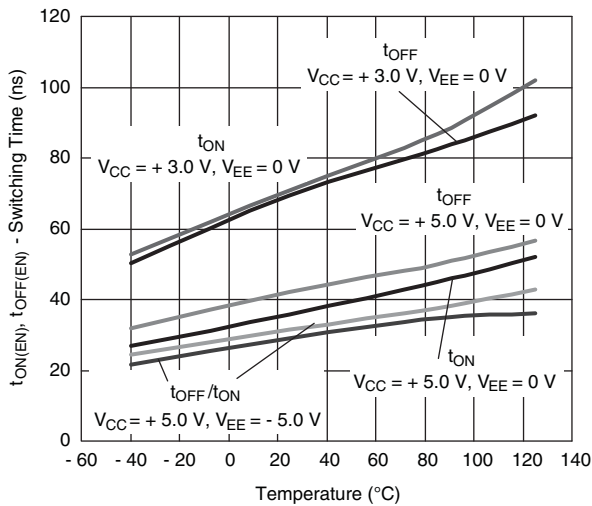
TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



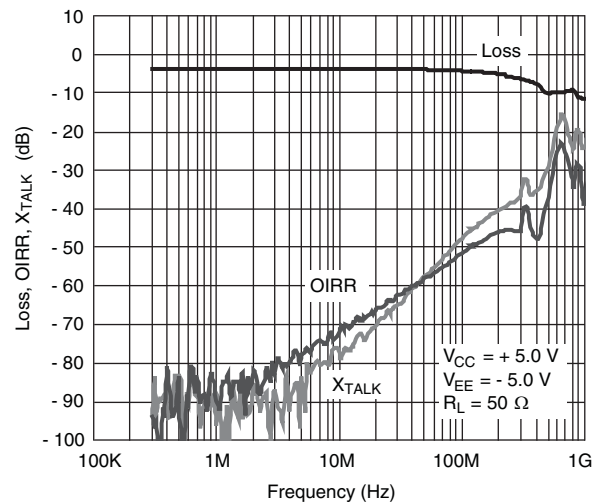
Leakage Current vs. Temperature



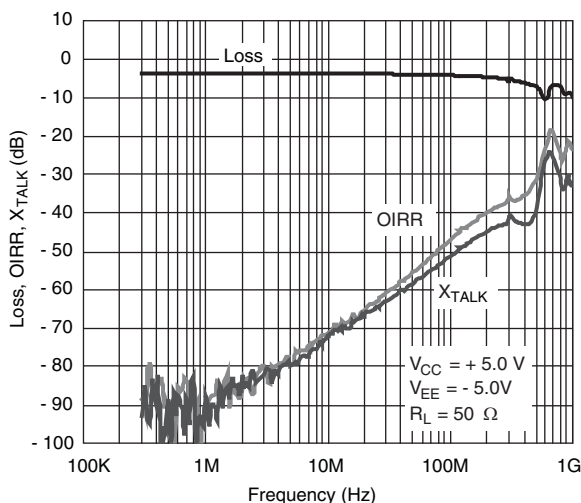
Leakage Current vs. Temperature



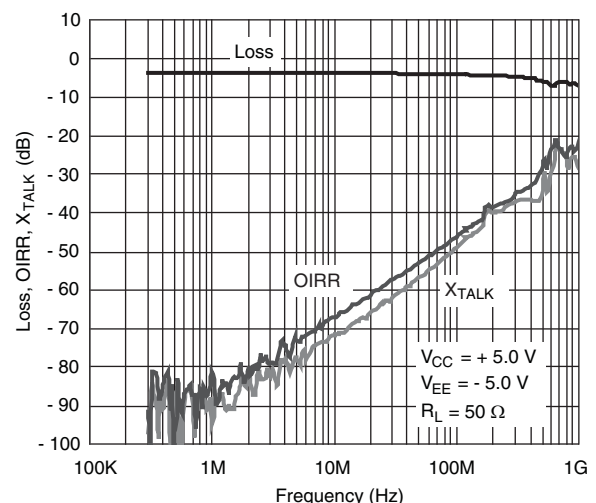
Switching Time vs. Temperature



DG4051A Insertion Loss, Off-Isolation, Crosstalk vs. Frequency at ± 5 V Supply

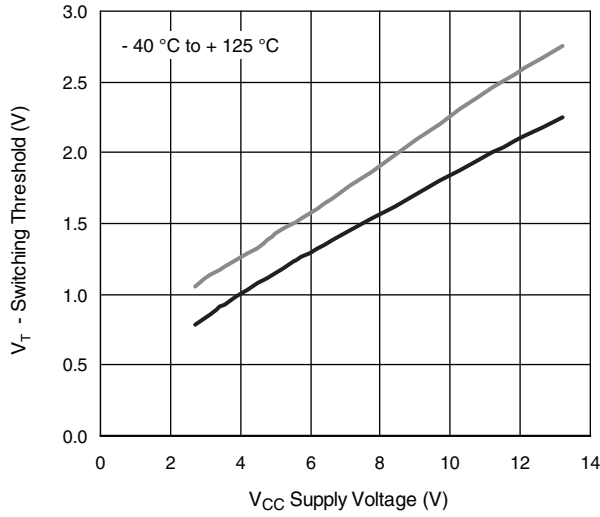


DG4052A Insertion Loss, Off-Isolation, Crosstalk vs. Frequency at ± 5 V Supply

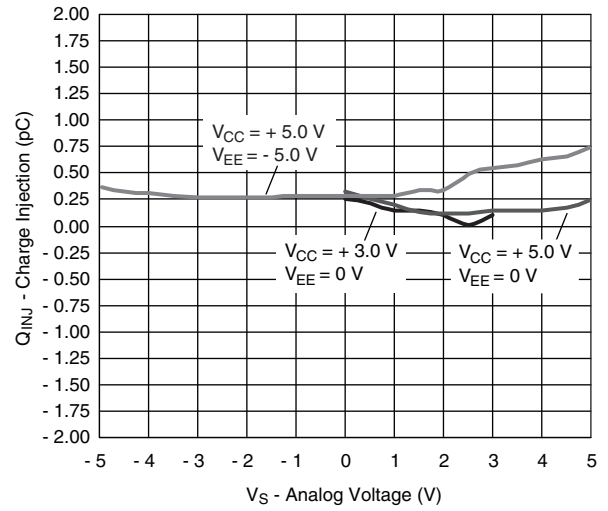


DG4053A Insertion Loss, Off-Isolation, Crosstalk vs. Frequency at ± 5 V Supply

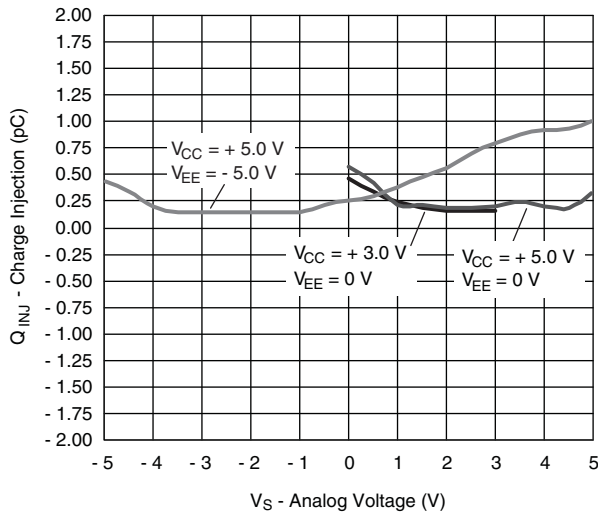
TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



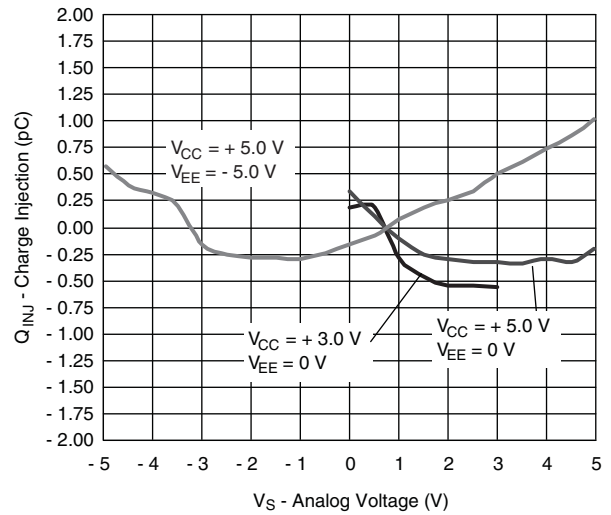
Switching Threshold vs. V_{CC} Supply Voltage



DG4051A Charge Injection vs. Analog Voltage



DG4052A Charge Injection vs. Analog Voltage



DG4053A Charge Injection vs. Analog Voltage

TEST CIRCUITS

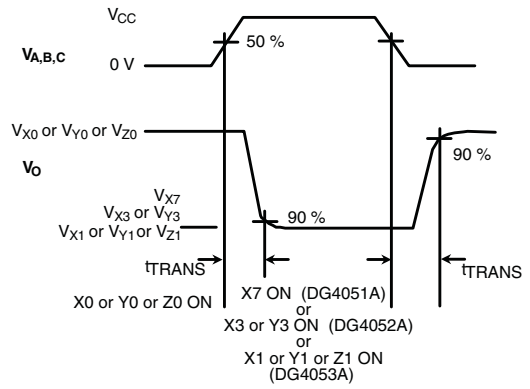
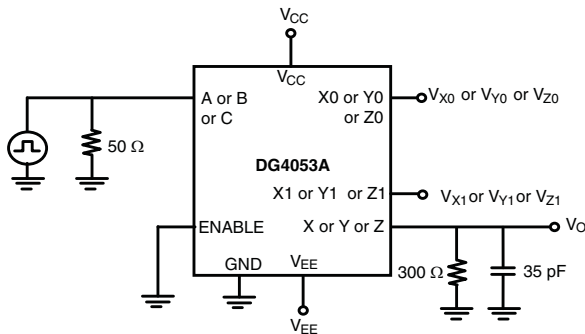
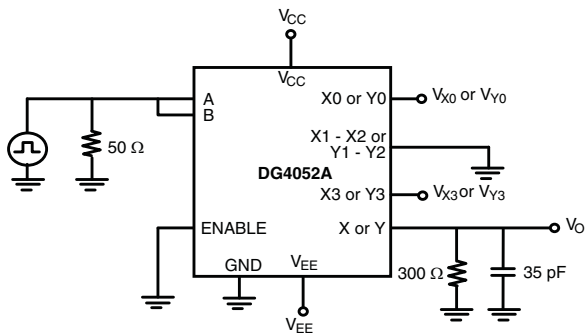
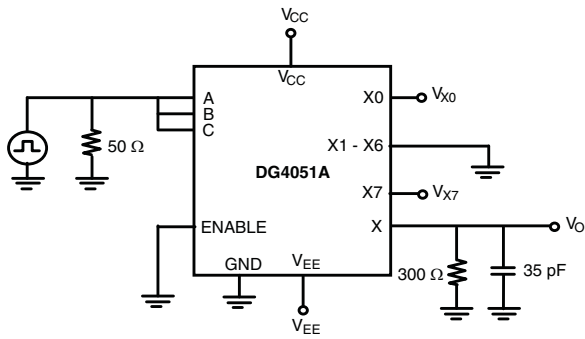


Figure 1. Transition Time

TEST CIRCUITS

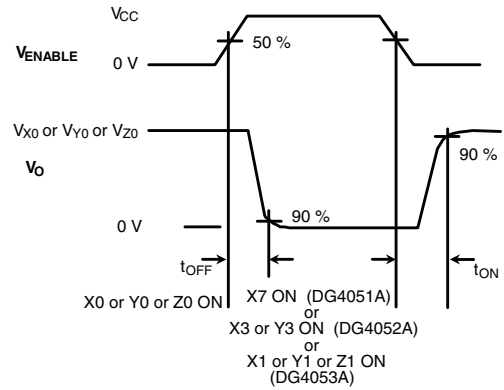
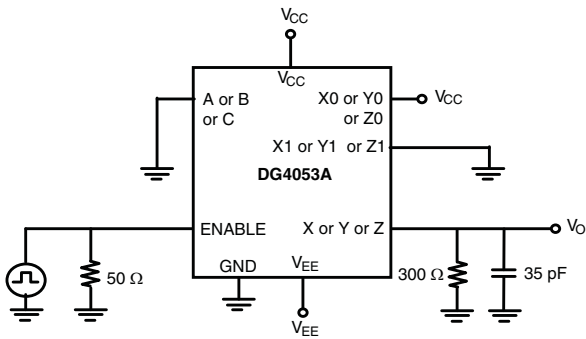
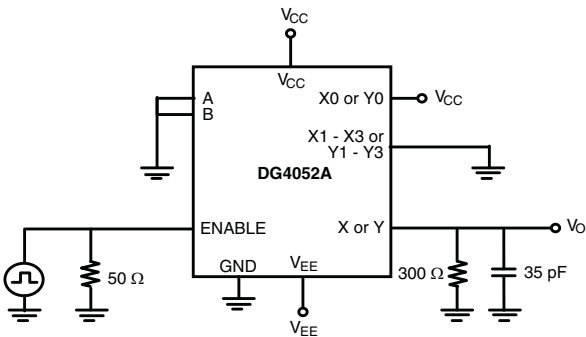
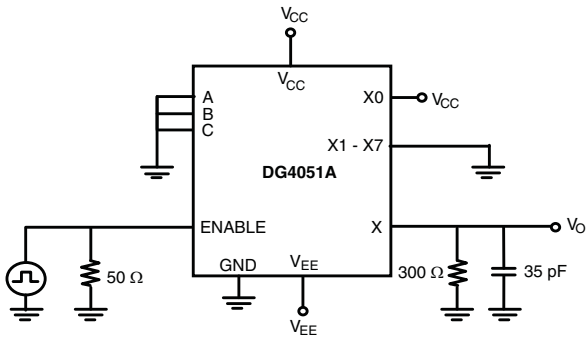


Figure 2. Enable Switching Time

TEST CIRCUITS

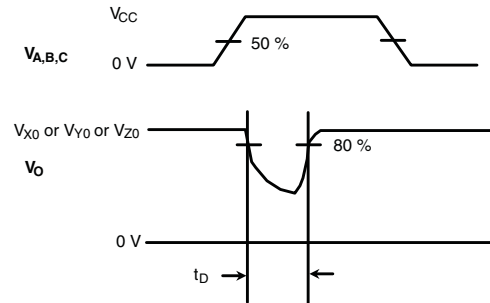
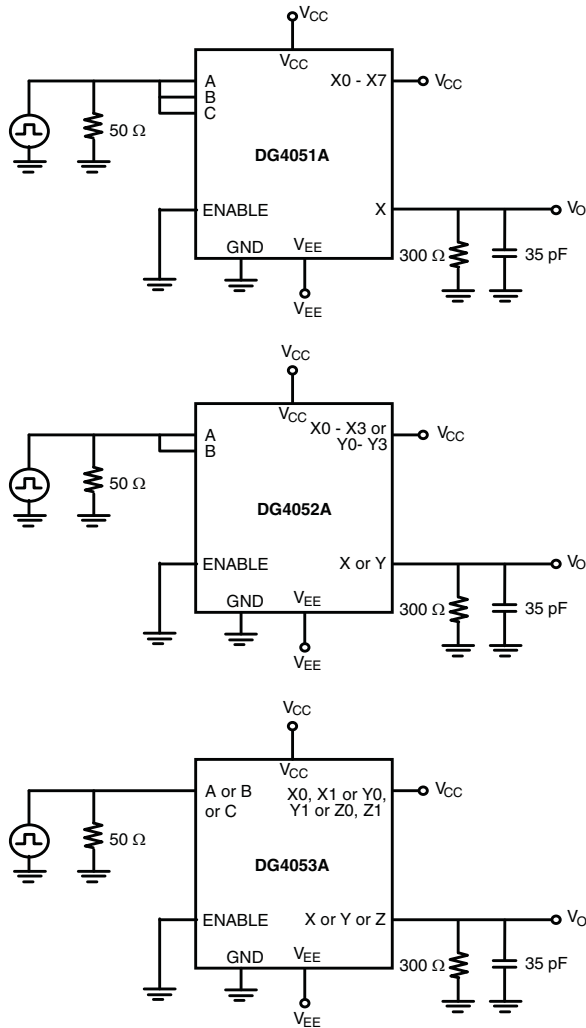


Figure 3. Break-Before-Make

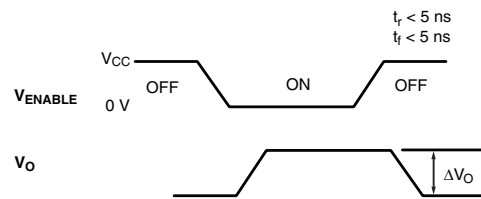
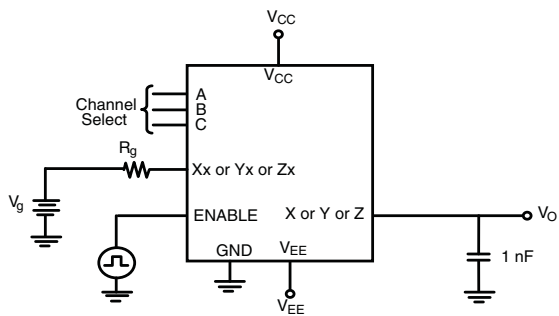
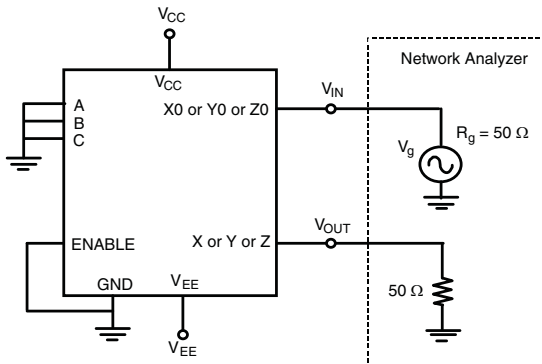


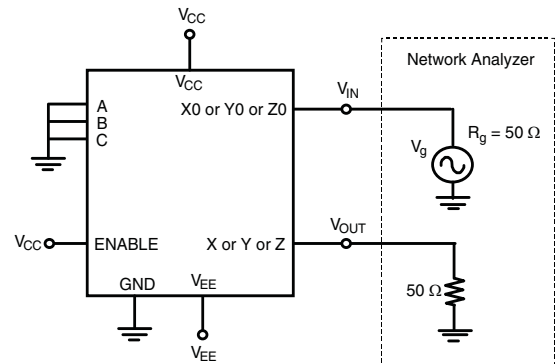
Figure 4. Charge Injection

TEST CIRCUITS



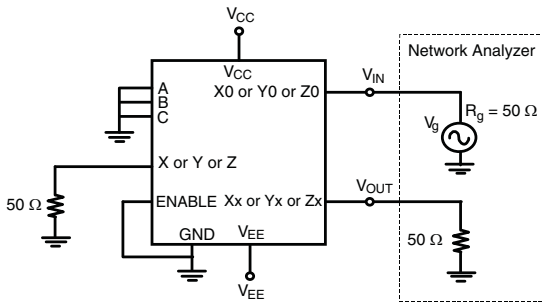
$$\text{Insertion Loss} = 20 \log \frac{V_{\text{OUT}}}{V_{\text{IN}}}$$

Figure 5. Insertion Loss



$$\text{Off Isolation} = 20 \log \frac{V_{\text{OUT}}}{V_{\text{IN}}}$$

Figure 6. Off Isolation



$$\text{Crosstalk} = 20 \log \frac{V_{\text{OUT}}}{V_{\text{IN}}}$$

Figure 7. Crosstalk

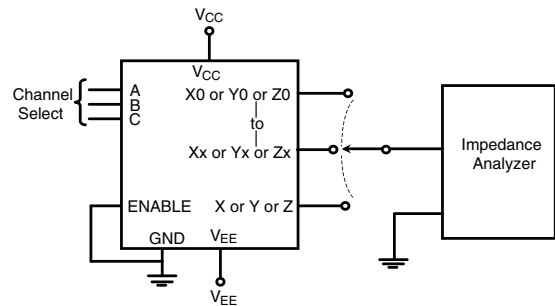
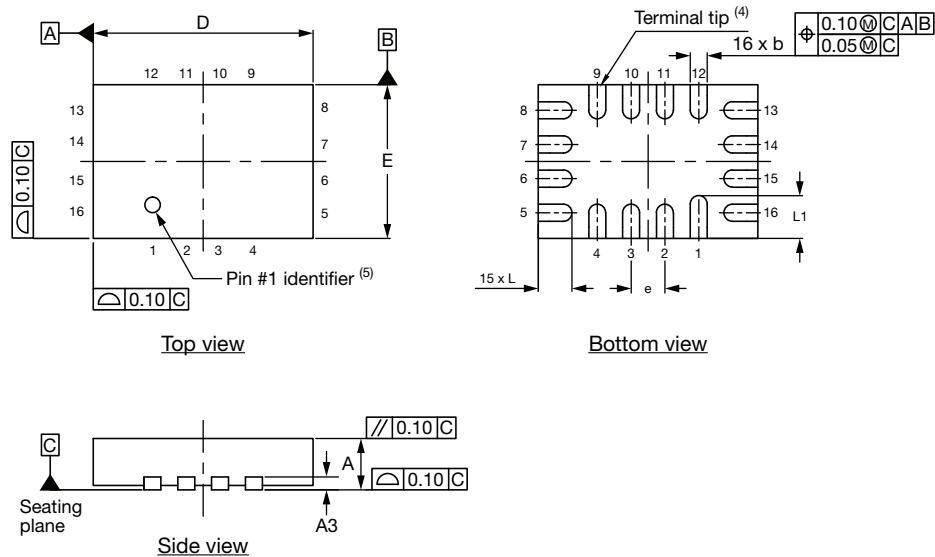


Figure 8. Source, Drain Capacitance

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Thin miniQFN16 Case Outline



| DIMENSIONS | MILLIMETERS ⁽¹⁾ | | | INCHES | | |
|-------------------|----------------------------|------|------|------------|-------|-------|
| | MIN. | NOM. | MAX. | MIN. | NOM. | MAX. |
| A | 0.50 | 0.55 | 0.60 | 0.020 | 0.022 | 0.024 |
| A1 | 0 | - | 0.05 | 0 | - | 0.002 |
| A3 | 0.15 ref. | | | 0.006 ref. | | |
| b | 0.15 | 0.20 | 0.25 | 0.006 | 0.008 | 0.010 |
| D | 2.50 | 2.60 | 2.70 | 0.098 | 0.102 | 0.106 |
| e | 0.40 BSC | | | 0.016 BSC | | |
| E | 1.70 | 1.80 | 1.90 | 0.067 | 0.071 | 0.075 |
| L | 0.35 | 0.40 | 0.45 | 0.014 | 0.016 | 0.018 |
| L1 | 0.45 | 0.50 | 0.55 | 0.018 | 0.020 | 0.022 |
| N ⁽³⁾ | 16 | | | 16 | | |
| Nd ⁽³⁾ | 4 | | | 4 | | |
| Ne ⁽³⁾ | 4 | | | 4 | | |

Notes

- (1) Use millimeters as the primary measurement.
- (2) Dimensioning and tolerances conform to ASME Y14.5M. - 1994.
- (3) N is the number of terminals. Nd and Ne is the number of terminals in each D and E site respectively.
- (4) Dimensions b applies to plated terminal and is measured between 0.15 mm and 0.30 mm from terminal tip.
- (5) The pin 1 identifier must be existed on the top surface of the package by using identification mark or other feature of package body.
- (6) Package warpage max. 0.05 mm.

ECN: T16-0226-Rev. B, 09-May-16
DWG: 6023

TSSOP: 16-LEAD



| Symbols | DIMENSIONS IN MILLIMETERS | | |
|---------|---------------------------|-------|------|
| | Min | Nom | Max |
| A | - | 1.10 | 1.20 |
| A1 | 0.05 | 0.10 | 0.15 |
| A2 | - | 1.00 | 1.05 |
| B | 0.22 | 0.28 | 0.38 |
| C | - | 0.127 | - |
| D | 4.90 | 5.00 | 5.10 |
| E | 6.10 | 6.40 | 6.70 |
| E1 | 4.30 | 4.40 | 4.50 |
| e | - | 0.65 | - |
| L | 0.50 | 0.60 | 0.70 |
| L1 | 0.90 | 1.00 | 1.10 |
| y | - | - | 0.10 |
| θ1 | 0° | 3° | 6° |

ECN: S-61920-Rev. D, 23-Oct-06
DWG: 5624



RECOMMENDED MINIMUM PAD FOR TSSOP-16



Recommended Minimum Pads
Dimensions in inches (mm)

RECOMMENDED MINIMUM PADS FOR MINI QFN 16L



Mounting Footprint
Dimensions in mm (inch)



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