

# RQJ0203WGDQA

Silicon P Channel MOS FET  
Power Switching

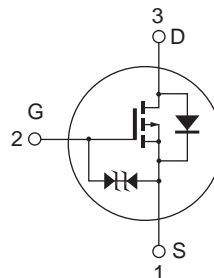
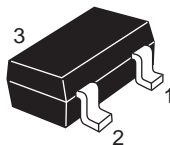
R07DS0292EJ0400  
(Previous: REJ03G1319-0300)  
Rev.4.00  
Mar 28, 2011

## Features

- Low on-resistance  
 $R_{DS(on)} = 142 \text{ m}\Omega$  typ ( $V_{GS} = -4.5 \text{ V}$ ,  $I_D = -1.1 \text{ A}$ )
- Low drive current
- High speed switching
- 2.5 V gate drive

## Outline

RENESAS Package code: PLSP0003ZB-A  
(Package name: MPAK)



1. Source
2. Gate
3. Drain

Note: Marking is "WG".

## Absolute Maximum Ratings

( $T_a = 25^\circ\text{C}$ )

Item	Symbol	Ratings	Unit
Drain to source voltage	$V_{DSS}$	-20	V
Gate to source voltage	$V_{GSS}$	+8 / -12	V
Drain current	$I_D$	-2.1	A
Drain peak current	$I_{D(pulse)}$ <sup>Note1</sup>	-6.0	A
Body - drain diode reverse drain current	$I_{DR}$	-2.1	A
Channel dissipation	$P_{ch}$ <sup>Note2</sup>	0.8	W
Channel temperature	$T_{ch}$	150	$^\circ\text{C}$
Storage temperature	$T_{stg}$	-55 to +150	$^\circ\text{C}$

Notes: 1.  $PW \leq 10 \mu\text{s}$ , duty cycle  $\leq 1\%$

2. When using the glass epoxy board (FR-4: 40 x 40 x 1 mm)

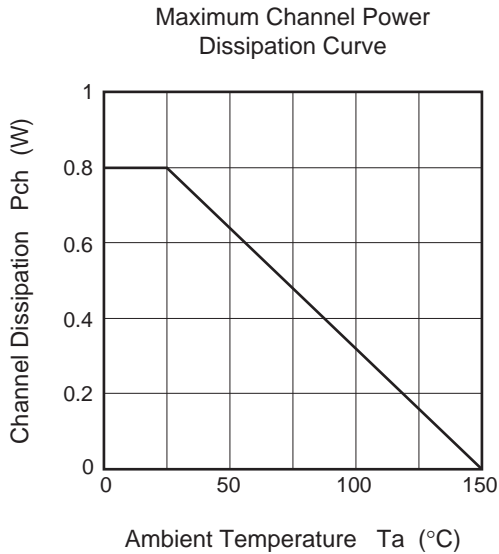
## Electrical Characteristics

(Ta = 25°C)

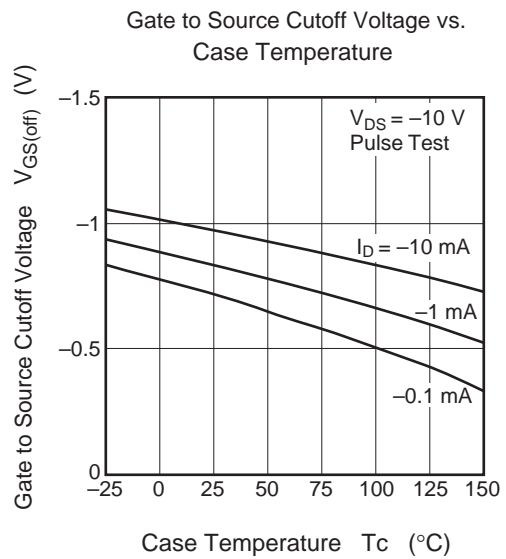
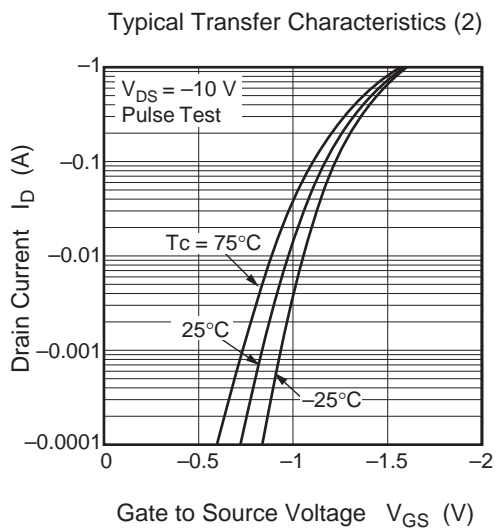
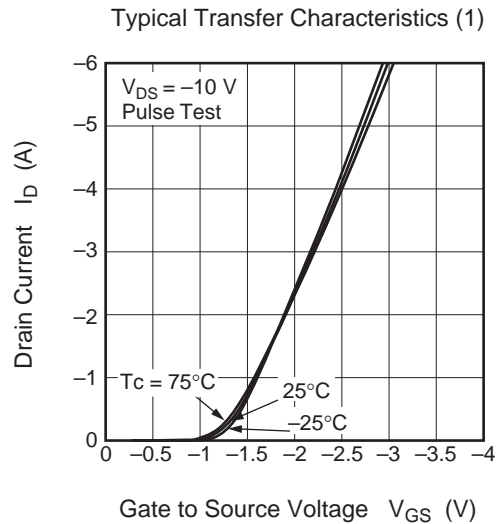
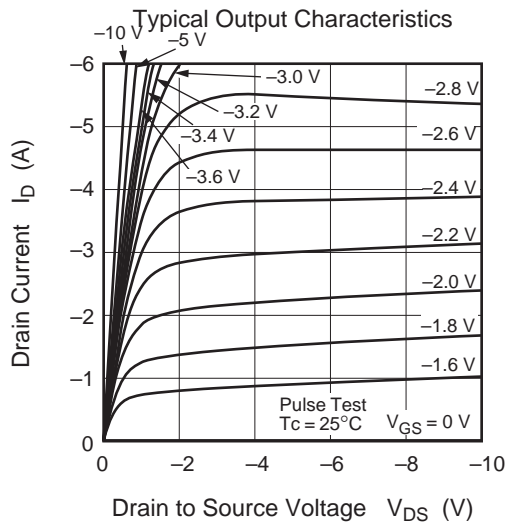
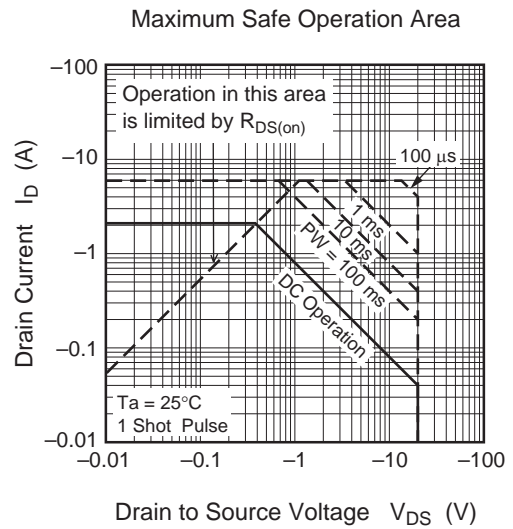
Item	Symbol	Min	Typ	Max	Unit	Test conditions
Drain to source breakdown voltage	$V_{(BR)DSS}$	-20	—	—	V	$I_D = -10 \text{ mA}$ , $V_{GS} = 0$
Gate to source breakdown voltage	$V_{(BR)GSS}$	+8	—	—	V	$I_G = +100 \text{ } \mu\text{A}$ , $V_{DS} = 0$
	$V_{(BR)GSS}$	-12	—	—	V	$I_G = -100 \text{ } \mu\text{A}$ , $V_{DS} = 0$
Gate to source leak current	$I_{GSS}$	—	—	+10	$\mu\text{A}$	$V_{GS} = +6 \text{ V}$ , $V_{DS} = 0$
	$I_{GSS}$	—	—	-10	$\mu\text{A}$	$V_{GS} = -10 \text{ V}$ , $V_{DS} = 0$
Drain to source leak current	$I_{DSS}$	—	—	-1	$\mu\text{A}$	$V_{DS} = -20 \text{ V}$ , $V_{GS} = 0$
Gate to source cutoff voltage	$V_{GS(off)}$	-0.4	—	-1.4	V	$V_{DS} = -10 \text{ V}$ , $I_D = -1 \text{ mA}$
Drain to source on state resistance	$R_{DS(on)}$	—	142	180	$\text{m}\Omega$	$I_D = -1.1 \text{ A}$ , $V_{GS} = -4.5 \text{ V}^{\text{Note3}}$
	$R_{DS(on)}$	—	216	300	$\text{m}\Omega$	$I_D = -1.1 \text{ A}$ , $V_{GS} = -2.5 \text{ V}^{\text{Note3}}$
Forward transfer admittance	$ y_{fs} $	2.0	2.8	—	S	$I_D = -1.1 \text{ A}$ , $V_{DS} = -10 \text{ V}^{\text{Note3}}$
Input capacitance	$C_{iss}$	—	205	—	pF	$V_{DS} = -10 \text{ V}$
Output capacitance	$C_{oss}$	—	57	—	pF	$V_{GS} = 0$
Reverse transfer capacitance	$C_{rss}$	—	39	—	pF	$f = 1 \text{ MHz}$
Turn - on delay time	$t_{d(on)}$	—	14	—	ns	$I_D = -1.1 \text{ A}$
Rise time	$t_r$	—	36	—	ns	$V_{GS} = -4.5 \text{ V}$
Turn - off delay time	$t_{d(off)}$	—	29	—	ns	$R_L = 9 \text{ } \Omega$
Fall time	$t_f$	—	9	—	ns	$R_g = 4.7 \text{ } \Omega$
Total gate charge	$Q_g$	—	2.6	—	nC	$V_{DD} = -10 \text{ V}$
Gate to source charge	$Q_{gs}$	—	0.4	—	nC	$V_{GS} = -4.5 \text{ V}$
Gate to drain charge	$Q_{gd}$	—	1.1	—	nC	$I_D = -2.1 \text{ A}$
Body - drain diode forward voltage	$V_{DF}$	—	-0.85	-1.1	V	$I_F = -2.1 \text{ A}$ , $V_{GS} = 0^{\text{Note3}}$

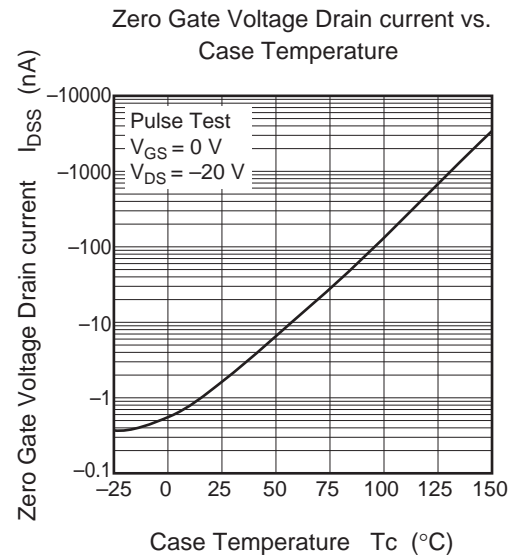
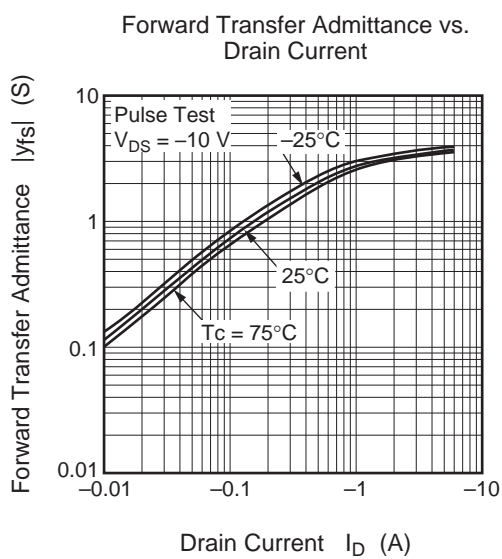
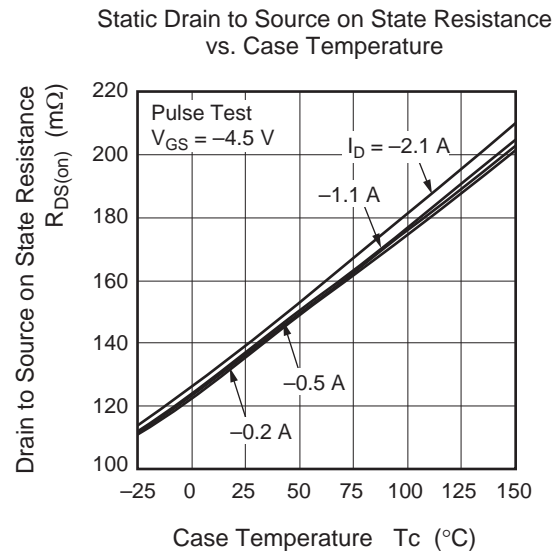
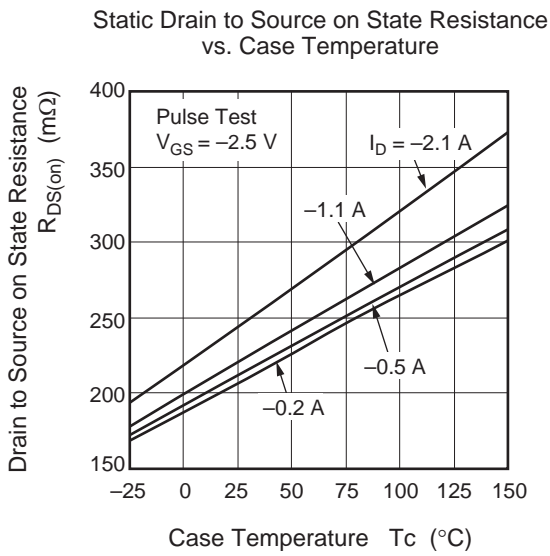
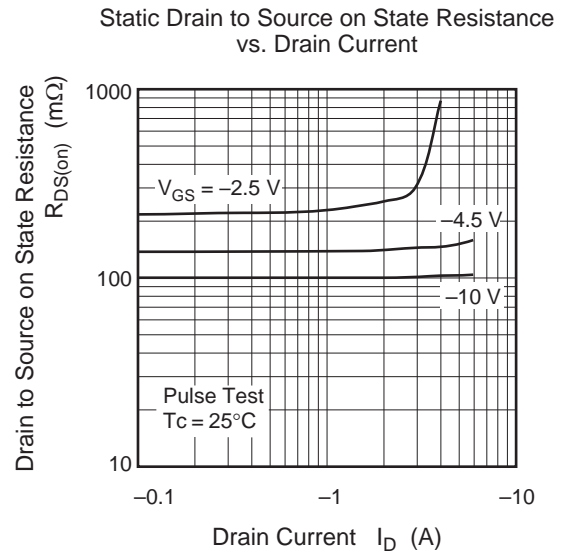
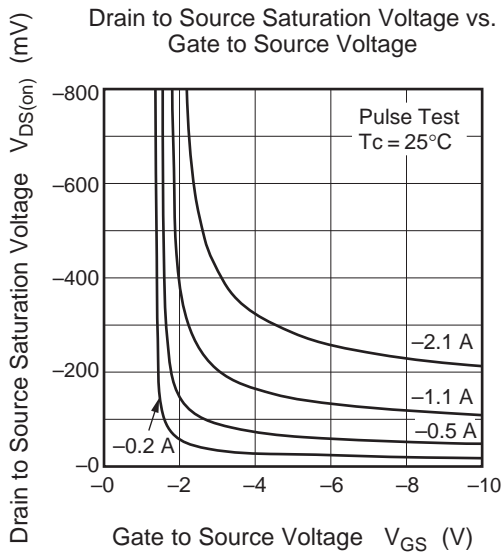
Notes: 3. Pulse test

Main Characteristics

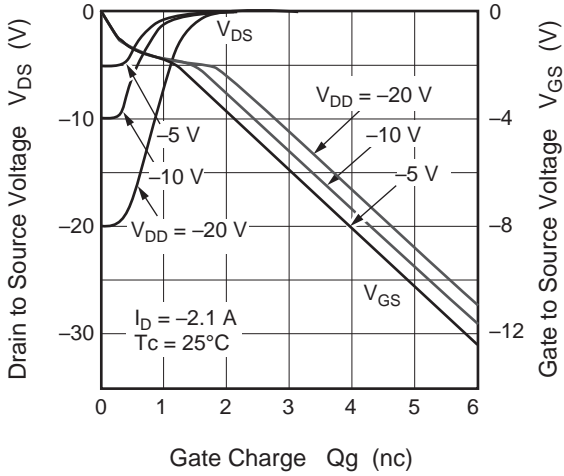


\*When using the glass epoxy board (FR-4: 40 × 40 × 1 mm)

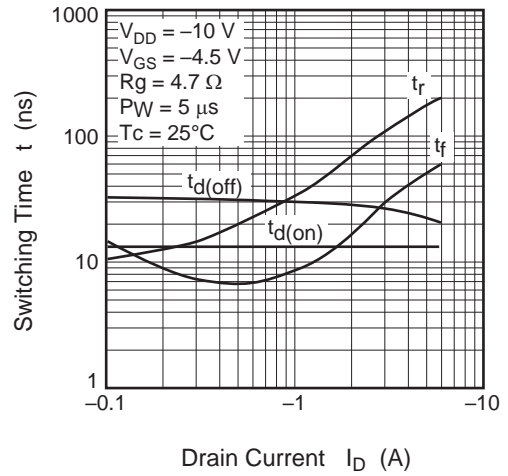




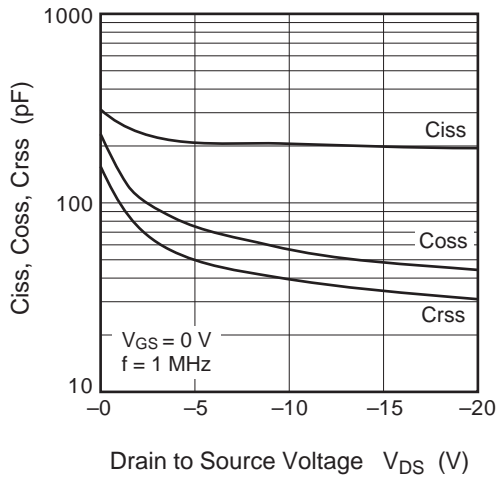
Dynamic Input Characteristics



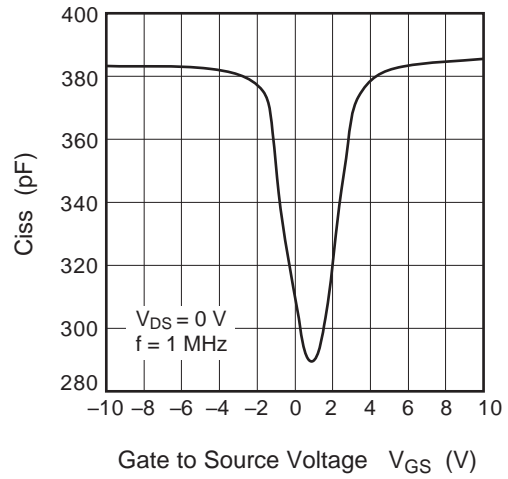
Switching Characteristics



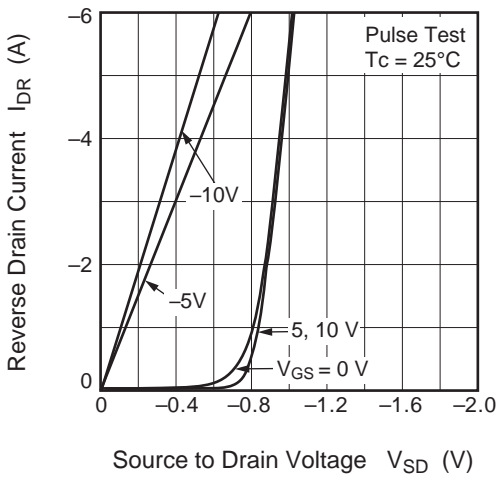
Typical Capacitance vs. Drain to Source Voltage



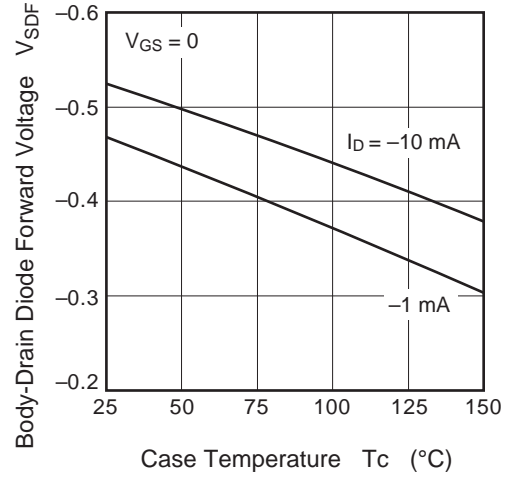
Input Capacitance vs. Gate to Source Voltage



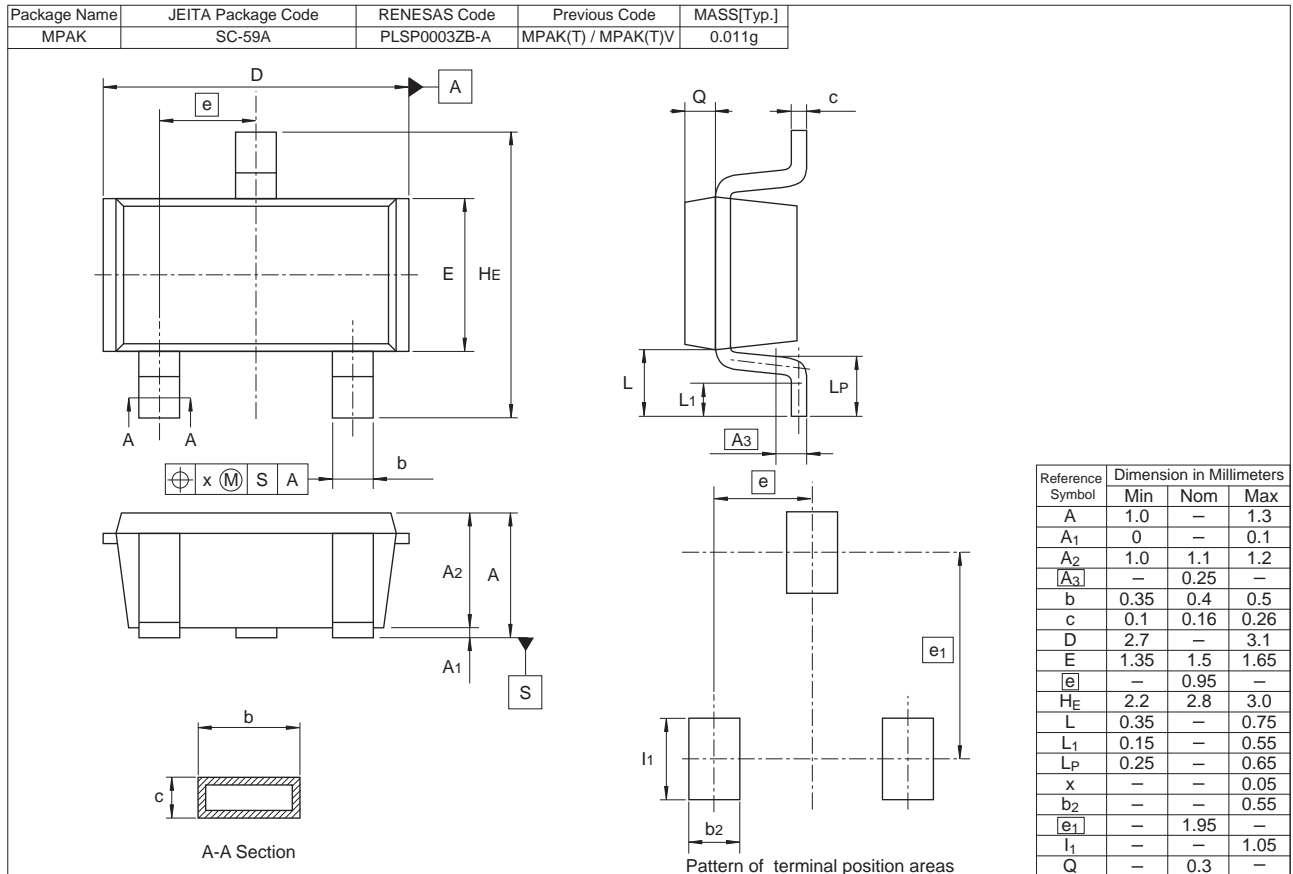
Reverse Drain Current vs. Source to Drain Voltage



Body-Drain Diode Forward Voltage vs. Case Temperature



### Package Dimensions



### Ordering Information

Orderable Part Number	Quantity	Shipping Container
RQJ0203WGDQATL-H	3000 pcs.	φ178 mm reel, 8 mm Emboss taping

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