DEIC515

15 Ampere Low-Side Ultrafast RF MOSFET Driver

Features

- Built using the advantages and compatibility of CMOS and IXYS HDMOS™ processes
- Latch-Up Protected
- High Peak Output Current: 15A Peak
- Wide Operating Range: 8V to 30V
- Rise And Fall Times of <4ns
- Minimum Pulse Width Of 8ns
- High Capacitive Load Drive Capability: 2nF in <4ns
- Matched Rise And Fall Times
- 18ns Input To Output Delay Time
- Low Output Impedance
- Low Quiescent Supply Current

Applications

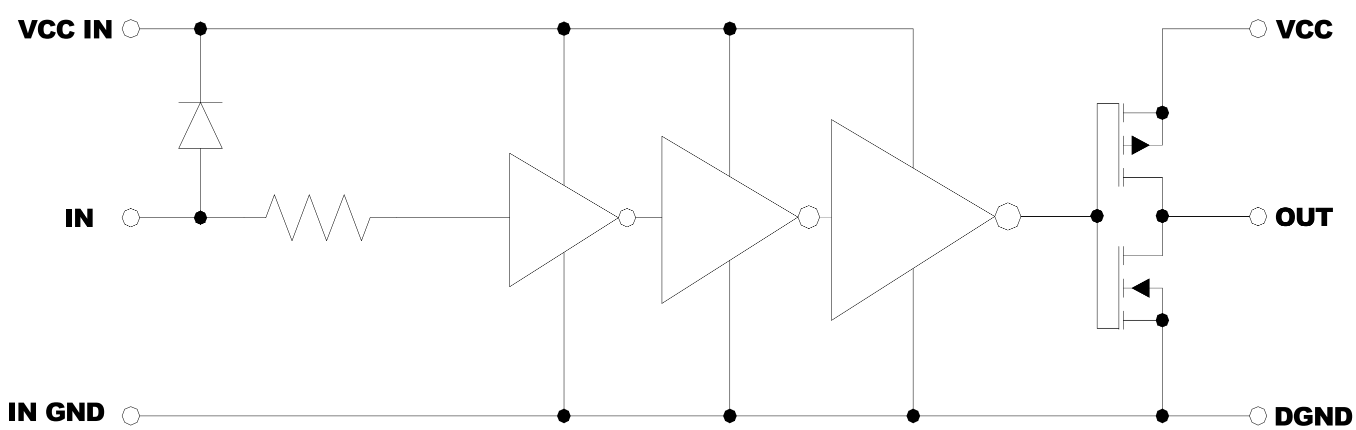
- Driving RF MOSFETs
- Class D or E Switching Amplifier Drivers
- Multi MHz Switch Mode Power Supplies (SMPS)
- Pulse Generators
- Acoustic Transducer Drivers
- Pulsed Laser Diode Drivers
- DC to DC Converters
- Pulse Transformer Driver

Description

The DEIC515 is a CMOS high speed high current gate driver specifically designed to drive MOSFETs in Class D, E, and HF, RF applications at up to 45MHz, as well as other applications requiring ultrafast rise and fall times or short minimum pulse widths. The DEIC515 can source and sink 15A of peak current while producing voltage rise and fall times of less than 4ns, and minimum pulse widths of 8ns. The input of the driver is fully immune to latch up over the entire operating range. Its features and wide safety margin in operating voltage and power make the DEIC515 unmatched in performance and value.

The DEIC515 is packaged in DEI's low inductance RF package incorporating DEI's patented (1) RF layout techniques to minimize stray lead inductances for optimum switching performance. The DEIC515 is a surface-mount device. (1) DEI U.S. Patent #4,891,686

Figure 1 - DEIC515 Functional Diagram



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Absolute Maximum Ratings **(Note 1)**

Parameter	Value
Supply Voltage V_{CC} / V_{CCIN}	30V (Note 2)
Input Voltage Level V_{IN}	-5V to V_{CCIN} + 0.3V (Note 2)
All Other Pins	-0.3V to (V_{CC}, V_{CCIN})+0.3V
Power Dissipation $T_{AMBIENT} \leq$ 25C $T_{case} \leq$ 25C	 2W 100W
Storage Temperature	-40°C to 150°C
Soldering Lead Temperature (10 seconds maximum)	300°C

Parameter	Value
Maximum Junction Temperature	150°C
Operating Temperature Range	-40°C to 85°C
Thermal Impedance (Junction To Case) θ_{JC}	0.13°C/W

Electrical Characteristics

Unless otherwise noted, TA = 25° C, 8V < V_{CC} = V_{CCIN} < 30V.
All voltage measurements with respect to DGND. DEIC515 configured as described in *Test Conditions*.

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
V_{IH}	High input voltage		V_{CCIN} -2			V
V_{IL}	Low input voltage				0.8	V
V_{IN}	Input voltage range		-5		V_{CC} + 0.3	V
I_{IN}	Input current	0V ≤ V_{IN} ≤ V_{CC}, V_{CCIN}	-10		10	µA
V_{OH}	High output voltage		V_{CC}, V_{CCIN} - .025			V
V_{OL}	Low output voltage				0.025	V
R_{OH}	Output resistance @ Output High	I_{OUT} = 10mA, V_{CC} = 15V		0.55	0.85	Ω
R_{OL}	Output resistance @ Output Low	I_{OUT} = 10mA, V_{CC} = 15V		0.35	0.85	Ω
I_{PEAK}	Peak output current	V_{CC}, V_{CCIN} = 15V		15		A
I_{DC}	Continuous output current			2.5		A
f_{MAX}	Maximum frequency	C_L=2nF V_{CC}, V_{CCIN} =15V			45	MHz
t_R	Rise time	C_L=1nF V_{CC}, V_{CCIN} =15V V_{OH}=2V to 12V C_L=2nF V_{CC}, V_{CCIN} =15V V_{OH}=2V to 12V		2.5 4.1		ns ns
t_F	Fall time	C_L=1nF V_{CC}, V_{CCIN} =15V V_{OH}=12V to 2V C_L=2nF V_{CC}, V_{CCIN} =15V V_{OH}=12V to 2V		2.5 3.9		ns ns
t_{ONDLY}	On-time propagation delay	C_L=2nF Vcc=15V		17.4	18.5	ns
t_{OFFDLY}	Off-time propagation delay	C_L=2nF Vcc=15V		14.6	16	ns
P_{Wmin}	Minimum pulse width	FWHM C_L=1nF V_{CC}, V_{CCIN} =15V +3V to +3V C_L=1nF V_{CC}, V_{CCIN} =15V		6.4 8.2		ns ns
Z_{IN}	Input Impeadance	f = 1MHz		7960		Ω
V_{CC}, V_{CCIN}	Power supply voltage		8	15	30	V
I_{CC}	Power supply current	V_{IN} = 0V V_{IN} = V_{CCIN}		0	10 10	µA µA

Note 1: Operating the device beyond parameters with listed "Absolute Maximum Ratings" may cause permanent damage to the device. Typical values indicate conditions for which the device is intended to be functional, but do not guarantee specific performance limits. The guaranteed specifications apply only for the test conditions listed. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.

Note 2: V_{CCIN} / V_{IN} must be within ±0.3V of V_{CC} due to the upper P channel switch of the output stage. Conduction will occur when V_{CCIN} is less than V_{CC} resulting in a negative V_{GS} on this P channel switch.

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Lead Description - DEIC515

SYMBOL	FUNCTION	DESCRIPTION
VCC	Output Supply Voltage	Output section voltage supply leads. These leads provide power to the output stage. Both VCC leads must be connected.
VCCIN	Supply Voltage	Input section voltage supply lead. This lead provides power to the input stage. This lead should not be directly connected to V_{CC}.
IN	Input	Drive signal input.
OUT	Output	Drive signal output.
PGND	Power Ground	The system ground leads. Internally connected to all circuitry, these leads provide ground reference for the entire chip. These leads should be connected to a low noise analog ground plane for optimum performance.
INGND	Input Ground	The input ground lead. This lead is a Kelvin connection internally connected to PGND. This lead must not be connected externally to PGND as excessive current can damage this lead.

CAUTION: These devices are sensitive to electrostatic discharge; follow proper ESD procedures when handling and assembling this component.

Figure 2 - DEIC515 Package Photo And Lead Diagram

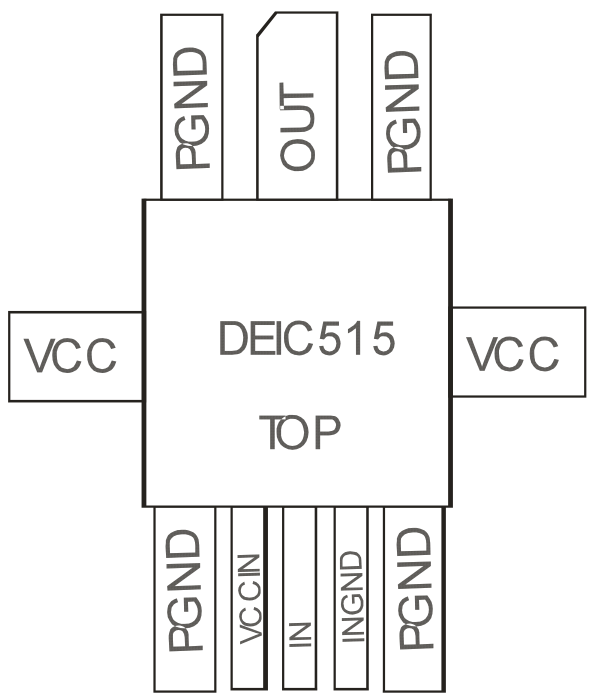
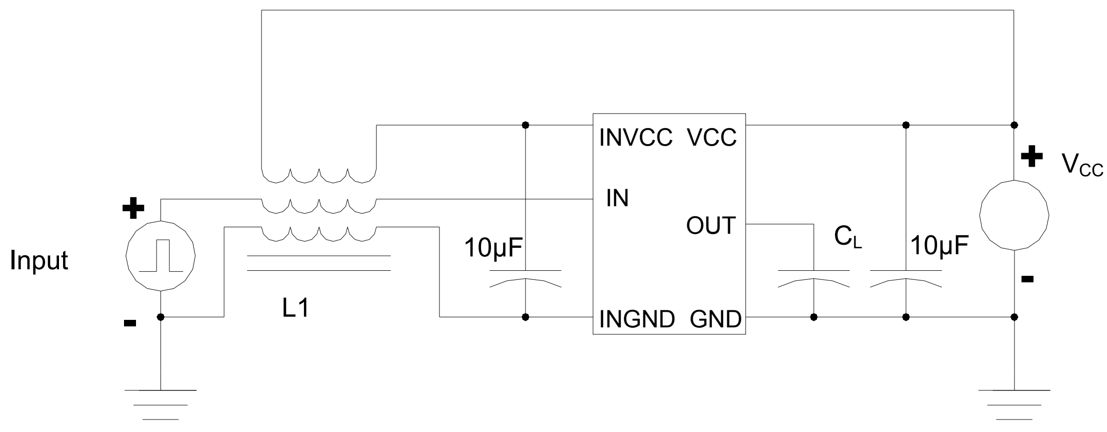


Figure 3 - Characteristics Test Diagram



Common Mode Choke Application

The very high currents and high speeds inside the DEIC515 create very large transients. To avoid problems with false triggering, the input to the DEIC515 should be supplied via a common mode choke. This is a simple tri-filar winding on a small ferrite core. This prevents high speed transients from impacting the input signal by allowing it to follow the internal die potential changes without changing the state of the input.

Fig. 4

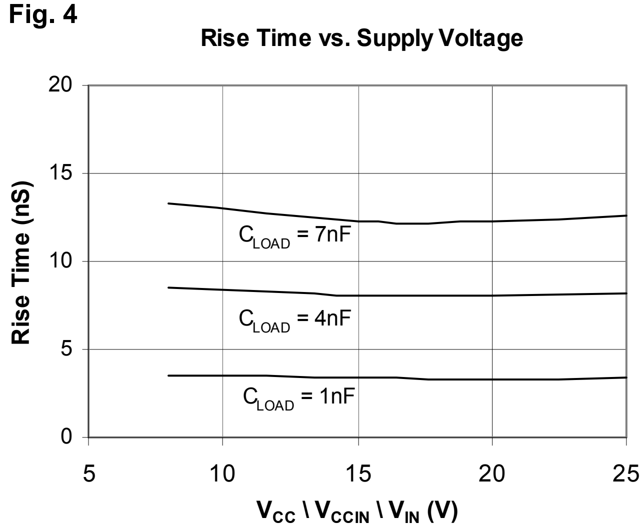


Fig. 5

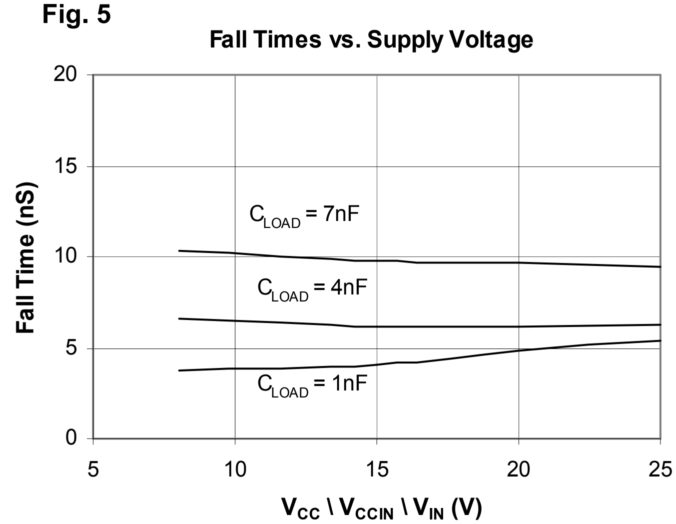


Fig. 6

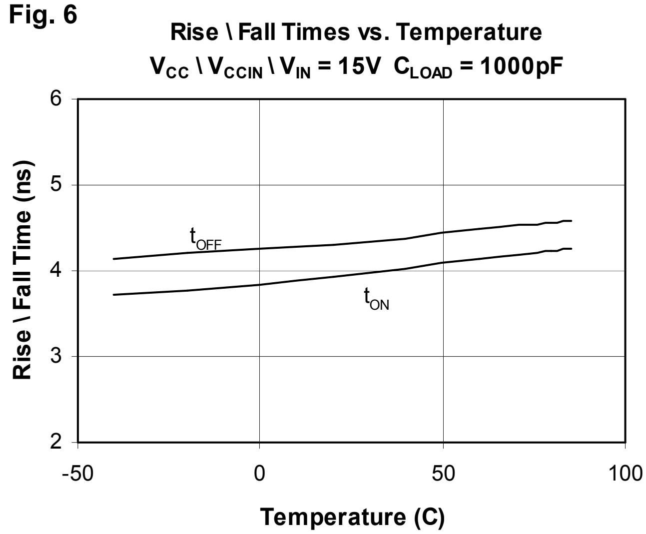


Fig. 7

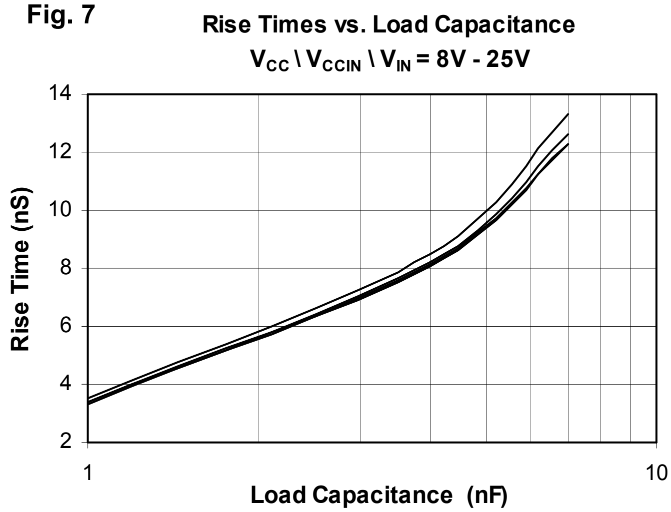


Fig. 8

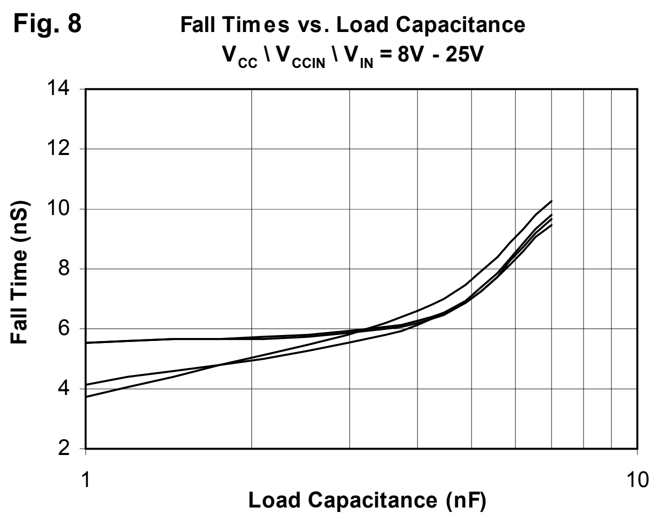


Fig. 9

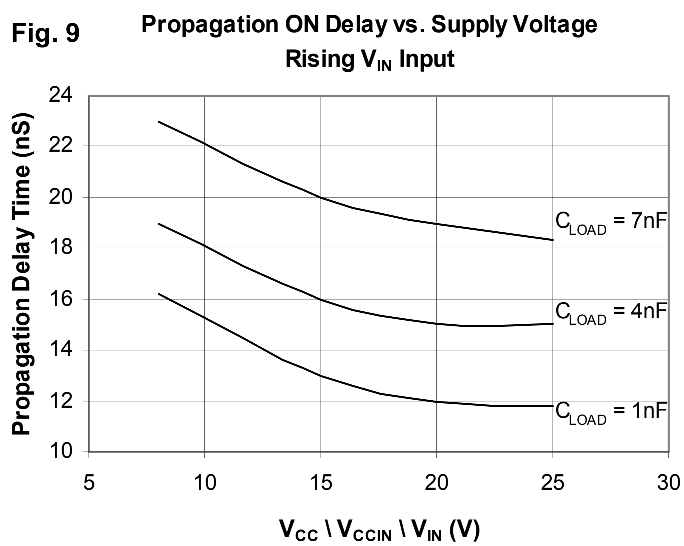


Fig. 10

Propagation OFF Delay vs. Supply Voltage
Falling V_{IN} Input

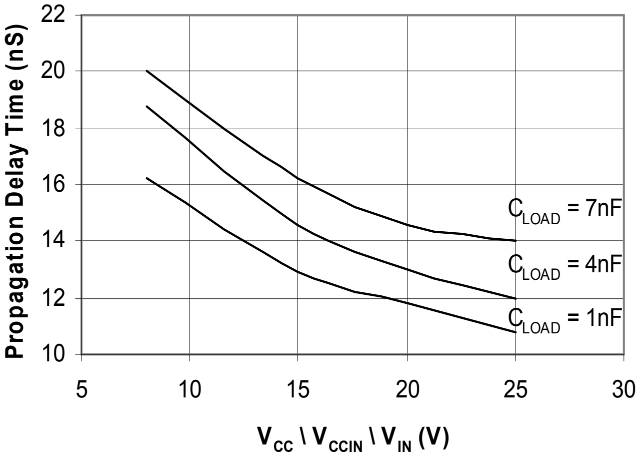


Fig. 11

Propagation Delay vs. Temperature
V_{CC} \ V_{CCIN} \ V_{IN} = 15V C_{LOAD} = 1000pF

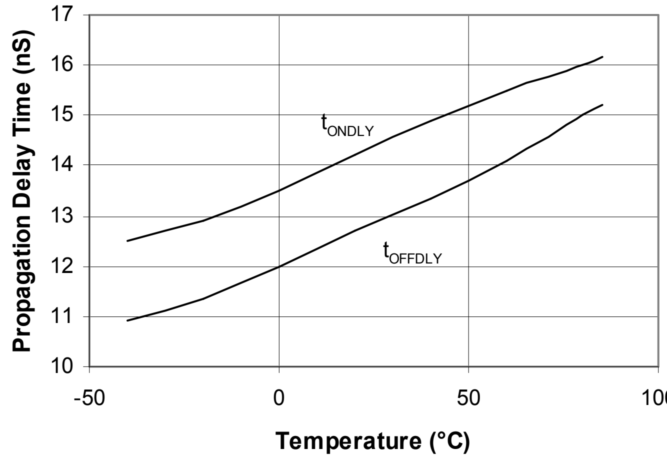


Fig. 12

V_{CCIN} Supply Current vs. Frequency
V_{IN} \ V_{CCIN} = V_{CC} C_{LOAD} = 1000pF

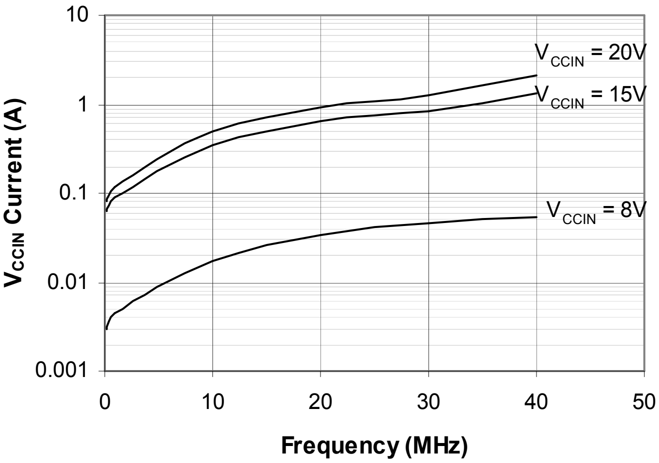


Fig. 13

V_{CCIN} Supply Current vs. Frequency
V_{IN} \ V_{CC} = V_{CCIN} C_{LOAD} = 7000pF

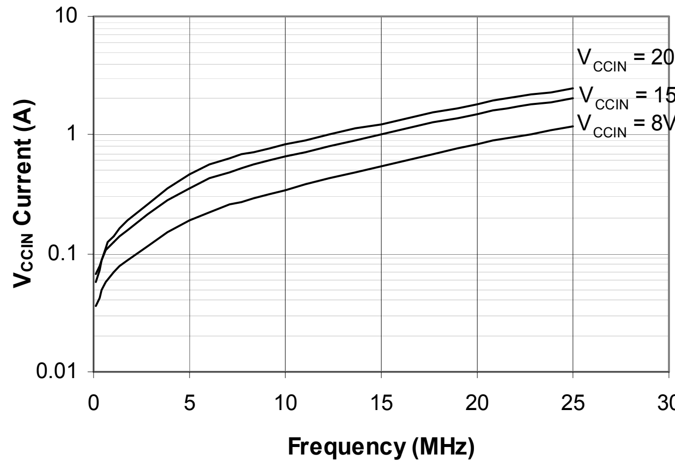


Fig. 14

V_{CC} Supply Current vs. Frequency
V_{IN} \ V_{CCIN} =V_{CC} C_{LOAD} = 1000pF

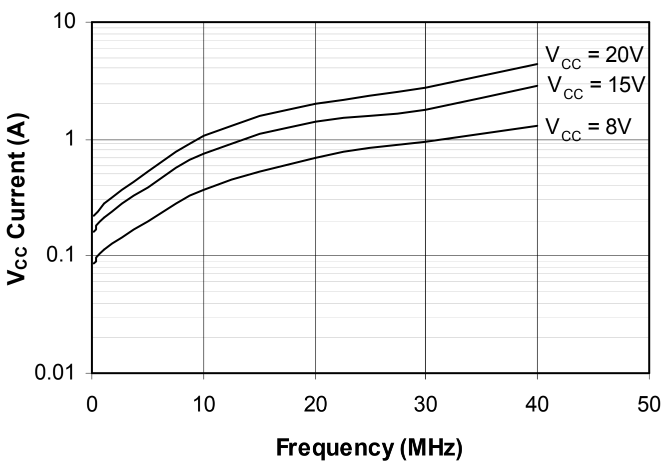


Fig. 15

V_{CC} Supply Current vs. Frequency
V_{IN} \ V_{CCIN} = V_{CC} C_{LOAD} = 7000pF

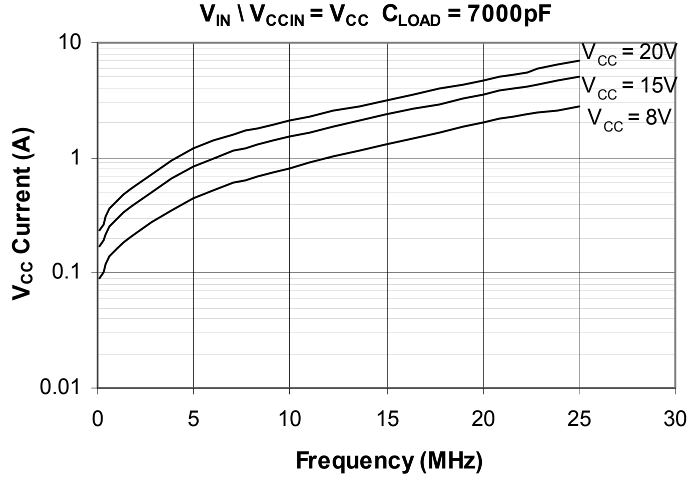


Fig. 16 Output Source Current vs. Supply Voltage

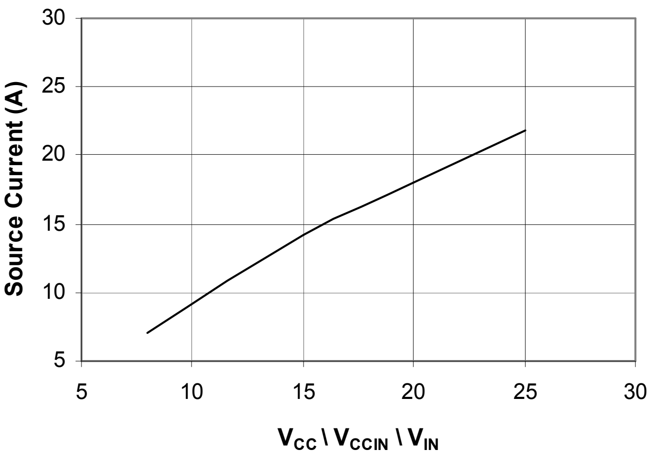


Fig. 17 Output Sink Current vs. Supply Voltage

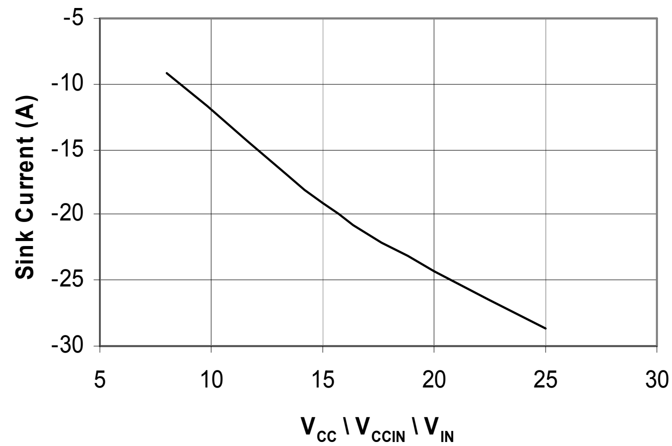


Fig. 18 Output Source Current vs. Temperature
V_{CC} \ V_{CCIN} \ V_{IN} = 15V

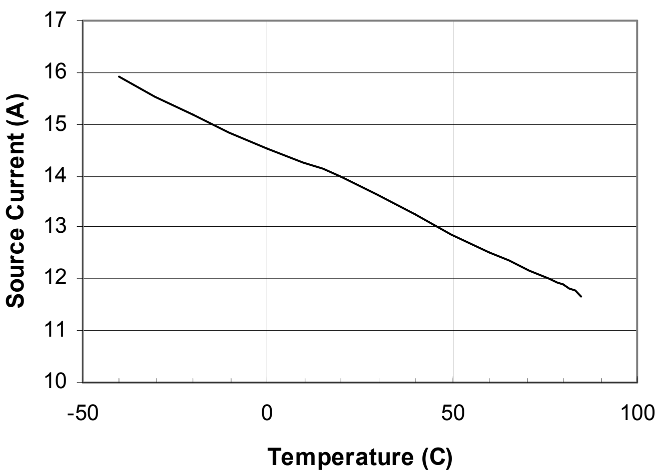


Fig. 19 Output Sink Current vs. Temperature
V_{CC} \ V_{CCIN} \ V_{IN} = 15V

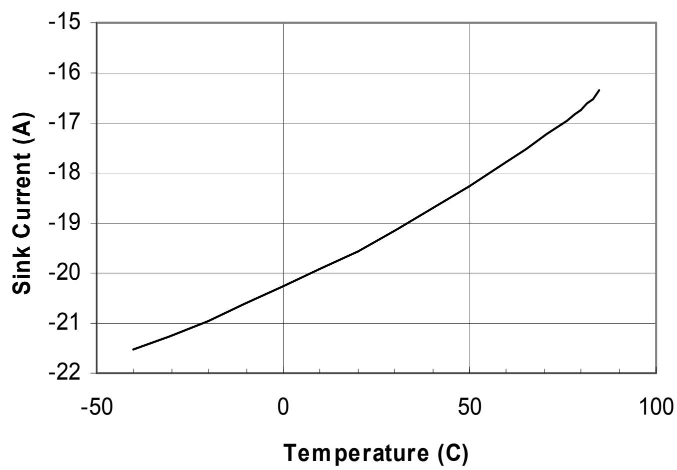
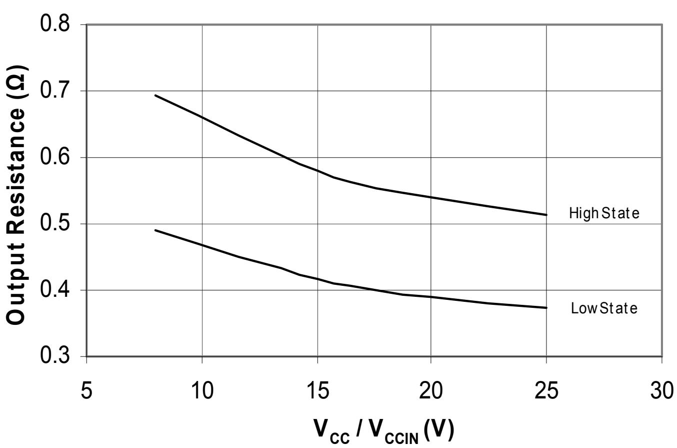


Fig. 20

High \ Low State Output Resistance vs. Supply Voltage



15 Ampere Low-Side Ultrafast RF MOSFET Driver

Application Information

Introduction
Circuits capable of very high switching speeds and high frequency operation require close attention to several important issues. Key elements include circuit loop inductance, Vcc bypassing, and grounding.

Circuit Loop Inductance
The Vcc to Vcc Ground current path defines the loop which will generate the inductive term. This loop must be kept as short as possible. The output lead must be no further than 0.375 inches (9.5mm) from the gate of the MOSFET. Furthermore, the output ground leads must provide a balanced symmetric coplanar ground return for optimum operation.

Vcc Bypassing
In order to turn a MOSFET on properly, the DEIC515 must be able to draw up to 15A of current from the Vcc power supply in 2-6ns (depending upon the input capacitance of the MOSFET being driven). Good performance requires very low impedance between the driver and the power supply. The most common method of achieving this low impedance is to bypass the power supply at the driver with a capacitance value much larger than the load capacitance. Usually, this is achieved by placing two or three different types of bypassing capacitors, with complementary impedance curves, very close to the driver itself. (These capacitors should be carefully selected, low inductance, low resistance, high-pulse-current-service capacitors.) Care should be taken to keep the lengths of the leads between these bypass capacitors and the DEIC515 to an absolute minimum.

The bypassing should be comprised of several values of chip capacitors symmetrically placed on either side of the IC. Recommended values are .01uF and .47uF chips and at least two 4.7uF tantalums.

Grounding
In order for the design to turn the load off properly, the DEIC515 must be able to drain this 15A of current into an adequate grounding system. There are two paths for returning current that need to be considered: Path #1 is between the DEIC515 and its load, and path #2 is between the DEIC515 and its power supply. Both of these paths should be as low in resistance and inductance as possible, and thus as short as practical.

The DEI515 has separate ground leads for input and power which allows the addition of a common mode choke at the input and input ground leads.

The common mode choke will provide a means of preventing ground bounce from affecting the input to the driver. The selection of the common mode choke is related to the device being driven, the board layout, and the Vcc bypassing.

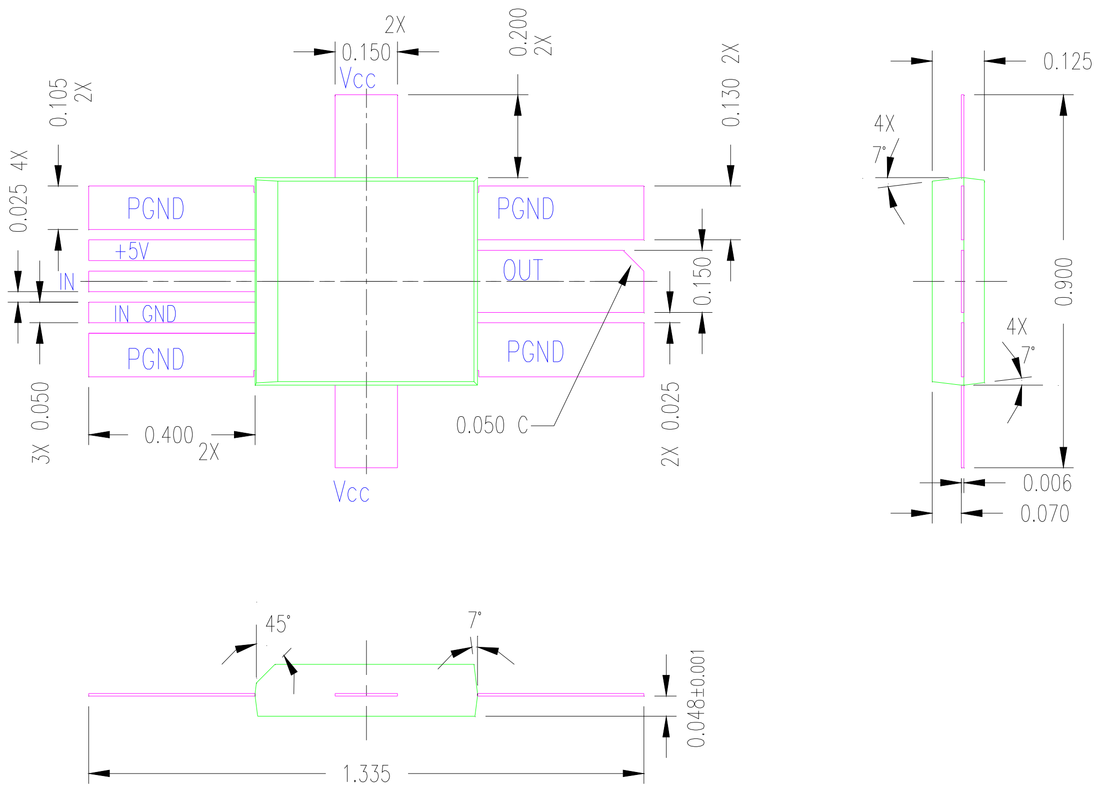
Output Lead Inductance
Of equal importance to supply bypassing and grounding are issues related to the output lead inductance. Every effort should be made to keep the leads between the driver and its load as short and wide as possible, and treated as coplanar transmission lines.

In configurations where the optimum configuration of circuit layout and bypassing cannot be used, a series resistance of a few ohms in the gate lead may be necessary to prevent ringing.

Heat Sinking
For high power operation, the bottom side metalized substrate should be placed in compression against an appropriate heat sink. The substrate is metalized for improved heat dissipation, and is not electrically connected to the device or to ground.

See the DEI technical note “DE-Series MOSFET and IC Mounting Instructions” on the IXYSRF website at www.ixysrf.com for detailed mounting instructions.

Fig. 21- Dimensional Drawing



Bottom View