Precision, Low Power Rail-to-Rail Output Differential Op Amp

FEATURES

- **100µV Max Offset Voltage**
- **50nA Max Input Offset Current**
- **Fast Settling: 780ns to 18-Bit, 8V$_{P-P}$ Output**
- **1.9mA Supply Current**
- **2.9nV/√Hz Input-Referred Noise**
- 2.8V (±1.4V) to 11V (±5.5V) Supply Voltage Range
- Differential Rail-to-Rail Outputs
- Input Common Mode Range Includes Ground
- Low Distortion: 115dB SFDR at 2kHz, 18V$_{P-P}$
- 500MHz Gain-Bandwidth Product
- 35MHz –3dB Bandwidth
- Low Power Shutdown: 20µA (V$_S$ = 3V)
- 8-lead MSOP and 2mm × 3mm 8-Lead DFN Packages

APPLICATIONS

- 20-Bit, 18-Bit and 16-Bit SAR ADC Drivers
- Single-Ended-to-Differential Conversion
- Low Power Pipeline ADC Drivers
- Differential Line Drivers
- Battery-Powered Instrumentation

DESCRIPTION

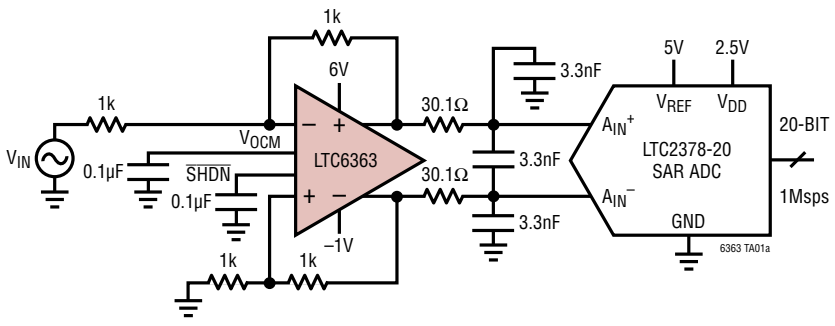
The LTC®6363 is a low power, low noise, fully differential op amp with rail-to-rail outputs optimized to drive low power SAR ADCs. The LTC6363 draws only 1.9mA supply current in active operation and features a shutdown mode which reduces the current consumption to 20µA (V$_S$ = 3V).

The amplifier may be configured to convert a single-ended input signal to a differential output signal or may be driven differentially. Low offset voltage and low input offset current make this amplifier suitable for use not only as an ADC driver but also earlier in the signal chain to provide filtering, gain or even attenuation by up to 10-to-1 to convert high voltage signals to levels suitable for low voltage ADCs.

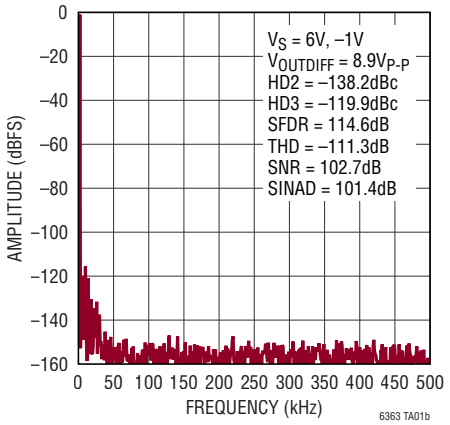
The LTC6363 is available in 8-lead MSOP and 2mm × 3mm leadless DFN packages, and operates with guaranteed specifications over a –40°C to 125°C temperature range.

TYPICAL APPLICATION

DC-Coupled Interface from a Ground-Referenced Single-Ended Input to an LTC2378-20 SAR ADC



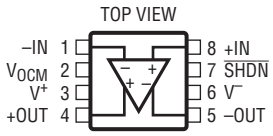
LTC6363 Driving LTC2378-20
f_{IN} = 2kHz, –1dBFS,175k-Point FFT



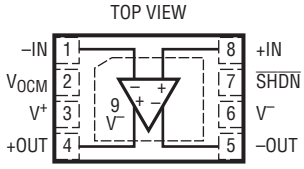
ABSOLUTE MAXIMUM RATINGS (Note 1)

Total Supply Voltage ($V^+ – V^–$) 12V
Input Current (+IN, –IN, V_{OCM}, $\overline{SHDN}$) (Note 2) ... ±10mA
Output Short-Circuit Duration
(Note 3) ..... Thermally Limited
Operating Temperature Range (Note 4)
LTC6363I ..... –40°C to 85°C
LTC6363H..... –40°C to 125°C
Specified Temperature Range (Note 5)
LTC6363I ..... –40°C to 85°C
LTC6363H..... –40°C to 125°C
Maximum Junction Temperature ..... 150°C
Storage Temperature Range ..... –65°C to 150°C
MSOP Lead Temperature (Soldering, 10 sec)..... 300°C

PIN CONFIGURATION



MS8 PACKAGE
8-LEAD PLASTIC MSOP
T_{JMAX} = 150°C, θ_{JA} = 273°C/W



DD PACKAGE
8-LEAD (2mm × 3mm) PLASTIC DFN
T_{JMAX} = 150°C, θ_{JA} = 64°C/W, θ_{JC} = 10.6°C/W
EXPOSED PAD (PIN 9) IS V–, MUST BE SOLDERED TO PCB

ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	SPECIFIED TEMPERATURE RANGE
LTC6363IMS8#PBF	LTC6363IMS8#TRPBF	LTGSQ	8-Lead Plastic MSOP	–40°C to 85°C
LTC6363HMS8#PBF	LTC6363HMS8#TRPBF	LTGSQ	8-Lead Plastic MSOP	–40°C to 125°C

Lead Free Finish

TAPE AND REEL (MINI)	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LTC6363IDCB#TRMPBF	LTC6363IDCB#TRPBF	LGVG	8-Lead (2mm × 3mm) Plastic DFN	–40°C to 85°C
LTC6363HDCB#TRMPBF	LTC6363HDCB#TRPBF	LGVG	8-Lead (2mm × 3mm) Plastic DFN	–40°C to 125°C

TRM = 500 pieces. *Temperature grades are identified by a label on the shipping container.

Consult LTC Marketing for parts specified with wider operating temperature ranges.
Consult LTC Marketing for information on lead based finish parts.

For more information on lead free part marking, go to: http://www.linear.com/leadfree/
For more information on tape and reel specifications, go to: http://www.linear.com/tapeandreel/

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V^+ = 10V, V^- = 0V, V_{CM} = V_{OCM} = V_{ICM} = 5V, $V_{\overline{SHDN}}$ = open. V_S is defined as ($V^+ - V^-$). V_{OUTCM} is defined as ($V_{+OUT} + V_{-OUT}$)/2. V_{ICM} is defined as ($V_{+IN} + V_{-IN}$)/2. $V_{OUTDIFF}$ is defined as ($V_{+OUT} - V_{-OUT}$).

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{OSDIFF}	Differential Offset Voltage (Input Referred)	V_S = 3V V_{ICM} =1.5V	 ●		25	100 200	µV µV
		V_S = 5V V_{ICM} = 2.5V	 ●		25	100 200	µV µV
		V_S = 10V V_{ICM} = 5V	 ●		25	100 200	µV µV
$\Delta V_{OSDIFF}/\Delta T$ (Note 6)	Differential Offset Voltage Drift (Input Referred)	V_S = 3V V_S = 5V V_S = 10V	● ● ●		0.45 0.45 0.45	1.25 1.25 1.25	µV/°C µV/°C µV/°C
I_B (Note 7)	Input Bias Current	V_S = 3V V_S = 5V V_S = 10V	● ● ●	–1 –1 –1	–0.5 –0.5 –0.5	–0.1 –0.1 –0.1	µA µA µA
I_{OS} (Note 7)	Input Offset Current	V_S = 3V	 ●		±5	±50 ±75	nA nA
		V_S = 5V	 ●		±5	±50 ±75	nA nA
		V_S = 10V	 ●		±5	±50 ±75	nA nA
$\Delta I_{OS}/\Delta T$ (Note 6)	Input Offset Current Drift	V_S = 3V V_S = 5V V_S = 10V	● ● ●		±30 ±30 ±30	±150 ±150 ±150	pA/°C pA/°C pA/°C
R_{IN}	Input Resistance	Common Mode Differential Mode			50 40		MΩ kΩ
C_{IN}	Input Capacitance	Differential Mode			2		pF
e_n	Differential Input Noise Voltage Differential Input Noise Voltage Density	0.1Hz to 10Hz f = 100kHz (Not Including R_I/R_F)			2.5 2.9		μV_{P-P} $nV/\sqrt{Hz}$
e_{nvocm}	Common Mode Noise Voltage Density	f = 100kHz			14		$nV/\sqrt{Hz}$
i_n	Input Noise Current Density	f = 100kHz (Not Including R_I/R_F)			0.55		$pA/\sqrt{Hz}$
V_{ICMR} (Note 8)	Input Common Mode Range	V_S = 3V V_S = 5V V_S = 10V	● ● ●	0 0 0		1.8 3.8 8.8	V V V
CMRRI (Note 9)	Input Common Mode Rejection Ratio (Input Referred) $\Delta V_{ICM}/\Delta V_{OSDIFF}$	V_S = 3V, V_{ICM} from 0V to 1.8V V_S = 5V, V_{ICM} from 0V to 3.8V V_S = 10V, V_{ICM} from 0V to 8.8V	● ● ●	78 85 90	110 115 120		dB dB dB
CMRRIO (Note 9)	Output Common Mode Rejection Ratio (Input Referred) $\Delta V_{OCM}/\Delta V_{OSDIFF}$	V_S = 3V, V_{OCM} from 0.5V to 2.5V V_S = 5V, V_{OCM} from 0.5V to 4.5V V_S = 10V, V_{OCM} from 0.5V to 9.5V	● ● ●	70 80 90	120 120 120		dB dB dB
PSRR (Note 10)	Differential Power Supply Rejection ($\Delta V_S/\Delta V_{OSDIFF}$)	V_S = 2.8V to 11V	●	90	125		dB
PSRRCM (Note 10)	Output Common Mode Power Supply Rejection ($\Delta V_S/\Delta V_{OSCM}$)	V_S = 2.8V to 11V	●	70	90		dB
GCM	Common Mode Gain ($\Delta V_{OUTCM}/\Delta V_{OCM}$)	V_S = 3V, V_{OCM} from 0.5V to 2.5V V_S = 5V, V_{OCM} from 0.5V to 4.5V V_S = 10V, V_{OCM} from 0.5V to 9.5V	● ● ●		1 1 1		V/V V/V V/V
ΔGCM	Common Mode Gain Error 100 • (GCM – 1)	V_S = 3V, V_{OCM} from 0.5V to 2.5V V_S = 5V, V_{OCM} from 0.5V to 4.5V V_S = 10V, V_{OCM} from 0.5V to 9.5V	● ● ●		0.2 0.1 0.07	1 0.5 0.4	% % %

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V^+ = 10V, V^- = 0V, V_{CM} = V_{OCM} = V_{ICM} = 5V, $V_{\overline{SHDN}}$ = open. V_S is defined as ($V^+ – V^-$). V_{OUTCM} is defined as ($V_{+OUT} + V_{–OUT}$)/2. V_{ICM} is defined as ($V_{+IN} + V_{–IN}$)/2. $V_{OUTDIFF}$ is defined as ($V_{+OUT} – V_{–OUT}$).

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
BAL	Output Balance ($\Delta V_{OUTCM}/\Delta V_{OUTDIFF}$)	$\Delta V_{OUTDIFF}$ = 2V					
		Single-Ended Input	●		–58	–35	dB
		Differential Input	●		–58	–35	dB
A_{VOL}	Open-Loop Voltage Gain				125		dB
V_{OSCM}	Common Mode Offset Voltage ($V_{OUTCM} – V_{OCM}$)	V_S = 3V	●		±1	±6	mV
		V_S = 5V	●		±1	±6	mV
		V_S = 10V	●		±1	±6	mV
$\Delta V_{OSCM}/\Delta T$	Common Mode Offset Voltage Drift		●		10		µV/°C
V_{OUTCMR} (Note 8)	Output Signal Common Mode Range (Voltage Range for the V_{OCM} Pin)	V_{OCM} Driven Externally, V_S = 3V	●	0.5		2.5	V
		V_{OCM} Driven Externally, V_S = 5V	●	0.5		4.5	V
		V_{OCM} Driven Externally, V_S = 10V	●	0.5		9.5	V
V_{OCM}	Self-Biased Voltage at the V_{OCM} Pin	V_{OCM} Not Connected, V_S = 3V	●	1.38	1.5	1.82	V
		V_{OCM} Not Connected, V_S = 5V	●	2.33	2.5	2.82	V
		V_{OCM} Not Connected, V_S = 10V	●	4.79	5	5.21	V
R_{INVOCM}	Input Resistance, V_{OCM} Pin		●	1.3	1.8	2.3	MΩ
V_{OUT}	Output Voltage, High, Either Output Pin	I_L= 0mA, V_S = 3V	●	2.8	2.88		V
		I_L = –5mA, V_S = 3V	●	2.75	2.83		V
		I_L= 0mA, V_S = 5V	●	4.8	4.88		V
		I_L = –5mA, V_S = 5V	●	4.75	4.83		V
		I_L= 0mA, V_S = 10V	●	9.8	9.88		V
		I_L = –5mA, V_S = 10V	●	9.7	9.83		V
	Output Voltage, Low, Either Output Pin	I_L= 0mA, V_S = 3V	●		0.1	0.15	V
		I_L = 5mA, V_S = 3V	●		0.15	0.25	V
		I_L= 0mA, V_S = 5V	●		0.1	0.15	V
		I_L = 5mA, V_S = 5V	●		0.15	0.25	V
		I_L= 0mA, V_S = 10V	●		0.1	0.2	V
		I_L = 5mA, V_S = 10V	●		0.15	0.3	V
I_{SC}	Output Short-Circuit Current, Either Output Pin, Sinking	V_S = 3V, Output Shorted to 1.5V	●	12	25		mA
		V_S = 5V, Output Shorted to 2.5V	●	13	35		mA
		V_S = 10V, Output Shorted to 5V	●	14	40		mA
	Output Short-Circuit Current, Either Output Pin, Sourcing	V_S = 3V, Output Shorted to 1.5V	●	25	55		mA
		V_S = 5V, Output Shorted to 2.5V	●	27	75		mA
		V_S = 10V, Output Shorted to 5V	●	30	90		mA
SR	Slew Rate	Differential 18V_{P-P} Output			75		V/µs
GBW	Gain-Bandwidth Product	f_{TEST} = 200kHz		390	500		MHz
			●	230			MHz
f_{-3dB}	-3dB Bandwidth	R_I = R_F =1k			35		MHz
FPBW (Note 12)	Full Power Bandwidth	10V_{P-P} Output			2.4		MHz
		18V_{P-P} Output			1.3		MHz
HD2/HD3	2nd/3rd Order Harmonic Distortion Single-Ended Input	f = 1kHz, V_{OUT} = 18V_{P-P}			–113/–118		dBc
		f = 10kHz, V_{OUT} = 18V_{P-P}			–122/–111		dBc
		f = 100kHz, V_{OUT} = 18V_{P-P}			–76/–79		dBc
t_S	Settling Time to a 8V_{P-P} Output Step	0.1%			350		ns
		0.01%			420		ns
		0.0015% (16-Bit)			470		ns
		4ppm (18-Bit)			780		ns
V_S (Note 11)	Supply Voltage Range		●	2.8		11	V

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V^+ = 10V, V^- = 0V, V_{CM} = V_{OCM} = V_{ICM} = 5V, $V_{\overline{SHDN}}$ = open. V_S is defined as ($V^+ – V^-$). V_{OUTCM} is defined as ($V_{+OUT} + V_{–OUT}$)/2. V_{ICM} is defined as ($V_{+IN} + V_{–IN}$)/2. $V_{OUTDIFF}$ is defined as ($V_{+OUT} – V_{–OUT}$).

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
I_S	Supply Current	V_S = 3V, Active	●		1.7	1.8 1.95	mA mA
		V_S = 3V, Shutdown	●		20	40	µA
		V_S = 5V, Active	●		1.75	1.85 2	mA mA
		V_S = 5V, Shutdown	●		30	65	µA
		V_S = 10V, Active	●		1.9	2 2.2	mA mA
		V_S = 10V, Shutdown	●		70	130	µA
V_{IL}	$\overline{SHDN}$ Input Logic Low		●			$(V^+ + V^-)/2 + 0.4$	V
V_{IH}	$\overline{SHDN}$ Input Logic High		●	$(V^+ + V^-)/2 + 1.2$			V
t_{ON}	Turn-On Time				4		µs
t_{OFF}	Turn-Off Time				2		µs
$R_{\overline{SHDN}}$	Input Resistance, $\overline{SHDN}$ Pin		●	300	500	700	kΩ

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: If input pins (+IN, –IN, V_{OCM} and $\overline{SHDN}$) should exceed either supply voltage, the input current should be limited to less than 10mA. Additionally, if the differential input voltage exceeds 1.4V, the input current should be limited to less than 10mA.

Note 3: A heat sink may be required to keep the junction temperature below the absolute maximum rating when the output is shorted indefinitely.

Note 4: The LTC6363I is guaranteed functional over the operating temperature range of –40°C to 85°C. The LTC6363H is guaranteed functional over the operating temperature range of –40°C to 125°C.

Note 5: The LTC6363I is guaranteed to meet specified performance from –40°C to 85°C. The LTC6363H is guaranteed to meet specified performance from –40°C to 125°C.

Note 6: Maximum differential input referred offset voltage drift and offset current drift are determined by sampling typical parts. Drift is not guaranteed by test or QA sampled at this value.

Note 7: Input bias current is defined as the average of the input currents flowing into the input pins (–IN and +IN). Input Offset current is defined as the difference between the input bias currents ($I_{OS} = I_B^+ – I_B^-$).

Note 8: Input common mode range is tested by verifying that at the limits stated in the Electrical Characteristics table, the differential offset (V_{OSDIFF}) and common mode offset (V_{OSCM}) have not deviated by more than ±200µV and ±10mV respectively compared to the V_{ICM} = 5V (at V_S = 10V), V_{ICM} = 2.5V (at V_S = 5V) and V_{ICM} = 1.5V (at V_S = 3V) cases.

Output common mode range is tested by verifying that at the limits stated in the Electrical Characteristics table, the common mode offset (V_{OSCM}) has not deviated by more than ±15mV compared to the V_{OCM} = 5V (at V_S = 10V), V_{OCM} = 2.5V (at V_S = 5V) and V_{OCM} = 1.5V (at V_S = 3V) cases.

Note 9: Input CMRR is defined as the ratio of the change in the input common mode voltage at the pins +IN or –IN to the change in differential input referred offset voltage. Output CMRR is defined as the ratio of the change in the voltage at the V_{OCM} pin to the change in differential input referred offset voltage. This specification is strongly dependent on feedback ratio matching between the two outputs and their respective inputs and it is difficult to measure amplifier performance (see Effects of Resistor Pair Mismatch in the Applications Information section of this data sheet). For a better indicator of actual amplifier performance independent of feedback component matching, refer to the PSRR specification.

Note 10: Differential power supply rejection (PSRR) is defined as the ratio of the change in supply voltage to the change in differential input referred offset voltage. Common mode power supply rejection (PSRRCM) is defined as the ratio of the change in supply voltage to the change in the common mode offset voltage.

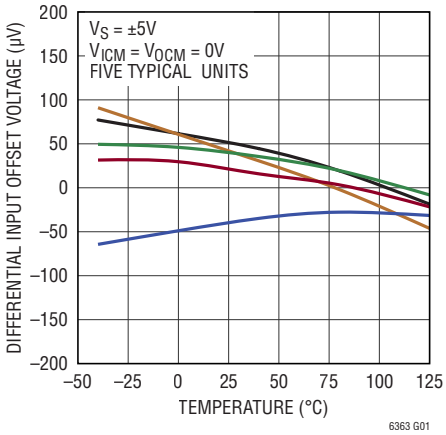
Note 11: Supply voltage range is guaranteed by power supply rejection ratio test.

Note 12: Full power bandwidth is calculated from the slew rate.

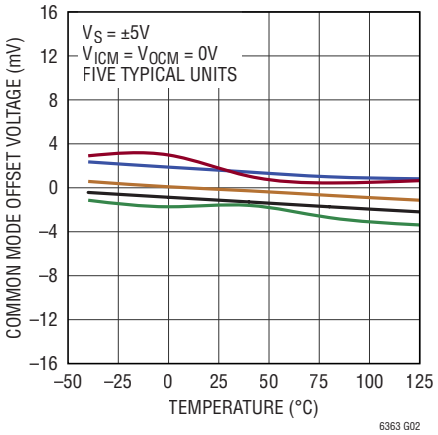
$FPBW = SR/(2 \bullet \pi \bullet V_P)$

TYPICAL PERFORMANCE CHARACTERISTICS

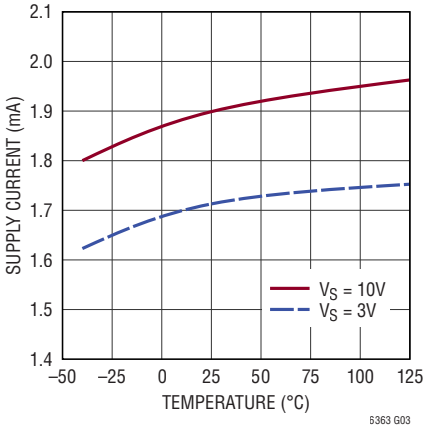
Differential Input Offset Voltage vs Temperature



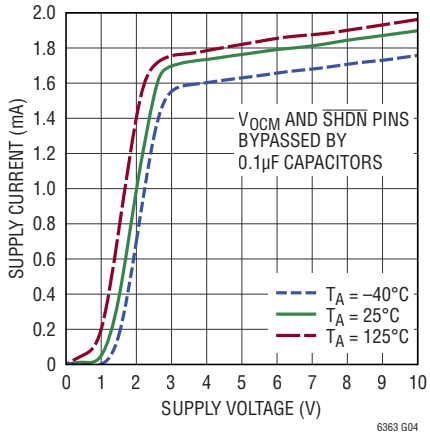
Common Mode Offset Voltage vs Temperature



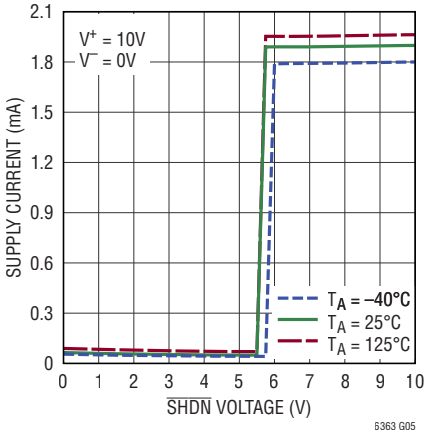
Supply Current vs Temperature



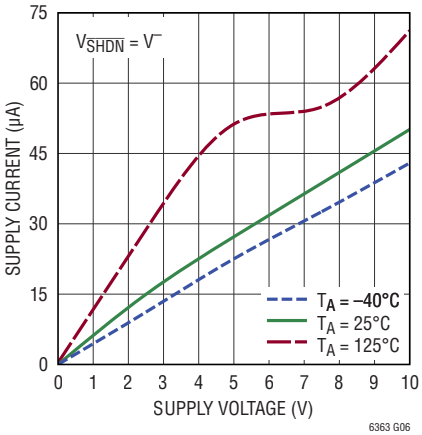
Supply Current vs Supply Voltage



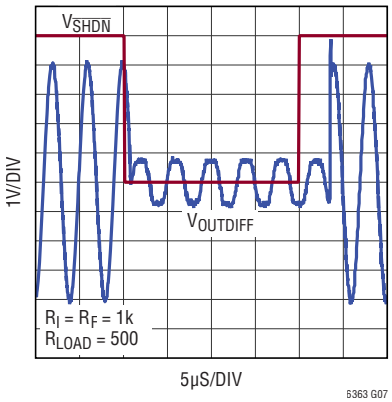
Supply Current vs $\overline{SHDN}$ Voltage



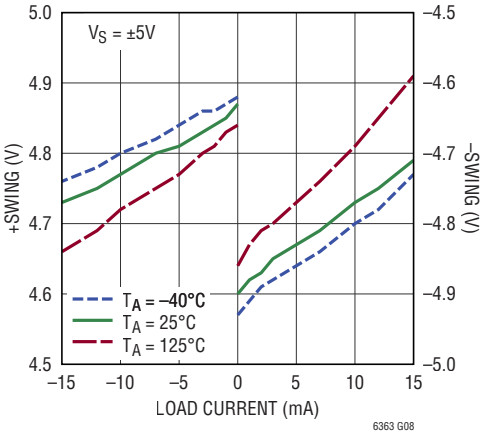
Shutdown Supply Current vs Supply Voltage



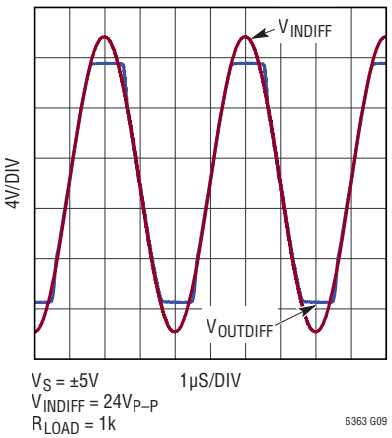
Turn-On and Turn-Off Transient Response



Output Voltage Swing vs Load Current

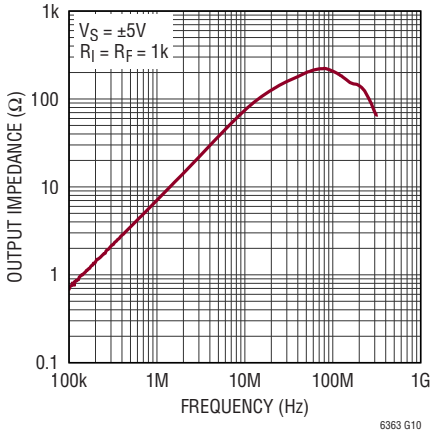


Output Overdrive Recovery

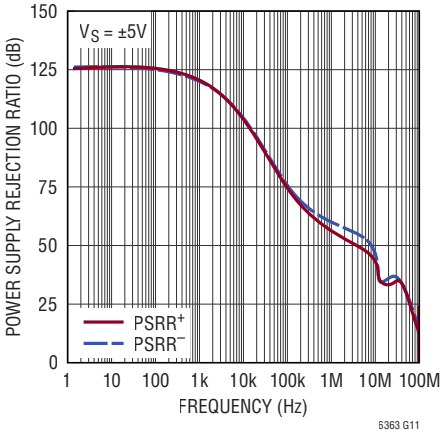


TYPICAL PERFORMANCE CHARACTERISTICS

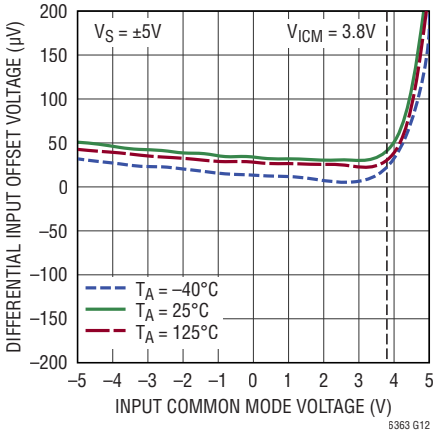
Differential Output Impedance vs Frequency



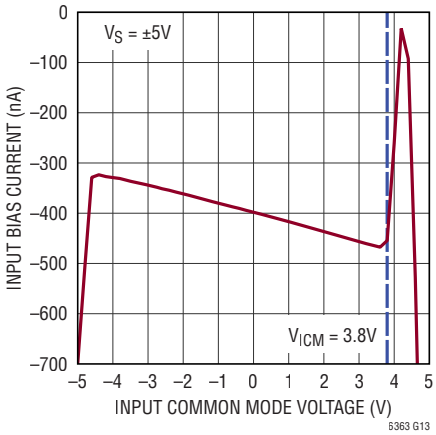
Differential Power Supply Rejection Ratio vs Frequency



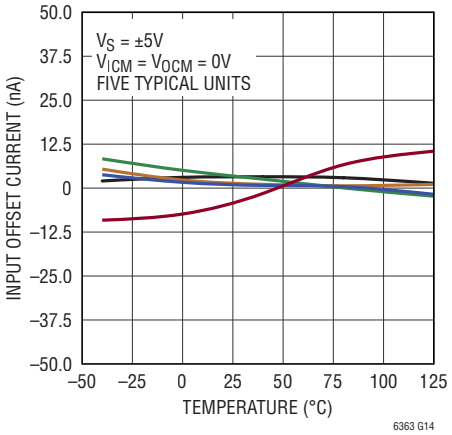
Differential Input Offset Voltage vs Input Common Mode Voltage



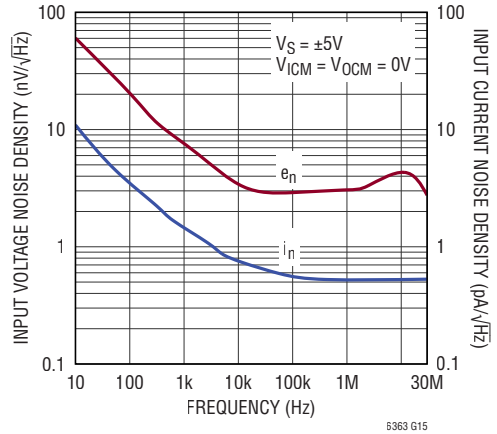
Input Bias Current vs Input Common Mode Voltage



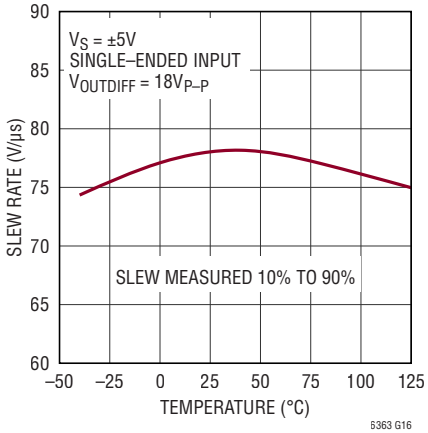
Input Offset Current vs Temperature



Input Noise Density vs Frequency

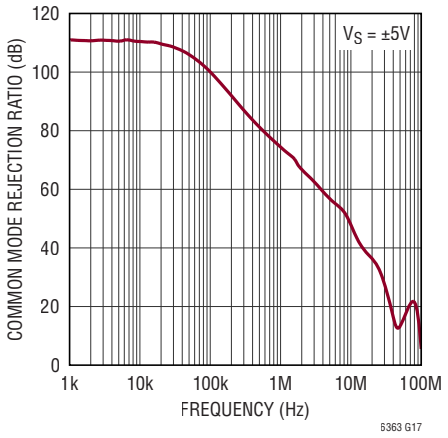


Slew Rate vs Temperature

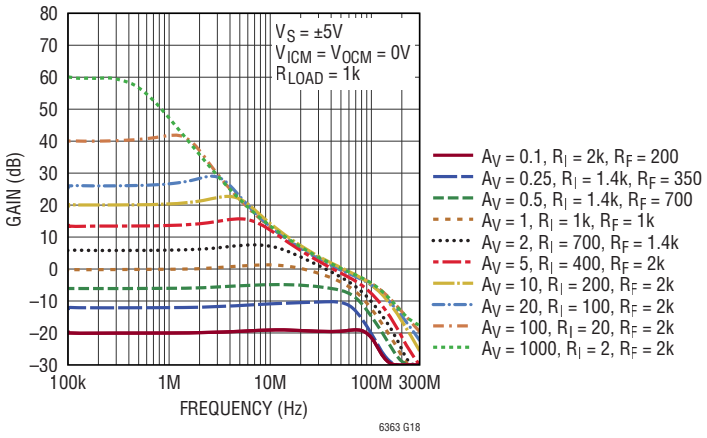


TYPICAL PERFORMANCE CHARACTERISTICS

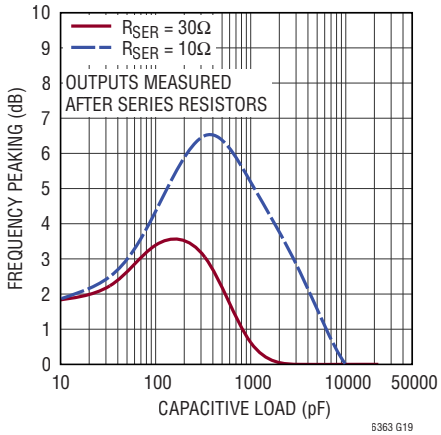
Input Common Mode Rejection Ratio vs Frequency



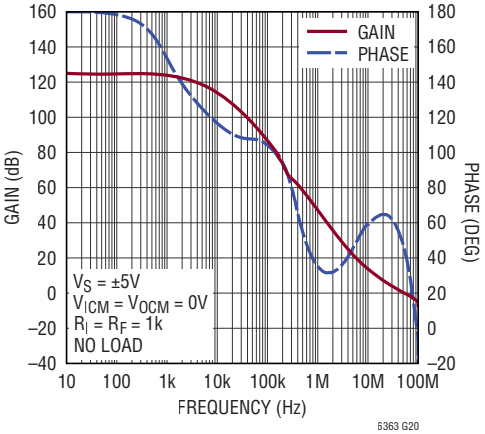
Frequency Response vs Closed-Loop Gain



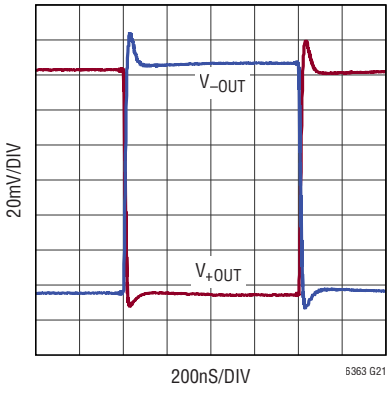
Frequency Peaking vs Load Capacitance and Series Output Resistance



Open-Loop Gain and Phase vs Frequency

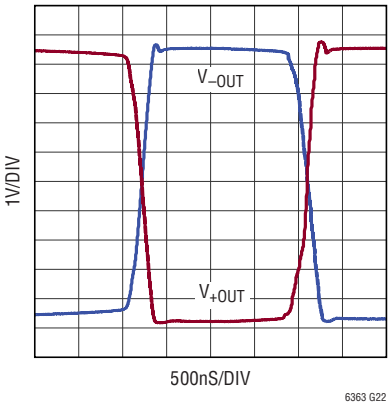


Small-Signal Step Response



V_S = ±5V
V_{ICM} = V_{OCM} = 0V
R_I = R_F = 1k
R_{LOAD} = 1k
V_{INDIFF} = 250mV_{P-P}
SINGLE-ENDED INPUT

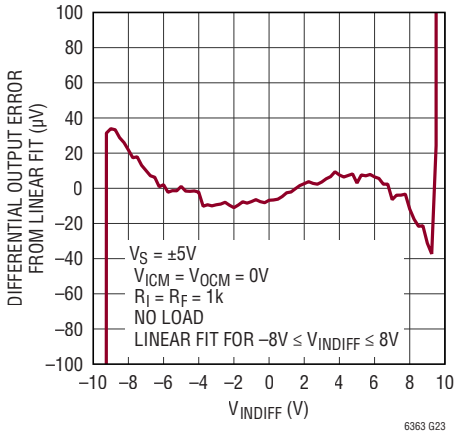
Large-Signal Step Response



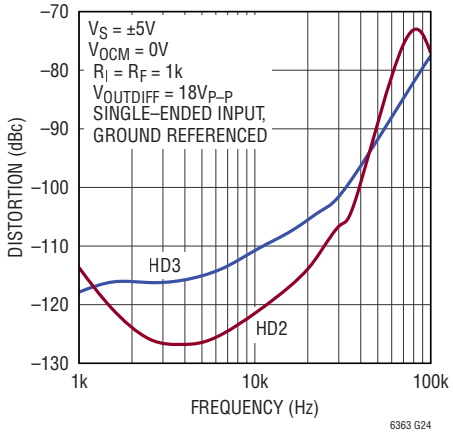
V_S = ±5V
V_{ICM} = V_{OCM} = 0V
R_I = R_F = 1k
R_{LOAD} = 1k
V_{INDIFF} = 18V_{P-P}
SINGLE-ENDED INPUT

TYPICAL PERFORMANCE CHARACTERISTICS

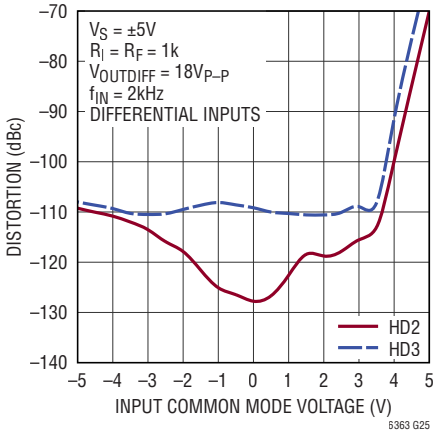
DC Linearity



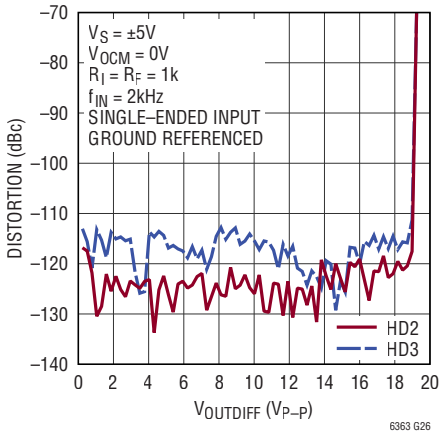
Harmonic Distortion vs Frequency



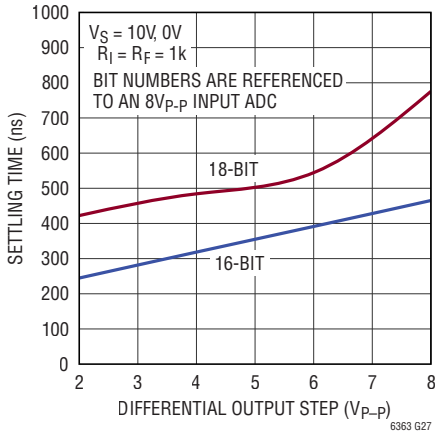
Harmonic Distortion vs Input Common Mode Voltage



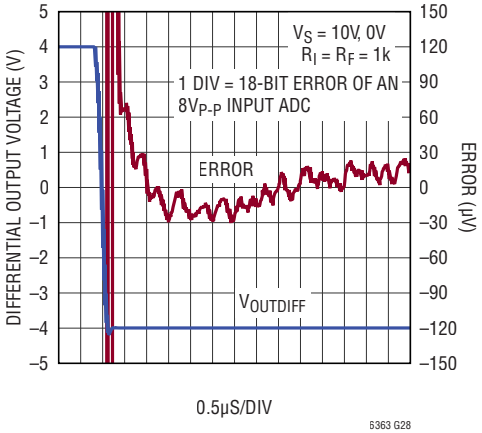
Harmonic Distortion vs Output Amplitude



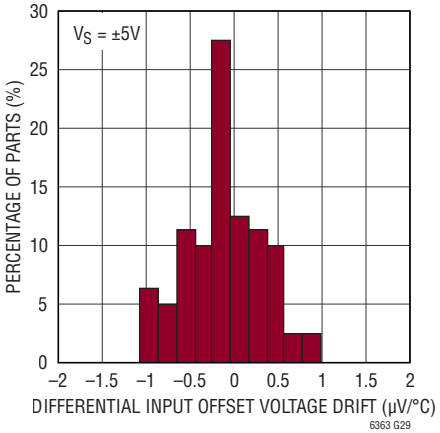
Settling Time vs Output Step



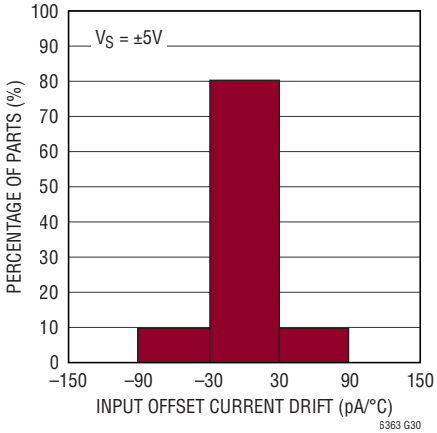
Settling Time to 8VP-P Output Step



Typical Distribution of Differential Input Offset Voltage Drift



Typical Distribution of Input Offset Current Drift



PIN FUNCTIONS

–IN (Pin 1): Inverting Input of Amplifier.

V_{OCM} (Pin 2): Output Common Mode Reference Voltage. Apply a voltage to this pin to set the output common mode voltage level. If left floating, an internal resistor divider develops a default voltage approximately halfway between V^+ and $V^–$.

V^+ (Pin 3): Positive Power Supply. Operational supply range is 2.8V to 11V when $V^–$ = 0V.

+OUT (Pin 4): Positive Output Pin. Output capable of swinging rail-to-rail.

–OUT (Pin 5): Negative Output Pin. Output capable of swinging rail-to-rail.

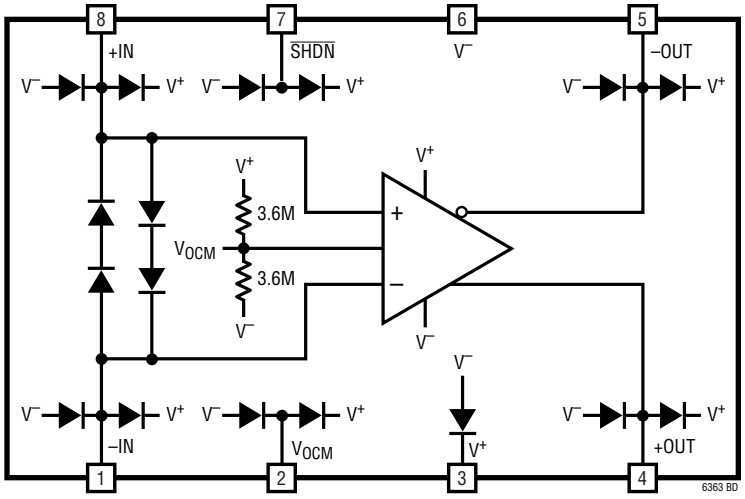
$V^–$ (Pin 6/Exposed Pad Pin 9): Negative Power Supply. Negative supply can be negative as long as 2.8V ≤ (V^+ – $V^–$) ≤ 11V still applies.

$\overline{SHDN}$ (Pin 7): When the $\overline{SHDN}$ pin is floating or driven high, the LTC6363 is in the normal (active) operating mode. When $\overline{SHDN}$ pin is connected to $V^–$ or driven low, the part is disabled and draws approximately 20µA of supply current (V_S = 3V). Refer to $\overline{SHDN}$ Pin in the Applications information section of this data sheet for more details.

+IN (Pin 8): Noninverting Input of Amplifier.

BLOCK DIAGRAM

LTC6363



APPLICATIONS INFORMATION

Functional Description

The LTC6363 is a fully-differential, low power, low-noise, precision amplifier. The amplifier is optimized to convert a fully differential or single-ended signal to a low impedance, balanced differential output suitable for driving high performance, low power differential ΣΔ or SAR ADCs. The balanced differential nature of the amplifier also provides even-order harmonic distortion cancellation, and low susceptibility to common mode noise (e.g. power supply noise).

The outputs of the LTC6363 are capable of swinging rail-to-rail and can source up to 90mA or sink up to 40mA of current. The LTC6363 is optimized for high bandwidth and low power applications. Load capacitances above 50pF to ground or 25pF differentially should be decoupled with 10Ω to 50Ω of series resistance from each output to prevent oscillation or ringing.

$\overline{SHDN}$ Pin

The LTC6363 has a $\overline{SHDN}$ pin which, when tied to V^- or driven to below $(V^+ + V^-)/2 + 0.4V$, will shut down amplifier operation such that only 20µA (at V_S = 3V) to 70µA (at V_S = 10V) is drawn from the supplies. Pull-down circuitry should be capable of sinking at least 12µA to guarantee complete shutdown over all conditions. For normal amplifier operation, the $\overline{SHDN}$ pin should be either:

a) Bypassed with a 0.1uF capacitor to ground

b) Driven to $(V^+ + V^-)/2 + 1.2V$ after supply voltages have been established for 30ms or longer.

This will ensure that the LTC6363 will power up in normal operation under any operating condition of temperature and supply voltage and will additionally prevent noise pickup and supply rail transients from inadvertently shutting down the amplifier. Do not tie the $\overline{SHDN}$ pin directly to the positive supply (V^+).

General Amplifier Applications

In Figure 1, the gain to $V_{OUTDIFF}$ from V_{INP} and V_{INM} is given by:

$$V_{OUTDIFF} = V_{+OUT} - V_{-OUT} \approx \left(\frac{R_F}{R_I}\right) \bullet \left(V_{INP} - V_{INM}\right)$$

Note from the previous equation, the differential output voltage ($V_{+OUT} - V_{-OUT}$) is independent of input and output common mode voltages, or the voltage at the common mode pin. This makes the LTC6363 ideally suited for pre-amplification, level shifting and conversion of single-ended signals to differential output signals for driving differential input ADCs.

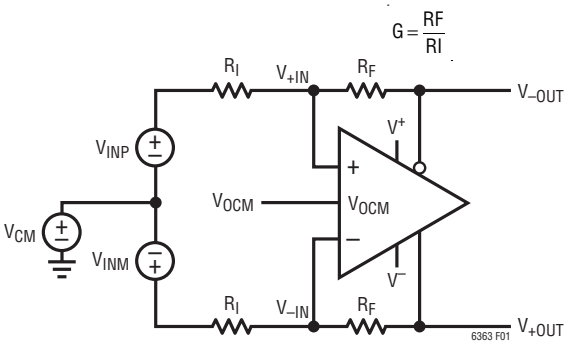


Figure 1. Definitions and Terminology

Output Common Mode and V_{OCM} Pin

The output common mode voltage is defined as the average of the two outputs:

$$V_{OUTCM} = \left(\frac{V_{+OUT} + V_{-OUT}}{2}\right) = V_{OCM}$$

As the equation shows, the output common mode voltage is independent of the input common mode voltage, and is instead determined by the voltage on the V_{OCM} pin, by means of an internal common mode feedback loop.

If the V_{OCM} pin is left open, an internal resistor divider develops a default voltage of approximately halfway between V^+ and V^-. The V_{OCM} pin can be overdriven to another voltage if desired for greater accuracy or flexibility. For example, when driving an ADC, if the ADC makes a reference available for setting the common mode voltage, it can be directly tied to the V_{OCM} pin, as long as the ADC is capable of driving the 1.8M input resistance presented by the V_{OCM} pin. The Electrical Characteristics table specifies the valid range that can be applied to the V_{OCM} pin (V_{OUTCMR}).

APPLICATIONS INFORMATION

Input Common Mode Voltage Range

The LTC6363's input common mode voltage (V_{ICM}) is defined as the average of the two input pins, V_{+IN} and $V_{–IN}$. The inputs of the LTC6363 are capable of swinging over the range defined in the Electrical Characteristics table (see V_{ICMR}). Due to the external resistive divider action of the gain and feedback resistors, the effective range of signals that can be processed is wider than the provided range. The input common mode range at the op amp inputs depends on the circuit configuration (G = gain), V_{OCM}, and V_{CM} (refer to Figure 1). For fully differential input applications, where $V_{INP} = –V_{INM}$, the common mode input is approximately:

$$V_{ICM} = V_{CM} \bullet \frac{G}{G+1} + V_{OCM} \bullet \frac{1}{G+1}$$

For single-ended applications, where $V_{INM} = 0$, the input common mode voltage also depends on the input signal. In this case, the input common mode voltage at the input pins of the LTC6363 is approximately :

$$V_{ICM} = \left(V_{CM} + V_{INP}/2\right) \bullet \frac{G}{G+1} + V_{OCM} \bullet \frac{1}{G+1}$$

If, for example, the input signal (V_{INP}) is a sinusoid, an attenuated version of that sinusoid also appears at the LTC6363 inputs.

In general, V_{CM} (refer to Figure 1) is valid if it satisfies the following inequality:

$$V^- \frac{G+1}{G} - \frac{V_{OCM}}{G} \le V_{CM} \le \left(V^+ - 1.2\right)\frac{G+1}{G} - \frac{V_{OCM}}{G}$$

Input Pin Protection

The input stage of the LTC6363 op amp is protected against differential input voltages which exceed 1.4V by two pairs of series diodes connected back-to-back between +IN and –IN. If the differential input voltage exceeds 1.4V, the input current should be limited to under 10mA to prevent damage to the IC. Moreover, all pins have clamping diodes to both power supplies. If any pin is driven to voltages which exceed either supply, the current should be limited to under 10mA to prevent damage to the IC.

Input Impedance and Loading Effects

The low frequency input impedance looking into the V_{INP} or V_{INM} input of Figure 1 depends on how the inputs are driven. For fully differential input sources ($V_{INP} = –V_{INM}$), the input impedance seen at either input is simply:

$$R_{INP} = R_{INM} = R_I$$

For single-ended inputs, due to the signal imbalance at the input, the input impedance increases over the balanced differential case. The input impedance looking into either input is:

$$R_{INP} = R_{INM} = \frac{R_I}{1 - \left(\frac{1}{2}\right) \bullet \left(\frac{R_F}{R_I + R_F}\right)}$$

Input signal sources with non-zero impedances can also cause feedback imbalance between the pair of feedback networks. For the best performance, it is recommended that the input source impedance be compensated. If impedance matching is required at the source, a termination resistor R1 should be chosen (see Figure 2) such that:

$$R1 = \frac{R_{INM} \bullet R_S}{R_{INM} - R_S}$$

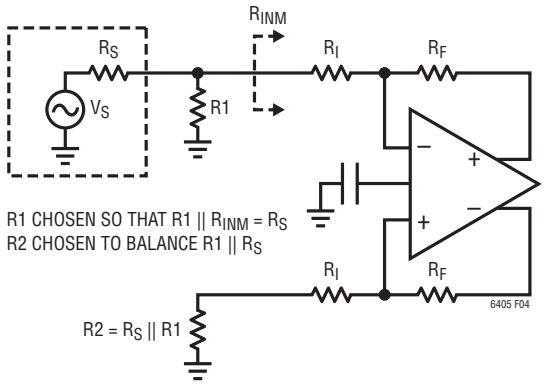


Figure 2. Optimal Compensation for Signal Source Impedance

APPLICATIONS INFORMATION

According to Figure 2, the input impedance looking into the differential amp (R_{INM}) reflects the single-ended source case, given above. Also, R2 is chosen as:

$$R2 = R1 || R_S = \frac{R1 \bullet R_S}{R1 + R_S}$$

Effects of Resistor Pair Mismatch

Figure 3 shows a circuit diagram which takes into consideration resistors mismatch. Often, resistor mismatch limits CMRR well below amplifier specifications. Assuming infinite open-loop gain, the differential output relationship is given by the equation:

$$V_{OUT(DIFF)} = V_{+OUT} - V_{-OUT}$$

$$\approx V_{INDIFF} \bullet \frac{R_F}{R_I} + V_{CM} \bullet \frac{\Delta\beta}{\beta_{AVG}} - V_{OCM} \bullet \frac{\Delta\beta}{\beta_{AVG}}$$

where R_F is the average of R_{F1} and R_{F2}, and R_I is the average of R_{I1} and R_{I2}.

β_{AVG} is defined as the average feedback factor from the outputs to their respective inputs:

$$\beta_{AVG} = \frac{1}{2} \bullet \left(\frac{R_{I1}}{R_{I1} + R_{F1}} + \frac{R_{I2}}{R_{I2} + R_{F2}} \right)$$

$\Delta\beta$ is defined as the difference in the feedback factors:

$$\Delta\beta = \frac{R_{I2}}{R_{I2} + R_{F2}} - \frac{R_{I1}}{R_{I1} + R_{F1}}$$

Here, V_{CM} and V_{INDIFF} are defined as the average and the difference of the two input voltages V_{INP} and V_{INM}, respectively:

$$V_{CM} = \frac{V_{INP} + V_{INM}}{2}$$

$$V_{INDIFF} = V_{INP} - V_{INM}$$

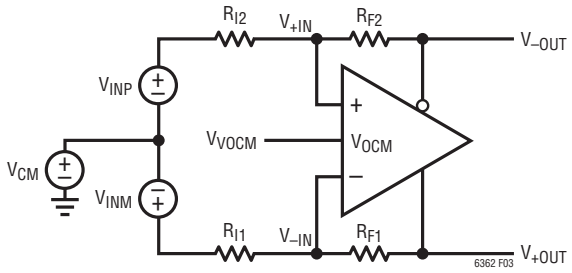


Figure 3. Real-World Application with Feedback Resistor Pair Mismatch

When the feedback ratios mismatch ($\Delta\beta$), common mode to differential conversion occurs. Setting the differential input to zero (V_{INDIFF} = 0), the degree of common mode to differential conversion is given by the equation:

$$V_{OUTDIFF} \approx (V_{CM} - V_{OCM}) \bullet \Delta\beta/\beta_{AVG}$$

In general, the degree of feedback pair mismatch is a source of common mode to differential conversion of both signals and noise. For instance, Table 1 shows the worst-case, resistor limited CMRR of the LTC6363 amplifier configured in a gain of 1 using external resistors.

Table 1.

Tolerance	CMRR
5%	20dB
1%	34dB
0.1%	54dB
0.01%	74dB
LT5400	86dB
0.001%	94dB

A low impedance ground plane should be used as a reference for both the input signal source and the V_{OCM} pin.

APPLICATIONS INFORMATION

Noise

The LTC6363's differential input referred voltage and current noise densities are 2.9nV/√Hz and 0.55pA/√Hz, respectively. In addition to the noise generated by the amplifier, the surrounding feedback resistors also contribute noise. A simplified noise model is shown in Figure 4. The output noise generated by both the amplifier and the feedback components is given by the equation:

$$e_{no} = \sqrt{\left[e_{ni} \bullet \left(1+\frac{R_F}{R_I}\right)\right]^2 + 2 \bullet \left(i_n \bullet R_F\right)^2 + 2 \bullet \left[e_{nRI} \bullet \frac{R_F}{R_I}\right]^2 + 2 \bullet e_{nRF}^{\,2}}$$

For example, if $R_F = R_I = 1k$, the output noise of the circuit $e_{no} = 10nV/\sqrt{Hz}$.

If the circuits surrounding the amplifier are well balanced, common mode noise (e_{nvocm}) does not appear in the differential output noise equation given above.

The LTC6363's input referred voltage noise contributes the equivalent noise of a 510Ω resistor. When the feedback network is comprised of resistors whose values are larger than this, the output noise is resistor noise and amplifier current noise dominant. For feedback networks consisting of resistors with values smaller than 510Ω, the output noise is voltage noise dominant.

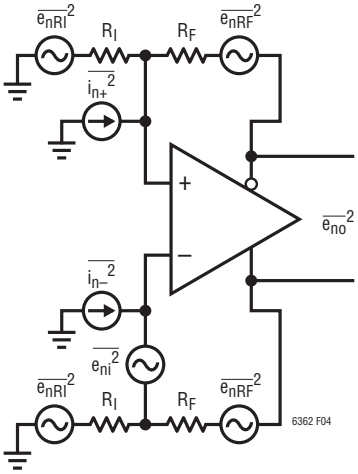


Figure 4. Simplified Noise Model

Lower resistor values always result in lower noise at the penalty of increased distortion due to increased loading of the feedback network on the output. Higher resistor values will result in higher output noise, but typically improved distortion due to less loading on the output.

GBW vs f_{-3dB}

Gain-bandwidth product (GBW) and –3dB frequency (f_{-3dB}) have been specified in the Electrical Characteristics table as two different metrics for the speed of the LTC6363. GBW is obtained by measuring the open-loop gain of the amplifier at a specific frequency (f_{TEST}), then calculating gain • f_{TEST}. GBW is a parameter that depends only on the internal design and compensation of the amplifier and is a suitable metric to specify the inherent speed capability of the internal amplifier.

Of more practical interest, f_{-3dB} is the frequency at which the closed-loop gain is 3dB lower than its low frequency value. The value of f_{-3dB} depends on the speed of the internal amplifier as well as the feedback factor.

In most amplifiers, the open-loop gain response exhibits a conventional single-pole roll-off for most of the frequencies before the unity-gain crossover frequency, and the GBW and unity-gain frequency are close to each other. However, the LTC6363 is intentionally compensated in such a way that its GBW is significantly larger than its f_{-3dB} in a closed loop gain of 1. This means that at lower frequencies where the amplifier inputs generally operate, the amplifier's gain and thus the feedback loop gain is larger. This further linearizes the amplifier and improves distortion at those frequencies.

APPLICATIONS INFORMATION

Feedback Capacitors

When the combination of parasitic capacitances (device + PCB) at the LTC6363's inputs form a pole whose frequency lies within the closed-loop bandwidth of the amplifier, a capacitor (C_F) can be added in parallel with the external feedback resistors (R_F) to cancel the degradation on stability. C_F should be chosen such that it generates a zero at a frequency close to the frequency of the pole.

Board Layout and Bypass Capacitors

For single supply applications, it is recommended that high quality 0.1µF ceramic bypass capacitors be placed directly between the V^+ and the $V^–$ pin with short connections. The $V^–$ pin should be tied directly to a low impedance ground plane with minimal routing. For dual (split) power supplies, it is recommended that additional high quality 0.1µF ceramic capacitors be used to bypass V^+ to ground and $V^–$ to ground, again with minimal routing. Small geometry (e.g., 0603) surface mount ceramic capacitors have a much higher self-resonant frequency than leaded capacitors, and perform best with the LTC6363.

To prevent degradation in stability response, it is highly recommended that any stray capacitance at the LTC6363's input pins, +IN and –IN, be kept to an absolute minimum by keeping printed circuit connections as short as possible.

At the output, always keep in mind the differential nature of the LTC6363, because it is critical that the load impedances seen by both outputs (stray or intended), be as balanced and symmetric as possible. This will help preserve the balanced operation of the LTC6363 that minimizes the generation of even-order harmonics and maximizes the rejection of common mode signals and noise.

The V_{OCM} pin should be bypassed to the ground plane with a high quality 0.1µF ceramic capacitor. This will prevent common mode signals and noise on this pin from being inadvertently converted to differential signals and noise by impedance mismatches both externally and internally to the IC.

Power Dissipation

Due to the wide supply voltage range, it is possible for the LTC6363 to exceed the maximum junction temperature under certain conditions. Maximum junction temperature (T_J) is calculated from the ambient temperature (T_A) and power dissipation (P_D) as follows: $T_J = T_A + (P_D \bullet \theta_{JA})$. The power dissipation in the IC is a function of the supply voltage, output voltage and the load, input and feedback resistances. For a given supply voltage, the worst-case power dissipation, $P_{D(MAX)}$, occurs at the maximum quiescent supply current and at an output voltage which is half of either supply voltage (or the maximum swing if it is less than half the supply voltage). In this condition, the LTC6363 will supply current to the load resistors and the input and feedback resistors, R_I and R_F. $P_{D(MAX)}$ is given by:

$$P_{D(MAX)} = \left(V^+ - V^-\right)\left(I_{S(MAX)}\right) + 2 \bullet \frac{\left(\frac{V^+}{2}\right)^2}{R_L} + 2 \bullet \frac{\left(\frac{V^+}{2}\left(1 + \frac{R_I}{R_F}\right)\right)^2}{R_I + R_F}$$

Example: An LTC6363HMS8 in the 8-Lead MSOP package has a thermal resistance of θ_{JA} = 273°C/W. Operating on ±5V supplies, with $R_I = R_F$ = 1k, and driving a 1k load to ground at each output, the worst-case power dissipation is given by:

$$P_{D(MAX)} = (10V)(2.2mA) + 2 \bullet \frac{(2.5V)^2}{1000\Omega} + 2 \bullet \frac{(5V)^2}{2000\Omega}$$
$$= 60mW$$

In this example, the maximum ambient temperature that the part is allowed to operate is:

$T_A = T_J – (P_{D(MAX)} \bullet 273°C/W)$

$T_A = 150°C – (60mW)(273°C/W) = 133.6°C$

To operate the device at a higher ambient temperature for the same conditions, use the LTC6363 in the 8-Lead DFN package.

APPLICATIONS INFORMATION

Interfacing to ADCs

When driving an ADC, an additional passive filter should be used between the outputs of the LTC6363 and the inputs of the ADC. Depending on the application, a single-pole RC filter will often be sufficient. The sampling process of ADCs creates a charge transient due to the switching in of the ADC sampling capacitor. This momentarily creates high frequency current pulses at the output of the amplifier as charge is transferred between amplifier and sampling capacitor. The amplifier must recover and settle from this load transient before the acquisition period has ended for a valid representation of the input signal. The RC network between the outputs of the driver and the inputs of the ADC decouples this sampling transient (see Figure 5). The capacitance serves to provide the bulk of the charge during the sampling process, and the two resistors at the outputs of the LTC6363 are used to dampen and attenuate any charge injected by the ADC. Additionally, the RC filter band limits broadband output noise.

The selection of an appropriate filter depends on the specific ADC, and the following procedure is suggested for choosing filter component values. Begin by selecting an appropriate RC time constant for the input signal. Generally, longer time constants improve SNR at the expense of settling time. Output transient settling to 20-bit accuracy will require nearly 14 RC time constants to completely settle. To select the resistor value, remember the resistors in the decoupling network should be at least 10Ω. Keep in mind that these resistors also serve to decouple the LTC6363 outputs from load capacitance. Too large of a resistor will leave insufficient settling time. Too small of a resistor will not properly dampen the load transient of the sampling process, prolonging the time required for settling. For lowest distortion, choose capacitors with low dielectric absorption (such as a C0G multilayer ceramic capacitor). In general, large capacitor values attenuate the fixed nonlinear charge kickback, however very large capacitor values will detrimentally load the driver at the desired input frequency and cause driver distortion. Smaller input swings will allow for larger filter capacitor values due to decreased loading demands on the driver. This property may be limited by the particular input amplitude dependence of differential nonlinear charge kickback for the specific ADC.

In some applications, placing series resistors at the inputs of the ADC may further improve distortion performance. These series resistors function with the ADC sampling capacitor to filter potential ground bounce or other high speed sampling disturbances. Additionally, the resistors limit the rise time of residual filter glitches that manage to propagate to the driver outputs. Restricting possible glitch propagation rise time to within the small signal bandwidth of the driver enables less disturbed output settling.

For the specific application of LTC6363 driving the LTC2378-20 SAR ADC, the recommended component values of the RC filter are provided in Figure 5. These component values are chosen for optimal distortion and noise performance.

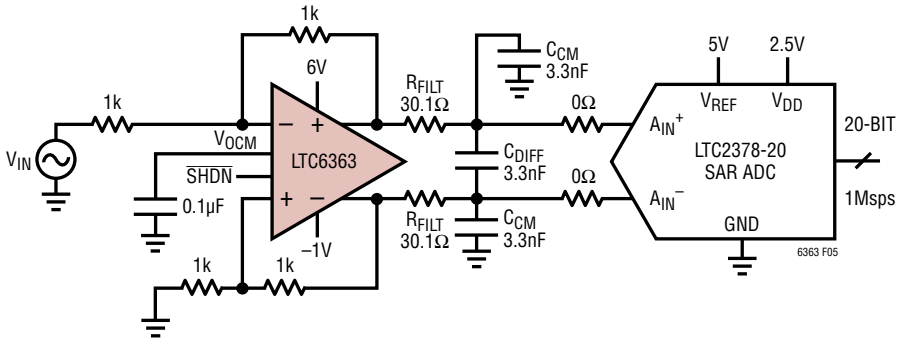
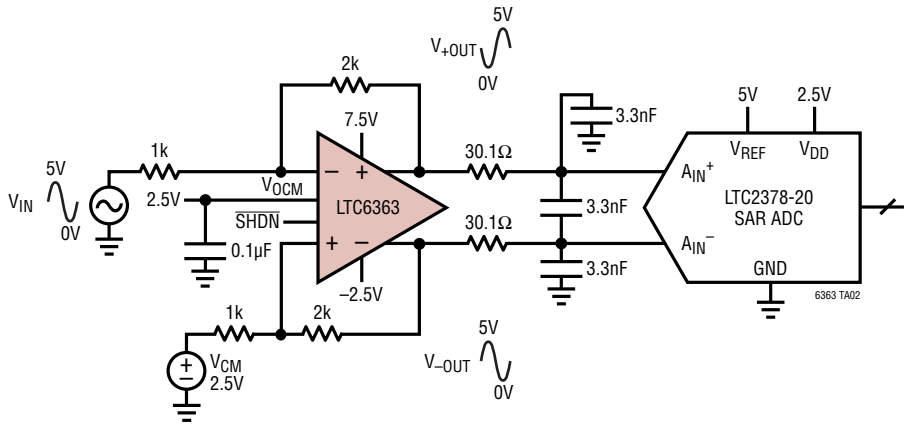


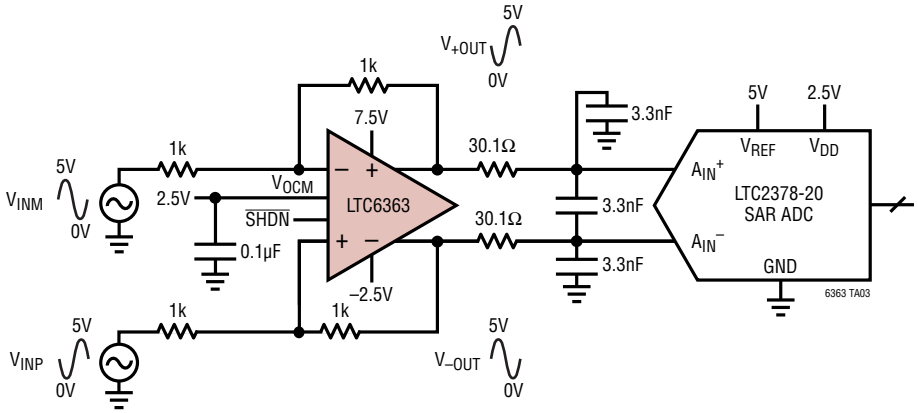
Figure 5. Recommended Interface Solution for Driving the LTC2378-20 SAR ADC

TYPICAL APPLICATIONS

Single-Ended-to-Differential Conversion of a $5V_{P-P}$, 2.5V Referenced Input with Gain of $A_V = 2$ to Drive an ADC

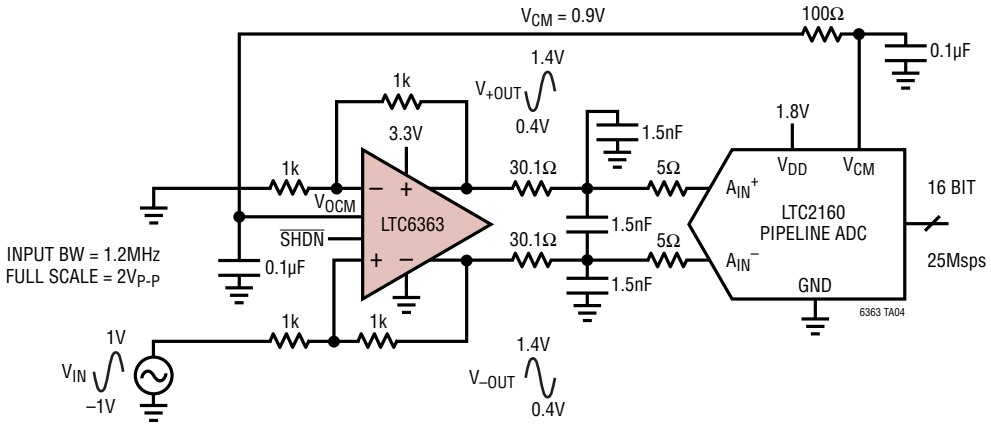


Differentially Driving an ADC with $\Delta V_{IN} = 10V_{P-P}$ and Gain of $A_V = 1$



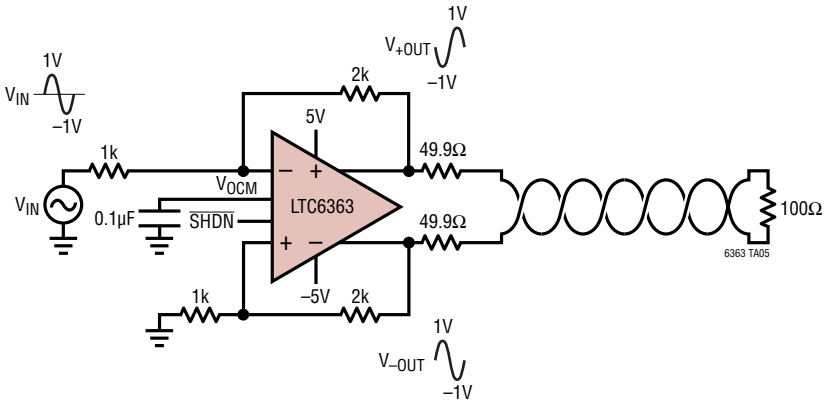
TYPICAL APPLICATIONS

Differentially Driving a Pipeline ADC with $A_V = 1$



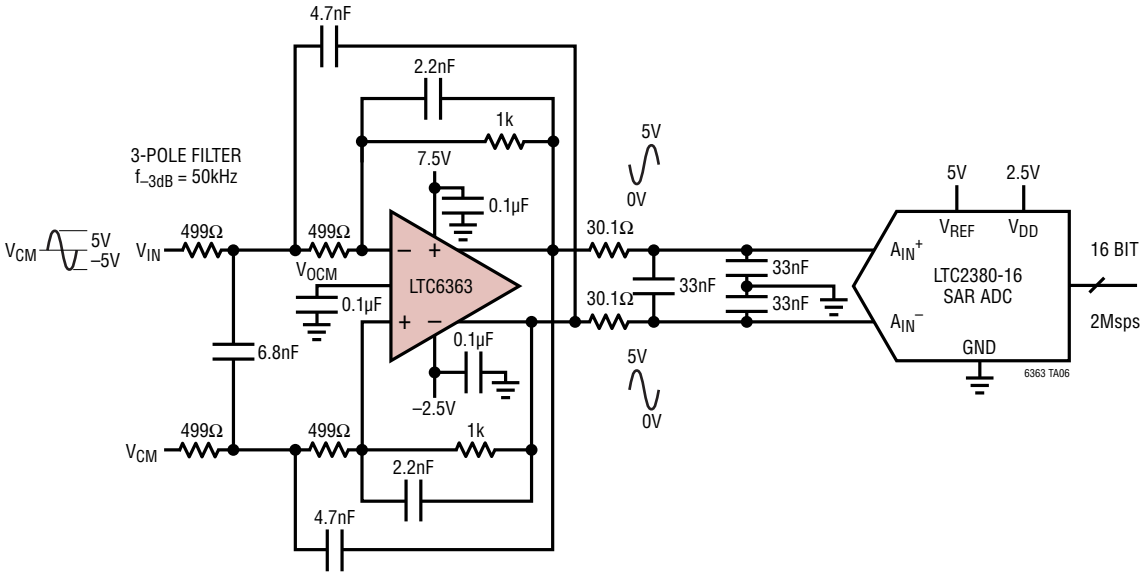
MEASURED PERFORMANCE FOR LTC6363 DRIVING LTC2160:
INPUT: f_{IN} = 2kHz, –1dBFS
SNR: 77dB
HD2: –100.0dBc
HD3: –100.2dBc
THD: –96.5dB

Differential Line Driver Connected in Gain of $A_V = 2$

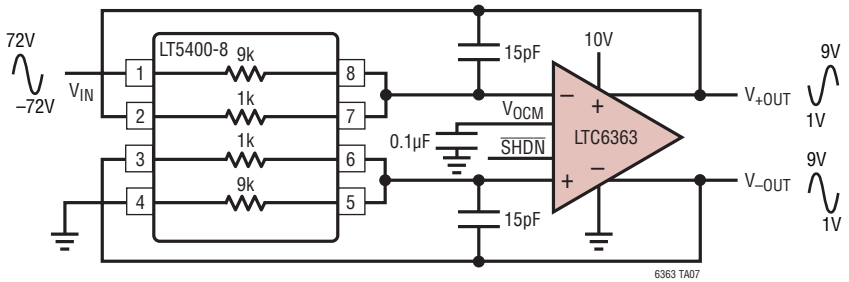


TYPICAL APPLICATIONS

LTC6363 Used as Lowpass Filter/Driver with 10V$_{P-P}$ Singled-Ended Input, Driving a SAR ADC



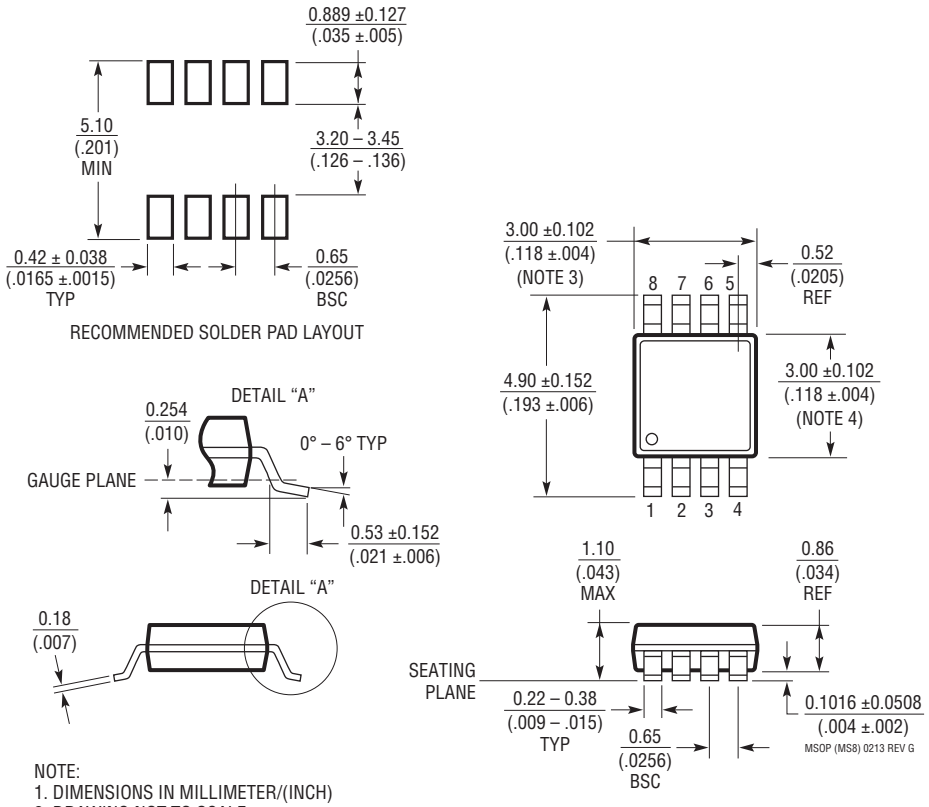
Differential A$_V$ = 1/9 Configuration Using an LT®5400 Quad-Matched Resistor Network



PACKAGE DESCRIPTION

Please refer to http://www.linear.com/designtools/packaging/ for the most recent package drawings.

MS8 Package
8-Lead Plastic MSOP
(Reference LTC DWG # 05-08-1660 Rev G)

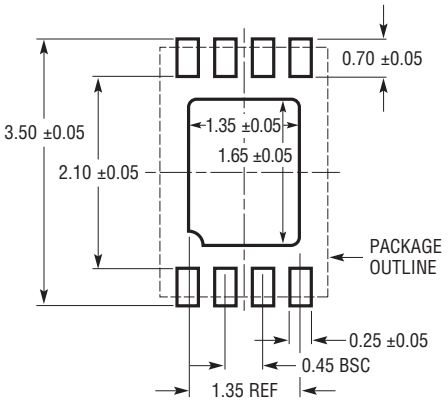


NOTE:
1. DIMENSIONS IN MILLIMETER/(INCH)
2. DRAWING NOT TO SCALE
3. DIMENSION DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
   MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.152mm (.006") PER SIDE
4. DIMENSION DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS.
   INTERLEAD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.152mm (.006") PER SIDE
5. LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.102mm (.004") MAX

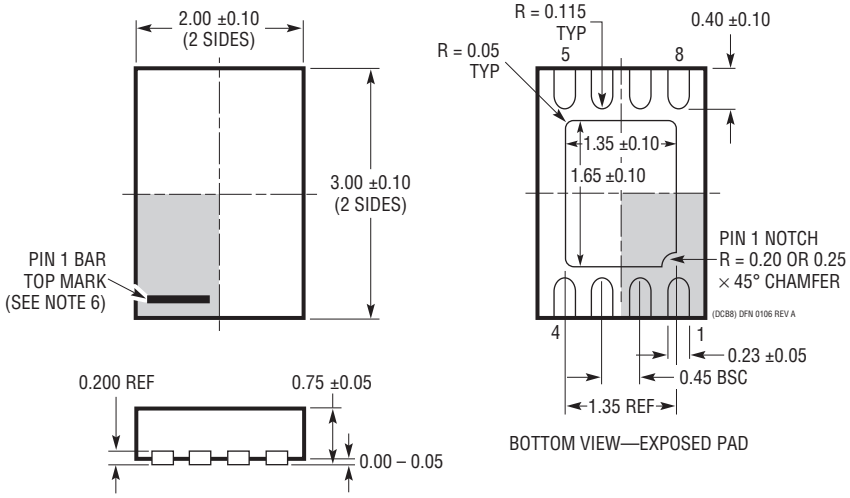
PACKAGE DESCRIPTION

Please refer to http://www.linear.com/designtools/packaging/ for the most recent package drawings.

DCB Package
8-Lead Plastic DFN (2mm × 3mm)
(Reference LTC DWG # 05-08-1718 Rev A)



RECOMMENDED SOLDER PAD PITCH AND DIMENSIONS
APPLY SOLDER MASK TO AREAS THAT ARE NOT SOLDERED

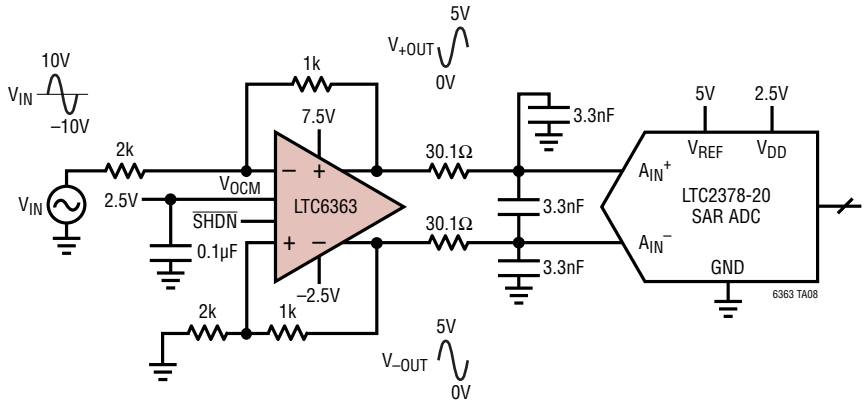


BOTTOM VIEW—EXPOSED PAD

NOTE:
1. DRAWING IS NOT A JEDEC PACKAGE OUTLINE
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE

TYPICAL APPLICATION

Single-Ended-to-Differential Conversion of a 20V_{P-P} Ground-Referenced Input with Gain of A_V = 0.5 to Drive an ADC



RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
Fully Differential Amplifiers		
LTC6362	Precision, Low Power Rail-to-Rail Input/Output Differential Op Amp/SAR ADC Driver	1mA, -116 dBc Distortion at 1kHz, 8V_{P-P} Output
LTC1992/LTC1992-X	3MHz to 4MHz Fully Differential Input/Output Amplifiers	Internal Feedback Resistors Available (G =1, 2, 5,10)
LT1994	70MHz Low Noise, Low Distortion Fully Differential Input/Output Amplifier/Driver	13mA, –94dBc Distortion at 1MHz, 2V_{P-P} Output
Operational Amplifiers		
LT6350	Low Noise, Single-Ended to Differential Converter/ ADC Driver	4.8mA, –97dBc Distortion at 100kHz, 4V_{P-P} Output
LTC6246/LTC6247/ LTC6248	Single/Dual/Quad 180MHz Rail-to-Rail Low Power Op Amps	1mA/Amplifier, 4.2nV/$\sqrt{Hz}$
LTC6360	1GHz Very Low Noise Single-Ended SAR ADC Driver with True Zero Output	13.6mA, HD2/HD3 = –103dBc/–109dBc at 40kHz, 4V_{P-P} Output
Matched Resistor Networks		
LT5400	Precision Quad Matched Resistor Networks	Ratios = 1:1, 1:4, 1:5, 1:9, 1:10
ADCs		
LTC2378-20	20-Bit, 1Msps, Low Power SAR ADC with 0.5ppm INL	2.5V Supply, Differential Input, 104dB SNR, ±5V Input Range, DGC, Pin Compatible Family in MSOP-16 and 4mm × 3mm DFN-16 Packages
LTC2379-18/LTC2378-18 LTC2377-18/LTC2376-18	18-Bit, 1.6Msps/1Msps/500ksps/250ksps Serial, Low Power ADC	2.5V Supply, Differential Input, 101.2dB SNR, ±5V Input Range, DGC, Pin Compatible Family in MSOP-16 and 4mm × 3mm DFN-16 Packages
LTC2380-16/LTC2378-16 LTC2377-16/LTC2376-16	16-Bit, 2Msps/1Msps/500ksps/250ksps Serial, Low Power ADC	2.5V Supply, Differential Input, 96.2dB SNR, ±5V Input Range, DGC, Pin Compatible Family in MSOP-16 and 4mm × 3mm DFN-16 Packages
LTC2393-16/LTC2392-16 /LTC2391-16	16-Bit, 1Msps/500ksps/250ksps Parallel/Serial ADC	5V Supply, Differential Input, 94dB SNR, ±4.096V Input Range, Pin Compatible Family in 7mm × 7mm LQFP-48 and QFN-48 Packages
LTC2383-16/LTC2382-16 /LTC2381-16	16-Bit, 1Msps/500ksps/250ksps Serial, Low Power ADC	2.5V Supply, Differential Input, 92dB SNR, ±2.5V Input Range, Pin Compatible Family in MSOP-16 and 4mm × 3mm DFN-16 Packages
LTC2355-14/LTC2356-14	14-Bit, 3.5Msps Serial ADC	3.3V Supply, 1-Channel, Unipolar/Bipolar, 18mW, MSOP-10 Package
LTC2366	12-Bit, 3Msps Serial ADC	2.35V to 3.6V Supply 6- and 8-Lead TSOT-23 Packages
LTC2162/LTC2161/ LTC2160	16-Bit, 65/40/25Msps Low Power ADC	1.8V Supply, Differential Input, 77dB SNR, 2V_{P-P} Input Range, Pipeline Converter in 7mm × 7mm QFN-48 Package

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