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## NTE5550 thru NTE5558 Silicon Controlled Rectifier (SCR) 25 Amp, TO220

**Description:**

The NTE5550 thru NTE5558 SCR's are designed primarily for half-wave AC control applications, such as motor controls, heating controls and power supply crowbar circuits.

**Features:**

- Glass Passivated Junctions with Center Gate Fire for Greater Parameter Uniformity and Stability.
- Small, Rugged, Thermowatt Constructed for Low Thermal Resistance, High Heat Dissipation and Durability.
- Blocking Voltage to 800 Volts
- 300A Surge Current Capability

**Absolute Maximum Ratings:**

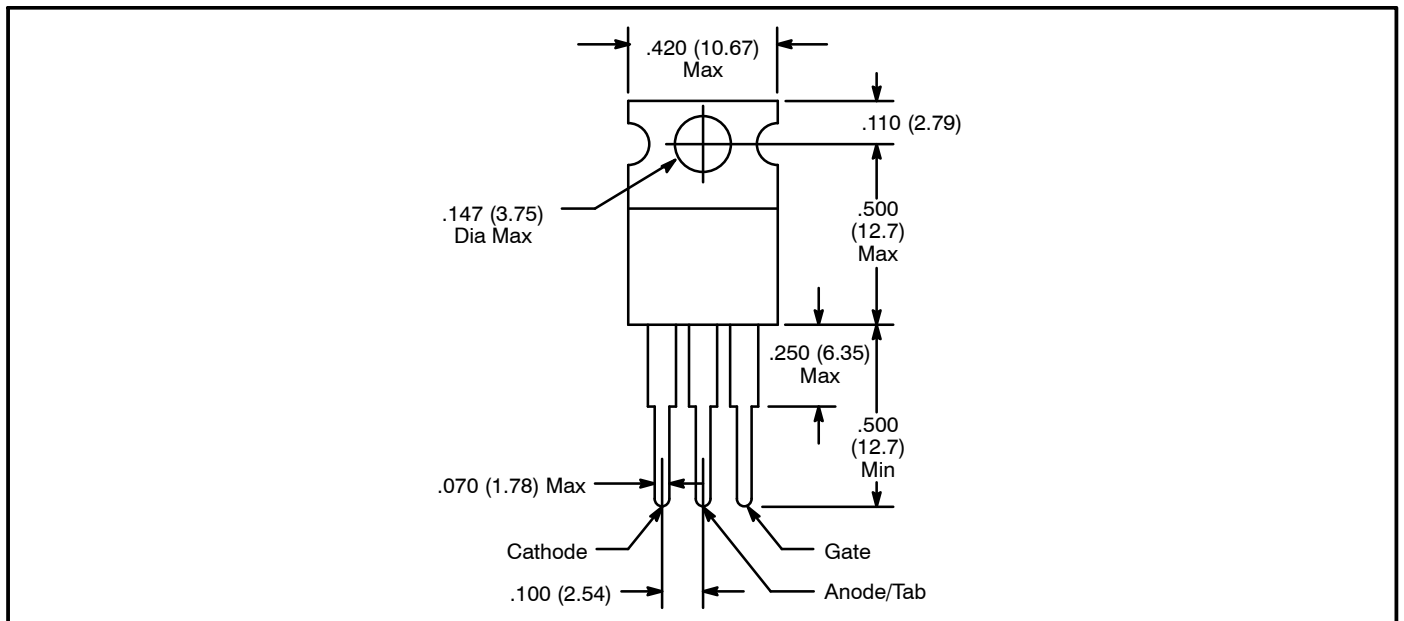
Peak Reverse Blocking Voltage (Note 1), $V_{RRM}$	
NTE5550 .....	50V
NTE5552 .....	200V
NTE5554 .....	400V
NTE5556 .....	600V
NTE5558 .....	800V
Forward Current ( $T_C = +85^\circ\text{C}$ ), $I_{T(RMS)}$ .....	25A
(All Conduction Angles), $I_{T(AV)}$ .....	16A
Peak Non-Repetitive Surge Current (8.3ms), $I_{TSM}$ .....	300A
(1/2 Cycle, Sine Wave, 1.5ms) .....	350A
Forward Peak Gate Power, $P_{GM}$ .....	20W
Forward Average Gate Power, $P_{G(AV)}$ .....	0.5W
Forward Peak Gate Current, $I_{GM}$ .....	2A
Operating Junction Temperature Range, $T_J$ .....	$-40^\circ$ to $+125^\circ\text{C}$
Storage Temperature Range, $T_{stg}$ .....	$-40^\circ$ to $+150^\circ\text{C}$
Thermal Resistance, Junction-to-Case, $R_{thJC}$ .....	$1.5^\circ\text{C/W}$

Note 1.  $V_{RRM}$  for all types can be applied on a continuous dc basis without incurring damage. Ratings apply for zero or negative gate voltage. Devices should not be tested for blocking capability in a manner such that the voltage supplied exceeds the rated blocking voltage.

**Electrical Characteristics:** ( $T_C = +25^\circ\text{C}$  unless otherwise noted.)

Parameter	Symbol	Min	Typ	Max	Unit
Peak Forward Blocking Voltage, ( $T_J = +125^\circ\text{C}$ ) NTE5550 NTE5552 NTE5554 NTE5556 NTE5558	$V_{\text{DRM}}$	50 200 400 600 800	- - - - -	- - - - -	V
Peak Forward or Reverse Blocking Current, (Rated $V_{\text{DRM}}$ or $V_{\text{RRM}}$ ) $T_J = +25^\circ\text{C}$ $T_J = +125^\circ\text{C}$	$I_{\text{DRM}}, I_{\text{RRM}}$	- -	- -	10 2	$\mu\text{A}$ mA
Forward "ON" Voltage, ( $I_{\text{TM}} = 50\text{A}$ , Note 2)	$V_{\text{TM}}$	-	-	1.8	V
Gate Trigger Current (Continuous DC), (Anode Voltage = 12Vdc, $R_L = 100\Omega$ ) $T_C = +25^\circ\text{C}$ $T_C = -40^\circ\text{C}$	$I_{\text{GT}}$	- -	- 25	40 75	mA
Gate Trigger Voltage (Continuous DC) (Anode Voltage = 12Vdc, $R_L = 100\Omega$ , $T_C = -40^\circ\text{C}$ )	$V_{\text{GT}}$	-	1	1.5	V
Gate Non-Trigger Voltage (Anode Voltage = Rated $V_{\text{DRM}}$ , $R_L = 100\Omega$ , $T_J = +125^\circ\text{C}$ )	$V_{\text{GD}}$	0.2	-	-	V
Holding Current (Anode Voltage = 12Vdc, $T_C = -40^\circ\text{C}$ )	$I_{\text{H}}$	-	35	40	mA
Turn-On Time ( $I_{\text{TM}} = 25\text{A}$ , $I_{\text{GT}} = 50\text{mA}$ )	$t_{\text{gt}}$	-	1.5	2	$\mu\text{s}$
Turn-Off Time ( $V_{\text{DRM}} = \text{rated voltage}$ ) ( $I_{\text{TM}} = 25\text{A}$ , $I_{\text{R}} = 25\text{A}$ ) ( $I_{\text{TM}} = 25\text{A}$ , $I_{\text{R}} = 25\text{A}$ , $T_J = +125^\circ\text{C}$ )	$t_{\text{q}}$	- -	15 35	- -	$\mu\text{s}$
Critical Rate of Rise of Off-State Voltage (Gate Open, Rated $V_{\text{DRM}}$ , Exponential Waveform)	dv/dt	-	50	-	V/ $\mu\text{s}$

Note 2. Pulse Test: Pulse Width  $\leq 300\mu\text{s}$ , Duty Cycle  $\leq 2\%$ .



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