Dust Networks

Eterna™ Serial Programmer Guide

For use with the following hardware, evaluation or development kits:

DC9010A and DC9010B.

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About This Guide

This document describes the use of the Eterna Serial Programmer hardware (DC9010) and the Eterna Serial Programming software application (ESP). An updated version of this document may be found on Linear Technology website.

Audience

This document is intended for system developers, hardware designers, and software developers.

Background

The Eterna SoC includes 512kB of flash memory similar to general purpose microcontroller devices. Eterna also includes a programming interface that may be enabled by asserting both the RESETn and FLASH_P_ENn signals. This interface provides the fastest method to program images on Eterna based products. All LTC5800 devices will ship with the flash erased and must be programmed to enable operation. All LTP products come pre-programmed and do not require programming prior to operation; however, including support via the recommended 10-pin header for programming of LTP products is strongly recommended. The DC9010 and ESP software have been optimized for fast programming of Eterna.

Eterna requires the use of a 20 MHz crystal oscillator. Eterna includes an internal capacitor array for centering the 20 MHz crystal reference on a layout by layout basis. For each new design, the correct value for the load trim needs to determined to ensure proper operation. The DC9010 provides a method in concert with the product software to determine the correct load trim value for a particular layout.

Supported Products

The DC9010 hardware and the ESP software currently support the following wireless sensor networks products:

- All LTC5800 devices
- LTP5900
- LTP5901
- LTP5902

Related Documents

The following related documents are available:

Eterna Integration Guide

Eterna Board Specific Parameter Configuration Guide

Eterna Serial Programmer Board Files (Schematics…)

Conventions and Terminology

This guide uses the following text conventions:

- `Computer type` indicates information that you enter, such as a URL.
- **Bold type** indicates buttons, fields, and menu commands.
- *Italic type* is used to introduce a new term.
- **Note:** Notes provide more detailed information about concepts.
- **Caution:** Cautions advise about actions that might result in loss of data.
- **Warning:** Warnings advise about actions that might cause physical harm to the hardware or your person.

Revision History

Revision	Date	Description
040-0110 rev 1	2/9/2012	Initial Release
040-0110 rev 2	12/05/12	Added Background, Programmer Hardware and crystal characterization procedure. Corrected read with offset command call.
040-0110 rev 3	3/3/13	Add Eterna Flash Emulator Section Update Target Crystal Characterization
040-0110 rev 4	5/3/13	Added histograms for target crystal calibration
040-0110 rev 5	5/30/13	Editorial changes to target crystal calibration language.
040-0110 rev 6	8/23/13	Add reference to DC9010 on front page Add mxtal usage restriction (radio off)
040-0110 rev 7	11/12/13	Add Hardware Versions section Update document formatting and block diagram

Getting Started

Introduction

The DC9010 Eterna Serial Programmer consists of a enclosed circuit board with a USB micro-B interface and a 2x5 2mm ribbon cable.

The DC9010 allows in-circuit access to an Eterna mote-on-a-chip installed with the programming header recommended in the Eterna Integration Guide.

The DC9010 is used in conjunction with the Eterna Serial Programmer (ESP) software utility herein described.

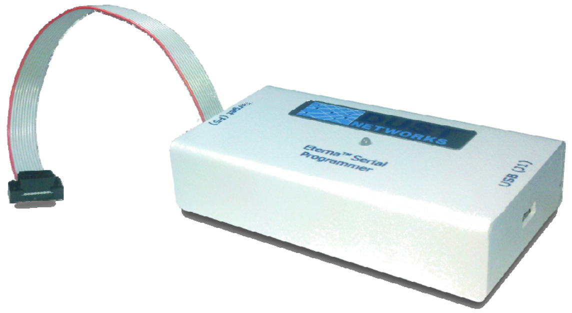
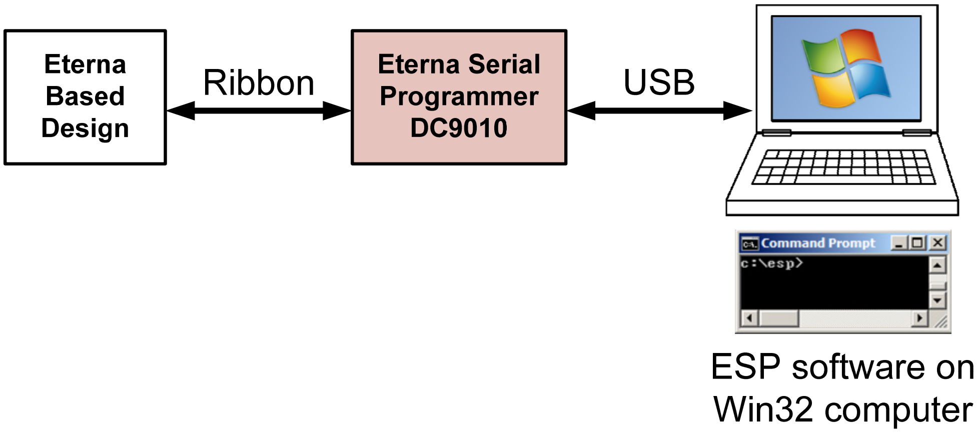


Figure 1 DC9010 Eterna Serial Programmer

Hardware Setup

Connect the DC9010 to the windows PC via USB and connect the target to the DC9010 via the ribbon cable.


Eterna Based Design
Ribbon
Eterna Serial Programmer DC9010
USB
Command Prompt
ESP software on Win32 computer

```
c:\esp>
```

Figure 2 Programming Configuration

Software Installation

ESP software is distributed as a .zip archive and does not require installation. ESP software can be downloaded from http://www.linear.com/designtools/software/#Dust. To install, unarchive all files into a directory (e.g. C:\esp). ESP software calls FTDI, http://www.ftdichip.com/, drivers that are required for operation. The FTDI drivers can be found at http://www.ftdichip.com/Drivers/D2XX.htm and are referred to by FTDI as "D2XX Drivers". ESP software has been tested against D2XX Drivers revision 2.08.14.

The utility should be executed from the directory where you placed the files.

Setup

The Eterna Serial Programming solution is comprised of the Windows ESP.exe application, which in turn use the drivers supported by Future Technology Devices International (FTDI) to interface to the Eterna Serial Programmer via USB. Pairing of USB hardware to drivers is most easily accomplished in most systems by connecting the hardware and following the windows driver installation instructions.

FTDI hardware solutions are very common and as such there is a reasonable chance that the required drivers have already been installed in a system. It should also be noted as the drivers are generic to many solutions, for some of the ESP commands manual notation of the Eterna Serial Programmer's target COM ports is required.

Note that the pairing of the FTDI hardware is done to a specific USB port on a system. Changing of the USB port used to pair the Eterna Serial Programmer to the FTDI driver will result in having to reinstall the driver and additional manual notation of the Eterna Serial Programmer's target COM ports.

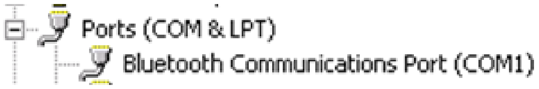
To pair the Eterna Serial Programmer to the FTDI driver on a system:

1) When the installation and mapping of the USB ports is complete, open the Device named Eterna Serial Programmer to find out the COM port numbers that have been assigned to the virtual serial ports. The third COM port number listed will be the COM port used by the ESP application for communications with the Eterna Serial Programmer.

   a. From the Start menu select **Settings → Control Panel → System**.

   b. Click the **Hardware** tab and then click on **Device Manager**.

   c. Open **Ports (COM & LPT)** and note the COM ports – later you will want to indentify the new COM ports that are added after the device drivers have been installed.



Ports (COM & LPT)
Bluetooth Communications Port (COM1)

2) Connect the USB cable between the Eterna Serial Programmer and the system.

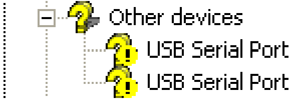
   If four new COM ports appear in the device manager, go to step 7.

   If the Found New Hardware Wizard appears, go to step 3.

   If the Found New Hardware Wizard does not appear, do the following:

a. Ensure that the port is functional, and that the device is connected correctly. If the Wizard still does not appear, open the Windows Device Eterna Serial Programmer to see how Windows has recognized the device.

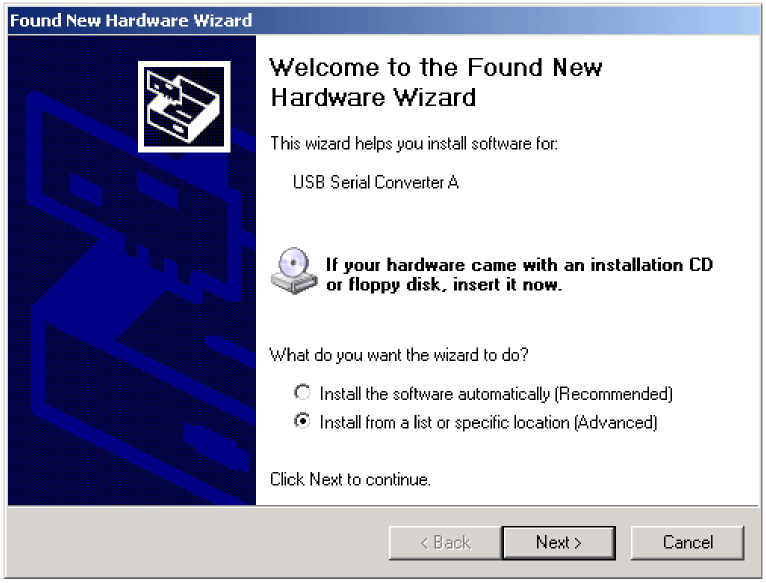
b. If a new “Question Mark Icon” appears , right-click the device and select Update Driver. This displays the Found New Hardware Wizard.



Other devices
- USB Serial Port
- USB Serial Port

c. Go to step 3.

3) In the Wizard, click the option to “Install from a list or specific location,” and click Next.



Found New Hardware Wizard

Welcome to the Found New Hardware Wizard

This wizard helps you install software for:

USB Serial Converter A

If your hardware came with an installation CD or floppy disk, insert it now.

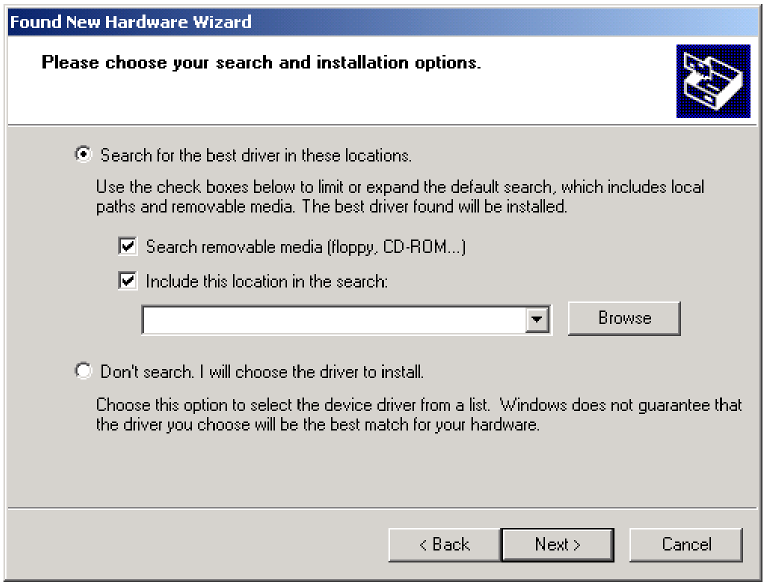
What do you want the wizard to do?

○ Install the software automatically (Recommended)
● Install from a list or specific location (Advanced)

Click Next to continue.

< Back | Next > | Cancel

4) Select the box to “Include this location in the search.” Then, use the Browse button to navigate to the directory where ESP and the associated drivers have been stored , and click Next.



Found New Hardware Wizard

Please choose your search and installation options.

● Search for the best driver in these locations.

Use the check boxes below to limit or expand the default search, which includes local paths and removable media. The best driver found will be installed.

☑ Search removable media (floppy, CD-ROM...)

☑ Include this location in the search:

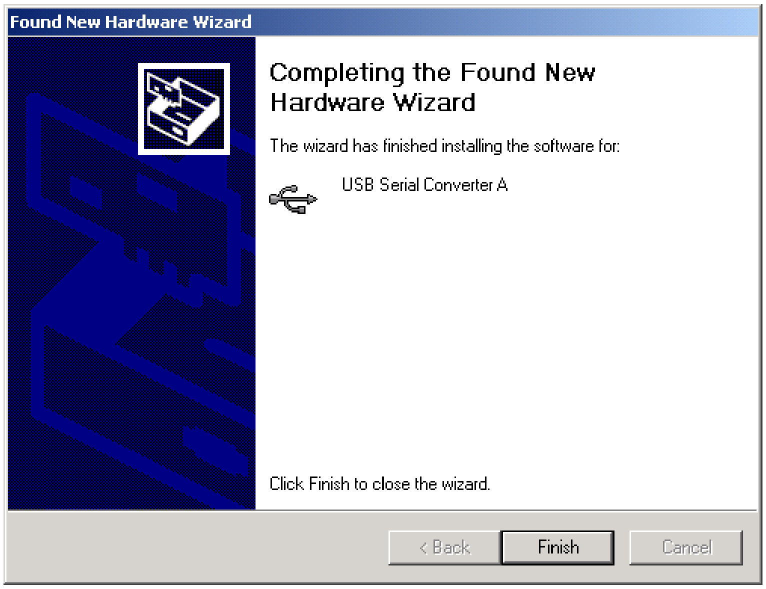
○ Don't search. I will choose the driver to install.

Choose this option to select the device driver from a list. Windows does not guarantee that the driver you choose will be the best match for your hardware.

5) After the Wizard installs the software, click **Finish**.

6) When the Found New Hardware Wizard reappears, repeat steps 2 through 5 to continue the installation. Repeat these steps each time the Wizard appears.

Because of the way Windows works, you may be prompted to go through the Wizard up to eight times to complete the installation and mapping of the USB port. The Eterna Serial Programmer will install a total of four virtual serial ports, along with the USB drivers to control them.



Found New Hardware Wizard

Completing the Found New Hardware Wizard

The wizard has finished installing the software for:

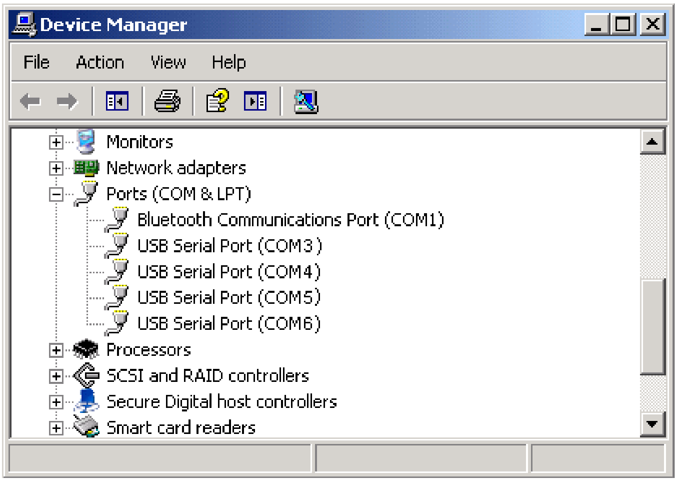
USB Serial Converter A

Click Finish to close the wizard.

7) When the installation and mapping of the USB ports is complete, open the Device Named Eterna Serial Programmer to find out the COM port numbers that have been assigned to the virtual serial ports. The third COM port number listed will be the COM port used by the ESP application for communications with the Eterna Serial Programmer.

a. Make a note of the third COM port identifier.

For example, if the new ports are COM3, COM4, COM5, and COM6, the PORT parameter used in some ESP commands and to initiate crystal characterization will be on COM5.



Monitors
Network adapters
Ports (COM & LPT)
Bluetooth Communications Port (COM1)
USB Serial Port (COM3)
USB Serial Port (COM4)
USB Serial Port (COM5)
USB Serial Port (COM6)
Processors
SCSI and RAID controllers
Secure Digital host controllers
Smart card readers

8) Configure the following Advanced Settings for each of the four new COM ports:

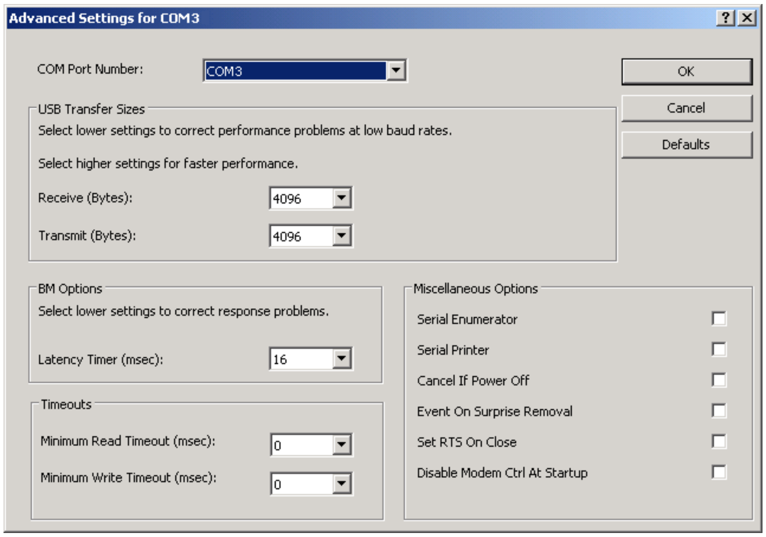
a. **Right-click** on a COM port and click **Properties**.

b. Click the **Port Settings** tab, and then click **Advanced**.

c. Deselect the **Serial Enumerator** option, and click **OK**.

d. Click **OK** to return to the Device Manager.

e. Repeat this step for each of the four new COM ports. When you are finished, close the Device Manager.



COM Port Number: COM3

USB Transfer Sizes

Select lower settings to correct performance problems at low baud rates.

Select higher settings for faster performance.

Receive (Bytes): 4096

Transmit (Bytes): 4096

BM Options

Select lower settings to correct response problems.

Latency Timer (msec): 16

Timeouts

Minimum Read Timeout (msec): 0

Minimum Write Timeout (msec): 0

Miscellaneous Options

Serial Enumerator □

Serial Printer □

Cancel If Power Off □

Event On Surprise Removal □

Set RTS On Close □

Disable Modem Ctrl At Startup □

Commands

Commands are issued via a Windows Command prompt. The commonly used command options are documented below – see the Help for how to view a complete list of supported commands.

Help

For a complete list of all the ESP options, enter:

```
C:\...\ESP\ESP
```

Erase

To erase the entire 512 KB of flash, enter:

```
C:\...\ESP\ESP -E
```

To erase a select number of pages of flash, enter:

```
C:\...\ESP\ESP –e OFFSET PAGES
```

Where OFFSET is in hexadecimal with no leading 0x and must be in multiples of 800 hexadecimal (2 KB). For example, to erase the 3rd and 4th pages enter:

```
C:\...\ESP\ESP –e 1800 2
```

Read (unlocked device)

To read the entire 512 KB of flash and store the image in a file, enter:

```
C:\...\ESP\ESP –R FILENAME
```

To read the entire a subset of flash and store the image in a file, enter:

```
C:\...\ESP\ESP –R FILENAME OFFSET BYTES
```

Where OFFSET and BYTES are in hexadecimal with no leading 0x and bytes.

Read (locked device)

Via the Hardware Lock Key, see *040-0109 Eterna Board Specific Parameter Configuration Guide* for details, a device can be locked to prevent access to all internal memory including the flash. To read a locked device enter:

```
C:\...\ESP\ESP –R FILENAME OFFSET –u KKKKKKKK
```

Where KKKKKKK is the Hardware Lock Key. This will store the entire 512 KB in FILENAME. This will not modify the locked state of the device.

Where OFFSET is in hexadecimal with no leading 0x and must be in multiples of 800 hexadecimal (2 KB). The device will only program the number of bytes from the starting OFFSET to OFFSET + size(FILENAME).

Program with Verify

To program an image enter:

```
C:\...\ESP\ESP -P FILENAME OFFSET
```

Where OFFSET is in hexadecimal with no leading 0x and must be in multiples of 800 hexadecimal (2 KB). The device will only program the number of bytes from the starting OFFSET to OFFSET + size(FILENAME). If the verification is successful ESP will report on a new line:

```
Verify: PASS
```

If the verification is unsuccessful ESP will report on a new line:

```
Verify: FAIL
```

Followed by a line indicating which address failed, the expected value and the value read from the failing location.

Verify

To verify an image enter:

```
C:\...\ESP\ESP -V FILENAME OFFSET
```

Where OFFSET is in hexadecimal with no leading 0x and must be in multiples of 800 hexadecimal (2 KB). The device will only verify the number of bytes from the starting OFFSET to OFFSET + size(FILENAME). If verification is unsuccessful ESP will report the first difference. If the verification is successful ESP will report:

```
Verify: PASS
```

If the verification is unsuccessful ESP will report on a new line:

```
Verify: FAIL
```

Followed by a line indicating which address failed, the expected value and the value read from the failing location.

Unlock (persistent)

Via the Hardware Lock Key, see *040-0109 Eterna Board Specific Parameter Configuration Guide* for details, a device can be locked to prevent access to all internal memory including the flash. **This command will alter part of the first page in flash, blanking the lock key in the process.** To unlock a locked device enter:

```
C:\...\ESP\ESP -u KKKKKKKK PORT
```

Where KKKKKKK is the Hardware Lock Key and PORT is the PC's third USB Serial Port assigned to the programmer.

Usage

Flash Image Construction

An Eterna's flash image is constructed with multiple individual binary files divided as shown in Figure 3.

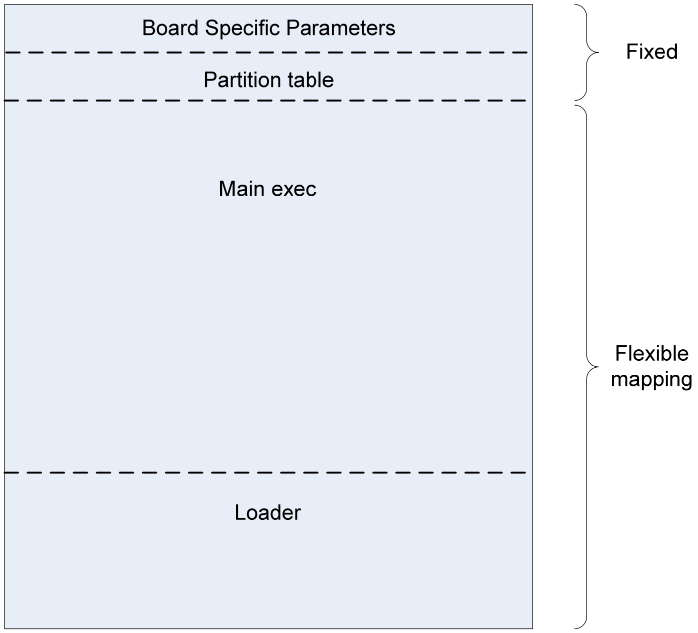


Figure 3 Eterna Flash Image

Users creating an image for the first time will need to load four individual images:

Image Name	Start Address (Hex)	Description
Board Specific Parameters	0	2 KB image containing hardware and software configuration settings. This file is required for proper operation and is created via the fuseTable.exe application described in Eterna Board Specific Parameter Configuration Guide.
Partition Table	800	Defines the location of the elements in the Flexible mapping portion of Eterna's image, including the Main Executable and Loader. The partition table is currently agnostic to the particular product software variants.
Main Executable	1000	The main executable image. Each variant of the Eterna product family will have a corresponding software image.

Loader	77800	The loader manages handling of completed Over The Air Programming, OTAP, images and starting the Main Executable image. The loader is currently agnostic to the particular product software variants.

For LTC5800 devices users will need to create the board specific parameters image - see the Eterna Board Specific Parameter Configuration Guide for details. Access to the Partition Table, Main Executable and Loader images should be obtained through your FAE.

Once a flash image has been created it can be moved from one device to a second device (of the same design and layout) by reading the entire 512 kB image of the first device and then loading the read image into the second device

To program all four of the images onto an **erased** device via ESP enter:

```
C:\...\ESP\ESP -P FuseTable.bin 0
C:\...\ESP\ESP -P PartitionTable.bin 800
C:\...\ESP\ESP -P Main.bin 1000
C:\...\ESP\ESP -P Loader.bin 77800
```

Target Crystal Characterization

Most modern crystal oscillators require two capacitors, often called load capacitors, to oscillate at the desired frequency. The LTC5800 family of products includes on-chip load capacitors for both the 32kHz and the 20MHz crystal oscillators. The load capacitance for the 32kHz oscillator is fixed at a standard value of 12.5pF while the load capacitance for the 20MHz crystal is adjustable via the “20 MHz load trim (ox13)” board support parameter as described in the Board Specific Configuration Guide. The adjustable load capacitors are used to center the resonating frequency of the 20MHz oscillator. Because the 20MHz oscillator is used as the radio frequency reference, the load capacitance must be trimmed to account for variations in printed-circuit board layout and dielectric stack-up. The DC9010 is used for characterizing the 20MHz frequency distribution as described below. The characterization procedure is performed on a sample of PCBs during product development to allow correct generation of the “20 MHz load trim (ox13)”; it is not necessary to trim every part in production.

The DC9010 includes a calibrated timing reference signal that may be used to characterize the target board layout. The DC9010 is calibrated at the time of manufacture and should be calibrated annually to maintain accuracy. See the Crystal Timing Reference & Calibration Procedure section of this document for how to calibrate the DC9010 reference. The CLI command mxtal is used to characterize an LTC5800 based design, comparing the DC9010 reference against Eterna’s crystal oscillator. The resulting characterized values should be used when creating the specific Board Specific Parameter binary image for each LTC5800 based design.

Characterization is performed by issuing the `mxtal` command over the target’s **CLI port**, not via the ESP software. Use a terminal program, such as Tera Term, set to 9600 baud, 8-bit, no parity, 1 stop bit and no flow control, on the serial port indentified in step 7) of the ESP setup. During the characterization of devices the actual value of the “20 MHz load trim (ox13)” board support parameter does not matter. After loading the product code image and a valid fuse table , enter the following command on the terminal:

```
> mxtal trim
```

After several seconds, Eterna will respond with approximately the following:

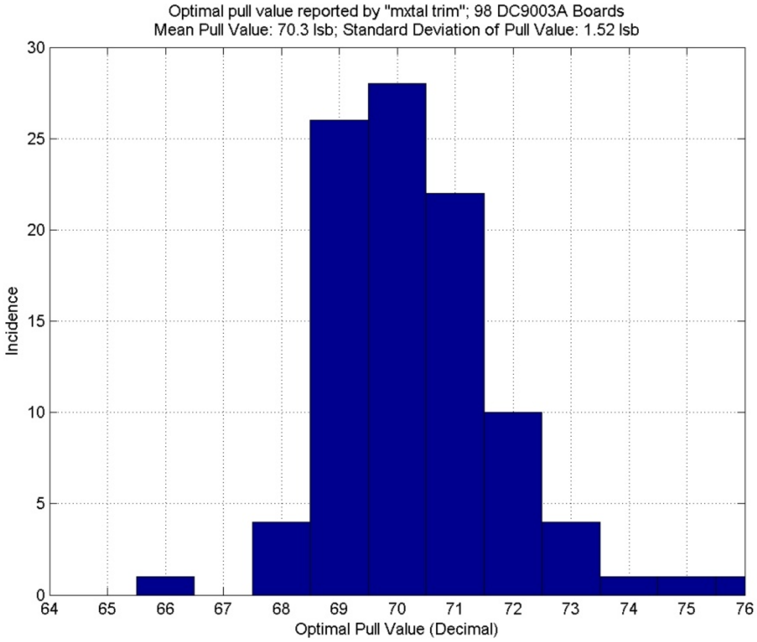
```
Optimal pullVal for this board=72 yields PPM err=15/16
```

The above output indicates

i) that this particular unit performs optimally with a “20 MHz load trim (ox13)” (e.g. pullVal) equal to 72 decimal and

ii) were this value to be used in the fuse table the center frequency would be trimmed to within 15 / 16 's of a ppm (e.g. 0.9375 ppm) of desired.

Crystal characterization should be performed over a statistically meaningful number of targets to account for unit-to-unit variation in crystals and load. As an example of the complete characterization process, we will now find the correct “20 MHz load trim (ox13)” for the DC9003A hardware. We start with a sample size of ninety-eight DC9003A units and run mxtal trim on the motes. The values of the pullVal are tabulated and the results are plotted in the histogram below:



The above histogram shows the pull value that centers the 20MHz frequency for 98 DC9003A boards. The histogram includes the effects of variability due to crystal frequency tolerance, due to LTC5800 load-capacitance variation, and due to variation in PCB-trace capacitance. This distribution is indicative of the variation one should expect when the LTC5800 layout guidelines are followed and may be used to select a starting sample size for characterization. However, the variability in the above plot is a function of board manufacturing tolerances and layout so the number of characterization units required may be different than the above data suggest for other designs. In general, the number of units that should be characterized to attain 0.5 lsb accuracy may be estimated to be at least:

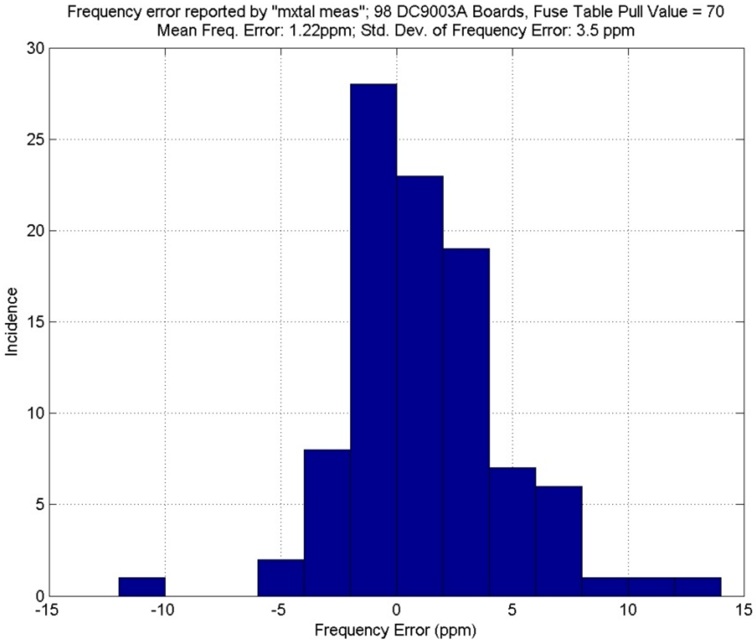
$$N = (\sigma / 0.5 \text{ lsb})^2$$

Where σ is the sample standard deviation of the pull values in lsb, and N is the total number of units needing to be characterized. From the histogram the standard deviation of frequency offset is 1.52 lsb which suggests, for this product, an absolute minimum of about 10 units need to be characterized and averaged to yield a pull value within 0.5 lsb of desired. Since the above equation is an approximation, it is a good idea to double the number of parts measured to offset errors in the approximation. So in this case, based upon the data from DC9003A implementation a conservative approach would be to use 20 parts to determine the "20 MHz load trim (ox13)".

We also note, from the above histogram, that the mean of the optimal pull value is 70.3 which is rounded to 70 because the fuse table field "20 MHz load trim (ox13)" is an integer. Now, to verify proper functionality, we generate a fuse table with "20 MHz load trim (ox13)" set to 70, and retest the units with the command:

```
> mxtal meas
pullVal used for measurement=70, PPM err=93/16
>
```

Where the "pullVal" indicates the correct "20 MHz load trim (ox13)" has been used and the PPM err of 93/16 shows the frequency error = 5.1825 PPM. Retesting the units with the correct fuse table ensures that the fuse table was generated correctly and shows the spread of the frequency errors using the value of the "20 MHz load trim (ox13)" to be loaded onto production boards.



The histogram above shows the results of the mxtal meas-reported 20MHz frequency error at room temperature for 98 DC9003A motes with 20 MHz load trim equal to 70. The histogram represents the trimmed unit-to-unit frequency variation. This distribution is indicative of the frequency variation one should expect of finished products in production. Note that the mean is not exactly zero which is principally because the pull value was rounded from 70.3 to 70. This distribution is well centered, has a single peak and bell-curve shaped. Thus a 20 MHz load trim equal to 70 is correct for this board.

Note: The crystal timing reference signal generator requires annual calibration from a GPS 1 Hz (PPS) clock source using the two SMA crystal timing reference maintenance interfaces and the on-board trim DIP switches. See Crystal Timing Reference & Calibration Procedure the section for details.

Note: This command may only be used when the mote's radio is not active, i.e. in the *slave* mode and prior to joining the network. After using this command, reboot the mote to continue normal operation.

Manufacturing Support

Multiple DC9010s can be enabled to run in parallel on a single PC. To accomplish this, ESP software must be provided with the specific location ID and serial port via the **–i** option. The serial port can be indentified via the PC's "Device Manager" as described in the Software Installation section of this document.

Location ID

To determine the Location ID for a specific DC9010 enter the following after connecting each DC9010:

```
C:\...\ESP\ESP –L
```

A list similar to the following will be presented:

```
locID[0] = 0x2121, devString = Eterna Serial Programmer A
locID[1] = 0x2122, devString = Eterna Serial Programmer B
```

Use the B port's location ID with the –i option with any of the commands to direct the command to a specific ESP. For example to program with verify to the ESP device identified above one, enter:

```
C:\...\ESP\ESP –i 2122 –P FILENAME OFFSET
```

Creating an image for manufacture

To create a single image for manufacturing:

1) Erase the contents of Eterna's flash
2) Load all components of the flash's image as described in the Usage section of this document
3) Configure any parameters via Eterna's API to the values needed for manufacture
4) Read Eterna's flash content to a 512 KB file

The binary image created from reading the flash content now represents a single image that can be loaded using the program with verify command with an offset of zero.

For network security purposes it is strongly recommended that the "Hardware Lock Key" Board Specific Parameter be enabled and set. It is essential that this value be tracked as once the "Hardware Lock Key" is enabled the only mechanism to enable in circuit reading and programming of flash is via unlocking of the device which requires the value of the "Hardware Lock Key".

It is also recommended that manufactures obtain a unique Manufacturer's ID with Linear Technology and assign the Manufacturer's ID along with a Board ID and Board Revision to each LTC5800 based design.

Eterna Flash Emulator

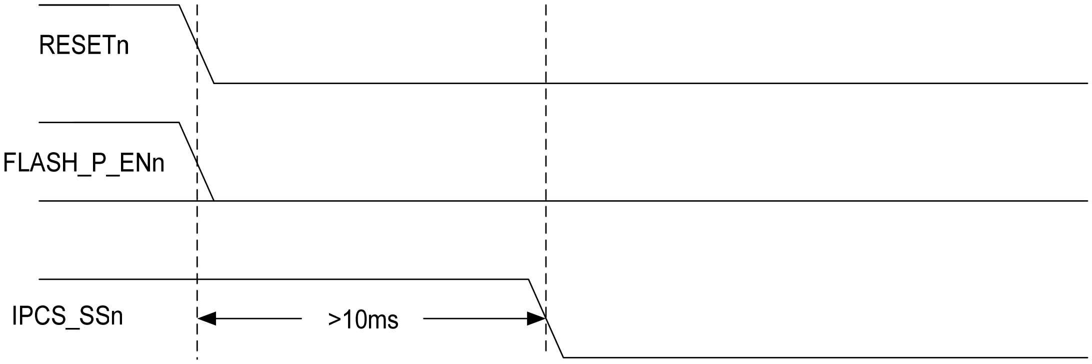
The Eterna Serial Programmer Software uses the Eterna Flash Emulator, part of the Eterna bootloader code, which supports a command protocol over IPCS that allows manipulation of the main pages on the Eterna Flash. The following describes the details of the Eterna Flash Emulator protocol.

A typical sequence in pseudo code for a simple example follows:

```
EnterFlashEmulator();      // assert FLASH_P_ENn,
// RESETn high 1ms, RESETn low,
// 10ms wait
BulkErase();   // SPI transaction to send Bulk Erase
command
WaitForRdy();  // SPI reads to poll STATUS until ready
ProgramFlash(  // SPI writes, in 16KB chunks max
0x0,           // start of flash
fullImage,     // pointer to buffer with desired image
 sizeof(fullImage) );
WaitForRdy();
ReadFlash(     // SPI reads
0x0,
   buf,
   sizeof(fullImage));
Verify(        // Verify image
buf,
fullImage,
sizeof(fullImage));
```

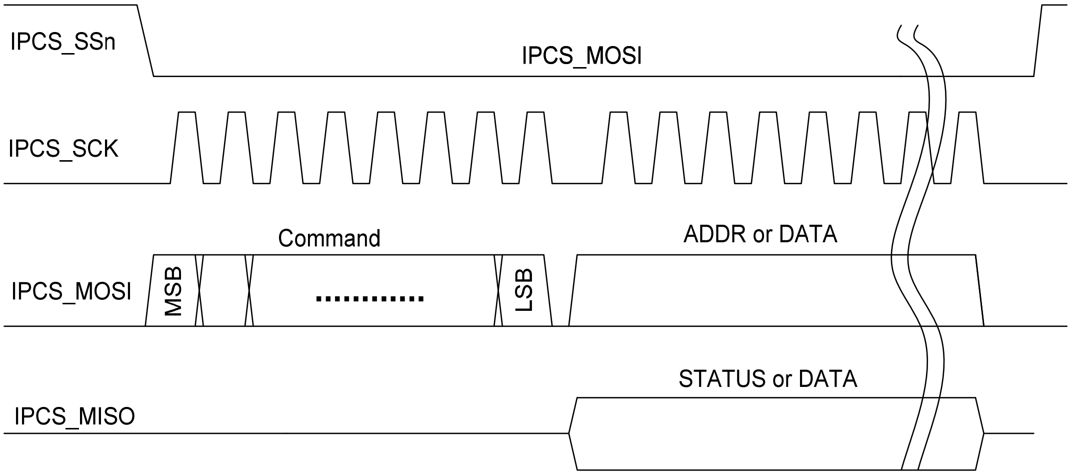
IPCS (SPI Slave)

The Eterna Flash emulator uses the IPCS bus in conjuction with the RESETn and FLASH_P_ENn signals. To enter the flash emulator, assert both RESETn and FLASH_P_ENn (both low), and then after 10ms, the host communicatew with the emulator via the bus, at a maximum rate of 14.7 MHz



Operation is controlled by a protocol mastered externally. Commands starts with the falling edge of IPCS_SSn followed by an appropriate 8-bit instruction, listed below, followed by appropriate address and/or data. While IPCS_SSn is low, data from IPCS_MOSI is clocked from the master on the rising edge of IPCS_SCK, MSB first.

As appropriate, status and read data from the device is clocked out on IPCS_MISO on the falling edge of IPCS_SCK, for sampling by the master on the rising edge.



Command Summary

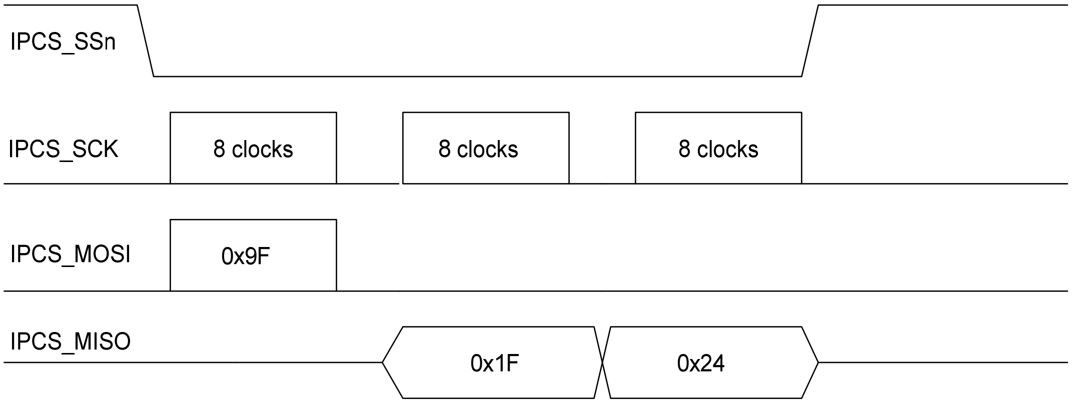
The emulator supports the following commands:

- 0x9F Read ID
- 0xD7 Read Status
- 0x03 Continuous Read (Low Frequency)
- 0x50 Page Erase
- 0xC7 Bulk Erase
- 0x44 Buffer Write and Program

Command values other than those defined above can lead to undefined behavior.

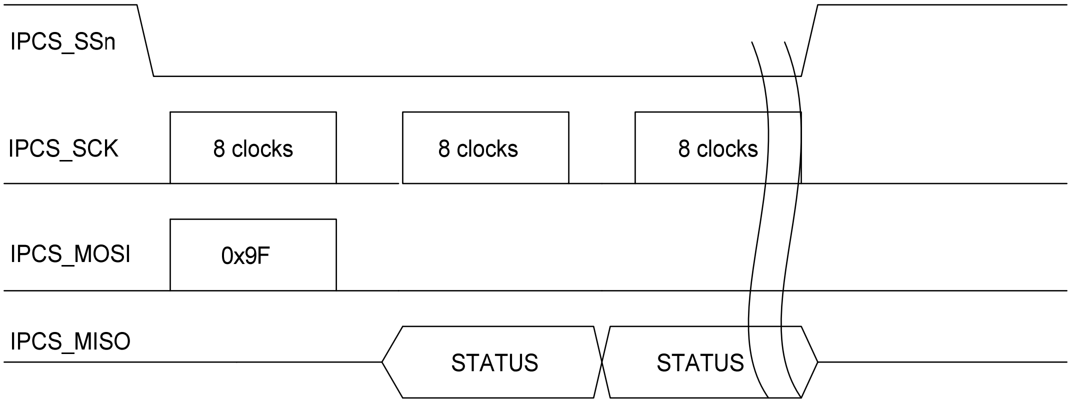
Read ID

The Read ID command will cause the device to clock out the two byte value 0x1F24.



Read Status

The Read Status command will continually output a status byte.



The status byte has the following format:

STATUS Byte

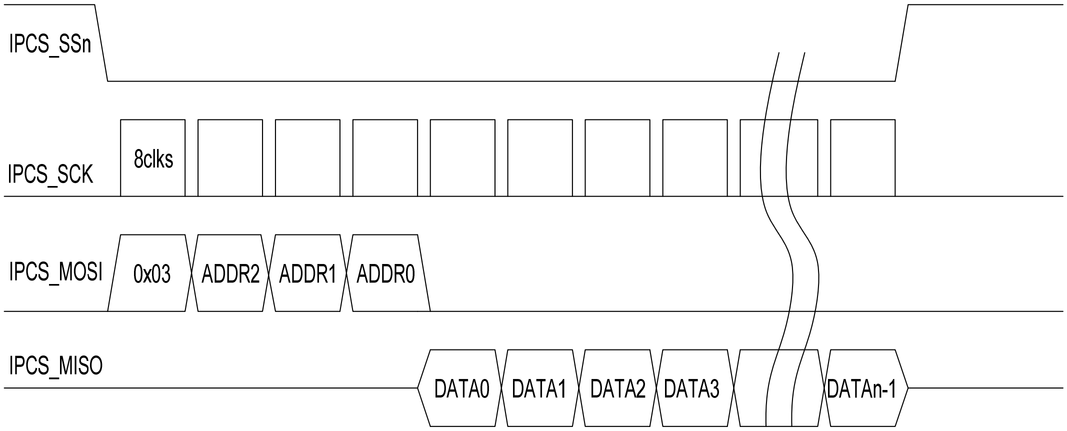
MSB

RDY	**0**	**0**	**1**	**1**	**1**	**X**	**X**

The RDY bit is true (high) if the device is ready for the next operation, and the RDY bit is false (low) if the device has not completed the previous command, such as an erase. The 2 LSBs are reserved for future use, and their values are undefined.

Continuous Read

The Continuous Read command takes an additional 3 bytes of address after the command, and is followed by data from the relative address (more on address below).



The 3 bytes of address is a byte address sent MSBs first. 0 represents the 1st byte address in Eterna Flash. The range of valid addresses is **0x000000** to **0x07FFFF**.

Address

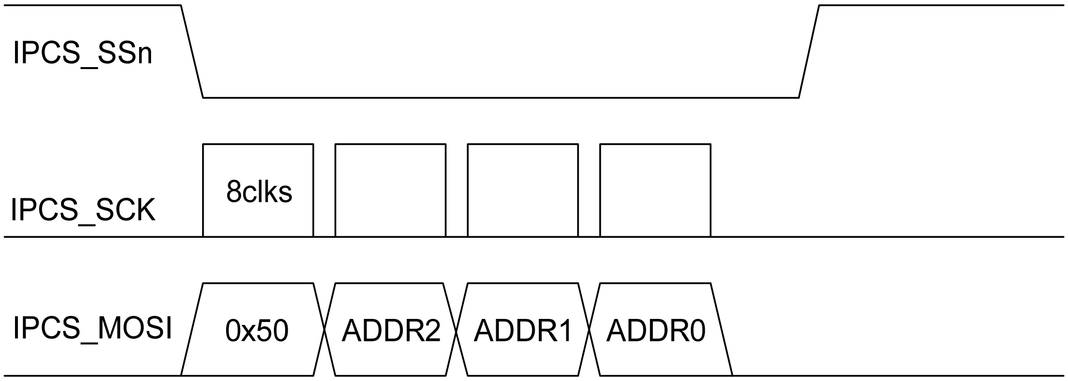
MSB

ADDR2	ADDR1	ADDR0

The data is returned starting from the byte address provided, incrementing byte address for each additional byte read before the cycle is terminated.

Page Erase

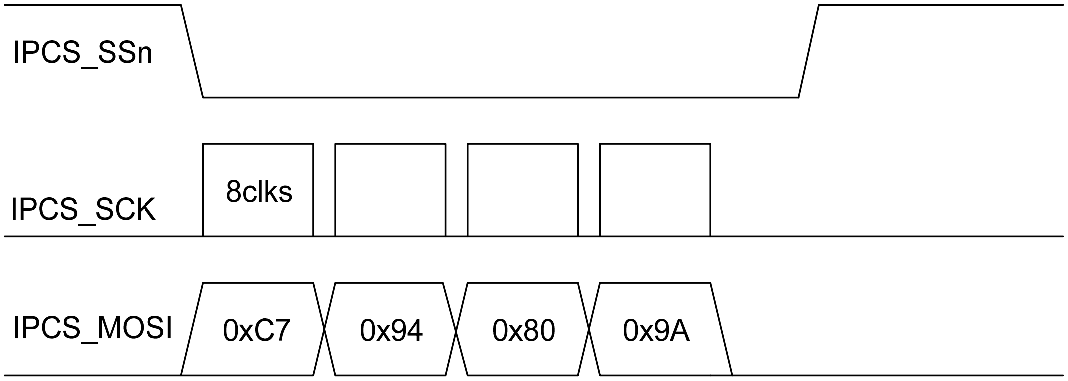
The Page Erase command erases the 2048 byte page pointed to by the 3 byte address (the lower 11 bits are ignored).



After issuing the Page Erase command, the host must insure that the erase operation is complete before proceeding by polling the Read Status Command, or waiting at least 40 ms.

Bulk Erase

The Bulk Erase command erases all 512 kBytes of Eterna flash. The Bulk Erase command must be followed by a 3 byte key: 0x94809A.



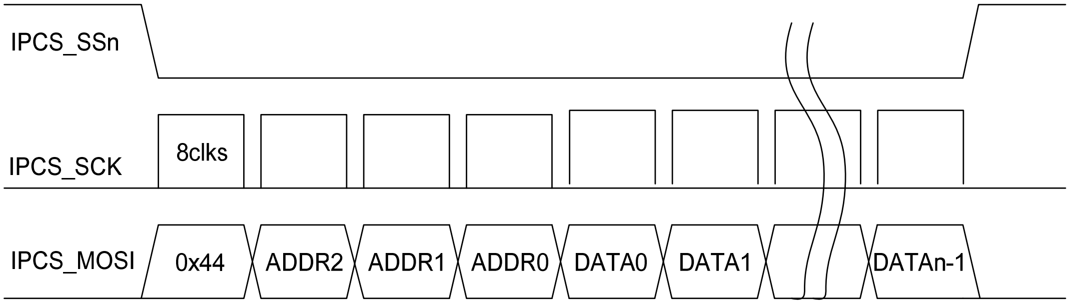
After issuing the Bulk Erase command, the host must insure that the erase operation is complete before proceeding by polling the Read Status Command, or waiting at least 40 ms.

Buffer Write

Buffer Program

Buffer Write and Program

The Buffer Write and Program command programs the passed data to the address provided. Writes must be integral 32-bits of data, and address must be 32-bit aligned. Maximum write length is 16KB.

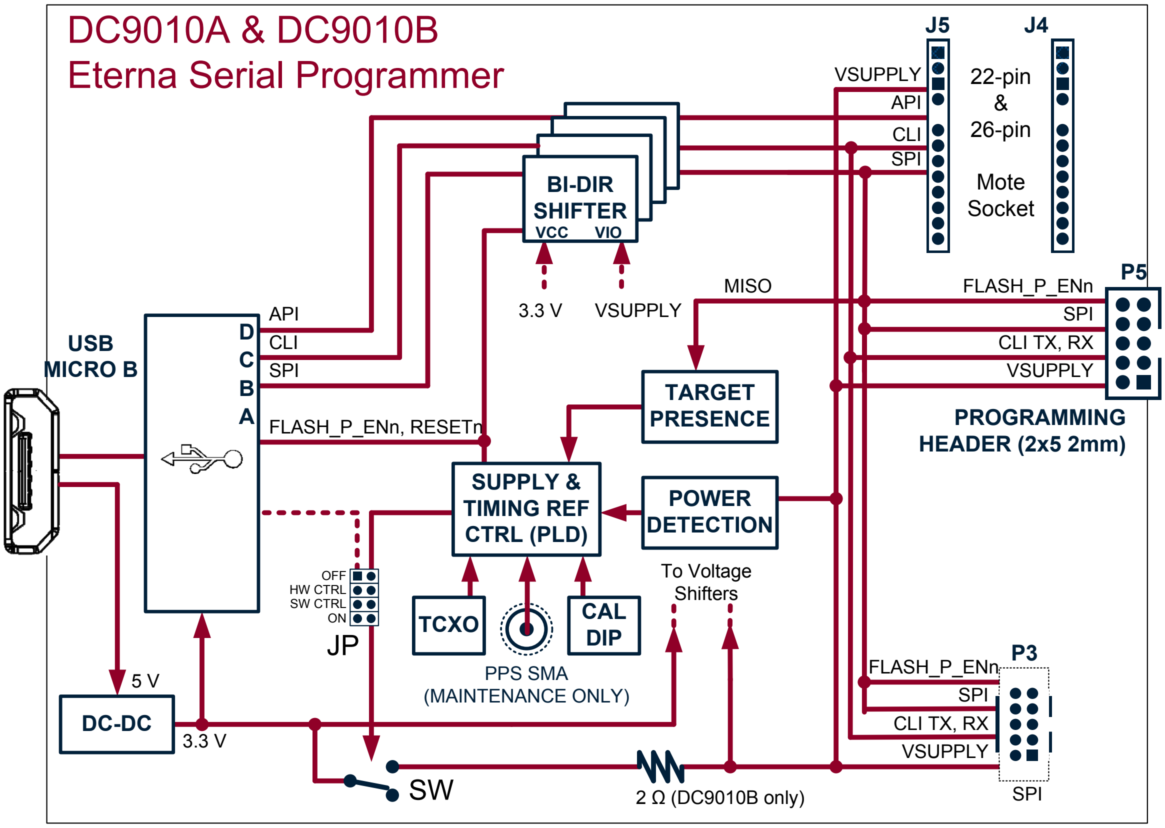


After issuing the Buffer Write and Program command, the host must insure that the erase operation is complete before proceeding by polling the Read Status Command, or waiting at least 40 us times the number of words written.

Hardware Reference

Functional Block Diagram

The following diagram depicts the internal circuitry of the DC9010.



Features

Programming

The DC9010 allows programming of Eterna with the following interfaces:

- a 2x5 2mm header (externally accessible),
- a 0.050” programming header (internal),
- a 22/26-pin through-hole mote socket (internal).

Supply Voltage

The DC9010 accommodates either self-powered or unpowered targets. The full voltage range of self-powered devices is supported (2.1V to 3.76V). Unpowered targets are provided a supply voltage of approximately 3V.

At the start of programming (upon assertion of FLASH_P_ENn) or when Eterna's serial interface is accessed (UARTC0_RX), the DC9010 senses the target voltage and provide power to the target if no voltage is detected.

The automatic power selection mechanism may be overridden with a 2-mm board jumper if required (P1). The P1 jumper is only accessible when the enclosure cover is removed. P1 jumper settings are as follows.

P1 Jumper	Power Setting Description
None	Automatic target power selection
"ON"	Unpowered target (DC9010 provides VSUPPLY)
"OFF"	Self-powered target

Serial Interfaces

The DC9010 PC interface consists of USB Serial Ports mapped to the Eterna's SPI, CLI and API interfaces.

ESP will operate over SPI for flash access and one of the CLI or API ports for device locking and unlocking.

Additionally any PC terminal application may open the available DC9010 USB Serial Ports, thus independently accessing Eterna's serial interfaces.

Visual Indicator

The DC9010 top LED flickers GREEN during programming and blinks GREEN at 4Hz rate when the crystal timing reference is provided (default).

Hardware Versions

DC9010A

The DC9010A is the initial version of the programmer. It includes all features listed above.

The DC9010A has been discontinued.

DC9010B

The DC9010B is an incremental enhancement to the DC9010A: it includes a simple limiter to the target current (2 ohm series resistance, see functional block diagram).

The DC9010B may be used with unpowered high capacitance targets such as energy harvesting boards with large storage capacitors.

Board Outline and Connector Pinout

Serial Programming Header (P5, right angle external 2mm)

Pin #	Signal	Direction
1	IPCS_SSn	O
3	IPCS _SCK	O
5	IPCS _MISO	I
7	VSUPPLY	-
9	UARTC0_TX	I

Pin #	Signal	Direction
2	FLASH_P_ENn	O
4	IPCS _MOSI	O
6	RESETn	O
8	GND	-
10	UARTC0_RX	O

22/26-Pin Mote Socket (J4 & J5, internal 2mm)

Pin #	J5 Signals	Direction
1	UARTC0_RX	O
2	UARTC0_TX	I
3	GND	-
4	VSUPPLY	-
5	KEY	-
6	UART_RX	O
7	UART_TX	I
8	UART_RX_RTSn	I
9	UART_TX_RTSn	O
10	UART_RX_CTSn	O
11	UART_TX_CTSn	I
12	TIMEn	I/O
13	MODE	I/O

Pin #	J4 Signals	Direction
1	LPTIMERn	I/O
2	SLEEPn	I/O
3	RESETn	O
4	IPCS_SSn	O
5	KEY	-
6	IPCS _MISO	I
7	IPCS _MOSI	O
8	IPCS _SCK	O
9	TCK	O
10	TDO	I
11	TDI	O
12	TMS	O
13	FLASH_P_ENn	O

Small Programming Header (P3, internal .050”)

Pin #	Signal	Direction
1	IPCS_SSn	O
3	IPCS _SCK	O
5	IPCS _MISO	I
7	VSUPPLY	-
9	UARTC0_TX	I

Pin #	Signal	Direction
2	FLASH_P_ENn	O
4	IPCS _MOSI	O
6	RESETn	O
8	GND	-
10	UARTC0_RX	O

Reference Calibration Connectors (J2, J3, SMA)

Pin #	J2, PPS Input	Direction
Signal	REF_IN	I
Shield	GND	-

Pin #	J3, Calibration Output	Direction
Signal	TEST_OUT	O
Shield	GND	-

Crystal Timing Reference & Calibration Procedure

Crystal Timing Reference, 4PPS

The DC9010 features a crystal timing reference signal also referred to as "4PPS". The 4PPS signal used for device calibration using the standard programming interface header.

The 4PPS signal consists of four pulses per second with precise ¼-second edge placement; each pulse is typically one eighth of a second.

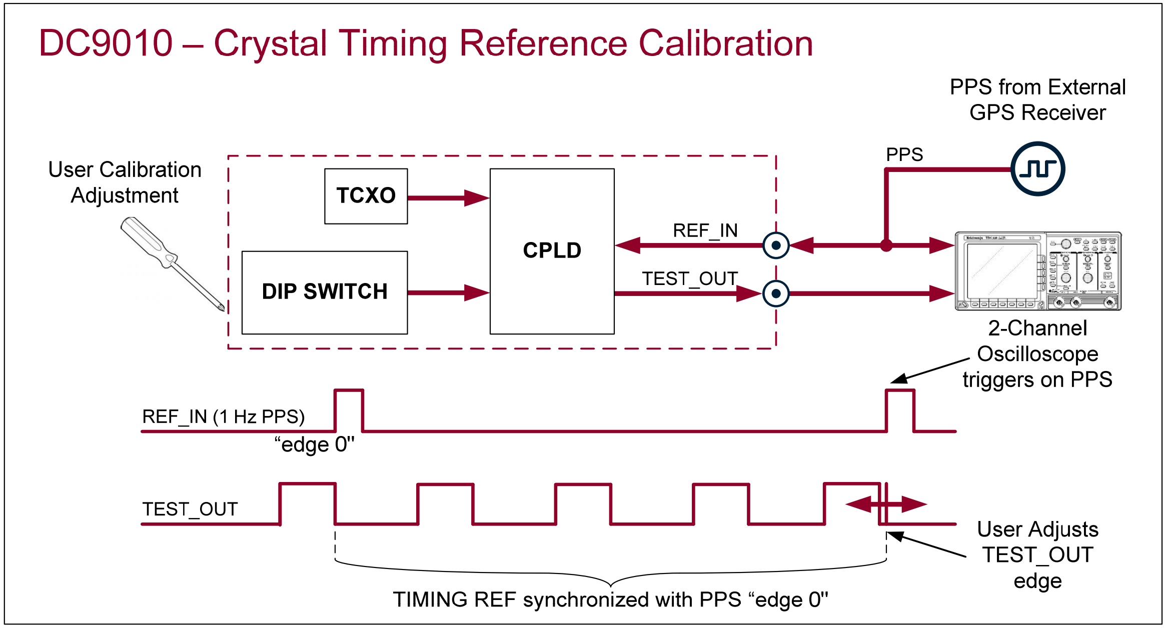
The DC9010's CPLD derives the a crystal timing reference signal from its on-board temperature compensated crystal oscillator 2.5ppm TCXO. The DC9010's CPLD implements a multi-bit counter, allowing for less than 0.5ppm resolution adjustment of the crystal timing reference signal.

The REF_IN signal shall be disconnected when the 4PPS is used to calibrate an Eterna product.

4PPS Calibration

An on-board 8-bits switch is available for of calibration and controls the offset of the multi-bit counter. With 0x80 (switches closed or ON = 0) creating a 0ppm offset from the on-board TCXO.

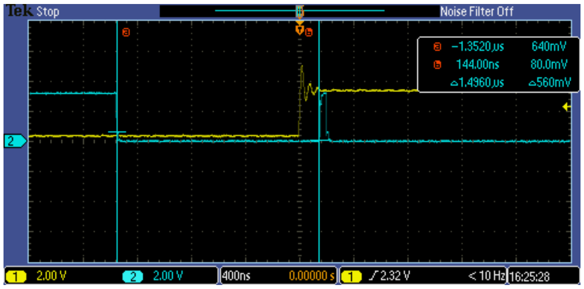
TCXO offsets are calibrated using a 1 PPS signal from a GPS source, connected to J2 (REF_IN), J3 (TEST_OUT) is a copy of the 4PPS signal. During the calibration of the DC9010 the 1PPS reference resets the 4PPS signal output.

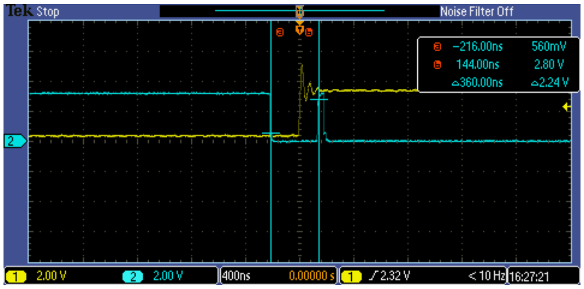

DC9010 – Crystal Timing Reference Calibration
PPS from External GPS Receiver
PPS
User Calibration Adjustment
TCXO
CPLD
DIP SWITCH
REF_IN
TEST_OUT
2-Channel Oscilloscope triggers on PPS
REF_IN (1 Hz PPS)
"edge 0"
TEST_OUT
User Adjusts TEST_OUT edge
TIMING REF synchronized with PPS "edge 0"

The purpose of the calibration is to set the offset 8-bit switch such that the 4PPS falling edge aligns with the PPS reference rising edge. With the calibration set correctly, and the scope zoomed into ~1us range (1us is 1ppm of 1s), the 4PPS falling edge can be observed slowly moving on the left of the reference rising edge, resetting periodically, and moving in that same direction again. One LSB change in the offset switch value will result in 400 nsec change in the 4PPS edge placement.

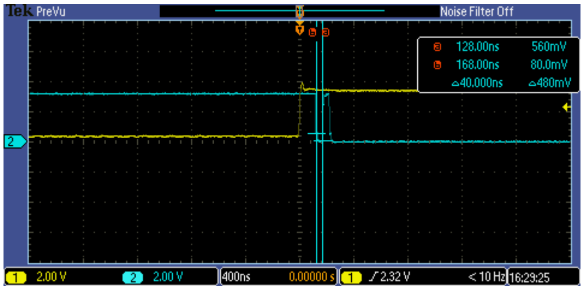
To calibrate:

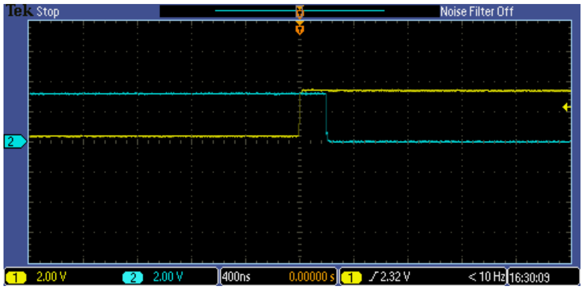
1. Pry open the DC9010 enclosure using the bottom slots and remove the top cover. Connect the DC9010 to a PC and allow for the temperature to stabilized to the environment for 30 min
2. Connect the DC9010 REF_IN SMA input to the channel 1 of the oscilloscope (set the scope input impedance to DC and high-Z, not 50 ohm) and then to a GPS 1PPS reference
3. Connect the DC9010 TEST_OUT SMA output to the channel 2 of the oscilloscope with a 50 ohm coax of the same length as the REF_IN connection to the oscilloscope
4. Start with a lower than nominal setting such as 0x70 (ON position is 0, OFF position is 1, pin 1 is LSB). Zoom in on PPS rising edge trigger (~1us/div) and observe the falling edge of the 4PPS signal. The falling edge of a valid 4PPS pulse should be on the left of the rising edge of the reference. A valid 4PPS pulse is a large pulse, rather than the reset narrow pulse (which is an artifact of the calibration).
5. Increment the setting value. The scope captures below show the 4PPS falling edge getting closer as the value is incremented. An LSB change corresponds to 100ns 4PPS period, or 0.4ppm. As the 4th pulse is used for alignment, 1 LSB results in 400ns shift over 1 second.





6. Calibration is complete once the falling edge of a large 4PPS pulse passes the REF_IN trigger edge and start merging into the reset pulse.





7. Disconnect the REF_IN signal from the DC9010 and verify that the 4PPS drift against the PPS reference is minimal.

Specifications

Specifications are at 25°C and 5V input supply voltage unless otherwise noted and may change without notice.

Electrical Parameters

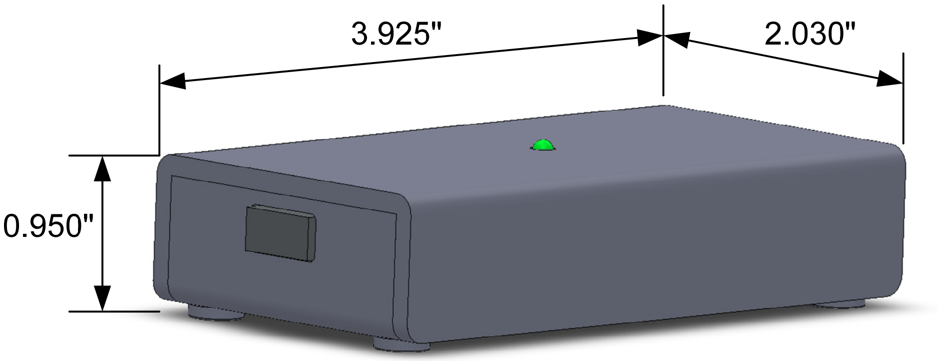
Parameter	Min	Typ	Max	Units	Comments
Input supply voltage	4.5	5	5.5	V	From USB
Input supply current (w/out target)		120		mA	
Eterna programming current		15		mA	
Target supply voltage	2.4	3		V	
Maximum target load current			200	mA	
Timing reference calibration resolution		0.4		ppm	
Timing reference stability Over operating temperature Aging		 +/- 2.5 +/- 1		 ppm ppm/year	

Environmental Parameters

Parameter	Min	Typ	Max	Units	Comments
Operating temperature	0		50	°C	
Storage temperature	-40		85	°C	
Humidity	10		90	% RH	Non-condensing
Altitude	0		3000	m	

Physical Parameters

Parameter	Min	Typ	Max	Units	Comments
Dimensions	24 x 100 x 52			mm^3	
Weight		80		g	



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