FemtoClock® Crystal-to-LVDS Frequency Synthesizer w/Integrated Fanout Buffer

ICS844246DI

DATA SHEET

General Description

The ICS844246DI is a Crystal-to-LVDS Clock Synthesizer/Fanout Buffer designed for Fibre Channel frequencies and Gigabit Ethernet applications. The output frequency can be set using the frequency select pins and a 25MHz crystal for Ethernet frequencies, or a 26.5625MHz crystal for a Fibre Channel. The low phase noise characteristics of the ICS844246DI make it an ideal clock for these demanding applications.

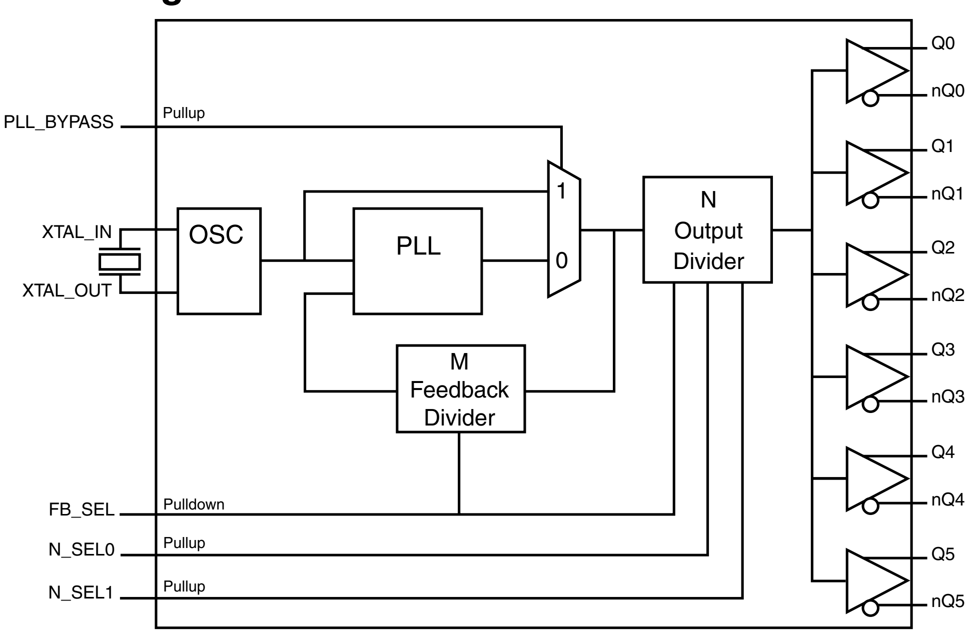
Features

- Six LVDS output pairs
- Crystal oscillator interface
- Output frequency range: 53.125MHz to 333.3333MHz
- Crystal input frequency range: 25MHz to 33.333MHz
- RMS phase jitter @ 125MHz, using a 25MHz crystal (1.875MHz - 20MHz): 0.416ps (typical)
- Full 3.3V or mixed 3.3V core, 2.5V output supply modes
- -40°C to 85°C ambient operating temperature
- Available in lead-free (RoHS 6) package

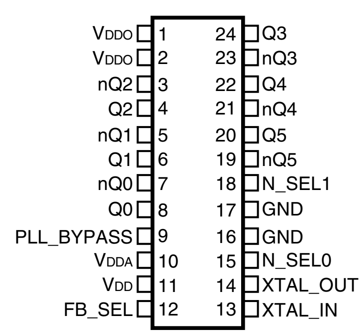
Select Function Table

Inputs			Function		
FB_SEL	**N_SEL1**	**N_SEL0**	**M Divide**	**N Divide**	**M/N**
0	0	0	20	2	10
0	0	1	20	4	5
0	1	0	20	5	4
0	1	1	20	8	2.5 (default)
1	0	0	24	3	8
1	0	1	24	4	6
1	1	0	24	6	4
1	1	1	24	12	2

Block Diagram



Pin Assignment



ICS844246DI
24-Lead TSSOP, E-Pad
4.4mm x 7.8mm x 0.925mm package body
G Package
Top View

Table 1. Pin Descriptions

Number	Name	Type		Description
1, 2	V_{DDO}	Power		Output supply pins.
3, 4	nQ2, Q2	Output		Differential output pair. LVDS interface levels.
5, 6	nQ1, Q1	Output		Differential output pair. LVDS interface levels.
7, 8	nQ0, Q0	Output		Differential output pair. LVDS interface levels.
9	PLL_BYPASS	Input	Pullup	Selects between the PLL and crystal inputs as the input to the dividers. When LOW, selects PLL. When HIGH, bypasses the PLL. LVCMOS / LVTTL interface levels.
10	V_{DDA}	Power		Analog supply pin.
11	V_{DD}	Power		Core supply pin.
12	FB_SEL	Input	Pulldown	Feedback frequency select pin. LVCMOS/LVTTL interface levels.
13 14	XTAL_IN, XTAL_OUT	Input		Crystal oscillator interface. XTAL_IN is the input. XTAL_OUT is the output.
15, 18	N_SEL0, N_SEL1	Input	Pullup	Output frequency select pin. LVCMOS/LVTTL interface levels.
16, 17	GND	Power		Power supply ground.
19, 20	nQ5, Q5	Output		Differential output pair. LVDS interface levels.
21, 22	nQ4, Q4	Output		Differential output pair. LVDS interface levels.
23, 24	nQ3, Q3	Output		Differential output pair. LVDS interface levels.

NOTE: *Pullup and Pulldown* refer to internal input resistors. See Table 2, *Pin Characteristics,* for typical values.

Table 2. Pin Characteristics

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
C_{IN}	Input Capacitance			4		pF
R_{PULLUP}	Input Pullup Resistor			51		kΩ
$R_{PULLDOWN}$	Input Pulldown Resistor			51		kΩ

Function Tables

Table 3. Crystal Function Table

Inputs				Function			Output Frequency (MHz)
XTAL (MHz)	FB_SEL	N_SEL1	N_SEL0	M	VCO (MHz)	N	
25	0	0	0	20	500	2	250
25	0	0	1	20	500	4	125
25	0	1	0	20	500	5	100
25	0	1	1	20	500	8	62.5
25	1	0	0	24	600	3	200
25	1	0	1	24	600	4	150
25	1	1	0	24	600	6	100
25	1	1	1	24	600	12	50
26.5625	0	1	0	20	531.25	5	106.25
26.5625	1	0	0	24	637.5	3	212.5
26.5625	1	0	1	24	637.5	4	159.375
26.5625	1	1	0	24	637.5	6	106.25
26.5625	1	1	1	24	637.5	12	53.125
30	0	0	0	20	600	2	300
30	0	0	1	20	600	4	150
30	0	1	0	20	600	5	120
30	0	1	1	20	600	8	75
31.25	0	0	0	20	625	2	312.5
31.25	0	0	1	20	625	4	156.25
31.25	0	1	0	20	625	5	125
31.25	0	1	1	20	625	8	78.125
33.3333	0	0	0	20	666.6667	2	333.3333
33.3333	0	0	1	20	666.6667	4	166.6667
33.3333	0	1	0	20	666.6667	5	133.3333
33.3333	0	1	1	20	666.6667	8	83.3333

Absolute Maximum Ratings

NOTE: Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics or AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Item	Rating
Supply Voltage, V_{DD}	4.6V
Inputs, V_I XTAL_IN Other Inputs	 0V to V_{DD} -0.5V to V_{DD} + 0.5V
Outputs, I_O (LVDS) Continuos Current Surge Current	 10mA 15mA
Package Thermal Impedance, θ_{JA}	32.1°C/W (0 mps)
Storage Temperature, T_{STG}	-65°C to 150°C

DC Electrical Characteristics

Table 4A. LVDS Power Supply DC Characteristics, $V_{DD} = V_{DDO} = 3.3V \pm 5\%$, $T_A = -40°C$ to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{DD}	Core Supply Voltage		3.135	3.3	3.465	V
V_{DDA}	Analog Supply Voltage		V_{DD} – 0.10	3.3	V_{DD}	V
V_{DDO}	Output Supply Voltage		3.135	3.3	3.465	V
I_{DD}	Power Supply Current				170	mA
I_{DDA}	Analog Supply Current				10	mA
I_{DDO}	Output Supply Current				100	mA

Table 4B. LVDS Power Supply DC Characteristics, $V_{DD} = 3.3V \pm 5\%$, $V_{DDO} = 2.5V \pm 5\%$, $T_A = -40°C$ to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{DD}	Core Supply Voltage		3.135	3.3	3.465	V
V_{DDA}	Analog Supply Voltage		V_{DD} – 0.10	3.3	V_{DD}	V
V_{DDO}	Output Supply Voltage		2.375	2.5	2.625	V
I_{DD}	Power Supply Current				165	mA
I_{DDA}	Analog Supply Current				10	mA
I_{DDO}	Output Supply Current				98	mA

Table 4C. LVCMOS/LVTTL DC Characteristics, V_{DD} = 3.3V ± 5% V_{DDO} = 3.3V ± 5% or 2.5V ± 5%, T_A = -40°C to 85°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
V_{IH}	Input High Voltage		V_{DD} = 3.465V	2		V_{DD} + 0.3	V
V_{IL}	Input Low Voltage		V_{DD} = 3.465V	-0.3		0.8	V
I_{IH}	Input High Current	N_SEL[1:0], PLL_BYPASS	V_{DD} = V_{IN} = 3.465V or 2.625V			5	µA
		FB_SEL	V_{DD} = V_{IN} = 3.465V or 2.625V			150	µA
I_{IL}	Input Low Current	N_SEL[1:0], PLL_BYPASS	V_{DD} = 3.465V or 2.625V, V_{IN} = 0V	-150			µA
		FB_SEL	V_{DD} = 3.465V or 2.625V, V_{IN} = 0V	-5			µA

Table 4D. LVDS DC Characteristics, V_{DD} = 3.3V ± 5%, V_{DDO} = 3.3V ± 5% or 2.5V ± 5%, T_A = -40°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{OD}	Differential Output Voltage		247		454	mV
ΔV_{OD}	V_{OD} Magnitude Change				100	mV
V_{OS}	Offset Voltage		1.10		1.50	V
ΔV_{OS}	V_{OS} Magnitude Change				120	mV

Table 5. Crystal Characteristics

Parameter	Test Conditions	Minimum	Typical	Maximum	Units
Mode of Oscillation			Fundamental		
Frequency		25		33.333	MHz
Equivalent Series Resistance (ESR)				50	Ω
Shunt Capacitance				7	pF

NOTE: Characterized using an 18pF parallel resonant crystal.

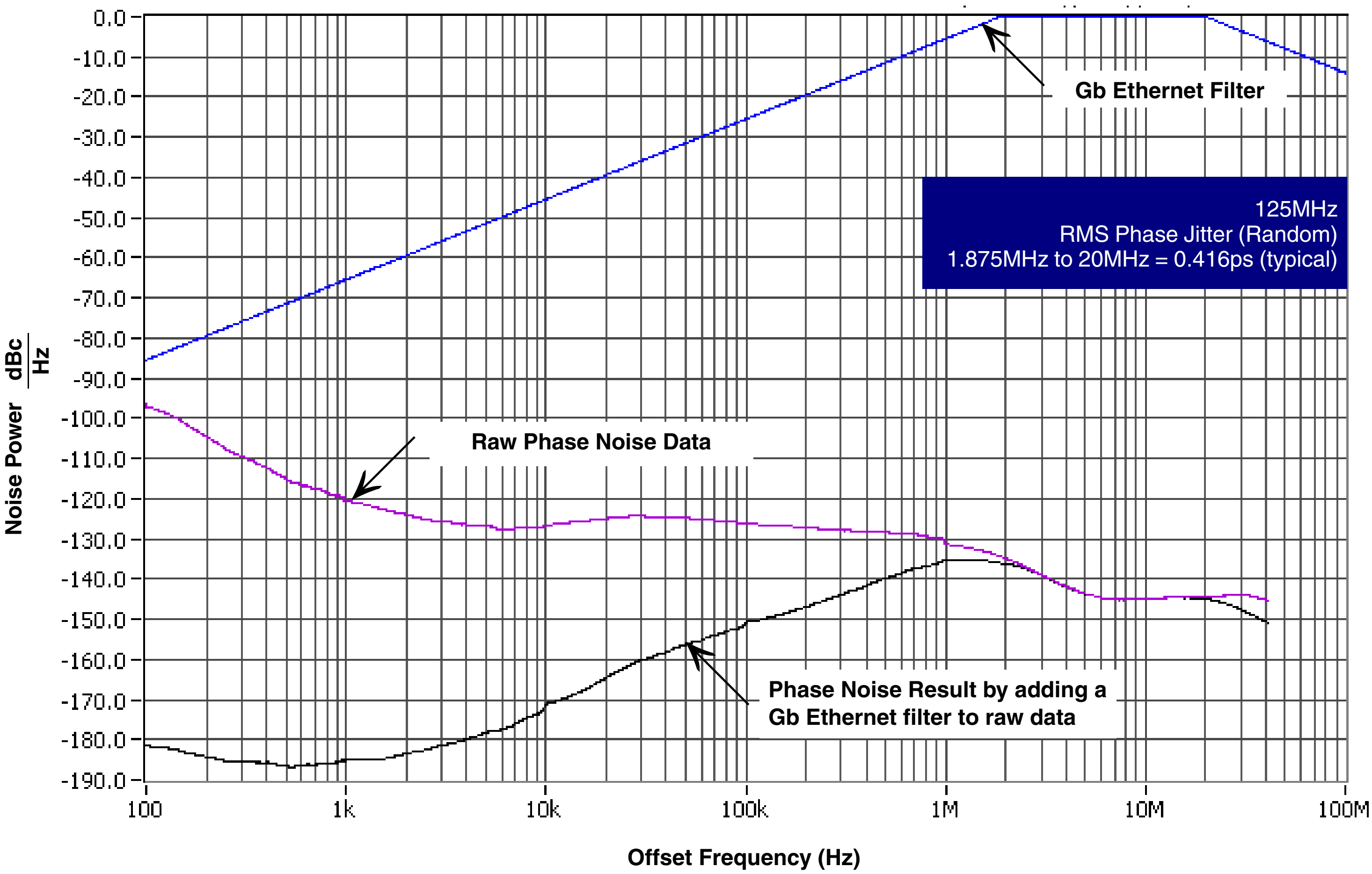
AC Electrical Characteristics

Table 6. LVDS AC Characteristics, V_{DD} = 3.3V ± 5%, V_{DDO} = 3.3V ± 5% or 2.5V ± 5%, T_A = -40°C to 85°C

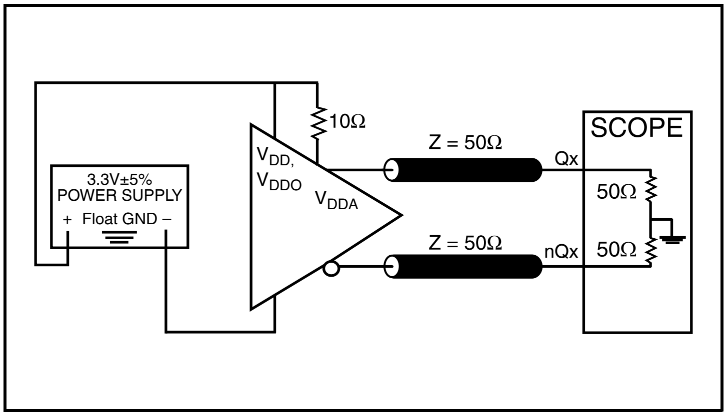
Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
f_{OUT}	Output Frequency	PLL_BYPASS = 0	50		333.33	MHz
		In bypass mode with 25MHz Crystal, PLL_BYPASS = 1 (default)		3.125		MHz
$tjit(Ø)$	RMS Phase Jitter (Random); NOTE 1	125MHz, Integration Range: 1.875MHz – 20MHz		0.416	0.560	ps
tsk(o)	Output Skew; NOTE 2, 3				45	ps
t_R / t_F	Output Rise/Fall Time	20% to 80%	220		380	ps
odc	Output Duty Cycle		45		55	%
t_{LOCK}	PLL Lock Time				25	ms

NOTE: Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lfpm. The device will meet specifications after thermal equilibrium has been reached under these conditions.
NOTE 1: See Phase Noise Plot.
NOTE 2: Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured at the output differential crosspoints.
NOTE 3: This parameter is defined in accordance with JEDEC Standard 65.

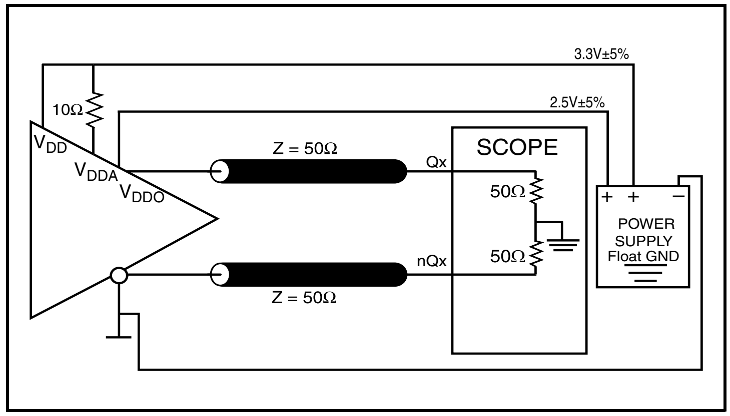
Typical Phase Noise at 125MHz



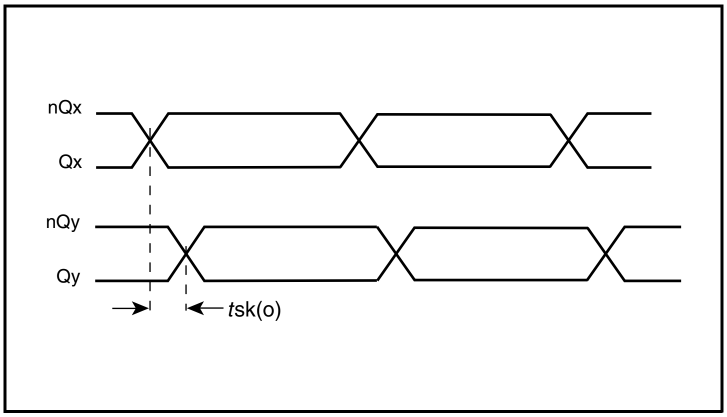
Parameter Measurement Information



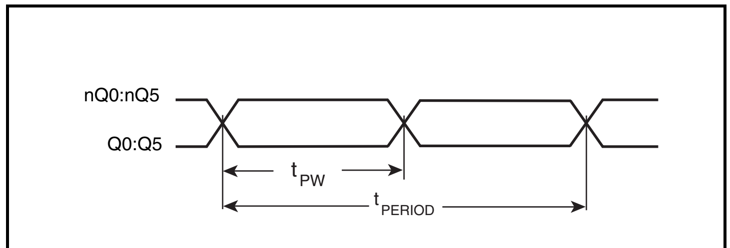
3.3V Core/3.3V LVDS Output Load AC Test Circuit



3.3V Core/2.5V LVDS Output Load AC Test Circuit

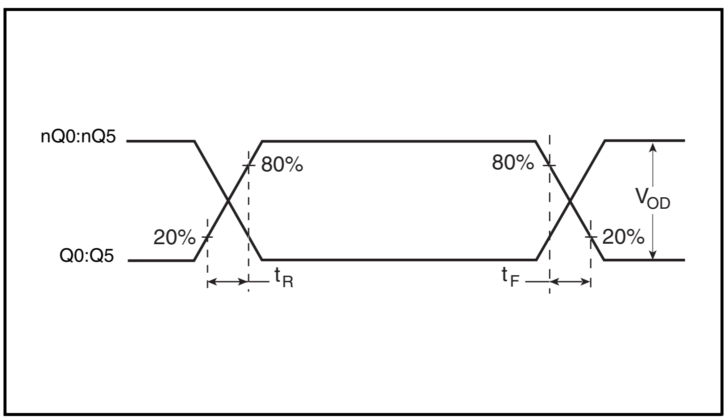


Output Skew

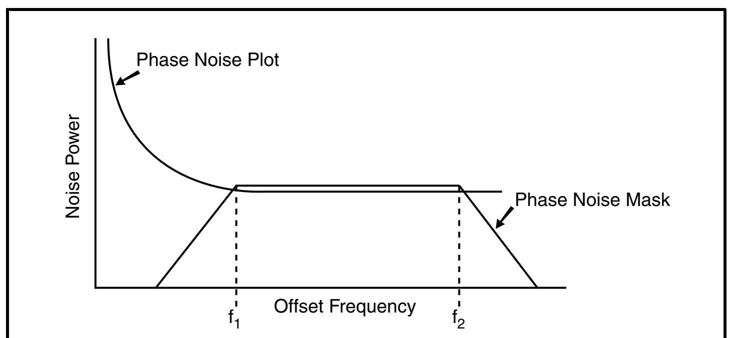


$$odc = \frac{t_{PW}}{t_{PERIOD}} \times 100\%$$

Output Duty Cycle/Pulse Width/Period



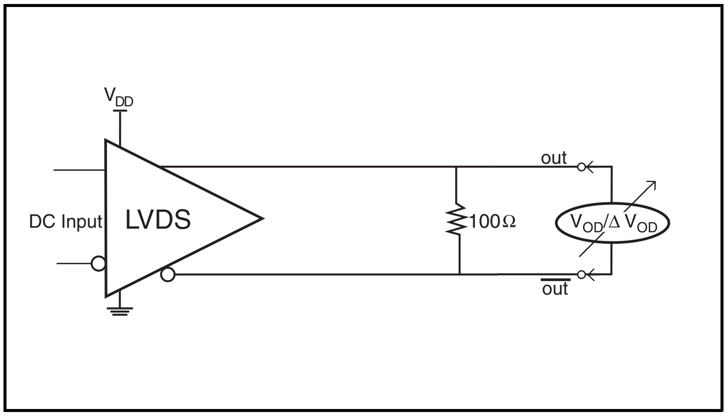
Output Rise/Fall Time



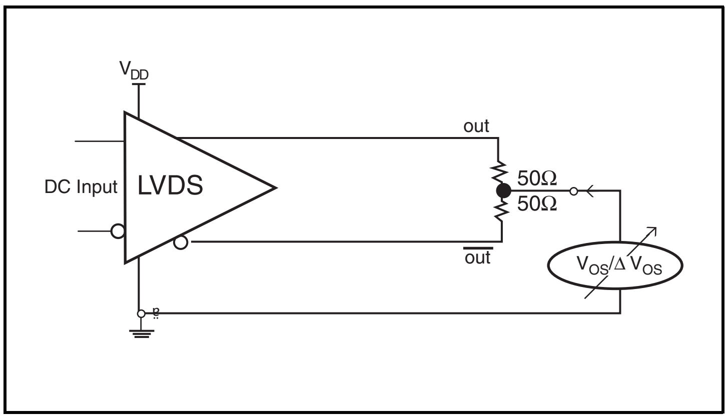
$$\text{RMS Jitter} = \sqrt{\text{Area Under the Masked Phase Noise Plot}}$$

RMS Phase Jitter

Parameter Measurement Information, continued



Differential Output Voltage Setup



Offset Voltage Setup

Applications Information

Overdriving the XTAL Interface

The XTAL_IN input can be overdriven by an LVCMOS driver or by one side of a differential driver through an AC coupling capacitor. The XTAL_OUT pin can be left floating. The amplitude of the input signal should be between 500mV and 1.8V and the slew rate should not be less than 0.2V/nS. For 3.3V LVCMOS inputs, the amplitude must be reduced from full swing to at least half the swing in order to prevent signal interference with the power rail and to reduce internal noise. *Figure 1A* shows an example of the interface diagram for a high speed 3.3V LVCMOS driver. This configuration requires that the sum of the output impedance of the driver (Ro) and the series resistance (Rs) equals the transmission line impedance. In addition, matched termination at the crystal input will attenuate the signal in half. This can be done in one of two ways. First, R1 and R2 in parallel should equal the transmission line impedance. For most 50Ω applications, R1 and R2 can be 100Ω. This can also be accomplished by removing R1 and changing R2 to 50Ω. The values of the resistors can be increased to reduce the loading for a slower and weaker LVCMOS driver. *Figure 1B* shows an example of the interface diagram for an LVPECL driver. This is a standard LVPECL termination with one side of the driver feeding the XTAL_IN input. It is recommended that all components in the schematics be placed in the layout. Though some components might not be used, they can be utilized for debugging purposes. The datasheet specifications are characterized and guaranteed by using a quartz crystal as the input.

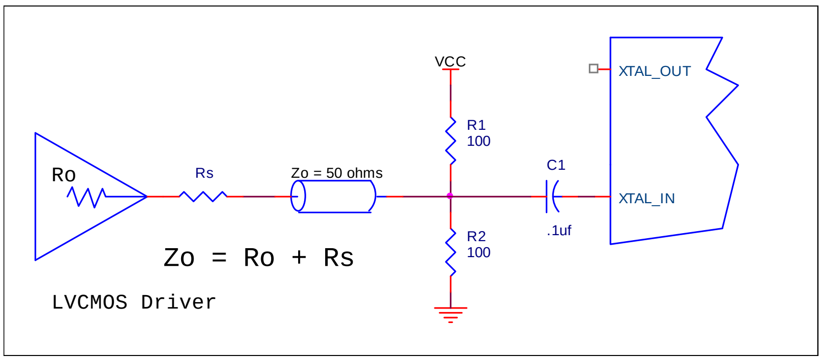


Figure 1A. General Diagram for LVCMOS Driver to XTAL Input Interface

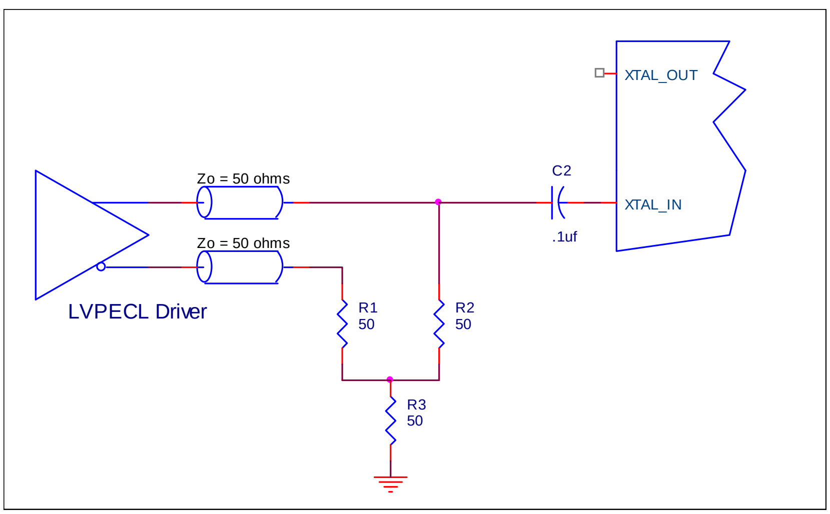


Figure 1B. General Diagram for LVPECL Driver to XTAL Input Interface

Recommendations for Unused Input and Output Pins

Inputs:

LVCMOS Control Pins

All control pins have internal pullups or pulldowns; additional resistance is not required but can be added for additional protection. A 1kΩ resistor can be used.

Outputs:

LVDS Outputs

All unused LVDS output pairs can be either left floating or terminated with 100Ω across. If they are left floating, there should be no trace attached.

LVDS Driver Termination

For a general LVDS interface, the recommended value for the termination impedance (Z_T) is between 90Ω and 132Ω. The actual value should be selected to match the differential impedance (Z_0) of your transmission line. A typical point-to-point LVDS design uses a 100Ω parallel resistor at the receiver and a 100Ω differential transmission-line environment. In order to avoid any transmission-line reflection issues, the components should be surface mounted and must be placed as close to the receiver as possible. IDT offers a full line of LVDS compliant devices with two types of output structures: current source and voltage source. The standard termination schematic as shown in *Figure 2A* can be used with either type of output structure. *Figure 2B*, which can also be used with both output types, is an optional termination with center tap capacitance to help filter common mode noise. The capacitor value should be approximately 50pF. If using a non-standard termination, it is recommended to contact IDT and confirm if the output structure is current source or voltage source type. In addition, since these outputs are LVDS compatible, the input receiver's amplitude and common-mode input range should be verified for compatibility with the output.

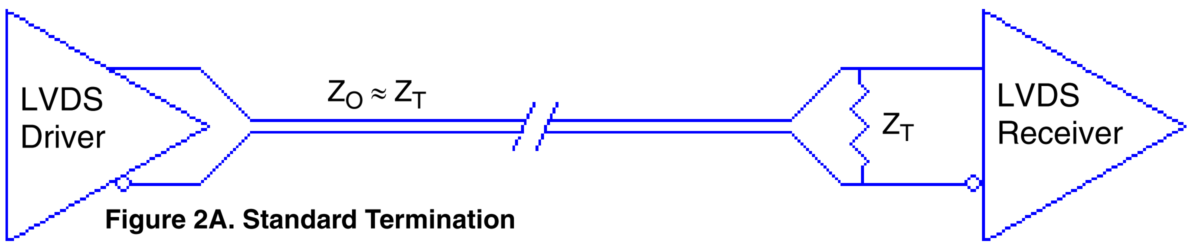


Figure 2A. Standard Termination

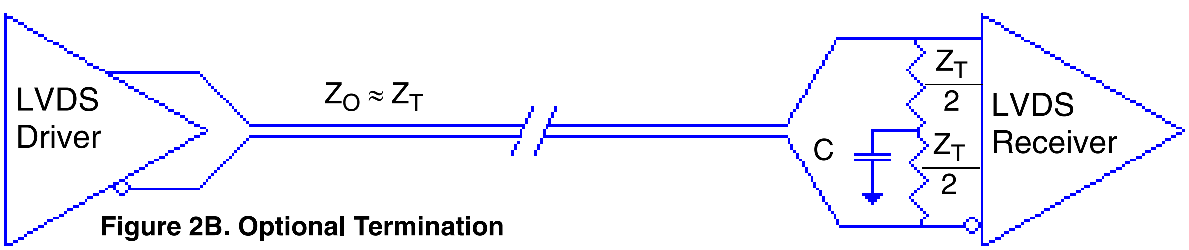


Figure 2B. Optional Termination

LVDS Termination

EPAD Thermal Release Path

In order to maximize both the removal of heat from the package and the electrical performance, a land pattern must be incorporated on the Printed Circuit Board (PCB) within the footprint of the package corresponding to the exposed metal pad or exposed heat slug on the package, as shown in *Figure 3.* The solderable area on the PCB, as defined by the solder mask, should be at least the same size/shape as the exposed pad/slug area on the package to maximize the thermal/electrical performance. Sufficient clearance should be designed on the PCB between the outer edges of the land pattern and the inner edges of pad pattern for the leads to avoid any shorts.

While the land pattern on the PCB provides a means of heat transfer and electrical grounding from the package to the board through a solder joint, thermal vias are necessary to effectively conduct from the surface of the PCB to the ground plane(s). The land pattern must be connected to ground through these vias. The vias act as “heat pipes”. The number of vias (i.e. “heat pipes”) are application specific and dependent upon the package power dissipation as well as electrical conductivity requirements. Thus, thermal and electrical analysis and/or testing are recommended to determine the minimum number needed. Maximum thermal and electrical performance is achieved when an array of vias is incorporated in the land pattern. It is recommended to use as many vias connected to ground as possible. It is also recommended that the via diameter should be 12 to 13mils (0.30 to 0.33mm) with 1oz copper via barrel plating. This is desirable to avoid any solder wicking inside the via during the soldering process which may result in voids in solder between the exposed pad/slug and the thermal land. Precautions should be taken to eliminate any solder voids between the exposed heat slug and the land pattern. Note: These recommendations are to be used as a guideline only. For further information, refer to the Application Note on the *Surface Mount Assembly* of Amkor’s Thermally/Electrically Enhance Leadframe Base Package, Amkor Technology.

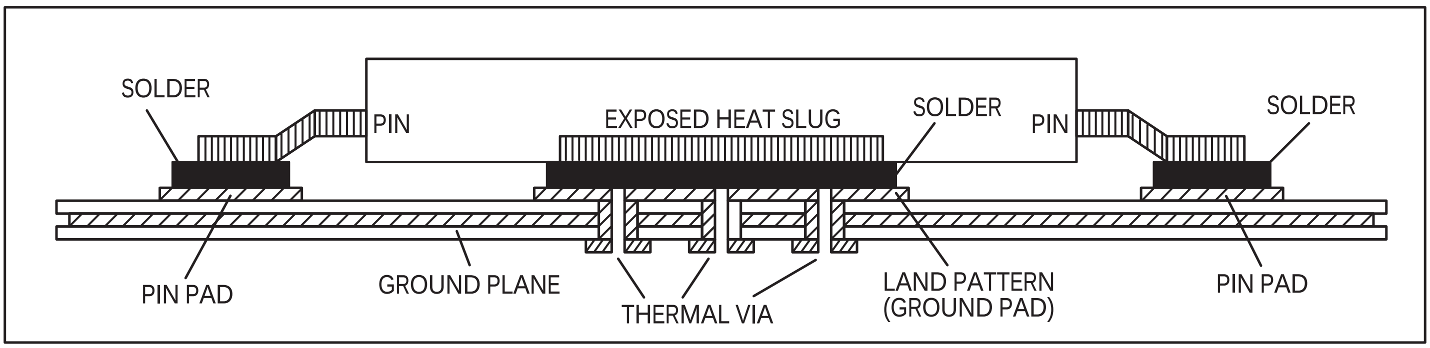


Figure 3. Assembly for Exposed Pad Thermal Release Path - Side View (drawing not to scale)

Schematic Layout

Figure 4 shows an example of ICS844246DI-08 application schematic. The schematic example focuses on functional connections and is not configuration specific. Refer to the pin description and functional tables in the datasheet to ensure the logic control inputs are properly set. Input and output terminations shown are intended as examples only and may not represent the exact user configuration.

In this example an 18pF parallel resonant 25MHz crystal is used with load caps C7 = C6 = 22pF. The load caps are recommended for frequency accuracy, but these may be adjusted for different board layouts. Crystals with different load capacities may be used, but the load capacitors will have to be changed accordingly. If different crystal types are used, please consult IDT for recommendations.

The schematic example shows two different LVDS output terminations; the standard termination 100Ω shunt termination for an LVDS compliant receiver and an AC coupled termination for a non-LVDS differential receiver. The AC coupled termination requires that the designer select the values of R4 and R6 in order to center the LVDS swing within the common mode range of the receiver. In addition the designer must make sure that the target receiver will operate reliably with the LVDS swing, which is reduced relative to other logic families such as HCSL or LVPECL.

As with any high speed analog circuitry, the power supply pins are vulnerable to random noise. To achieve optimum jitter performance, power supply isolation is required. The ICS844246DI provides separate V_{DD}, V_{DDA} and V_{DDO} pins to isolate any high speed switching noise at the outputs from coupling into the internal PLL.

In order to achieve the best possible filtering, it is recommended that the placement of the filter components be on the device side of the PCB as close to the power pins as possible. If space is limited, the 0.1uF capacitor in each power pin filter should be placed on the device side of the PCB and the other components can be placed on the opposite side.

Power supply filter recommendations are a general guideline to be used for reducing external noise from coupling into the devices. The filter performance is designed for wide range of noise frequencies. This low-pass filter starts to attenuate noise at approximately 10kHz. If a specific frequency noise component is known, such as switching power supply frequencies, it is recommended that component values be adjusted and if required, additional filtering be added. Additionally, good general design practices for power plane voltage stability suggests adding bulk capacitances in the local area of all devices.

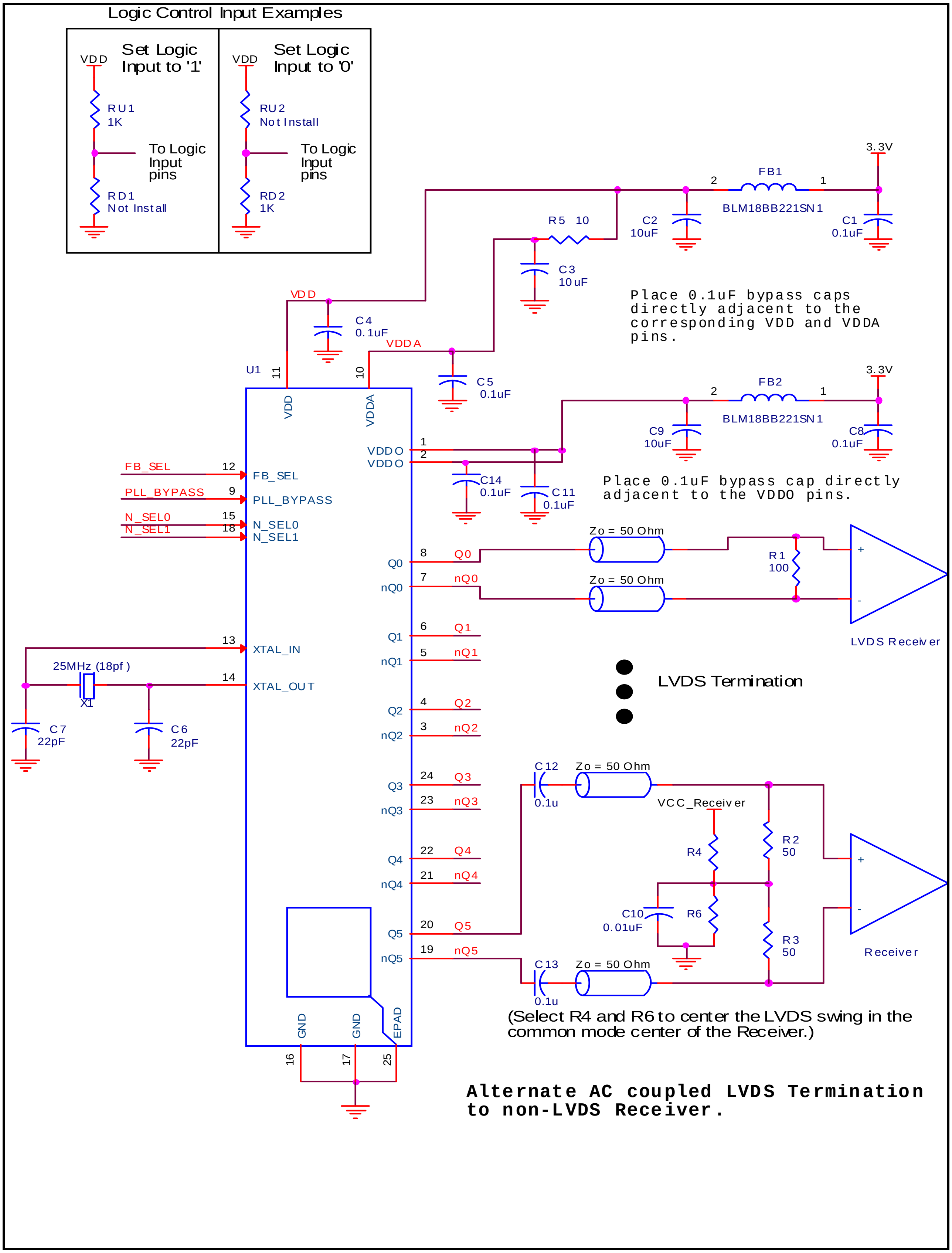


Figure 4. ICS844246DI Application Schematic

Power Considerations

This section provides information on power dissipation and junction temperature for the ICS844246DI.
Equations and example calculations are also provided.

1. Power Dissipation.

The total power dissipation for the ICS844246DI is the sum of the core power plus the analog power plus the power dissipated in the load(s). The following is the power dissipation for V_{DD} = 3.3V + 5% = 3.465V, which gives worst case results.

NOTE: Please refer to Section 3 for details on calculating power dissipated in the load.

- Power $(core)_{MAX} = V_{DD\_MAX} * (I_{DD\_MAX} + I_{DDA\_MAX})$ = 3.465V * (170mA + 10mA) = **623.7mW**
- Power $(outputs)_{MAX} = V_{DDO\_MAX} * I_{DDO\_MAX}$ = 3.465V * 100mA = **346.5mW**

Total Power$_{\_MAX}$ = 623.7mW + 346.5mW = **970.2mW**

2. Junction Temperature.

Junction temperature, Tj, is the temperature at the junction of the bond wire and bond pad, and directly affects the reliability of the device. The maximum recommended junction temperature is 125°C. Limiting the internal transistor junction temperature, Tj, to 125°C ensures that the bond wire and bond pad temperature remains below 125°C.

The equation for Tj is as follows: Tj = θ_{JA} * Pd_total + T_A

Tj = Junction Temperature

θ_{JA} = Junction-to-Ambient Thermal Resistance

Pd_total = Total Device Power Dissipation (example calculation is in section 1 above)

T_A = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance θ_{JA} must be used. Assuming no air flow and a multi-layer board, the appropriate value is 32.1°C/W per Table 7 below.

Therefore, Tj for an ambient temperature of 85°C with all outputs switching is:

85°C + 0.970W * 32.1°C/W = 116.1°C. This is below the limit of 125°C.

This calculation is only an example. Tj will obviously vary depending on the number of loaded outputs, supply voltage, air flow and the type of board (multi-layer).

Table 7. Thermal Resistance θ_{JA} for 24 Lead TSSOP, E-Pad Forced Convection

θ_{JA} by Velocity			
Meters per Second	**0**	**1**	**2.5**
Multi-Layer PCB, JEDEC Standard Test Boards	32.1°C/W	25.5°C/W	24.0°C/W

Reliability Information

Table 8. θ_{JA} vs. Air Flow Table for a 24 Lead TSSOP, E-Pad

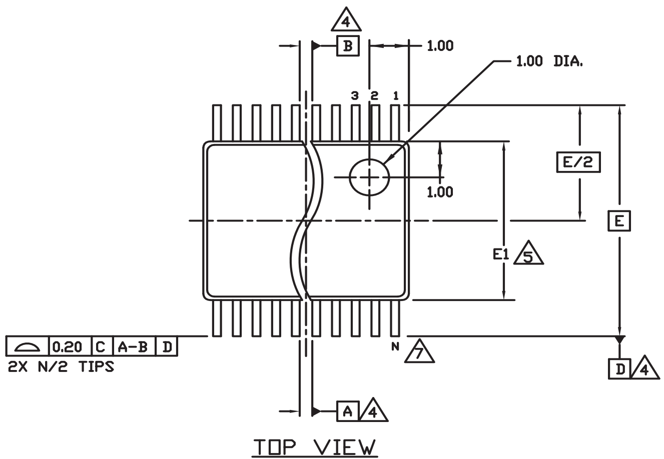
θ_{JA} vs. Air Flow			
Meters per Second	**0**	**1**	**2.5**
Multi-Layer PCB, JEDEC Standard Test Boards	32.1°C/W	25.5°C/W	24.0°C/W

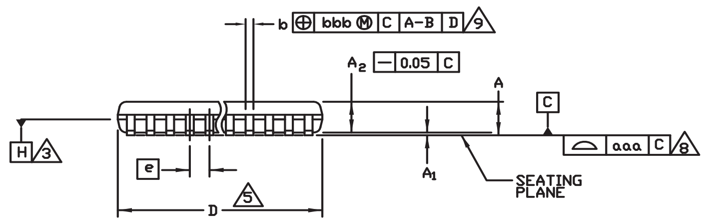
Transistor Count

The transistor count for ICS844246DI is: 3887

Package Outline and Package Dimensions

Package Outline - G Suffix for 24 Lead TSSOP, E-Pad





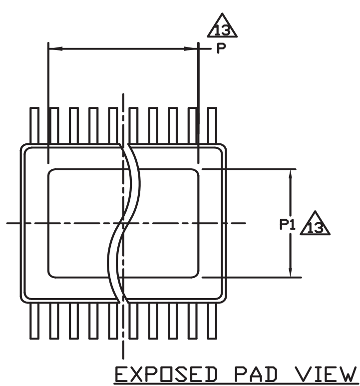
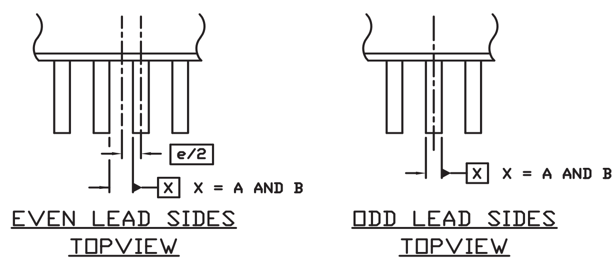
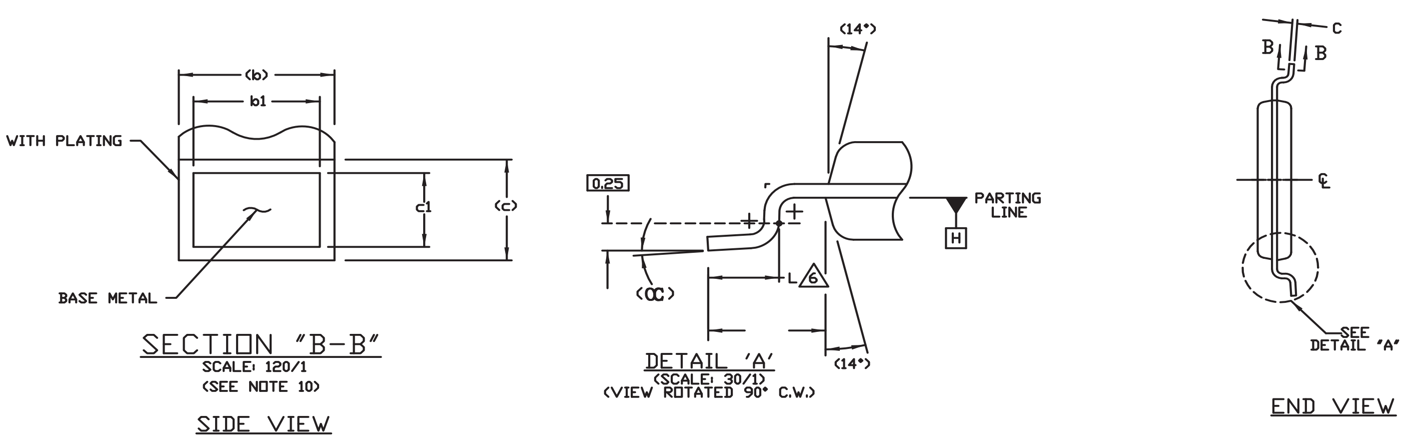


Table 9. Package Dimensions for 24 Lead TSSOP, E-Pad)

All Dimensions in Millimeters			
Symbol	**Minimum**	**Nominal**	**Maximum**
N		24	
A			1.10
A1	0.05		0.15
A2	0.85	0.90	0.95
b	0.19		0.30
b1	0.19	0.22	0.25
c	0.09		0.20
c1	0.09	0.127	0.16
D	7.70		7.90
E		6.40 Basic	
E1	4.30	4.40	4.50
e		0.65 Basic	
L	0.50	0.60	0.70
P	5.0		5.5
P1	3.0		3.2
α	0°		8°
ααα		0.076	
bbb		0.10	

Reference Document: JEDEC Publication 95, MO-153





Ordering Information

Table 10. Ordering Information

Part/Order Number	Marking	Package	Shipping Packaging	Temperature
844246DGILF	ICS844246DGIL	"Lead-Free" 24 Lead TSSOP, E-Pad	Tube	-40°C to 85°C
844246DGILFT	ICS844246DGIL	"Lead-Free" 24 Lead TSSOP, E-Pad	Tape & Reel	-40°C to 85°C

Revision History Sheet

Rev	Table	Page	Description of Change	Date
A		7	Phase Noise Plot - corrected font arrow characters.	11/28/2012

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