



0.5 dB LSB GaAs MMIC 6-BIT DIGITAL VARIABLE GAIN AMPLIFIER, 70 MHz - 4 GHz

Typical Applications

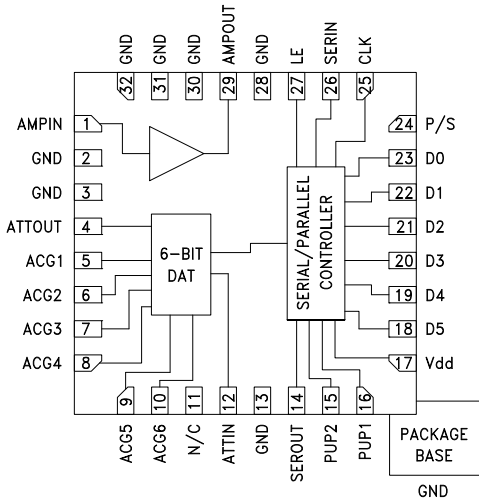
The HMC742ALP5E is ideal for:

- Cellular/3G Infrastructure
- WiBro / WiMAX / 4G
- Microwave Radio & VSAT
- Test Equipment and Sensors
- IF & RF Applications

Features

- 19.5 to 12 dB Gain Control in 0.5 dB Steps
- Power-up State Selection
- High Output IP3: +39 dBm
- TTL/CMOS Compatible
- Serial, Parallel, or latched Parallel Control
- ±0.25 dB Typical Gain Step Error
- Single +5V Supply
- 32 Lead 5x5 mm SMT Package: 25 mm²

Functional Diagram



General Description

The HMC742ALP5E is a digitally controlled variable gain amplifier which operates from 70 MHz to 4 GHz, and can be programmed to provide from -19.5 dB attenuation, to 12 dB of gain, in 0.5 dB steps. The HMC742ALP5E delivers noise figure of 4 dB in its maximum gain state, with output IP3 of up to +39 dBm in any state. The dual mode gain control interface accepts either a three-wire serial input or a 6 bit parallel word. The HMC742ALP5E also features a user selectable power up state and a serial output for cascading other serially controlled Hittite components. The HMC742ALP5E is housed in an RoHS compliant 5x5 mm QFN leadless package, and requires minimal external components.

Electrical Specifications, $T_A = +25^\circ C$, 50 Ohm System $V_{dd} = +5V$, $V_s = +5V$

| Parameter | Min. | Typ. | Max. | Min. | Typ. | Max. | Units | |
|---|--|------|------|--|------|------|-------|------------|
| | | | | 70 - 1000 | | | | 500 - 4000 |
| Gain (Maximum Gain State) | | 12 | | | 10 | | dB | |
| Gain Control Range | | 31.5 | | | 31.5 | | dB | |
| Input Return Loss | | 15 | | | 12 | | dB | |
| Output Return Loss | | 14 | | | 10 | | dB | |
| Gain Accuracy: (Referenced to Maximum Gain State) All Gain States | 70 MHz - 350 MHz ± (0.3 + 5% of relative gain setting) Max. | | | 350 MHz - 1000 MHz ± (0.3 + 4% of relative gain setting) Max. | | | dB | |
| Output Power for 1 dB Compression | | 21.5 | | | 22 | | dBm | |
| Output Third Order Intercept Point (Two-Tone Output Power= 12 dBm Each Tone) | | 39 | | | 39 | | dBm | |
| Noise Figure (Max Gain State) | | 4 | | | 4.5 | | dB | |
| Switching Characteristics tRISE, tFall (10 / 90% RF) | | 70 | | | 70 | | ns | |
| tON, tOFF (Latch Enable to 10 / 90% RF) | | 140 | | | 140 | | ns | |
| Supply Current (Amplifier) I_s | 130 | 150 | 175 | 130 | 150 | 175 | mA | |
| Supply Current (Controller) I_{dd} | 1.0 | 2.5 | 3.5 | 1.0 | 2.5 | 3.5 | mA | |

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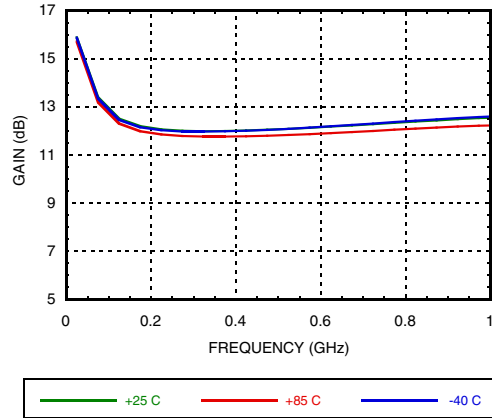
For price, delivery, and to place orders: Analog Devices, Inc., One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106 Phone: 781-329-4700 • Order online at www.analog.com Application Support: Phone: 1-800-ANALOG-D



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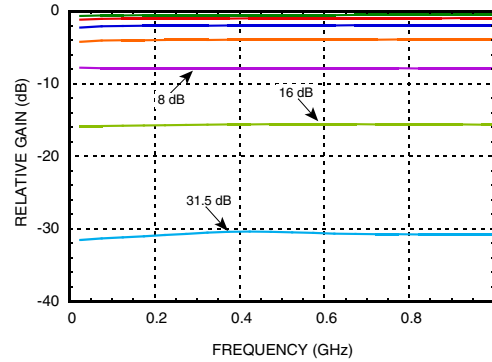
70 to 1000 MHz Tuning

Maximum Gain vs. Temperature

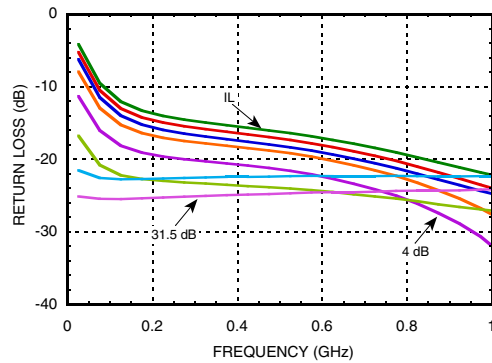


Relative Gain Setting

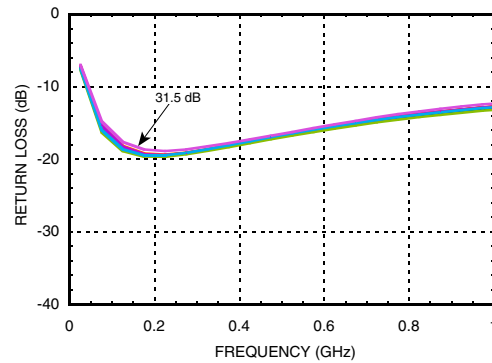
(Referenced to Maximum Gain State)



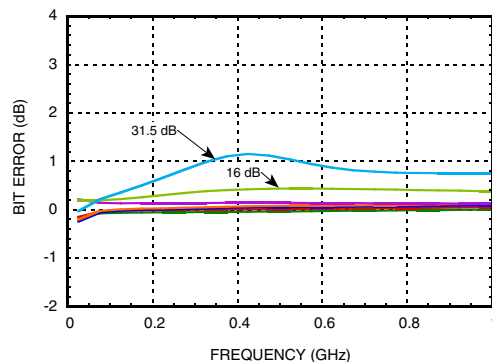
Input Return Loss



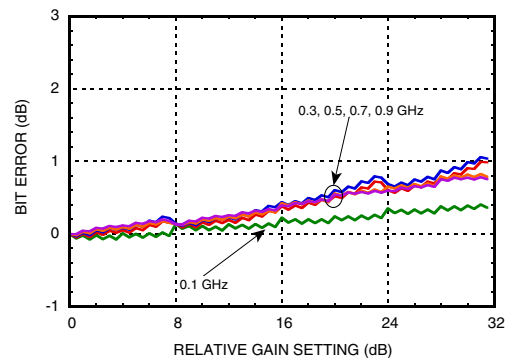
Output Return Loss



Bit Error vs. Frequency



Bit Error vs. Relative Gain



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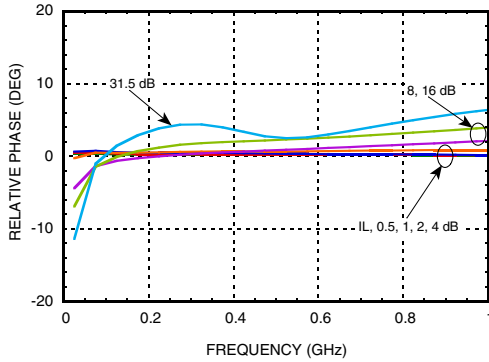


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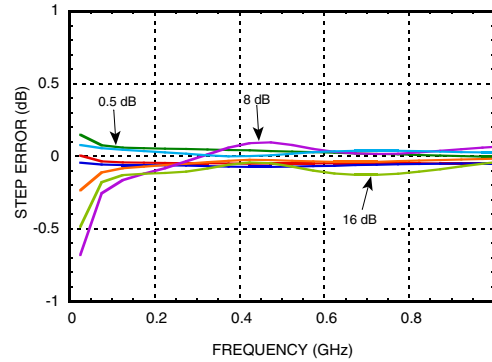
70 to 1000 MHz Tuning

VARIABLE GAIN AMPLIFIERS - DIGITAL - SMT

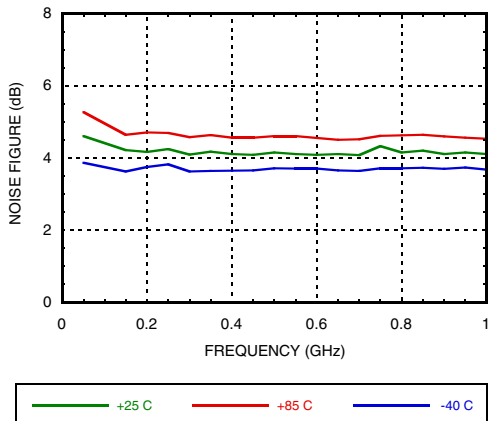
Relative Phase vs. Frequency



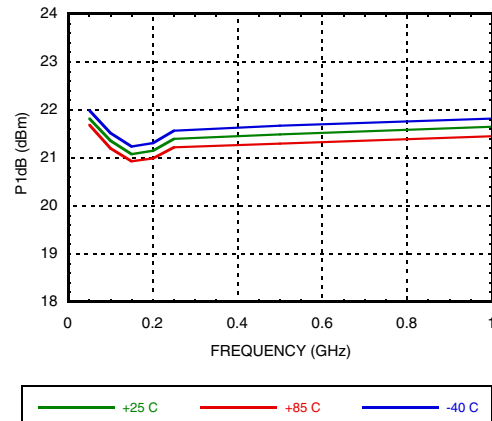
Step Error vs. Frequency



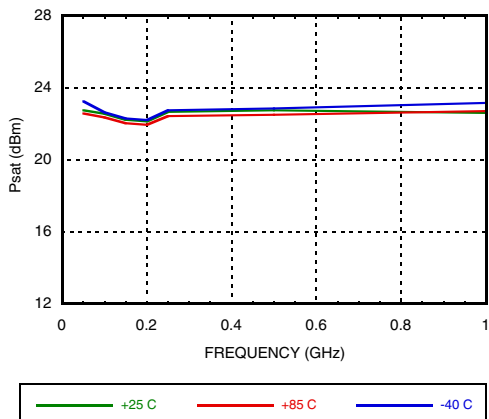
Noise Figure vs. Temperature [1]



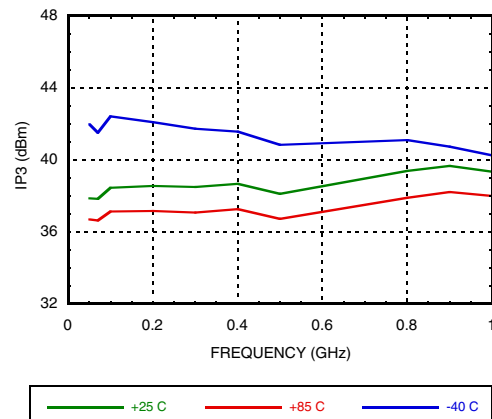
Output P1dB vs. Temperature



Psat vs. Temperature



Output IP3 vs. Temperature



[1] Max Gain State

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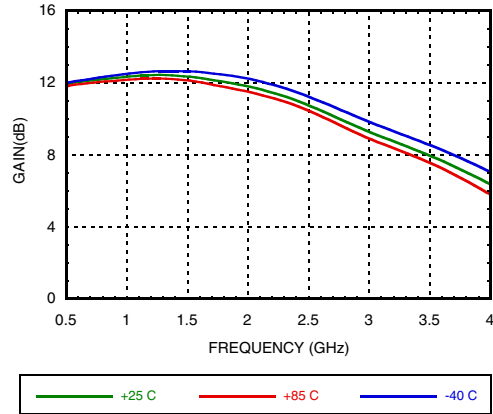
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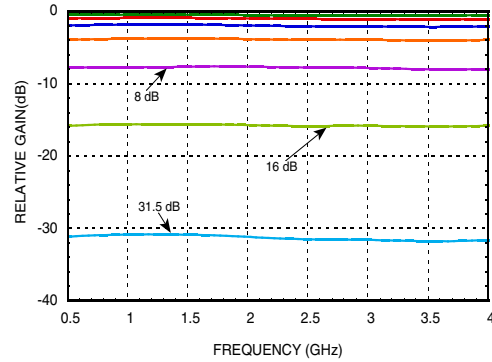
0.5 to 4.0 GHz Tuning

Maximum Gain vs. Frequency

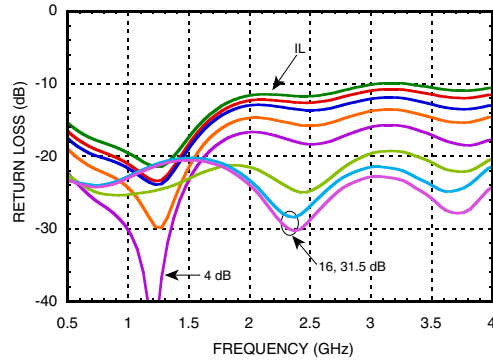


Relative Gain Setting

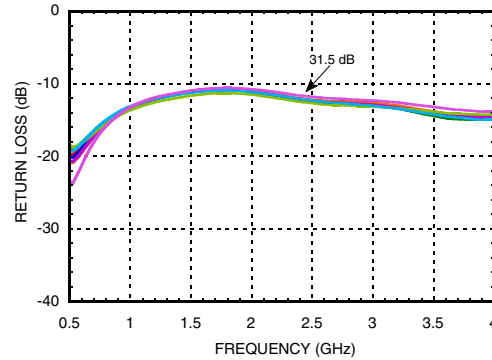
(Referenced to Maximum Gain State)



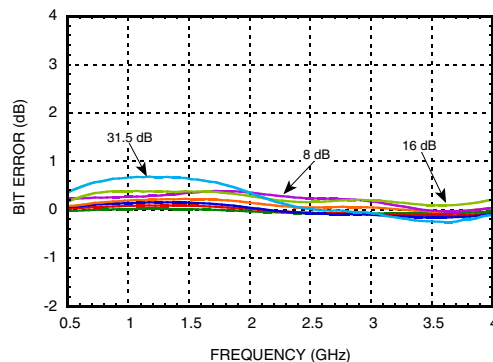
Input Return Loss



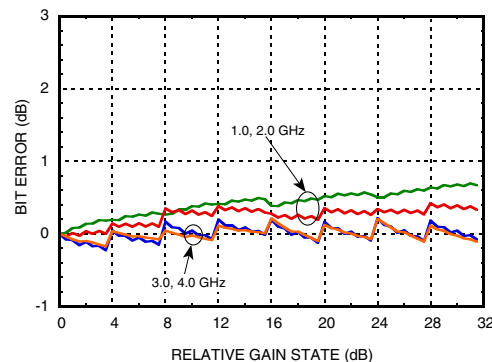
Output Return Loss



Bit Error vs. Frequency



Bit Error vs. Relative Gain



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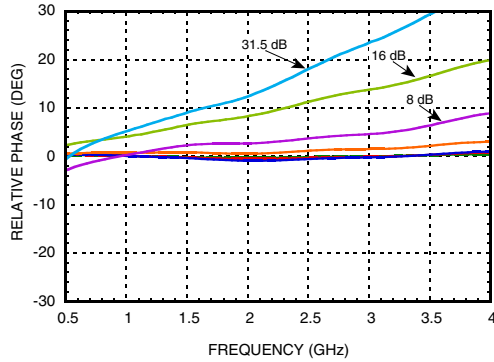
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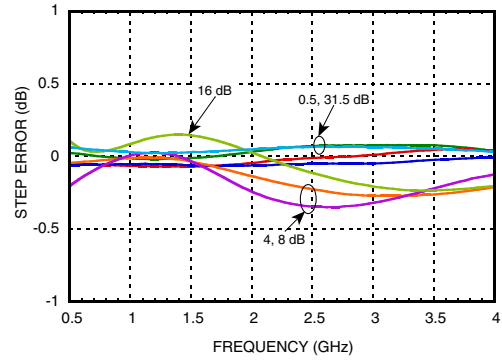
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0.5 to 4.0 GHz Tuning

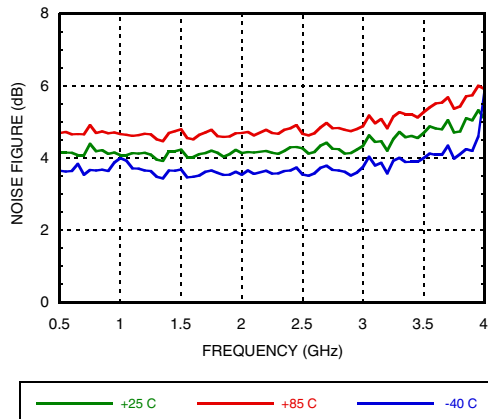
Relative Phase vs. Frequency



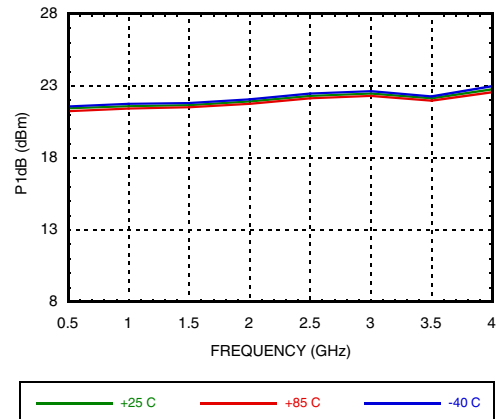
Step Error vs. Frequency



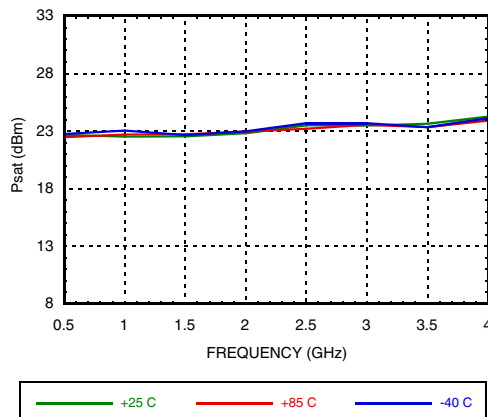
Noise Figure vs. Frequency [1]



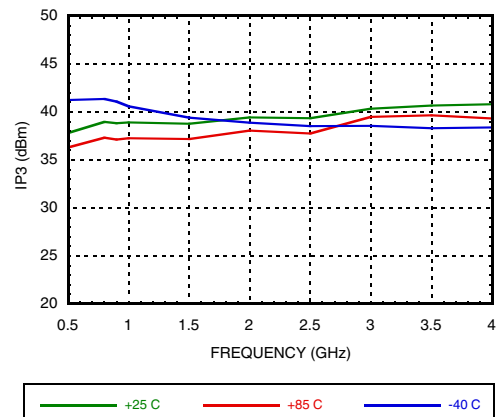
Output P1dB vs. Temperature



Psat vs. Temperature



Output IP3 vs. Temperature



[1] Max Gain State

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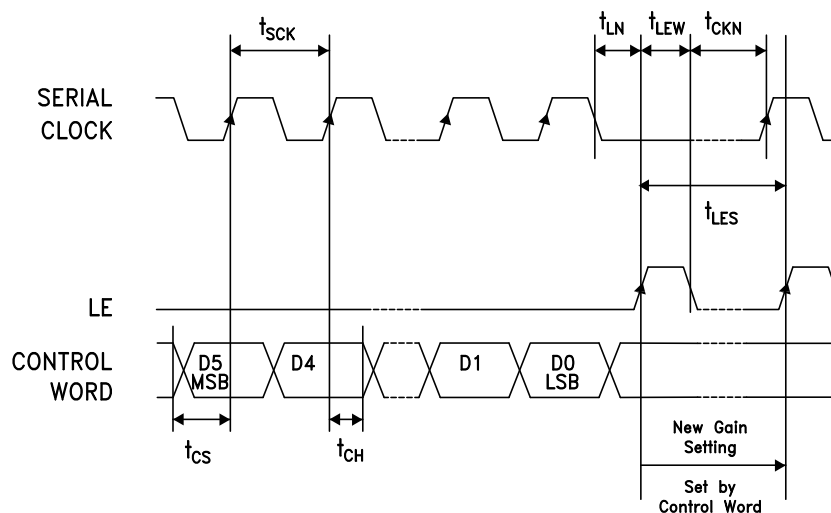
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Serial Control Interface

The HMC742ALP5E contains a 3-wire SPI compatible digital interface (SERIN, CLK, LE). The serial control interface is activated when P/S is kept high. The 6-bit serial word must be loaded MSB first. The positive-edge sensitive CLK and LE requires clean transitions. If mechanical switches are used, sufficient debouncing should be provided. When LE is high, 6-bit data in the serial input register is transferred to the attenuator. When LE is high CLK is masked to prevent data transition during output loading.

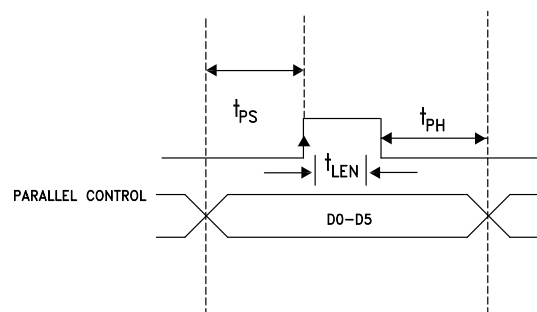
When P/S is low, 3-wire SPI interface inputs (SERIN, CLK, LE) are disabled and the input register is loaded with parallel digital inputs (D0-D5). When LE is high, 6-bit parallel data changes the state of the part per truth table.

For all modes of operations, the DVGA state will stay constant while LE is kept low.



| Parameter | Typ. |
|---|--------|
| Min. serial period, t_{SCK} | 100 ns |
| Control set-up time, t_{CS} | 20 ns |
| Control hold-time, t_{CH} | 20 ns |
| LE setup-time, t_{LN} | 10 ns |
| Min. LE pulse width, t_{LEW} | 10 ns |
| Min LE pulse spacing, t_{LES} | 630 ns |
| Serial clock hold-time from LE, t_{CKN} | 10 ns |
| Hold Time, t_{PH} | 0 ns |
| Latch Enable Minimum Width, t_{LEN} | 10 ns |
| Setup Time, t_{PS} | 2 ns |

Timing Diagram (Latched Parallel Mode)



Parallel Mode

(Direct Parallel Mode & Latched Parallel Mode)

Note: The parallel mode is enabled when P/S is set to low.

Direct Parallel Mode - The attenuation state is changed by the control voltage inputs D0-D5 directly. The LE (Latch Enable) must be at a logic high at all times to control the attenuator in this manner.

Latched Parallel Mode - The attenuation state is selected using the control voltage inputs D0-D5 and set while the LE is in the Low state. The attenuator will not change state while LE is Low. Once all Control Voltage Inputs are at the desired states the LE is pulsed. See timing diagram above for reference.



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Power-Up States

If LE is set to logic LOW at power-up, the logic state of PUP1 and PUP2 determines the power-up state of the part per PUP truth table. If the LE is set to logic HIGH at power-up, the logic state of D0-D5 determines the power-up state of the part per truth table. The DVGA latches in the desired power-up state approximately 200 ms after power-up.

Power-On Sequence

The ideal power-up sequence is: GND, Vdd, digital inputs, RF inputs. The relative order of the digital inputs are not important as long as they are powered after Vdd / GND

Absolute Maximum Ratings

| | |
|---|-----------------------|
| RF Input Power at Max Gain ^[1] | 17.5 dBm (T = +85 °C) |
| Digital Inputs (Reset, Shift Clock, Latch Enable & Serial Input) | -0.5 to Vdd +0.5V |
| Bias Voltage (Vdd) | 5.6V |
| Collector Bias Voltage (Vcc) | 5.5V |
| Channel Temperature | 150 °C |
| Continuous P _{diss} (T = 85 °C) (derate 13.3 mW/°C above 85 °C) ^[2] | 0.86 W |
| Thermal Resistance ^[3] | 75.6 °C/W |
| Storage Temperature | -65 to +150 °C |
| Operating Temperature | -40 to +85 °C |
| ESD Sensitivity (HBM) | Class 1A |

[1] The maximum RF input power increases by the same amount the gain is reduced. The maximum input power at any state is no more than 28 dBm.

[2] This value is the total power dissipation in the amplifier.

[3] This is the thermal resistance for the amplifier.

Bias Voltage

| | |
|--------------------|-----------------------------|
| Vdd (V) | I _{dd} (Typ.) (mA) |
| +5.0 | 2.5 |
| V _s (V) | I _s (mA) |
| +5.0 | 150 |

PUP Truth Table

| LE | PUP1 | PUP2 | Gain Relative to Maximum Gain |
|----|------|------|-------------------------------|
| 0 | 0 | 0 | -31.5 |
| 0 | 1 | 0 | -24 |
| 0 | 0 | 1 | -16 |
| 0 | 1 | 1 | Insertion Loss |
| 1 | X | X | 0 to -31.5 dB |

Note: The logic state of D0 - D5 determines the power-up state per truth table shown below when LE is high at power-up.

Truth Table

| Control Voltage Input | | | | | | Gain Relative to Maximum Gain |
|-----------------------|------|------|------|------|------|-------------------------------|
| D5 | D4 | D3 | D2 | D1 | D0 | |
| High | High | High | High | High | High | 0 dB |
| High | High | High | High | High | Low | -0.5 dB |
| High | High | High | High | Low | High | -1 dB |
| High | High | High | Low | High | High | -2 dB |
| High | High | Low | High | High | High | -4 dB |
| High | Low | High | High | High | High | -8 dB |
| Low | High | High | High | High | High | -16 dB |
| Low | Low | Low | Low | Low | Low | -31.5 dB |

Any combination of the above states will provide a reduction in gain approximately equal to the sum of the bits selected.

Control Voltage Table

| State | Vdd = +3V | Vdd = +5V |
|-------|-------------------|-------------------|
| Low | 0 to 0.5V @ <1 μA | 0 to 0.8V @ <1 μA |
| High | 2 to 3V @ <1 μA | 2 to 5V @ <1 μA |

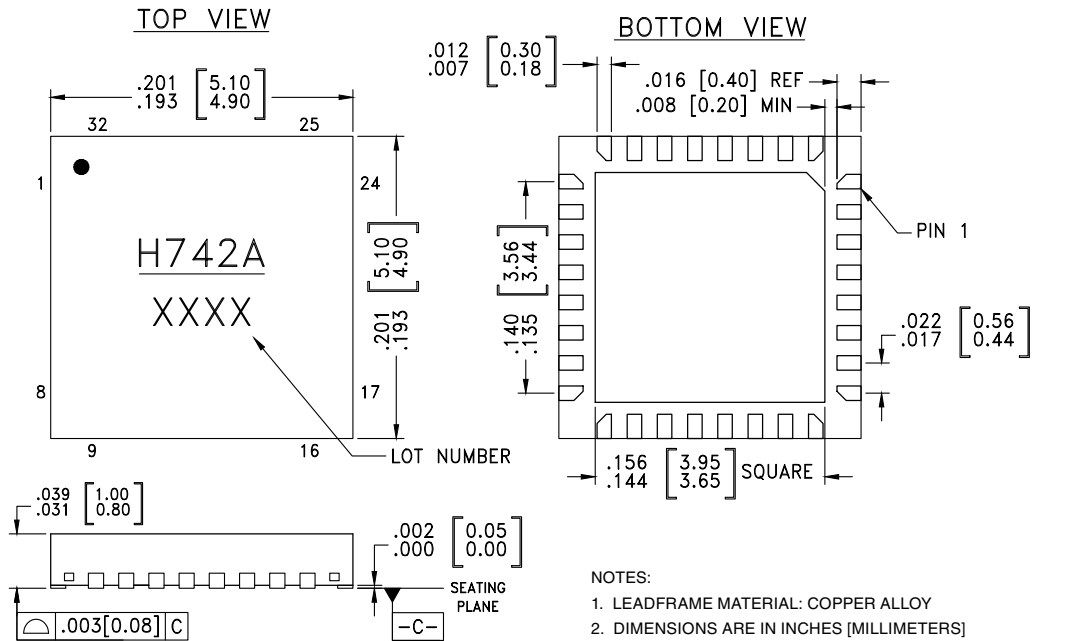


ELECTROSTATIC SENSITIVE DEVICE
OBSERVE HANDLING PRECAUTIONS

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Outline Drawing



Package Information

| Part Number | Package Body Material | Lead Finish | MSL Rating | Package Marking ^[1] |
|-------------|--|---------------|---------------------|--------------------------------|
| HMC742ALP5E | RoHS-compliant Low Stress Injection Molded Plastic | 100% matte Sn | MSL1 ^[2] | H742A XXXX |

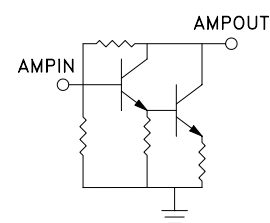

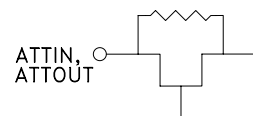
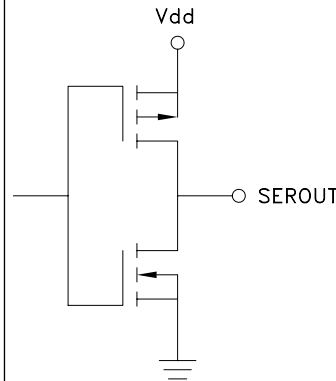
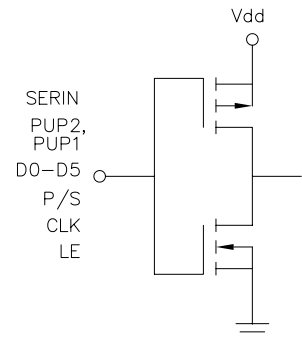
[1] 4-Digit lot number XXXX

[2] Max peak reflow temperature of 260 °C



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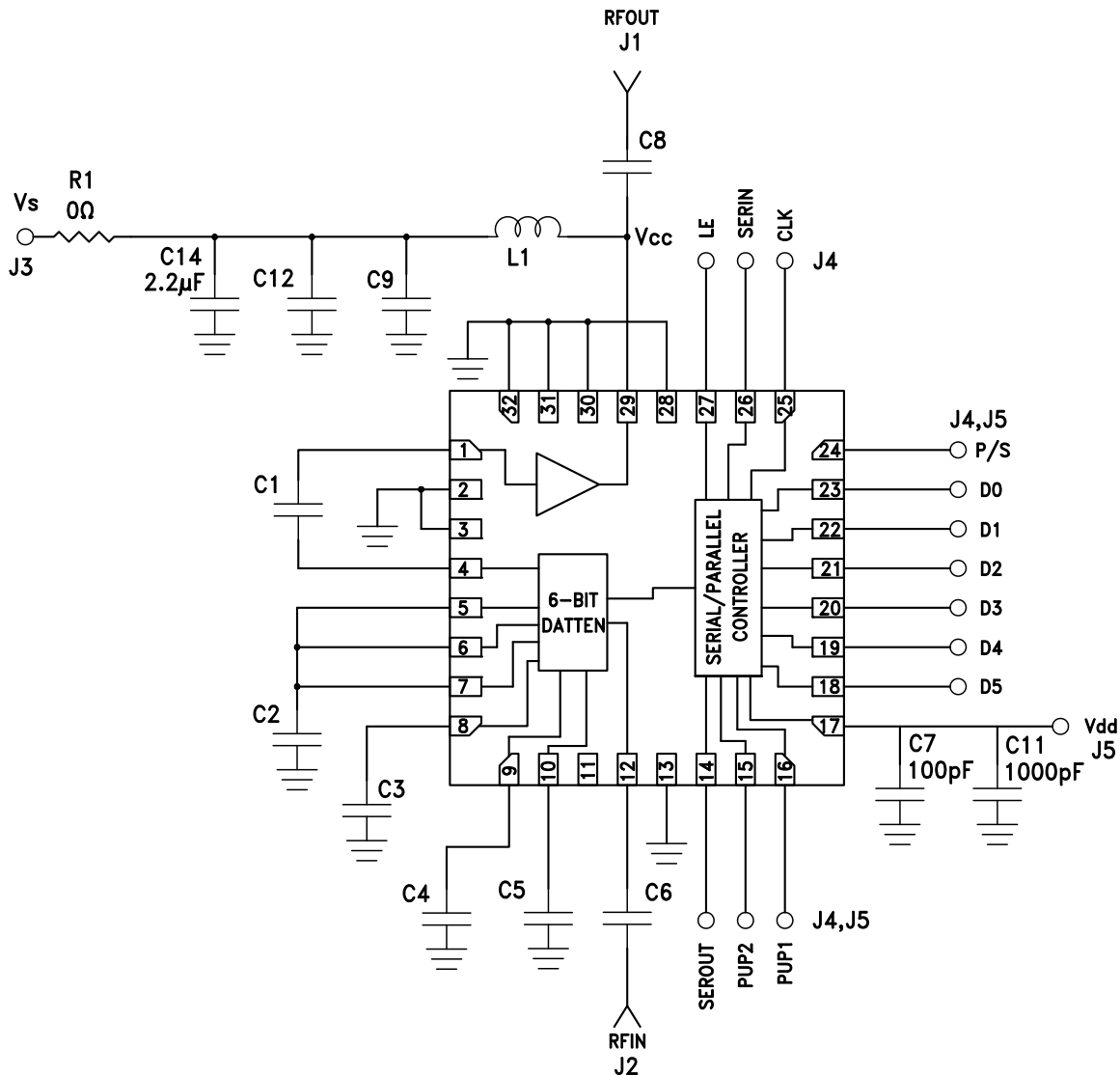
Pin Descriptions

| Pin Number | Function | Description | Interface Schematic |
|--------------------------|---------------------------|--|---|
| 1 | AMPIN | This pin is DC coupled. An off chip DC blocking capacitor is required. |  |
| 29 | AMPOUT | RF output and DC bias (Vcc) for the output stage of the amplifier. | |
| 2, 3, 13, 28, 30 - 32 | GND | These pins and package bottom must be connected to RF/DC ground. |  |
| 4, 12 | ATTOUT, ATTIN | These pins are DC coupled and matched to 50 Ohms. Blocking capacitors are required. Select value based on lowest frequency of operation. |  |
| 5 - 10 | ACG1 - ACG6 | External capacitors to ground is required. Select value for lowest frequency of operation. Place capacitor as close to pins as possible. | |
| 11 | N/C | No connection | |
| 14 | SEROUT | Serial input data delayed by 6 clock cycles. |  |
| 15, 16 | PUP2, PUP1 | |  |
| 18 - 23 | D5, D4, D3, D2, D1, D0 | | |
| 24 | P/S | | |
| 25 | CLK | | |
| 26 | SERIN | | |
| 27 | LE | | |
| 17 | Vdd | Supply Voltage | |



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Application Circuit



Components for Selected Frequencies

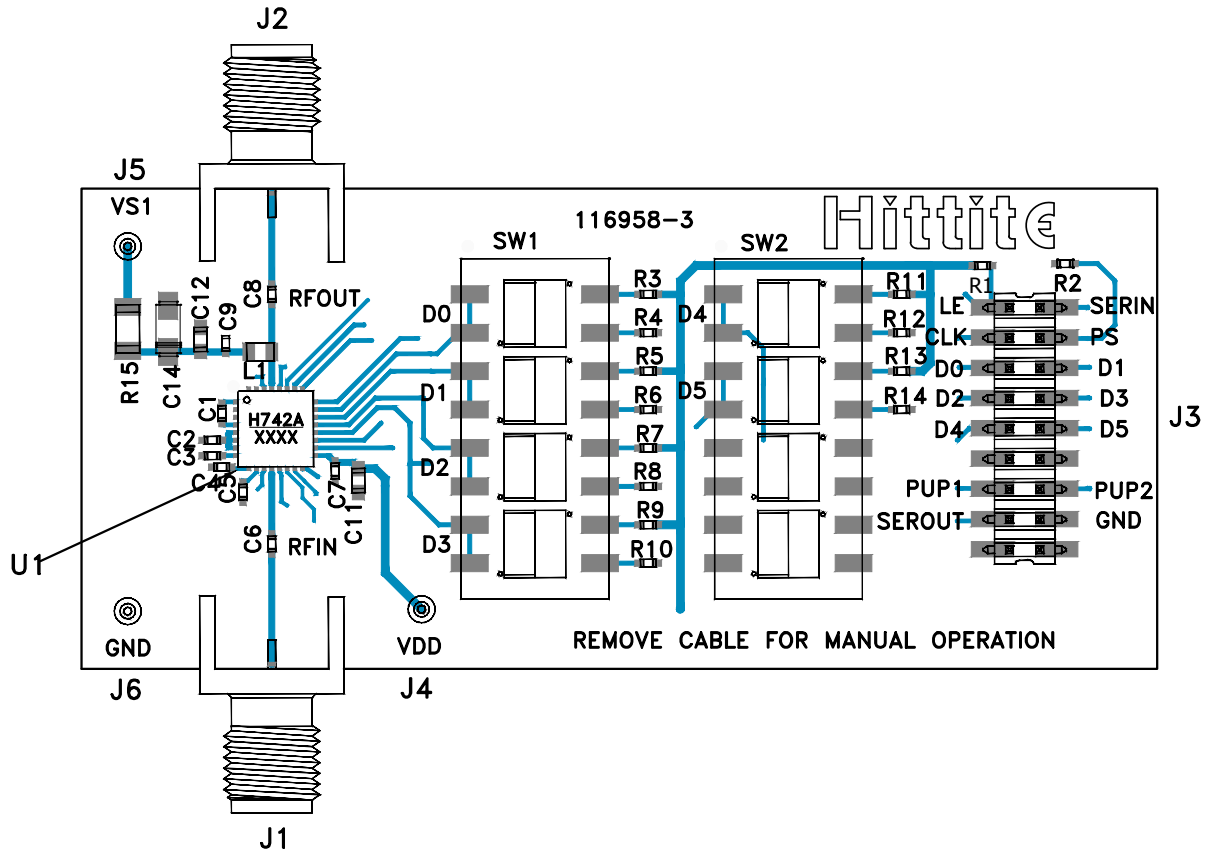
| Tuned Frequency | 70 - 1000 MHz | 500 - 4000 MHz |
|-----------------|-----------------------|-----------------------|
| Evaluation PCB | 124694-HMC742ALP5 [1] | 124695-HMC742ALP5 [1] |
| C1 ,C6, C8 (pF) | 10000 | 330 |
| C3, C4 (pF) | 1000 | 100 |
| C2, C5 (pF) | 1000 | N/A |
| C9 (pF) | 1000 | 100 |
| C12 (pF) | 5600 | 1000 |
| L1 (nH) | 560 | 47 |

[1] Reference this number when ordering complete evaluation PCB



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Evaluation PCB



List of Materials for Evaluation PCB [2]

| Item | Description |
|-----------------|-------------------------------------|
| J1 - J2 | PCB Mount SMA Connectors |
| J3 | 18 Pin DC Connector |
| J4 - J6 | DC Pin |
| C1 - C6, C8, C9 | Capacitor, 0402 Pkg. [2] |
| C7 | 100pF Capacitor. 0402 Pkg. |
| C11 | 1000 pF Capacitor, 0402 Pkg. |
| C12 | Capacitor, 0603 Pkg. [2] |
| C14 | 2.2 μF Capacitor, CASE A Pkg. |
| R1 - R14 | 100 kOhm Resistor, 0402 Pkg. |
| R15 | 0 Ohm Resistor, 1206 Pkg. |
| L1 | Inductor, 0603 Pkg. [2] |
| SW1, SW2 | SPDT 4 Position DIP Switch |
| U1 | HMC742ALP5E Variable Gain Amplifier |
| PCB [1] | 116958 Evaluation PCB |

[1] Circuit Board Material: Arlon 25FR, FR4

[2] Please reference Components for Selected Frequencies Table shown on previous page.

The circuit board used in the application should use RF circuit design techniques. Signal lines should have 50 Ohm impedance while the package ground leads and exposed paddle should be connected directly to the ground plane similar to that shown. A sufficient number of via holes should be used to connect the top and bottom ground planes. The evaluation circuit board shown is available from Hittite upon request.

**0.5 dB LSB GaAs MMIC 6-BIT DIGITAL
VARIABLE GAIN AMPLIFIER, 70 MHz - 4 GHz****Notes:**

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[MAAP-015036-DIEEV2](#) [EV1HMC1113LP5](#) [EV1HMC252AQS24](#) [EV1HMC6146BLC5A](#) [EV1HMC637ALP5](#) [EVAL01-HMC1048LC3B](#)
[EVAL01-HMC661LC4B](#) [EVAL-ADF7020-1DBZ4](#) [EVAL-ADF7020-1DBZ5](#) [EVAL-ADF7020-1DBZ6](#) [EVAL-ADF7021DB9Z](#) [EVAL-](#)
[ADF7021DBJZ](#) [EVAL-ADF7021DBZ2](#) [EVAL-ADF7021DBZ6](#) [EVAL-ADF7021-NDBZ2](#) [EVAL-ADF7021-VDB3Z](#) [EVAL-ADF7023DB3Z](#)
[EVAL-ADF7023-JDB3Z](#) [EVAL-ADF70XXEKZ1](#) [EVAL-ADF7241DB1Z](#) [F0440EVBI](#) [F1423EVB-DI](#) [F1423EVB-SI](#) [F1701EVBI](#)
[F1751EVBI](#) [F2250EVBI](#) [MICRF219A-433 EV](#) [122410-HMC686LP4E](#) [AD6679-500EBZ](#) [126223-HMC789ST89E](#) [ADL5363-EVALZ](#)
[ADL5369-EVALZ](#) [130437-HMC1010LP4E](#) [131352-HMC1021LP4E](#) [131372-HMC951LP4E](#) [130436-HMC1010LP4E](#) [DEMOBOARD-](#)
[U2790B](#) [ATR2406-PNQW](#) [EKIT01-HMC1197LP7F](#) [Si4705-D60-EVB](#) [Si4835-Demo](#) [LMV228SDEVAL](#) [SKYA21001-EVB](#) [SMP1331-08-](#)
[EVB](#) [EV1HMC618ALP3](#) [EV1HMC641ALC4](#) [EV1HMC8410LP2F](#) [EVAL_PAN4555ETU](#) [EVAL01-HMC1041LC4](#) [EVAL-ADF7012DBZ2](#)