

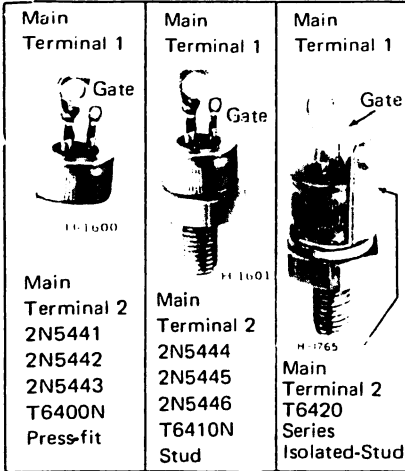


# Thyristors

## 2N5441 2N5442 2N5443

## 2N5444 2N5445 2N5446

## T6400 T6410 T6420 Series



### 40-A Silicon Triacs

Press-Fit, Stud, and Isolated-Stud Packages

For 120-V Line Operation . . . 2N5441, 2N5444, T6420B  
For 240-V Line Operation . . . 2N5442, 2N5445, T6420D  
For High-Voltage Operation . . 2N5443, 2N5446, T6420M  
T6400N, T6410N, T6420N

#### Features:

- di/dt Capability = 100 A/μs
- Shorted-Emitter, Center-Gate Design
- Low Switching Losses
- Low On-State Voltage at High Current Levels
- Low Thermal Resistance

Triacs are gate-controlled, full-wave silicon ac switches. They are designed to switch from an off-state to an on-state

for either polarity of applied voltage with positive or negative gate-triggering voltages.

**MAXIMUM RATINGS, Absolute-Maximum Values:**  
For Operation with Sinusoidal Supply Voltage at Frequencies up to 50/60 Hz and with Resistive or Inductive Load.

	2N5441	2N5442	2N5443	T6400N
	2N5444	2N5445	2N5446	T6410N
	T6420B	T6420D	T6420M	T6420N

- **REPETITIVE PEAK OFF-STATE VOLTAGE:**<sup>•</sup>  
Gate open,  $T_J = -65$  to  $110^\circ\text{C}$  . . . . .
- RMS ON-STATE CURRENT (Conduction angle =  $360^\circ$ ):**  
Case temperature
  - $T_C = 70^\circ\text{C}$  (Press-fit types) . . . . .
  - $= 65^\circ\text{C}$  (Stud types) . . . . .
  - $= 60^\circ\text{C}$  (Isolated-stud types) . . . . .
 For other conditions . . . . .
- PEAK SURGE (NON-REPETITIVE) ON-STATE CURRENT:**  
For one cycle of applied principal voltage
  - 60 Hz (sinusoidal) . . . . .
  - 50 Hz (sinusoidal) . . . . .
 For more than one cycle of applied principal voltage . . . . .
- RATE OF CHANGE OF ON-STATE CURRENT:**  
 $V_{DM} = V_{DROM}$ ,  $I_{GT} = 200\text{ mA}$ ,  $t_r = 0.1\ \mu\text{s}$  (See Fig. 13) . . . . .
- FUSING CURRENT (for Triac Protection):**  
 $T_J = -65$  to  $110^\circ\text{C}$ ,  $t = 1.25$  to  $10\text{ ms}$  . . . . .
- **PEAK GATE-TRIGGER CURRENT:**<sup>■</sup>  
For  $1\ \mu\text{s}$  max., See Fig. 7 . . . . .
- **GATE POWER DISSIPATION:**  
PEAK (For  $10\ \mu\text{s}$  max.,  $I_{GTM} \leq 4\text{ A}$ , See Fig. 7) . . . . .  
AVERAGE . . . . .
- **TEMPERATURE RANGE:**<sup>▲</sup>  
Storage . . . . .  
Operating (Case) . . . . .
- **TERMINAL TEMPERATURE (During soldering):**  
For  $10\text{ s}$  max. (terminals and case) . . . . .

	2N5441	2N5442	2N5443	T6400N	
$V_{DROM}$	200	400	600	800	V
$I_T(RMS)$	_____				A
	_____				A
	_____				A
	See Fig. 3				
$I_{TSM}$	_____				A
	_____				A
	See Fig. 4				
di/dt	_____				A/μs
$I^2_t$	_____				A <sup>2</sup> s
$I_{GTM}$	_____				A
	_____				A
$P_{GM}$	_____				W
$P_{G(AV)}$	_____				W
$T_{stg}$	_____				°C
$T_C$	_____				°C
$T_T$	_____				°C
	225				°C

• In accordance with JEDEC registration data format (JS-14, ROP2) filed for the JEDEC (2N-Series) types.    ■ For either polarity of gate voltage ( $V_G$ ) with reference to main terminal  
 • For either polarity of main terminal 2 voltage ( $V_{MT2}$ ) with reference to main terminal 1.    ▲ For temperature measurement reference point, see Dimensional Outline.

**ELECTRICAL CHARACTERISTICS**

At Maximum Ratings Unless Otherwise Specified and at Indicated Case Temperature ( $T_C$ )

CHARACTERISTIC	SYMBOL	LIMITS			UNITS
		FOR ALL TYPES UNLESS OTHERWISE SPECIFIED			
		MIN.	TYP.	MAX.	
Peak Off-State Current: <sup>♠</sup> Gate open, $T_J = 110^\circ\text{C}$ , $V_{DROM} = \text{Max. rated value}$ . . . . .	$I_{DROM}$	–	0.2	4*	mA
Maximum On-State Voltage: <sup>♠</sup> For $i_T = 100\text{ A (peak)}$ , $T_C = 25^\circ\text{C}$ . . . . . For $i_T = 56\text{ A (peak)}$ , $T_C = 25^\circ\text{C}$ . . . . .	$V_{TM}$	– –	1.7 1.5	2 1.85*	V
DC Holding Current: <sup>♠</sup> Gate open, Initial principal current = 500 mA (dc), $v_D = 12\text{V}$ : $T_C = 25^\circ\text{C}$ . . . . . $T_C = -65^\circ\text{C}$ . . . . . For other case temperatures . . . . .	$I_{HO}$	– –	25 –	60 100*	mA
See Fig. 6					
Critical Rate of Rise of Commutation Voltage: <sup>♠</sup> For $v_D = V_{DROM}$ , $I_T(\text{RMS}) = 40\text{ A}$ , commutating $di/dt = 22\text{ A/ms}$ , gate unenergized, (See Fig. 14): $T_C = 70^\circ\text{C}$ (Press-fit types) . . . . . $T_C = 65^\circ\text{C}$ (Stud types) . . . . . $T_C = 60^\circ\text{C}$ (Isolated-stud types) . . . . .	$dv/dt$	5* 5* 5	30 30 30	– – –	$\text{V}/\mu\text{s}$
Critical Rate of Rise of Off-State Voltage: <sup>♠</sup> For $v_D = V_{DROM}$ , exponential voltage rise, gate open, $T_C = 110^\circ\text{C}$ : 2N5441, 2N5444, T6420B, . . . . . 2N5442, 2N5445, T6420D, . . . . . 2N5443, 2N5446, T6420M . . . . . T6400N, T6410N, T6420N, . . . . .	$dv/dt$	50* 30* 20* 10	200 150 100 75	– – – –	$\text{V}/\mu\text{s}$
DC Gate-Trigger Current: <sup>♠♠</sup> For $v_D = 12\text{ V (dc)}$ $R_L = 30\ \Omega$ $T_C = 25^\circ\text{C}$ Mode $V_{MT2}$ $V_G$ $I^+$ positive positive $III^-$ negative negative $I^-$ positive negative $III^+$ negative positive  For $v_D = 12\text{ V (dc)}$ $R_L = 30\ \Omega$ $T_C = -65^\circ\text{C}$ Mode $V_{MT2}$ $V_G$ $I^+$ positive positive $III^-$ negative negative $I^-$ positive negative $III^+$ negative positive  For other case temperatures . . . . .	$I_{GT}$	– – – – – – – –	15 20 30 40 – – – –	50 50 80 80 125* 125* 240* 240*	mA
See Figs. 8 & 9					
DC Gate-Trigger Voltage: <sup>♠♠</sup> For $v_D = 12\text{ V (dc)}$ , $R_L = 30\ \Omega$ , $T_C = 25^\circ\text{C}$ . . . . . $T_C = -65^\circ\text{C}$ . . . . . For other case temperatures . . . . . For $v_D = V_{DROM}$ , $R_L = 125\ \Omega$ , $T_C = 110^\circ\text{C}$ . . . . .	$V_{GT}$	– – 0.2	1.35 1.8 –	2.5 3.4* –	V
See Fig. 10					
Gate-Controlled Turn-On Time: (Delay Time + Rise Time) For $v_D = V_{DROM}$ , $I_{GT} = 200\text{ mA}$ , $t_r = 0.1\ \mu\text{s}$ , $i_T = 60\text{ A (peak)}$ , $T_C = 25^\circ\text{C}$ (See Figs. 11 & 15) . . . . .	$t_{gt}$	–	1.7	3	$\mu\text{s}$
Thermal Resistance, Junction-to-Case: Steady-State Press-fit types . . . . . Stud types . . . . . Isolated-stud types . . . . . Transient (Press-fit & stud types) . . . . .	$R_{\theta JC}$	– – –	– – –	0.8* 0.9* 1	$^\circ\text{C}/\text{W}$
See Fig. 12					

\* In accordance with JEDEC registration data format (JS-14, RDF 2) filed for the JEDEC (2N-Series) types.  
<sup>♠</sup> For either polarity of main terminal 2 voltage ( $V_{MT2}$ ) with reference to main terminal 1.  
<sup>♠♠</sup> For either polarity of gate voltage ( $V_G$ ) with reference to main terminal 1.

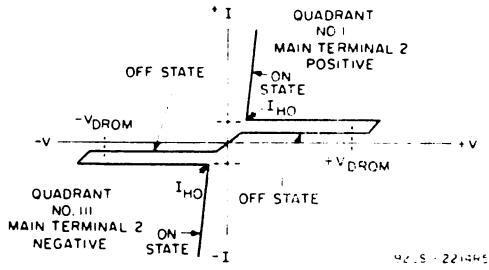


Fig.1—Principal voltage-current characteristic.

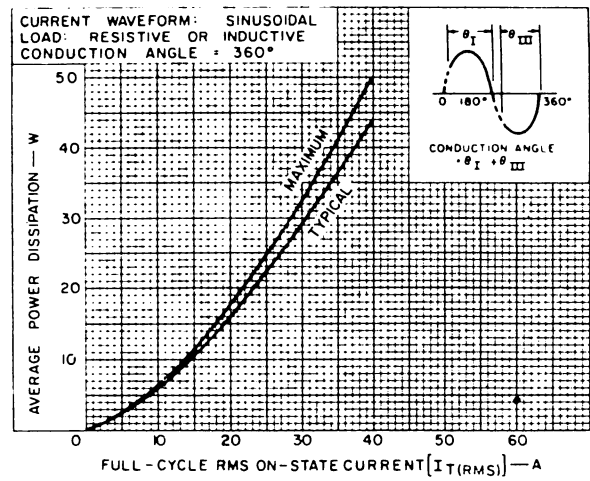


Fig.2—Power dissipation vs. on-state current.

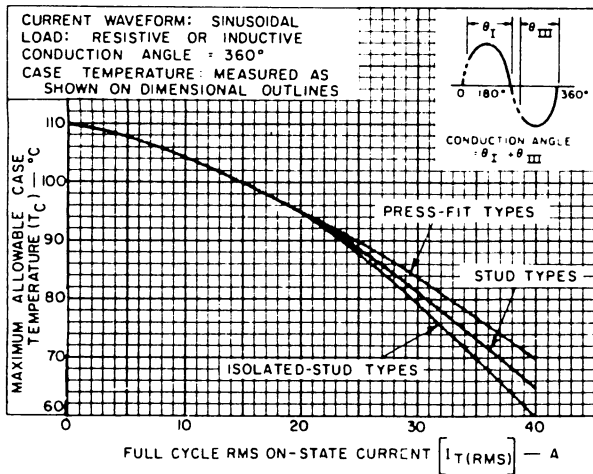


Fig.3—Maximum allowable case temperature vs. on-state current.

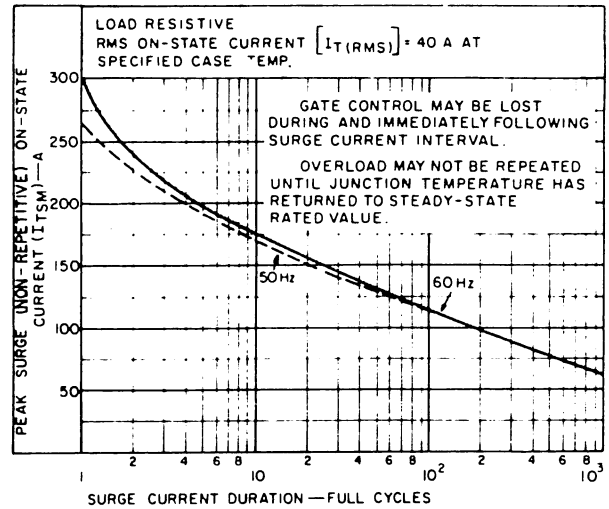


Fig.4—Peak surge on-state current vs. surge current duration.

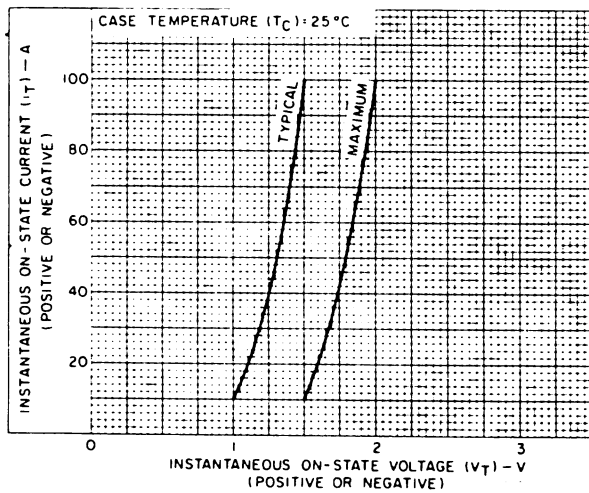


Fig.5—On-state current vs. on-state voltage.

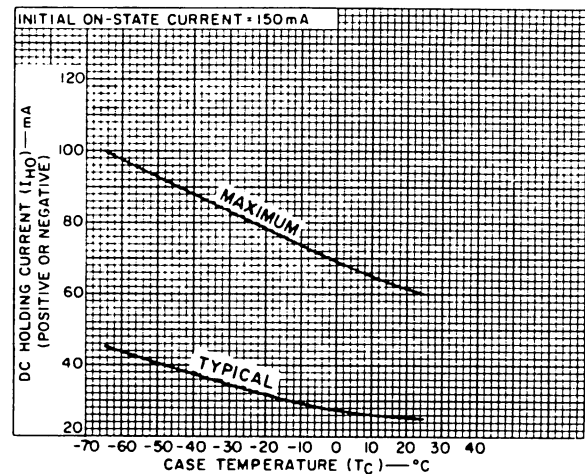


Fig.6—DC holding current vs. case temperature.

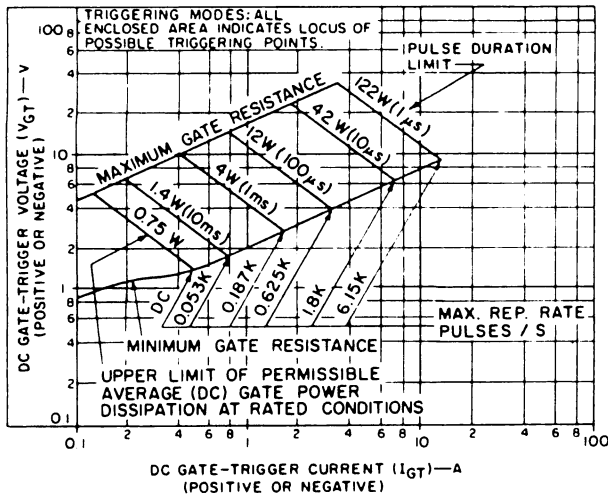


Fig. 7—Gate-trigger characteristics and limiting conditions for determination of permissible gate-trigger pulses.

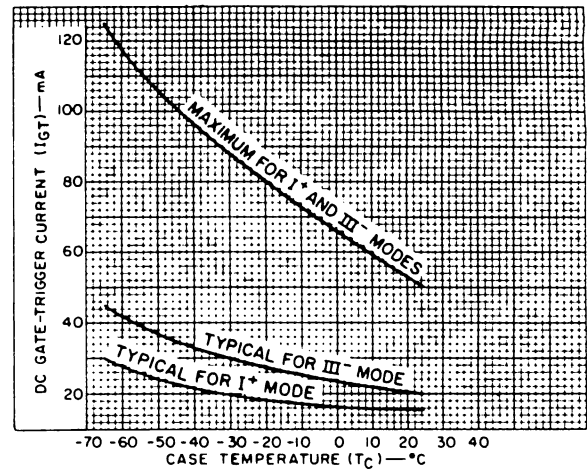


Fig. 8—DC gate-trigger current vs. case temperature ( $I^*$  &  $III^*$  modes).

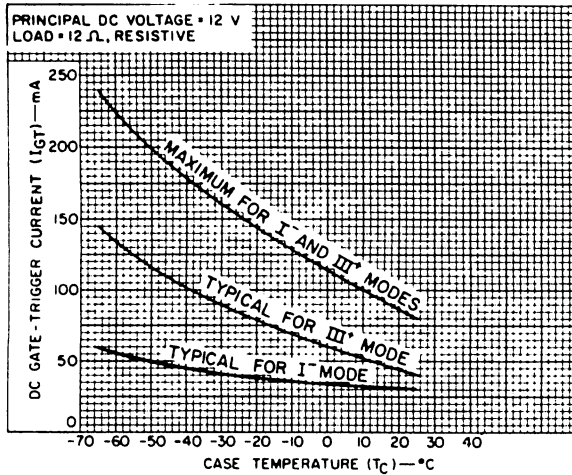


Fig. 9—DC gate-trigger current vs. case temperature ( $I^*$  &  $III^*$  modes).

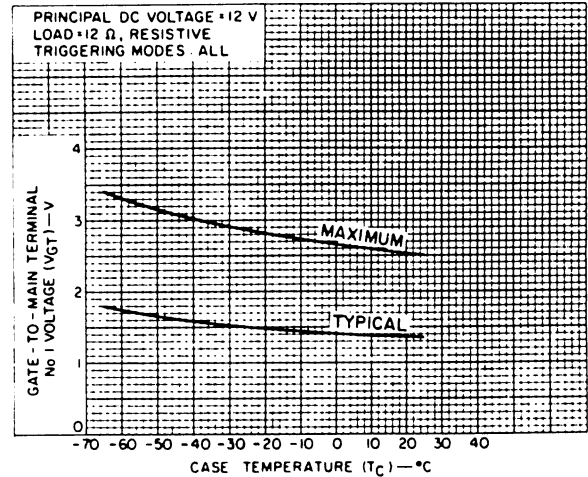


Fig. 10—DC gate-trigger voltage vs. case temperature.

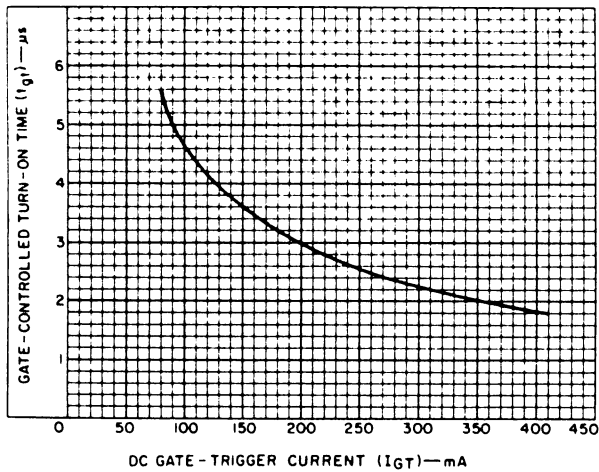


Fig. 11—Turn-on time vs. gate-trigger current.

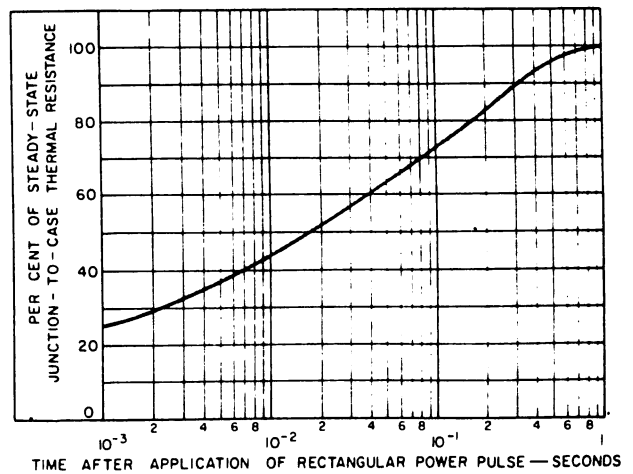


Fig. 12—Transient junction-to-case thermal resistance vs. time for press-fit and stud types.

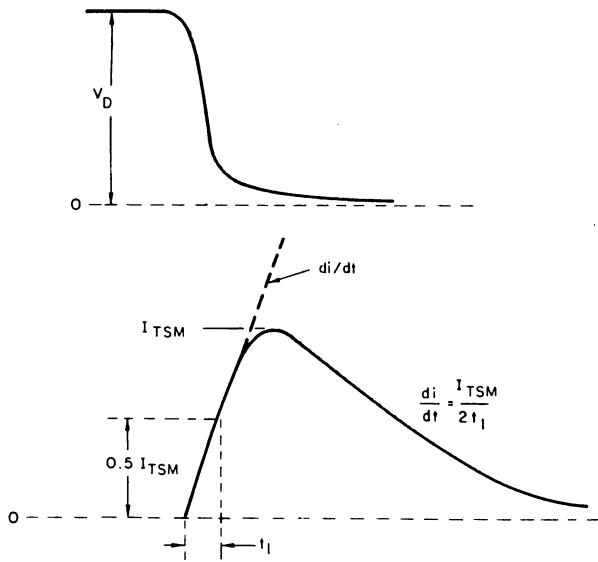


Fig. 13—Rate of change of on-state current with time (defining  $di/dt$ ).

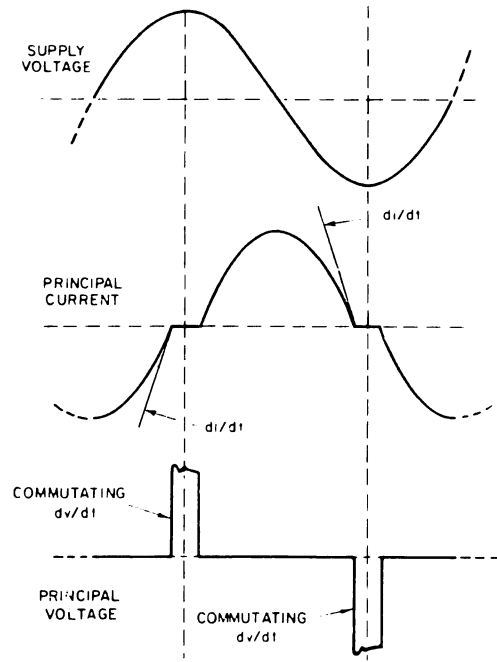


Fig. 14—Relationship between supply voltage and principal current (inductive load) showing reference points for definition of commutating voltage ( $dv/dt$ ).

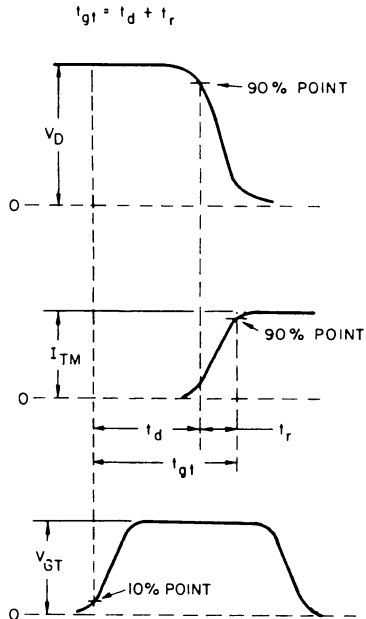


Fig. 15—Relationship between off-state voltage, on-state current, and gate-trigger voltage showing reference points for definition of turn-on time ( $t_{gt}$ ).

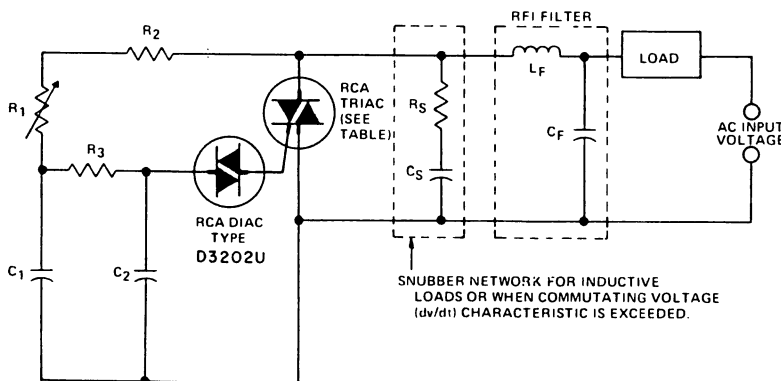
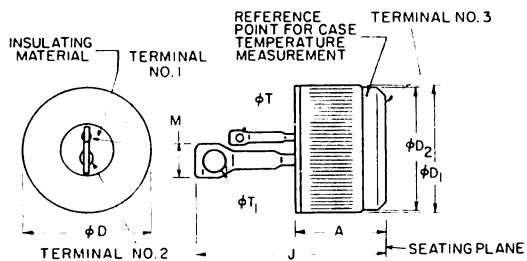


Fig. 16—Typical phase-control circuit for lamp dimming, heat control, and universal-motor speed control.

AC INPUT VOLTAGE	120V 60Hz	240V 60Hz	240V 50Hz	
C <sub>1</sub>	0.1μF 200V	0.1μF 400V	0.1μF 400V	
C <sub>2</sub>	0.1μF 100V	0.1μF 100V	0.1μF 100V	
R <sub>1</sub>	100KΩ 1/2W	200KΩ 1/2W	250KΩ 1W	
R <sub>2</sub>	2.2KΩ 1/2W	3.3KΩ 1/2W	3.3KΩ 1/2W	
R <sub>3</sub>	15KΩ 1/2W	15KΩ 1/2W	15KΩ 1/2W	
SNUBBER NETWORK FOR 40-A (RMS)* INDUCTIVE LOAD	C <sub>S</sub>	0.18- 0.22μF 200V	0.18- 0.22μF 400V	0.18- 0.22μF 400V
	R <sub>S</sub>	330- 390Ω 1/2W	330- 390Ω 1/2W	330- 390Ω 1/2W
RFI FILTER	C <sub>F</sub> *	0.1μF 200V	0.1μF 400V	0.1μF 400V
	L <sub>F</sub> *	100μH	200μH	200μH
RCA TRIACS	2N5441 T6420B	2N5442 T6420D	2N5442 2N5445 T6420D	

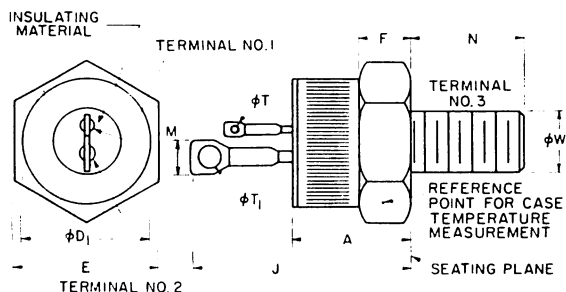
\* For other RMS current values refer to RCA Application Note AN-4745.  
\* Typical values for lamp dimming circuits.

**DIMENSIONAL OUTLINE FOR TYPES  
2N5441, 2N5442, 2N5443, T6400N  
PRESS-FIT**



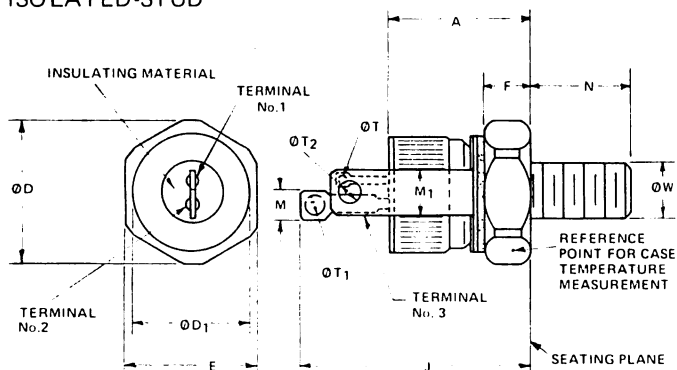
SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN.	MAX.	MIN.	MAX.	
A	—	0.380	—	9.65	
φD	0.501	0.510	12.73	12.95	
φD <sub>1</sub>	—	0.505	—	12.83	
φD <sub>2</sub>	0.465	0.475	11.81	12.07	
J	0.825	1.000	20.95	25.40	
M	0.215	0.225	5.46	5.71	
φT	0.058	0.068	1.47	1.73	
φT <sub>1</sub>	0.138	0.148	3.51	3.75	

**DIMENSIONAL OUTLINE FOR TYPES  
2N5444, 2N5445, 2N5446, T6410N  
STUD**



SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN.	MAX.	MIN.	MAX.	
A	0.330	0.505	8.4	12.8	
φD <sub>1</sub>	—	0.544	—	13.81	
E	0.544	0.562	13.82	14.28	
F	0.113	0.200	2.87	5.08	
J	0.950	1.100	24.13	27.94	
M	0.215	0.225	5.46	5.71	
N	0.422	0.453	10.72	11.50	
φT	0.058	0.068	1.47	1.73	
φT <sub>1</sub>	0.138	0.148	3.51	3.75	
φW	¼-28	UNF-2A	¼-28	UNF-2A	

**DIMENSIONAL OUTLINE FOR  
T6420 SERIES  
ISOLATED-STUD**



SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN.	MAX.	MIN.	MAX.	
A	—	0.673	—	17.09	
φD	0.604	0.614	15.34	15.59	
φD <sub>1</sub>	0.501	0.505	12.72	12.82	
E	0.551	0.557	13.99	14.14	
F	0.100	0.110	2.54	2.79	
J	—	1.298	—	32.96	
M	0.210	0.230	5.33	5.84	
M <sub>1</sub>	0.200	0.210	5.08	5.33	
N	0.422	0.452	10.72	11.48	
φT	0.058	0.068	1.47	1.73	
φT <sub>1</sub>	0.138	0.148	3.51	3.75	
φT <sub>2</sub>	0.138	0.148	3.51	3.75	
φW	¼-28	UNF-2A	¼-28	UNF-2A	

**TERMINAL CONNECTIONS**

- No. 1—Gate
- No. 2—Main Terminal 1
- Case, No. 3—Main Terminal 2

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