

To our customers,

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## Old Company Name in Catalogs and Other Documents

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Renesas Electronics website: <http://www.renesas.com>

April 1<sup>st</sup>, 2010  
Renesas Electronics Corporation

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# R1LV1616HBG-I Series

Wide Temperature Range Version  
16 M SRAM (1-Mword × 16-bit)

REJ03C0263-0100

Rev.1.00

Sep.21.2005

## Description

The R1LV1616HBG-I Series is 16-Mbit static RAM organized 1-Mword × 16-bit. R1LV1616HBG-I Series has realized higher density, higher performance and low power consumption by employing CMOS process technology (6-transistor memory cell). It offers low power standby power dissipation; therefore, it is suitable for battery backup systems. It is packaged in 48-ball plastic FBGA for high density surface mounting.

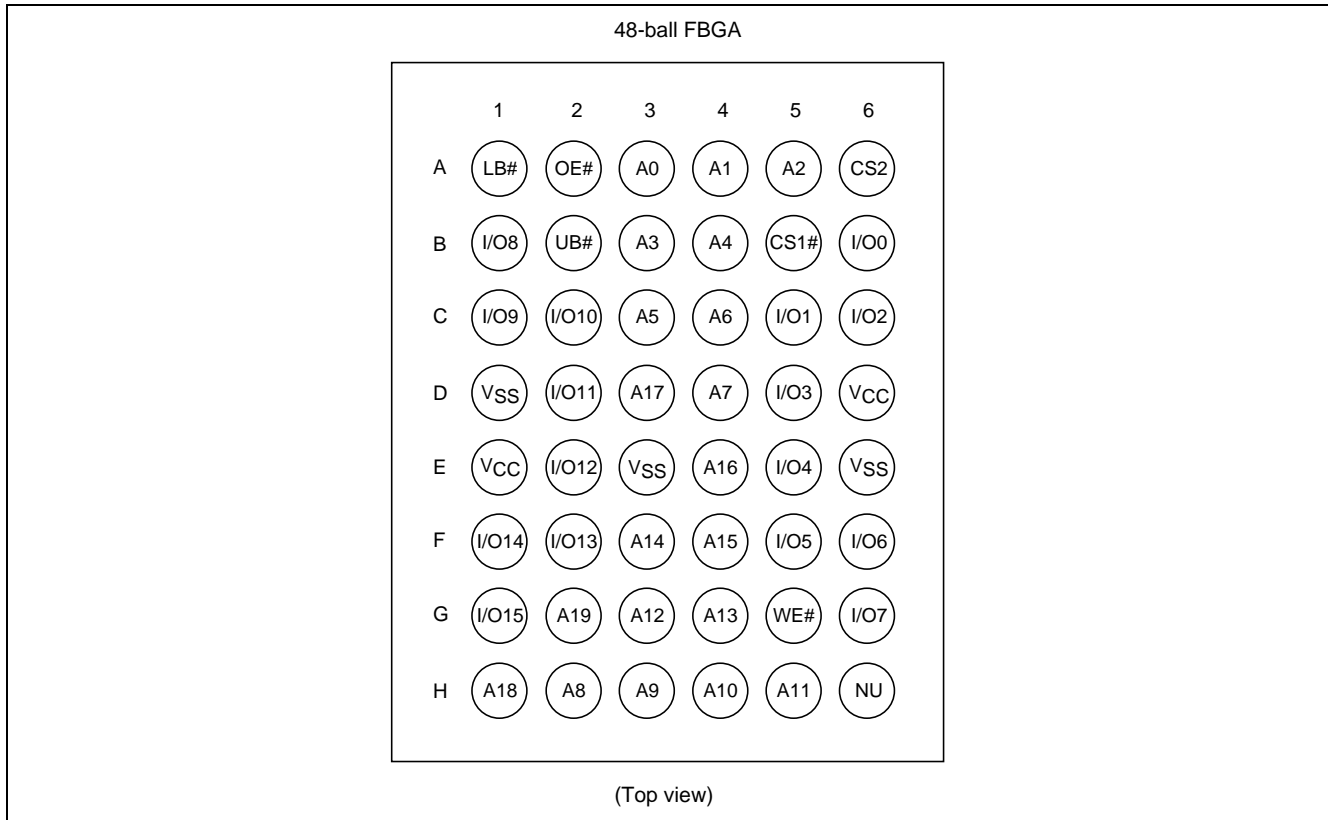
## Features

- Single 3.0 V supply: 2.7 V to 3.6 V
- Fast access time: 45/55 ns (max)
- Power dissipation:
  - Active: 9 mW/MHz (typ)
  - Standby: 1.5  $\mu$ W (typ)
- Completely static memory.
  - No clock or timing strobe required
- Equal access and cycle times
- Common data input and output.
  - Three state output
- Battery backup operation.
  - 2 chip selection for battery backup
- Temperature range: -40 to +85°C

## Ordering Information

Type No.	Access time	Package
R1LV1616HBG-4SI	45 ns	48-ball plastic FBGA with 0.75 mm ball pitch
R1LV1616HBG-5SI	55 ns	PTBG0048HF (48FHJ)

## Pin Arrangement

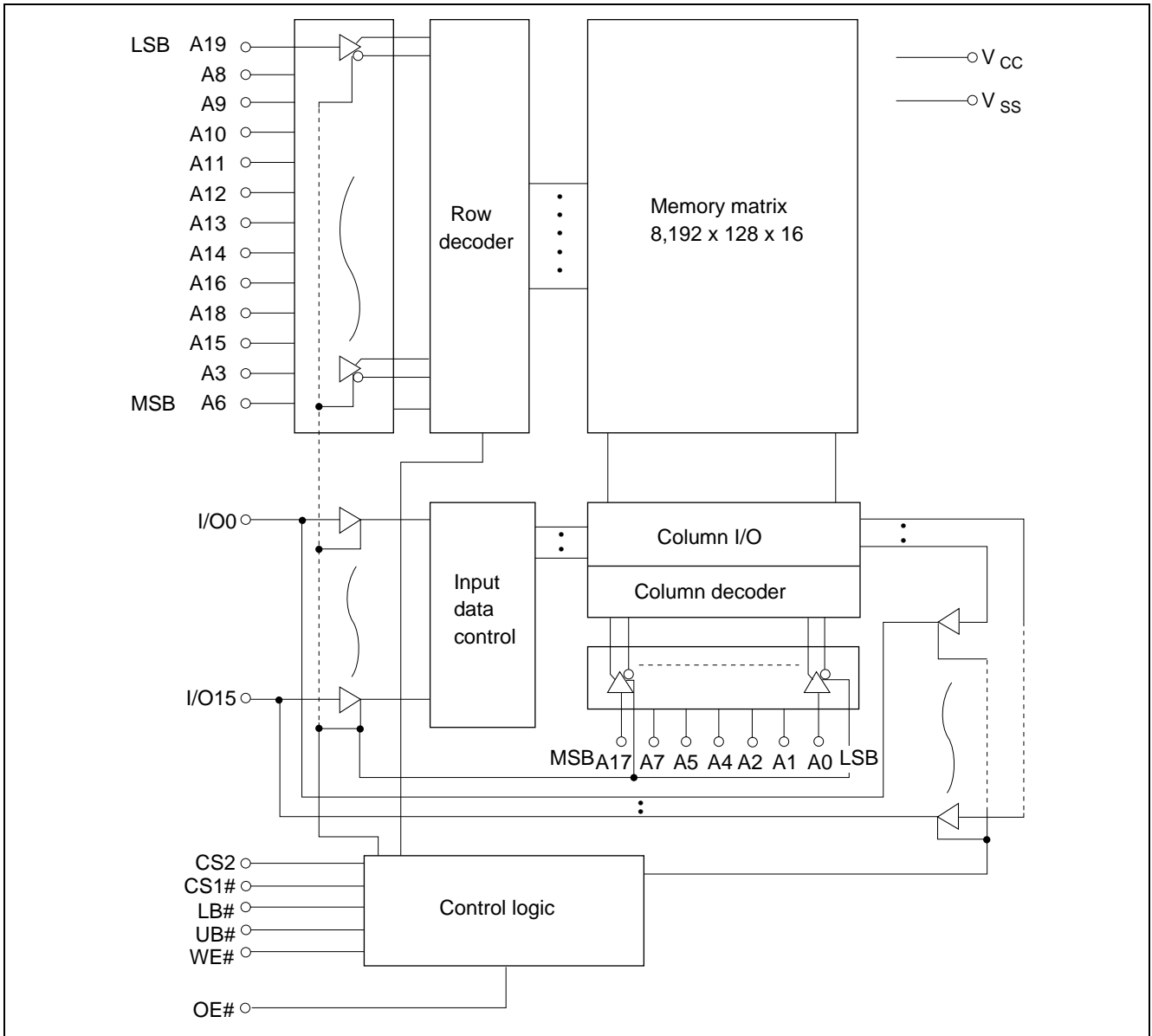


## Pin Description

Pin name	Function
A0 to A19	Address input
I/O0 to I/O15	Data input/output
CS1# ( $\overline{CS1}$ )	Chip select 1
CS2	Chip select 2
WE# ( $\overline{WE}$ )	Write enable
OE# ( $\overline{OE}$ )	Output enable
LB# ( $\overline{LB}$ )	Lower byte select
UB# ( $\overline{UB}$ )	Upper byte select
V <sub>CC</sub>	Power supply
V <sub>SS</sub>	Ground
NU* <sup>1</sup>	Not used (test mode pin)

Note: 1. This pin should be connected to a ground (V<sub>SS</sub>), or not be connected (open).

Block Diagram



## Operation Table

CS1#	CS2	WE#	OE#	UB#	LB#	I/O0 to I/O7	I/O8 to I/O15	Operation
H	×	×	×	×	×	High-Z	High-Z	Standby
×	L	×	×	×	×	High-Z	High-Z	Standby
×	×	×	×	H	H	High-Z	High-Z	Standby
L	H	H	L	L	L	Dout	Dout	Read
L	H	H	L	H	L	Dout	High-Z	Lower byte read
L	H	H	L	L	H	High-Z	Dout	Upper byte read
L	H	L	×	L	L	Din	Din	Write
L	H	L	×	H	L	Din	High-Z	Lower byte write
L	H	L	×	L	H	High-Z	Din	Upper byte write
L	H	H	H	×	×	High-Z	High-Z	Output disable

Note: H:  $V_{IH}$ , L:  $V_{IL}$ , ×:  $V_{IH}$  or  $V_{IL}$

## Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
Power supply voltage relative to $V_{SS}$	$V_{CC}$	-0.5 to +4.6	V
Terminal voltage on any pin relative to $V_{SS}$	$V_T$	-0.5* <sup>1</sup> to $V_{CC} + 0.3$ * <sup>2</sup>	V
Power dissipation	$P_T$	1.0	W
Storage temperature range	$T_{stg}$	-55 to +125	°C
Storage temperature range under bias	$T_{bias}$	-40 to +85	°C

Notes: 1.  $V_T$  min: -2.0 V for pulse half-width  $\leq$  10 ns.  
2. Maximum voltage is +4.6 V.

## DC Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit	Note
Supply voltage	$V_{CC}$	2.7	3.0	3.6	V	
	$V_{SS}$	0	0	0	V	
Input high voltage	$V_{IH}$	2.2	—	$V_{CC} + 0.3$	V	
Input low voltage	$V_{IL}$	-0.3	—	0.6	V	1
Ambient temperature range	$T_a$	-40	—	+85	°C	

Note: 1.  $V_{IL}$  min: -2.0 V for pulse half-width  $\leq$  10 ns.

## DC Characteristics

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions
Input leakage current	$ I_{LI} $	—	—	1	$\mu\text{A}$	$V_{in} = V_{SS}$ to $V_{CC}$
Output leakage current	$ I_{LO} $	—	—	1	$\mu\text{A}$	CS1# = $V_{IH}$ or CS2 = $V_{IL}$ or OE# = $V_{IH}$ or WE# = $V_{IL}$ or LB# = UB# = $V_{IH}$ , $V_{IO} = V_{SS}$ to $V_{CC}$
Operating current	$I_{CC}$	—	—	20	mA	CS1# = $V_{IL}$ , CS2 = $V_{IH}$ , Others = $V_{IH}/V_{IL}$ , $I_{IO} = 0$ mA
Average operating current	$I_{CC1}$ (READ)	—	$22^{*1}$	35	mA	Min. cycle, duty = 100%, $I_{IO} = 0$ mA, CS1# = $V_{IL}$ , CS2 = $V_{IH}$ , WE# = $V_{IH}$ , Others = $V_{IH}/V_{IL}$
	$I_{CC1}$	—	$30^{*1}$	50	mA	Min. cycle, duty = 100%, $I_{IO} = 0$ mA, CS1# = $V_{IL}$ , CS2 = $V_{IH}$ , Others = $V_{IH}/V_{IL}$
	$I_{CC2}$ (READ)	—	$3^{*1}$	8	mA	Cycle time = 70 ns, duty = 100%, $I_{IO} = 0$ mA, CS1# = $V_{IL}$ , CS2 = $V_{IH}$ , WE# = $V_{IH}$ , Others = $V_{IH}/V_{IL}$ Address increment scan or decrement scan
	$I_{CC2}$	—	$20^{*1}$	30	mA	Cycle time = 70 ns, duty = 100%, $I_{IO} = 0$ mA, CS1# = $V_{IL}$ , CS2 = $V_{IH}$ , Others = $V_{IH}/V_{IL}$ Address increment scan or decrement scan
	$I_{CC3}$	—	$3^{*1}$	8	mA	Cycle time = 1 $\mu\text{s}$ , duty = 100%, $I_{IO} = 0$ mA, CS1# $\leq 0.2$ V, CS2 $\geq V_{CC} - 0.2$ V $V_{IH} \geq V_{CC} - 0.2$ V, $V_{IL} \leq 0.2$ V
Standby current	$I_{SB}$	—	$0.1^{*1}$	0.5	mA	CS2 = $V_{IL}$
	$I_{SB1}$	—	$0.5^{*1}$	8	$\mu\text{A}$	$0 \text{ V} \leq V_{in}$ (1) $0 \text{ V} \leq \text{CS2} \leq 0.2 \text{ V}$ or (2) CS1# $\geq V_{CC} - 0.2 \text{ V}$ , CS2 $\geq V_{CC} - 0.2 \text{ V}$ or (3) LB# = UB# $\geq V_{CC} - 0.2 \text{ V}$ , CS2 $\geq V_{CC} - 0.2 \text{ V}$ , CS1# $\leq 0.2 \text{ V}$ Average value
Output high voltage	$V_{OH}$	2.4	—	—	V	$I_{OH} = -1$ mA
	$V_{OH}$	$V_{CC} - 0.2$	—	—	V	$I_{OH} = -100$ $\mu\text{A}$
Output low voltage	$V_{OL}$	—	—	0.4	V	$I_{OL} = 2$ mA
	$V_{OL}$	—	—	0.2	V	$I_{OL} = 100$ $\mu\text{A}$

Notes: 1. Typical values are at  $V_{CC} = 3.0$  V,  $T_a = +25^\circ\text{C}$  and not guaranteed.

## Capacitance

(Ta = +25°C, f = 1.0 MHz)

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions	Note
Input capacitance	C <sub>in</sub>	—	—	8	pF	V <sub>in</sub> = 0 V	1
Input/output capacitance	C <sub>I/O</sub>	—	—	10	pF	V <sub>I/O</sub> = 0 V	1

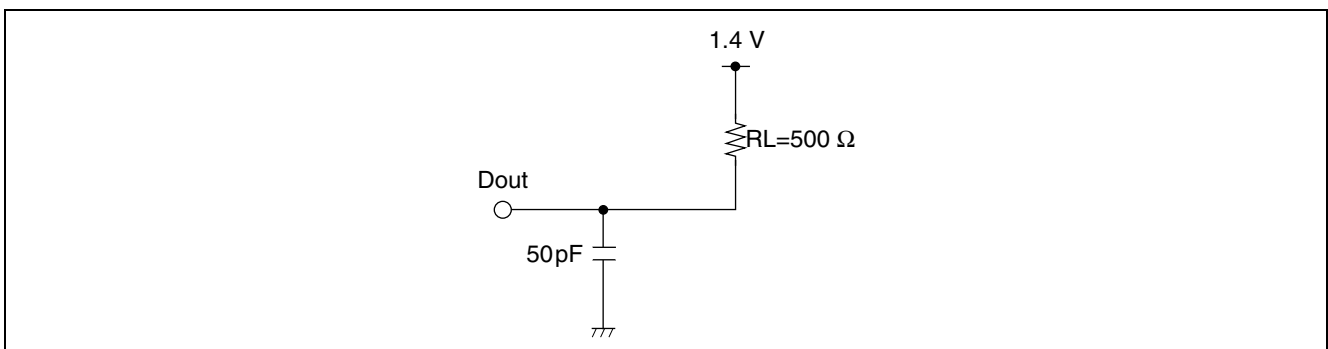
Note: 1. This parameter is sampled and not 100% tested.

## AC Characteristics

(Ta = -40 to +85°C, V<sub>CC</sub> = 2.7 V to 3.6 V)

### Test Conditions

- Input pulse levels: V<sub>IL</sub> = 0.4 V, V<sub>IH</sub> = 2.4 V
- Input rise and fall time: 5 ns
- Input and output timing reference levels: 1.4 V
- Output load: See figures (Including scope and jig)





## Read Cycle

Parameter	Symbol	R1LV1616HBG-I				Unit	Notes
		-4SI		-5SI			
		Min	Max	Min	Max		
Read cycle time	$t_{RC}$	45	—	55	—	ns	
Address access time	$t_{AA}$	—	45	—	55	ns	
Chip select access time	$t_{ACS1}$	—	45	—	55	ns	
	$t_{ACS2}$	—	45	—	55	ns	
Output enable to output valid	$t_{OE}$	—	30	—	35	ns	
Output hold from address change	$t_{OH}$	10	—	10	—	ns	
LB#, UB# access time	$t_{BA}$	—	45	—	55	ns	
Chip select to output in low-Z	$t_{CLZ1}$	10	—	10	—	ns	2, 3
	$t_{CLZ2}$	10	—	10	—	ns	2, 3
LB#, UB# enable to low-Z	$t_{BLZ}$	5	—	5	—	ns	2, 3
Output enable to output in low-Z	$t_{OLZ}$	5	—	5	—	ns	2, 3
Chip deselect to output in high-Z	$t_{CHZ1}$	0	20	0	20	ns	1, 2, 3
	$t_{CHZ2}$	0	20	0	20	ns	1, 2, 3
LB#, UB# disable to high-Z	$t_{BHZ}$	0	15	0	20	ns	1, 2, 3
Output disable to output in high-Z	$t_{OHZ}$	0	15	0	20	ns	1, 2, 3

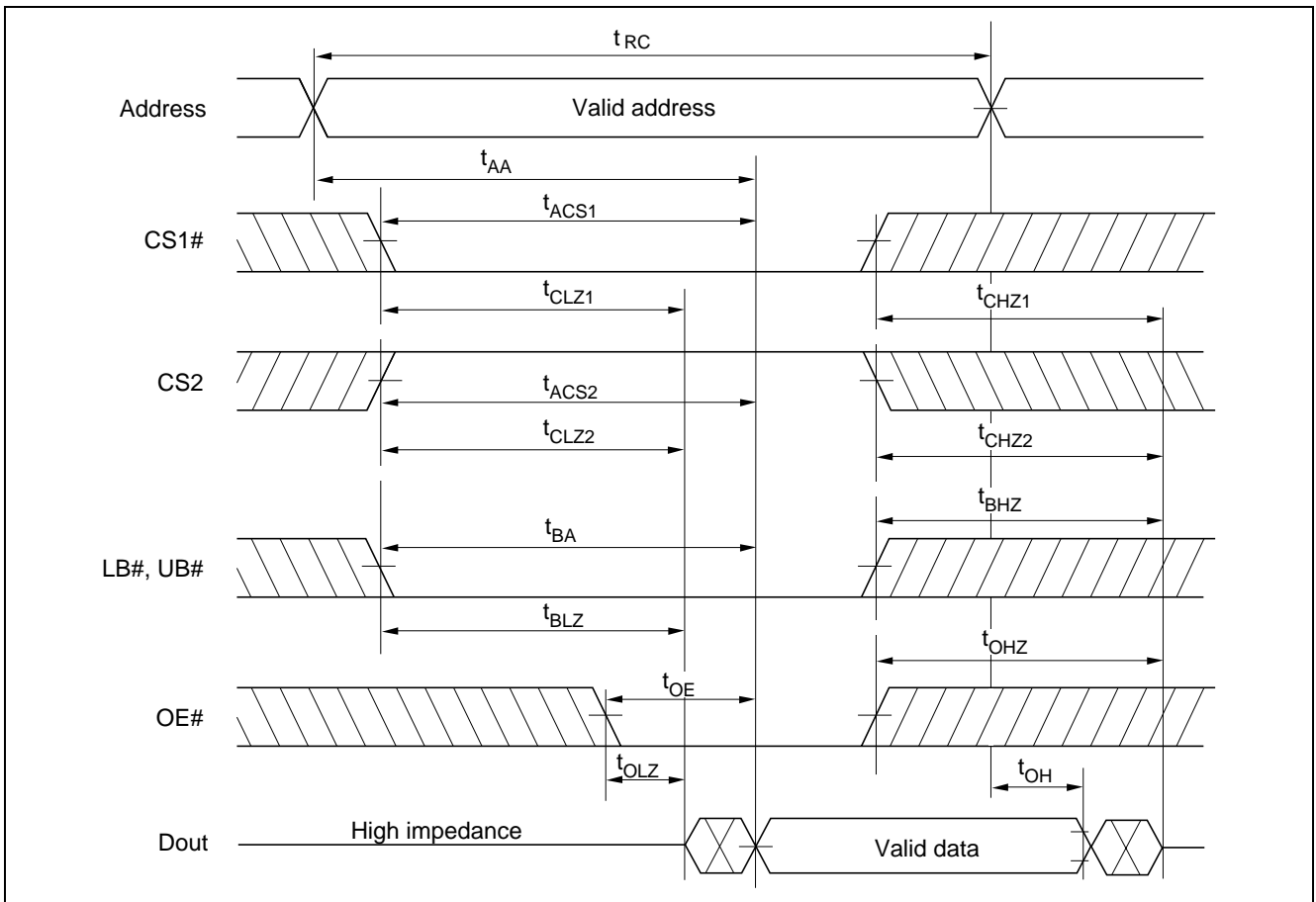
## Write Cycle

Parameter	Symbol	R1LV1616HBG-I				Unit	Notes
		-4SI		-5SI			
		Min	Max	Min	Max		
Write cycle time	$t_{WC}$	45	—	55	—	ns	
Address valid to end of write	$t_{AW}$	45	—	50	—	ns	
Chip selection to end of write	$t_{CW}$	45	—	50	—	ns	5
Write pulse width	$t_{WP}$	35	—	40	—	ns	4
LB#, UB# valid to end of write	$t_{BW}$	45	—	50	—	ns	
Address setup time	$t_{AS}$	0	—	0	—	ns	6
Write recovery time	$t_{WR}$	0	—	0	—	ns	7
Data to write time overlap	$t_{DW}$	25	—	25	—	ns	
Data hold from write time	$t_{DH}$	0	—	0	—	ns	
Output active from end of write	$t_{OW}$	5	—	5	—	ns	2
Output disable to output in high-Z	$t_{OHZ}$	0	15	0	20	ns	1, 2
Write to output in high-Z	$t_{WHZ}$	0	15	0	20	ns	1, 2

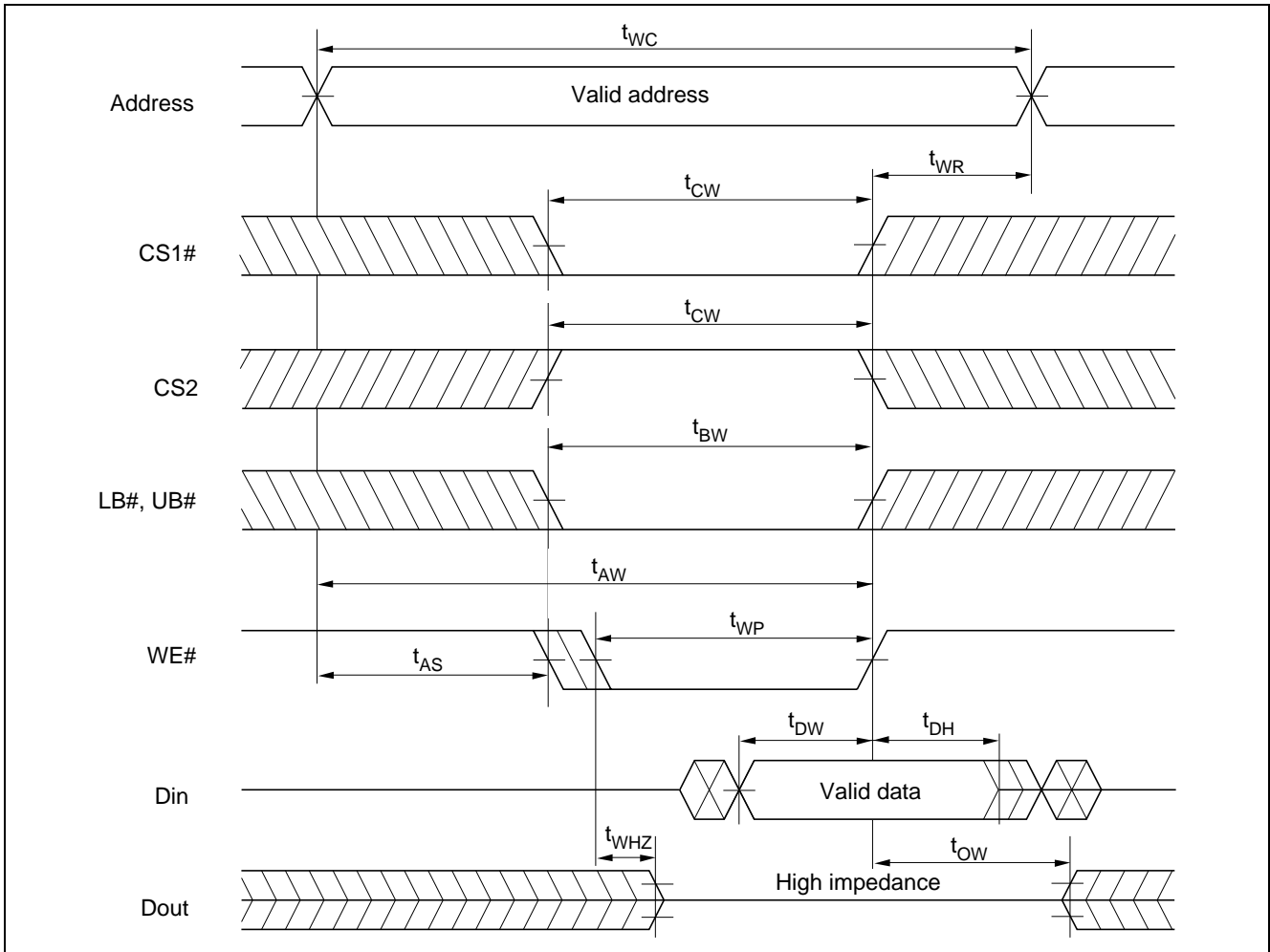
- Notes:
- $t_{CHZ}$ ,  $t_{OHZ}$ ,  $t_{WHZ}$  and  $t_{BHZ}$  are defined as the time at which the outputs achieve the open circuit conditions and are not referred to output voltage levels.
  - This parameter is sampled and not 100% tested.
  - At any given temperature and voltage condition,  $t_{HZ}$  max is less than  $t_{LZ}$  min both for a given device and from device to device.
  - A write occurs during the overlap of a low CS1#, a high CS2, a low WE# and a low LB# or a low UB#. A write begins at the latest transition among CS1# going low, CS2 going high, WE# going low and LB# going low or UB# going low. A write ends at the earliest transition among CS1# going high, CS2 going low, WE# going high and LB# going high or UB# going high.  $t_{WP}$  is measured from the beginning of write to the end of write.
  - $t_{CW}$  is measured from the later of CS1# going low or CS2 going high to the end of write.
  - $t_{AS}$  is measured from the address valid to the beginning of write.
  - $t_{WR}$  is measured from the earliest of CS1# or WE# going high or CS2 going low to the end of write cycle.

## Timing Waveform

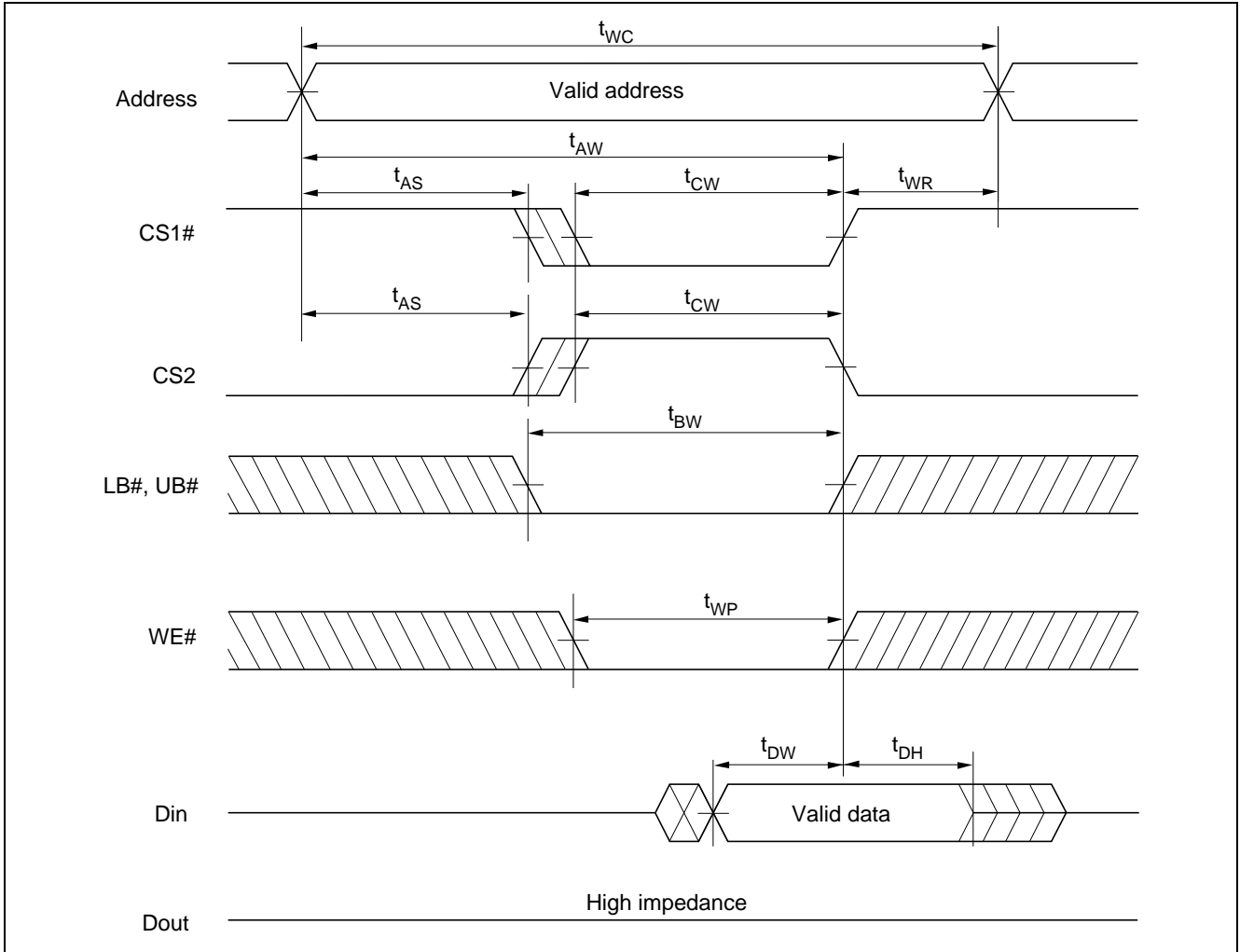
### Read Cycle



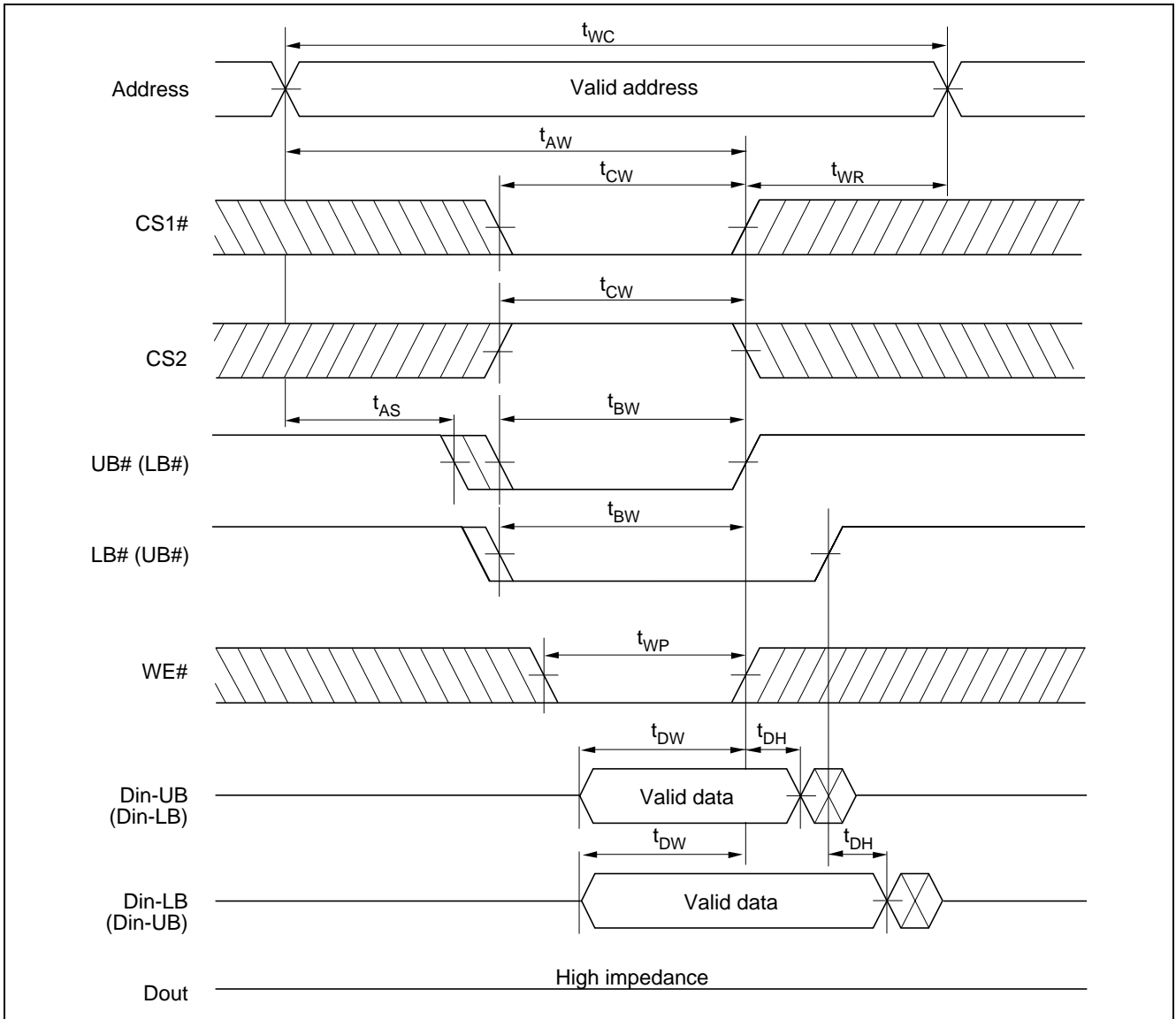
Write Cycle (1) (WE# Clock)



Write Cycle (2) (CS1#, CS2 Clock, OE# = V<sub>IH</sub>)



Write Cycle (3) (LB#, UB# Clock, OE# = V<sub>IH</sub>)



Low  $V_{CC}$  Data Retention Characteristics

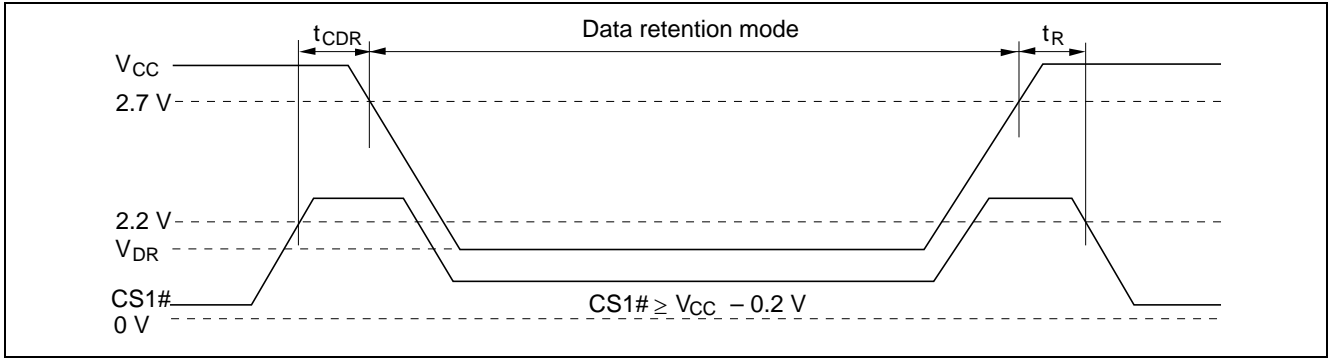
(Ta = -40 to +85°C)

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions*2
$V_{CC}$ for data retention	$V_{DR}$	1.5	—	3.6	V	$V_{in} \geq 0$ V (1) $0$ V $\leq$ CS2 $\leq$ 0.2 V or (2) CS2 $\geq$ $V_{CC} - 0.2$ V, CS1# $\geq$ $V_{CC} - 0.2$ V or (3) LB# = UB# $\geq$ $V_{CC} - 0.2$ V, CS2 $\geq$ $V_{CC} - 0.2$ V, CS1# $\leq$ 0.2 V
Data retention current	$I_{CCDR}$	—	0.5*1	8	$\mu$ A	$V_{CC} = 3.0$ V, $V_{in} \geq 0$ V (1) $0$ V $\leq$ CS2 $\leq$ 0.2 V or (2) CS2 $\geq$ $V_{CC} - 0.2$ V, CS1# $\geq$ $V_{CC} - 0.2$ V or (3) LB# = UB# $\geq$ $V_{CC} - 0.2$ V, CS2 $\geq$ $V_{CC} - 0.2$ V, CS1# $\leq$ 0.2 V Average value
Chip deselect to data retention time	$t_{CDR}$	0	—	—	ns	See retention waveforms
Operation recovery time	$t_R$	5	—	—	ms	

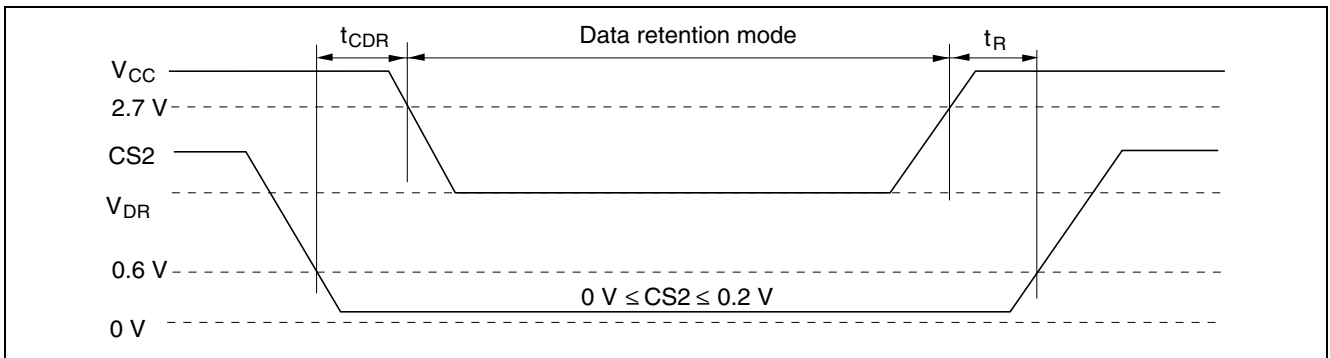
Notes: 1. Typical values are at  $V_{CC} = 3.0$  V, Ta = +25°C and not guaranteed.

2. CS2 controls address buffer, WE# buffer, CS1# buffer, OE# buffer, LB#, UB# buffer and Din buffer. If CS2 controls data retention mode,  $V_{in}$  levels (address, WE#, OE#, CS1#, LB#, UB#, I/O) can be in the high impedance state. If CS1# controls data retention mode, CS2 must be CS2  $\geq$   $V_{CC} - 0.2$  V or  $0$  V  $\leq$  CS2  $\leq$  0.2 V. The other input levels (address, WE#, OE#, LB#, UB#, I/O) can be in the high impedance state.

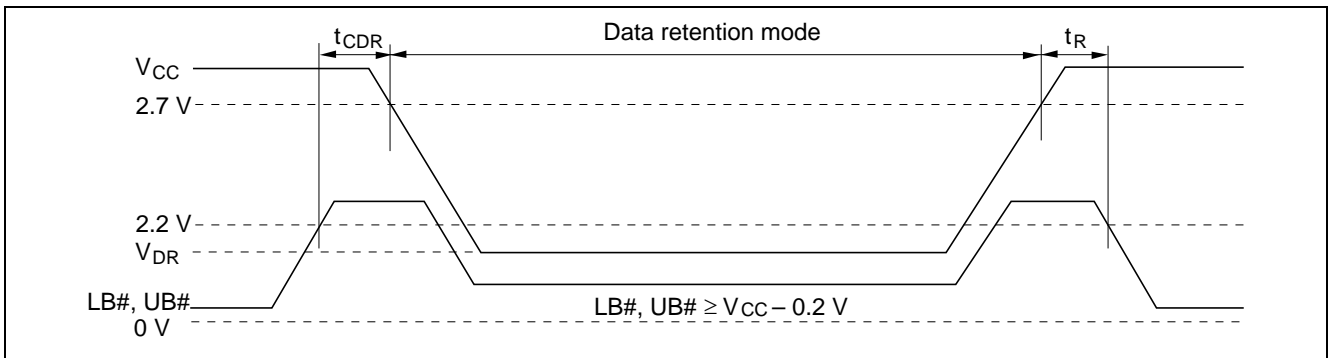
Low  $V_{CC}$  Data Retention Timing Waveform (1) (CS1# Controlled)



Low  $V_{CC}$  Data Retention Timing Waveform (2) (CS2 Controlled)



Low  $V_{CC}$  Data Retention Timing Waveform (3) (LB#, UB# Controlled)



**Revision History****R1LV1616HBG-I Series Data Sheet**

Rev.	Date	Contents of Modification	
		Page	Description
0.01	Apr. 29. 2005	—	Initial issue
1.00	Sep. 21. 2005	—	Deletion of Preliminary



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Tel: <44> (1628) 585-100, Fax: <44> (1628) 585-900

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#### **Renesas Technology Taiwan Co., Ltd.**

10th Floor, No.99, Fushing North Road, Taipei, Taiwan  
Tel: <886> (2) 2715-2888, Fax: <886> (2) 2713-2999

#### **Renesas Technology (Shanghai) Co., Ltd.**

Unit2607 Ruijing Building, No.205 Maoming Road (S), Shanghai 200020, China  
Tel: <86> (21) 6472-1001, Fax: <86> (21) 6415-2952

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Tel: <65> 6213-0200, Fax: <65> 6278-8001

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Kukje Center Bldg. 18th Fl., 191, 2-ka, Hangang-ro, Yongsan-ku, Seoul 140-702, Korea  
Tel: <82> 2-796-3115, Fax: <82> 2-796-2145

#### **Renesas Technology Malaysia Sdn. Bhd.**

Unit 906, Block B, Menara Amcorp, Amcorp Trade Centre, No.18, Jalan Persiaran Barat, 46050 Petaling Jaya, Selangor Darul Ehsan, Malaysia  
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