

# R1LV5256E Series

256Kb Advanced LPSRAM (32k word x 8bit)

R10DS0068EJ0100  
Rev.1.00  
2011.04.13

## Description

The R1LV5256E Series is a family of low voltage 256-Kbit static RAMs organized as 32,768-word by 8-bit, fabricated by Renesas's high-performance 0.15um CMOS and TFT technologies. The R1LV5256E Series has realized higher density, higher performance and low power consumption. The R1LV5256E Series is suitable for memory applications where a simple interfacing, battery operating and battery backup are the important design objectives. It has been packaged in 28-pin SOP and 28-pin TSOP.

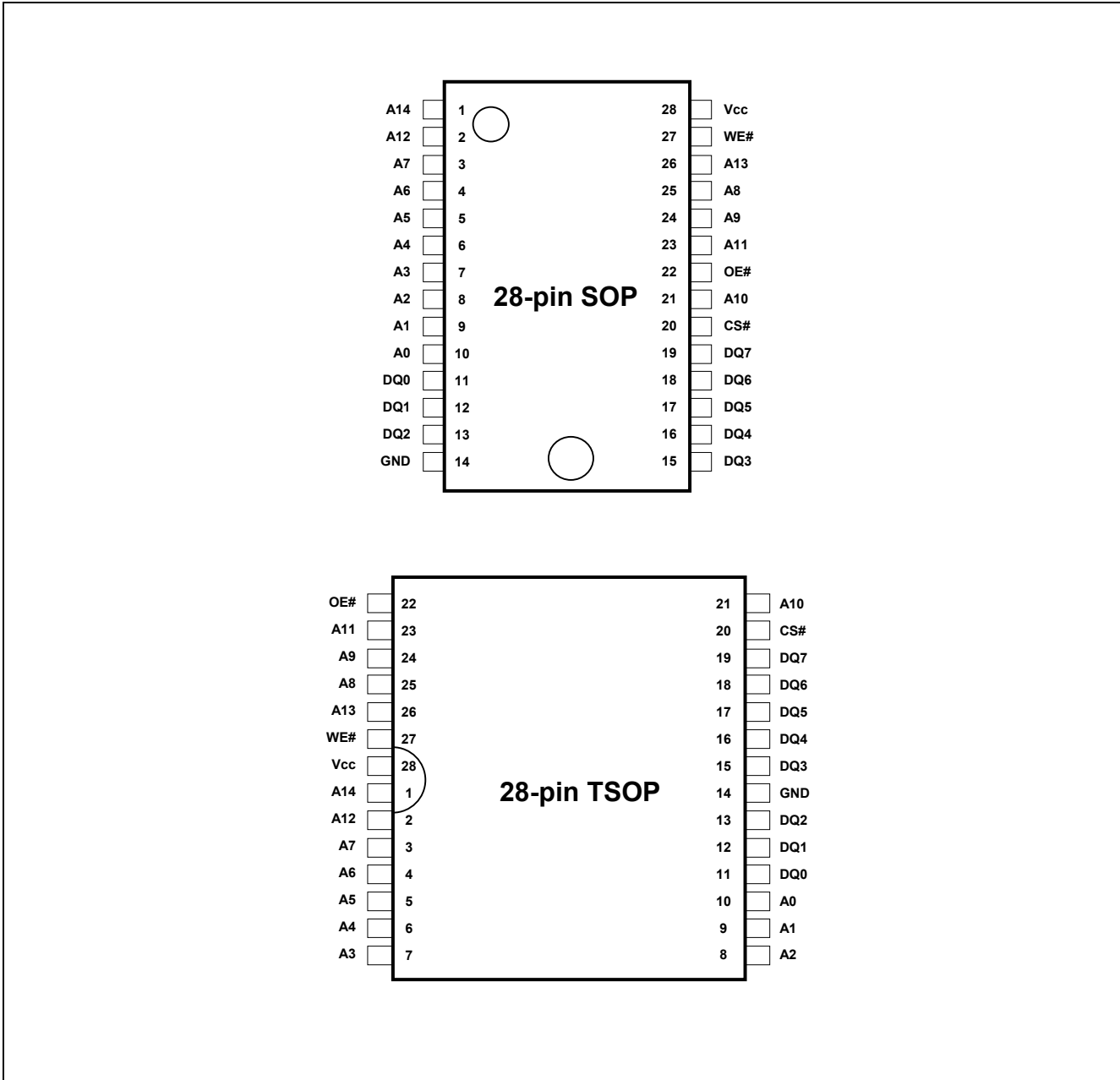
## Features

- Single 2.7~3.6V power supply
- Small stand-by current: 1μA (3.0V, typical)
- No clocks, No refresh
- All inputs and outputs are TTL compatible.
- Easy memory expansion by CS#
- Common Data I/O
- Three-state outputs: OR-tie Capability
- OE# prevents data contention on the I/O bus

## Ordering Information

| Orderable Part Name | Access time | Temperature Range | Package   | Shipping Container | Quantity   |
|---------------------|-------------|-------------------|---|--------------------|--|
| R1LV5256ESP-5SR#B0  | 55 ns       | 0 ~ +70°C         | 450-mil 28-pin plastic SOP                        | Tube               | Max. 30pcs/Tube<br>Max. 300pcs/Inner Bag<br>Max. 1200pcs/Inner Box |
| R1LV5256ESP-5SI#B0  |             | -40 ~ +85°C       |   |                    |  |
| R1LV5256ESP-7SR#B0  | 70 ns       | 0 ~ +70°C         |   |                    |  |
| R1LV5256ESP-7SI#B0  |             | -40 ~ +85°C       |   |                    |  |
| R1LV5256ESP-5SR#S0  | 55 ns       | 0 ~ +70°C         | PRSP0028DB-B (28P2W-C)                            | Embossed tape      | 1000pcs/Reel   |
| R1LV5256ESP-5SI#S0  |             | -40 ~ +85°C       |   |                    |  |
| R1LV5256ESP-7SR#S0  | 70 ns       | 0 ~ +70°C         |   |                    |  |
| R1LV5256ESP-7SI#S0  |             | -40 ~ +85°C       |   |                    |  |
| R1LV5256ESA-5SR#B0  | 55 ns       | 0 ~ +70°C         | 8mm×13.4mm 28-pin plastic TSOP (normal-bend type) | Tray               | Max. 234pcs/Tray<br>Max. 1872pcs/Inner Box                         |
| R1LV5256ESA-5SI#B0  |             | -40 ~ +85°C       |   |                    |  |
| R1LV5256ESA-7SR#B0  | 70 ns       | 0 ~ +70°C         |   |                    |  |
| R1LV5256ESA-7SI#B0  |             | -40 ~ +85°C       |   |                    |  |
| R1LV5256ESA-5SR#S0  | 55 ns       | 0 ~ +70°C         | PTSA0028ZA-A (28P2C-A)                            | Embossed tape      | 1000pcs/Reel   |
| R1LV5256ESA-5SI#S0  |             | -40 ~ +85°C       |   |                    |  |
| R1LV5256ESA-7SR#S0  | 70 ns       | 0 ~ +70°C         |   |                    |  |
| R1LV5256ESA-7SI#S0  |             | -40 ~ +85°C       |   |                    |  |

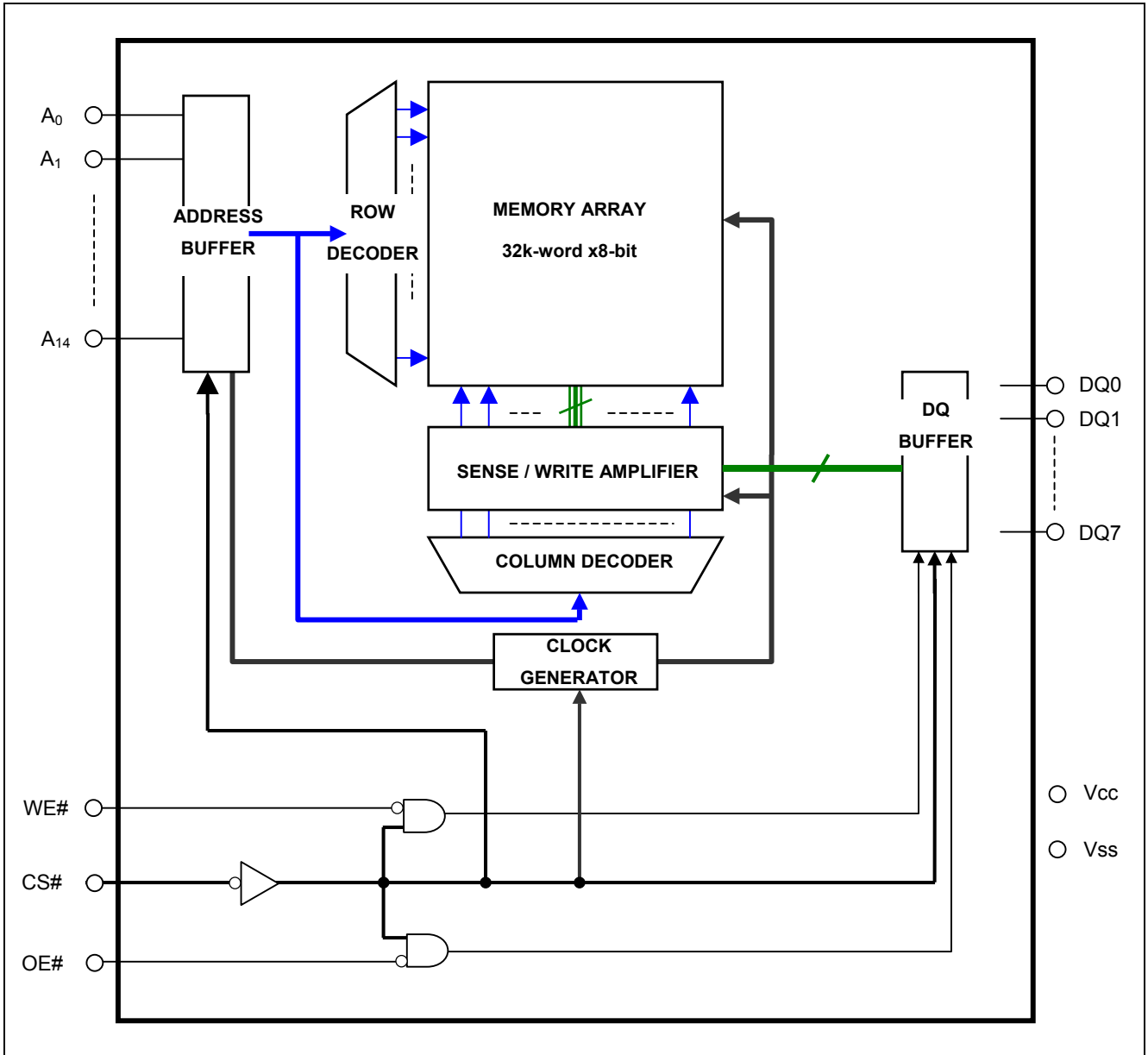
Pin Arrangement



Pin Description

| Pin name   | Function          |
|------------|-------------------|
| Vcc        | Power supply      |
| Vss        | Ground            |
| A0 to A14  | Address input     |
| DQ0 to DQ7 | Data input/output |
| CS#        | Chip select       |
| WE#        | Write enable      |
| OE#        | Output enable     |

### Block Diagram



## Operation Table

| CS# | WE# | OE# | DQ0~7  | Operation      |
|-----|-----|-----|--------|----------------|
| H   | X   | X   | High-Z | Stand-by       |
| L   | L   | X   | Din    | Write          |
| L   | H   | L   | Dout   | Read           |
| L   | H   | H   | High-Z | Output disable |

Note 1. H:  $V_{IH}$  L:  $V_{IL}$  X:  $V_{IH}$  or  $V_{IL}$

## Absolute Maximum

| Parameter                                   | Symbol          | Value                            | unit       |
|---|-----------------|----------------------------------|------------|
| Power supply voltage relative to Vss        | Vcc             | -0.3 to +4.6                     | V          |
| Terminal voltage on any pin relative to Vss | $V_T$           | $-0.3^{*1}$ to $V_{cc}+0.3^{*2}$ | V          |
| Power dissipation                           | $P_T$           | 0.7                              | W          |
| Operation temperature                       | $T_{opr}^{*3}$  | R Ver.                           | 0 to +70   |
|   |                 | I Ver.                           | -40 to +85 |
| Storage temperature range                   | $T_{stg}$       | -65 to 150                       | °C         |
| Storage temperature range under bias        | $T_{bias}^{*3}$ | R Ver.                           | 0 to +70   |
|   |                 | I Ver.                           | -40 to +85 |

- Note
1. -3.0V for pulse  $\leq$  30ns (full width at half maximum)
  2. Maximum voltage is +4.6V.
  3. Ambient temperature range depends on R/I-version. Please see table on page 1.

## DC Operating Conditions

| Parameter                 |        | Symbol          | Min. | Typ. | Max.                 | Unit | Note |
|---------------------------|--------|-----------------|------|------|----------------------|------|------|
| Supply voltage            |        | V <sub>CC</sub> | 2.7  | 3.0  | 3.6                  | V    |      |
|                           |        | V <sub>SS</sub> | 0    | 0    | 0                    | V    |      |
| Input high voltage        |        | V <sub>IH</sub> | 2.0  | -    | V <sub>CC</sub> +0.3 | V    |      |
| Input low voltage         |        | V <sub>IL</sub> | -0.3 | -    | 0.6                  | V    | 1    |
| Ambient temperature range | R Ver. | T <sub>a</sub>  | 0    | -    | +70                  | °C   | 2    |
|                           | I Ver. |                 | -40  | -    | +85                  | °C   | 2    |

Note 1. -3.0V for pulse ≤ 30ns (full width at half maximum)

2. Ambient temperature range depends on R/I-version. Please see table on page 1.

## DC Characteristics

| Parameter                 | Symbol           | Min.                     | Typ.            | Max. | Unit | Test conditions  |   |
|---------------------------|------------------|--------------------------|-----------------|------|------|--|---|
| Input leakage current     | I <sub>LI</sub>  | -                        | -               | 1    | μA   | V <sub>in</sub> = V <sub>SS</sub> to V <sub>CC</sub>   |   |
| Output leakage current    | I <sub>LO</sub>  | -                        | -               | 1    | μA   | CS# = V <sub>IH</sub> or OE# = V <sub>IH</sub> ,<br>V <sub>I/O</sub> = V <sub>SS</sub> to V <sub>CC</sub>                          |   |
| Average operating current | I <sub>CC1</sub> | -                        | 14              | 25   | mA   | Min. cycle, duty = 100%, I <sub>I/O</sub> = 0mA<br>CS# = V <sub>IL</sub> , Others = V <sub>IH</sub> /V <sub>IL</sub>               |   |
|                           | I <sub>CC2</sub> | -                        | 2               | 5    | mA   | Cycle = 1μs, duty = 100%, I <sub>I/O</sub> = 0mA<br>CS# ≤ 0.2V,<br>V <sub>IH</sub> ≥ V <sub>CC</sub> -0.2V, V <sub>IL</sub> ≤ 0.2V |   |
| Standby current           | I <sub>SB</sub>  | -                        | -               | 0.33 | mA   | CS# = V <sub>IH</sub> ,<br>Others = V <sub>SS</sub> to V <sub>CC</sub>   |   |
| Standby current           | I <sub>SB1</sub> | -                        | 1 <sup>*1</sup> | 2    | μA   | ~+25°C   | V <sub>in</sub> = V <sub>SS</sub> to V <sub>CC</sub><br>CS# ≥ V <sub>CC</sub> -0.2V |
|                           |                  | -                        | -               | 3    | μA   | ~+40°C   |   |
|                           |                  | -                        | -               | 8    | μA   | ~+70°C   |   |
|                           |                  | -                        | -               | 10   | μA   | ~+85°C   |   |
| Output high voltage       | V <sub>OH</sub>  | 2.4                      | -               | -    | V    | I <sub>OH</sub> = -0.5mA   |   |
|                           | V <sub>OH2</sub> | V <sub>CC</sub><br>- 0.5 | -               | -    | V    | I <sub>OH</sub> = -0.05mA  |   |
| Output low voltage        | V <sub>OL</sub>  | -                        | -               | 0.4  | V    | I <sub>OL</sub> = 1mA  |   |

Note 1. Typical parameter indicates the value for the center of distribution at 3.0V (T<sub>a</sub> = 25°C), and not 100% tested.

## Capacitance

( $V_{CC} = 2.7V \sim 3.6V$ ,  $f = 1MHz$ ,  $T_a = 0 \sim +70^{\circ}C / -40 \sim +85^{\circ}C^{*2}$ )

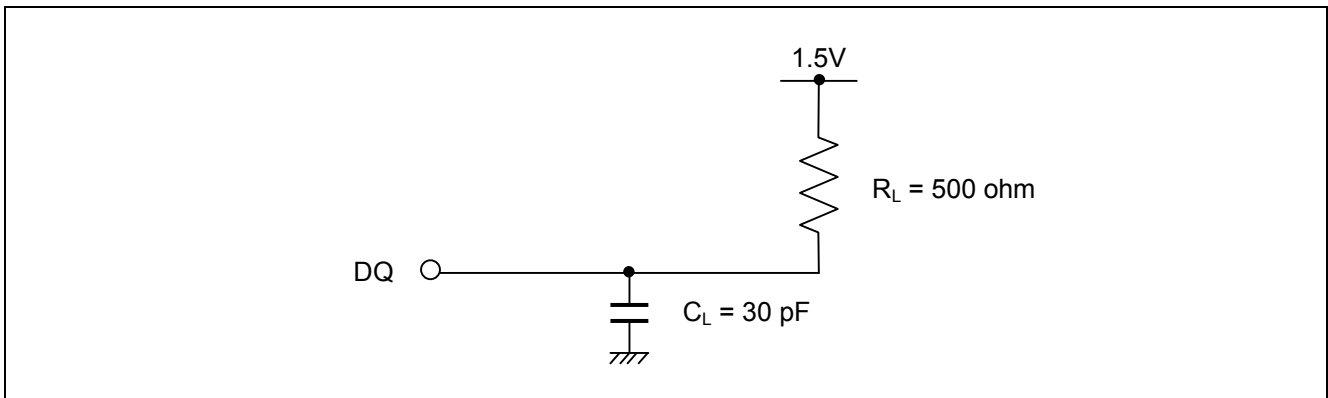
| Parameter                  | Symbol    | Min. | Typ. | Max. | Unit | Test conditions | Note |
|----------------------------|-----------|------|------|------|------|-----------------|------|
| Input capacitance          | $C_{in}$  | -    | -    | 6    | pF   | $V_{in} = 0V$   | 1    |
| Input / output capacitance | $C_{I/O}$ | -    | -    | 8    | pF   | $V_{I/O} = 0V$  | 1    |

- Note
1. This parameter is sampled and not 100% tested.
  2. Ambient temperature range depends on R/I-version. Please see table on page 1.

## AC Characteristics

Test Conditions ( $V_{CC} = 2.7V \sim 3.6V$ ,  $T_a = 0 \sim +70^{\circ}C / -40 \sim +85^{\circ}C^{*1}$ )

- Input pulse levels:  $V_{IL} = 0.4V$ ,  $V_{IH} = 2.4V$
- Input rise and fall time: 5ns
- Input and output timing reference level: 1.5V
- Output load: See figures (Including scope and jig)



- Note
1. Ambient temperature range depends on R/I-version. Please see table on page 1.

**Read Cycle**

| Parameter                          | Symbol           | R1LV5256E**-5S* |      | R1LV5256E**-7S* |      | Unit | Note  |
|------------------------------------|------------------|-----------------|------|-----------------|------|------|-------|
|                                    |                  | Min.            | Max. | Min.            | Max. |      |       |
| Read cycle time                    | t <sub>RC</sub>  | 55              | -    | 70              | -    | ns   |       |
| Address access time                | t <sub>AA</sub>  | -               | 55   | -               | 70   | ns   |       |
| Chip select access time            | t <sub>ACS</sub> | -               | 55   | -               | 70   | ns   |       |
| Output enable to output valid      | t <sub>OE</sub>  | -               | 30   | -               | 35   | ns   |       |
| Output hold from address change    | t <sub>OH</sub>  | 10              | -    | 10              | -    | ns   |       |
| Chip select to output in low-Z     | t <sub>CLZ</sub> | 5               | -    | 5               | -    | ns   | 2,3   |
| Output enable to output in low-Z   | t <sub>OLZ</sub> | 5               | -    | 5               | -    | ns   | 2,3   |
| Chip deselect to output in high-Z  | t <sub>CHZ</sub> | 0               | 20   | 0               | 25   | ns   | 1,2,3 |
| Output disable to output in high-Z | t <sub>OHZ</sub> | 0               | 20   | 0               | 25   | ns   | 1,2,3 |

## Write Cycle

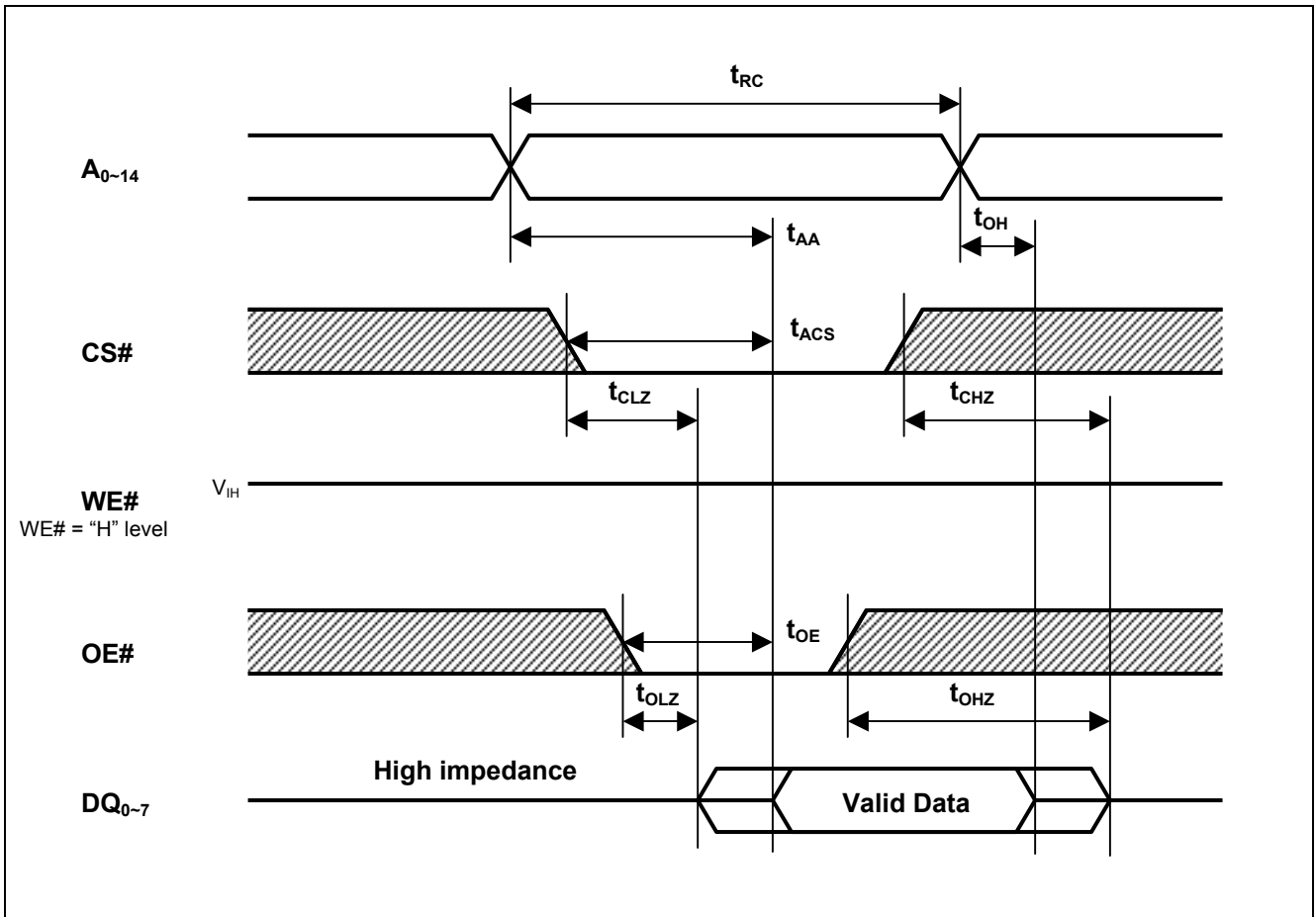
| Parameter                          | Symbol    | R1LV5256E**-5S* |      | R1LV5256E**-7S* |      | Unit | Note |
|------------------------------------|-----------|-----------------|------|-----------------|------|------|------|
|                                    |           | Min.            | Max. | Min.            | Max. |      |      |
| Write cycle time                   | $t_{WC}$  | 55              | -    | 70              | -    | ns   |      |
| Address valid to end of write      | $t_{AW}$  | 50              | -    | 65              | -    | ns   |      |
| Chip select to end of write        | $t_{CW}$  | 50              | -    | 65              | -    | ns   | 5    |
| Write pulse width                  | $t_{WP}$  | 40              | -    | 50              | -    | ns   | 4    |
| Address setup time                 | $t_{AS}$  | 0               | -    | 0               | -    | ns   | 6    |
| Write recovery time                | $t_{WR}$  | 0               | -    | 0               | -    | ns   | 7    |
| Data to write time overlap         | $t_{DW}$  | 25              | -    | 30              | -    | ns   |      |
| Data hold from write time          | $t_{DH}$  | 0               | -    | 0               | -    | ns   |      |
| Output enable from end of write    | $t_{OW}$  | 5               | -    | 5               | -    | ns   | 2    |
| Output disable to output in high-Z | $t_{OHZ}$ | 0               | 20   | 0               | 25   | ns   | 1,2  |
| Write to output in high-Z          | $t_{WHZ}$ | 0               | 20   | 0               | 25   | ns   | 1,2  |

- Note
1.  $t_{CHZ}$ ,  $t_{OHZ}$  and  $t_{WHZ}$  are defined as the time at which the outputs achieve the open circuit conditions and are not referred to output voltage levels.
  2. This parameter is sampled and not 100% tested.
  3. At any given temperature and voltage condition,  $t_{HZ}$  max is less than  $t_{LZ}$  min both for a given device and from device to device.
  4. A write occurs during the overlap of a low CS#, a low WE#.
    - A write begins at the latest transition among CS# going low and WE# going low.
    - A write ends at the earliest transition among CS# going high and WE# going high.
    - $t_{WP}$  is measured from the beginning of write to the end of write.
  5.  $t_{CW}$  is measured from the later of CS# going low to end of write.
  6.  $t_{AS}$  is measured the address valid to the beginning of write.
  7.  $t_{WR}$  is measured from the earliest of CS# or WE# going high to the end of write cycle.
  8. Don't apply inverted phase signal externally when DQ pin is output mode.

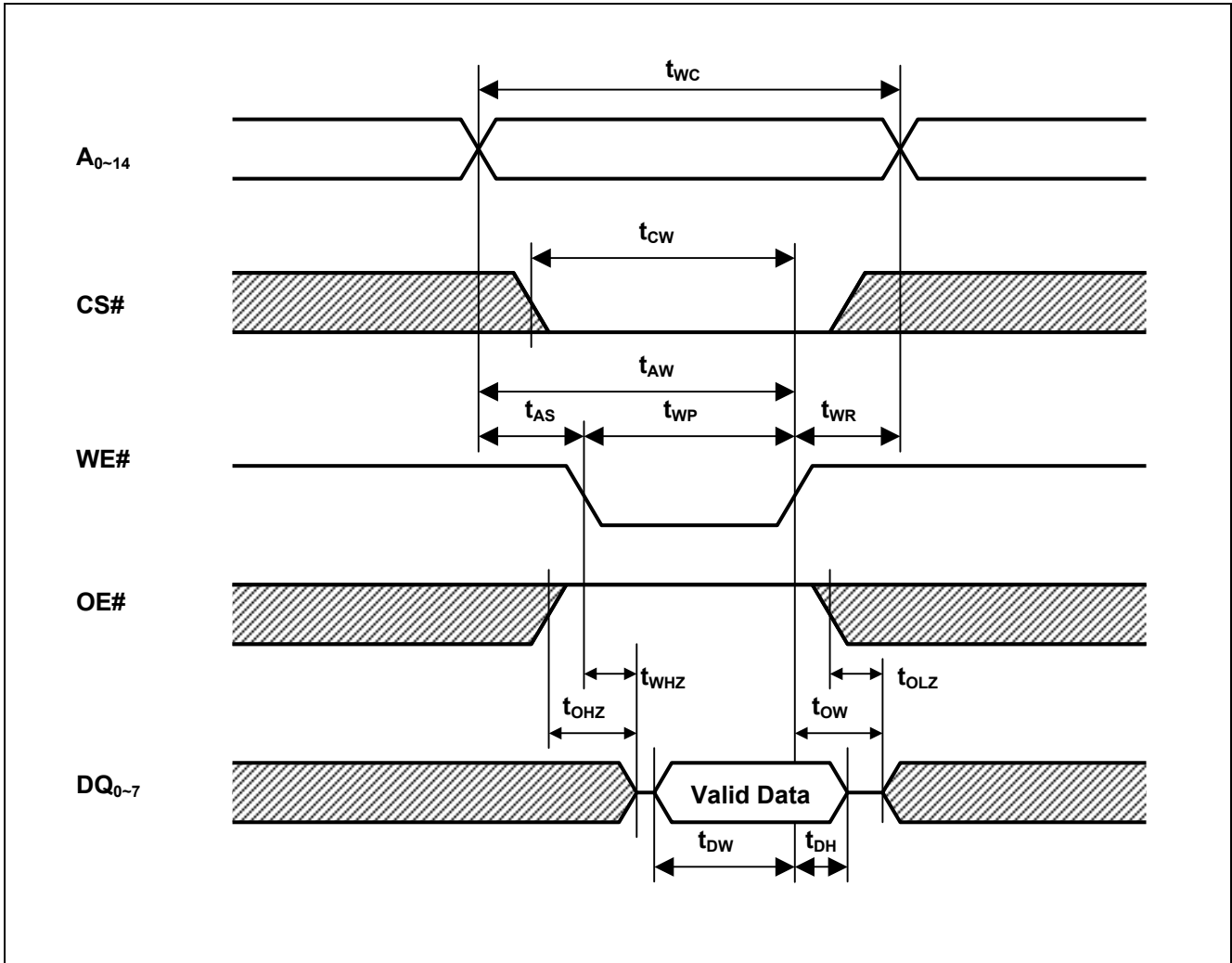


## Timing Waveforms

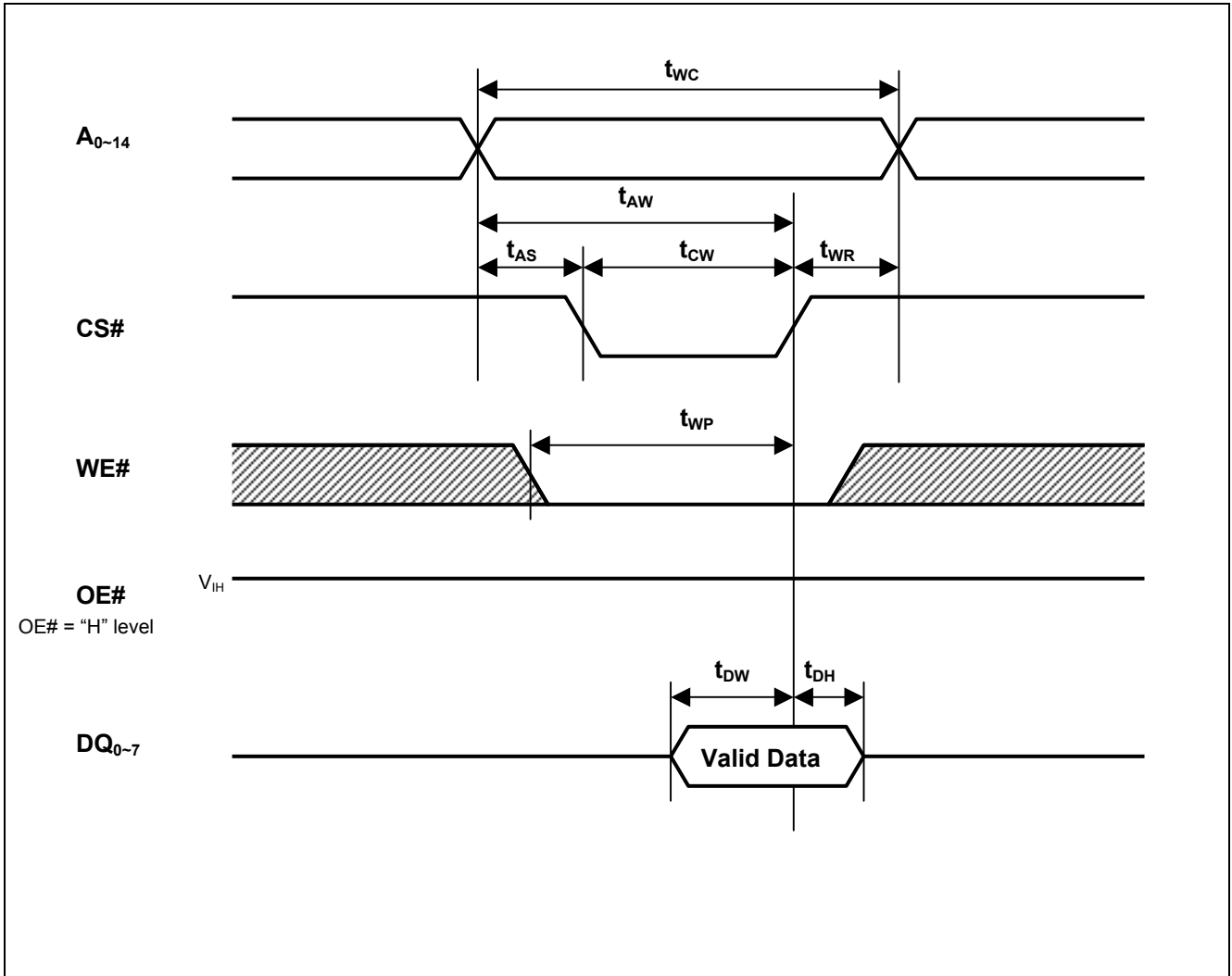
### Read Cycle



Write Cycle (1) (WE# CLOCK)



Write Cycle (2) (CS# CLOCK)

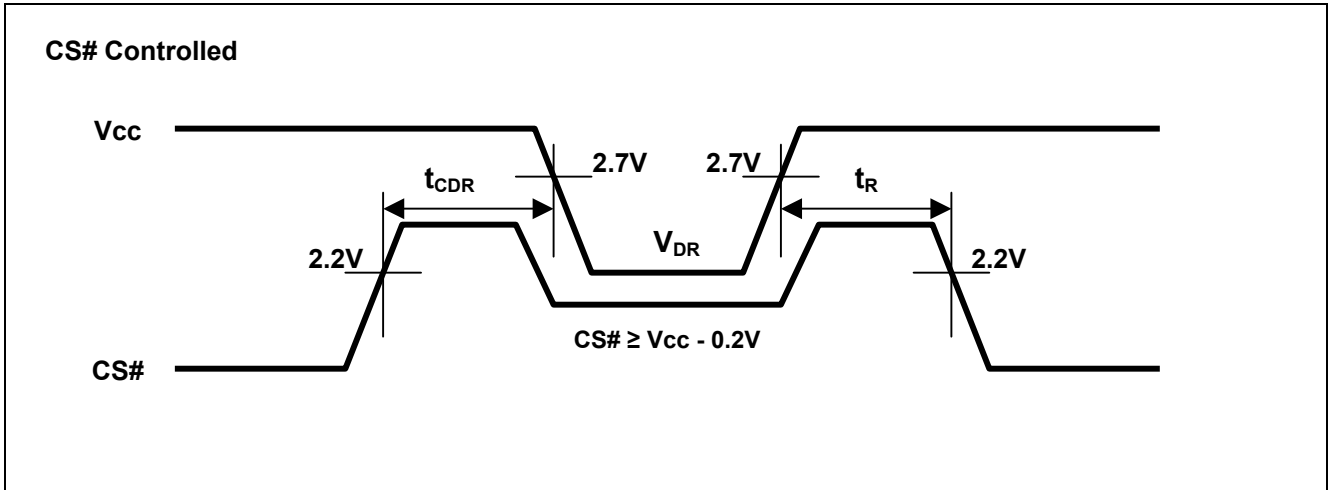


## Low Vcc Data Retention Characteristics

| Parameter                            | Symbol            | Min. | Typ.            | Max. | Unit | Test conditions <sup>2</sup>                        |   |
|--------------------------------------|-------------------|------|-----------------|------|------|---|---|
| V <sub>CC</sub> for data retention   | V <sub>DR</sub>   | 2.0  | -               | 3.6  | V    | V <sub>in</sub> ≥ 0V<br>CS# ≥ V <sub>CC</sub> -0.2V |   |
| Data retention current               | I <sub>CCDR</sub> | -    | 1 <sup>*1</sup> | 2    | μA   | ~+25°C  | V <sub>CC</sub> =3.0V, V <sub>in</sub> ≥ 0V,<br>CS# ≥ V <sub>CC</sub> -0.2V |
|                                      |                   | -    | -               | 3    | μA   | ~+40°C  |   |
|                                      |                   | -    | -               | 8    | μA   | ~+70°C  |   |
|                                      |                   | -    | -               | 10   | μA   | ~+85°C  |   |
| Chip deselect to data retention time | t <sub>CDR</sub>  | 0    | -               | -    | ns   | See retention waveform.                             |   |
| Operation recovery time              | t <sub>R</sub>    | 5    | -               | -    | ms   |   |   |

- Note
1. Typical parameter indicates the value for the center of distribution at 3.0V (T<sub>a</sub>= 25°C), and not 100% tested.
  2. CS# controls address buffer, WE# buffer, OE# buffer and Din buffer. If CS# controls data retention mode, V<sub>in</sub> levels (address, WE#, OE#, DQ) can be in the high impedance state.

Low Vcc Data Retention Timing Waveforms



|                  |                             |
|------------------|-----------------------------|
| Revision History | R1LV5256E Series Data Sheet |
|------------------|-----------------------------|

| Rev. | Date       | Description |                      |
|------|------------|-------------|----------------------|
|      |            | Page        | Summary              |
| 1.00 | 2011.04.13 | -           | First Edition issued |
|      |            |             |                      |

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