

RL78/G14

R01DS0053EJ0100

RENESAS MCU

Rev. 1.00

Feb 21, 2012

True Low Power Platform (as low as 66 μ A/MHz, and 0.60 μ A for RTC + LVD), 1.6 V to 5.5 V operation, 16 to 256 Kbyte Flash, 44 DMIPS at 32 MHz, for General Purpose Applications

1. OUTLINE

1.1 Features

Ultra-Low Power Technology

- 1.6 V to 5.5 V operation from a single supply
- Stop (RAM retained): 0.24 μ A, (LVD enabled): 0.32 μ A
- Halt (RTC + LVD): 0.60 μ A
- Snooze: T.B.D
- Operating: 66 μ A/MHz

16-bit RL78 CPU Core

- Delivers 44 DMIPS at maximum operating frequency of 32 MHz
- Instruction execution: 86% of instructions can be executed in 1 to 2 clock cycles
- CISC architecture (Harvard) with 3-stage pipeline
- Multiply signed & unsigned: 16 x 16 to 32-bit result in 1 clock cycle
- MAC: 16 x 16 to 32-bit result in 2 clock cycles
- 16-bit barrel shifter for shift & rotate in 1 clock cycle
- 1-wire on-chip debug function

Code Flash Memory

- Density: 16 KB to 256 KB
- Block size: 1KB
- On-chip single voltage flash memory with protection from block erase/writing
- Self-programming with secure boot swap function and flash shield window function

Data Flash Memory

- Data flash with background operation
- Data flash size: 4 KB to 8 KB size options
- Erase cycles: 1 Million (typ.)
- Erase/programming voltage: 1.8 V to 5.5 V

RAM

- 2.5 KB to 24 KB size options
- Supports operands or instructions
- Back-up retention in all modes

High-speed On-chip Oscillator

- 32 MHz with +/- 1% accuracy over voltage (1.8 V to 5.5 V) and temperature (-20°C to 85°C)
- Pre-configured settings: 64 MHz, 48 MHz, 32 MHz, 24 MHz, 16 MHz, 12 MHz, 8 MHz, 4 MHz & 1 MHz
- 64 MHz, 48 MHz for timer RD

Reset and Supply Management

- Power-on reset (POR) monitor/generator
- Low voltage detection (LVD) with 14 setting options (Interrupt and/or reset function)

General Purpose I/O

- 5 V tolerant, high-current (up to 20 mA per pin)
- Open-drain, on-chip pull-up resistor

Data Transfer Controller (DTC)

- 39 sources & 24 different settings
- Transfer data: 8 bits/16 bits
- Normal mode and repeat mode

Event Link Controller (ELC)

- Reduce interrupt intervention
- Link 26 events to specified peripheral function

Multiple Communication Interfaces

- Up to 8 x I²C master
- Up to 2 x I²C multi-master
- Up to 8 x CSI/SPI (7-, 8-bit)
- Up to 4 x UART (7-, 8-, 9-bit)
- Up to 1 x LIN

Extended-Function Timers

- Multi-function 16-bit timers: Up to 8 channels
- Motor control timer (3 ph - complementary mode)
- Timer with encoder function: 16-bit, 1 channel
- Real-time clock (RTC): 1 channel (full calendar and alarm function with watch correction function)
- Interval timer: 12-bit, 1 channel
- 15 kHz watchdog timer: 1 channel (window function)

Rich Analog

- ADC: Up to 20 channels, 10-bit resolution, 2.1 μ s conversion time
- Supports 1.6 V
- 2 x window comparators, with ELC connection
- D/A converter: 2 channels, 8-bit resolution
- Internal voltage reference (1.45 V)
- On-chip temperature sensor

Safety Features (IEC or UL 60730 compliance)

- Flash memory CRC calculation
- RAM parity error check
- RAM write protection
- SFR write protection
- Illegal memory access detection
- Clock stop/frequency detection
- ADC self-test
- I/O port read back function (echo)

Operating Ambient Temperature

- Standard: -40°C to + 85°C
- Extended: -40°C to + 105°C <under planning>

Package Type and Pin Count

From 4 mm x 4 mm to 14 mm x 20 mm
 QFP: 32, 44, 48, 52, 64, 80, 100
 QFN: 32, 40, 48
 SSOP: 30
 LGA: 36, 64

○ ROM, RAM capacities

Flash ROM	Data flash	RAM	RL78/G14			
			30 pins	32 pins	36 pins	40 pins
192 KB	8 KB	20 KB	—	—	—	R5F104EH
128 KB	8 KB	16 KB	R5F104AG	R5F104BG	R5F104CG	R5F104EG
96 KB	8 KB	12 KB	R5F104AF	R5F104BF	R5F104CF	R5F104EF
64 KB	4 KB	5.5 KB Note 1	R5F104AE	R5F104BE	R5F104CE	R5F104EE
48 KB	4 KB	5.5 KB Note 1	R5F104AD	R5F104BD	R5F104CD	R5F104ED
32 KB	4 KB	4 KB	R5F104AC	R5F104BC	R5F104CC	R5F104EC
16 KB	4 KB	2.5 KB	R5F104AA	R5F104BA	R5F104CA	R5F104EA

Flash ROM	Data flash	RAM	RL78/G14			
			44 pins	48 pins	52 pins	64 pins
256 KB	8 KB	24 KB Note 2	R5F104FJ	R5F104GJ	R5F104JJ	R5F104LJ
192 KB	8 KB	20 KB	R5F104FH	R5F104GH	R5F104JH	R5F104LH
128 KB	8 KB	16 KB	R5F104FG	R5F104GG	R5F104JG	R5F104LG
96 KB	8 KB	12 KB	R5F104FF	R5F104GF	R5F104JF	R5F104LF
64 KB	4 KB	5.5 KB Note 1	R5F104FE	R5F104GE	R5F104JE	R5F104LE
48 KB	4 KB	5.5 KB Note 1	R5F104FD	R5F104GD	R5F104JD	R5F104LD
32 KB	4 KB	4 KB	R5F104FC	R5F104GC	R5F104JC	R5F104LC
16 KB	4 KB	2.5 KB	R5F104FA	R5F104GA	—	—

Flash ROM	Data flash	RAM	RL78/G14	
			80 pins	100 pins
256 KB	8 KB	24 KB Note 2	R5F104MJ	R5F104PJ
192 KB	8 KB	20 KB	R5F104MH	R5F104PH
128 KB	8 KB	16 KB	R5F104MG	R5F104PG
96 KB	8 KB	12 KB	R5F104MF	R5F104PF

Note 1. This is about 4.5 KB when the self-programming function and data flash function are used.

Note 2. This is about 23 KB when the self-programming function and data flash function are used.

1.2 Ordering Information

(1/2)

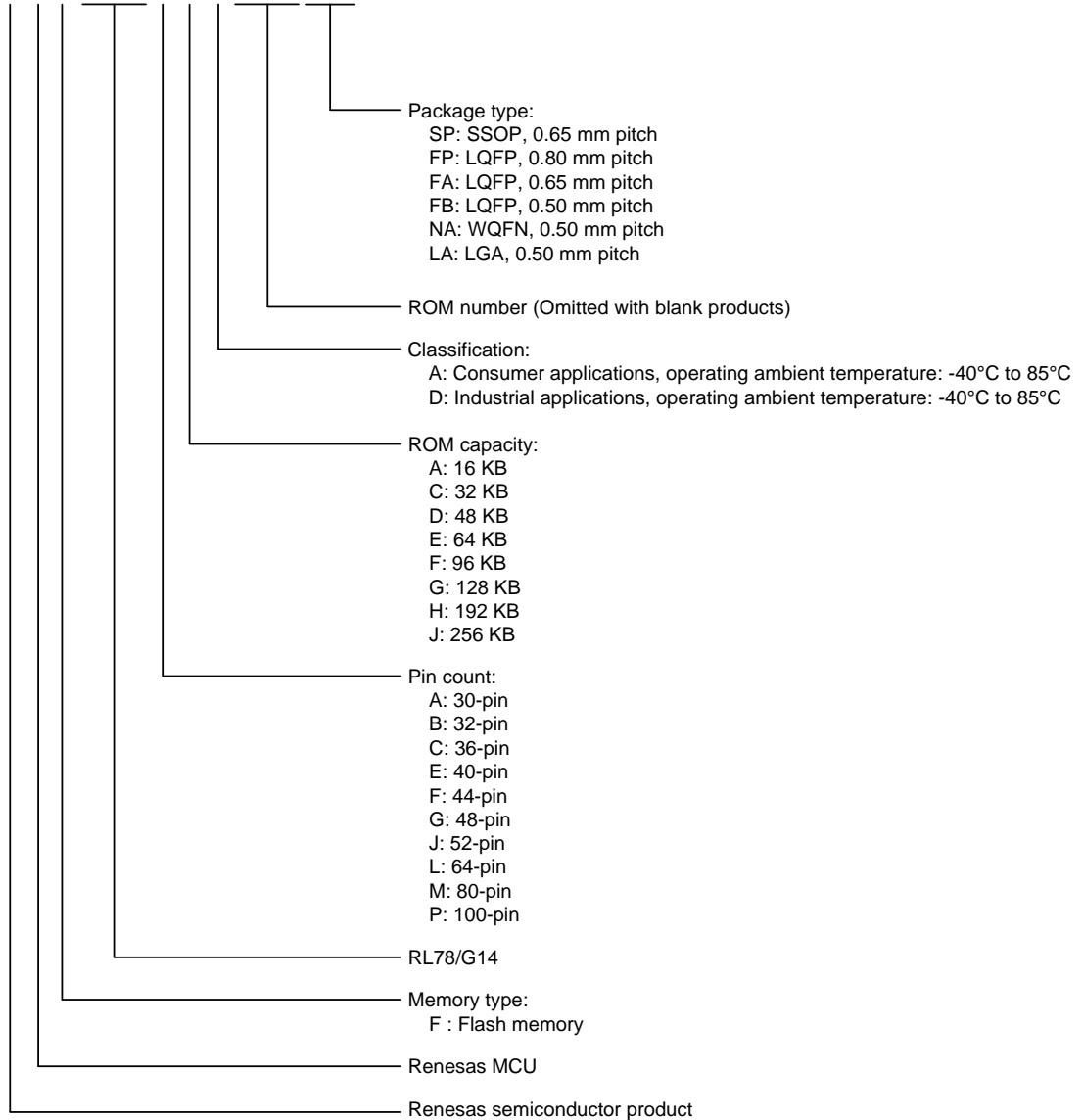
Pin count	Package	Part Number
30 pins	30-pin plastic SSOP (7.62 mm (300))	R5F104AAASP, R5F104ACASP, R5F104ADASP, R5F104AEASP, R5F104AFASP, R5F104AGASP R5F104AADSP, R5F104ACDSP, R5F104ADDSP, R5F104AEDSP, R5F104AFDSP, R5F104AGDSP
32 pins	32-pin plastic WQFN (fine pitch) (5 × 5)	R5F104BAANA, R5F104BCANA, R5F104BDANA, R5F104BEANA, R5F104BFANA, R5F104BGANA R5F104BADNA, R5F104BCDNA, R5F104BDDNA, R5F104BEDNA, R5F104BFDNA, R5F104BGDNA
	32-pin plastic LQFP (7 × 7)	R5F104BAAFP, R5F104BCAFP, R5F104BDAFP, R5F104BEAFP, R5F104BFAFP, R5F104BGAFP R5F104BADFP, R5F104BCDFP, R5F104BDDFP, R5F104BEDFP, R5F104BFDFP, R5F104BGDFP
36 pins	36-pin plastic FLGA (4 × 4)	R5F104CAALA, R5F104CCALA, R5F104CDALA, R5F104CEALA, R5F104CFALA, R5F104CGALA R5F104CADLA, R5F104CCDLA, R5F104CDDL A, R5F104CEDLA, R5F104CFDLA, R5F104CGDLA
40 pins	40-pin plastic WQFN (fine pitch) (6 × 6)	R5F104EAANA, R5F104ECANA, R5F104EDANA, R5F104EEANA, R5F104EFANA, R5F104EGANA, R5F104EHANA R5F104EADNA, R5F104ECDNA, R5F104EDDNA, R5F104EEDNA, R5F104EFDNA, R5F104EGDNA, R5F104EHDNA
44 pins	44-pin plastic LQFP (10 × 10)	R5F104FAAFP, R5F104FCAFP, R5F104FDAFP, R5F104FEAFP, R5F104FFAFP, R5F104FGAFP, R5F104FHAFP, R5F104FJAFP R5F104FADFP, R5F104FCDFP, R5F104FDDFP, R5F104FEDFP, R5F104FFDFP, R5F104FGDFP, R5F104FHDFP, R5F104FJDFP
48 pins	48-pin plastic LQFP (fine pitch) (7 × 7)	R5F104GAAFB, R5F104GCAFB, R5F104GD AFB, R5F104GE AFB, R5F104GFAFB, R5F104GG AFB, R5F104GH AFB, R5F104GJ AFB R5F104GADFB, R5F104GCDFB, R5F104GD DFB, R5F104GEDFB, R5F104GFDFB, R5F104GGDFB, R5F104GHDFB, R5F104GJDFB
	48-pin plastic WQFN (7 × 7)	R5F104GAANA, R5F104GCANA, R5F104GDANA, R5F104GEANA, R5F104GFANA, R5F104GGANA, R5F104GHANA, R5F104GJANA R5F104GADNA, R5F104GCDNA, R5F104GDDNA, R5F104GEDNA, R5F104GFDNA, R5F104GGDNA, R5F104GHDNA, R5F104GJDNA
52 pins	52-pin plastic LQFP (10 × 10)	R5F104JCAFA, R5F104JDAFA, R5F104JEAFA, R5F104JFAFA, R5F104JGAFA, R5F104JHAFA, R5F104JJAFA R5F104JCDFA, R5F104JDDFA, R5F104JEDFA, R5F104JFDFA, R5F104JGDFA, R5F104JHDFA, R5F104JJDFA

(2/2)

Pin count	Package	Part Number
64 pins	64-pin plastic LQFP (12 × 12)	R5F104LCAFA, R5F104LDAFA, R5F104LEAFA, R5F104LFAFA, R5F104LGAFB, R5F104LHAFB, R5F104LJAFB R5F104LCDFB, R5F104LDDFB, R5F104LEDFB, R5F104LDFDB, R5F104LGDFB, R5F104LHDFB, R5F104LJDFB
	64-pin plastic LQFP (fine pitch) (10 × 10)	R5F104LCAFB, R5F104LDAFB, R5F104LEAFB, R5F104LFAFB, R5F104LGAFB, R5F104LHAFB, R5F104LJAFB R5F104LCDFB, R5F104LDDFB, R5F104LEDFB, R5F104LDFDB, R5F104LGDFB, R5F104LHDFB, R5F104LJDFB
	64-pin plastic FLGA (5 × 5)	R5F104LCALA, R5F104LDALA, R5F104LEALA, R5F104LFALA, R5F104LGALA, R5F104LHALA, R5F104LJALA R5F104LCDLA, R5F104LDDLA, R5F104LEDLA, R5F104LFDLA, R5F104LGDLA, R5F104LHDLA, R5F104LJDLA
	64-pin plastic LQFP (14 × 14)	R5F104LCAFP, R5F104LDAFP, R5F104LEAFP, R5F104LFAFP, R5F104LGAFP, R5F104LHAFP, R5F104LJAFP R5F104LCDFP, R5F104LDDFP, R5F104LEDFP, R5F104LDFDP, R5F104LGDFP, R5F104LHDFP, R5F104LJDFP
80 pins	80-pin plastic LQFP (fine pitch) (12 × 12)	R5F104MFAFB, R5F104MGAFB, R5F104MHAFB, R5F104MJAFB R5F104MDFDB, R5F104MGDFB, R5F104MHDFB, R5F104MJDFB
	80-pin plastic LQFP (14 × 14)	R5F104MFAFA, R5F104MGAFB, R5F104MHAFB, R5F104MJAFB R5F104MDFDA, R5F104MGDFA, R5F104MHDFA, R5F104MJDFA
100 pins	100-pin plastic LQFP (fine pitch) (14 × 14)	R5F104PFAFB, R5F104PGAFA, R5F104PHAFA, R5F104PJAFB R5F104PFDDB, R5F104PGDFB, R5F104PHDFB, R5F104PJDFB
	100-pin plastic LQFP (14 × 20)	R5F104PFAFA, R5F104PGAFA, R5F104PHAFA, R5F104PJAFB R5F104PFDFA, R5F104PGDFA, R5F104PHDFA, R5F104PJDFB

Figure 1 - 1 Part Number, Memory Size, and Package of RL78/G14

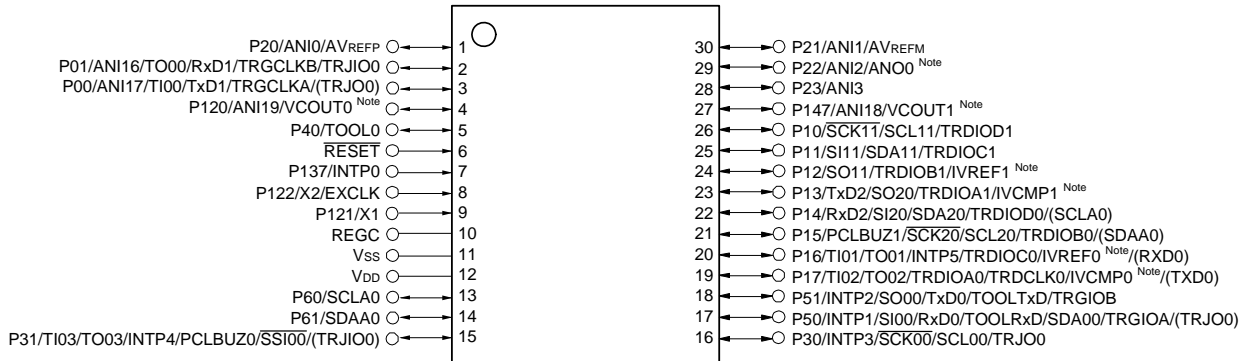
Part No. R 5 F 1 0 4 L E A x x x F B



1.3 Pin Configuration (Top View)

1.3.1 30-pin products

- 30-pin plastic SSOP (7.62 mm (300))



Note Mounted on the 96 KB or more code flash memory products.

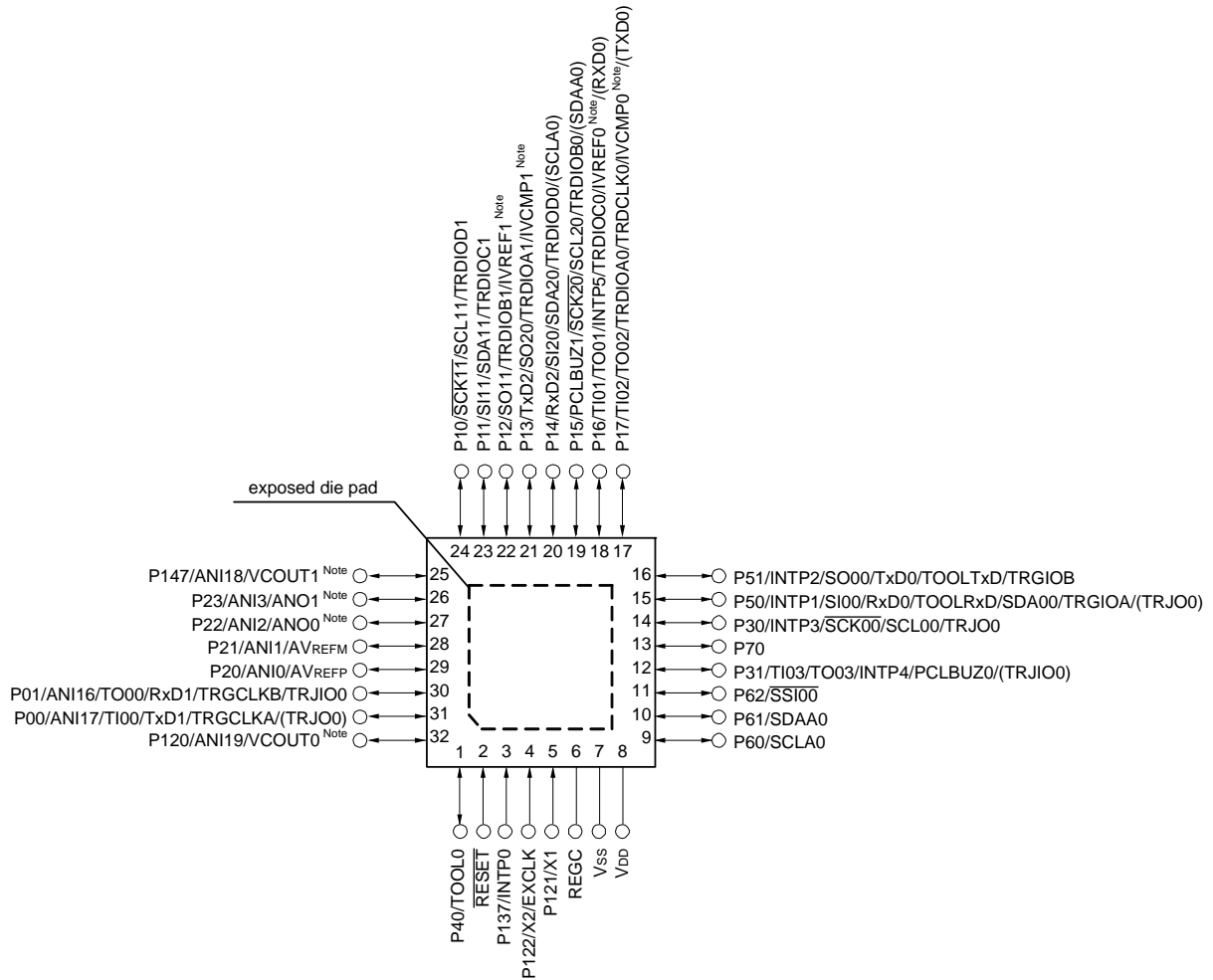
Caution Connect the REGC pin to Vss pin via a capacitor (0.47 to 1 μF).

Remark 1. For pin identification, see 1.4 Pin Identification.

Remark 2. Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register 0, 1 (PIOR0, 1).

1.3.2 32-pin products

- 32-pin plastic WQFN (fine pitch) (5 × 5)
- 32-pin plastic LQFP (7 × 7)



Note Mounted on the 96 KB or more code flash memory products.

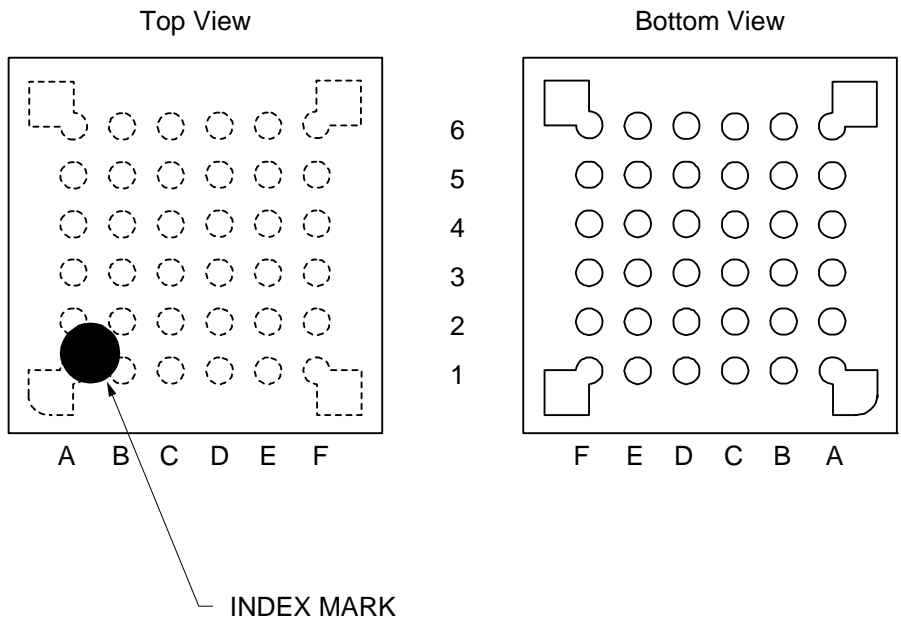
Caution Connect the REGC pin to V_{SS} pin via a capacitor (0.47 to 1 μF).

Remark 1. For pin identification, see 1.4 Pin Identification.

Remark 2. Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register 0, 1 (PIOR0, 1).

1.3.3 36-pin products

- 36-pin plastic FLGA (4 × 4)



	A	B	C	D	E	F	
6	P60/SCLA0	VDD	P121/X1	P122/X2/EXCLK	P137/INTP0	P40/TOOL0	6
5	P62/ $\overline{\text{SSI00}}$	P61/SDAA0	VSS	REGC	$\overline{\text{RESET}}$	P120/ANI19/ VCOUT0 Note	5
4	P72/SO21	P71/SI21/ SDA21	P14/RxD2/SI20/ SDA20/TRDIOD0/ (SCLA0)	P31/TI03/TO03/ INTP4/PCLBUZ0/ (TRJIO0)	P00/TI00/TxD1/ TRGCLKA/ (TRJO0)	P01/TO00/ RxD1/TRGCLKB/ TRJIO0	4
3	P50/INTP1/ SI00/RxD0/ TOOLRxD/ SDA00/TRGIOA/ (TRJO0)	P70/ $\overline{\text{SCK21}}$ / SCL21	P15/PCLBUZ1/ $\overline{\text{SCK20}}$ /SCL20/ TRDIOB0/ (SDAA0)	P22/ANI2/ ANO0 Note	P20/ANI0/ AVREFP	P21/ANI1/ AVREFM	3
2	P30/INTP3/ $\overline{\text{SCK00}}$ /SCL00/ TRJO0	P16/TI01/TO01/ INTP5/TRDIOC0/ IVREF0 Note/ (RXD0)	P12/SO11/ TRDIOB1/ IVREF1 Note	P11/SI11/ SDA11/ TRDIOC1	P24/ANI4	P23/ANI3/ ANO1 Note	2
1	P51/INTP2/ SO00/TxD0/ TOOLTxD/ TRGIOB	P17/TI02/TO02/ TRDIOA0/ TRDCLK0/ IVCMP0 Note/ (TXD0)	P13/TxD2/ SO20/TRDIOA1/ IVCMP1 Note	P10/ $\overline{\text{SCK11}}$ / SCL11/ TRDIOD1	P147/ANI18/ VCOUT1 Note	P25/ANI5	1
	A	B	C	D	E	F	

Note Mounted on the 96 KB or more code flash memory products.

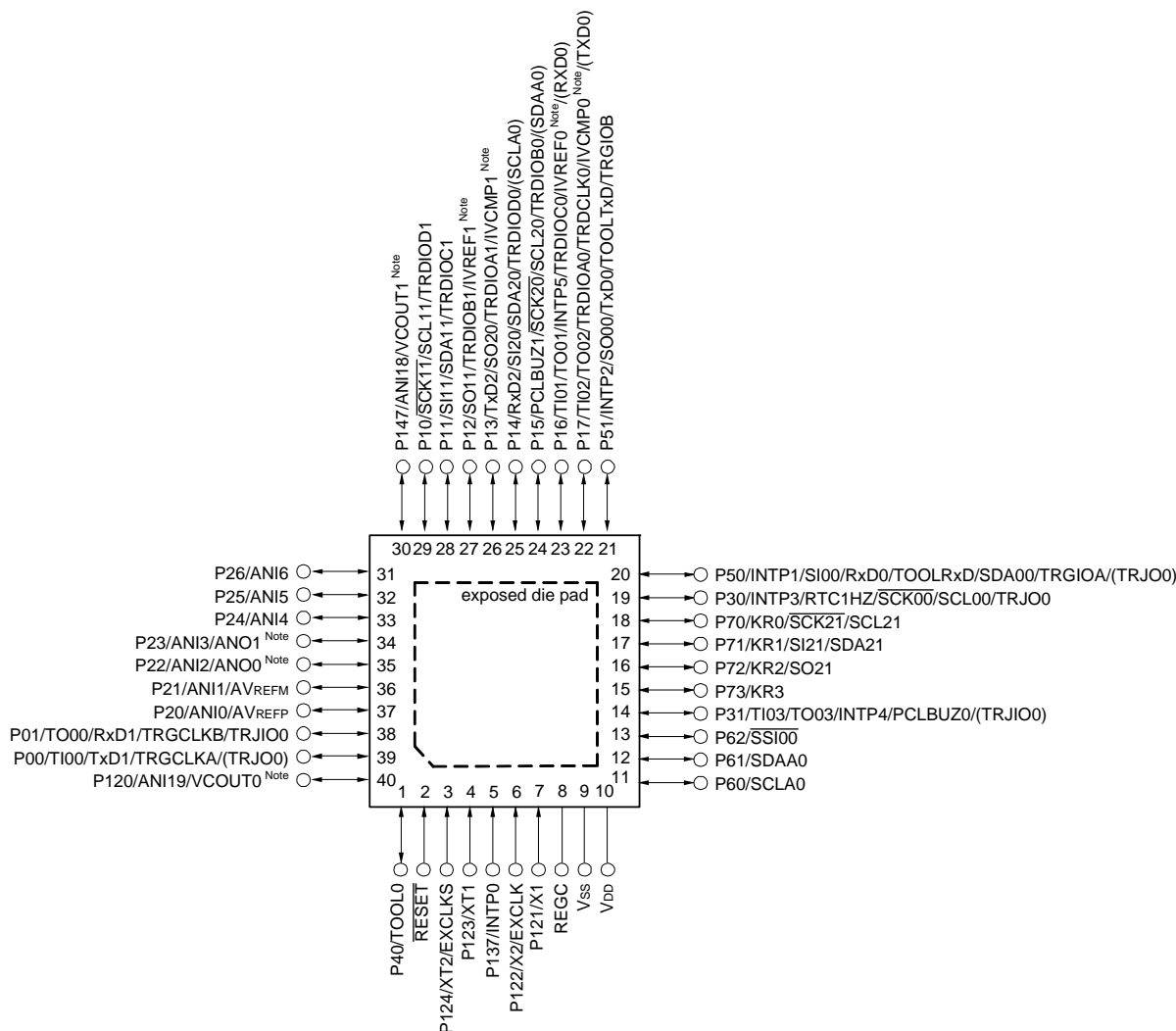
Caution Connect the REGC pin to Vss pin via a capacitor (0.47 to 1 μ F).

Remark 1. For pin identification, see 1.4 Pin Identification.

Remark 2. Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register 0, 1 (PIOR0, 1).

1.3.4 40-pin products

- 40-pin plastic WQFN (fine pitch) (6 × 6)



Note Mounted on the 96 KB or more code flash memory products.

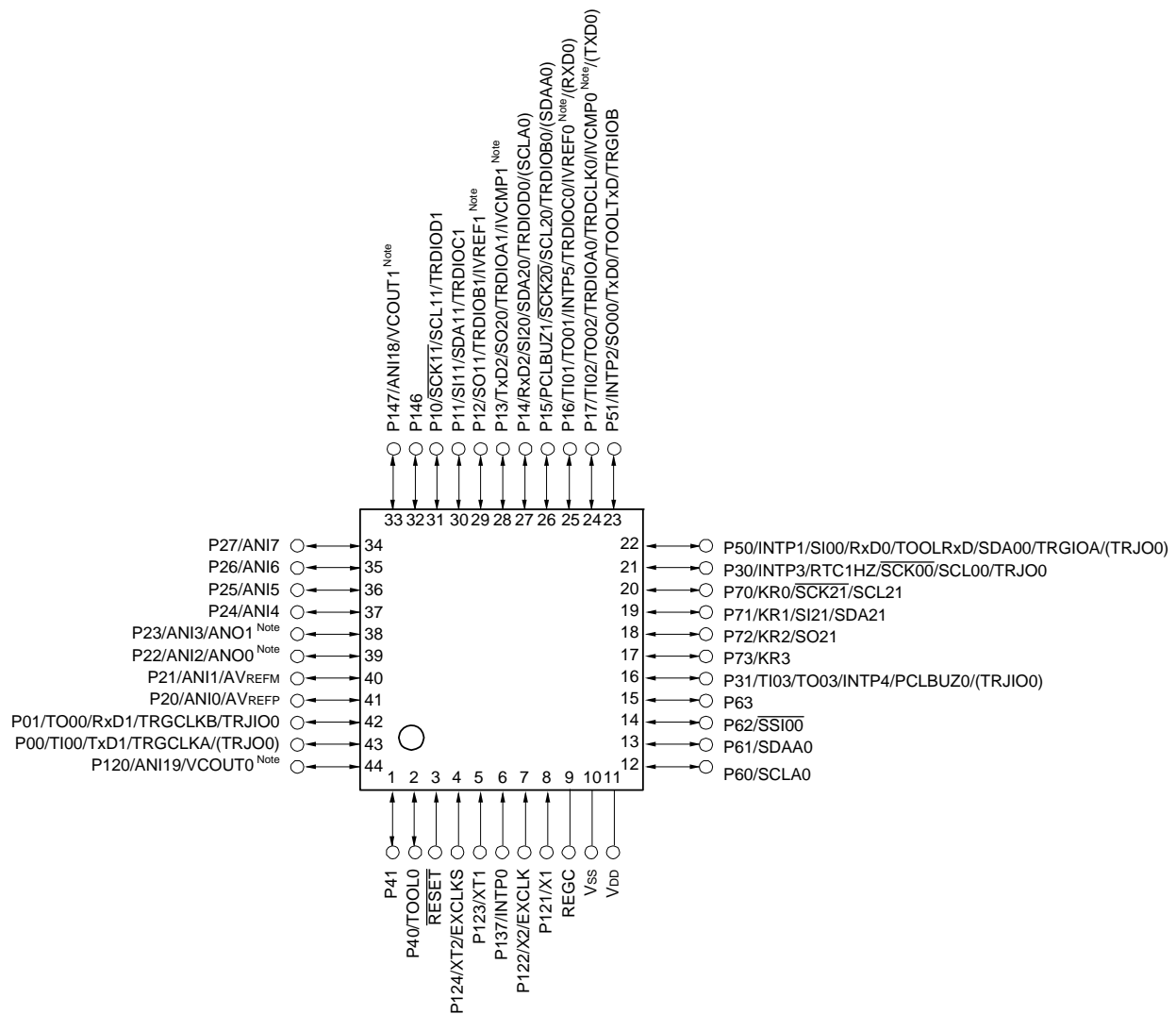
Caution Connect the REGC pin to Vss pin via a capacitor (0.47 to 1 μF).

Remark 1. For pin identification, see 1.4 Pin Identification.

Remark 2. Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register 0, 1 (PIOR0, 1).

1.3.5 44-pin products

- 44-pin plastic LQFP (10 × 10)



Note Mounted on the 96 KB or more code flash memory products.

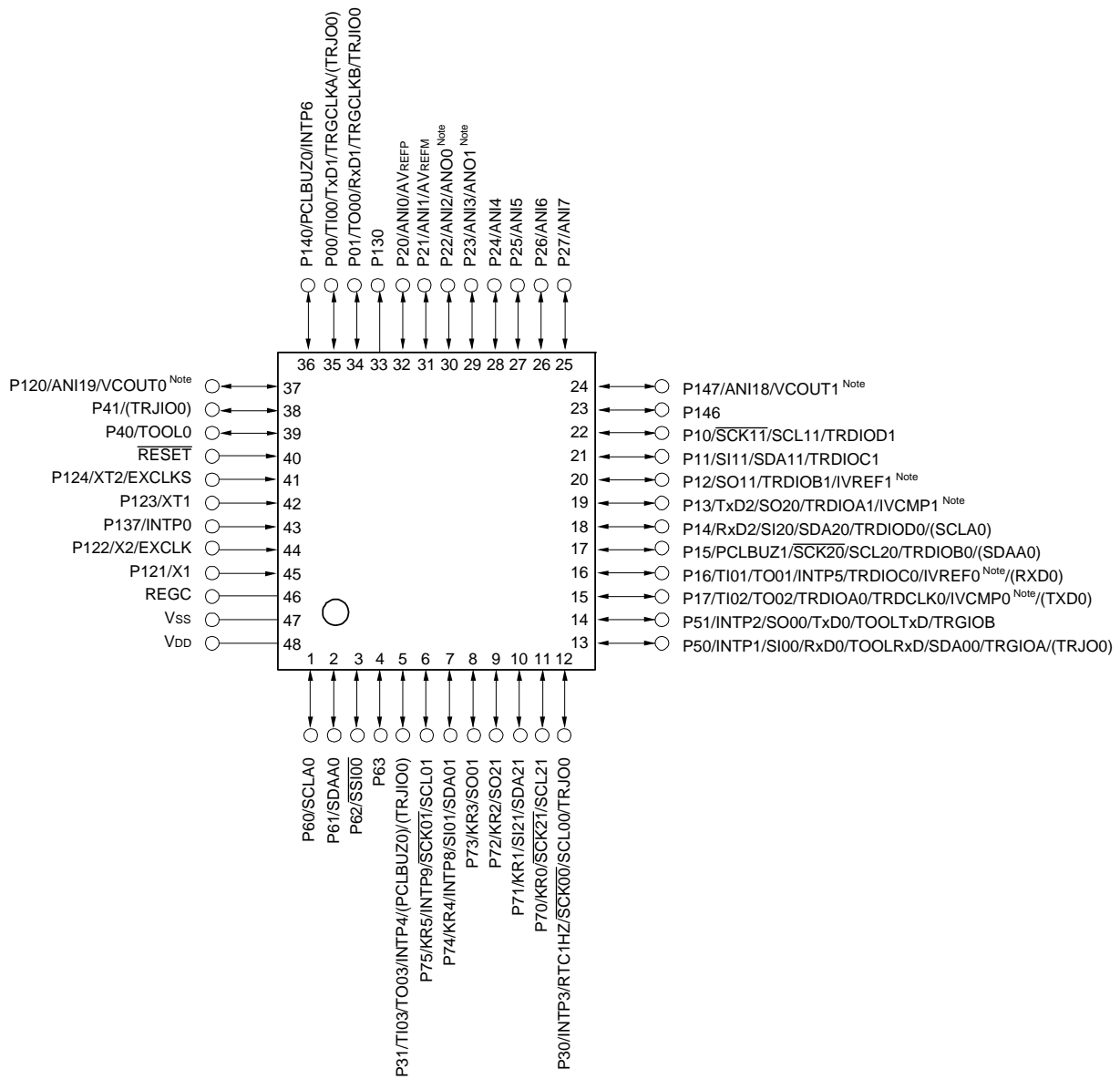
Caution Connect the REGC pin to Vss pin via a capacitor (0.47 to 1 μF).

Remark 1. For pin identification, see 1.4 Pin Identification.

Remark 2. Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register 0, 1 (PIOR0, 1).

1.3.6 48-pin products

- 48-pin plastic LQFP (fine pitch) (7 × 7)



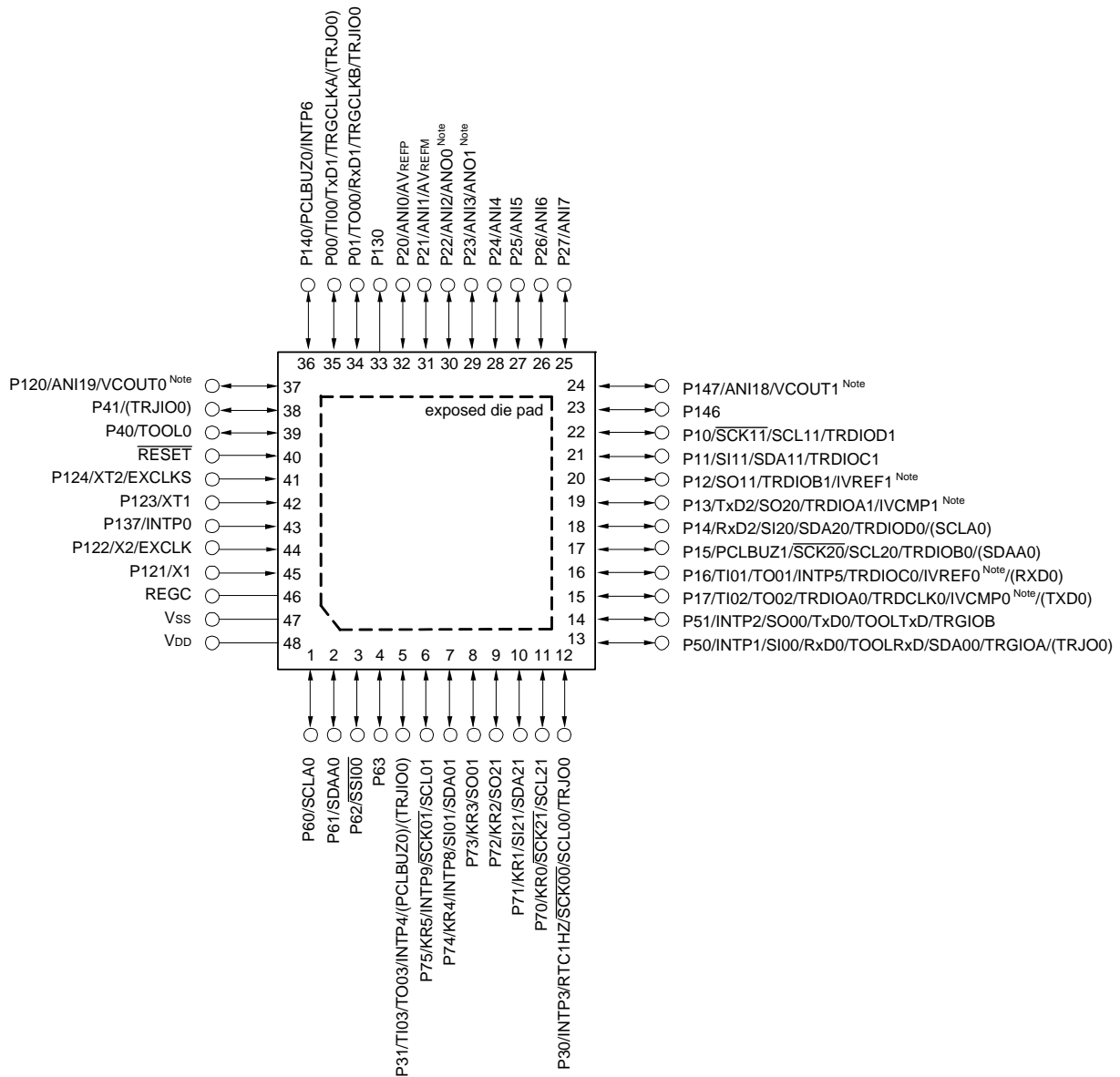
Note Mounted on the 96 KB or more code flash memory products.

Caution Connect the REGC pin to Vss pin via a capacitor (0.47 to 1 μF).

Remark 1. For pin identification, see 1.4 Pin Identification.

Remark 2. Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register 0, 1 (PIOR0, 1).

- 48-pin plastic WQFN (7 × 7)



Note Mounted on the 96 KB or more code flash memory products.

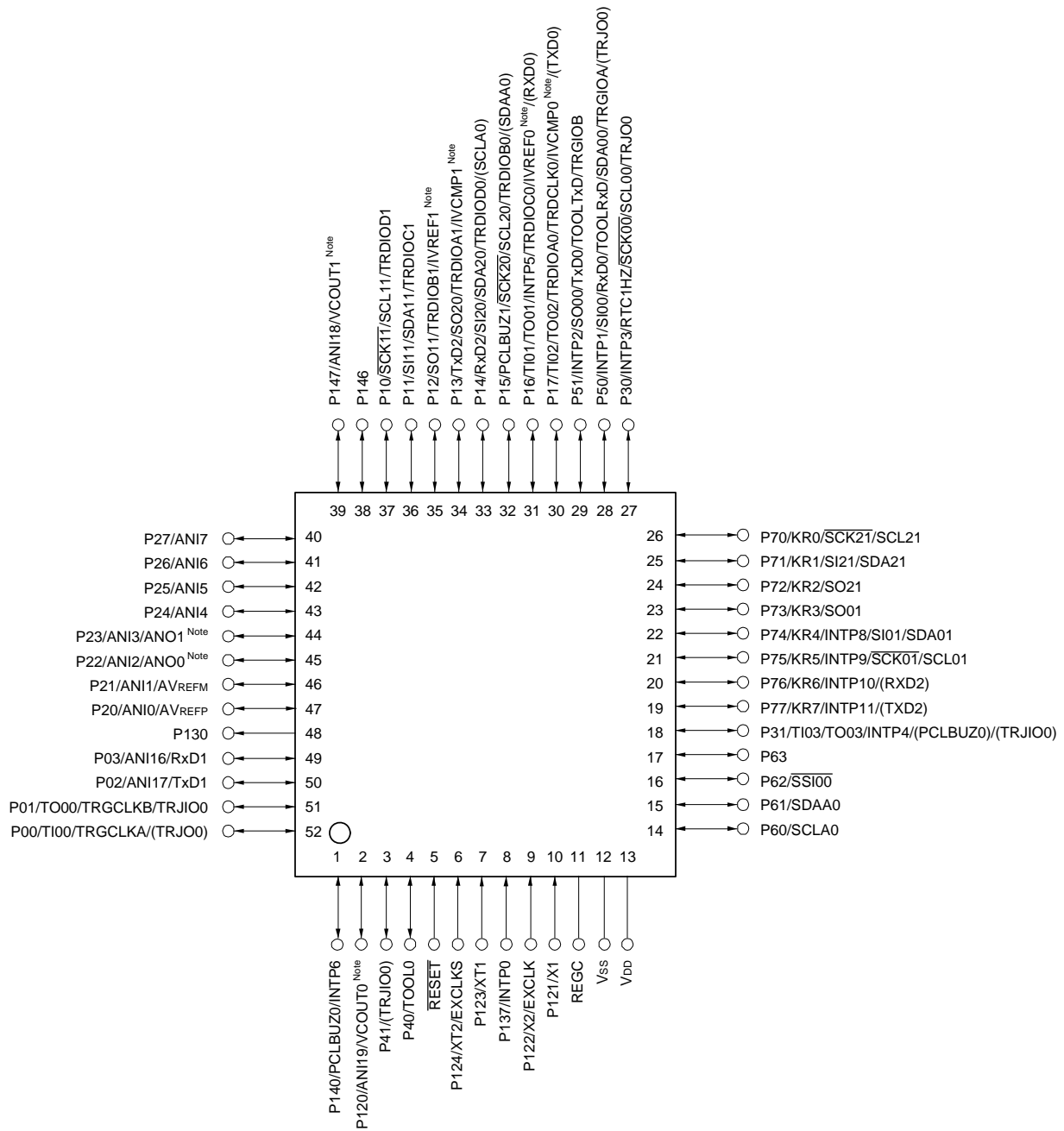
Caution Connect the REGC pin to Vss pin via a capacitor (0.47 to 1 μ F).

Remark 1. For pin identification, see 1.4 Pin Identification.

Remark 2. Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register 0, 1 (PIOR0, 1).

1.3.7 52-pin products

- 52-pin plastic LQFP (10 × 10)



Note Mounted on the 96 KB or more code flash memory products.

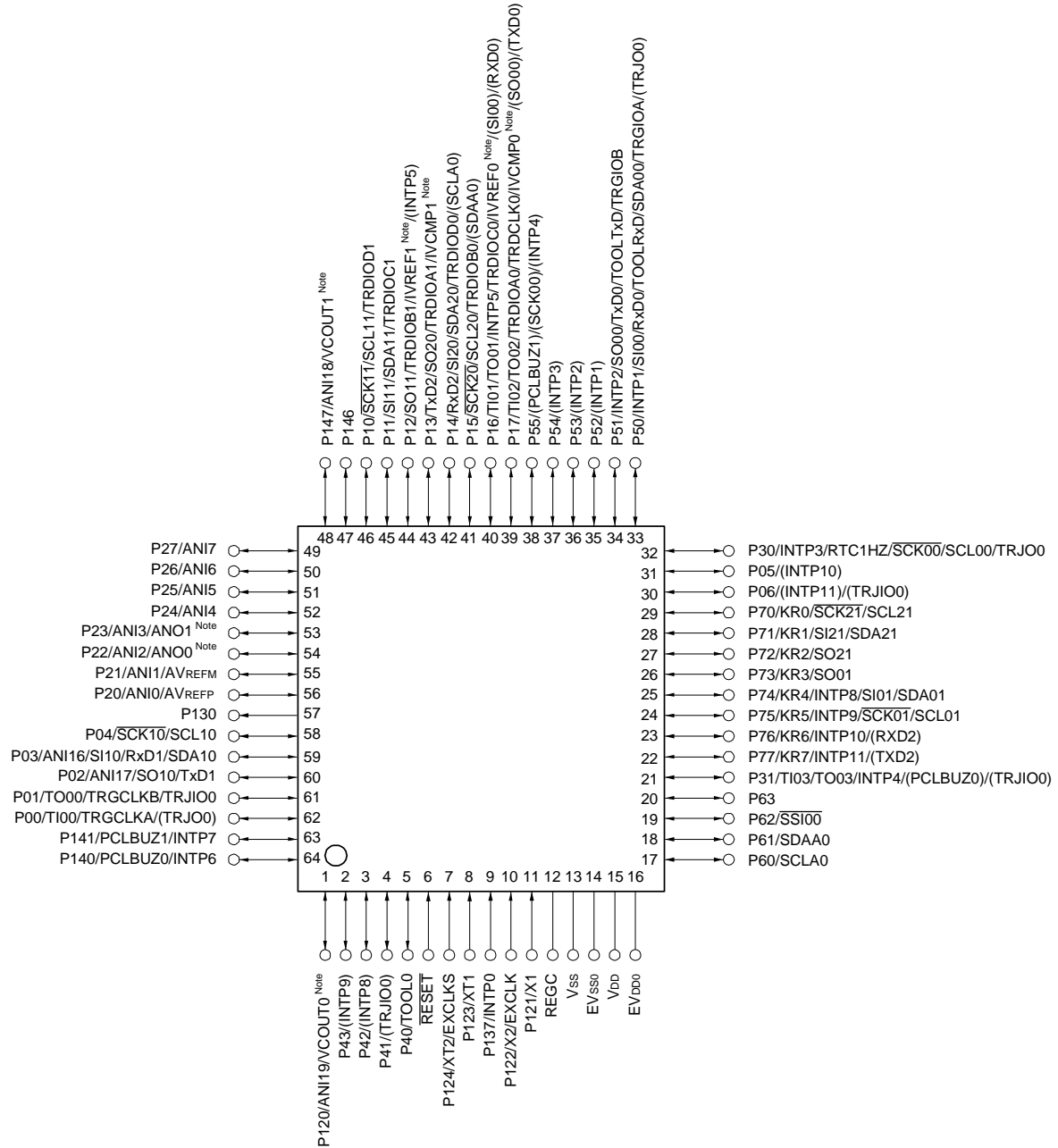
Caution Connect the REGC pin to Vss pin via a capacitor (0.47 to 1 μF).

Remark 1. For pin identification, see 1.4 Pin Identification.

Remark 2. Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register 0, 1 (PIOR0, 1).

1.3.8 64-pin products

- 64-pin plastic LQFP (14 × 14)
- 64-pin plastic LQFP (12 × 12)
- 64-pin plastic LQFP (fine pitch) (10 × 10)



Note Mounted on the 96 KB or more code flash memory products.

Caution 1. Make EVSS0 pin the same potential as Vss pin.

Caution 2. Make VDD pin the same potential as EVDD0 pin, or the potential that is higher than the EVDD0 pin.

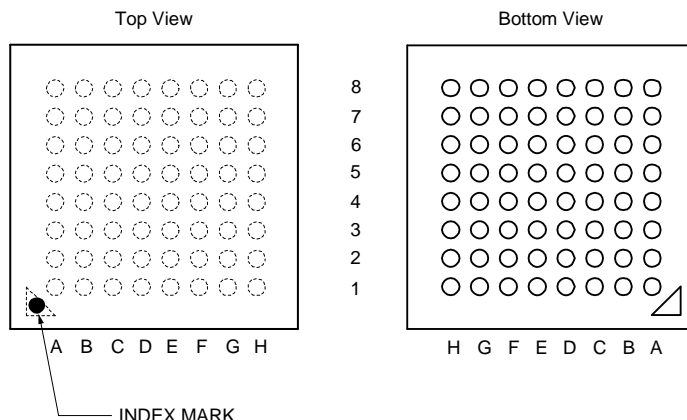
Caution 3. Connect the REGC pin to Vss pin via a capacitor (0.47 to 1 μF).

Remark 1. For pin identification, see 1.4 Pin Identification.

Remark 2. When using the microcontroller for an application where the noise generated inside the microcontroller must be reduced, it is recommended to supply separate powers to the VDD and EVDD0 pins and connect the Vss and EVSS0 pins to separate ground lines.

Remark 3. Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register 0, 1 (PIOR0, 1).

- 64-pin plastic FLGA (5 × 5)



	A	B	C	D	E	F	G	H	
8	EV _{DD0}	EV _{SS0}	P121/X1	P122/X2/ EXCLK	P137/INTP0	P123/XT1	P124/XT2/ EXCLKS	P120/ANI19/ VCOUT0 <i>Note</i>	8
7	P60/SCLA0	V _{DD}	V _{SS}	REGC	RESET	P01/TO00/ TRGCLKB/ TRJIO0	P00/TI00/ TRGCLKA/ (TRJO0)	P140/ PCLBUZ0/ INTP6	7
6	P61/SDAA0	P62/SSIO0	P63	P40/TOOL0	P41/(TRJIO0)	P43/(INTP9)	P02/ANI17/ SO10/TxD1	P141/ PCLBUZ1/ INTP7	6
5	P77/KR7/ INTP11/(TXD2)	P31/TI03/ TO03/INTP4/ (PCLBUZ0)/ (TRJIO0)	P53/(INTP2)	P42/(INTP8)	P03/ANI16/ SI10/RxD1/ SDA10	P04/SCK10/ SCL10	P130	P20/ANI0/ AVREFP	5
4	P75/KR5/ INTP9/ SCK01/ SCL01	P76/KR6/ INTP10/ (RxD2)	P52/(INTP1)	P54/(INTP3)	P16/TI01/ TO01/INTP5/ TRDI0C0/ IVREF0 <i>Note</i> / (SI00)/(RxD0)	P21/ANI1/ AVREFM	P22/ANI2/ ANO0 <i>Note</i>	P23/ANI3/ ANO1 <i>Note</i>	4
3	P70/KR0/ SCK21/ SCL21	P73/KR3/ SO01	P74/KR4/ INTP8/SI01/ SDA01	P17/TI02/TO02/ TRDIOA0/ TRDCLK0/ IVCMP0 <i>Note</i> / (SO00)/(TXD0)	P15/SCK20/ SCL20/ TRDIOB0/ (SDAA0)	P12/SO11/ TRDIOB1/ IVREF1 <i>Note</i> / (INTP5)	P24/ANI4	P26/ANI6	3
2	P30/INTP3/ RTC1HZ/ SCK00/ SCL00/TRJO0	P72/KR2/ SO21	P71/KR1/ SI21/SDA21	P06/(INTP11)/ (TRJIO0)	P14/RxD2/ SI20/SDA20/ TRDIOD0/ (SCLA0)	P11/SI11/ SDA11/ TRDI0C1	P25/ANI5	P27/ANI7	2
1	P05/(INTP10)	P50/INTP1/ SI00/RxD0/ TOOLRxD/ SDA00/ TRGIOA/ (TRJO0)	P51/INTP2/ SO00/TxD0/ TOOLTxD/ TRGIOB	P55/ (PCLBUZ1)/ (SCK00)/ (INTP4)	P13/TxD2/ SO20/ TRDIOA1/ IVCMP1 <i>Note</i>	P10/SCK11/ SCL11/ TRDIOD1	P146	P147/ANI18/ VCOUT1 <i>Note</i>	1
	A	B	C	D	E	F	G	H	

Note Mounted on the 96 KB or more code flash memory products.

Caution 1. Make EV_{SS0} pin the same potential as V_{SS} pin.

Caution 2. Make V_{DD} pin the same potential as EV_{DD0} pin, or the potential that is higher than the EV_{DD0} pin.

Caution 3. Connect the REGC pin to V_{SS} pin via a capacitor (0.47 to 1 μF).

(Remarks are listed on the next page.)

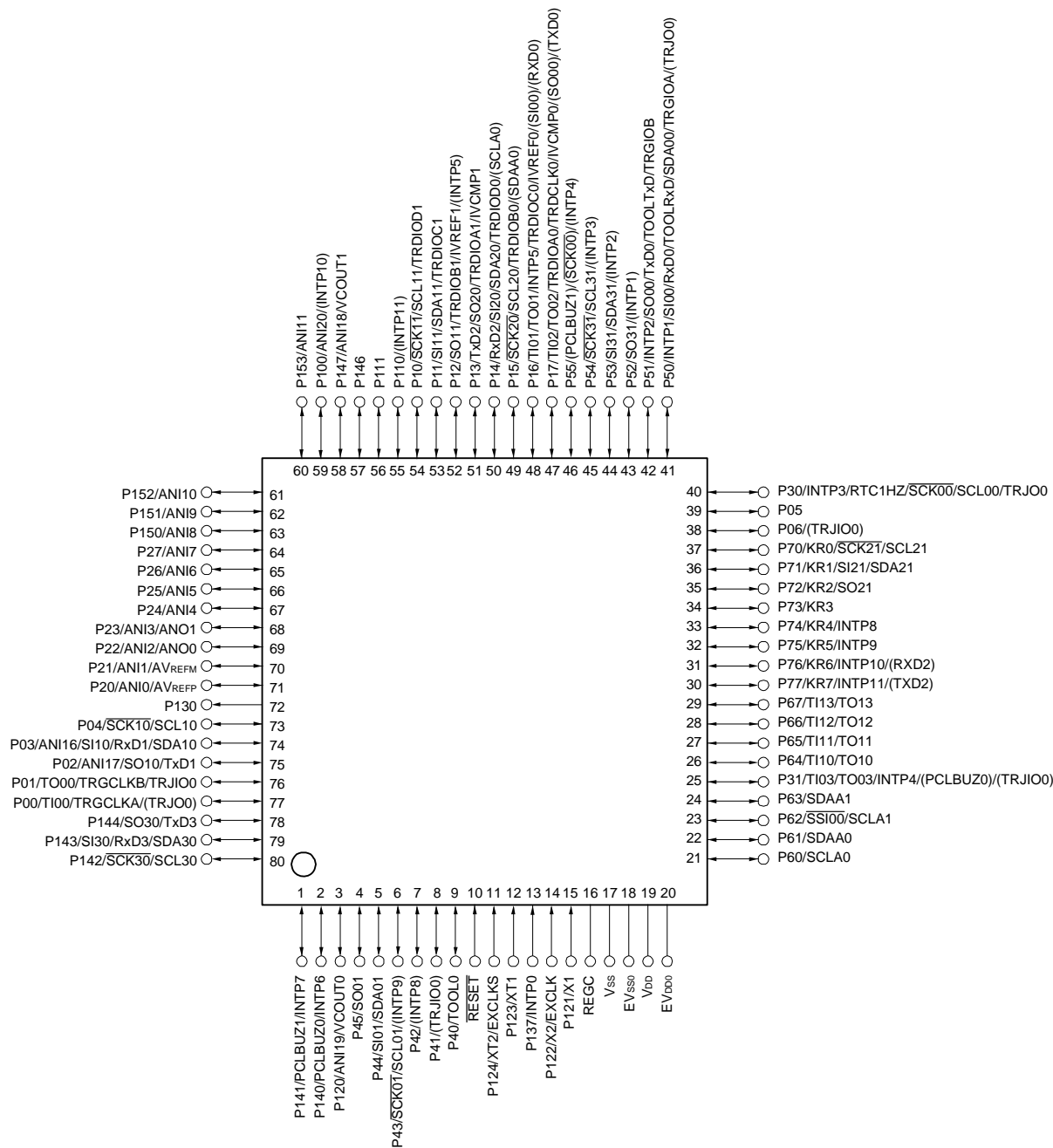
Remark 1. For pin identification, see **1.4 Pin Identification**.

Remark 2. When using the microcontroller for an application where the noise generated inside the microcontroller must be reduced, it is recommended to supply separate powers to the VDD and EVDD0 pins and connect the VSS and EVSS0 pins to separate ground lines.

Remark 3. Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register 0, 1 (PIOR0, 1).

1.3.9 80-pin products

- 80-pin plastic LQFP (14 × 14)
- 80-pin plastic LQFP (fine pitch) (12 × 12)



Caution Make EV_{SS0} pin the same potential as V_{SS} pin.

Caution 1. Make V_{DD} pin the same potential as EV_{DD0} pin, or the potential that is higher than the EV_{DD0} pin.

Caution 2. Connect the REGC pin to V_{SS} pin via a capacitor (0.47 to 1 μF).

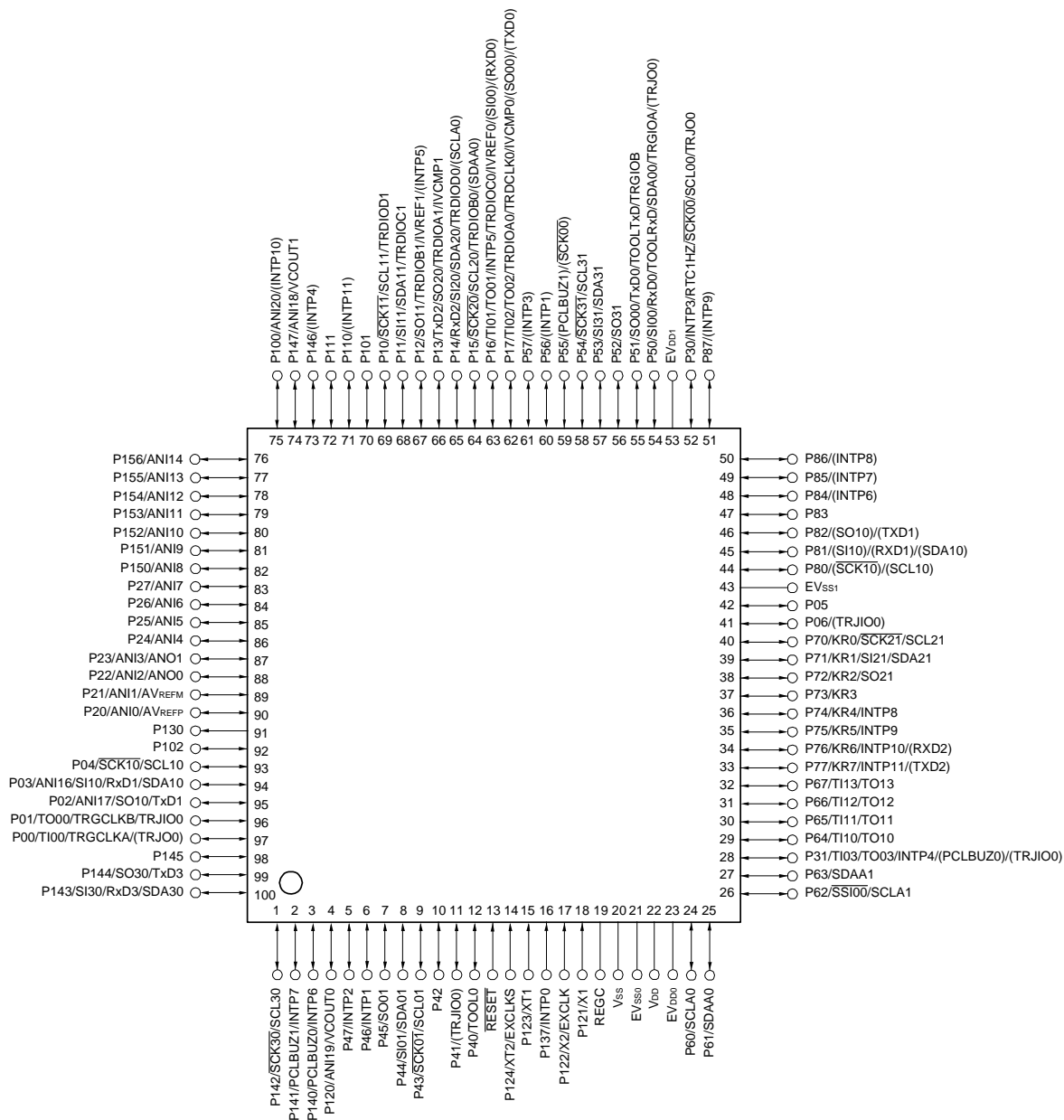
Remark 1. For pin identification, see 1.4 Pin Identification.

Remark 2. When using the microcontroller for an application where the noise generated inside the microcontroller must be reduced, it is recommended to supply separate powers to the V_{DD} and EV_{DD0} pins and connect the V_{SS} and EV_{SS0} pins to separate ground lines.

Remark 3. Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register 0, 1 (PIOR0, 1).

1.3.10 100-pin products

- 100-pin plastic LQFP (fine pitch) (14 × 14)



Caution Make EVss0, EVss1 pins the same potential as Vss pin.

Caution 1. Make VDD pin the same potential as EVDD0 pin, or the potential that is higher than the EVDD0 pin.
Make EVDD1 pin the same potential as EVDD0 pin.

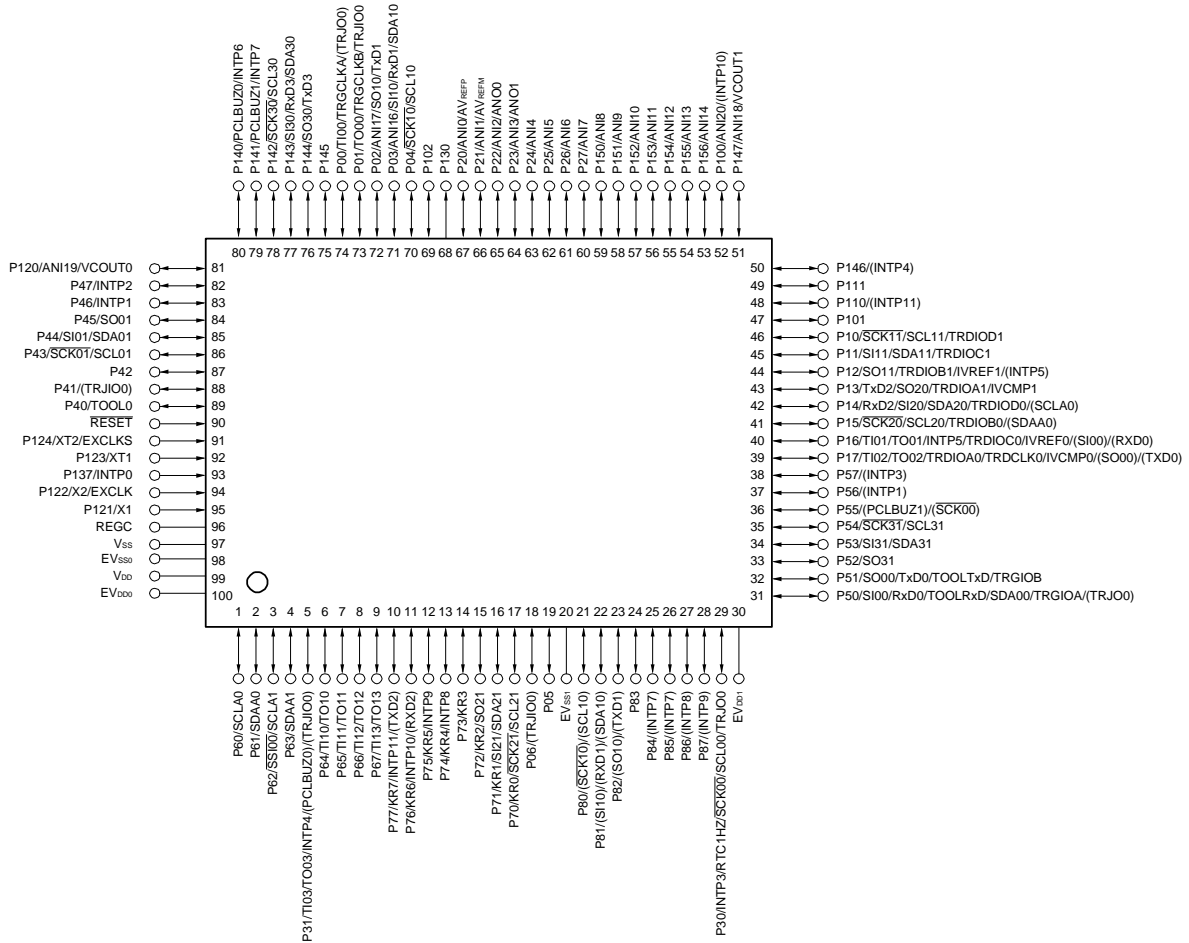
Caution 2. Connect the REGC pin to Vss pin via a capacitor (0.47 to 1 μF).

Remark 1. For pin identification, see 1.4 Pin Identification.

Remark 2. When using the microcontroller for an application where the noise generated inside the microcontroller must be reduced, it is recommended to supply separate powers to the VDD, EVDD0 and EVDD1 pins and connect the Vss, EVss0 and EVss1 pins to separate ground lines.

Remark 3. Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register 0, 1 (PIOR0, 1).

- 100-pin plastic LQFP (fine pitch) (14 × 20)



Caution Make EV_{SS0}, EV_{SS1} pins the same potential as V_{SS} pin.

Caution 1. Make V_{DD} pin the same potential as EV_{DD0} pin, or the potential that is higher than the EV_{DD0} pin.

Make EV_{DD1} pin the same potential as EV_{DD0} pin

Caution 2. Connect the REGC pin to V_{SS} pin via a capacitor (0.47 to 1 μF).

Remark 1. For pin identification, see 1.4 Pin Identification.

Remark 2. When using the microcontroller for an application where the noise generated inside the microcontroller must be reduced, it is recommended to supply separate powers to the V_{DD}, EV_{DD0} and EV_{DD1} pins and connect the V_{SS}, EV_{SS0} and EV_{SS1} pins to separate ground lines.

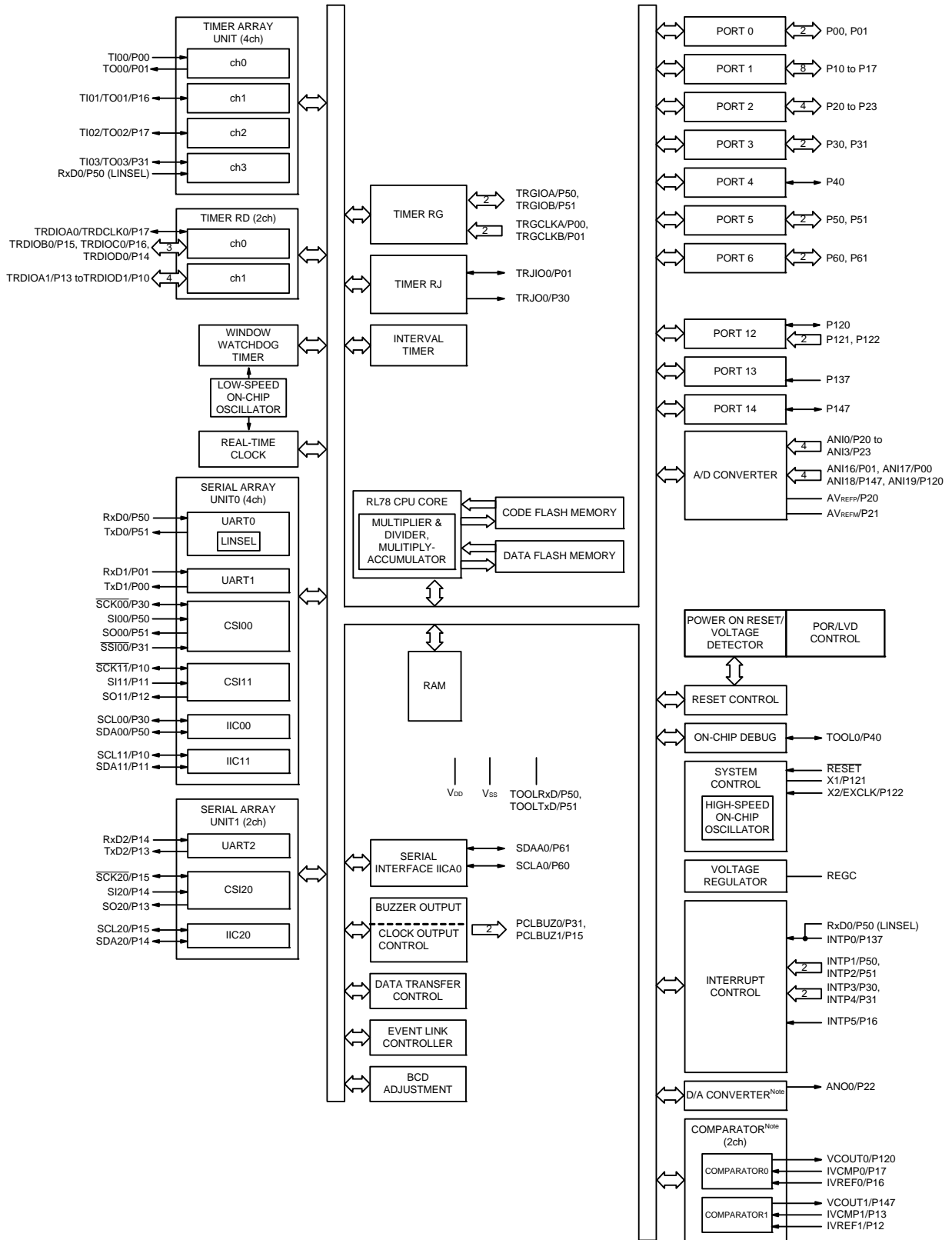
Remark 3. Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register 0, 1 (PIOR0, 1).

1.4 Pin Identification

ANI0 to ANI14,:	Analog input	RxD0 to RxD3:	Receive data
ANI16 to ANI20		$\overline{\text{SCK00}}$, $\overline{\text{SCK01}}$, $\overline{\text{SCK10}}$,:	Serial clock input/output
ANO0, ANO1:	Analog output	$\overline{\text{SCK11}}$, $\overline{\text{SCK20}}$, $\overline{\text{SCK21}}$,	
AVREFM:	A/D converter reference potential (– side) input	$\overline{\text{SCK30}}$, $\overline{\text{SCK31}}$	
AVREFP:	A/D converter reference potential (+ side) input	SCLA0, SCLA1, SCL00,:	Serial clock input/output
EVDD0, EVDD1:	Power supply for port	SCL01, SCL10, SCL11,	
EVSS0, EVSS1:	Ground for port	SCL20, SCL21, SCL30,	
EXCLK:	External clock input (main system clock)	SCL31	
EXCLKS:	External clock input (sub system clock)	SDAA0, SDAA1, SDA00,:	Serial data input/output
INTP0 to INTP11:	External interrupt input	SDA01, SDA10, SDA11,	
IVCMP0, IVCMP1:	Comparator input	SDA20, SDA21, SDA30,	
IVREF0, IVREF1:	Comparator reference input	SDA31	
KR0 to KR7:	Key return	SI00, SI01, SI10, SI11,:	Serial data input
P00 to P06:	Port 0	SI20, SI21, SI30, SI31	
P10 to P17:	Port 1	SO00, SO01, SO10,:	Serial data output
P20 to P27:	Port 2	SO11, SO20, SO21,	
P30, P31:	Port 3	SO30, SO31	
P40 to P47:	Port 4	$\overline{\text{SSI00}}$:	Serial interface chip select input
P50 to P57:	Port 5	TI00 to TI03,:	Timer input
P60 to P67:	Port 6	TI10 to TI13	
P70 to P77:	Port 7	TO00 to TO03,:	Timer output
P80 to P87:	Port 8	TO10 to TO13, TRJ00	
P100 to P102:	Port 10	TOOL0:	Data input/output for tool
P110, P111:	Port 11	TOOLRxD, TOOLTxD:	Data input/output for external device
P120 to P124:	Port 12	TRDCLK0, TRGCLKA,:	Timer external input clock
P130, P137:	Port 13	TRGCLKB	
P140 to P147:	Port 14	TRDIOA0, TRDIOB0,:	Timer input/output
P150 to P156:	Port 15	TRDIOC0, TRDIOD0,	
PCLBUZ0, PCLBUZ1:	Programmable clock output/buzzer output	TRDIOA1, TRDIOB1,	
REGC:	Regulator capacitance	TRDIOC1, TRDIOD1,	
$\overline{\text{RESET}}$:	Reset	TRGIOA, TRGIOB, TRJIO0	
RTC1HZ:	Real-time clock correction clock (1 Hz) output	TxD0 to TxD3:	Transmit data
		VCOUT0, VCOUT1:	Comparator output
		VDD:	Power supply
		VSS:	Ground
		X1, X2:	Crystal oscillator (main system clock)
		XT1, XT2:	Crystal oscillator (subsystem clock)

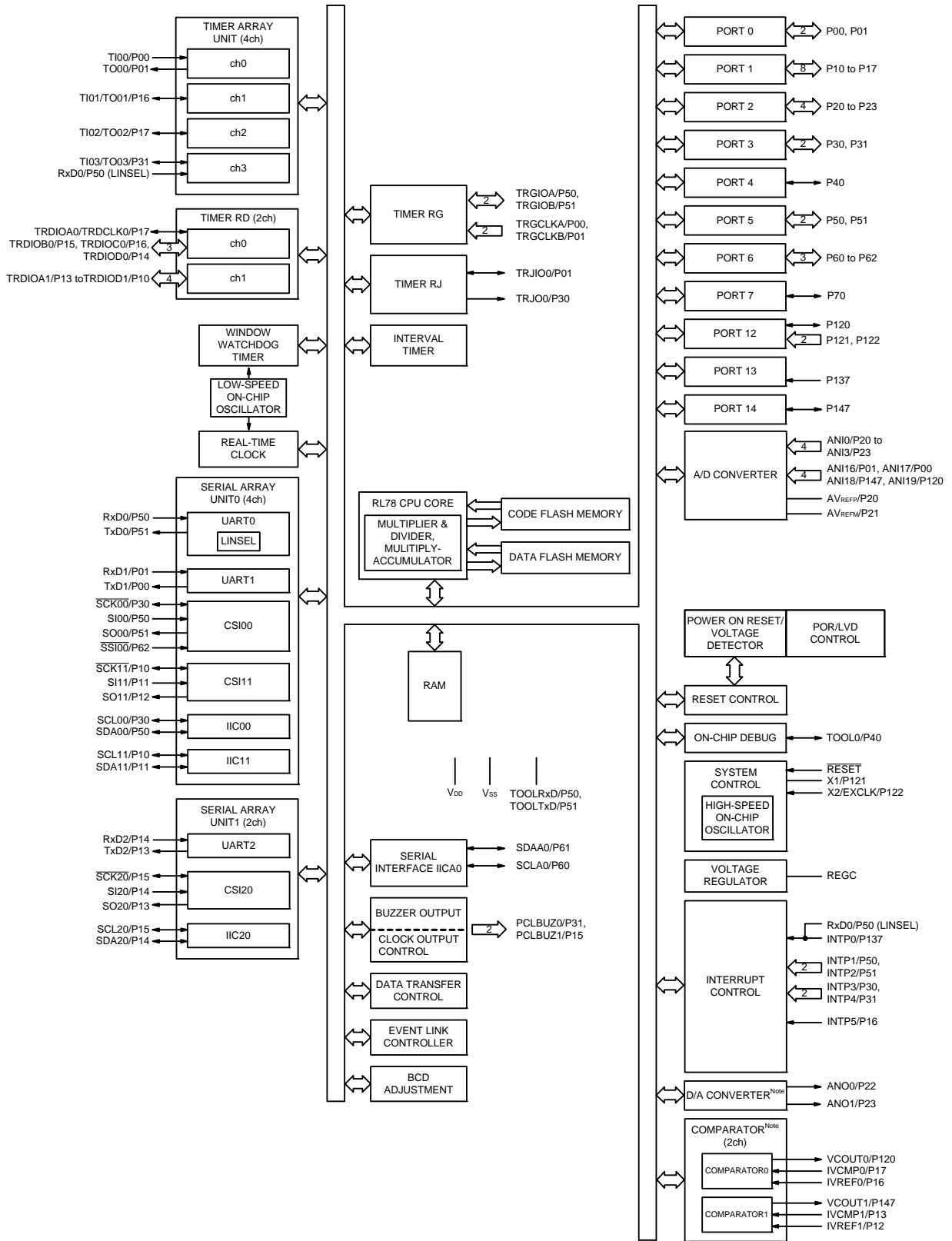
1.5 Block Diagram

1.5.1 30-pin products



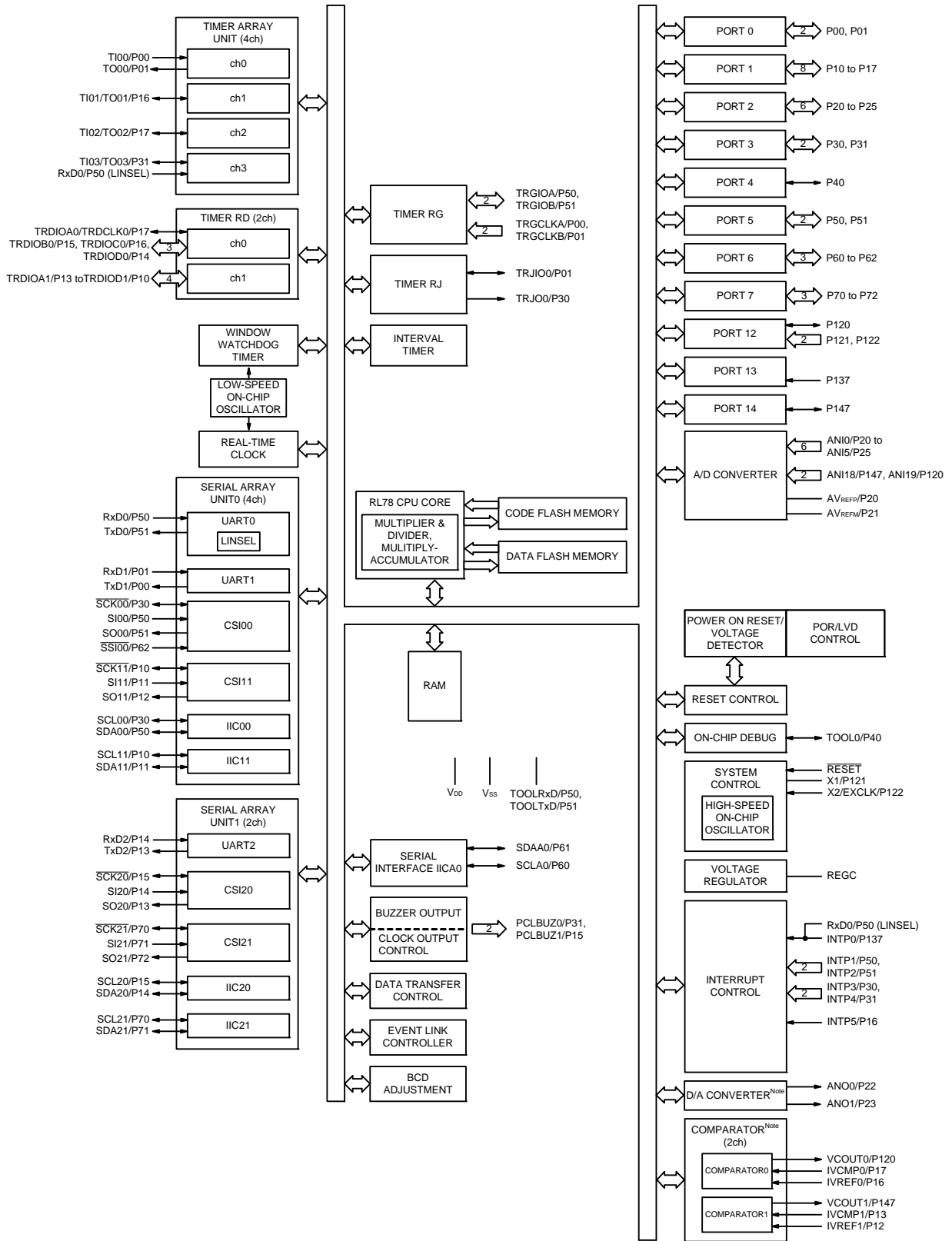
Note Mounted on the 96 KB or more code flash memory products.

1.5.2 32-pin products



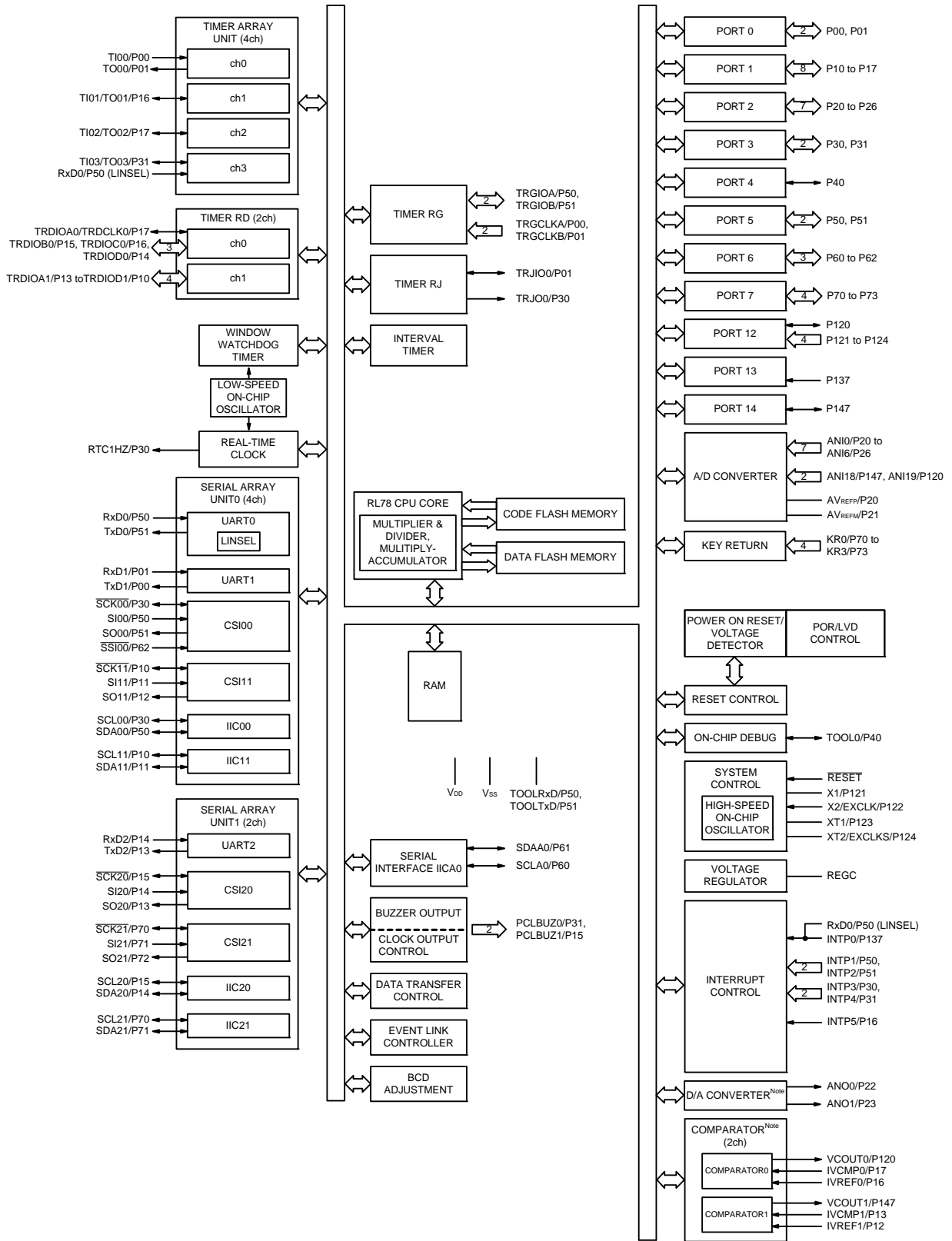
Note Mounted on the 96 KB or more code flash memory products.

1.5.3 36-pin products



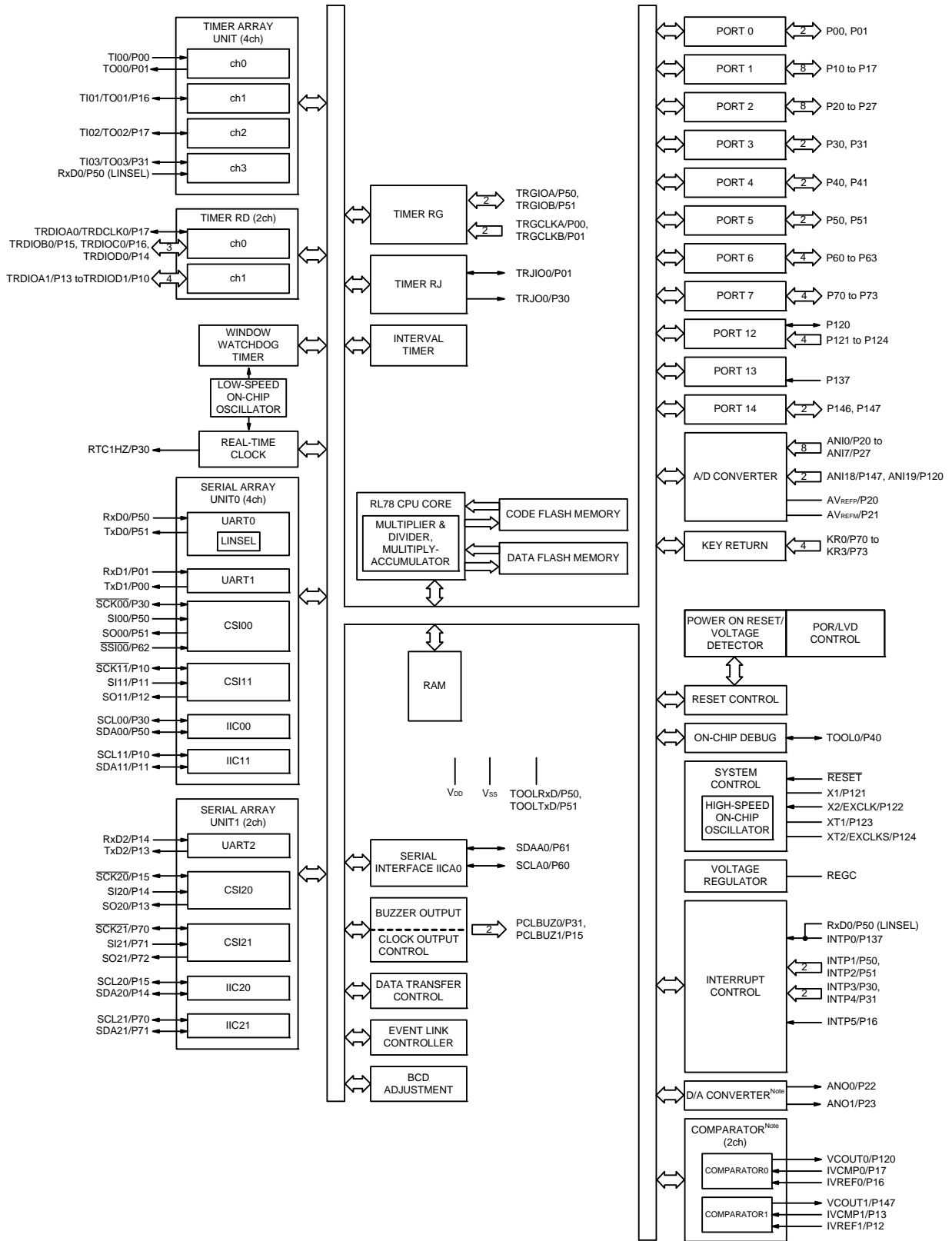
Note Mounted on the 96 KB or more code flash memory products.

1.5.4 40-pin products



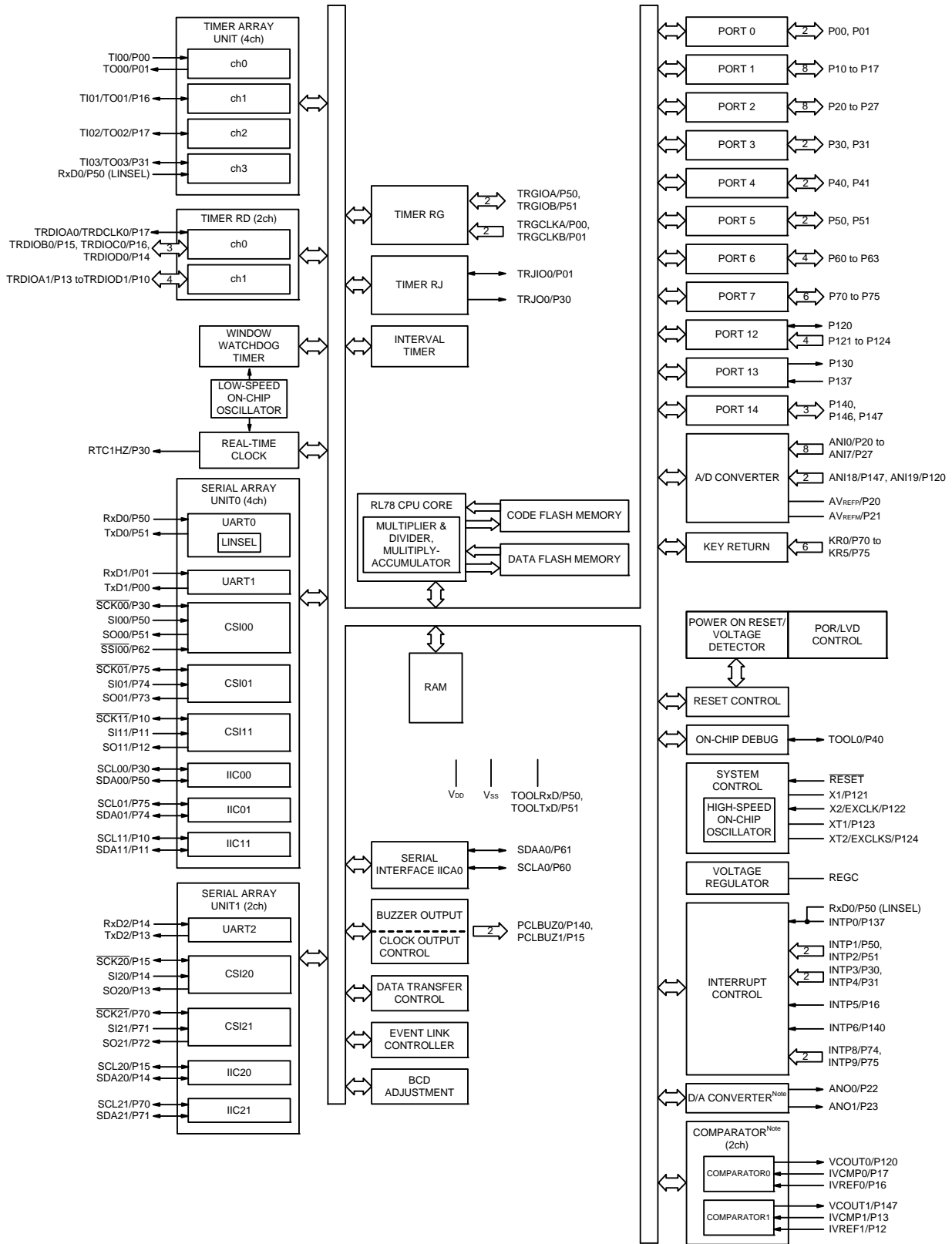
Note Mounted on the 96 KB or more code flash memory products.

1.5.5 44-pin products



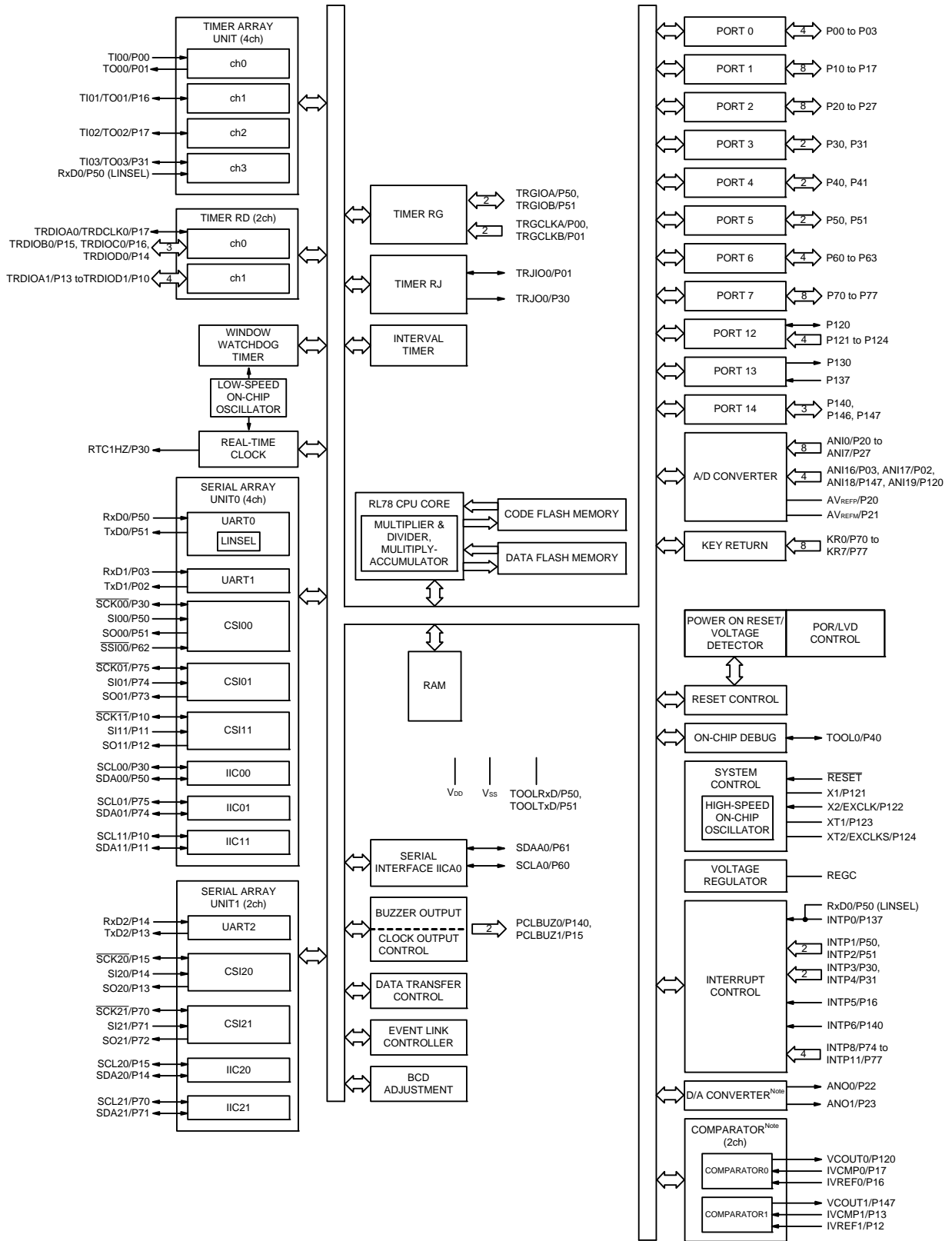
Note Mounted on the 96 KB or more code flash memory products.

1.5.6 48-pin products



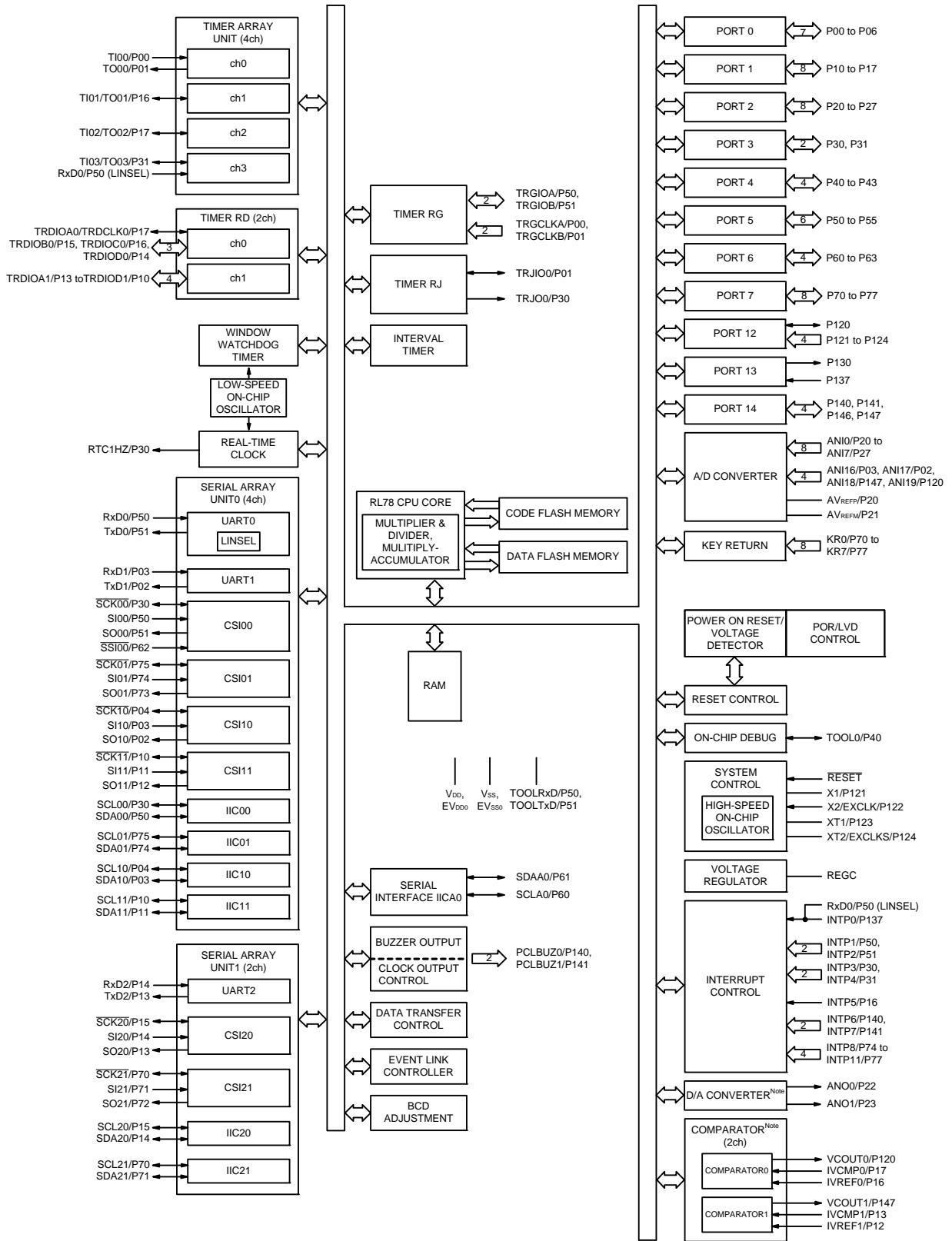
Note Mounted on the 96 KB or more code flash memory products.

1.5.7 52-pin products



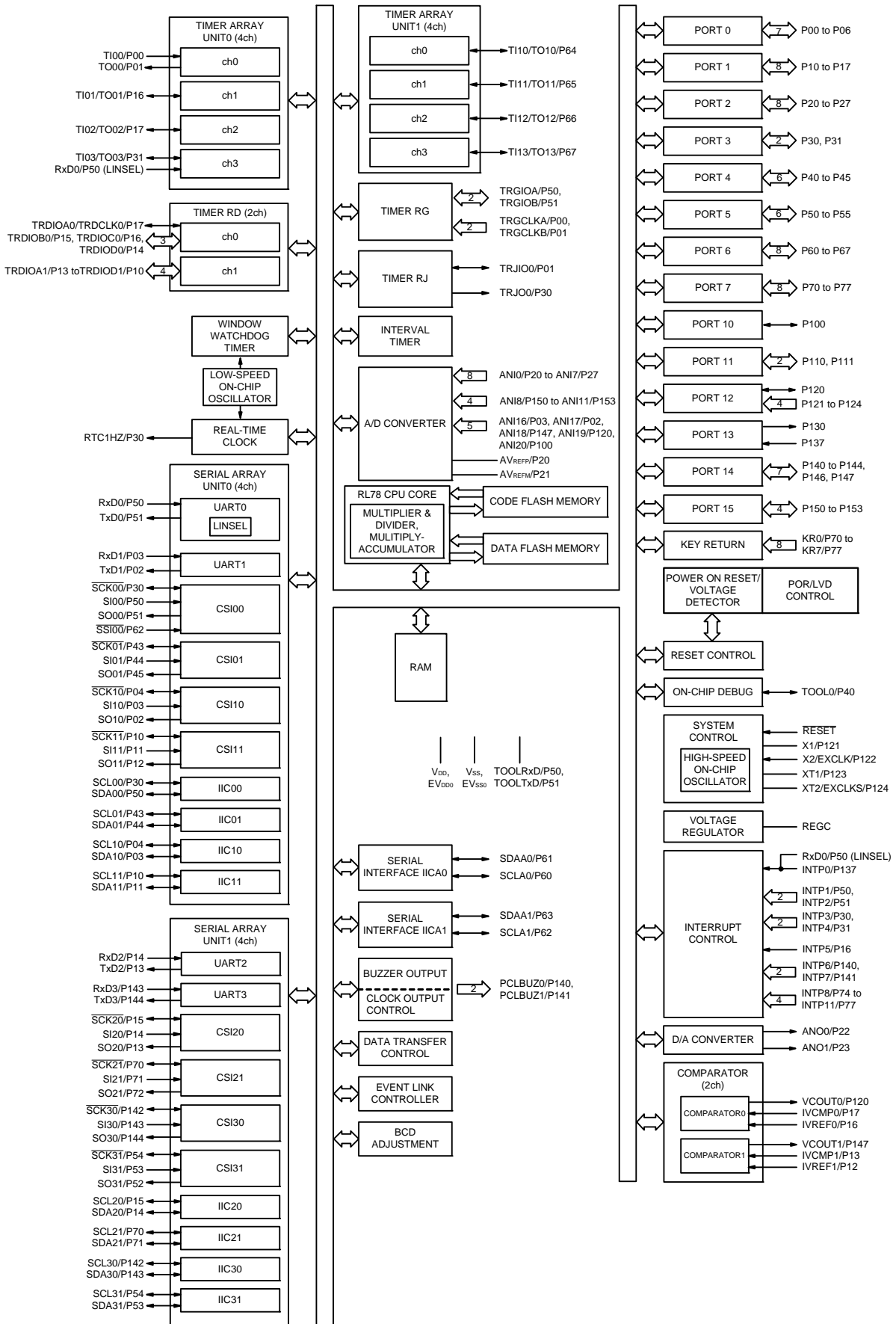
Note Mounted on the 96 KB or more code flash memory products.

1.5.8 64-pin products

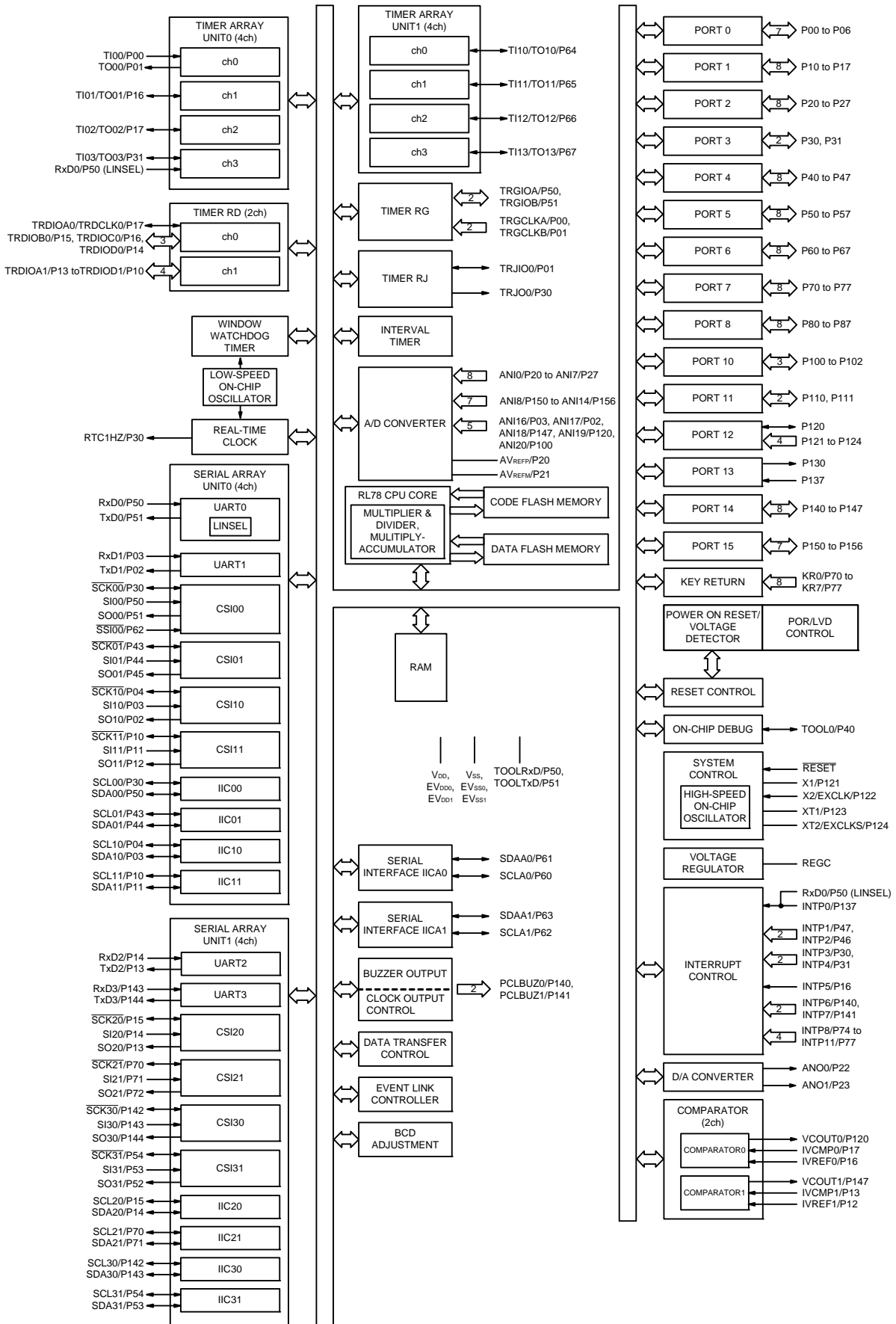


Note Mounted on the 96 KB or more code flash memory products.

1.5.9 80-pin products



1.5.10 100-pin products



1.6 Outline of Functions

[30-pin, 32-pin, 36-pin, 40-pin products (code flash memory 16 KB to 64 KB)]

Caution This outline describes the functions at the time when Peripheral I/O redirection register 0, 1 (PIOR0, 1) are set to 00H.

(1/2)

Item		30-pin	32-pin	36-pin	40-pin
		R5F104Ax (x = A, C to E)	R5F104Bx (x = A, C to E)	R5F104Cx (x = A, C to E)	R5F104Ex (x = A, C to E)
Code flash memory (KB)		16 to 64	16 to 64	16 to 64	16 to 64
Data flash memory (KB)		4	4	4	4
RAM (KB)		2.5 to 5.5 ^{Note}	2.5 to 5.5 ^{Note}	2.5 to 5.5 ^{Note}	2.5 to 5.5 ^{Note}
Memory space		1 MB			
Main system clock	High-speed system clock	X1 (crystal/ceramic) oscillation, external main system clock input (EXCLK) 1 to 20 MHz: V _{DD} = 2.7 to 5.5 V, 1 to 8 MHz: V _{DD} = 1.8 to 2.7 V, 1 to 4 MHz: V _{DD} = 1.6 to 1.8 V			
	High-speed on-chip oscillator clock (f _{IH})	High-speed operation: 1 to 32 MHz (V _{DD} = 2.7 to 5.5 V), High-speed operation: 1 to 16 MHz (V _{DD} = 2.4 to 5.5 V), Low-speed operation: 1 to 8 MHz (V _{DD} = 1.8 to 5.5 V), Low-voltage operation: 1 to 4 MHz (V _{DD} = 1.6 to 5.5 V)			
Subsystem clock		—			XT1 (crystal) oscillation 32.768 kHz (TYP.): V _{DD} = 1.6 to 5.5 V
Low-speed on-chip oscillator clock		15 kHz (TYP.): V _{DD} = 1.6 to 5.5 V			
General-purpose register		8 bits × 32 registers (8 bits × 8 registers × 4 banks)			
Minimum instruction execution time		0.03125 μs (High-speed on-chip oscillator clock: f _{IH} = 32 MHz operation)			
		0.05 μs (High-speed system clock: f _{MX} = 20 MHz operation)			
		—			30.5 μs (Subsystem clock: f _{SUB} = 32.768 kHz operation)
Instruction set		<ul style="list-style-type: none"> • Data transfer (8/16 bits) • Adder and subtractor/logical operation (8/16 bits) • Multiplication (8 bits × 8 bits, 16 bits × 16 bits), Division (16 bits ÷ 16 bits, 32 bits ÷ 32 bits) • Multiplication and Accumulation (16 bits × 16 bits + 32 bits) • Rotate, barrel shift, and bit manipulation (Set, reset, test, and Boolean operation), etc. 			
I/O port	Total	26	28	32	36
	CMOS I/O	21	22	26	28
	CMOS input	3	3	3	5
	CMOS output	—	—	—	—
	N-ch open-drain I/O (6 V tolerance)	2	3	3	3
Timer	16-bit timer	8 channels (TAU: 4 channels, Timer RJ: 1 channel, Timer RD: 2 channels, Timer RG: 1 channel)			
	Watchdog timer	1 channel			
	Real-time clock (RTC)	1 channel			
	12-bit interval timer	1 channel			
	Timer output	16 (TAU: 4, Timer RJ: 2, Timer RD: 8, Timer RG: 2) PWM outputs: 10 (TAU: 3, Timer RD: 6, Timer RG: 1)			
	RTC output	—			1 • 1 Hz (subsystem clock: f _{SUB} = 32.768 kHz)

Note In the case of the 5.5 KB, this is about 4.5 KB when the self-programming function and data flash function are used.

(2/2)

Item	30-pin	32-pin	36-pin	40-pin
	R5F104Ax (x = A, C to E)	R5F104Bx (x = A, C to E)	R5F104Cx (x = A, C to E)	R5F104Ex (x = A, C to E)
Clock output/buzzer output	2	2	2	2
	[30-pin, 32-pin, 36-pin products] • 2.44 kHz, 4.88 kHz, 9.76 kHz, 1.25 MHz, 2.5 MHz, 5 MHz, 10 MHz (Main system clock: $f_{MAIN} = 20$ MHz operation) [40-pin products] • 2.44 kHz, 4.88 kHz, 9.76 kHz, 1.25 MHz, 2.5 MHz, 5 MHz, 10 MHz (Main system clock: $f_{MAIN} = 20$ MHz operation) • 256 Hz, 512 Hz, 1.024 kHz, 2.048 kHz, 4.096 kHz, 8.192 kHz, 16.384 kHz, 32.768 kHz (Subsystem clock: $f_{SUB} = 32.768$ kHz operation)			
8/10-bit resolution A/D converter	8 channels	8 channels	8 channels	9 channels
Serial interface	[30-pin, 32-pin products] • CSI: 1 channel/UART (UART supporting LIN-bus): 1 channel/simplified I ² C: 1 channel • CSI: 1 channel/UART: 1 channel/simplified I ² C: 1 channel • CSI: 1 channel/UART: 1 channel/simplified I ² C: 1 channel [36-pin, 40-pin products] • CSI: 1 channel/UART (UART supporting LIN-bus): 1 channel/simplified I ² C: 1 channel • CSI: 1 channel/UART: 1 channel/simplified I ² C: 1 channel • CSI: 2 channels/UART: 1 channel/simplified I ² C: 2 channels			
I ² C bus	1 channel	1 channel	1 channel	1 channel
Data transfer controller (DTC)	28 sources			29 sources
Event link controller (ELC)	Event input: 20 Event trigger output: 7			
Vectored interrupt sources	Internal	24	24	24
	External	6	6	7
Key interrupt	—	—	—	4
Reset	<ul style="list-style-type: none"> • Reset by \overline{RESET} pin • Internal reset by watchdog timer • Internal reset by power-on-reset • Internal reset by voltage detector • Internal reset by illegal instruction execution ^{Note} • Internal reset by RAM parity error • Internal reset by illegal-memory access 			
Power-on-reset circuit	<ul style="list-style-type: none"> • Power-on-reset: 1.51 ±0.03 V • Power-down-reset: 1.50 ±0.03 V 			
Voltage detector	1.63 V to 4.06 V (14 stages)			
On-chip debug function	Provided			
Power supply voltage	$V_{DD} = 1.6$ to 5.5 V			
Operating ambient temperature	$T_A = -40$ to +85 °C			

Note The illegal instruction is generated when instruction code FFH is executed.
 Reset by the illegal instruction execution not is issued by emulation with the in-circuit emulator or on-chip debug emulator.

[30-pin, 32-pin, 36-pin, 40-pin products (code flash memory 96 KB to 256 KB)]

Caution This outline describes the functions at the time when Peripheral I/O redirection register 0, 1 (PIOR0, 1) are set to 00H.

(1/2)

Item		30-pin	32-pin	36-pin	40-pin
		R5F104Ax (x = F, G)	R5F104Bx (x = F, G)	R5F104Cx (x = F, G)	R5F104Ex (x = F to H)
Code flash memory (KB)		96 to 128	96 to 128	96 to 128	96 to 192
Data flash memory (KB)		8	8	8	8
RAM (KB)		12 to 16	12 to 16	12 to 16	12 to 20
Memory space		1 MB			
Main system clock	High-speed system clock	X1 (crystal/ceramic) oscillation, external main system clock input (EXCLK) 1 to 20 MHz: V _{DD} = 2.7 to 5.5 V, 1 to 8 MHz: V _{DD} = 1.8 to 2.7 V, 1 to 4 MHz: V _{DD} = 1.6 to 1.8 V			
	High-speed on-chip oscillator clock (f _{IH})	High-speed operation: 1 to 32 MHz (V _{DD} = 2.7 to 5.5 V), High-speed operation: 1 to 16 MHz (V _{DD} = 2.4 to 5.5 V), Low-speed operation: 1 to 8 MHz (V _{DD} = 1.8 to 5.5 V), Low-voltage operation: 1 to 4 MHz (V _{DD} = 1.6 to 5.5 V)			
Subsystem clock		—			XT1 (crystal) oscillation 32.768 kHz (TYP): V _{DD} = 1.6 to 5.5 V
Low-speed on-chip oscillator clock		15 kHz (TYP): V _{DD} = 1.6 to 5.5 V			
General-purpose register		8 bits × 32 registers (8 bits × 8 registers × 4 banks)			
Minimum instruction execution time		0.03125 μs (High-speed on-chip oscillator clock: f _{IH} = 32 MHz operation)			
		0.05 μs (High-speed system clock: f _{MX} = 20 MHz operation)			
		—			30.5 μs (Subsystem clock: f _{SUB} = 32.768 kHz operation)
Instruction set		<ul style="list-style-type: none"> • Data transfer (8/16 bits) • Adder and subtractor/logical operation (8/16 bits) • Multiplication (8 bits × 8 bits, 16 bits × 16 bits), Division (16 bits ÷ 16 bits, 32 bits ÷ 32 bits) • Multiplication and Accumulation (16 bits × 16 bits + 32 bits) • Rotate, barrel shift, and bit manipulation (Set, reset, test, and Boolean operation), etc. 			
I/O port	Total	26	28	32	36
	CMOS I/O	21	22	26	28
	CMOS input	3	3	3	5
	CMOS output	—	—	—	—
	N-ch open-drain I/O (6 V tolerance)	2	3	3	3
Timer	16-bit timer	8 channels (TAU: 4 channels, Timer RJ: 1 channel, Timer RD: 2 channels, Timer RG: 1 channel)			
	Watchdog timer	1 channel			
	Real-time clock (RTC)	1 channel			
	12-bit interval timer	1 channel			
	Timer output	16 (TAU: 4, Timer RJ: 2, Timer RD: 8, Timer RG: 2) PWM outputs: 10 (TAU: 3, Timer RD: 6, Timer RG: 1)			
	RTC output	—			1 • 1 Hz (subsystem clock: f _{SUB} = 32.768 kHz)

(2/2)

Item	30-pin	32-pin	36-pin	40-pin
	R5F104Ax (x = F, G)	R5F104Bx (x = F, G)	R5F104Cx (x = F, G)	R5F104Ex (x = F to H)
Clock output/buzzer output	2	2	2	2
	[30-pin, 32-pin, 36-pin products] • 2.44 kHz, 4.88 kHz, 9.76 kHz, 1.25 MHz, 2.5 MHz, 5 MHz, 10 MHz (Main system clock: $f_{MAIN} = 20$ MHz operation) [40-pin products] • 2.44 kHz, 4.88 kHz, 9.76 kHz, 1.25 MHz, 2.5 MHz, 5 MHz, 10 MHz (Main system clock: $f_{MAIN} = 20$ MHz operation) • 256 Hz, 512 Hz, 1.024 kHz, 2.048 kHz, 4.096 kHz, 8.192 kHz, 16.384 kHz, 32.768 kHz (Subsystem clock: $f_{SUB} = 32.768$ kHz operation)			
8/10-bit resolution A/D converter	8 channels	8 channels	8 channels	9 channels
D/A converter	1 channel	2 channels		
Comparator	2 channels			
Serial interface	[30-pin, 32-pin products] • CSI: 1 channel/UART (UART supporting LIN-bus): 1 channel/simplified I ² C: 1 channel • CSI: 1 channel/UART: 1 channel/simplified I ² C: 1 channel • CSI: 1 channel/UART: 1 channel/simplified I ² C: 1 channel [36-pin, 40-pin products] • CSI: 1 channel/UART (UART supporting LIN-bus): 1 channel/simplified I ² C: 1 channel • CSI: 1 channel/UART: 1 channel/simplified I ² C: 1 channel • CSI: 2 channels/UART: 1 channel/simplified I ² C: 2 channels			
	I ² C bus	1 channel	1 channel	1 channel
Data transfer controller (DTC)	28 sources			29 sources
Event link controller (ELC)	Event input: 20 Event trigger output: 7			
Vectored interrupt sources	Internal	24	24	24
	External	6	6	7
Key interrupt	—	—	—	4
Reset	<ul style="list-style-type: none"> • Reset by RESET pin • Internal reset by watchdog timer • Internal reset by power-on-reset • Internal reset by voltage detector • Internal reset by illegal instruction execution ^{Note} • Internal reset by RAM parity error • Internal reset by illegal-memory access 			
Power-on-reset circuit	<ul style="list-style-type: none"> • Power-on-reset: 1.51 ±0.03 V • Power-down-reset: 1.50 ±0.03 V 			
Voltage detector	1.63 V to 4.06 V (14 stages)			
On-chip debug function	Provided			
Power supply voltage	V _{DD} = 1.6 to 5.5 V			
Operating ambient temperature	T _A = -40 to +85 °C			

Note The illegal instruction is generated when instruction code FFH is executed.
 Reset by the illegal instruction execution not is issued by emulation with the in-circuit emulator or on-chip debug emulator.

[44-pin, 48-pin, 52-pin, 64-pin products (code flash memory 16 KB to 64 KB)]

Caution This outline describes the functions at the time when Peripheral I/O redirection register 0, 1 (PIOR0, 1) are set to 00H.

(1/2)

Item		44-pin	48-pin	52-pin	64-pin
		R5F104Fx (x = A, C to E)	R5F104Gx (x = A, C to E)	R5F104Jx (x = C to E)	R5F104Lx (x = C to E)
Code flash memory (KB)		16 to 64	16 to 64	32 to 64	32 to 64
Data flash memory (KB)		4	4	4	4
RAM (KB)		2.5 to 5.5 Note	2.5 to 5.5 Note	4 to 5.5 Note	4 to 5.5 Note
Memory space		1 MB			
Main system clock	High-speed system clock	X1 (crystal/ceramic) oscillation, external main system clock input (EXCLK) 1 to 20 MHz: V _{DD} = 2.7 to 5.5 V, 1 to 8 MHz: V _{DD} = 1.8 to 2.7 V, 1 to 4 MHz: V _{DD} = 1.6 to 1.8 V			
	High-speed on-chip oscillator clock (f _{IH})	High-speed operation: 1 to 32 MHz (V _{DD} = 2.7 to 5.5 V), High-speed operation: 1 to 16 MHz (V _{DD} = 2.4 to 5.5 V), Low-speed operation: 1 to 8 MHz (V _{DD} = 1.8 to 5.5 V), Low-voltage operation: 1 to 4 MHz (V _{DD} = 1.6 to 5.5 V)			
Subsystem clock		XT1 (crystal) oscillation 32.768 kHz (TYP.): V _{DD} = 1.6 to 5.5 V			
Low-speed on-chip oscillator clock		15 kHz (TYP.): V _{DD} = 1.6 to 5.5 V			
General-purpose register		8 bits × 32 registers (8 bits × 8 registers × 4 banks)			
Minimum instruction execution time		0.03125 μs (High-speed on-chip oscillator clock: f _{IH} = 32 MHz operation)			
		0.05 μs (High-speed system clock: f _{MX} = 20 MHz operation)			
		30.5 μs (Subsystem clock: f _{SUB} = 32.768 kHz operation)			
Instruction set		<ul style="list-style-type: none"> • Data transfer (8/16 bits) • Adder and subtractor/logical operation (8/16 bits) • Multiplication (8 bits × 8 bits, 16 bits × 16 bits), Division (16 bits ÷ 16 bits, 32 bits ÷ 32 bits) • Multiplication and Accumulation (16 bits × 16 bits + 32 bits) • Rotate, barrel shift, and bit manipulation (Set, reset, test, and Boolean operation), etc. 			
I/O port	Total	40	44	48	58
	CMOS I/O	31	34	38	48
	CMOS input	5	5	5	5
	CMOS output	—	1	1	1
	N-ch open-drain I/O (6 V tolerance)	4	4	4	4
Timer	16-bit timer	8 channels (TAU: 4 channels, Timer RJ: 1 channel, Timer RD: 2 channels, Timer RG: 1 channel)			
	Watchdog timer	1 channel			
	Real-time clock (RTC)	1 channel			
	12-bit interval timer	1 channel			
	Timer output	16 (TAU: 4, Timer RJ: 2, Timer RD: 8, Timer RG: 2) PWM outputs: 10 (TAU: 3, Timer RD: 6, Timer RG: 1)			
	RTC output	1 • 1 Hz (subsystem clock: f _{SUB} = 32.768 kHz)			

Note In the case of the 5.5 KB, this is about 4.5 KB when the self-programming function and data flash function are used.

(2/2)

Item	44-pin	48-pin	52-pin	64-pin
	R5F104Fx (x = A, C to E)	R5F104Gx (x = A, C to E)	R5F104Jx (x = C to E)	R5F104Lx (x = C to E)
Clock output/buzzer output	2	2	2	2
	<ul style="list-style-type: none"> • 2.44 kHz, 4.88 kHz, 9.76 kHz, 1.25 MHz, 2.5 MHz, 5 MHz, 10 MHz (Main system clock: f_{MAIN} = 20 MHz operation) • 256 Hz, 512 Hz, 1.024 kHz, 2.048 kHz, 4.096 kHz, 8.192 kHz, 16.384 kHz, 32.768 kHz (Subsystem clock: f_{SUB} = 32.768 kHz operation) 			
8/10-bit resolution A/D converter	10 channels	10 channels	12 channels	12 channels
Serial interface	<p>[44-pin products]</p> <ul style="list-style-type: none"> • CSI: 1 channel/UART (UART supporting LIN-bus): 1 channel/simplified I²C: 1 channel • CSI: 1 channel/UART: 1 channel/simplified I²C: 1 channel • CSI: 2 channels/UART: 1 channel/simplified I²C: 2 channels <p>[48-pin, 52-pin products]</p> <ul style="list-style-type: none"> • CSI: 2 channels/UART (UART supporting LIN-bus): 1 channel/simplified I²C: 2 channels • CSI: 1 channel/UART: 1 channel/simplified I²C: 1 channel • CSI: 2 channels/UART: 1 channel/simplified I²C: 2 channels <p>[64-pin products]</p> <ul style="list-style-type: none"> • CSI: 2 channels/UART (UART supporting LIN-bus): 1 channel/simplified I²C: 2 channels • CSI: 2 channels/UART: 1 channel/simplified I²C: 2 channels • CSI: 2 channels/UART: 1 channel/simplified I²C: 2 channels 			
	I ² C bus	1 channel	1 channel	1 channel
Data transfer controller (DTC)	29 sources	30 sources		31 sources
Event link controller (ELC)	Event input: 20 Event trigger output: 7			
Vectored interrupt sources	Internal	24	24	24
	External	7	10	12
Key interrupt	4	6	8	8
Reset	<ul style="list-style-type: none"> • Reset by $\overline{\text{RESET}}$ pin • Internal reset by watchdog timer • Internal reset by power-on-reset • Internal reset by voltage detector • Internal reset by illegal instruction execution ^{Note} • Internal reset by RAM parity error • Internal reset by illegal-memory access 			
Power-on-reset circuit	<ul style="list-style-type: none"> • Power-on-reset: 1.51 ±0.03 V • Power-down-reset: 1.50 ±0.03 V 			
Voltage detector	1.63 V to 4.06 V (14 stages)			
On-chip debug function	Provided			
Power supply voltage	V _{DD} = 1.6 to 5.5 V			
Operating ambient temperature	T _A = -40 to +85 °C			

Note The illegal instruction is generated when instruction code FFH is executed.
Reset by the illegal instruction execution is not issued by emulation with the in-circuit emulator or on-chip debug emulator.

[44-pin, 48-pin, 52-pin, 64-pin products (code flash memory 96 KB to 256 KB)]

Caution This outline describes the functions at the time when Peripheral I/O redirection register 0, 1 (PIOR0, 1) are set to 00H.

(1/2)

Item		44-pin	48-pin	52-pin	64-pin
		R5F104Fx (x = F to H, J)	R5F104Gx (x = F to H, J)	R5F104Jx (x = F to H, J)	R5F104Lx (x = F to H, J)
Code flash memory (KB)		96 to 256	96 to 256	96 to 256	96 to 256
Data flash memory (KB)		8	8	8	8
RAM (KB)		12 to 24 Note	12 to 24 Note	12 to 24 Note	12 to 24 Note
Memory space		1 MB			
Main system clock	High-speed system clock	X1 (crystal/ceramic) oscillation, external main system clock input (EXCLK) 1 to 20 MHz: V _{DD} = 2.7 to 5.5 V, 1 to 8 MHz: V _{DD} = 1.8 to 2.7 V, 1 to 4 MHz: V _{DD} = 1.6 to 1.8 V			
	High-speed on-chip oscillator clock (f _{IH})	High-speed operation: 1 to 32 MHz (V _{DD} = 2.7 to 5.5 V), High-speed operation: 1 to 16 MHz (V _{DD} = 2.4 to 5.5 V), Low-speed operation: 1 to 8 MHz (V _{DD} = 1.8 to 5.5 V), Low-voltage operation: 1 to 4 MHz (V _{DD} = 1.6 to 5.5 V)			
Subsystem clock		XT1 (crystal) oscillation 32.768 kHz (TYP.): V _{DD} = 1.6 to 5.5 V			
Low-speed on-chip oscillator clock		15 kHz (TYP.): V _{DD} = 1.6 to 5.5 V			
General-purpose register		8 bits × 32 registers (8 bits × 8 registers × 4 banks)			
Minimum instruction execution time		0.03125 μs (High-speed on-chip oscillator clock: f _{IH} = 32 MHz operation)			
		0.05 μs (High-speed system clock: f _{MX} = 20 MHz operation)			
		30.5 μs (Subsystem clock: f _{SUB} = 32.768 kHz operation)			
Instruction set		<ul style="list-style-type: none"> • Data transfer (8/16 bits) • Adder and subtractor/logical operation (8/16 bits) • Multiplication (8 bits × 8 bits, 16 bits × 16 bits), Division (16 bits ÷ 16 bits, 32 bits ÷ 32 bits) • Multiplication and Accumulation (16 bits × 16 bits + 32 bits) • Rotate, barrel shift, and bit manipulation (Set, reset, test, and Boolean operation), etc. 			
I/O port	Total	40	44	48	58
	CMOS I/O	31	34	38	48
	CMOS input	5	5	5	5
	CMOS output	—	1	1	1
	N-ch open-drain I/O (6 V tolerance)	4	4	4	4
Timer	16-bit timer	8 channels (TAU: 4 channels, Timer RJ: 1 channel, Timer RD: 2 channels, Timer RG: 1 channel)			
	Watchdog timer	1 channel			
	Real-time clock (RTC)	1 channel			
	12-bit interval timer	1 channel			
	Timer output	16 (TAU: 4, Timer RJ: 2, Timer RD: 8, Timer RG: 2) PWM outputs: 10 (TAU: 3, Timer RD: 6, Timer RG: 1)			
	RTC output	1 • 1 Hz (subsystem clock: f _{SUB} = 32.768 kHz)			

Note In the case of the 24 KB, this is about 23 KB when the self-programming function and data flash function are used.

(2/2)

Item	44-pin	48-pin	52-pin	64-pin	
	R5F104Fx (x = F to H, J)	R5F104Gx (x = F to H, J)	R5F104Jx (x = F to H, J)	R5F104Lx (x = F to H, J)	
Clock output/buzzer output	2	2	2	2	
	<ul style="list-style-type: none"> • 2.44 kHz, 4.88 kHz, 9.76 kHz, 1.25 MHz, 2.5 MHz, 5 MHz, 10 MHz (Main system clock: f_{MAIN} = 20 MHz operation) • 256 Hz, 512 Hz, 1.024 kHz, 2.048 kHz, 4.096 kHz, 8.192 kHz, 16.384 kHz, 32.768 kHz (Subsystem clock: f_{SUB} = 32.768 kHz operation) 				
8/10-bit resolution A/D converter	10 channels	10 channels	12 channels	12 channels	
D/A converter	2 channels				
Comparator	2 channels				
Serial interface	[44-pin products] <ul style="list-style-type: none"> • CSI: 1 channel/UART (UART supporting LIN-bus): 1 channel/simplified I²C: 1 channel • CSI: 1 channel/UART: 1 channel/simplified I²C: 1 channel • CSI: 2 channels/UART: 1 channel/simplified I²C: 2 channels [48-pin, 52-pin products] <ul style="list-style-type: none"> • CSI: 2 channels/UART (UART supporting LIN-bus): 1 channel/simplified I²C: 2 channels • CSI: 1 channel/UART: 1 channel/simplified I²C: 1 channel • CSI: 2 channels/UART: 1 channel/simplified I²C: 2 channels [64-pin products] <ul style="list-style-type: none"> • CSI: 2 channels/UART (UART supporting LIN-bus): 1 channel/simplified I²C: 2 channels • CSI: 2 channels/UART: 1 channel/simplified I²C: 2 channels • CSI: 2 channels/UART: 1 channel/simplified I²C: 2 channels 				
	I ² C bus	1 channel	1 channel	1 channel	1 channel
Data transfer controller (DTC)	29 sources	30 sources		31 sources	
Event link controller (ELC)	Event input: 20 Event trigger output: 7				
Vectored interrupt sources	Internal	24	24	24	24
	External	7	10	12	13
Key interrupt	4	6	8	8	
Reset	<ul style="list-style-type: none"> • Reset by <u>RESET</u> pin • Internal reset by watchdog timer • Internal reset by power-on-reset • Internal reset by voltage detector • Internal reset by illegal instruction execution ^{Note} • Internal reset by RAM parity error • Internal reset by illegal-memory access 				
Power-on-reset circuit	<ul style="list-style-type: none"> • Power-on-reset: 1.51 ±0.03 V • Power-down-reset: 1.50 ±0.03 V 				
Voltage detector	1.63 V to 4.06 V (14 stages)				
On-chip debug function	Provided				
Power supply voltage	V _{DD} = 1.6 to 5.5 V				
Operating ambient temperature	T _A = -40 to +85 °C				

Note The illegal instruction is generated when instruction code FFH is executed.
Reset by the illegal instruction execution is not issued by emulation with the in-circuit emulator or on-chip debug emulator.

[80-pin, 100-pin products (code flash memory 96 KB to 256 KB)]

Caution This outline describes the functions at the time when Peripheral I/O redirection register 0, 1 (PIOR0, 1) are set to 00H.

(1/2)

Item		80-pin	100-pin
		R5F104Mx (x = F to H, J)	R5F104Px (x = F to H, J)
Code flash memory (KB)		96 to 256	96 to 256
Data flash memory (KB)		8	8
RAM (KB)		12 to 24 Note	12 to 24 Note
Memory space		1 MB	
Main system clock	High-speed system clock	X1 (crystal/ceramic) oscillation, external main system clock input (EXCLK) 1 to 20 MHz: $V_{DD} = 2.7$ to 5.5 V, 1 to 8 MHz: $V_{DD} = 1.8$ to 2.7 V, 1 to 4 MHz: $V_{DD} = 1.6$ to 1.8 V	
	High-speed on-chip oscillator clock (f_{IH})	High-speed operation: 1 to 32 MHz ($V_{DD} = 2.7$ to 5.5 V), High-speed operation: 1 to 16 MHz ($V_{DD} = 2.4$ to 5.5 V), Low-speed operation: 1 to 8 MHz ($V_{DD} = 1.8$ to 5.5 V), Low-voltage operation: 1 to 4 MHz ($V_{DD} = 1.6$ to 5.5 V)	
Subsystem clock		XT1 (crystal) oscillation 32.768 kHz (TYP.): $V_{DD} = 1.6$ to 5.5 V	
Low-speed on-chip oscillator clock		15 kHz (TYP.): $V_{DD} = 1.6$ to 5.5 V	
General-purpose register		8 bits \times 32 registers (8 bits \times 8 registers \times 4 banks)	
Minimum instruction execution time		0.03125 μ s (High-speed on-chip oscillator clock: $f_{IH} = 32$ MHz operation)	
		0.05 μ s (High-speed system clock: $f_{MX} = 20$ MHz operation)	
		30.5 μ s (Subsystem clock: $f_{SUB} = 32.768$ kHz operation)	
Instruction set		<ul style="list-style-type: none"> • Data transfer (8/16 bits) • Adder and subtractor/logical operation (8/16 bits) • Multiplication (8 bits \times 8 bits, 16 bits \times 16 bits), Division (16 bits \div 16 bits, 32 bits \div 32 bits) • Multiplication and Accumulation (16 bits \times 16 bits + 32 bits) • Rotate, barrel shift, and bit manipulation (Set, reset, test, and Boolean operation), etc. 	
I/O port	Total	74	92
	CMOS I/O	64	82
	CMOS input	5	5
	CMOS output	1	1
	N-ch open-drain I/O (6 V tolerance)	4	4
Timer	16-bit timer	12 channels (TAU: 8 channels, Timer RJ: 1 channel, Timer RD: 2 channels, Timer RG: 1 channel)	
	Watchdog timer	1 channel	
	Real-time clock (RTC)	1 channel	
	12-bit interval timer	1 channel	
	Timer output	20 (TAU: 8, Timer RJ: 2, Timer RD: 8, Timer RG: 2) PWM outputs: 13 (TAU: 6, Timer RD: 6, Timer RG: 1)	
	RTC output	1 • 1 Hz (subsystem clock: $f_{SUB} = 32.768$ kHz)	

Note In the case of the 24 KB, this is about 23 KB when the self-programming function and data flash function are used.

(2/2)

Item	80-pin		100-pin	
	R5F104Mx (x = F to H, J)		R5F104Px (x = F to H, J)	
Clock output/buzzer output	2		2	
	<ul style="list-style-type: none"> • 2.44 kHz, 4.88 kHz, 9.76 kHz, 1.25 MHz, 2.5 MHz, 5 MHz, 10 MHz (Main system clock: f_{MAIN} = 20 MHz operation) • 256 Hz, 512 Hz, 1.024 kHz, 2.048 kHz, 4.096 kHz, 8.192 kHz, 16.384 kHz, 32.768 kHz (Subsystem clock: f_{SUB} = 32.768 kHz operation) 			
8/10-bit resolution A/D converter	17 channels		20 channels	
D/A converter	2 channels		2 channels	
Comparator	2 channels		2 channels	
Serial interface	[80-pin, 100-pin products]			
	<ul style="list-style-type: none"> • CSI: 2 channels/UART (UART supporting LIN-bus): 1 channel/simplified I²C: 2 channels • CSI: 2 channels/UART: 1 channel/simplified I²C: 2 channels • CSI: 2 channels/UART: 1 channel/simplified I²C: 2 channels • CSI: 2 channels/UART: 1 channel/simplified I²C: 2 channels 			
I ² C bus	2 channels		2 channels	
Data transfer controller (DTC)	39 sources		39 sources	
Event link controller (ELC)	Event input: 26 Event trigger output: 9			
Vectored interrupt sources	Internal	32		32
	External	13		13
Key interrupt	8		8	
Reset	<ul style="list-style-type: none"> • Reset by $\overline{\text{RESET}}$ pin • Internal reset by watchdog timer • Internal reset by power-on-reset • Internal reset by voltage detector • Internal reset by illegal instruction execution ^{Note} • Internal reset by RAM parity error • Internal reset by illegal-memory access 			
Power-on-reset circuit	<ul style="list-style-type: none"> • Power-on-reset: 1.51 ±0.03 V • Power-down-reset: 1.50 ±0.03 V 			
Voltage detector	1.63 V to 4.06 V (14 stages)			
On-chip debug function	Provided			
Power supply voltage	V _{DD} = 1.6 to 5.5 V			
Operating ambient temperature	T _A = -40 to +85 °C			

Note The illegal instruction is generated when instruction code FFH is executed.
Reset by the illegal instruction execution is not issued by emulation with the in-circuit emulator or on-chip debug emulator.

2. ELECTRICAL SPECIFICATIONS

Caution 1. The RL78/G14 has an on-chip debug function, which is provided for development and evaluation. Do not use the on-chip debug function in products designated for mass production, because the guaranteed number of rewritable times of the flash memory may be exceeded when this function is used, and product reliability therefore cannot be guaranteed. Renesas Electronics is not liable for problems occurring when the on-chip debug function is used.

Caution 2. The pins mounted depend on the product. Refer to 1.3.1 30-pin products to 1.3.10 100-pin products.

Caution The pins mounted depend on the product. Refer to 1.3.1 30-pin products to 1.3.10 100-pin products.

2.1 Absolute Maximum Ratings

Absolute Maximum Ratings (TA = 25 °C) (1/2)

(1/2)

Parameter	Symbols	Conditions	Ratings	Unit
Supply voltage	V _{DD}		-0.5 to +6.5	V
	EV _{DD0} , EV _{DD1}	EV _{DD0} = EV _{DD1}	-0.5 to +6.5	V
	V _{SS}		-0.5 to +0.3	V
	EV _{SS0} , EV _{SS1}	EV _{SS0} = EV _{SS1}	-0.5 to +0.3	V
REGC pin input voltage	V _I REGC	REGC	-0.3 to +2.8 and -0.3 to V _{DD} +0.3 Note 1	V
Input voltage	V _{I1}	P00 to P06, P10 to P17, P30, P31, P40 to P47, P50 to P57, P64 to P67, P70 to P77, P80 to P87, P100 to P102, P110, P111, P120, P140 to P147	-0.3 to EV _{DD0} +0.3 and -0.3 to V _{DD} +0.3 Note 2	V
	V _{I2}	P60 to P63 (N-ch open-drain)	-0.3 to +6.5	V
	V _{I3}	P20 to P27, P121 to P124, P137, P150 to P156, EXCLK, EXCLKS, $\overline{\text{RESET}}$	-0.3 to V _{DD} +0.3 Note 2	V
Output voltage	V _{O1}	P00 to P06, P10 to P17, P30, P31, P40 to P47, P50 to P57, P60 to P67, P70 to P77, P80 to P87, P100 to P102, P110, P111, P120, P130, P140 to P147	-0.3 to EV _{DD0} +0.3 Note 2	V
	V _{O2}	P20 to P27, P150 to P156	-0.3 to V _{DD} +0.3	V
Analog input voltage	V _{AI1}	ANI16 to ANI20	-0.3 to EV _{DD0} +0.3 Note 2	V
	V _{AI2}	ANI0 to ANI14	-0.3 to V _{DD} +0.3 Note 2	V

Note 1. Connect the REGC pin to V_{SS} via a capacitor (0.47 to 1 μF). This value regulates the absolute maximum rating of the REGC pin. Do not use this pin with voltage applied to it.

Note 2. Must be 6.5 V or lower.

Caution Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

Caution The pins mounted depend on the product. Refer to 1.3.1 30-pin products to 1.3.10 100-pin products.

Absolute Maximum Ratings (TA = 25 °C) (2/2)

(2/2)

Parameter	Symbols	Conditions		Ratings	Unit
Output current, high	IOH1	Per pin	P00 to P06, P10 to P17, P30, P31, P40 to P47, P50 to P57, P64 to P67, P70 to P77, P80 to P87, P100 to P102, P110, P111, P120, P130, P140 to P147	-40	mA
		Total of all pins	P00 to P04, P40 to P47, P102, P120, P130, P140 to P145	-70	mA
		-170 mA	P05, P06, P10 to P17, P30, P31, P50 to P57, P64 to P67, P70 to P77, P80 to P87, P100, P101, P110, P111, P146, P147	-100	mA
	IOH2	Per pin	P20 to P27, P150 to P156	-0.5	mA
		Total of all pins		-2	mA
	Output current, low	IOL1	Per pin	P00 to P06, P10 to P17, P30, P31, P40 to P47, P50 to P57, P64 to P67, P70 to P77, P80 to P87, P100 to P102, P110, P111, P120, P130, P140 to P147	40
Total of all pins			P00 to P04, P40 to P47, P102, P120, P130, P140 to P145	70	mA
170 mA			P05, P06, P10 to P17, P30, P31, P50 to P57, P60 to P67, P70 to P77, P80 to P87, P100, P101, P110, P111, P146, P147	100	mA
IOL2		Per pin	P20 to P27, P150 to P156	1	mA
		Total of all pins		5	mA
Operating ambient temperature		TA	In normal operation mode		-40 to +85
	In flash memory programming mode				
Storage temperature	Tstg			-65 to +150	°C

Caution Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

Caution The pins mounted depend on the product. Refer to 1.3.1 30-pin products to 1.3.10 100-pin products.

2.2 Oscillator Characteristics

2.2.1 Main system clock oscillator characteristics

($T_A = -40$ to $+85$ °C, $1.6\text{ V} \leq EV_{DD0} = EV_{DD1} \leq V_{DD} \leq 5.5\text{ V}$, $V_{SS} = EV_{SS0} = EV_{SS1} = 0\text{ V}$)

Resonator	Recommended Circuit	Parameter	Conditions	MIN.	TYP.	MAX.	Unit
Ceramic resonator		X1 clock oscillation frequency (fx) Note	$2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	1.0		20.0	MHz
			$1.8\text{ V} \leq V_{DD} < 2.7\text{ V}$	1.0		8.0	
			$1.6\text{ V} \leq V_{DD} < 1.8\text{ V}$	1.0		4.0	
Crystal resonator		X1 clock oscillation frequency (fx) Note	$2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	1.0		20.0	MHz
			$1.8\text{ V} \leq V_{DD} < 2.7\text{ V}$	1.0		8.0	
			$1.6\text{ V} \leq V_{DD} < 1.8\text{ V}$	1.0		4.0	

Note Indicates only oscillator characteristics. Refer to AC Characteristics for instruction execution time.

Caution 1. When using the X1 oscillator, wire as follows in the area enclosed by the broken lines in the above figures to avoid an adverse effect from wiring capacitance.

- Keep the wiring length as short as possible.
- Do not cross the wiring with the other signal lines.
- Do not route the wiring near a signal line through which a high fluctuating current flows.
- Always make the ground point of the oscillator capacitor the same potential as Vss.
- Do not ground the capacitor to a ground pattern through which a high current flows.
- Do not fetch signals from the oscillator.

Caution 2. Since the CPU is started by the high-speed on-chip oscillator clock after a reset release, check the X1 clock oscillation stabilization time using the oscillation stabilization time counter status register (OSTC) by the user. Determine the oscillation stabilization time of the OSTC register and the oscillation stabilization time select register (OSTS) after sufficiently evaluating the oscillation stabilization time with the resonator to be used.

Caution The pins mounted depend on the product. Refer to 1.3.1 30-pin products to 1.3.10 100-pin products.

2.2.2 On-chip oscillator characteristics

($T_A = -40$ to $+85$ °C, $1.6\text{ V} \leq EV_{DD0} = EV_{DD1} \leq V_{DD} \leq 5.5\text{ V}$, $V_{SS} = EV_{SS0} = EV_{SS1} = 0\text{ V}$)

Oscillators	Parameters	Conditions		MIN.	TYP.	MAX.	Unit
High-speed on-chip oscillator clock frequency ^{Note 1}	f _{IH}			1		32	MHz
High-speed on-chip oscillator clock frequency accuracy ^{Note 2}		-20 to +85 °C	$1.8\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	-1		+1	%
			$1.6\text{ V} \leq V_{DD} \leq 1.8\text{ V}$	-5		+5	%
		-40 to -20 °C	$1.8\text{ V} \leq V_{DD} < 5.5\text{ V}$	-1.5		+1.5	%
			$1.6\text{ V} \leq V_{DD} \leq 1.8\text{ V}$	-5.5		+5.5	%
Low-speed on-chip oscillator clock frequency	f _{IL}				15		kHz
Low-speed on-chip oscillator clock frequency accuracy				-15		+15	%

Note 1. High-speed on-chip oscillator frequency is selected with bits 0 to 4 of the option byte (000C2H/010C2H) and bits 0 to 2 of the HOCODIV register.

Note 2. This only indicates the oscillator characteristics. Refer to AC Characteristics for instruction execution time.
When SSOP (30-pin), WQFN (32-, 40-, 48-pin), FLGA (36-pin), LQFP (7 × 7) (48-pin), LQFP (10 × 10) (52-pin), LQFP (12 × 12) (64-, 80-pin), LQFP (14 × 14) (80-, 100-pin), LQFP (14 × 20) (100-pin) products, these specifications show target values, which may change after device evaluation.

2.2.3 Subsystem clock oscillator characteristics

($T_A = -40$ to $+85$ °C, $1.6\text{ V} \leq EV_{DD0} = EV_{DD1} \leq 5.5\text{ V}$, $V_{SS} = EV_{SS0} = EV_{SS1} = 0\text{ V}$)

Resonator	Recommended Circuit	Items	Conditions	MIN.	TYP.	MAX.	Unit
Crystal resonator		XT1 clock oscillation frequency (f_{XT}) Note		32	32.768	35	kHz

Note Indicates only oscillator characteristics. Refer to **AC Characteristics** for instruction execution time.

Caution 1. When using the XT1 oscillator, wire as follows in the area enclosed by the broken lines in the above figures to avoid an adverse effect from wiring capacitance.

- Keep the wiring length as short as possible.
- Do not cross the wiring with the other signal lines.
- Do not route the wiring near a signal line through which a high fluctuating current flows.
- Always make the ground point of the oscillator capacitor the same potential as Vss.
- Do not ground the capacitor to a ground pattern through which a high current flows.
- Do not fetch signals from the oscillator.

Caution 2. The XT1 oscillator is designed as a low-amplitude circuit for reducing power consumption, and is more prone to malfunction due to noise than the X1 oscillator. Particular care is therefore required with the wiring method when the XT1 clock is used.

Remark For the resonator selection and oscillator constant, customers are requested to either evaluate the oscillation themselves or apply to the resonator manufacturer for evaluation.

Caution The pins mounted depend on the product. Refer to 1.3.1 30-pin products to 1.3.10 100-pin products.

2.3 DC Characteristics

2.3.1 Pin characteristics

($T_A = -40$ to $+85$ °C, $1.6\text{ V} \leq EV_{DD0} = EV_{DD1} \leq V_{DD} \leq 5.5\text{ V}$, $V_{SS} = EV_{SS0} = EV_{SS1} = 0\text{ V}$)

Items	Symbol	Conditions	MIN.	TYP.	MAX.	Unit	
Output current, high ^{Note 1}	IOH1	Per pin for P00 to P06, P10 to P17, P30, P31, P40 to P47, P50 to P57, P64 to P67, P70 to P77, P80 to P87, P100 to P102, P110, P111, P120, P130, P140 to P147	$1.6\text{ V} \leq EV_{DD0} \leq 5.5\text{ V}$			-10.0 ^{Note 2}	mA
		Total of P00 to P04, P40 to P47, P102, P120, P130, P140 to P145 (When duty = 70% ^{Note 3})	$4.0\text{ V} \leq EV_{DD0} \leq 5.5\text{ V}$			-55.0	mA
			$2.7\text{ V} \leq EV_{DD0} < 4.0\text{ V}$			-10.0	mA
			$1.8\text{ V} \leq EV_{DD0} < 2.7\text{ V}$			-5.0	mA
			$1.6\text{ V} \leq EV_{DD0} < 1.8\text{ V}$			-2.5	mA
		Total of P05, P06, P10 to P17, P30, P31, P50 to P57, P64 to P67, P70 to P77, P80 to P87, P100, P101, P110, P111, P146, P147 (When duty = 70% ^{Note 3})	$4.0\text{ V} \leq EV_{DD0} \leq 5.5\text{ V}$			-80.0	mA
			$2.7\text{ V} \leq EV_{DD0} < 4.0\text{ V}$			-19.0	mA
			$1.8\text{ V} \leq EV_{DD0} < 2.7\text{ V}$			-10.0	mA
			$1.6\text{ V} \leq EV_{DD0} < 1.8\text{ V}$			-5.0	mA
	Total of all pins (When duty = 70% ^{Note 3})	$1.6\text{ V} \leq EV_{DD0} \leq 5.5\text{ V}$			-135.0 ^{Note 4}	mA	
	IOH2	Per pin for P20 to P27, P150 to P156	$1.6\text{ V} \leq V_{DD} \leq 5.5\text{ V}$			-0.1 ^{Note 2}	mA
Total of all pins (When duty = 70% ^{Note 3})			$1.6\text{ V} \leq V_{DD} \leq 5.5\text{ V}$			-1.5	mA

Note 1. Value of current at which the device operation is guaranteed even if the current flows from the EV_{DD0} , EV_{DD1} , V_{DD} pins to an output pin.

Note 2. However, do not exceed the total current value.

Note 3. Specification under conditions where the duty factor is 70%.

The output current value that has changed the duty ratio can be calculated with the following expression (when changing the duty factor from 70 % to n %).

- Total output current of pins = $(I_{OH} \times 0.7)/(n \times 0.01)$

<Example> Where n = 50 % and $I_{OH} = -10.0\text{ mA}$

$$\text{Total output current of pins} = (-10.0 \times 0.7)/(50 \times 0.01) = -14.0\text{ mA}$$

However, the current that is allowed to flow into one pin does not vary depending on the duty factor. A current higher than the absolute maximum rating must not flow into one pin.

Note 4. The applied current for the products of industrial application (R5F104xxDxx) is -100 mA.

Caution P00, P02 to P04, P10, P11, P13 to P15, P17, P30, P43 to P45, P50 to P55, P71, P74, P80 to P82, and P142 to P144 do not output high level in N-ch open-drain mode.

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

Caution The pins mounted depend on the product. Refer to 1.3.1 30-pin products to 1.3.10 100-pin products.

($T_A = -40$ to $+85$ °C, $1.6\text{ V} \leq EV_{DD0} = EV_{DD1} \leq V_{DD} \leq 5.5\text{ V}$, $V_{SS} = EV_{SS0} = EV_{SS1} = 0\text{ V}$)

Items	Symbol	Conditions	MIN.	TYP.	MAX.	Unit		
Output current, low ^{Note 1}	IOL1	Per pin for P00 to P06, P10 to P17, P30, P31, P40 to P47, P50 to P57, P64 to P67, P70 to P77, P80 to P87, P100 to P102, P110, P111, P120, P130, P140 to P147			20.0 Note 2	mA		
			Per pin for P60 to P63			15.0 Note 2	mA	
				Total of P00 to P04, P40 to P47, P102, P120, P130, P140 to P145 (When duty = 70% ^{Note 3})	$4.0\text{ V} \leq EV_{DD0} \leq 5.5\text{ V}$		70.0	mA
					$2.7\text{ V} \leq EV_{DD0} < 4.0\text{ V}$		15.0	mA
		$1.8\text{ V} \leq EV_{DD0} < 2.7\text{ V}$			9.0	mA		
		$1.6\text{ V} \leq EV_{DD0} < 1.8\text{ V}$			4.5	mA		
		Total of P05, P06, P10 to P17, P30, P31, P50 to P57, P60 to P67, P70 to P77, P80 to P87, P100, P101, P110, P111, P146, P147 (When duty = 70% ^{Note 3})	$4.0\text{ V} \leq EV_{DD0} \leq 5.5\text{ V}$		80.0	mA		
			$2.7\text{ V} \leq EV_{DD0} < 4.0\text{ V}$		35.0	mA		
			$1.8\text{ V} \leq EV_{DD0} < 2.7\text{ V}$		20.0	mA		
			$1.6\text{ V} \leq EV_{DD0} < 1.8\text{ V}$		10.0	mA		
	Total of all pins (When duty = 70% ^{Note 3})				150.0	mA		
	IOL2	Per pin for P20 to P27, P150 to P156			0.4 Note 2	mA		
			Total of all pins (When duty = 70% ^{Note 3})	$1.6\text{ V} \leq V_{DD} \leq 5.5\text{ V}$		5.0	mA	

Note 1. Value of current at which the device operation is guaranteed even if the current flows from an output pin to the EV_{SS0} , EV_{SS1} , and V_{SS} pins.

Note 2. However, do not exceed the total current value.

Note 3. Specification under conditions where the duty factor is 70 %.

The output current value that has changed the duty ratio can be calculated with the following expression (when changing the duty factor from 70 % to n %).

- Total output current of pins = $(I_{OL} \times 0.7)/(n \times 0.01)$

<Example> Where $n = 50\%$ and $I_{OL} = 10.0\text{ mA}$

$$\text{Total output current of pins} = (10.0 \times 0.7)/(50 \times 0.01) = 14.0\text{ mA}$$

However, the current that is allowed to flow into one pin does not vary depending on the duty factor. A current higher than the absolute maximum rating must not flow into one pin.

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

Caution The pins mounted depend on the product. Refer to 1.3.1 30-pin products to 1.3.10 100-pin products.

($T_A = -40$ to $+85$ °C, $1.6\text{ V} \leq EV_{DD0} = EV_{DD1} \leq V_{DD} \leq 5.5\text{ V}$, $V_{SS} = EV_{SS0} = EV_{SS1} = 0\text{ V}$)

Items	Symbol	Conditions	MIN.	TYP.	MAX.	Unit	
Input voltage, high	V_{IH1}	P00 to P06, P10 to P17, P30, P31, P40 to P47, P50 to P57, P64 to P67, P70 to P77, P80 to P87, P100 to P102, P110, P111, P120, P140 to P147	Normal input buffer	0.8 EV_{DD0}		EV_{DD0}	V
	V_{IH2}	P01, P03, P04, P10, P14 to P17, P30, P31, P43, P44, P50, P53 to P55, P80, P81, P142, P143	TTL input buffer $4.0\text{ V} \leq EV_{DD0} \leq 5.5\text{ V}$	2.2		EV_{DD0}	V
			TTL input buffer $3.3\text{ V} \leq EV_{DD0} < 4.0\text{ V}$	2.0		EV_{DD0}	V
			TTL input buffer $1.6\text{ V} \leq EV_{DD0} < 3.3\text{ V}$	1.50		EV_{DD0}	V
	V_{IH3}	P20 to P27, P150 to P156		0.7 V_{DD}		V_{DD}	V
	V_{IH4}	P60 to P63		0.7 EV_{DD0}		6.0	V
V_{IH5}	P121 to P124, P137, EXCLK, EXCLKS, $\overline{\text{RESET}}$		0.8 V_{DD}		V_{DD}	V	
Input voltage, low	V_{IL1}	P00 to P06, P10 to P17, P30, P31, P40 to P47, P50 to P57, P64 to P67, P70 to P77, P80 to P87, P100 to P102, P110, P111, P120, P140 to P147	Normal input buffer	0		0.2 EV_{DD0}	V
	V_{IL2}	P01, P03, P04, P10, P14 to P17, P30, P31, P43, P44, P50, P53 to P55, P80, P81, P142, P143	TTL input buffer $4.0\text{ V} \leq EV_{DD0} \leq 5.5\text{ V}$	0		0.8	V
			TTL input buffer $2.7\text{ V} \leq EV_{DD0} < 4.0\text{ V}$	0		0.5	V
			TTL input buffer $1.6\text{ V} \leq EV_{DD0} < 2.7\text{ V}$	0		0.32	V
	V_{IL3}	P20 to P27, P150 to P156		0		0.3 V_{DD}	V
	V_{IL4}	P60 to P63		0		0.3 EV_{DD0}	V
V_{IL5}	P121 to P124, P137, EXCLK, EXCLKS, $\overline{\text{RESET}}$		0		0.2 V_{DD}	V	

Caution The maximum value of V_{IH} of pins P00, P02 to P04, P10, P11, P13 to P15, P17, P30, P43 to P45, P50 to P55, P71, P74, P80 to P82, and P142 to P144 is EV_{DD0} , even in the N-ch open-drain mode.

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

Caution The pins mounted depend on the product. Refer to 1.3.1 30-pin products to 1.3.10 100-pin products.

($T_A = -40$ to $+85$ °C, $1.6\text{ V} \leq EV_{DD0} = EV_{DD1} \leq V_{DD} \leq 5.5\text{ V}$, $V_{SS} = EV_{SS0} = EV_{SS1} = 0\text{ V}$)

Items	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Output voltage, high	VOH1	P00 to P06, P10 to P17, P30, P31, P40 to P47, P50 to P57, P64 to P67, P70 to P77, P80 to P87, P100 to P102, P110, P111, P120, P130, P140 to P147	$4.0\text{ V} \leq EV_{DD0} \leq 5.5\text{ V}$, $I_{OH1} = -10.0\text{ mA}$			V
			$4.0\text{ V} \leq EV_{DD0} \leq 5.5\text{ V}$, $I_{OH1} = -3.0\text{ mA}$			V
			$1.8\text{ V} \leq EV_{DD0} \leq 5.5\text{ V}$, $I_{OH1} = -1.5\text{ mA}$			V
			$1.6\text{ V} \leq EV_{DD0} < 1.8\text{ V}$, $I_{OH1} = -1.0\text{ mA}$			V
	VOH2	P20 to P27, P150 to P156	$1.6\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, $I_{OH2} = -100\text{ }\mu\text{A}$			V
Output voltage, low	VOL1	P00 to P06, P10 to P17, P30, P31, P40 to P47, P50 to P57, P64 to P67, P70 to P77, P80 to P87, P100 to P102, P110, P111, P120, P130, P140 to P147	$4.0\text{ V} \leq EV_{DD0} \leq 5.5\text{ V}$, $I_{OL1} = 20.0\text{ mA}$		1.3	V
			$4.0\text{ V} \leq EV_{DD0} \leq 5.5\text{ V}$, $I_{OL1} = 8.5\text{ mA}$		0.7	V
			$4.0\text{ V} \leq EV_{DD0} \leq 5.5\text{ V}$, $I_{OL1} = 4.0\text{ mA}$		0.4	V
			$2.7\text{ V} \leq EV_{DD0} \leq 5.5\text{ V}$, $I_{OL1} = 1.5\text{ mA}$		0.4	V
			$1.8\text{ V} \leq EV_{DD0} \leq 5.5\text{ V}$, $I_{OL1} = 0.6\text{ mA}$		0.4	V
			$1.6\text{ V} \leq EV_{DD0} < 1.8\text{ V}$, $I_{OL1} = 0.3\text{ mA}$		0.4	V
			VOL2	P20 to P27, P150 to P156	$1.6\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, $I_{OL2} = 400\text{ }\mu\text{A}$	
	VOL3	P60 to P63	$4.0\text{ V} \leq EV_{DD0} \leq 5.5\text{ V}$, $I_{OL3} = 15.0\text{ mA}$		2.0	V
			$4.0\text{ V} \leq EV_{DD0} \leq 5.5\text{ V}$, $I_{OL3} = 5.0\text{ mA}$		0.4	V
			$2.7\text{ V} \leq EV_{DD0} \leq 5.5\text{ V}$, $I_{OL3} = 3.0\text{ mA}$		0.4	V
			$1.8\text{ V} \leq EV_{DD0} \leq 5.5\text{ V}$, $I_{OL3} = 2.0\text{ mA}$		0.4	V
			$1.6\text{ V} \leq EV_{DD0} \leq 5.5\text{ V}$, $I_{OL3} = 1.0\text{ mA}$		0.4	V

Caution P00, P02 to P04, P10, P11, P13 to P15, P17, P30, P43 to P45, P50 to P55, P71, P74, P80 to P82, P142 to P144 do not output high level in N-ch open-drain mode.

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

Caution The pins mounted depend on the product. Refer to 1.3.1 30-pin products to 1.3.10 100-pin products.

($T_A = -40$ to $+85$ °C, $1.6\text{ V} \leq EV_{DD0} = EV_{DD1} \leq V_{DD} \leq 5.5\text{ V}$, $V_{SS} = EV_{SS0} = EV_{SS1} = 0\text{ V}$)

Items	Symbol	Conditions	MIN.	TYP.	MAX.	Unit		
Input leakage current, high	ILIH1	P00 to P06, P10 to P17, P30, P31, P40 to P47, P50 to P57, P64 to P67, P70 to P77, P80 to P87, P100 to P102, P110, P111, P120, P140 to P147	$V_I = EV_{DD0}$		1	μA		
	ILIH2	P20 to P27, P137, P150 to P156, $\overline{\text{RESET}}$	$V_I = V_{DD}$		1	μA		
	ILIH3	P121 to P124 (X1, X2, EXCLK, XT1, XT2, EXCLKS)	$V_I = V_{DD}$	In input port or external clock input	1	μA		
			In resonator connection	10	μA			
Input leakage current, low	ILIL1	P00 to P06, P10 to P17, P30, P31, P40 to P47, P50 to P57, P64 to P67, P70 to P77, P80 to P87, P100 to P102, P110, P111, P120, P140 to P147	$V_I = EV_{SS0}$		-1	μA		
	ILIL2	P20 to P27, P137, P150 to P156, $\overline{\text{RESET}}$	$V_I = V_{SS}$		-1	μA		
	ILIL3	P121 to P124 (X1, X2, EXCLK, XT1, XT2, EXCLKS)	$V_I = V_{SS}$	In input port or external clock input	-1	μA		
			In resonator connection	-10	μA			
On-chip pll-up resistance	Ru	P00 to P06, P10 to P17, P30, P31, P40 to P47, P50 to P57, P64 to P67, P70 to P77, P80 to P87, P100 to P102, P110, P111, P120, P140 to P147	$V_I = EV_{SS0}$, In input port		10	20	100	$\text{k}\Omega$

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

Caution The pins mounted depend on the product. Refer to 1.3.1 30-pin products to 1.3.10 100-pin products.

2.3.2 Supply current characteristics

(1) Flash ROM: 16 to 64 KB of 30- to 64-pin products

(TA = -40 to +85 °C, 1.6 V ≤ EVDD0 ≤ VDD ≤ 5.5 V, VSS = EVSS0 = 0 V)

(1/2)

Parameter	Symbol	Conditions				MIN.	TYP.	MAX.	Unit			
Supply current Note 1	IDD1	Operating mode	High-speed operation Notes 3, 5	fHOCO = 64 MHz, fIH = 32 MHz	Basic operation	VDD = 5.0 V		2.4		mA		
						VDD = 3.0 V		2.4				
					fHOCO = 32 MHz, fIH = 32 MHz	Basic operation	VDD = 5.0 V		2.1			
						VDD = 3.0 V		2.1				
					High-speed operation Notes 3, 5	fHOCO = 64 MHz, fIH = 32 MHz	Normal operation	VDD = 5.0 V		5.2	8.7	mA
							VDD = 3.0 V		5.2	8.7		
				fHOCO = 32 MHz, fIH = 32 MHz		Normal operation	VDD = 5.0 V		4.8	8.1		
						VDD = 3.0 V		4.8	8.1			
				fHOCO = 48 MHz, fIH = 24 MHz		Normal operation	VDD = 5.0 V		4.1	6.9		
						VDD = 3.0 V		4.1	6.9			
				fHOCO = 24 MHz, fIH = 24 MHz	Normal operation	VDD = 5.0 V		3.8	6.3			
					VDD = 3.0 V		3.8	6.3				
				fHOCO = 16 MHz, fIH = 16 MHz	Normal operation	VDD = 5.0 V		2.8	4.6			
					VDD = 3.0 V		2.8	4.6				
				Low-speed operation Notes 3, 5	fHOCO = 8 MHz, fIH = 8 MHz	Normal operation	VDD = 3.0 V		1.3	2.0	mA	
						VDD = 2.0 V		1.3	2.0			
				Low-voltage operation Notes 3, 5	fHOCO = 4 MHz, fIH = 4 MHz	Normal operation	VDD = 3.0 V		1.3	1.8	mA	
						VDD = 2.0 V		1.3	1.8			
				High-speed operation Notes 2, 5	fMX = 20 MHz, VDD = 5.0 V	Normal operation	Square wave input		3.3	5.3	mA	
							Resonator connection		3.5	5.5		
						Normal operation	Square wave input		3.3	5.3		
							Resonator connection		3.5	5.5		
					fMX = 10 MHz, VDD = 5.0 V	Normal operation	Square wave input		2.0	3.1		
							Resonator connection		2.1	3.2		
	Normal operation	Square wave input				2.0	3.1					
		Resonator connection				2.1	3.2					
	Low-speed operation Notes 2, 5	fMX = 8 MHz, VDD = 3.0 V	Normal operation	Square wave input		1.2	1.9	mA				
				Resonator connection		1.2	2.0					
		fMX = 8 MHz, VDD = 2.0 V	Normal operation	Square wave input		1.2	1.9					
				Resonator connection		1.2	2.0					
	Subsystem clock operation Note 4	fSUB = 32.768 kHz TA = -40 °C	Normal operation	Square wave input		4.7		μA				
				Resonator connection		4.7						
		fSUB = 32.768 kHz TA = +25 °C	Normal operation	Square wave input		4.7	6.1					
				Resonator connection		4.7	6.1					
		fSUB = 32.768 kHz TA = +50 °C	Normal operation	Square wave input		4.8	6.7					
				Resonator connection		4.8	6.7					
		fSUB = 32.768 kHz TA = +70 °C	Normal operation	Square wave input		4.8	7.5					
				Resonator connection		4.8	7.5					
		fSUB = 32.768 kHz TA = +85 °C	Normal operation	Square wave input		5.4	8.9					
				Resonator connection		5.4	8.9					

(Notes and Remarks are listed on the next page.)

- Note 1.** Total current flowing into V_{DD} and EV_{DD0} , including the input leakage current flowing when the level of the input pin is fixed to V_{DD} , EV_{DD0} or V_{SS} , EV_{SS0} . The values below the MAX. column include the peripheral operation current (except for background operation (BGO)). However, not including the current flowing into the A/D converter, LVD circuit, I/O port, and on-chip pull-up/pull-down resistors.
- Note 2.** When high-speed on-chip oscillator and subsystem clock are stopped.
- Note 3.** When high-speed system clock and subsystem clock are stopped.
- Note 4.** When high-speed on-chip oscillator and high-speed system clock are stopped. When real-time counter and watchdog timer is stopped. When AMPHS1 = 1 (Ultra-low power consumption oscillation).
- Note 5.** Relationship between operation voltage width, operation frequency of CPU and operation mode is as below.
 High speed operation: $V_{DD} = 2.7\text{ V to }5.5\text{ V}@1\text{ MHz to }32\text{ MHz}$
 $V_{DD} = 2.4\text{ V to }5.5\text{ V}@1\text{ MHz to }16\text{ MHz}$
 Low speed operation: $V_{DD} = 1.8\text{ V to }5.5\text{ V}@1\text{ MHz to }8\text{ MHz}$
 Low voltage operation: $V_{DD} = 1.6\text{ V to }5.5\text{ V}@1\text{ MHz to }4\text{ MHz}$

Remark 1. f_{MX} : High-speed system clock frequency (X1 clock oscillation frequency or external main system clock frequency)

Remark 2. f_{HOCO} : High-speed on-chip oscillator clock frequency (64 MHz max.)

Remark 3. f_{IH} : High-speed on-chip oscillator clock frequency (32 MHz max.) ^{Note}

Remark 4. f_{SUB} : Subsystem clock frequency (XT1 clock oscillation frequency)

Remark 5. Except subsystem clock operation, temperature condition of the TYP. value is $T_A = 25^\circ\text{C}$

Note f_{IH} is controlled by hardware to be set to two frequency division of f_{HOCO} when f_{HOCO} is set to 64 MHz or 48 MHz, and the same clock frequency as f_{HOCO} when f_{HOCO} is set to 32 MHz or less. When supplying 64 MHz or 48 MHz to timer RD, set f_{CLK} to f_{IH} .

Caution The pins mounted depend on the product. Refer to 1.3.1 30-pin products to 1.3.10 100-pin products.

(1) Flash ROM: 16 to 64 KB of 30- to 64-pin products

(TA = -40 to +85 °C, 1.6 V ≤ EVDD0 ≤ VDD ≤ 5.5 V, VSS = EVSS0 = 0 V)

(2/2)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit	
Supply current Note 1	IDD2 Note 2	HALT mode	High-speed operation Notes 4, 7	fHOCO = 64 MHz, fIH = 32 MHz	VDD = 5.0 V	0.80	3.09	mA
					VDD = 3.0 V	0.80	3.09	
				fHOCO = 32 MHz, fIH = 32 MHz	VDD = 5.0 V	0.54	2.40	
					VDD = 3.0 V	0.54	2.40	
				fHOCO = 48 MHz, fIH = 24 MHz	VDD = 5.0 V	0.62	2.40	
					VDD = 3.0 V	0.62	2.40	
			fHOCO = 24 MHz, fIH = 24 MHz	VDD = 5.0 V	0.44	1.83		
				VDD = 3.0 V	0.44	1.83		
			fHOCO = 16 MHz, fIH = 16 MHz	VDD = 5.0 V	0.40	1.38		
				VDD = 3.0 V	0.40	1.38		
			Low-speed operation Notes 4, 7	fHOCO = 8 MHz, fIH = 8 MHz	VDD = 3.0 V	260	710	μA
					VDD = 2.0 V	260	710	
			Low-voltage operation Notes 4, 7	fHOCO = 4 MHz, fIH = 4 MHz	VDD = 3.0 V	420	700	μA
					VDD = 2.0 V	420	700	
			High-speed operation Notes 3, 7	fMX = 20 MHz, VDD = 5.0 V	Square wave input	0.28	1.55	mA
					Resonator connection	0.53	1.74	
					Square wave input	0.28	1.55	
					Resonator connection	0.49	1.74	
		fMX = 10 MHz, VDD = 5.0 V		Square wave input	0.19	0.86		
				Resonator connection	0.30	0.93		
		fMX = 10 MHz, VDD = 3.0 V		Square wave input	0.19	0.86		
				Resonator connection	0.30	0.93		
		Low-speed operation Notes 3, 7	fMX = 7 MHz, VDD = 3.0 V	Square wave input	95	550	μA	
				Resonator connection	145	590		
			fMX = 8 MHz, VDD = 2.0 V	Square wave input	95	550		
				Resonator connection	145	590		
		Subsystem clock operation Note 5	fsUB = 32.768 kHz, TA = -40 °C	Square wave input	0.25		μA	
Resonator connection	0.44							
fsUB = 32.768 kHz, TA = +25 °C	Square wave input		0.30	0.57				
	Resonator connection		0.49	0.76				
fsUB = 32.768 kHz, TA = +50 °C	Square wave input		0.33	1.17				
	Resonator connection		0.52	1.36				
fsUB = 32.768 kHz, TA = +70 °C	Square wave input		0.36	1.97				
	Resonator connection		0.55	2.16				
fsUB = 32.768 kHz, TA = +85 °C	Square wave input	0.97	3.37					
	Resonator connection	0.16	3.56					
IDD3	STOP mode Note 6	TA = -40 °C		0.18		μA		
		TA = +25 °C		0.24	0.51			
		TA = +50 °C		0.26	1.10			
		TA = +70 °C		0.29	1.90			
		TA = +85 °C		0.90	3.30			

(Notes and Remarks are listed on the next page.)

- Note 1.** Total current flowing into V_{DD} and EV_{DD0} , including the input leakage current flowing when the level of the input pin is fixed to V_{DD} , EV_{DD0} or V_{SS} , EV_{SS0} . The values below the MAX. column include the peripheral operation current. However, not including the current flowing into the A/D converter, LVD circuit, I/O port, and on-chip pull-up/pull-down resistors.
- Note 2.** During HALT instruction execution by flash memory.
- Note 3.** When high-speed on-chip oscillator and subsystem clock are stopped.
- Note 4.** When high-speed system clock and subsystem clock are stopped.
- Note 5.** When operating real-time clock (RTC) and setting ultra-low current consumption ($AMP_{HS1} = 1$). When high-speed on-chip oscillator and high-speed system clock are stopped. When watchdog timer is stopped. The values below the MAX. column include the leakage current.
- Note 6.** When high-speed on-chip oscillator, high-speed system clock, and subsystem clock are stopped. When watchdog timer is stopped. The values below the MAX. column include the leakage current.
- Note 7.** Relationship between operation voltage width, operation frequency of CPU and operation mode is as below.
 High speed operation: $V_{DD} = 2.7\text{ V to }5.5\text{ V}@1\text{ MHz to }32\text{ MHz}$
 $V_{DD} = 2.4\text{ V to }5.5\text{ V}@1\text{ MHz to }16\text{ MHz}$
 Low speed operation: $V_{DD} = 1.8\text{ V to }5.5\text{ V}@1\text{ MHz to }8\text{ MHz}$
 Low voltage operation: $V_{DD} = 1.6\text{ V to }5.5\text{ V}@1\text{ MHz to }4\text{ MHz}$
- Remark 1.** f_{MX} : High-speed system clock frequency (X1 clock oscillation frequency or external main system clock frequency)
- Remark 2.** f_{HOCO} : High-speed on-chip oscillator clock frequency (64 MHz max.)
- Remark 3.** f_{IH} : High-speed on-chip oscillator clock frequency (32 MHz max.) ^{Note}
- Remark 4.** f_{SUB} : Subsystem clock frequency (XT1 clock oscillation frequency)
- Remark 5.** Except subsystem clock operation and STOP mode, temperature condition of the TYP. value is $T_A = 25\text{ }^\circ\text{C}$
- Note** f_{IH} is controlled by hardware to be set to two frequency division of f_{HOCO} when f_{HOCO} is set to 64 MHz or 48 MHz, and the same clock frequency as f_{HOCO} when f_{HOCO} is set to 32 MHz or less. When supplying 64 MHz or 48 MHz to timer RD, set f_{CLK} to f_{IH} .

Caution The pins mounted depend on the product. Refer to 1.3.1 30-pin products to 1.3.10 100-pin products.

(2) Flash ROM: 96 to 256 KB of 30- to 100-pin products

(TA = -40 to +85 °C, 1.6 V ≤ EVDD0 = EVDD1 ≤ VDD ≤ 5.5 V, VSS = EVSS0 = EVSS1 = 0 V)

(1/2)

Parameter	Symbol	Conditions				MIN.	TYP.	MAX.	Unit		
Supply current Note 1	IDD1	Operating mode	High-speed operation Notes 3, 5	fHOCO = 64 MHz, fIH = 32 MHz	Basic operation	VDD = 5.0 V		2.6		mA	
						VDD = 3.0 V		2.6			
				fHOCO = 32 MHz, fIH = 32 MHz	Basic operation	VDD = 5.0 V		2.3			
						VDD = 3.0 V		2.3			
				High-speed operation Notes 3, 5	fHOCO = 64 MHz, fIH = 32 MHz	Normal operation	VDD = 5.0 V		5.8		10.2
							VDD = 3.0 V		5.8		10.2
			fHOCO = 32 MHz, fIH = 32 MHz		Normal operation	VDD = 5.0 V		5.4	9.6		
						VDD = 3.0 V		5.4	9.6		
			fHOCO = 48 MHz, fIH = 24 MHz		Normal operation	VDD = 5.0 V		4.5	7.8		
						VDD = 3.0 V		4.5	7.8		
			fHOCO = 24 MHz, fIH = 24 MHz	Normal operation	VDD = 5.0 V		4.2	7.4			
					VDD = 3.0 V		4.2	7.4			
		fHOCO = 16 MHz, fIH = 16 MHz	Normal operation	VDD = 5.0 V		3.1	5.3				
				VDD = 3.0 V		3.1	5.3				
		Low-speed operation Notes 3, 5	fHOCO = 8 MHz, fIH = 8 MHz	Normal operation	VDD = 3.0 V		1.4	2.3			
					VDD = 2.0 V		1.4	2.3			
		Low-voltage operation Notes 3, 5	fHOCO = 4 MHz, fIH = 4 MHz	Normal operation	VDD = 3.0 V		1.4	1.9			
					VDD = 2.0 V		1.4	1.9			
		High-speed operation Notes 2, 5	fMX = 20 MHz, VDD = 5.0 V	Normal operation	Square wave input		3.7	6.2			
					Resonator connection		3.9	6.4			
				Normal operation	Square wave input		3.7	6.2			
					Resonator connection		3.9	6.4			
			fMX = 10 MHz, VDD = 5.0 V	Normal operation	Square wave input		2.2	3.6			
					Resonator connection		2.3	3.7			
fMX = 10 MHz, VDD = 3.0 V	Normal operation		Square wave input		2.2	3.6					
			Resonator connection		2.3	3.7					
Low-speed operation Notes 2, 5	fMX = 8 MHz, VDD = 3.0 V	Normal operation	Square wave input		1.3	2.2					
			Resonator connection		1.3	2.3					
	fMX = 8 MHz, VDD = 2.0 V	Normal operation	Square wave input		1.3	2.2					
			Resonator connection		1.3	2.3					
Subsystem clock operation Note 4	fSUB = 32.768 kHz TA = -40 °C	Normal operation	Square wave input		5.0						
			Resonator connection		5.0						
	fSUB = 32.768 kHz TA = +25 °C	Normal operation	Square wave input		5.0	7.1					
			Resonator connection		5.0	7.1					
	fSUB = 32.768 kHz TA = +50 °C	Normal operation	Square wave input		5.1	8.8					
			Resonator connection		5.1	8.8					
fSUB = 32.768 kHz TA = +70 °C	Normal operation	Square wave input		5.5	10.5						
		Resonator connection		5.5	10.5						
fSUB = 32.768 kHz TA = +85 °C	Normal operation	Square wave input		6.5	14.5						
		Resonator connection		6.5	14.5						

(Notes and Remarks are listed on the next page.)

- Note 1.** Total current flowing into V_{DD} , EV_{DD0} and EV_{DD1} , including the input leakage current flowing when the level of the input pin is fixed to V_{DD} , EV_{DD0} or V_{SS} , EV_{SS0} . The values below the MAX. column include the peripheral operation current (except for background operation (BGO)). However, not including the current flowing into the A/D converter, D/A converter, comparator, LVD circuit, I/O port, and on-chip pull-up/pull-down resistors.
- Note 2.** When high-speed on-chip oscillator and subsystem clock are stopped.
- Note 3.** When high-speed system clock and subsystem clock are stopped.
- Note 4.** When high-speed on-chip oscillator and high-speed system clock are stopped. When real-time counter and watchdog timer is stopped. When $AMP_{HS1} = 1$ (Ultra-low power consumption oscillation).
- Note 5.** Relationship between operation voltage width, operation frequency of CPU and operation mode is as below.
 High speed operation: $V_{DD} = 2.7\text{ V to }5.5\text{ V}@1\text{ MHz to }32\text{ MHz}$
 $V_{DD} = 2.4\text{ V to }5.5\text{ V}@1\text{ MHz to }16\text{ MHz}$
 Low speed operation: $V_{DD} = 1.8\text{ V to }5.5\text{ V}@1\text{ MHz to }8\text{ MHz}$
 Low voltage operation: $V_{DD} = 1.6\text{ V to }5.5\text{ V}@1\text{ MHz to }4\text{ MHz}$

Remark 1. f_{MX} : High-speed system clock frequency (X1 clock oscillation frequency or external main system clock frequency)

Remark 2. f_{HOCO} : High-speed on-chip oscillator clock frequency (64 MHz max.)

Remark 3. f_{IH} : High-speed on-chip oscillator clock frequency (32 MHz max.) ^{Note}

Remark 4. f_{SUB} : Subsystem clock frequency (XT1 clock oscillation frequency)

Remark 5. Except subsystem clock operation, temperature condition of the TYP. value is $T_A = 25\text{ }^\circ\text{C}$

Note f_{IH} is controlled by hardware to be set to two frequency division of f_{HOCO} when f_{HOCO} is set to 64 MHz or 48 MHz, and the same clock frequency as f_{HOCO} when f_{HOCO} is set to 32 MHz or less. When supplying 64 MHz or 48 MHz to timer RD, set f_{CLK} to f_{IH} .

Caution The pins mounted depend on the product. Refer to 1.3.1 30-pin products to 1.3.10 100-pin products.

(2) Flash ROM: 96 to 256 KB of 30- to 100-pin products

($T_A = -40$ to $+85$ °C, $1.6\text{ V} \leq EV_{DD0} = EV_{DD1} \leq V_{DD} \leq 5.5\text{ V}$, $V_{SS} = EV_{SS0} = EV_{SS1} = 0\text{ V}$)

(2/2)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit			
Supply current Note 1	IDD2	HALT mode Note 2	High-speed operation Notes 4, 7	fHOCO = 64 MHz, fIH = 32 MHz	VDD = 5.0 V	0.88	3.32	mA		
					VDD = 3.0 V	0.88	3.32			
				fHOCO = 32 MHz, fIH = 32 MHz	VDD = 5.0 V	0.62	2.63			
					VDD = 3.0 V	0.62	2.63			
				fHOCO = 48 MHz, fIH = 24 MHz	VDD = 5.0 V	0.68	2.57			
					VDD = 3.0 V	0.68	2.57			
				fHOCO = 24 MHz, fIH = 24 MHz	VDD = 5.0 V	0.50	2.00			
					VDD = 3.0 V	0.50	2.00			
				fHOCO = 16 MHz, fIH = 16 MHz	VDD = 5.0 V	0.44	1.49			
					VDD = 3.0 V	0.44	1.49			
				Low-speed operation Notes 4, 7	fHOCO = 8 MHz, fIH = 8 MHz	VDD = 3.0 V	290		800	μA
						VDD = 2.0 V	290		800	
			Low-voltage operation Notes 4, 7	fHOCO = 4 MHz, fIH = 4 MHz	VDD = 3.0 V	440	755	μA		
					VDD = 2.0 V	440	755			
			High-speed operation Notes 3, 7	fMX = 20 MHz, VDD = 5.0 V	Square wave input	0.31	1.63	mA		
					Resonator connection	0.50	1.85			
					Square wave input	0.31	1.63			
					Resonator connection	0.50	1.85			
				fMX = 10 MHz, VDD = 5.0 V	Square wave input	0.21	0.89			
					Resonator connection	0.30	0.97			
				fMX = 10 MHz, VDD = 3.0 V	Square wave input	0.21	0.89			
					Resonator connection	0.30	0.97			
			Low-speed operation Notes 3, 7	fMX = 8 MHz, VDD = 3.0 V	Square wave input	110	580	μA		
					Resonator connection	160	630			
				fMX = 8 MHz, VDD = 2.0 V	Square wave input	110	580			
					Resonator connection	160	630			
			Subsystem clock operation Note 5	fSUB = 32.768 kHz, TA = -40 °C	Square wave input	0.28		μA		
					Resonator connection	0.47				
				fSUB = 32.768 kHz, TA = +25 °C	Square wave input	0.34	0.66			
					Resonator connection	0.53	0.85			
				fSUB = 32.768 kHz, TA = +50 °C	Square wave input	0.37	2.35			
					Resonator connection	0.56	2.54			
fSUB = 32.768 kHz, TA = +70 °C	Square wave input	0.61		4.08						
	Resonator connection	0.80		4.27						
fSUB = 32.768 kHz, TA = +85 °C	Square wave input	1.55	8.09							
	Resonator connection	1.74	8.28							
IDD3	STOP mode Note 6	TA = -40 °C		0.19		μA				
		TA = +25 °C		0.25	0.57					
		TA = +50 °C		0.28	2.26					
		TA = +70 °C		0.52	3.99					
		TA = +85 °C		1.46	8.00					

(Notes and Remarks are listed on the next page.)

- Note 1.** Total current flowing into V_{DD} , EV_{DD0} and EV_{DD1} , including the input leakage current flowing when the level of the input pin is fixed to V_{DD} , EV_{DD0} , EV_{DD1} or V_{SS} , EV_{SS0} , EV_{SS1} . The values below the MAX. column include the peripheral operation current. However, not including the current flowing into the A/D converter, D/A converter, comparator, LVD circuit, I/O port, and on-chip pull-up/pull-down resistors.
- Note 2.** During HALT instruction execution by flash memory.
- Note 3.** When high-speed on-chip oscillator and subsystem clock are stopped.
- Note 4.** When high-speed system clock and subsystem clock are stopped.
- Note 5.** When operating real-time clock (RTC) and setting ultra-low current consumption ($AMP_{HS1} = 1$). When high-speed on-chip oscillator and high-speed system clock are stopped. When watchdog timer is stopped. The values below the MAX. column include the leakage current.
- Note 6.** When high-speed on-chip oscillator, high-speed system clock, and subsystem clock are stopped. When watchdog timer is stopped. The values below the MAX. column include the leakage current.
- Note 7.** Relationship between operation voltage width, operation frequency of CPU and operation mode is as below.
 High speed operation: $V_{DD} = 2.7\text{ V to }5.5\text{ V}@1\text{ MHz to }32\text{ MHz}$
 $V_{DD} = 2.4\text{ V to }5.5\text{ V}@1\text{ MHz to }16\text{ MHz}$
 Low speed operation: $V_{DD} = 1.8\text{ V to }5.5\text{ V}@1\text{ MHz to }8\text{ MHz}$
 Low voltage operation: $V_{DD} = 1.6\text{ V to }5.5\text{ V}@1\text{ MHz to }4\text{ MHz}$
- Remark 1.** f_{MX} : High-speed system clock frequency (X1 clock oscillation frequency or external main system clock frequency)
- Remark 2.** f_{HOCO} : High-speed on-chip oscillator clock frequency (64 MHz max.)
- Remark 3.** f_{IH} : High-speed on-chip oscillator clock frequency (32 MHz max.) ^{Note}
- Remark 4.** f_{SUB} : Subsystem clock frequency (XT1 clock oscillation frequency)
- Remark 5.** Except subsystem clock operation and STOP mode, temperature condition of the TYP. value is $T_A = 25\text{ }^\circ\text{C}$
- Note** f_{IH} is controlled by hardware to be set to two frequency division of f_{HOCO} when f_{HOCO} is set to 64 MHz or 48 MHz, and the same clock frequency as f_{HOCO} when f_{HOCO} is set to 32 MHz or less. When supplying 64 MHz or 48 MHz to timer RD, set f_{CLK} to f_{IH} .

Caution The pins mounted depend on the product. Refer to 1.3.1 30-pin products to 1.3.10 100-pin products.

(3) Common to RL78/G14 all products

($T_A = -40$ to $+85$ °C, 1.6 V \leq $EV_{DD0} = EV_{DD1} \leq V_{DD} \leq 5.5$ V, $V_{SS} = EV_{SS0} = EV_{SS1} = 0$ V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
RTC operating current	IRTC Notes 1, 2	f _{SUB} = 32.768 kHz	Real-time clock operation		0.02		μA
			12-bit interval timer operation		0.02		
Watchdog timer operating current	I _{WDT} Notes 2, 3	f _{IL} = 15 kHz			0.22		μA
A/D converter operating current	I _{ADC} Note 4	When conversion at maximum speed	Normal mode, AV _{REFP} = V _{DD} = 5.0 V		1.3	1.7	mA
			Low voltage mode, AV _{REFP} = V _{DD} = 3.0 V		0.5	0.7	mA
A/D converter reference voltage current	I _{ADREF}				75		μA
D/A converter operating current	I _{DAC} Notes 5, 9	Per D/A converter channel				1.5	mA
Comparator operating current	I _{COMP} Notes 6, 9	V _{DD} = 5.0 V, Regulator output voltage = 2.1 V	Window comparator mode		12.5		μA
			High-speed comparator mode		6.5		μA
			Low-speed comparator mode		1.7		μA
		V _{DD} = 5.0 V, Regulator output voltage = 1.8 V	Window comparator mode		8.0		μA
			High-speed comparator mode		4.0		μA
			Low-speed comparator mode		1.3		μA
Temperature sensor operating current	I _{TMPS}				75		μA
LVD operating current	I _{LVI} Note 7				0.08		μA
BGO operating current	I _{BGO} Note 8				2.50	12.20	mA

Note 1. Current flowing only to the real-time clock (excluding the operating current of the XT1 oscillator). The TYP. value of the current value of the RL78/G14 is the sum of the TYP. values of either I_{DD1} or I_{DD2}, and I_{RTC}, when the real-time clock operates in operation mode or HALT mode. The I_{DD1} and I_{DD2} MAX. values also include the real-time clock operating current. However, I_{DD2} subsystem clock operation includes the operational current of the real-time clock.

Note 2. When high speed on-chip oscillator and high-speed system clock are stopped.

Note 3. Current flowing only to the watchdog timer (including the operating current of the low-speed on-chip oscillator). The current value of the RL78/G14 is the sum of I_{DD1}, I_{DD2} or I_{DD3} and I_{WDT} when the watchdog timer operates in STOP mode.

Note 4. Current flowing only to the A/D converter. The current value of the RL78/G14 is the sum of I_{DD1} or I_{DD2} and I_{ADC} when the A/D converter operates in an operation mode or the HALT mode.

Note 5. Current flowing only to the D/A converter. The current value of the RL78/G14 is the sum of I_{DD1} or I_{DD2} and I_{ADC} when the D/A converter operates in an operation mode or the HALT mode.

Note 6. Current flowing only to the comparator circuit. The current value of the RL78/G14 is the sum of I_{DD1}, I_{DD2} or I_{DD3} and I_{COMP} when the comparator circuit operates in the Operating, HALT or STOP mode.

Note 7. Current flowing only to the LVD circuit. The current value of the RL78/G14 is the sum of I_{DD1}, I_{DD2} or I_{DD3} and I_{LVI} when the LVD circuit operates in the Operating, HALT or STOP mode.

Note 8. Current flowing only to the BGO. The current value of the RL78/G14 is the sum of I_{DD1} or I_{DD2} and I_{BGO} when the BGO operates in an operation mode.

Note 9. A comparator and D/A converter are provided in products with 96 KB or more code flash memory.

Remark 1. f_{IL}: Low-speed on-chip oscillator clock frequency

Remark 2. f_{SUB}: Subsystem clock frequency (XT1 clock oscillation frequency)

Remark 3. f_{CLK}: CPU/peripheral hardware clock frequency

Remark 4. Temperature condition of the TYP. value is T_A = 25 °C

Caution The pins mounted depend on the product. Refer to 1.3.1 30-pin products to 1.3.10 100-pin products.

2.4 AC Characteristics

2.4.1 Basic operation

($T_A = -40$ to $+85$ °C, $1.6\text{ V} \leq EV_{DD0} = EV_{DD1} \leq V_{DD} \leq 5.5\text{ V}$, $V_{SS} = EV_{SS0} = EV_{SS1} = 0\text{ V}$)

(1/2)

Items	Symbol	Conditions		MIN.	TYP.	MAX.	Unit	
Instruction cycle (minimum instruction execution time)	T _{CY}	Main system clock (f _{MAIN}) operation	High-speed main mode	$2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	0.03125		1	μs
				$2.4\text{ V} \leq V_{DD} < 2.7\text{ V}$	0.0625		1	μs
			Low voltage main mode	$1.6\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	0.25		1	μs
			Low-speed main mode	$1.8\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	0.125		1	μs
			Subsystem clock (f _{SUB}) operation	$1.8\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	28.5	30.5	31.3	μs
		In the self programming mode	High-speed main mode	$2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	0.03125		1	μs
	$2.4\text{ V} \leq V_{DD} < 2.7\text{ V}$			0.0625		1	μs	
	Low voltage main mode		$1.8\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	0.25		1	μs	
Low-speed main mode	$1.8\text{ V} \leq V_{DD} \leq 5.5\text{ V}$		0.125		1	μs		
External main system clock frequency	f _{EX}	$2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}$		1.0		20.0	MHz	
		$1.8\text{ V} \leq V_{DD} < 2.7\text{ V}$		1.0		8.0	MHz	
		$1.6\text{ V} \leq V_{DD} < 1.8\text{ V}$		1.0		4.0	MHz	
	f _{EXS}			32		35	kHz	
External main system clock input high-level width, low-level width	t _{EXH} , t _{EXL}	$2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}$		24			ns	
		$1.8\text{ V} \leq V_{DD} < 2.7\text{ V}$		60			ns	
		$1.6\text{ V} \leq V_{DD} < 1.8\text{ V}$		120			ns	
	t _{EXHS} , t _{EXLS}			13.7			μs	
T _{I00} to T _{I03} , T _{I10} to T _{I13} input high-level width, low-level width	t _{TIH} , t _{TIL}			1/f _{MCK} + 10 Note			ns	
Timer RJ input cycle	f _c	TRJIO	$2.7\text{ V} \leq EV_{DD0} \leq 5.5\text{ V}$	100			ns	
			$1.8\text{ V} \leq EV_{DD0} < 2.7\text{ V}$	300			ns	
			$1.6\text{ V} \leq EV_{DD0} < 1.8\text{ V}$	500			ns	
Timer RJ input high- level width, low-level width	f _{WH} , f _{WL}	TRJIO	$2.7\text{ V} \leq EV_{DD0} \leq 5.5\text{ V}$	40			ns	
			$1.8\text{ V} \leq EV_{DD0} < 2.7\text{ V}$	120			ns	
			$1.6\text{ V} \leq EV_{DD0} < 1.8\text{ V}$	200			ns	

Note The following conditions are required for low voltage interface when $EV_{DD0} < V_{DD}$

$1.8\text{ V} \leq EV_{DD0} < 2.7\text{ V}$: MIN. 125 ns

$1.6\text{ V} \leq EV_{DD0} < 1.8\text{ V}$: MIN. 250 ns

Remark f_{MCK}: Timer array unit operation clock frequency

(Operation clock to be set by the CKSmn bit of timer mode register mn (TMRmn). m: Unit number (m = 0, 1), n: Channel number (n = 0 to 3))

(TA = -40 to +85 °C, 1.6 V ≤ EVDD0 = EVDD1 ≤ VDD ≤ 5.5 V, VSS = EVSS0 = EVSS1 = 0 V)

(2/2)

Items	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
TO00 to TO03, TO10 to T13 output frequency	f _{ro}	High-speed main mode	4.0 V ≤ EVDD0 ≤ 5.5 V		16	MHz
			2.7 V ≤ EVDD0 < 4.0 V		8	MHz
			1.8 V ≤ EVDD0 < 2.7 V		4	MHz
			1.6 V ≤ EVDD0 < 1.8 V		2	MHz
		Low voltage main mode	1.6 V ≤ EVDD0 ≤ 5.5 V		2	MHz
		Low-speed main mode	1.8 V ≤ EVDD0 ≤ 5.5 V		4	MHz
		1.6 V ≤ EVDD0 < 1.8 V		2	MHz	
PCLBUZ0, PCLBUZ1 output frequency	f _{PCL}	High-speed main mode	4.0 V ≤ EVDD0 ≤ 5.5 V		16	MHz
			2.7 V ≤ EVDD0 < 4.0 V		8	MHz
			1.8 V ≤ EVDD0 < 2.7 V		4	MHz
			1.6 V ≤ EVDD0 < 1.8 V		2	MHz
		Low voltage main mode	1.8 V ≤ EVDD0 ≤ 5.5 V		4	MHz
		Low-speed main mode	1.6 V ≤ EVDD0 < 1.8 V		2	MHz
Interrupt input high-level width, low-level width	t _{INTH} ,	INTP0	1.6 V ≤ VDD ≤ 5.5 V	1		μs
	t _{INTL}	INTP1 to INTP11	1.6 V ≤ EVDD0 ≤ 5.5 V	1		μs
Key interrupt input low-level width	t _{KR}	1.8 V ≤ EVDD0 ≤ 5.5 V	250			ns
		1.6 V ≤ EVDD0 < 1.8 V	1			μs
RESET low-level width	t _{RSL}		10			μs

Caution The pins mounted depend on the product. Refer to 1.3.1 30-pin products to 1.3.10 100-pin products.

2.5 Peripheral Functions Characteristics

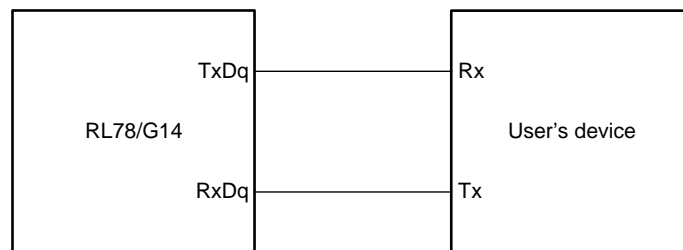
2.5.1 Serial array unit

(1) During communication at same potential (UART mode) (dedicated baud rate generator output)

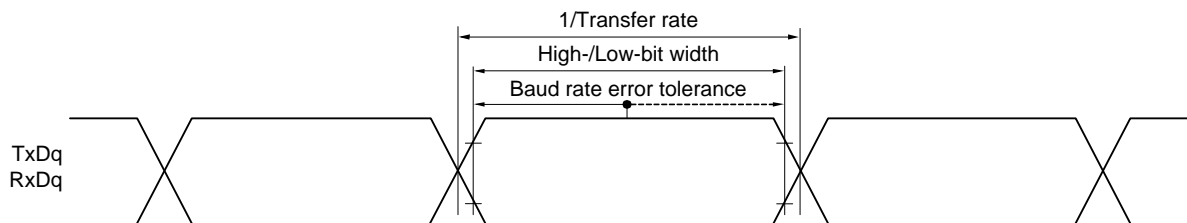
($T_A = -40$ to $+85$ °C, $1.6\text{ V} \leq EV_{DD0} = EV_{DD1} \leq 5.5\text{ V}$, $V_{SS} = EV_{SS0} = EV_{SS1} = 0\text{ V}$)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Transfer rate Note 1					fMCK/6 Note 2	bps
		Theoretical value of the maximum transfer rate fCLK = 32 MHz, fMCK = fCLK			5.3	Mbps

UART mode connection diagram (during communication at same potential)



UART mode bit width (during communication at same potential) (reference)



Note 1. Transfer rate in the SNOOZE mode is MAX. 9600 bps and MIN. 4800 bps.

Note 2. The following conditions are required for low voltage interface when $EV_{DD0} < V_{DD}$.

$2.4\text{ V} \leq EV_{DD0} < 2.7\text{ V}$: MAX. 2.6 Mbps

$1.8\text{ V} \leq EV_{DD0} < 2.4\text{ V}$: MAX. 1.3 Mbps

$1.6\text{ V} \leq EV_{DD0} < 1.8\text{ V}$: MAX. 0.6 Mbps

Caution Select the normal input buffer for the RxDq pin and the normal output mode for the TxDq pin by using port input mode register g (PIMg) and port output mode register g (POMg).

Remark 1. q: UART number (q = 0 to 3), g: PIM and POM number (g = 0, 1, 5, 14)

Remark 2. fMCK: Serial array unit operation clock frequency

(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number, n: Channel number (mn = 00 to 03, 10 to 13))

Caution The pins mounted depend on the product. Refer to 1.3.1 30-pin products to 1.3.10 100-pin products.

(2) During communication at same potential (CSI mode) (master mode (fmck/2), $\overline{\text{SCKp}}$... internal clock output)
(TA = -40 to +85 °C, 2.7 V ≤ EVDD0 = EVDD1 ≤ VDD ≤ 5.5 V, VSS = EVSS0 = EVSS1 = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
$\overline{\text{SCKp}}$ cycle time	tkCY1	2.7 V ≤ EVDD0 ≤ 5.5 V	62.5 Note 1			ns
$\overline{\text{SCKp}}$ high-/low-level width	tkH1, tkL1	4.0 V ≤ EVDD0 ≤ 5.5 V	tkCY1/2 - 7			ns
		2.7 V ≤ EVDD0 ≤ 5.5 V	tkCY1/2 - 10			ns
Slp setup time (to $\overline{\text{SCKp}}\uparrow$) Note 2	tsIK1	4.0 V ≤ EVDD0 ≤ 5.5 V	23			ns
		2.7 V ≤ EVDD0 ≤ 5.5 V	33 Note 5			ns
Slp hold time (from $\overline{\text{SCKp}}\uparrow$) Note 3	tkSI1	2.7 V ≤ EVDD0 ≤ 5.5 V	10			ns
Delay time from $\overline{\text{SCKp}}\downarrow$ to SOp output Note 4	tkSO1	C = 20 pF Note 6			10	ns

Note 1. The value must also be $2/f_{\text{CLK}}$ or more.

Note 2. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The Slp setup time becomes “to $\overline{\text{SCKp}}\downarrow$ ” when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

Note 3. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The Slp hold time becomes “from $\overline{\text{SCKp}}\downarrow$ ” when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

Note 4. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The delay time to SOp output becomes “from $\overline{\text{SCKp}}\uparrow$ ” when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

Note 5. Using the fmck within 24 MHz.

Note 6. C is the load capacitance of the $\overline{\text{SCKp}}$ and SOp output lines.

Caution Select the normal input buffer for the Slp pin and the normal output mode for the SOp pin and $\overline{\text{SCKp}}$ pin by using port input mode register g (PIMg) and port output mode register g (POMg).

Remark 1. This specification is valid only when CSI00's peripheral I/O redirect function is not used.

Remark 2. p: CSI number (p = 00), m: Unit number (m = 0), n: Channel number (n = 0),
g: PIM and POM numbers (g = 1)

Remark 3. fmck: Serial array unit operation clock frequency
(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number,
n: Channel number (mn = 00))

Caution The pins mounted depend on the product. Refer to 1.3.1 30-pin products to 1.3.10 100-pin products.

(3) During communication at same potential (CSI mode) (master mode (fmck/4), $\overline{\text{SCKp}}$... internal clock output)
($T_A = -40$ to $+85$ °C, $1.6\text{ V} \leq \text{EVDD0} = \text{EVDD1} \leq \text{VDD} \leq 5.5\text{ V}$, $\text{Vss} = \text{EVss0} = \text{EVss1} = 0\text{ V}$)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
$\overline{\text{SCKp}}$ cycle time	tkCY1	$2.7\text{ V} \leq \text{EVDD0} \leq 5.5\text{ V}$	125 Note 1			ns
		$2.4\text{ V} \leq \text{EVDD0} \leq 5.5\text{ V}$	250 Note 1			ns
		$1.8\text{ V} \leq \text{EVDD0} \leq 5.5\text{ V}$	500 Note 1			ns
		$1.6\text{ V} \leq \text{EVDD0} \leq 5.5\text{ V}$	1000 Note 1			ns
$\overline{\text{SCKp}}$ high-/low-level width	tkH1, tkL1	$4.0\text{ V} \leq \text{EVDD0} \leq 5.5\text{ V}$	tkCY1/2 - 12			ns
		$2.7\text{ V} \leq \text{EVDD0} \leq 5.5\text{ V}$	tkCY1/2 - 18			ns
		$2.4\text{ V} \leq \text{EVDD0} \leq 5.5\text{ V}$	tkCY1/2 - 38			ns
		$1.8\text{ V} \leq \text{EVDD0} \leq 5.5\text{ V}$	tkCY1/2 - 50			ns
		$1.6\text{ V} \leq \text{EVDD0} \leq 5.5\text{ V}$	tkCY1/2 - 100			ns
Slp setup time (to $\overline{\text{SCKp}}\uparrow$) Note 2	tsIK1	$4.0\text{ V} \leq \text{EVDD0} \leq 5.5\text{ V}$	44			ns
		$2.7\text{ V} \leq \text{EVDD0} \leq 5.5\text{ V}$	44			ns
		$2.4\text{ V} \leq \text{EVDD0} \leq 5.5\text{ V}$	75			ns
		$1.8\text{ V} \leq \text{EVDD0} \leq 5.5\text{ V}$	110			ns
		$1.6\text{ V} \leq \text{EVDD0} \leq 5.5\text{ V}$	220			ns
Slp hold time (from $\overline{\text{SCKp}}\uparrow$) Note 3	tkS1		19			ns
Delay time from $\overline{\text{SCKp}}\downarrow$ to SOp output Note 4	tkSO1	C = 30 pF Note 5			25	ns

Note 1. The value must also be $4/f_{\text{CLK}}$ or more.

Note 2. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The Slp setup time becomes “to $\overline{\text{SCKp}}\downarrow$ ” when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

Note 3. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The Slp hold time becomes “from $\overline{\text{SCKp}}\downarrow$ ” when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

Note 4. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The delay time to SOp output becomes “from $\overline{\text{SCKp}}\uparrow$ ” when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

Note 5. C is the load capacitance of the $\overline{\text{SCKp}}$ and SOp output lines.

Caution Select the normal input buffer for the Slp pin and the normal output mode for the SOp pin and $\overline{\text{SCKp}}$ pin by using port input mode register g (PIMg) and port output mode register g (POMg).

Remark 1. p: CSI number (p = 00, 01, 10, 11, 20, 21, 30, 31), m: Unit number (m = 0, 1), n: Channel number (n = 0 to 3), g: PIM number (g = 0, 1, 3 to 5, 14)

Remark 2. fmck: Serial array unit operation clock frequency
(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number, n: Channel number (mn = 00 to 03, 10 to 13))

Caution The pins mounted depend on the product. Refer to 1.3.1 30-pin products to 1.3.10 100-pin products.

(4) During communication at same potential (CSI mode) (slave mode, $\overline{\text{SCKp}}$... external clock input)

($T_A = -40$ to $+85$ °C, $1.6\text{ V} \leq \text{EVDD0} = \text{EVDD1} \leq \text{VDD} \leq 5.5\text{ V}$, $\text{VSS} = \text{EVSS0} = \text{EVSS1} = 0\text{ V}$)

(1/2)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
$\overline{\text{SCKp}}$ cycle time Note 5	tkCY2	$4.0\text{ V} \leq \text{EVDD0} \leq 5.5\text{ V}$	$20\text{ MHz} < \text{fMCK}$	$8/\text{fMCK}$		ns
			$\text{fMCK} \leq 20\text{ MHz}$	$6/\text{fMCK}$		ns
		$2.7\text{ V} \leq \text{EVDD0} < 4.0\text{ V}$	$16\text{ MHz} < \text{fMCK}$	$8/\text{fMCK}$		ns
			$\text{fMCK} \leq 16\text{ MHz}$	$6/\text{fMCK}$		ns
		$1.8\text{ V} \leq \text{EVDD0} < 2.7\text{ V}$	$16\text{ MHz} < \text{fMCK}$	$8/\text{fMCK}$		ns
			$\text{fMCK} \leq 16\text{ MHz}$	$6/\text{fMCK}$		ns
$1.6\text{ V} \leq \text{EVDD0} < 1.8\text{ V}$		$6/\text{fMCK}$		ns		
$\overline{\text{SCKp}}$ high-/low-level width	tkH2, tkL2	$1.6\text{ V} \leq \text{EVDD0} \leq 5.5\text{ V}$	tkCY2/2			ns
Slp setup time (to $\overline{\text{SCKp}}\uparrow$) Note 1	tsIK2	$2.7\text{ V} \leq \text{EVDD0} \leq 5.5\text{ V}$	$1/\text{fMCK} + 20$			ns
		$1.8\text{ V} \leq \text{EVDD0} < 2.7\text{ V}$	$1/\text{fMCK} + 30$			ns
		$1.6\text{ V} \leq \text{EVDD0} < 1.8\text{ V}$	$1/\text{fMCK} + 40$			ns
Slp hold time (from $\overline{\text{SCKp}}\uparrow$) Note 2	tkSI2	$2.7\text{ V} \leq \text{EVDD0} \leq 5.5\text{ V}$	$1/\text{fMCK} + 31$			ns
		$2.4\text{ V} \leq \text{EVDD0} < 2.7\text{ V}$	$1/\text{fMCK} + 31$			ns
		$1.8\text{ V} \leq \text{EVDD0} < 2.4\text{ V}$	$1/\text{fMCK} + 31$			ns
		$1.6\text{ V} \leq \text{EVDD0} < 1.8\text{ V}$	$1/\text{fMCK} + 250$			ns
Delay time from $\overline{\text{SCKp}}\downarrow$ to SOp output Note 3	tkSO2	C = 30 pF Note 4	$4.0\text{ V} \leq \text{EVDD0} \leq 5.5\text{ V}$		$2/\text{fMCK} + 44$	ns
			$2.7\text{ V} \leq \text{EVDD0} < 4.0\text{ V}$		$2/\text{fMCK} + 44$	ns
			$2.4\text{ V} \leq \text{EVDD0} < 2.7\text{ V}$		$2/\text{fMCK} + 75$	ns
			$1.8\text{ V} \leq \text{EVDD0} < 2.4\text{ V}$		$2/\text{fMCK} + 110$	ns
			$1.6\text{ V} \leq \text{EVDD0} < 1.8\text{ V}$		$2/\text{fMCK} + 220$	ns

Note 1. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The Slp setup time becomes “to $\overline{\text{SCKp}}\downarrow$ ” when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

Note 2. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The Slp hold time becomes “from $\overline{\text{SCKp}}\downarrow$ ” when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

Note 3. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The delay time to SOp output becomes “from $\overline{\text{SCKp}}\uparrow$ ” when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

Note 4. C is the load capacitance of the SOp output lines.

Note 5. The maximum transfer rate when using the SNOOZE mode is 1 Mbps.

Caution Select the TTL input buffer for the Slp pin and $\overline{\text{SCKp}}$ pin and the normal output mode for the SOp pin by using port input mode register g (PIMg) and port output mode register g (POMg).

Remark 1. p: CSI number (p = 00, 01, 10, 11, 20, 21, 30, 31), m: Unit number (m = 0, 1),
n: Channel number (n = 0 to 3), g: PIM number (g = 0, 1, 3 to 5, 14)

Remark 2. fMCK: Serial array unit operation clock frequency
(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number,
n: Channel number (mn = 00 to 03, 10 to 13))

Caution The pins mounted depend on the product. Refer to 1.3.1 30-pin products to 1.3.10 100-pin products.

(4) During communication at same potential (CSI mode) (slave mode, $\overline{\text{SCKp}}$... external clock input)

($T_A = -40$ to $+85$ °C, $1.6 \text{ V} \leq \text{EVDD0} = \text{EVDD1} \leq \text{VDD} \leq 5.5 \text{ V}$, $\text{Vss} = \text{EVss0} = \text{EVss1} = 0 \text{ V}$)

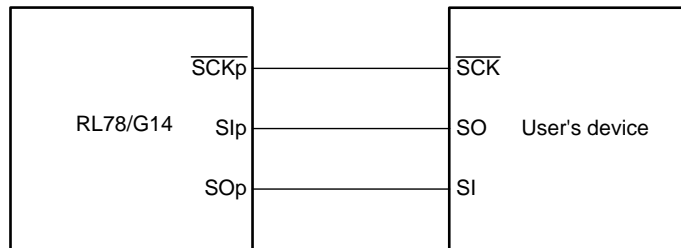
(2/2)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
$\overline{\text{SSI00}}$ setup time	tssik	DAPmn = 0	$2.7 \text{ V} \leq \text{EVDD0} \leq 5.5 \text{ V}$	120		ns
			$1.8 \text{ V} \leq \text{EVDD0} < 2.7 \text{ V}$	200		ns
			$1.6 \text{ V} \leq \text{EVDD0} < 1.8 \text{ V}$	400		ns
		DAPmn = 1	$2.7 \text{ V} \leq \text{EVDD0} \leq 5.5 \text{ V}$	$1/\text{fmck} + 120$		ns
			$1.8 \text{ V} \leq \text{EVDD0} < 2.7 \text{ V}$	$1/\text{fmck} + 200$		ns
			$1.6 \text{ V} \leq \text{EVDD0} < 1.8 \text{ V}$	$1/\text{fmck} + 400$		ns
$\overline{\text{SSI00}}$ hold time	tkssi	DAPmn = 0	$2.7 \text{ V} \leq \text{EVDD0} \leq 5.5 \text{ V}$	$1/\text{fmck} + 120$		ns
			$1.8 \text{ V} \leq \text{EVDD0} < 2.7 \text{ V}$	$1/\text{fmck} + 200$		ns
			$1.6 \text{ V} \leq \text{EVDD0} < 1.8 \text{ V}$	$1/\text{fmck} + 400$		ns
		DAPmn = 1	$2.7 \text{ V} \leq \text{EVDD0} \leq 5.5 \text{ V}$	120		ns
			$1.8 \text{ V} \leq \text{EVDD0} < 2.7 \text{ V}$	200		ns
			$1.6 \text{ V} \leq \text{EVDD0} < 1.8 \text{ V}$	400		ns

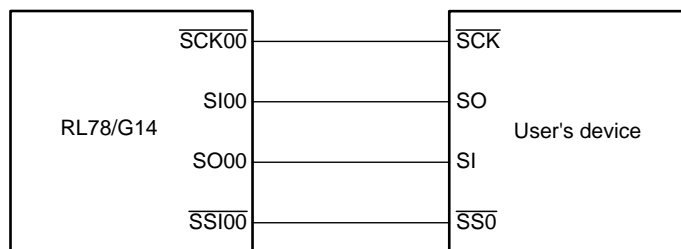
Caution Select the normal input buffer for the Slp pin and the normal output mode for the SOp pin and $\overline{\text{SCKp}}$ pin by using port input mode register g (PIMg) and port output mode register g (POMg).

Remark p: CSI number (p = 00), m: Unit number (m = 0), n: Channel number (n = 0), g: PIM number (g = 3, 5)

CSI mode connection diagram (during communication at same potential)



**CSI mode connection diagram (during communication at same potential)
(Slave Transmission of slave select input function (CSI00))**

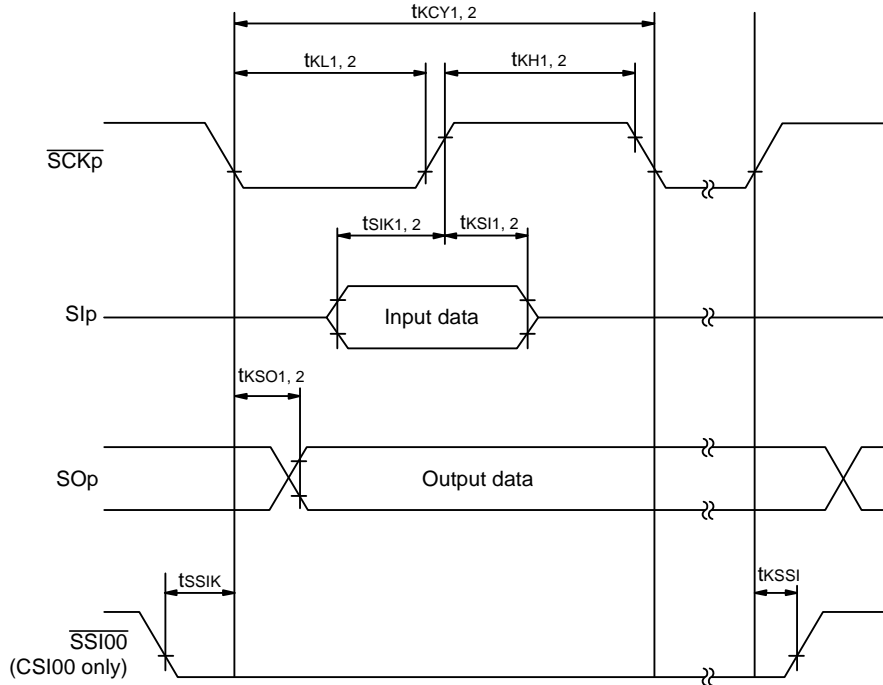


Remark 1. p: CSI number (p = 00, 01, 10, 11, 20, 21, 30, 31)

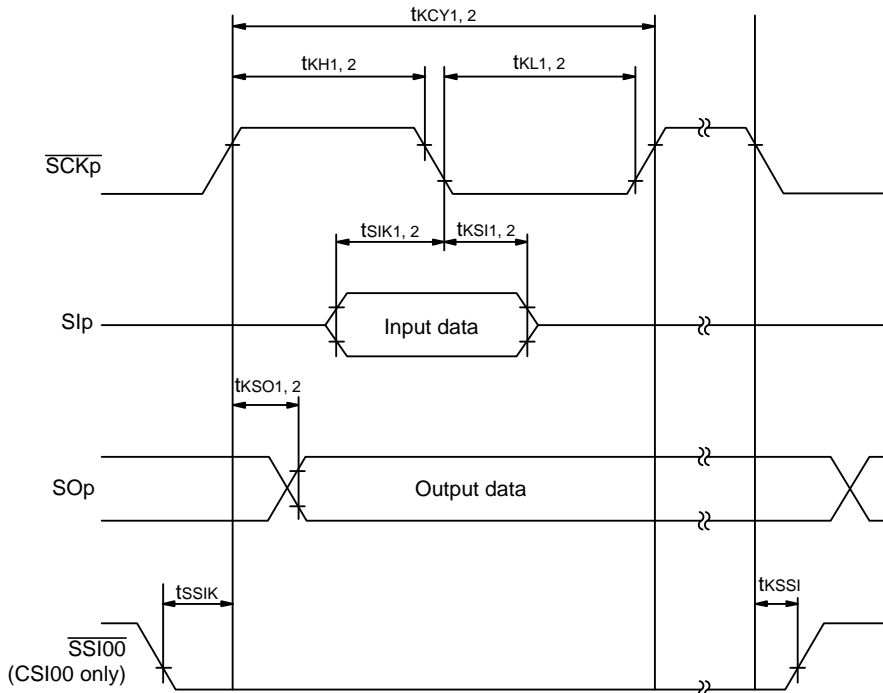
Remark 2. m: Unit number, n: Channel number (mn = 00 to 03, 10 to 13)

Caution The pins mounted depend on the product. Refer to 1.3.1 30-pin products to 1.3.10 100-pin products.

**CSI mode serial transfer timing (during communication at same potential)
(When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1.)**



**CSI mode serial transfer timing (during communication at same potential)
(When DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.)**



Remark 1. p: CSI number (p = 00, 01, 10, 11, 20, 21, 30, 31)

Remark 2. m: Unit number, n: Channel number (mn = 00 to 03, 10 to 13)

Caution The pins mounted depend on the product. Refer to 1.3.1 30-pin products to 1.3.10 100-pin products.

(5) During communication at same potential (simplified I²C mode)

(TA = -40 to +85 °C, 1.6 V ≤ EVDD0 = EVDD1 ≤ VDD ≤ 5.5 V, VSS = EVSS0 = EVSS1 = 0 V)

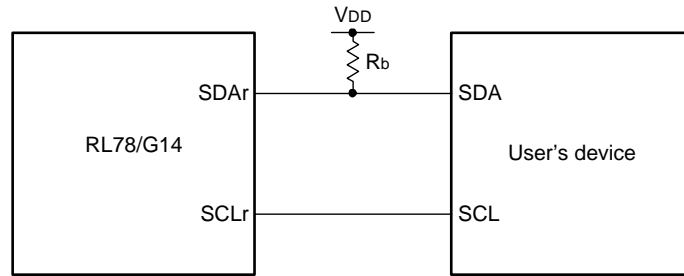
Parameter	Symbol	Conditions	MIN.	MAX.	Unit
SCLr clock frequency	f _{SCL}	2.7 V ≤ EVDD0 ≤ 5.5 V, Cb = 50 pF, Rb = 2.7 kΩ		1000	kHz
		1.8 V ≤ EVDD0 ≤ 5.5 V, Cb = 100 pF, Rb = 3 kΩ		400	kHz
		1.8 V ≤ EVDD0 < 2.7 V, Cb = 100 pF, Rb = 5 kΩ		300	kHz
		1.6 V ≤ EVDD0 < 1.8 V, Cb = 100 pF, Rb = 5 kΩ		250	kHz
Hold time when SCLr = "L"	t _{LOW}	2.7 V ≤ EVDD0 ≤ 5.5 V, Cb = 50 pF, Rb = 2.7 kΩ	475		ns
		1.8 V ≤ VDD0 ≤ 5.5 V, Cb = 100 pF, Rb = 3 kΩ	1150		ns
		1.8 V ≤ EVDD0 < 2.7 V, Cb = 100 pF, Rb = 5 kΩ	1550		ns
		1.6 V ≤ EVDD0 < 1.8 V, Cb = 100 pF, Rb = 5 kΩ	1850		ns
Hold time when SCLr = "H"	t _{HIGH}	2.7 V ≤ EVDD0 ≤ 5.5 V, Cb = 50 pF, Rb = 2.7 kΩ	475		ns
		1.8 V ≤ EVDD0 ≤ 5.5 V, Cb = 100 pF, Rb = 3 kΩ	1150		ns
		1.8 V ≤ EVDD0 < 2.7 V, Cb = 100 pF, Rb = 5 kΩ	1550		ns
		1.6 V ≤ EVDD0 < 1.8 V, Cb = 100 pF, Rb = 5 kΩ	1850		ns
Data setup time (reception)	t _{SU:DAT}	2.7 V ≤ EVDD0 ≤ 5.5 V, Cb = 50 pF, Rb = 2.7 kΩ	1/f _{MCK} + 85 Note		ns
		1.8 V ≤ EVDD0 ≤ 5.5 V, Cb = 100 pF, Rb = 3 kΩ	1/f _{MCK} + 145 Note		ns
		1.8 V ≤ EVDD0 < 2.7 V, Cb = 100 pF, Rb = 5 kΩ	1/f _{MCK} + 230 Note		ns
		1.6 V ≤ EVDD0 < 1.8 V, Cb = 100 pF, Rb = 5 kΩ	1/f _{MCK} + 290 Note		ns
Data hold time (transmission)	t _{HD:DAT}	2.7 V ≤ EVDD0 ≤ 5.5 V, Cb = 50 pF, Rb = 2.7 kΩ	0	305	ns
		1.8 V ≤ EVDD0 ≤ 5.5 V, Cb = 100 pF, Rb = 3 kΩ	0	355	ns
		1.8 V ≤ EVDD0 < 2.7 V, Cb = 100 pF, Rb = 5 kΩ	0	405	ns
		1.6 V ≤ EVDD0 < 1.8 V, Cb = 100 pF, Rb = 5 kΩ	0	405	ns

Note Set the f_{MCK} value to keep the hold time of SCLr = "L" and SCLr = "H".

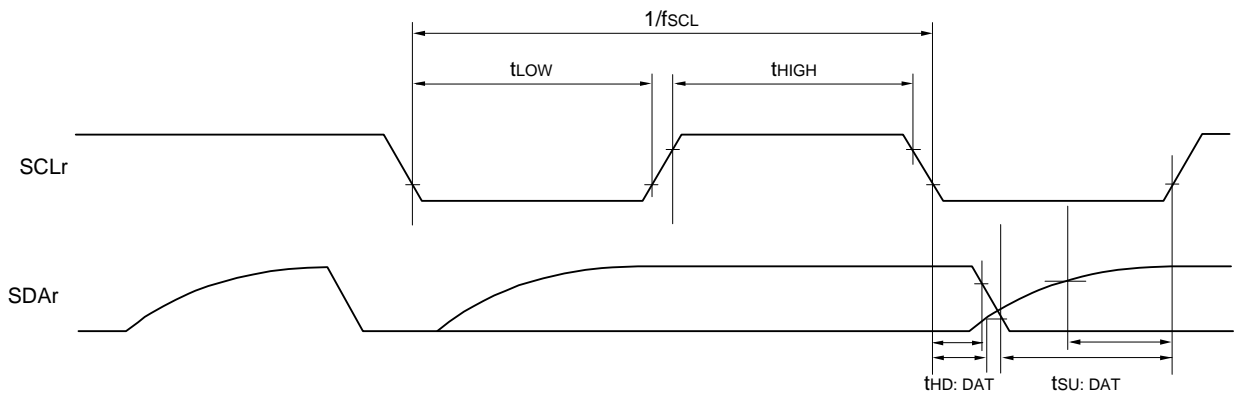
(**Caution** and **Remarks** are listed on the next page.)

Caution The pins mounted depend on the product. Refer to 1.3.1 30-pin products to 1.3.10 100-pin products.

Simplified I²C mode connection diagram (during communication at same potential)



Simplified I²C mode serial transfer timing (during communication at same potential)



Caution Select the TTL input buffer and the N-ch open drain output (EV_{DD0} tolerance) mode for the SDAr pin and the N-ch open drain output (EV_{DD0} tolerance) mode for the SCLr pin by using port input mode register g (PIMg) and port output mode register h (POMh).

Remark 1. R_b[Ω]: Communication line (SDAr) pull-up resistance, C_b[F]: Communication line (SDAr, SCLr) load capacitance

Remark 2. r: IIC number (r = 00, 01, 10, 11, 20, 21, 30, 31), g: PIM number (g = 0, 1, 3 to 5, 14),
h: POM number (h = 0, 1, 3 to 5, 7, 14)

Remark 3. f_{MCK}: Serial array unit operation clock frequency
(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number (m = 0, 1),
n: Channel number (n = 0, 2), mn = 00 to 03, 10 to 13)

Caution The pins mounted depend on the product. Refer to 1.3.1 30-pin products to 1.3.10 100-pin products.

(6) Communication at different potential (2.5 V, 3 V) (UART mode) (dedicated baud rate generator output)

($T_A = -40$ to $+85$ °C, $1.8\text{ V} \leq EV_{DD0} = EV_{DD1} \leq V_{DD} \leq 5.5\text{ V}$, $V_{SS} = EV_{SS0} = EV_{SS1} = 0\text{ V}$)

(1/2)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Transfer rate Notes 1, 2		reception	$4.0\text{ V} \leq EV_{DD0} \leq 5.5\text{ V}$, $2.7\text{ V} \leq V_b \leq 4.0\text{ V}$			$f_{MCK}/6$ Note 1	bps
				Theoretical value of the maximum transfer rate $f_{CLK} = 32\text{ MHz}$, $f_{MCK} = f_{CLK}$			5.3
			$2.7\text{ V} \leq EV_{DD0} < 4.0\text{ V}$, $2.3\text{ V} \leq V_b \leq 2.7\text{ V}$			$f_{MCK}/6$ Note 1	bps
				Theoretical value of the maximum transfer rate $f_{CLK} = 32\text{ MHz}$, $f_{MCK} = f_{CLK}$			5.3
			$1.8\text{ V} \leq EV_{DD0} < 3.3\text{ V}$, $1.6\text{ V} \leq V_b \leq 2.0\text{ V}$			$f_{MCK}/6$ Note 1 to Note 3	bps
				Theoretical value of the maximum transfer rate $f_{CLK} = 8\text{ MHz}$, $f_{MCK} = f_{CLK}$			1.3

Note 1. Transfer rate in the SNOOZE mode : MAX. 9600 bps, MIN. 4800 bps

Note 2. Use it with $EV_{DD0} \geq V_b$.

Note 3. The following conditions are required for low voltage interface when $EV_{DD0} < V_{DD}$.

$2.4\text{ V} \leq EV_{DD0} < 2.7\text{ V}$: MAX. 2.6 Mbps

$1.8\text{ V} \leq EV_{DD0} < 2.4\text{ V}$: MAX. 1.3 Mbps

$1.6\text{ V} \leq EV_{DD0} < 1.8\text{ V}$: MAX. 0.6 Mbps

Caution Select the TTL input buffer for the RxDq pin and the N-ch open drain output (EV_{DD0} tolerance) mode for the TxDq pin by using port input mode register g (PIMg) and port output mode register g (POMg).

Remark 1. $V_b[V]$: Communication line voltage

Remark 2. q: UART number (q = 0 to 3), g: PIM and POM number (g = 0, 1, 5, 14)

Remark 3. f_{MCK} : Serial array unit operation clock frequency

(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number, n: Channel number (mn = 00 to 03, 10 to 13))

Remark 4. V_{IH} and V_{IL} below are observation points for the AC characteristics of the serial array unit when communicating at different potentials in UART mode.

$4.0\text{ V} \leq EV_{DD0} \leq 5.5\text{ V}$, $2.7\text{ V} \leq V_b \leq 4.0\text{ V}$: $V_{IH} = 2.2\text{ V}$, $V_{IL} = 0.8\text{ V}$

$2.7\text{ V} \leq EV_{DD0} < 4.0\text{ V}$, $2.3\text{ V} \leq V_b \leq 2.7\text{ V}$: $V_{IH} = 2.0\text{ V}$, $V_{IL} = 0.5\text{ V}$

$1.8\text{ V} \leq EV_{DD0} < 3.3\text{ V}$, $1.6\text{ V} \leq V_b \leq 2.0\text{ V}$: $V_{IH} = 1.50\text{ V}$, $V_{IL} = 0.32\text{ V}$

Remark 5. UART2 cannot communicate at different potential when bit 1 (PIOR01) of peripheral I/O redirection register 0 (PIOR0) is 1.

Caution The pins mounted depend on the product. Refer to 1.3.1 30-pin products to 1.3.10 100-pin products.

(6) Communication at different potential (2.5 V, 3 V) (UART mode) (dedicated baud rate generator output)

(TA = -40 to +85 °C, 1.8 V ≤ EVDD0 = EVDD1 ≤ VDD ≤ 5.5 V, VSS = EVSS0 = EVSS1 = 0 V)

(2/2)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Transfer rate		transmission	4.0 V ≤ EVDD0 ≤ 5.5 V, 2.7 V ≤ Vb ≤ 4.0 V			Notes 1, 2	bps
				Theoretical value of the maximum transfer rate Cb = 50 pF, Rb = 1.4 kΩ, Vb = 2.7 V		2.8 Note 3	Mbps
			2.7 V ≤ EVDD0 < 4.0 V, 2.3 V ≤ Vb ≤ 2.7 V			Notes 2, 4	bps
				Theoretical value of the maximum transfer rate Cb = 50 pF, Rb = 2.7 kΩ, Vb = 2.3 V		1.2 Note 5	Mbps
			1.8 V ≤ EVDD0 < 3.3 V, 1.6 V ≤ Vb ≤ 2.0 V			Notes 2, 6, 7	bps
				Theoretical value of the maximum transfer rate Cb = 50 pF, Rb = 5.5 kΩ, Vb = 1.6 V		0.40 Note 8	Mbps

Note 1. The smaller maximum transfer rate derived by using fmck/6 or the following expression is the valid maximum transfer rate.

Expression for calculating the transfer rate when 4.0 V ≤ EVDD0 ≤ 5.5 V and 2.7 V ≤ Vb ≤ 4.0 V

$$\text{Maximum transfer rate} = \frac{1}{\{-C_b \times R_b \times \ln(1 - \frac{2.2}{V_b})\} \times 3} \text{ [bps]}$$

$$\text{Baud rate error (theoretical value)} = \frac{\frac{1}{\text{Transfer rate} \times 2} - \{-C_b \times R_b \times \ln(1 - \frac{2.2}{V_b})\}}{\left(\frac{1}{\text{Transfer rate}}\right) \times \text{Number of transferred bits}} \times 100 \text{ [%]}$$

* This value is the theoretical value of the relative difference between the transmission and reception sides.

Note 2. Transfer rate in the SNOOZE mode: MAX. 9600 bps, MIN. 4800 bps

Note 3. This value as an example is calculated when the conditions described in the "Conditions" column are met. Refer to Note 1 above to calculate the maximum transfer rate under conditions of the customer.

Note 4. The smaller maximum transfer rate derived by using fmck/6 or the following expression is the valid maximum transfer rate.

Expression for calculating the transfer rate when 2.7 V ≤ EVDD0 < 4.0 V and 2.3 V ≤ Vb ≤ 2.7 V

$$\text{Maximum transfer rate} = \frac{1}{\{-C_b \times R_b \times \ln(1 - \frac{2.0}{V_b})\} \times 3} \text{ [bps]}$$

$$\text{Baud rate error (theoretical value)} = \frac{\frac{1}{\text{Transfer rate} \times 2} - \{-C_b \times R_b \times \ln(1 - \frac{2.0}{V_b})\}}{\left(\frac{1}{\text{Transfer rate}}\right) \times \text{Number of transferred bits}} \times 100 \text{ [%]}$$

* This value is the theoretical value of the relative difference between the transmission and reception sides.

Note 5. This value as an example is calculated when the conditions described in the "Conditions" column are met. Refer to Note 4 above to calculate the maximum transfer rate under conditions of the customer.

Note 6. Use it with EVDD0 ≥ Vb.

Note 7. The smaller maximum transfer rate derived by using $f_{mck}/6$ or the following expression is the valid maximum transfer rate.

Expression for calculating the transfer rate when $1.8\text{ V} \leq E_{VDD0} < 3.3\text{ V}$ and $1.6\text{ V} \leq V_b \leq 2.0\text{ V}$

$$\text{Maximum transfer rate} = \frac{1}{\{-C_b \times R_b \times \ln(1 - \frac{1.5}{V_b})\} \times 3} \text{ [bps]}$$

$$\text{Baud rate error (theoretical value)} = \frac{\frac{1}{\text{Transfer rate} \times 2} - \{-C_b \times R_b \times \ln(1 - \frac{1.5}{V_b})\}}{(\frac{1}{\text{Transfer rate}}) \times \text{Number of transferred bits}} \times 100 \text{ [%]}$$

* This value is the theoretical value of the relative difference between the transmission and reception sides.

Note 8. This value as an example is calculated when the conditions described in the "Conditions" column are met. Refer to Note 7 above to calculate the maximum transfer rate under conditions of the customer.

Caution Select the TTL input buffer for the RxDq pin and the N-ch open drain output (EVDD0 tolerance) mode for the TxDq pin by using port input mode register g (PIMg) and port output mode register g (POMg).

Remark 1. $R_b[\Omega]$: Communication line (TxDq) pull-up resistance,
 $C_b[F]$: Communication line (TxDq) load capacitance, $V_b[V]$: Communication line voltage

Remark 2. q: UART number (q = 0 to 3), g: PIM and POM number (g = 0, 1, 5, 14)

Remark 3. f_{mck} : Serial array unit operation clock frequency
 (Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn).
 m: Unit number, n: Channel number (mn = 00 to 03, 10 to 13))

Remark 4. V_{IH} and V_{IL} below are observation points for the AC characteristics of the serial array unit when communicating at different potentials in UART mode.

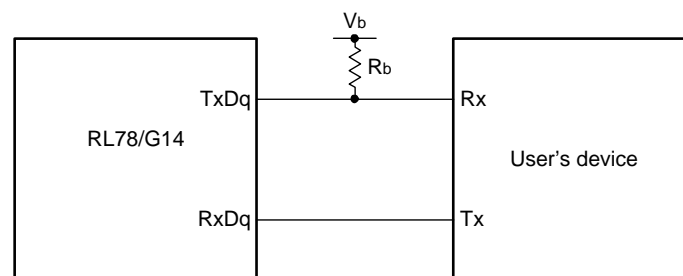
$4.0\text{ V} \leq E_{VDD0} \leq 5.5\text{ V}$, $2.7\text{ V} \leq V_b \leq 4.0\text{ V}$: $V_{IH} = 2.2\text{ V}$, $V_{IL} = 0.8\text{ V}$

$2.7\text{ V} \leq E_{VDD0} < 4.0\text{ V}$, $2.3\text{ V} \leq V_b \leq 2.7\text{ V}$: $V_{IH} = 2.0\text{ V}$, $V_{IL} = 0.5\text{ V}$

$1.8\text{ V} \leq E_{VDD0} < 3.3\text{ V}$, $1.6\text{ V} \leq V_b \leq 2.0\text{ V}$: $V_{IH} = 1.50\text{ V}$, $V_{IL} = 0.32\text{ V}$

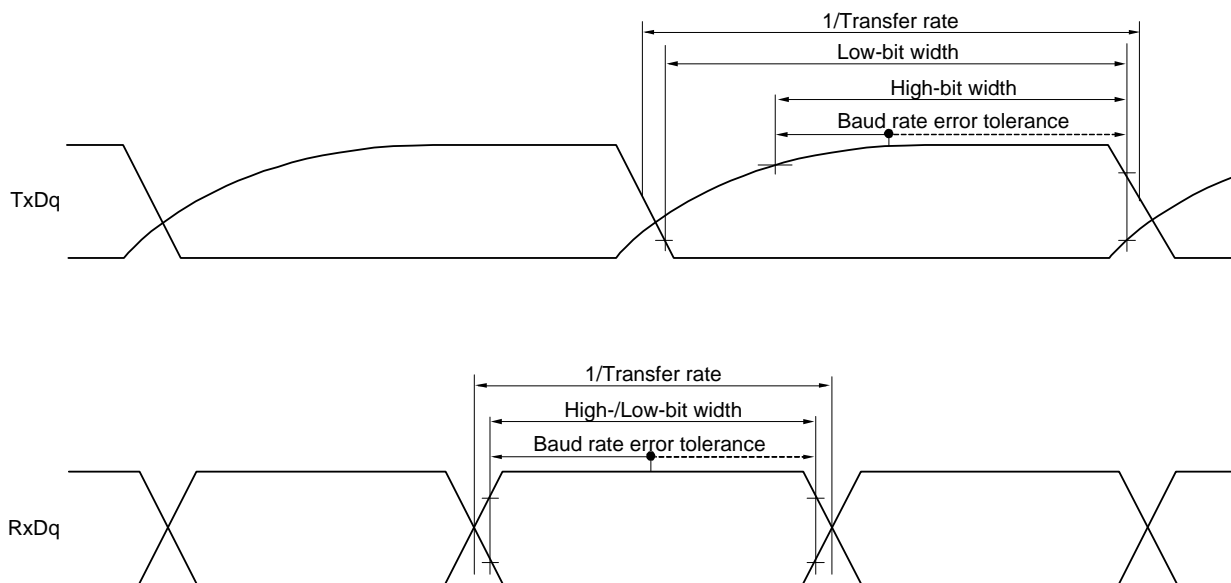
Remark 5. UART2 cannot communicate at different potential when bit 1 (PIOR01) of peripheral I/O redirection register 0 (PIOR0) is 1.

UART mode connection diagram (during communication at different potential)



Caution The pins mounted depend on the product. Refer to 1.3.1 30-pin products to 1.3.10 100-pin products.

UART mode bit width (during communication at different potential) (reference)



Caution Select the TTL input buffer for the RxDq pin and the N-ch open drain output (EVDD0 tolerance) mode for the TxDq pin by using port input mode register g (PIMg) and port output mode register g (POMg).

Remark 1. $R_b[\Omega]$: Communication line (TxDq) pull-up resistance, $V_b[V]$: Communication line voltage

Remark 2. q: UART number (q = 0 to 3), g: PIM and POM number (g = 0, 1, 5, 14)

Caution The pins mounted depend on the product. Refer to 1.3.1 30-pin products to 1.3.10 100-pin products.

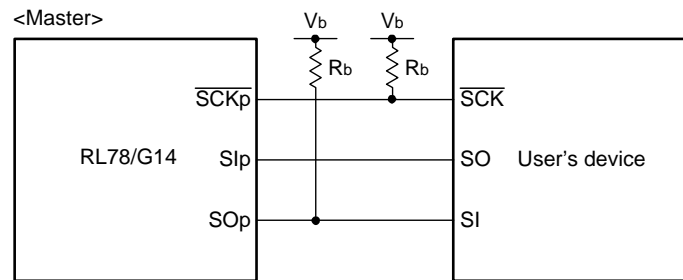
**(7) Communication at different potential (2.5 V, 3 V) (fmck/2) (CSI mode) (master mode, $\overline{\text{SCKp}}$... internal clock output)
($T_A = -40$ to $+85$ °C, $2.7\text{ V} \leq \text{EVDD0} = \text{EVDD1} \leq \text{VDD} \leq 5.5\text{ V}$, $\text{VSS} = \text{EVSS0} = \text{EVSS1} = 0\text{ V}$)**

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
$\overline{\text{SCKp}}$ cycle time	tkCY1	$4.0\text{ V} \leq \text{EVDD0} \leq 5.5\text{ V}$, $2.7\text{ V} \leq \text{Vb} \leq 4.0\text{ V}$, $\text{Cb} = 20\text{ pF}$, $\text{Rb} = 1.4\text{ k}\Omega$	200 Note 1			ns
		$2.7\text{ V} \leq \text{EVDD0} < 4.0\text{ V}$, $2.3\text{ V} \leq \text{Vb} \leq 2.7\text{ V}$, $\text{Cb} = 20\text{ pF}$, $\text{Rb} = 2.7\text{ k}\Omega$	300 Note 1			ns
$\overline{\text{SCKp}}$ high-level width	tkH1	$4.0\text{ V} \leq \text{EVDD0} \leq 5.5\text{ V}$, $2.7\text{ V} \leq \text{Vb} \leq 4.0\text{ V}$, $\text{Cb} = 20\text{ pF}$, $\text{Rb} = 1.4\text{ k}\Omega$	tkCY1/2 - 50			ns
		$2.7\text{ V} \leq \text{EVDD0} < 4.0\text{ V}$, $2.3\text{ V} \leq \text{Vb} \leq 2.7\text{ V}$, $\text{Cb} = 20\text{ pF}$, $\text{Rb} = 2.7\text{ k}\Omega$	tkCY1/2 - 120			ns
$\overline{\text{SCKp}}$ low-level width	tkL1	$4.0\text{ V} \leq \text{EVDD0} \leq 5.5\text{ V}$, $2.7\text{ V} \leq \text{Vb} \leq 4.0\text{ V}$, $\text{Cb} = 20\text{ pF}$, $\text{Rb} = 1.4\text{ k}\Omega$	tkCY1/2 - 7			ns
		$2.7\text{ V} \leq \text{EVDD0} < 4.0\text{ V}$, $2.3\text{ V} \leq \text{Vb} \leq 2.7\text{ V}$, $\text{Cb} = 20\text{ pF}$, $\text{Rb} = 2.7\text{ k}\Omega$	tkCY1/2 - 10			ns
Slp setup time (to $\overline{\text{SCKp}}\uparrow$) Note 2	tsIK1	$4.0\text{ V} \leq \text{EVDD0} \leq 5.5\text{ V}$, $2.7\text{ V} \leq \text{Vb} \leq 4.0\text{ V}$, $\text{Cb} = 20\text{ pF}$, $\text{Rb} = 1.4\text{ k}\Omega$	58			ns
		$2.7\text{ V} \leq \text{EVDD0} < 4.0\text{ V}$, $2.3\text{ V} \leq \text{Vb} \leq 2.7\text{ V}$, $\text{Cb} = 20\text{ pF}$, $\text{Rb} = 2.7\text{ k}\Omega$	121			ns
Slp hold time (from $\overline{\text{SCKp}}\uparrow$) Note 2	tkSI1	$4.0\text{ V} \leq \text{EVDD0} \leq 5.5\text{ V}$, $2.7\text{ V} \leq \text{Vb} \leq 4.0\text{ V}$, $\text{Cb} = 20\text{ pF}$, $\text{Rb} = 1.4\text{ k}\Omega$	10			ns
		$2.7\text{ V} \leq \text{EVDD0} < 4.0\text{ V}$, $2.3\text{ V} \leq \text{Vb} \leq 2.7\text{ V}$, $\text{Cb} = 20\text{ pF}$, $\text{Rb} = 2.7\text{ k}\Omega$	10			ns
Delay time from $\overline{\text{SCKp}}\downarrow$ to SOP output Note 2	tkSO1	$4.0\text{ V} \leq \text{EVDD0} \leq 5.5\text{ V}$, $2.7\text{ V} \leq \text{Vb} \leq 4.0\text{ V}$, $\text{Cb} = 20\text{ pF}$, $\text{Rb} = 1.4\text{ k}\Omega$			60	ns
		$2.7\text{ V} \leq \text{EVDD0} < 4.0\text{ V}$, $2.3\text{ V} \leq \text{Vb} \leq 2.7\text{ V}$, $\text{Cb} = 20\text{ pF}$, $\text{Rb} = 2.7\text{ k}\Omega$			130	ns
Slp setup time (to $\overline{\text{SCKp}}\downarrow$) Note 3	tsIK1	$4.0\text{ V} \leq \text{EVDD0} \leq 5.5\text{ V}$, $2.7\text{ V} \leq \text{Vb} \leq 4.0\text{ V}$, $\text{Cb} = 20\text{ pF}$, $\text{Rb} = 1.4\text{ k}\Omega$	23			ns
		$2.7\text{ V} \leq \text{EVDD0} < 4.0\text{ V}$, $2.3\text{ V} \leq \text{Vb} \leq 2.7\text{ V}$, $\text{Cb} = 20\text{ pF}$, $\text{Rb} = 2.7\text{ k}\Omega$	33			ns
Slp hold time (from $\overline{\text{SCKp}}\downarrow$) Note 3	tkSI1	$4.0\text{ V} \leq \text{EVDD0} \leq 5.5\text{ V}$, $2.7\text{ V} \leq \text{Vb} \leq 4.0\text{ V}$, $\text{Cb} = 20\text{ pF}$, $\text{Rb} = 1.4\text{ k}\Omega$	10			ns
		$2.7\text{ V} \leq \text{EVDD0} < 4.0\text{ V}$, $2.3\text{ V} \leq \text{Vb} \leq 2.7\text{ V}$, $\text{Cb} = 20\text{ pF}$, $\text{Rb} = 2.7\text{ k}\Omega$	10			ns
Delay time from $\overline{\text{SCKp}}\uparrow$ to SOP output Note 3	tkSO1	$4.0\text{ V} \leq \text{EVDD0} \leq 5.5\text{ V}$, $2.7\text{ V} \leq \text{Vb} \leq 4.0\text{ V}$, $\text{Cb} = 20\text{ pF}$, $\text{Rb} = 1.4\text{ k}\Omega$			10	ns
		$2.7\text{ V} \leq \text{EVDD0} < 4.0\text{ V}$, $2.3\text{ V} \leq \text{Vb} \leq 2.7\text{ V}$, $\text{Cb} = 20\text{ pF}$, $\text{Rb} = 2.7\text{ k}\Omega$			10	ns

(Notes, Caution and Remarks are listed on the next page.)

Caution The pins mounted depend on the product. Refer to 1.3.1 30-pin products to 1.3.10 100-pin products.

CSI mode connection diagram (during communication at different potential)



Note 1. The value must also be $2/f_{CLK}$ or more.

Note 2. When $DAP_{mn} = 0$ and $CKP_{mn} = 0$, or $DAP_{mn} = 1$ and $CKP_{mn} = 1$.

Note 3. When $DAP_{mn} = 0$ and $CKP_{mn} = 1$, or $DAP_{mn} = 1$ and $CKP_{mn} = 0$.

Caution Select the TTL input buffer for the Slp pin and the N-ch open drain output (EVDD0 tolerance) mode for the SOp pin and SCKp pin by using port input mode register g (PIMg) and port output mode register g (POMg).

Remark 1. $R_b[\Omega]$: Communication line (\overline{SCKp} , SOp) pull-up resistance, $C_b[F]$: Communication line (\overline{SCKp} , SOp) load capacitance, $V_b[V]$: Communication line voltage

Remark 2. p: CSI number (p = 00, 01, 10, 20, 30, 31), m: Unit number (m = 0, 1), n: Channel number (n = 0 to 3), g: PIM and POM number (g = 0, 1, 3 to 5, 14)

Remark 3. V_{IH} and V_{IL} below are observation points for the AC characteristics of the serial array unit when communicating at different potentials in CSI mode.

$4.0\text{ V} \leq EV_{DD0} \leq 5.5\text{ V}$, $2.7\text{ V} \leq V_b \leq 4.0\text{ V}$: $V_{IH} = 2.2\text{ V}$, $V_{IL} = 0.8\text{ V}$

$2.7\text{ V} \leq EV_{DD0} < 4.0\text{ V}$, $2.3\text{ V} \leq V_b \leq 2.7\text{ V}$: $V_{IH} = 2.0\text{ V}$, $V_{IL} = 0.5\text{ V}$

Remark 4. CSI01 of 48-, 52-, 64-pin products, and CSI11 and CSI21 cannot communicate at different potential. Use other CSI for communication at different potential.

Remark 5. This specification is valid only when CSI00's peripheral I/O redirect function is not used.

Caution The pins mounted depend on the product. Refer to 1.3.1 30-pin products to 1.3.10 100-pin products.

(8) Communication at different potential (2.5 V, 3 V) (fmck/4) (CSI mode) (master mode, $\overline{\text{SCKp}}$... internal clock output)
($T_A = -40$ to $+85$ °C, $1.8 \text{ V} \leq \text{EVDD0} = \text{EVDD1} \leq \text{VDD} \leq 5.5 \text{ V}$, $\text{VSS} = \text{EVSS0} = \text{EVSS1} = 0 \text{ V}$) **(1/2)**

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
$\overline{\text{SCKp}}$ cycle time	tkCY1	$4.0 \text{ V} \leq \text{EVDD0} \leq 5.5 \text{ V}$, $2.7 \text{ V} \leq \text{Vb} \leq 4.0 \text{ V}$, $C_b = 30 \text{ pF}$, $R_b = 1.4 \text{ k}\Omega$	300 Note			ns
		$2.7 \text{ V} \leq \text{EVDD0} < 4.0 \text{ V}$, $2.3 \text{ V} \leq \text{Vb} \leq 2.7 \text{ V}$, $C_b = 30 \text{ pF}$, $R_b = 2.7 \text{ k}\Omega$	500 Note			ns
		$1.8 \text{ V} \leq \text{EVDD0} < 3.3 \text{ V}$, $1.6 \text{ V} \leq \text{Vb} \leq 2.0 \text{ V}$, $C_b = 30 \text{ pF}$, $R_b = 5.5 \text{ k}\Omega$	1150 Note			ns
$\overline{\text{SCKp}}$ high-level width	tkH1	$4.0 \text{ V} \leq \text{EVDD0} \leq 5.5 \text{ V}$, $2.7 \text{ V} \leq \text{Vb} \leq 4.0 \text{ V}$, $C_b = 30 \text{ pF}$, $R_b = 1.4 \text{ k}\Omega$	tkCY1/2 - 75			ns
		$2.7 \text{ V} \leq \text{EVDD0} < 4.0 \text{ V}$, $2.3 \text{ V} \leq \text{Vb} \leq 2.7 \text{ V}$, $C_b = 30 \text{ pF}$, $R_b = 2.7 \text{ k}\Omega$	tkCY1/2 - 170			ns
		$1.8 \text{ V} \leq \text{EVDD0} < 3.3 \text{ V}$, $1.6 \text{ V} \leq \text{Vb} \leq 2.0 \text{ V}$, $C_b = 30 \text{ pF}$, $R_b = 5.5 \text{ k}\Omega$	tkCY1/2 - 458			ns
$\overline{\text{SCKp}}$ low-level width	tkL1	$4.0 \text{ V} \leq \text{EVDD0} \leq 5.5 \text{ V}$, $2.7 \text{ V} \leq \text{Vb} \leq 4.0 \text{ V}$, $C_b = 30 \text{ pF}$, $R_b = 1.4 \text{ k}\Omega$	tkCY1/2 - 12			ns
		$2.7 \text{ V} \leq \text{EVDD0} < 4.0 \text{ V}$, $2.3 \text{ V} \leq \text{Vb} \leq 2.7 \text{ V}$, $C_b = 30 \text{ pF}$, $R_b = 2.7 \text{ k}\Omega$	tkCY1/2 - 18			ns
		$1.8 \text{ V} \leq \text{EVDD0} < 3.3 \text{ V}$, $1.6 \text{ V} \leq \text{Vb} \leq 2.0 \text{ V}$, $C_b = 30 \text{ pF}$, $R_b = 5.5 \text{ k}\Omega$	tkCY1/2 - 50			ns

Note 1. The value must also be $4/f_{\text{CLK}}$ or more.

Caution 1. Select the TTL input buffer for the SIp pin and the N-ch open drain output (EVDD0 tolerance) mode for the SOp pin and $\overline{\text{SCKp}}$ pin by using port input mode register g (PIMg) and port output mode register g (POMg).

Caution 2. Use it with $\text{EVDD0} \geq \text{Vb}$.

Remark 1. $R_b[\Omega]$: Communication line ($\overline{\text{SCKp}}$, SOp) pull-up resistance, $C_b[\text{F}]$: Communication line ($\overline{\text{SCKp}}$, SOp) load capacitance, $V_b[\text{V}]$: Communication line voltage

Remark 2. p: CSI number (p = 00, 01, 10, 20, 30, 31), m: Unit number (m = 0, 1), n: Channel number (n = 0 to 3),
g: PIM and POM number (g = 0, 1, 3 to 5, 14)

Remark 3. V_{IH} and V_{IL} below are observation points for the AC characteristics of the serial array unit when communicating at different potentials in CSI mode.

$4.0 \text{ V} \leq \text{EVDD0} \leq 5.5 \text{ V}$, $2.7 \text{ V} \leq \text{Vb} \leq 4.0 \text{ V}$: $V_{\text{IH}} = 2.2 \text{ V}$, $V_{\text{IL}} = 0.8 \text{ V}$

$2.7 \text{ V} \leq \text{EVDD0} < 4.0 \text{ V}$, $2.3 \text{ V} \leq \text{Vb} \leq 2.7 \text{ V}$: $V_{\text{IH}} = 2.0 \text{ V}$, $V_{\text{IL}} = 0.5 \text{ V}$

$1.8 \text{ V} \leq \text{EVDD0} < 3.3 \text{ V}$, $1.6 \text{ V} \leq \text{Vb} \leq 2.0 \text{ V}$: $V_{\text{IH}} = 1.50 \text{ V}$, $V_{\text{IL}} = 0.32 \text{ V}$

Remark 4. 4. CSI01 of 48-, 52-, 64-pin products, and CSI11 and CSI21 cannot communicate at different potential. Use other CSI for communication at different potential.

Caution The pins mounted depend on the product. Refer to 1.3.1 30-pin products to 1.3.10 100-pin products.

(8) Communication at different potential (2.5 V, 3 V) (fmck/4) (CSI mode) (master mode, $\overline{\text{SCKp}}$... internal clock output)

($T_A = -40$ to $+85$ °C, $1.8 \text{ V} \leq \text{EVDD0} = \text{EVDD1} \leq \text{VDD} \leq 5.5 \text{ V}$, $\text{Vss} = \text{EVss0} = \text{EVss1} = 0 \text{ V}$)

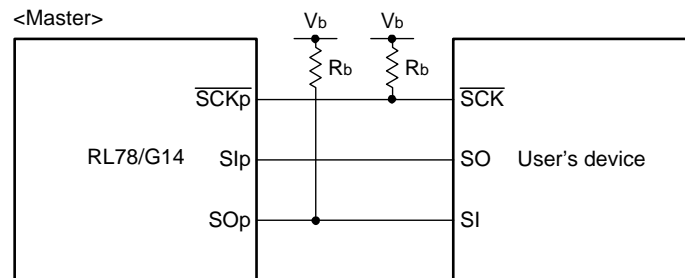
(2/2)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Slp setup time (to $\overline{\text{SCKp}}\uparrow$) Note 1	tSIK1	$4.0 \text{ V} \leq \text{EVDD0} \leq 5.5 \text{ V}$, $2.7 \text{ V} \leq \text{Vb} \leq 4.0 \text{ V}$, $C_b = 30 \text{ pF}$, $R_b = 1.4 \text{ k}\Omega$	81			ns
		$2.7 \text{ V} \leq \text{EVDD0} < 4.0 \text{ V}$, $2.3 \text{ V} \leq \text{Vb} \leq 2.7 \text{ V}$, $C_b = 30 \text{ pF}$, $R_b = 2.7 \text{ k}\Omega$	177			ns
		$1.8 \text{ V} \leq \text{EVDD0} < 3.3 \text{ V}$, $1.6 \text{ V} \leq \text{Vb} \leq 2.0 \text{ V}$, $C_b = 30 \text{ pF}$, $R_b = 5.5 \text{ k}\Omega$	479			ns
Slp hold time (from $\overline{\text{SCKp}}\uparrow$) Note 1	tKSI1	$4.0 \text{ V} \leq \text{EVDD0} \leq 5.5 \text{ V}$, $2.7 \text{ V} \leq \text{Vb} \leq 4.0 \text{ V}$, $C_b = 30 \text{ pF}$, $R_b = 1.4 \text{ k}\Omega$	19			ns
		$2.7 \text{ V} \leq \text{EVDD0} < 4.0 \text{ V}$, $2.3 \text{ V} \leq \text{Vb} \leq 2.7 \text{ V}$, $C_b = 30 \text{ pF}$, $R_b = 2.7 \text{ k}\Omega$	19			ns
		$1.8 \text{ V} \leq \text{EVDD0} < 3.3 \text{ V}$, $1.6 \text{ V} \leq \text{Vb} \leq 2.0 \text{ V}$, $C_b = 30 \text{ pF}$, $R_b = 5.5 \text{ k}\Omega$	19			ns
Delay time from $\overline{\text{SCKp}}\downarrow$ to SOp output Note 1	tKSO1	$4.0 \text{ V} \leq \text{EVDD0} \leq 5.5 \text{ V}$, $2.7 \text{ V} \leq \text{Vb} \leq 4.0 \text{ V}$, $C_b = 30 \text{ pF}$, $R_b = 1.4 \text{ k}\Omega$			100	ns
		$2.7 \text{ V} \leq \text{EVDD0} < 4.0 \text{ V}$, $2.3 \text{ V} \leq \text{Vb} \leq 2.7 \text{ V}$, $C_b = 30 \text{ pF}$, $R_b = 2.7 \text{ k}\Omega$			195	ns
		$1.8 \text{ V} \leq \text{EVDD0} < 3.3 \text{ V}$, $1.6 \text{ V} \leq \text{Vb} \leq 2.0 \text{ V}$, $C_b = 30 \text{ pF}$, $R_b = 5.5 \text{ k}\Omega$			483	ns
Slp setup time (to $\overline{\text{SCKp}}\downarrow$) Note 2	tSIK1	$4.0 \text{ V} \leq \text{EVDD0} \leq 5.5 \text{ V}$, $2.7 \text{ V} \leq \text{Vb} \leq 4.0 \text{ V}$, $C_b = 30 \text{ pF}$, $R_b = 1.4 \text{ k}\Omega$	44			ns
		$2.7 \text{ V} \leq \text{EVDD0} < 4.0 \text{ V}$, $2.3 \text{ V} \leq \text{Vb} \leq 2.7 \text{ V}$, $C_b = 30 \text{ pF}$, $R_b = 2.7 \text{ k}\Omega$	44			ns
		$1.8 \text{ V} \leq \text{EVDD0} < 3.3 \text{ V}$, $1.6 \text{ V} \leq \text{Vb} \leq 2.0 \text{ V}$, $C_b = 30 \text{ pF}$, $R_b = 5.5 \text{ k}\Omega$	110			ns
Slp hold time (from $\overline{\text{SCKp}}\downarrow$) Note 2	tKSI1	$4.0 \text{ V} \leq \text{EVDD0} \leq 5.5 \text{ V}$, $2.7 \text{ V} \leq \text{Vb} \leq 4.0 \text{ V}$, $C_b = 30 \text{ pF}$, $R_b = 1.4 \text{ k}\Omega$	19			ns
		$2.7 \text{ V} \leq \text{EVDD0} < 4.0 \text{ V}$, $2.3 \text{ V} \leq \text{Vb} \leq 2.7 \text{ V}$, $C_b = 30 \text{ pF}$, $R_b = 2.7 \text{ k}\Omega$	19			ns
		$1.8 \text{ V} \leq \text{EVDD0} < 3.3 \text{ V}$, $1.6 \text{ V} \leq \text{Vb} \leq 2.0 \text{ V}$, $C_b = 30 \text{ pF}$, $R_b = 5.5 \text{ k}\Omega$	19			ns
Delay time from $\overline{\text{SCKp}}\uparrow$ to SOp output Note 2	tKSO1	$4.0 \text{ V} \leq \text{EVDD0} \leq 5.5 \text{ V}$, $2.7 \text{ V} \leq \text{Vb} \leq 4.0 \text{ V}$, $C_b = 30 \text{ pF}$, $R_b = 1.4 \text{ k}\Omega$			25	ns
		$2.7 \text{ V} \leq \text{EVDD0} < 4.0 \text{ V}$, $2.3 \text{ V} \leq \text{Vb} \leq 2.7 \text{ V}$, $C_b = 30 \text{ pF}$, $R_b = 2.7 \text{ k}\Omega$			25	ns
		$1.8 \text{ V} \leq \text{EVDD0} < 3.3 \text{ V}$, $1.6 \text{ V} \leq \text{Vb} \leq 2.0 \text{ V}$, $C_b = 30 \text{ pF}$, $R_b = 5.5 \text{ k}\Omega$			25	ns

(Notes, Caution and Remarks are listed on the next page.)

Caution The pins mounted depend on the product. Refer to 1.3.1 30-pin products to 1.3.10 100-pin products.

CSI mode connection diagram (during communication at different potential)



Note 1. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1.

Note 2. When DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

Caution 1. Select the TTL input buffer for the Slp pin and the N-ch open drain output (EVDD0 tolerance) mode for the SOp pin and SCKp pin by using port input mode register g (PIMg) and port output mode register g (POMg).

Caution 2. Use it with $EVDD0 \geq V_b$.

Remark 1. $R_b[\Omega]$: Communication line (\overline{SCKp} , SOp) pull-up resistance, $C_b[F]$: Communication line (\overline{SCKp} , SOp) load capacitance, $V_b[V]$: Communication line voltage

Remark 2. p: CSI number (p = 00, 01, 10, 20, 30, 31), m: Unit number (m = 0, 1), n: Channel number (n = 0 to 3),
g: PIM and POM number (g = 0, 1, 3 to 5, 14)

Remark 3. V_{IH} and V_{IL} below are observation points for the AC characteristics of the serial array unit when communicating at different potentials in CSI mode.

$4.0\text{ V} \leq EVDD0 \leq 5.5\text{ V}$, $2.7\text{ V} \leq V_b \leq 4.0\text{ V}$: $V_{IH} = 2.2\text{ V}$, $V_{IL} = 0.8\text{ V}$

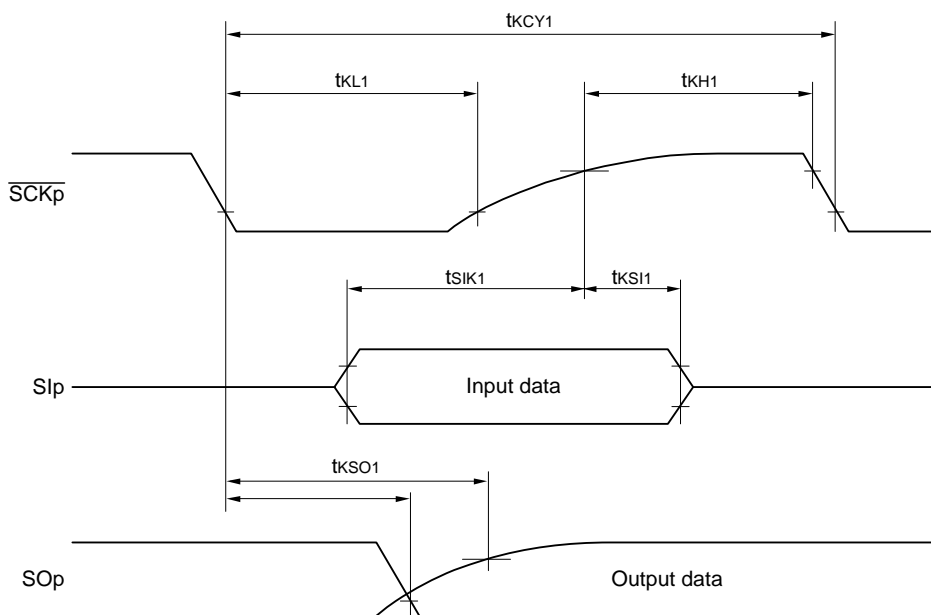
$2.7\text{ V} \leq EVDD0 < 4.0\text{ V}$, $2.3\text{ V} \leq V_b \leq 2.7\text{ V}$: $V_{IH} = 2.0\text{ V}$, $V_{IL} = 0.5\text{ V}$

$1.8\text{ V} \leq EVDD0 < 3.3\text{ V}$, $1.6\text{ V} \leq V_b \leq 2.0\text{ V}$: $V_{IH} = 1.50\text{ V}$, $V_{IL} = 0.32\text{ V}$

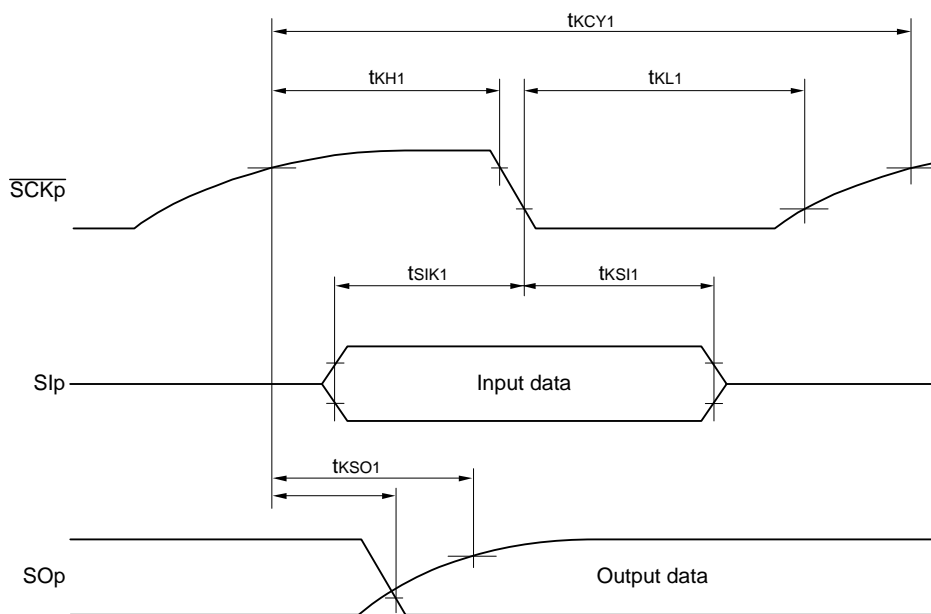
Remark 4. CSI01 of 48-, 52-, 64-pin products, and CSI11 and CSI21 cannot communicate at different potential. Use other CSI for communication at different potential.

Caution The pins mounted depend on the product. Refer to 1.3.1 30-pin products to 1.3.10 100-pin products.

**CSI mode serial transfer timing (master mode) (during communication at different potential)
(When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1.)**



**CSI mode serial transfer timing (master mode) (during communication at different potential)
(When DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.)**



Caution Select the TTL input buffer for the Slp pin and the N-ch open drain output (EVDD0 tolerance) mode for the SOp pin and \overline{SCKp} pin by using port input mode register g (PIMg) and port output mode register g (POMg).

Remark 1. p: CSI number (p = 00, 01, 10, 20, 30, 31), m: Unit number (m = 0, 1), n: Channel number (n = 0 to 3), g: PIM and POM number (g = 0, 1, 3 to 5, 14)

Remark 2. CSI01 of 48-, 52-, 64-pin products, and CSI11 and CSI21 cannot communicate at different potential. Use other CSI for communication at different potential.

Caution The pins mounted depend on the product. Refer to 1.3.1 30-pin products to 1.3.10 100-pin products.

(9) Communication at different potential (2.5 V, 3 V) (CSI mode) (slave mode, $\overline{\text{SCKp}}$... external clock input)

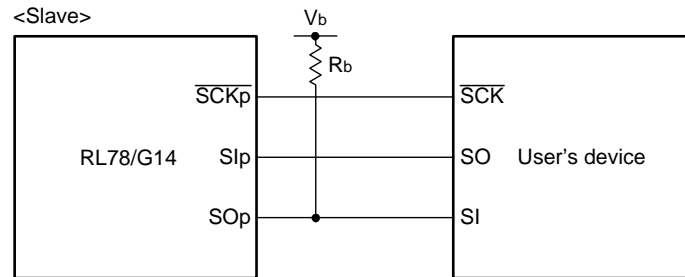
($T_A = -40$ to $+85$ °C, $1.8 \text{ V} \leq \text{EVDD0} = \text{EVDD1} \leq \text{VDD} \leq 5.5 \text{ V}$, $\text{VSS} = \text{EVSS0} = \text{EVSS1} = 0 \text{ V}$)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
$\overline{\text{SCKp}}$ cycle time Note 1	tkCY2	$4.0 \text{ V} \leq \text{EVDD0} \leq 5.5 \text{ V}$, $2.7 \text{ V} \leq \text{Vb} \leq 4.0 \text{ V}$	$24 \text{ MHz} \leq \text{fmCK}$	14/fmCK		ns
			$20 \text{ MHz} < \text{fmCK} \leq 24 \text{ MHz}$	12/fmCK		ns
			$8 \text{ MHz} < \text{fmCK} \leq 20 \text{ MHz}$	10/fmCK		ns
			$4 \text{ MHz} < \text{fmCK} \leq 8 \text{ MHz}$	8/fmCK		ns
			$\text{fmCK} \leq 4 \text{ MHz}$	6/fmCK		ns
		$2.7 \text{ V} \leq \text{EVDD0} < 4.0 \text{ V}$, $2.3 \text{ V} \leq \text{Vb} \leq 2.7 \text{ V}$	$24 \text{ MHz} < \text{fmCK}$	20/fmCK		ns
			$20 \text{ MHz} < \text{fmCK} \leq 24 \text{ MHz}$	16/fmCK		ns
			$16 \text{ MHz} < \text{fmCK} \leq 20 \text{ MHz}$	14/fmCK		ns
			$8 \text{ MHz} < \text{fmCK} \leq 16 \text{ MHz}$	12/fmCK		ns
			$4 \text{ MHz} < \text{fmCK} \leq 8 \text{ MHz}$	8/fmCK		ns
		$1.8 \text{ V} \leq \text{EVDD0} < 3.3 \text{ V}$, $1.6 \text{ V} \leq \text{Vb} \leq 2.0 \text{ V}$ Note 2	$24 \text{ MHz} \leq \text{fmCK}$	48/fmCK		ns
			$20 \text{ MHz} < \text{fmCK} \leq 24 \text{ MHz}$	36/fmCK		ns
			$16 \text{ MHz} < \text{fmCK} \leq 20 \text{ MHz}$	32/fmCK		ns
			$8 \text{ MHz} < \text{fmCK} \leq 16 \text{ MHz}$	26/fmCK		ns
			$4 \text{ MHz} < \text{fmCK} \leq 8 \text{ MHz}$	16/fmCK		ns
		$\text{fmCK} \leq 4 \text{ MHz}$	10/fmCK		ns	
		$4.0 \text{ V} \leq \text{EVDD0} \leq 5.5 \text{ V}$, $2.7 \text{ V} \leq \text{Vb} \leq 4.0 \text{ V}$	tkCY2/2 - 12		ns	
			$2.7 \text{ V} \leq \text{EVDD0} < 4.0 \text{ V}$, $2.3 \text{ V} \leq \text{Vb} \leq 2.7 \text{ V}$	tkCY2/2 - 18		ns
				$1.8 \text{ V} \leq \text{EVDD0} < 3.3 \text{ V}$, $1.6 \text{ V} \leq \text{Vb} \leq 2.0 \text{ V}$ Note 2	tkCY2/2 - 50	
		Slp setup time (to $\overline{\text{SCKp}}\uparrow$) Note 3	tSIK2	$2.7 \text{ V} \leq \text{EVDD0} < 5.5 \text{ V}$	1/fmCK + 20	
$1.8 \text{ V} \leq \text{EVDD0} < 3.3 \text{ V}$	1/fmCK + 30				ns	
Slp hold time (from $\overline{\text{SCKp}}\uparrow$) Note 4	tkSI2		1/fmCK + 31		ns	
Delay time from $\overline{\text{SCKp}}\downarrow$ to SOp output Note 5	tkSO2	$4.0 \text{ V} \leq \text{EVDD0} \leq 5.5 \text{ V}$, $2.7 \text{ V} \leq \text{Vb} \leq 4.0 \text{ V}$, $C_b = 30 \text{ pF}$, $R_b = 1.4 \text{ k}\Omega$	1/fmCK + 250		2/fmCK + 120	ns
		$2.7 \text{ V} \leq \text{EVDD0} < 4.0 \text{ V}$, $2.3 \text{ V} \leq \text{Vb} \leq 2.7 \text{ V}$, $C_b = 30 \text{ pF}$, $R_b = 2.7 \text{ k}\Omega$			2/fmCK + 214	ns
		$1.8 \text{ V} \leq \text{EVDD0} < 3.3 \text{ V}$, $1.6 \text{ V} \leq \text{Vb} \leq 2.0 \text{ V}$ Note 2, $C_b = 30 \text{ pF}$, $R_b = 5.5 \text{ k}\Omega$			2/fmCK + 573	ns

(Notes, Caution and Remarks are listed on the next page.)

Caution The pins mounted depend on the product. Refer to 1.3.1 30-pin products to 1.3.10 100-pin products.

CSI mode connection diagram (during communication at different potential)



Note 1. Transfer rate in the SNOOZE mode: MAX. 1 Mbps

Note 2. Use it with $EV_{DD0} \geq V_b$.

Note 3. When $DAP_{mn} = 0$ and $CKP_{mn} = 0$, or $DAP_{mn} = 1$ and $CKP_{mn} = 1$. The Slp setup time becomes “to $\overline{SCKp}\downarrow$ ” when $DAP_{mn} = 0$ and $CKP_{mn} = 1$, or $DAP_{mn} = 1$ and $CKP_{mn} = 0$.

Note 4. When $DAP_{mn} = 0$ and $CKP_{mn} = 0$, or $DAP_{mn} = 1$ and $CKP_{mn} = 1$. The Slp hold time becomes “from $\overline{SCKp}\downarrow$ ” when $DAP_{mn} = 0$ and $CKP_{mn} = 1$, or $DAP_{mn} = 1$ and $CKP_{mn} = 0$.

Note 5. When $DAP_{mn} = 0$ and $CKP_{mn} = 0$, or $DAP_{mn} = 1$ and $CKP_{mn} = 1$. The delay time to SOp output becomes “from $\overline{SCKp}\uparrow$ ” when $DAP_{mn} = 0$ and $CKP_{mn} = 1$, or $DAP_{mn} = 1$ and $CKP_{mn} = 0$.

Caution Select the TTL input buffer for the Slp pin and \overline{SCKp} pin and the N-ch open drain output (EV_{DD0} tolerance) mode for the SOp pin by using port input mode register g (PIMg) and port output mode register g (POMg).

Remark 1. $R_b[\Omega]$: Communication line (SOp) pull-up resistance, $C_b[F]$: Communication line (SOp) load capacitance, $V_b[V]$: Communication line voltage

Remark 2. p: CSI number (p = 00, 01, 10, 20, 30, 31), m: Unit number (m = 0, 1), n: Channel number (n = 0 to 3), g: PIM and POM number (g = 0, 1, 3 to 5, 14)

Remark 3. f_{MCK} : Serial array unit operation clock frequency
(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn).
m: Unit number, n: Channel number (mn = 00, 02, 10))

Remark 4. V_{IH} and V_{IL} below are observation points for the AC characteristics of the serial array unit when communicating at different potentials in CSI mode.

$4.0\text{ V} \leq EV_{DD0} \leq 5.5\text{ V}$, $2.7\text{ V} \leq V_b \leq 4.0\text{ V}$: $V_{IH} = 2.2\text{ V}$, $V_{IL} = 0.8\text{ V}$

$2.7\text{ V} \leq EV_{DD0} < 4.0\text{ V}$, $2.3\text{ V} \leq V_b \leq 2.7\text{ V}$: $V_{IH} = 2.0\text{ V}$, $V_{IL} = 0.5\text{ V}$

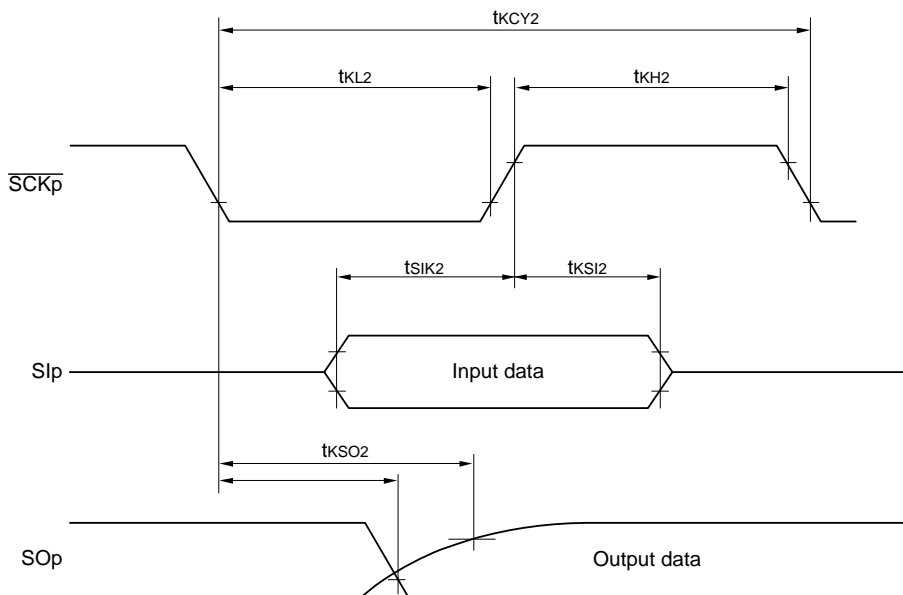
$1.8\text{ V} \leq EV_{DD0} < 3.3\text{ V}$, $1.6\text{ V} \leq V_b \leq 2.0\text{ V}$: $V_{IH} = 1.50\text{ V}$, $V_{IL} = 0.32\text{ V}$

Remark 5. CSI01 of 48-, 52-, 64-pin products, and CSI11 and CSI21 cannot communicate at different potential. Use other CSI for communication at different potential.

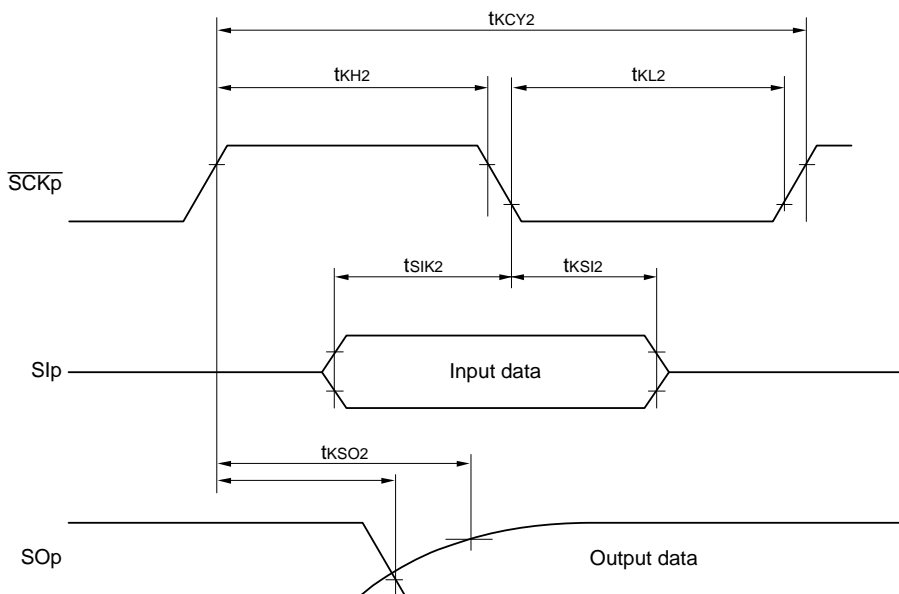
Also, communication at different potential cannot be performed during clock synchronous serial communication with the slave select function.

Caution The pins mounted depend on the product. Refer to 1.3.1 30-pin products to 1.3.10 100-pin products.

**CSI mode serial transfer timing (slave mode) (during communication at different potential)
(When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1.)**



**CSI mode serial transfer timing (slave mode) (during communication at different potential)
(When DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.)**



Caution Select the TTL input buffer for the SIp pin and SCKp pin and the N-ch open drain output (EVDDo tolerance) mode for the SOp pin by using port input mode register g (PIMg) and port output mode register g (POMg).

Remark 1. p: CSI number (p = 00, 01, 10, 20, 30, 31), m: Unit number (m = 0, 1), n: Channel number (n = 0 to 3), g: PIM and POM number (g = 0, 1, 3 to 5, 14)

Remark 2. CSI01 of 48-, 52-, 64-pin products, and CSI11 and CSI21 cannot communicate at different potential. Use other CSI for communication at different potential.

Also, communication at different potential cannot be performed during clock synchronous serial communication with the slave select function.

Caution The pins mounted depend on the product. Refer to 1.3.1 30-pin products to 1.3.10 100-pin products.

(10) Communication at different potential (2.5 V, 3 V) (simplified I²C mode)

(TA = -40 to +85 °C, 1.8 V ≤ EVDD0 = EVDD1 ≤ VDD ≤ 5.5 V, VSS = EVSS0 = EVSS1 = 0 V)

(1/2)

Parameter	Symbol	Conditions	MIN.	MAX.	Unit
SCLr clock frequency	f _{SCL}	4.0 V ≤ EVDD0 ≤ 5.5 V, 2.7 V ≤ Vb ≤ 4.0 V, Cb = 50 pF, Rb = 2.7 kΩ		1000	kHz
		2.7 V ≤ EVDD0 < 4.0 V, 2.3 V ≤ Vb < 2.7 V, Cb = 50 pF, Rb = 2.7 kΩ		1000	kHz
		4.0 V ≤ EVDD0 ≤ 5.5 V, 2.7 V ≤ Vb ≤ 4.0 V, Cb = 100 pF, Rb = 2.8 kΩ		400	kHz
		2.7 V ≤ EVDD0 < 4.0 V, 2.3 V ≤ Vb < 2.7 V, Cb = 100 pF, Rb = 2.7 kΩ		400	kHz
		1.8 V ≤ EVDD0 < 3.3 V, 1.6 V ≤ Vb ≤ 2.0 V Note 1, Cb = 100 pF, Rb = 5.5 kΩ		300	kHz
Hold time when SCLr = "L"	t _{LOW}	4.0 V ≤ EVDD0 ≤ 5.5 V, 2.7 V ≤ Vb ≤ 4.0 V, Cb = 50 pF, Rb = 2.7 kΩ	475		ns
		2.7 V ≤ EVDD0 < 4.0 V, 2.3 V ≤ Vb < 2.7 V, Cb = 50 pF, Rb = 2.7 kΩ	475		ns
		4.0 V ≤ EVDD0 ≤ 5.5 V, 2.7 V ≤ Vb ≤ 4.0 V, Cb = 100 pF, Rb = 2.8 kΩ	1150		ns
		2.7 V ≤ EVDD0 < 4.0 V, 2.3 V ≤ Vb < 2.7 V, Cb = 100 pF, Rb = 2.7 kΩ	1150		ns
		1.8 V ≤ EVDD0 < 3.3 V, 1.6 V ≤ Vb ≤ 2.0 V Note 1, Cb = 100 pF, Rb = 5.5 kΩ	1550		ns
Hold time when SCLr = "H"	t _{HIGH}	4.0 V ≤ EVDD0 ≤ 5.5 V, 2.7 V ≤ Vb ≤ 4.0 V, Cb = 50 pF, Rb = 2.7 kΩ	245		ns
		2.7 V ≤ EVDD0 < 4.0 V, 2.3 V ≤ Vb < 2.7 V, Cb = 50 pF, Rb = 2.7 kΩ	200		ns
		4.0 V ≤ EVDD0 ≤ 5.5 V, 2.7 V ≤ Vb ≤ 4.0 V, Cb = 100 pF, Rb = 2.8 kΩ	675		ns
		2.7 V ≤ EVDD0 < 4.0 V, 2.3 V ≤ Vb < 2.7 V, Cb = 100 pF, Rb = 2.7 kΩ	600		ns
		1.8 V ≤ EVDD0 < 3.3 V, 1.6 V ≤ Vb ≤ 2.0 V Note 1, Cb = 100 pF, Rb = 5.5 kΩ	610		ns

(Notes, Caution and Remarks are listed on the next page.)

Caution The pins mounted depend on the product. Refer to 1.3.1 30-pin products to 1.3.10 100-pin products.

(10) Communication at different potential (2.5 V, 3 V) (simplified I²C mode)

(TA = -40 to +85 °C, 1.8 V ≤ EV_{DD0} = EV_{DD1} ≤ V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS0} = EV_{SS1} = 0 V)

(2/2)

Parameter	Symbol	Conditions	MIN.	MAX.	Unit
Data setup time (reception)	tsu:DAT	4.0 V ≤ EV _{DD0} ≤ 5.5 V, 2.7 V ≤ V _b ≤ 4.0 V, C _b = 50 pF, R _b = 2.7 kΩ	1/f _{MCK} + 135 Note 2		ns
		2.7 V ≤ EV _{DD0} < 4.0 V, 2.3 V ≤ V _b < 2.7 V, C _b = 50 pF, R _b = 2.7 kΩ	1/f _{MCK} + 135 Note 2		ns
		4.0 V ≤ EV _{DD0} ≤ 5.5 V, 2.7 V ≤ V _b ≤ 4.0 V, C _b = 100 pF, R _b = 2.8 kΩ	1/f _{MCK} + 190 Note 2		ns
		2.7 V ≤ EV _{DD0} < 4.0 V, 2.3 V ≤ V _b < 2.7 V, C _b = 100 pF, R _b = 2.7 kΩ	1/f _{MCK} + 190 Note 2		ns
		1.8 V ≤ EV _{DD0} < 3.3 V, 1.6 V ≤ V _b ≤ 2.0 V Note 1, C _b = 100 pF, R _b = 5.5 kΩ	1/f _{MCK} + 190 Note 2		ns
Data hold time (transmission)	thd:DAT	4.0 V ≤ EV _{DD0} ≤ 5.5 V, 2.7 V ≤ V _b ≤ 4.0 V, C _b = 50 pF, R _b = 2.7 kΩ	0	305	ns
		2.7 V ≤ EV _{DD0} < 4.0 V, 2.3 V ≤ V _b < 2.7 V, C _b = 50 pF, R _b = 2.7 kΩ	0	305	ns
		4.0 V ≤ EV _{DD0} ≤ 5.5 V, 2.7 V ≤ V _b ≤ 4.0 V, C _b = 100 pF, R _b = 2.8 kΩ	0	355	ns
		2.7 V ≤ EV _{DD0} < 4.0 V, 2.3 V ≤ V _b < 2.7 V, C _b = 100 pF, R _b = 2.7 kΩ	0	355	ns
		1.8 V ≤ EV _{DD0} < 3.3 V, 1.6 V ≤ V _b ≤ 2.0 V Note 1, C _b = 100 pF, R _b = 5.5 kΩ	0	405	ns

Note 1. Use it with EV_{DD0} ≥ V_b.

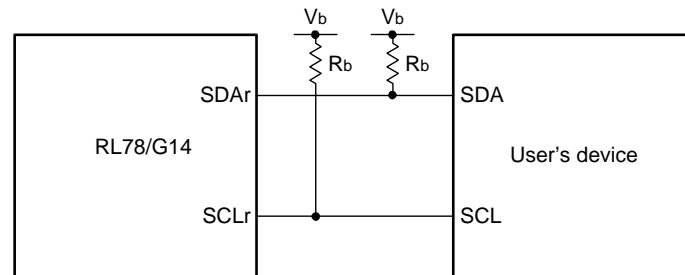
Note 2. Set the f_{MCK} value to keep the hold time of SCLr = "L" and SCLr = "H".

Caution Select the TTL input buffer and the N-ch open drain output (EV_{DD0} tolerance) mode for the SDAr pin and the N-ch open drain output (EV_{DD0} tolerance) mode for the SCLr pin by using port input mode register g (PIMg) and port output mode register g (POMg).

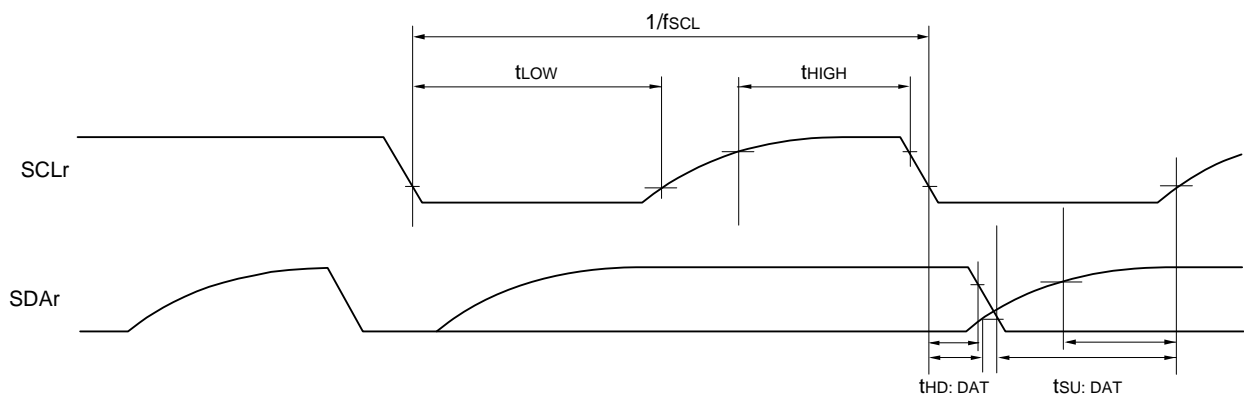
(Remarks are listed on the next page.)

Caution The pins mounted depend on the product. Refer to 1.3.1 30-pin products to 1.3.10 100-pin products.

Simplified I²C mode connection diagram (during communication at different potential)



Simplified I²C mode serial transfer timing (during communication at different potential)



Caution Select the TTL input buffer and the N-ch open drain output (EV_{DD0} tolerance) mode for the SDAr pin and the N-ch open drain output (EV_{DD0} tolerance) mode for the SCLr pin by using port input mode register g (PIMg) and port output mode register g (POMg).

Remark 1. $R_b[\Omega]$: Communication line (SDAr, SCLr) pull-up resistance, $C_b[F]$: Communication line (SDAr, SCLr) load capacitance, $V_b[V]$: Communication line voltage

Remark 2. r: IIC number (r = 00, 01, 10, 11, 20, 30, 31), g: PIM, POM number (g = 0, 1, 3 to 5, 14)

Remark 3. f_{MCK} : Serial array unit operation clock frequency
(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number (m = 0, 1), n: Channel number (n = 0, 3), mn = 00 to 03, 10, 12, 13)

Remark 4. V_{IH} and V_{IL} below are observation points for the AC characteristics of the serial array unit when communicating at different potentials in simplified I²C mode.

$4.0\text{ V} \leq EV_{DD0} \leq 5.5\text{ V}$, $2.7\text{ V} \leq V_b \leq 4.0\text{ V}$: $V_{IH} = 2.2\text{ V}$, $V_{IL} = 0.8\text{ V}$

$2.7\text{ V} \leq EV_{DD0} < 4.0\text{ V}$, $2.3\text{ V} \leq V_b \leq 2.7\text{ V}$: $V_{IH} = 2.0\text{ V}$, $V_{IL} = 0.5\text{ V}$

$1.8\text{ V} \leq EV_{DD0} < 3.3\text{ V}$, $1.6\text{ V} \leq V_b \leq 2.0\text{ V}$: $V_{IH} = 1.50\text{ V}$, $V_{IL} = 0.32\text{ V}$

Caution The pins mounted depend on the product. Refer to 1.3.1 30-pin products to 1.3.10 100-pin products.

2.5.2 Serial interface IICA

($T_A = -40$ to $+85$ °C, $1.6\text{ V} \leq EV_{DD0} = EV_{DD1} \leq V_{DD} \leq 5.5\text{ V}$, $V_{SS} = EV_{SS0} = EV_{SS1} = 0\text{ V}$)

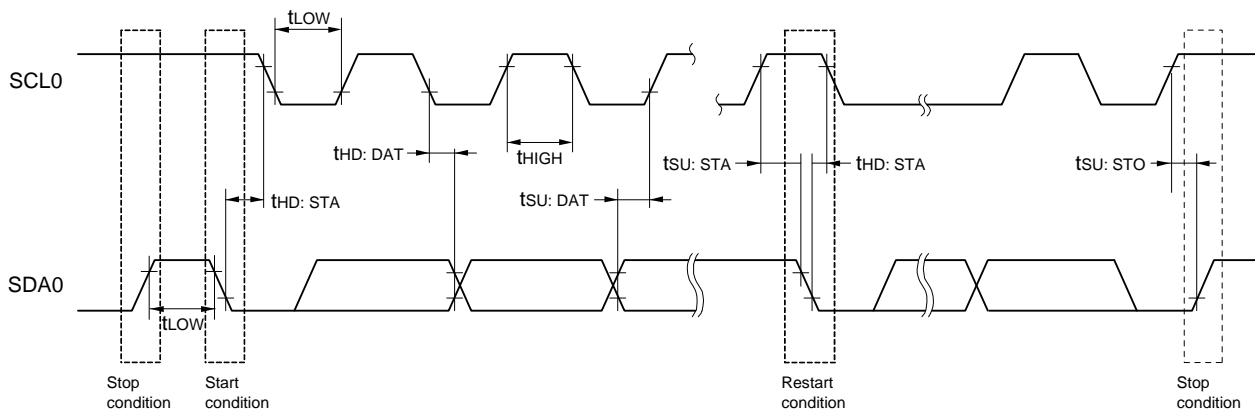
Parameter	Symbol	Conditions	Standard Mode		Fast Mode		Fast Mode Plus		Unit
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
SCLA0 clock frequency	f _{SCL}	Fast mode plus: f _{CLK} ≥ 10 MHz	2.7 V ≤ EV _{DD0} ≤ 5.5 V				0	1000	kHz
		Fast mode: f _{CLK} ≥ 3.5 MHz	1.8 V ≤ EV _{DD0} ≤ 5.5 V				0	400	kHz
		Normal mode: f _{CLK} ≥ 1 MHz	1.6 V ≤ EV _{DD0} ≤ 5.5 V		0	100			kHz
Setup time of restart condition <small>Note 1</small>	t _{SU:STA}		4.7		0.6		0.26		μs
Hold time	t _{HD:STA}		4.0		0.6		0.26		μs
Hold time when SCLA0 = "L"	t _{LOW}		4.7		1.3		0.5		μs
Hold time when SCLA0 = "H"	t _{HIGH}		4.0		0.6		0.26		μs
Data setup time (reception)	t _{SU:DAT}		250		100		50		ns
Data hold time (transmission) <small>Note 2</small>	t _{HD:DAT}		0	3.45	0	0.9	0		μs
Setup time of stop condition	t _{SU:STO}		4.0		0.6		0.26		μs
Bus-free time	t _{BUF}		4.7		1.3		0.5		μs

Note 1. The first clock pulse is generated after this period when the start/restart condition is detected.

Note 2. The maximum value (MAX.) of t_{HD:DAT} is during normal transfer and a wait state is inserted in the \overline{ACK} (acknowledge) timing.

Remark The maximum value of C_b (communication line capacitance) and the value of R_b (communication line pull-up resistor) at that time in each mode are as follows.
 Standard mode: C_b = 400 pF, R_b = 2.7 kΩ
 Fast mode: C_b = 320 pF, R_b = 1.1 kΩ
 Fast mode plus: C_b = 120 pF, R_b = 1.1 kΩ

IICA serial transfer timing



Caution The pins mounted depend on the product. Refer to 1.3.1 30-pin products to 1.3.10 100-pin products.

2.5.3 On-chip debug (UART)

($T_A = -40$ to $+85$ °C, $1.8\text{ V} \leq EV_{DD0} = EV_{DD1} \leq V_{DD} \leq 5.5\text{ V}$, $V_{SS} = EV_{SS0} = EV_{SS1} = 0\text{ V}$)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Transfer rate			115.2 k		1 M	bps

2.6 Analog Characteristics

2.6.1 A/D converter characteristics

(1) When $AV_{REF}(+) = AV_{REFP}/ANI0$ ($ADREFP1 = 0$, $ADREFP0 = 1$), $AV_{REF}(-) = AV_{REFM}/ANI1$ ($ADREFM = 1$), target ANI pin: ANI2 to ANI14 (supply ANI pin to V_{DD})

($T_A = -40$ to $+85$ °C, $1.6\text{ V} \leq EV_{DD0} = EV_{DD1} \leq V_{DD} \leq 5.5\text{ V}$, $V_{SS} = EV_{SS0} = EV_{SS1} = 0\text{ V}$, Reference voltage (+) = AV_{REFP} , Reference voltage (-) = $AV_{REFM} = 0\text{ V}$)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit	
Resolution	RES		8		10	bit	
Overall error Notes 1, 2	AINL	10-bit resolution $AV_{REFP} = V_{DD}$	$1.8\text{ V} \leq V_{DD} \leq 5.5\text{ V}$		1.2	± 3.5	LSB
			$1.6\text{ V} \leq V_{DD} \leq 5.5\text{ V}$		1.2	± 7.0	LSB
Conversion time	tCONV	10-bit resolution $AV_{REFP} = V_{DD}$	$3.6\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	2.125		39	μs
			$2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	3.1875		39	μs
			$1.8\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	17		39	μs
			$1.6\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	57		95	μs
Zero-scale error Notes 1, 2	EZS	10-bit resolution $AV_{REFP} = V_{DD}$	$1.8\text{ V} \leq V_{DD} \leq 5.5\text{ V}$			± 0.25	% FSR
			$1.6\text{ V} \leq V_{DD} < 5.5\text{ V}$			± 0.50	% FSR
Full-scale error Notes 1, 2	EFS	10-bit resolution $AV_{REFP} = V_{DD}$	$1.8\text{ V} \leq V_{DD} \leq 5.5\text{ V}$			± 0.25	% FSR
			$1.6\text{ V} \leq V_{DD} \leq 5.5\text{ V}$			± 0.50	% FSR
Integral linearity error Note 1	ILE	10-bit resolution $AV_{REFP} = V_{DD}$	$1.8\text{ V} \leq V_{DD} \leq 5.5\text{ V}$			± 2.5	LSB
			$1.6\text{ V} \leq V_{DD} \leq 5.5\text{ V}$			± 5.0	LSB
Differential linearity error Note 1	DLE	10-bit resolution $AV_{REFP} = V_{DD}$	$1.8\text{ V} \leq V_{DD} \leq 5.5\text{ V}$			± 1.5	LSB
			$1.6\text{ V} \leq V_{DD} \leq 5.5\text{ V}$			± 2.0	LSB
Reference voltage (+)	AV_{REFP}		1.6		V_{DD}	V	
Analog input voltage	V_{AIN}		0		AV_{REFP}	V	
	V_{BGR}	$2.4\text{ V} \leq V_{DD} < 5.5\text{ V}$, HS (high-speed main) mode	1.38	1.45	1.5	V	

Note 1. Excludes quantization error ($\pm 1/2$ LSB).

Note 2. This value is indicated as a ratio (% FSR) to the full-scale value.

Caution The pins mounted depend on the product. Refer to 1.3.1 30-pin products to 1.3.10 100-pin products.

(2) When $AV_{REF} (+) = AV_{REFP}/ANI0$ ($ADREFP1 = 0, ADREFP0 = 1$), $AV_{REF} (-) = AV_{REFM}/ANI1$ ($ADREFM = 1$), target ANI pin: ANI16 to ANI20 (supply ANI pin to EV_{DD0})

($T_A = -40$ to $+85$ °C, $1.6\text{ V} \leq EV_{DD0} = EV_{DD1} \leq V_{DD} \leq 5.5\text{ V}$, $V_{SS} = EV_{SS0} = EV_{SS1} = 0\text{ V}$, Reference voltage (+) = AV_{REFP} , Reference voltage (-) = $AV_{REFM} = 0\text{ V}$)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Resolution	RES			8		10	bit
Overall error Notes 1, 2	AINL	10-bit resolution $AV_{REFP} = V_{DD}$	$1.8\text{ V} \leq V_{DD} \leq 5.5\text{ V}$		1.2	± 5.0	LSB
			$1.6\text{ V} \leq V_{DD} \leq 5.5\text{ V}$		1.2	± 8.5	LSB
Conversion time	tCONV	10-bit resolution $AV_{REFP} = V_{DD}$	$3.6\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	2.125		39	μs
			$2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	3.1875		39	μs
			$1.8\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	17		39	μs
			$1.6\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	57		95	μs
Zero-scale error Notes 1, 2	EZS	10-bit resolution $AV_{REFP} = V_{DD}$	$1.8\text{ V} \leq V_{DD} \leq 5.5\text{ V}$			± 0.35	% FSR
			$1.6\text{ V} \leq V_{DD} \leq 5.5\text{ V}$			± 0.60	% FSR
Full-scale error Notes 1, 2	EFS	10-bit resolution $AV_{REFP} = V_{DD}$	$1.8\text{ V} \leq V_{DD} \leq 5.5\text{ V}$			± 0.35	% FSR
			$1.6\text{ V} \leq V_{DD} \leq 5.5\text{ V}$			± 0.60	% FSR
Integral linearity error Note 1	ILE	10-bit resolution $AV_{REFP} = V_{DD}$	$1.8\text{ V} \leq V_{DD} \leq 5.5\text{ V}$			± 3.5	LSB
			$1.6\text{ V} \leq V_{DD} \leq 5.5\text{ V}$			± 6.0	LSB
Differential linearity error Note 1	DLE	10-bit resolution $AV_{REFP} = V_{DD}$	$1.8\text{ V} \leq V_{DD} \leq 5.5\text{ V}$			± 2.0	LSB
			$1.6\text{ V} \leq V_{DD} \leq 5.5\text{ V}$			± 2.5	LSB
Reference voltage (+)	AV_{REFP}			1.6		V_{DD}	V
Analog input voltage	V_{AIN}			0		AV_{REFP} and EV_{DD0}	V
	V_{BGR}	$2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, HS (high-speed main) mode		1.38	1.45	1.5	V

Note 1. Excludes quantization error ($\pm 1/2$ LSB).

Note 2. This value is indicated as a ratio (% FSR) to the full-scale value.

Caution The pins mounted depend on the product. Refer to 1.3.1 30-pin products to 1.3.10 100-pin products.

(3) When $AV_{REF}(+) = V_{DD}$ ($ADREFP1 = 0$, $ADREFP0 = 0$), $AV_{REF}(-) = V_{SS}$ ($ADREFM = 0$), target ANI pin: ANI0 to ANI14, ANI16 to ANI20

($T_A = -40$ to $+85$ °C, $1.6\text{ V} \leq EV_{DD0} = EV_{DD1} \leq V_{DD} \leq 5.5\text{ V}$, $V_{SS} = EV_{SS0} = EV_{SS1} = 0\text{ V}$, Reference voltage (+) = V_{DD} , Reference voltage (-) = V_{SS})

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Resolution	RES			8		10	bit
Overall error Notes 1, 2	AINL	10-bit resolution	$1.8\text{ V} \leq V_{DD} \leq 5.5\text{ V}$		1.2	± 7.0	LSB
			$1.6\text{ V} \leq V_{DD} \leq 5.5\text{ V}$		1.2	± 10.5	LSB
Conversion time	tCONV	10-bit resolution	$3.6\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	2.125		39	μs
			$2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	3.1875		39	μs
			$1.8\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	17		39	μs
			$1.6\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	57		95	μs
Zero-scale error Notes 1, 2	EZS	10-bit resolution	$1.8\text{ V} \leq V_{DD} \leq 5.5\text{ V}$			± 0.60	% FSR
			$1.6\text{ V} \leq V_{DD} \leq 5.5\text{ V}$			± 0.85	% FSR
Full-scale error Notes 1, 2	EFS	10-bit resolution	$1.8\text{ V} \leq V_{DD} \leq 5.5\text{ V}$			± 0.60	% FSR
			$1.6\text{ V} \leq V_{DD} \leq 5.5\text{ V}$			± 0.85	% FSR
Integral linearity error Note 1	ILE	10-bit resolution	$1.8\text{ V} \leq V_{DD} \leq 5.5\text{ V}$			± 4.0	LSB
			$1.6\text{ V} \leq V_{DD} \leq 5.5\text{ V}$			± 6.5	LSB
Differential linearity error Note 1	DLE	10-bit resolution	$1.8\text{ V} \leq V_{DD} \leq 5.5\text{ V}$			± 2.0	LSB
			$1.6\text{ V} \leq V_{DD} \leq 5.5\text{ V}$			± 2.5	LSB
Analog input voltage	VAIN	ANI0 to ANI14		0		V_{DD}	V
		ANI16 to ANI20		0		EV_{DD0}	V
	VBGR	$2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, HS (high-speed main) mode		1.38	1.45	1.5	V

Note 1. Excludes quantization error ($\pm 1/2$ LSB).

Note 2. This value is indicated as a ratio (% FSR) to the full-scale value.

Caution The pins mounted depend on the product. Refer to 1.3.1 30-pin products to 1.3.10 100-pin products.

(4) When $AV_{REF} (+)$ = Internal reference voltage ($ADREFP1 = 1$, $ADREFP0 = 0$), $AV_{REF} (-)$ = $AV_{REFM}/ANI1$ ($ADREFM = 1$), target ANI pin: ANI0 to ANI14, ANI16 to ANI20

($T_A = -40$ to $+85$ °C, $2.4\text{ V} \leq EV_{DD0} = EV_{DD1} \leq V_{DD} \leq 5.5\text{ V}$, $V_{SS} = EV_{SS0} = EV_{SS1} = 0\text{ V}$, Reference voltage (+) = V_{BGR} , Reference voltage (-) = $AV_{REFM} = 0\text{ V}$, HS (high-speed main) mode)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Resolution	RES			8			bit
Conversion time	t _{CONV}	8-bit resolution	$2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	17		39	μs
Zero-scale error Notes 1, 2	EZS	8-bit resolution	$2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$			±0.60	% FSR
Integral linearity error Note 1	ILE	8-bit resolution	$2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$			±2.0	LSB
Differential linearity error Note 1	DLE	8-bit resolution	$2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$			±1.0	LSB
Reference voltage (+)	V_{BGR}			1.38	1.45	1.5	V
Reference voltage (-)	AV_{REFM}			V_{SS}			V
Analog input voltage	V_{AIN}			0		V_{BGR}	V

Note 1. Excludes quantization error ($\pm 1/2$ LSB).

Note 2. This value is indicated as a ratio (% FSR) to the full-scale value.

Caution The pins mounted depend on the product. Refer to 1.3.1 30-pin products to 1.3.10 100-pin products.

2.6.2 Temperature sensor characteristics

($T_A = -40$ to $+85$ °C, $2.4\text{ V} \leq EV_{DD0} = EV_{DD1} \leq V_{DD} \leq 5.5\text{ V}$, $V_{SS} = EV_{SS0} = EV_{SS1} = 0\text{ V}$, HS (high-speed main) mode)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Temperature sensor output voltage	VTMPS25	Setting ADS register = 80H, $T_A = +25$ °C		1.05		V
Reference output voltage	VCONST	Setting ADS register = 81H	1.38	1.45	1.5	V
Temperature coefficient	FVTMPS	Temperature sensor that depends on the temperature		-3.6		mV/C
Operation stabilization wait time	tAMP				5	μs

2.6.3 D/A converter characteristics

($T_A = -40$ to $+85$ °C, $1.6\text{ V} \leq EV_{DD0} = EV_{DD1} \leq V_{DD} \leq 5.5\text{ V}$, $V_{SS} = EV_{SS0} = EV_{SS1} = 0\text{ V}$)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Resolution	RES					8	bit
Overall error	AINL	Rload = 4 MΩ	$1.8\text{ V} \leq V_{DD} \leq 5.5\text{ V}$			±2.5	LSB
		Rload = 8 MΩ	$1.8\text{ V} \leq V_{DD} \leq 5.5\text{ V}$			±2.5	LSB
Settling time	tSET	Cload = 20 pF	$2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}$			3	μs
			$1.6\text{ V} \leq V_{DD} < 2.7\text{ V}$			6	μs

2.6.4 Comparator

($T_A = -40$ to $+85$ °C, $1.6\text{ V} \leq EV_{DD0} = EV_{DD1} \leq V_{DD} \leq 5.5\text{ V}$, $V_{SS} = EV_{SS0} = EV_{SS1} = 0\text{ V}$)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Input voltage range	lvref			0		$EV_{DD0} - 1.4$	V
	lvcmp			-0.3		$EV_{DD0} + 0.3$	V
Output delay	td	$V_{DD} = 3.0\text{ V}$ Input slew rate $> 50\text{ mV}/\mu\text{s}$	High-speed comparator mode, standard mode			1.2	μs
			High-speed comparator mode, window mode			2.0	μs
			Low-speed comparator mode, standard mode		3		μs
High-electric-potential judgment voltage	VTW+	High-speed comparator mode, window mode			$0.76 V_{DD}$		V
Low-electric-potential judgment voltage	VTW-	High-speed comparator mode, window mode			$0.24 V_{DD}$		V

2.6.5 POR circuit characteristics

($T_A = -40$ to $+85$ °C, $V_{SS} = 0\text{ V}$)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Detection voltage	V_{POR}	Power supply rise time		1.51	1.54	V
	V_{PDR}	Power supply fall time		1.50	1.53	V
Minimum pulse width	TPW		300			μs
Detection delay time					350	μs

Caution The pins mounted depend on the product. Refer to 1.3.1 30-pin products to 1.3.10 100-pin products.

2.6.6 LVD circuit characteristics

($T_A = -40$ to $+85$ °C, $V_{PDR} \leq EV_{DD0} = EV_{DD1} \leq V_{DD} \leq 5.5$ V, $V_{SS} = EV_{SS0} = EV_{SS1} = 0$ V)

Parameter		Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Detection voltage	Supply voltage level	VLVI0	Power supply rise time	3.98	4.06	4.14	V
			Power supply fall time	3.90	3.98	4.06	V
		VLVI1	Power supply rise time	3.68	3.75	3.82	V
			Power supply fall time	3.60	3.67	3.74	V
		VLVI2	Power supply rise time	3.07	3.13	3.19	V
			Power supply fall time	3.00	3.06	3.12	V
		VLVI3	Power supply rise time	2.96	3.02	3.08	V
			Power supply fall time	2.90	2.96	3.02	V
		VLVI4	Power supply rise time	2.86	2.92	2.97	V
			Power supply fall time	2.80	2.86	2.91	V
		VLVI5	Power supply rise time	2.76	2.81	2.87	V
			Power supply fall time	2.70	2.75	2.81	V
		VLVI6	Power supply rise time	2.66	2.71	2.76	V
			Power supply fall time	2.60	2.65	2.70	V
		VLVI7	Power supply rise time	2.56	2.61	2.66	V
			Power supply fall time	2.50	2.55	2.60	V
		VLVI8	Power supply rise time	2.45	2.50	2.55	V
			Power supply fall time	2.40	2.45	2.50	V
		VLVI9	Power supply rise time	2.05	2.09	2.13	V
			Power supply fall time	2.00	2.04	2.08	V
		VLVI10	Power supply rise time	1.94	1.98	2.02	V
			Power supply fall time	1.90	1.94	1.98	V
		VLVI11	Power supply rise time	1.84	1.88	1.91	V
			Power supply fall time	1.80	1.84	1.87	V
VLVI12	Power supply rise time	1.74	1.77	1.81	V		
	Power supply fall time	1.70	1.73	1.77	V		
VLVI13	Power supply rise time	1.64	1.67	1.70	V		
	Power supply fall time	1.60	1.63	1.66	V		
Minimum pulse width	tLW		300				μs
Detection delay time	tLD					300	μs

Caution Set the detection voltage (VLVI) to be within the operating voltage range. The operating voltage range depends on the setting of the user option byte (000C2H/010C2H). The following shows the operating voltage range.

HS (high-speed main) mode: $V_{DD} = 2.7$ to 5.5 V@1 MHz to 32 MHz
 $V_{DD} = 2.4$ to 5.5 V@1 MHz to 16 MHz

LS (low-speed main) mode: $V_{DD} = 1.8$ to 5.5 V@1 MHz to 8 MHz

LV (low voltage main) mode: $V_{DD} = 1.6$ to 5.5 V@1 MHz to 4 MHz

Remark $VLVI(n-1) > VLVI_n$: $n = 1$ to 13

Caution The pins mounted depend on the product. Refer to 1.3.1 30-pin products to 1.3.10 100-pin products.

LVD Detection Voltage of Interrupt & Reset Mode

($T_A = -40$ to $+85$ °C, $V_{PDR} \leq EV_{DD0} = EV_{DD1} \leq V_{DD} \leq 5.5$ V, $V_{SS} = EV_{SS0} = EV_{SS1} = 0$ V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit	
Interrupt and reset mode	VLVI13	$V_{POC0}, V_{POC1}, V_{POC2} = 0, 0, 0$, falling reset voltage: 1.6 V	1.60	1.63	1.66	V	
	VLVI12	$LVIS0, LVIS1 = 1, 0$ (+0.1 V)	Rising release reset voltage	1.74	1.77	1.81	V
			Falling interrupt voltage	1.70	1.73	1.77	V
	VLVI11	$LVIS0, LVIS1 = 0, 1$ (+0.2 V)	Rising release reset voltage	1.84	1.88	1.91	V
			Falling interrupt voltage	1.80	1.84	1.87	V
	VLVI4	$LVIS0, LVIS1 = 0, 0$ (+1.2 V)	Rising release reset voltage	2.86	2.92	2.97	V
			Falling interrupt voltage	2.80	2.86	2.91	V
	VLVI11	$V_{POC0}, V_{POC1}, V_{POC2} = 0, 0, 1$, falling reset voltage: 1.8 V	1.80	1.84	1.87	V	
	VLVI10	$LVIS0, LVIS1 = 1, 0$ (+0.1 V)	Rising release reset voltage	1.94	1.98	2.02	V
			Falling interrupt voltage	1.90	1.94	1.98	V
	VLVI9	$LVIS0, LVIS1 = 0, 1$ (+0.2 V)	Rising release reset voltage	2.05	2.09	2.13	V
			Falling interrupt voltage	2.00	2.04	2.08	V
	VLVI2	$LVIS0, LVIS1 = 0, 0$ (+1.2 V)	Rising release reset voltage	3.07	3.13	3.19	V
			Falling interrupt voltage	3.00	3.06	3.12	V
	VLVI8	$V_{POC0}, V_{POC1}, V_{POC2} = 0, 1, 0$, falling reset voltage: 2.4 V	2.40	2.45	2.50	V	
	VLVI7	$LVIS0, LVIS1 = 1, 0$ (+0.1 V)	Rising release reset voltage	2.56	2.61	2.66	V
Falling interrupt voltage			2.50	2.55	2.60	V	
VLVI6	$LVIS0, LVIS1 = 0, 1$ (+0.2 V)	Rising release reset voltage	2.66	2.71	2.76	V	
		Falling interrupt voltage	2.60	2.65	2.70	V	
VLVI1	$LVIS0, LVIS1 = 0, 0$ (+1.2 V)	Rising release reset voltage	3.68	3.75	3.82	V	
		Falling interrupt voltage	3.60	3.67	3.74	V	
VLVI5	$V_{POC0}, V_{POC1}, V_{POC2} = 0, 1, 1$, falling reset voltage: 2.7 V	2.70	2.75	2.81	V		
VLVI4	$LVIS0, LVIS1 = 1, 0$ (+0.1 V)	Rising release reset voltage	2.86	2.92	2.97	V	
		Falling interrupt voltage	2.80	2.86	2.91	V	
VLVI3	$LVIS0, LVIS1 = 0, 1$ (+0.2 V)	Rising release reset voltage	2.96	3.02	3.08	V	
		Falling interrupt voltage	2.90	2.96	3.02	V	
VLVI0	$LVIS0, LVIS1 = 0, 0$ (+1.2 V)	Rising release reset voltage	3.98	4.06	4.14	V	
		Falling interrupt voltage	3.90	3.98	4.06	V	

Caution Set the detection voltage (VLVI) to be within the operating voltage range. The operating voltage range depends on the setting of the user option byte (000C2H/010C2H). The following shows the operating voltage range.

HS (high-speed main) mode: $V_{DD} = 2.7$ to 5.5 V@1 MHz to 32 MHz

$V_{DD} = 2.4$ to 5.5 V@1 MHz to 16 MHz

LS (low-speed main) mode: $V_{DD} = 1.8$ to 5.5 V@1 MHz to 8 MHz

LV (low voltage main) mode: $V_{DD} = 1.6$ to 5.5 V@1 MHz to 4 MHz

Caution The pins mounted depend on the product. Refer to 1.3.1 30-pin products to 1.3.10 100-pin products.

2.7 Power Supply Rise Time

($T_A = -40$ to $+85$ °C, $V_{SS} = EV_{SS0} = EV_{SS1} = 0$ V)

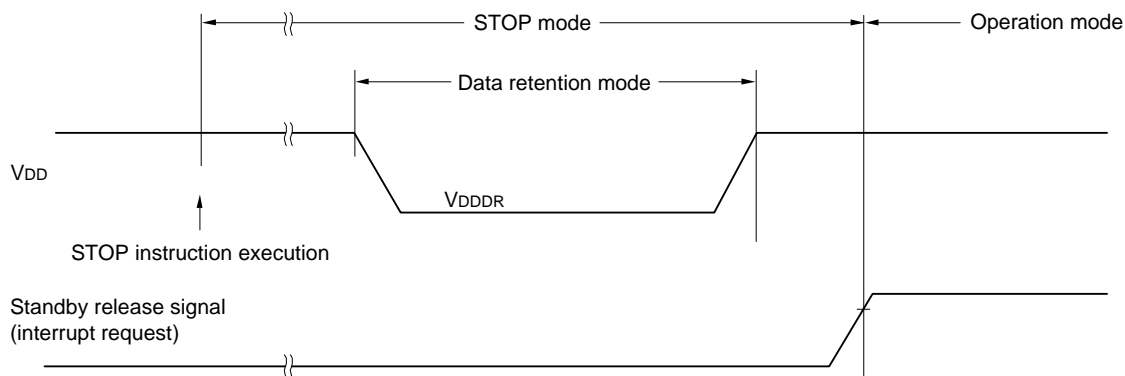
Parameter	Conditions	MIN.	TYP.	MAX.	Unit
VDD rise inclination	TPUP			53.0	V/ms

2.8 Data Memory STOP Mode Low Supply Voltage Data Retention Characteristics

($T_A = -40$ to $+85$ °C)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Data retention supply voltage	VDDDR		1.5 Note		5.5	V

Note The value depends on the POR detection voltage. When the voltage drops, the data is retained before a POR reset is effected, but data is not retained when a POR reset is effected.



2.9 Flash Memory Programming Characteristics

($T_A = -40$ to $+85$ °C, 1.8 V \leq $EV_{DD0} = EV_{DD1} \leq$ $V_{DD} \leq$ 5.5 V, $V_{SS} = EV_{SS0} = EV_{SS1} = 0$ V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
CPU/peripheral hardware clock frequency	fCLK	1.8 V \leq $V_{DD} \leq$ 5.5 V	1		32	MHz
Number of code flash rewrites	Cenwr	1 erase + 1 write after the erase is regarded as 1 rewrite. The retaining years are until next rewrite after the rewrite.	Retained for 20 years (Self/serial programming) Note	1,000		Times
Number of data flash rewrites			Retained for 1 years (Self/serial programming) Note		1,000,000	
			Retained for 5 years (Self/serial programming) Note	100,000		

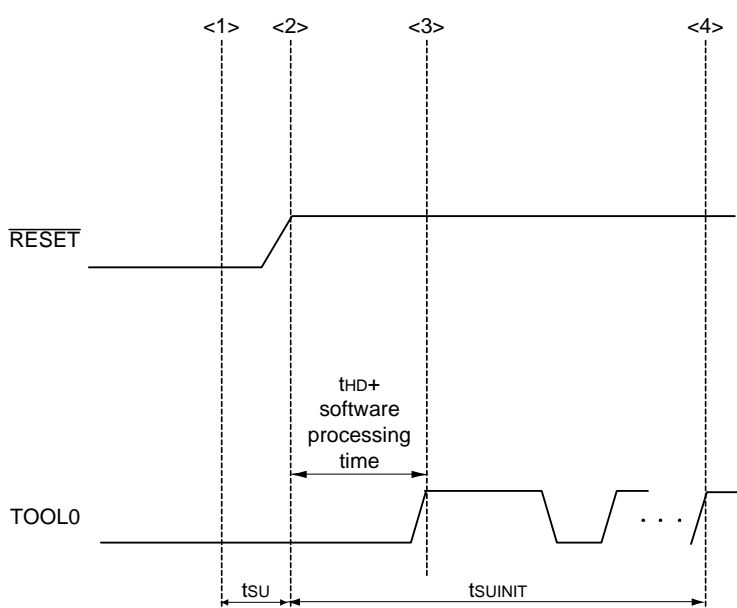
Note When using flash memory programmer and Renesas Electronics self programming library.

Remark When updating data multiple times, use the flash memory as one for updating data.

Caution The pins mounted depend on the product. Refer to 1.3.1 30-pin products to 1.3.10 100-pin products.

2.10 Timing Specs for Switching Modes

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
How long from when a pin reset ends until the initial communication settings are specified	tsUINIT	POR and LVD reset must end before the pin reset ends.			100	ms
How long from when the TOOL0 pin is placed at the low level until a pin reset ends	tsU	POR and LVD reset must end before the pin reset ends.	10			μs
How long the TOOL0 pin must be kept at the low level after a reset ends	tHD	POR and LVD reset must end before the pin reset ends.	1			ms



- <1> The low level is input to the TOOL0 pin.
- <2> The pins reset ends (POR and LVD reset must end before the pin reset ends.).
- <3> The TOOL0 pin is set to the high level.
- <4> Setting of the flash memory programming mode by UART reception and complete the baud rate setting.

Remark t_{SUINIT} : The segment shows that it is necessary to finish specifying the initial communication settings within 100 ms from when the external and internal resets end.
 t_{SU} : How long from when the TOOL0 pin is placed at the low level until a pin reset ends
 t_{HD} : How long to keep the TOOL0 pin at the low level from when the external and internal resets end

REVISION HISTORY	RL78/G14 Datasheet
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Rev.	Date	Description	
		Page	Summary
0.01	Feb 10, 2011	—	First Edition issued
0.02	May 01, 2011	1 to 2 3 4 to 13 14 15 to 17 23 to 26	1.1 Features revised 1.2 Ordering Information revised 1.3 Pin Configuration (Top View) revised 1.4 Pin Identification revised 1.5.1 30-pin products to 1.5.3 36-pin products revised 1.6 Outline of Functions revised
0.03	Jul 28, 2011	1	1.1 Features revised
1.00	Feb 21, 2012	1 to 40 41 to 97	1. OUTLINE revised 2. ELECTRICAL SPECIFICATIONS added

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NOTES FOR CMOS DEVICES

- (1) **VOLTAGE APPLICATION WAVEFORM AT INPUT PIN:** Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between VIL (MAX) and VIH (MIN) due to noise, etc., the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between VIL (MAX) and VIH (MIN).
- (2) **HANDLING OF UNUSED INPUT PINS:** Unconnected CMOS device inputs can be cause of malfunction. If an input pin is unconnected, it is possible that an internal input level may be generated due to noise, etc., causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using pull-up or pull-down circuitry. Each unused pin should be connected to VDD or GND via a resistor if there is a possibility that it will be an output pin. All handling related to unused pins must be judged separately for each device and according to related specifications governing the device.
- (3) **PRECAUTION AGAINST ESD:** A strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it when it has occurred. Environmental control must be adequate. When it is dry, a humidifier should be used. It is recommended to avoid using insulators that easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors should be grounded. The operator should be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with mounted semiconductor devices.
- (4) **STATUS BEFORE INITIALIZATION:** Power-on does not necessarily define the initial status of a MOS device. Immediately after the power source is turned ON, devices with reset functions have not yet been initialized. Hence, power-on does not guarantee output pin levels, I/O settings or contents of registers. A device is not initialized until the reset signal is received. A reset operation must be executed immediately after power-on for devices with reset functions.
- (5) **POWER ON/OFF SEQUENCE:** In the case of a device that uses different power supplies for the internal operation and external interface, as a rule, switch on the external power supply after switching on the internal power supply. When switching the power supply off, as a rule, switch off the external power supply and then the internal power supply. Use of the reverse power on/off sequences may result in the application of an overvoltage to the internal elements of the device, causing malfunction and degradation of internal elements due to the passage of an abnormal current. The correct power on/off sequence must be judged separately for each device and according to related specifications governing the device.
- (6) **INPUT OF SIGNAL DURING POWER OFF STATE :** Do not input signals or an I/O pull-up power supply while the device is not powered. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Input of signals during the power off state must be judged separately for each device and according to related specifications governing the device.

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