KTBCD430-D1

Product

Bi-stable Cholesteric Display Module
128 x 64 Dots Matrix
Build In Voltage Booster

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CONTENTS

1. Document revision history :

DOCUMENT REVISION	DATE	DESCRIPTION	PREPARED BY	APPROVED BY
01	2011.10.10	First Release.	XW Li	

2. General Description

- 128 x 64 dots, Reflective.
- Wide viewing angle.
- 4-Wire SPI interface.
- Logic voltage: 2.8V (typ.).

3. Mechanical Specifications

The mechanical detail is shown in Fig. 1 and summarized in Table 1 below.

Table 1

Parameter		Specifications	Unit
Outline dimensions		65.0W) x 43.4(H) x 3.15(D) (Exclude FPC cables and pin header)	mm
128x64 Dot Matrix	View area	61.0(W) x 31.4 (H)	mm
	TP active area	-	mm
	LCD active area	55.025(W) x 27.505(H)	mm
	Display format	128 x 64 dot matrix	dots
	Dot pitch	0.43(RGB)(W) x 0.43(H)	mm
Weight		TBD	grams

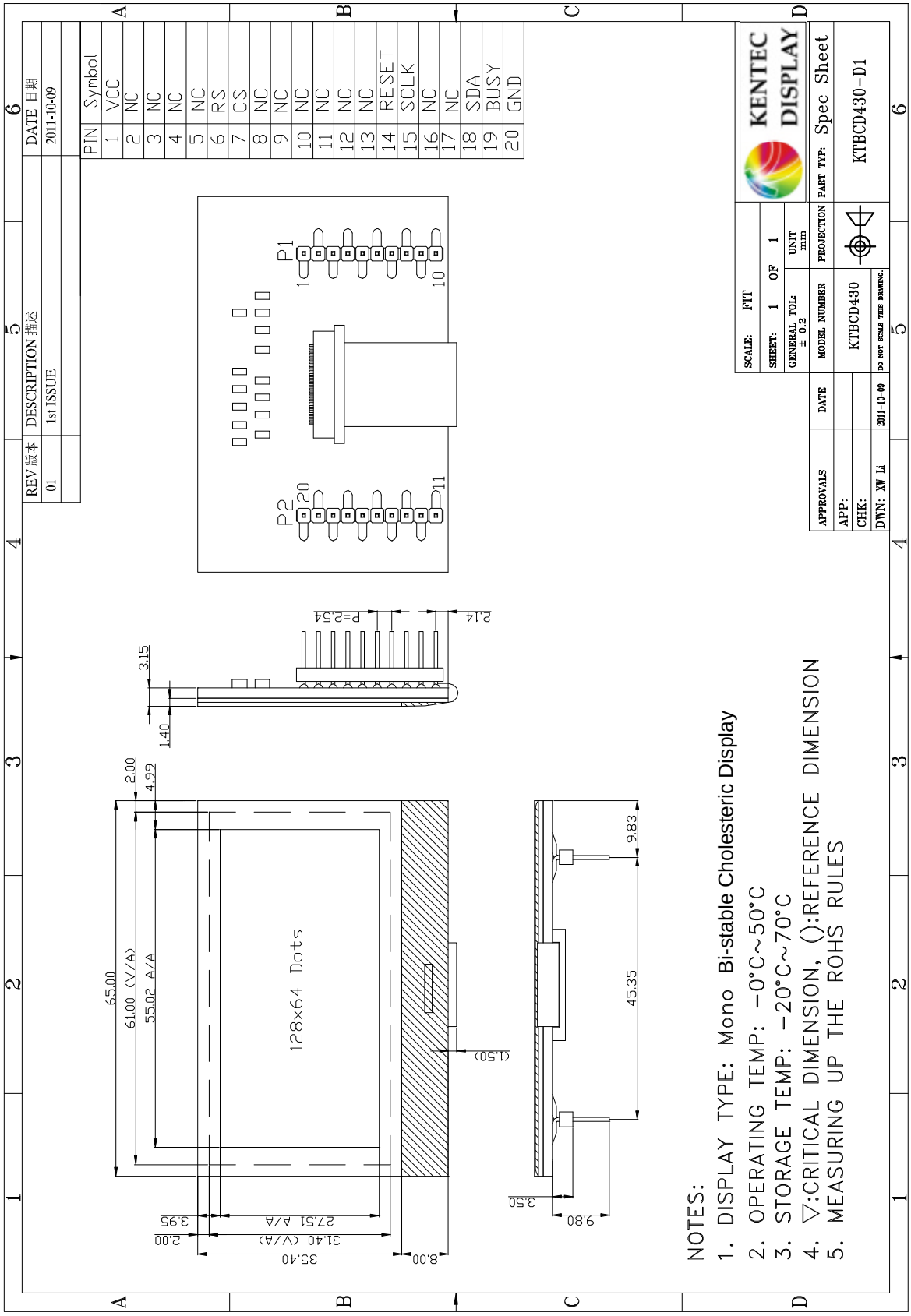


Figure 1: Outline Drawing

4. Interface signals

Table 2: Pin assignment

Pin No.	Symbol	Description
1	VCC	Power supply voltage (3.3V)
2-5	NC	No connection
6	RS	Data/Register select, set high for data input and low for register input
7	CS	Chip select, low active
8-13	NC	No connection
14	RESET	Reset signal input, low active
15	SCLK	Serial clock input
16-17	NC	No connection
18	SDA	Serial data input
19	BUSY	Chip busy signal output, output high level indicates busy status
20	GND	Ground (0V)

5. Absolute Maximum Ratings

5.1 Electrical Maximum Ratings

Table 3: Electrical Maximum Ratings – for IC

Parameter	Symbol	Min.	Max.	Unit	Note
Power supply voltage	VCC	-0.3	+3.6	V	1
Input voltage	Vin	-0.3	+3.9	V	1

Note:

1.VCC, GND must be maintained.

2.The modules may be destroyed if they are used beyond the absolute maximum ratings.

5.2 Environmental Condition

Table 4

Item	Operating temperature (Topr)		Storage temperature (Tstg) (Note 1)		Remark
	Min.	Max.	Min.	Max.	
Ambient temperature	-0°C	+50°C	-20°C	+70°C	Dry
Humidity (Note 1)	90% max. RH for Ta ≤ 40°C < 50% RH for 40°C < Ta ≤ Maximum operating temperature				No condensation

Note 1: Product cannot sustain at extreme storage conditions for long time.

6. Electrical Specifications

Typical Electrical Characteristics

At Ta = 25 °C, VCC = 3.3V, GND=0V.

Table 5

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Supply voltage	VCC-GND		3.1	3.3	3.5	V
	VLCD(Note1)		23.3	24	24.7	V
Input voltage low	VIL		**0**	-	0.2VCC	V
Input voltage high	VIH		**0.8VCC**	-	VCC	V
Supply current (Logic & LCD)	ICC	VCC=3.3V	-	2	3	mA

7. Optical Characteristics

Table 6: Optical specifications

Items		Symbol	Condition	Specifications			Unit
				Min.	Typ.	Max.	
Image refresh time		-	VCC=3.3V, VLCD=24V, @25°C	-	1.8	-	s
Contrast Ratio		CR		-	6	-	-
Viewing angle CR≧2	Hor.	ϕ1(3 o'clock)	VLCD= optimum voltage	-	80	-	deg.
		ϕ2(9 o'clock)		-	80	-	
	Ver.	θ2(12 o'clock)		-	80	-	
		θ1(6 o'clock)		-	80	-	

Note 1: Contrast Ratio

B1 = Pixel luminance at stable dark state

B2 = Pixel luminance at stable bright state

Contrast Ratio = B1/B2.

Note 2: Viewing Angle

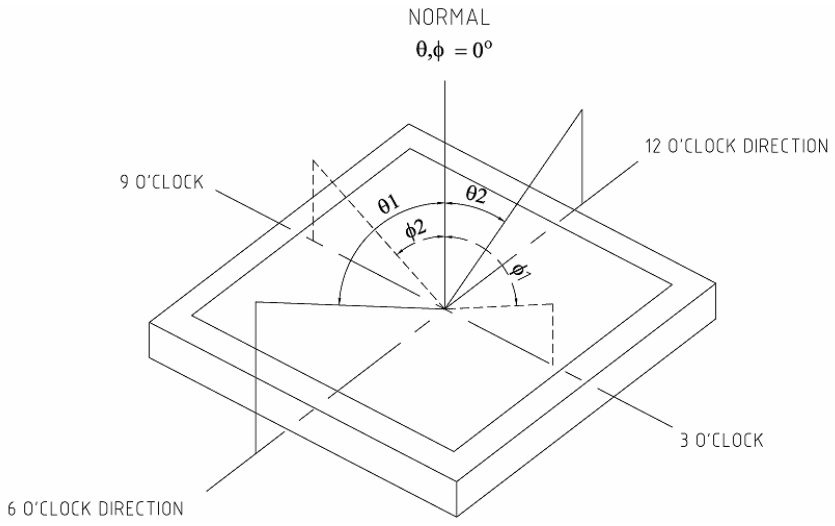


Figure 2

8. Timing Characteristics

8.1 SPI write timing

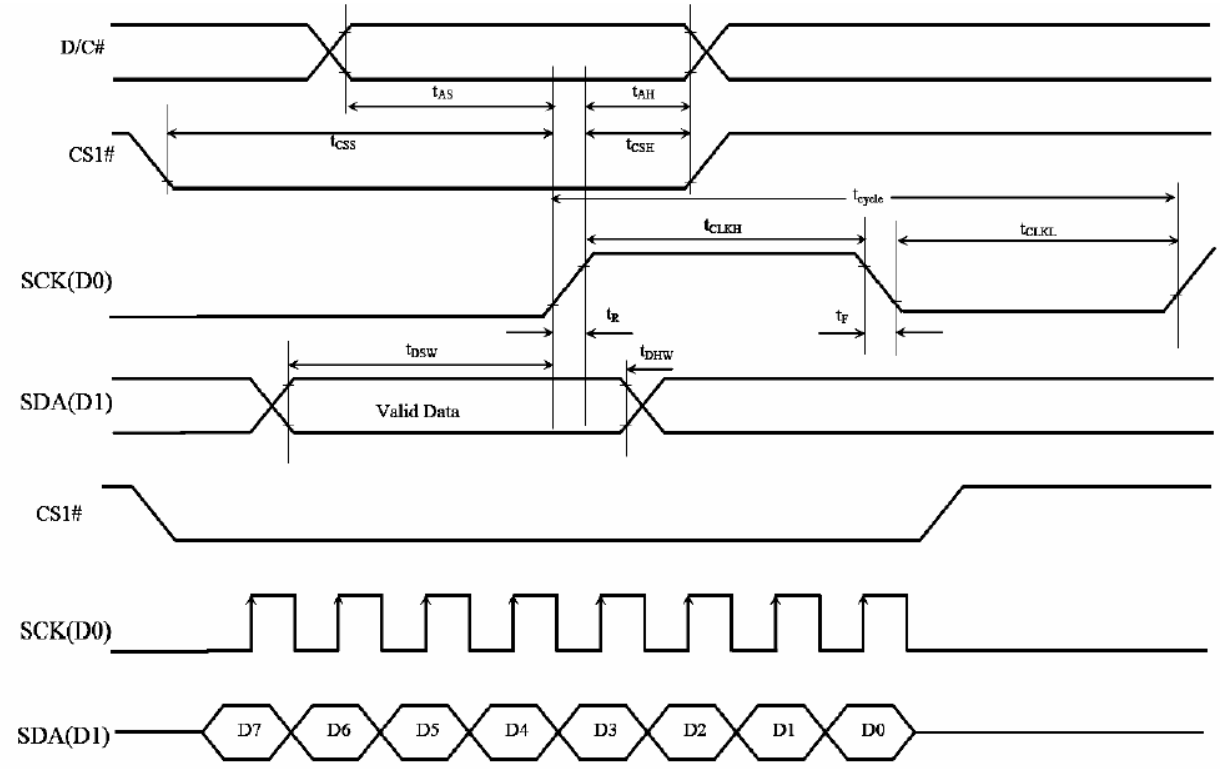


Figure 3: 4-Wire SPI write procedure

Table 7: 4-Wire SPI write timing

Symbol	Parameter	Min	Typ	Max	Unit
t_{cycle}	Clock Cycle Time	60	-	-	ns
t_{AS}	Address Setup Time	10	-	-	ns
t_{AH}	Address Hold Time	20	-	-	ns
t_{DSW}	Write Data Setup Time	30	-	-	ns
t_{DHW}	Write Data Hold Time	30	-	-	ns
T_{CLKL}	Clock Low Time	30	-	-	ns
T_{CLKH}	Clock High Time	30	-	-	ns
t_{CSS}	Chip Select Setup Time (for D7 input)	30	- -	- -	ns
t_{CSH}	Chip Select Hold Time (for D0 input)	30	- -	- -	ns
t_R	Rise Time	-	-	10	ns
t_F	Fall Time	-	-	10	ns

8.2 Command table

RS	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description
0	10-1F	0	0	0	1	A_3	A_2	A_1	A_0	Set column address	Set the higher nibble of the column address register using A3A2A1A0 as data bits. The higher nibble of column address is reset to 0000b after POR.
		0	0	0	0	B_3	B_2	B_1	B_0		Set the lower nibble of the column address register using B3B2B1B0 as data bits. The lower nibble of column address is reset to 0000b after POR.
0	2A-2F	0	0	1	0	1	X_2	1	X_0	Set Power Control Register	X2: 0: turns off the internal voltage booster (POR) 1: turns on the internal voltage booster X0: 0: turns off the Bias Voltage buffer (POR) 1: turns on the Bias Voltage buffer
0	31	0	0	1	1	0	0	0	1	Driving update	Update RAM content to the screen through segment and common pins. Driving sequence is always in: VA clearing phase ? VA Idle phase ? AA clearing phase ? AA Idle phase ? Driving phase
0	32	0	0	1	1	0	0	1	0	Driving Scheme	X6: Segment value at active clearing 1: All segment (exclude DSEG) are zero at active clear 0: All segment (exclude DSEG) are one at active clear (POR=0) X5X4: 00: SEG_D and COM_D are in Hi-Z 01: NA 10: SEG_D as data 0, COM_D scanning (POR) 11: SEG_D as data 1, COM_D scanning X3: drive polarity 0: M starts as 1 at Drive phase for Scheme A (POR) 1: M starts as 0 at Drive phase for Scheme A X2: view area and active area clearing polarity 0: M starts as 1 at Clear phase for Scheme A (POR) 1: M starts as 0 at Clear phase for Scheme A Refer to the Table 8-2 : Polarity Setting in Scheme B for Scheme B setting X1: All segment data in viewing area clear phase 0: Data = 0 (POR) 1: Data = 1 X0: Driving Scheme 0: Scheme A (POR) 1: Scheme B – Frame Inversion Display start line register is reset to 000000 after POR for all MUX modes.
0	40-4F	0	1	X_5	X_4	X_3	X_2	X_1	X_0	Set Display Start Line	Display start line register is reset to 000000 after POR for all MUX modes.

RS	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description
0	80	1	0	0	0	0	0	0	0	Set the Driving Parameter Table	Set the table data by sending the command 0x80 and then 8 byte data. A[6:0] : 0X00 B[4:0] : View Area Clearing Duration C[4:0] : View Area Idle Duration D[4:0] : Active Area Clearing Duration E[4:0] : Active Area Idle Duration F[4:0] : Driving Duration G[6:0] : Clearing Voltage H[6:0] : Driving Voltage
0	A[6:0]	*	0	0	0	0	0	0	0		
0	B[4:0]	*	*	B_5	B_4	B_3	B_2	B_1	B_0		
0	C[4:0]	*	*	C_5	C_4	C_3	C_2	C_1	C_0		
0	D[4:0]	*	*	D_5	D_4	D_3	D_2	D_1	D_0		
0	E[4:0]	*	*	E_5	E_4	E_3	E_2	E_1	E_0		
0	F[4:0]	*	*	F_5	F_4	F_3	F_2	F_1	F_0		
0	G[6:0]	*	G_6	G_5	G_4	G_3	G_2	G_1	G_0		
0	H[6:0]	*	H_6	H_5	H_4	H_3	H_2	H_1	H_0		
0	93	1	0	0	1	0	0	1	1	Set VA clearing phase repeat times	Repeat times is $X_3X_2X_1X_0$ (POR=0001) *Remark: If VA clearing phase repeat time is set to 0, it is also needed to set the idle1 phase repeat time to 0.
0		0	0	0	0	X_3	X_2	X_1	X_0		
0	94	1	0	0	1	0	1	0	0	Set idle1 phase repeat times	Repeat times is $X_3X_2X_1X_0$ (POR=0001) *Remark: If Idle1 phase repeat time is set to 0, it is also needed to set the VA clearing phase repeat time to 0.
0		0	0	0	0	X_3	X_2	X_1	X_0		
0	95	1	0	0	1	0	1	0	1	Set AA clearing phase repeat times	Repeat times is $X_3X_2X_1X_0$ (POR=0001) *Remark: If AA clearing phase repeat time is set to 0, it is also needed to set the idle2 phase repeat time to 0.
0		0	0	0	0	X_3	X_2	X_1	X_0		
0	96	1	0	0	1	0	1	1	0	Set idle2 phase repeat times	Repeat times is $X_3X_2X_1X_0$ (POR=0001) *Remark: If Idle2 phase repeat time is set to 0, it is also needed to set the AA clearing phase repeat time to 0.
		0	0	0	0	X_3	X_2	X_1	X_0		
0	97	1	0	0	1	0	1	1	1	Set drive phase repeat times	Repeat times is $X_3X_2X_1X_0$ (POR=0001)
0		0	0	0	0	X_3	X_2	X_1	X_0		
0	A0-A1	1	0	1	0	0	0	0	X_0	Set Segment Re-map	X0: 0: Column address 00h is mapped to SEG0 (POR) 1: Column address 83h is mapped to SEG0
0	A2	1	0	1	0	0	0	1	0	Set LCD Bias	X2X1X0: 000: 1/9 001: 1/8, 010: 1/7, (POR) 011: 1/6, 100: 1/5, 101: 1/ 4.6, 110: 1/ 4.3, 111: 1/4
0		0	0	0	0	0	X_2	X_1	X_0		
0	A3	1	0	1	0	0	0	1	1	Set analog control	Analog Block Control X4X3 = 00: Disable X4X3 = 11: Enable X1 = 0: Standard BIAS VOLTAGE Buffer Setting X1 = 1: Extra BIAS VOLTAGE Buffer Setting
0		0	0	0	X_4	X_3	0	X_1	0		
0	A4-A5	1	0	1	0	0	1	0	X_0	Set Entire Display	X0=0: normal display (POR) X0=1: entire display on
0	A6-A7	1	0	1	0	0	1	1	X_0	Set Reverse Display	X0=0: normal display (POR) X0=1: reverse display
0	A8	1	0	1	0	1	0	0	0	Set Multiplex Ratio	To select multiplex ratio N MUX N = X6X5X4X3X2X1X0 from 2 to 64(POR)
0		0	X_6	X_5	X_4	X_3	X_2	X_1	X_0		

RS	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description
0 0	A9	1 0	0 0	1 0	0 0	1 0	0 0	0 0	1 X_0	Analog Control Auto	X0: 0: OFF (POR) 1: ON
0 0	AD	1 0	0 0	1 0	0 0	1 0	1 0	0 0	1 X_0	RAM Read/Write Direction	X0: 0: RAM read/write horizontal (POR) 1: RAM read/write vertical
0	B0-B7	1	0	1	1	0	X_2	X_1	X_0	Set Page Address	Set GDDRAM Page Address (0-7) for read/write using X2X1X0 (POR=000)
	C0 – C8	1	1	0	0	X_3	0	0	0	Set COM Output Scan Direction	X3=0: normal mode (POR) X3=1: remapped mode COM0 to COM [N-1] becomes COM [N-1] to COM0 when Multiplex ratio is equal to N.
0 0	D3	1 0	1 0	0 X_5	1 X_4	0 X_3	0 X_2	1 X_1	1 X_0	Set Display Offset	After POR, X5X4X3X2X1X0 = 0 After setting MUX ratio less than default value, data will be displayed at the beginning/towards the end of display matrix. To move display towards Row 0 by L, X5X4X3X2X1X0 = L To move display away from Row 0 by L, X5X4X3X2X1X0 = Y - L Note: max value of L = Y – display MUX Y represents POR default MUX
0 0	E2	1 1	1 1	1 1	0 0	0 0	0 0	1 1	0 1	Software Reset	Initialize internal status registers.
0	E3	1	1	1	0	0	0	1	1	NOP	No operation
0 0	E9	1 X7	1 0	1 0	0 0	1 0	0 1	0 0	1 0	Set Bias Resistor Ladder	X7: Bias Resistor Ladder Enable 0: Disable (POR) 1: Enable
0 0	F6	1 0	1 X_6	1 0	1 0	0 0	1 0	1 0	0 0	Set Internal Oscillator	X6: Oscillator Enable 0: Disable (POR) 1: Enable

9. Reliability Test Item

Test Item	Test Condition	Test result determinant gist
High temperature storage	70±3℃; 240H	the inspection of appearance and function character.
Low temperature storage	-20±3℃; 240H	
High temperature /humidity storage	40℃±3℃, 90%±3%RH; 96H	
High temperature operation	50±3℃; 240H	no objection of the function character; no fatal objection of the appearance.
Low temperature operation	0±3℃; 240H	
Temperature Shock	-0±3℃, 30min? 50±3℃, 30min; 10cycle	inspect the objections appearance、function & the whole structure

10. Suggestions for using LCD modules

10.1 Handling of LCM

1. The LCD screen is made of glass. Don't give excessive external shock, or drop from a high place.
2. If the LCD screen is damaged and the liquid crystal leaks out, do not lick and swallow. When the liquid is attach to your hand, skin, cloth etc, wash it off by using soap and water thoroughly and immediately.
3. Don't apply excessive force on the surface of the LCM.
4. If the surface is contaminated ,clean it with soft cloth. If the LCM is severely contaminated , use Isopropyl alcohol/Ethyl alcohol to clean. Other solvents may damage the polarizer . The following solvents is especially prohibited: water , ketone Aromatic solvents etc.
5. Exercise care to minimize corrosion of the electrode. Corrosion of the electrodes is accelerated by water droplets, moisture condensation or a current flow in a high-humidity environment.
6. Install the LCD Module by using the mounting holes. When mounting the LCD module make sure it is free of twisting, warping and distortion. In particular, do not forcibly pull or bend the I/O cable or the backlight cable.
7. Don’t disassemble the LCM.
8. To prevent destruction of the elements by static electricity, be careful to maintain an optimum work environment.
    - Be sure to ground the body when handling the LCD modules.
    - Tools required for assembling, such as soldering irons, must be properly grounded.
    - To reduce the amount of static electricity generated, do not conduct assembling and other work under dry conditions.
    - The LCD module is coated with a film to protect the display surface. Exercise care when peeling off this protective film since static electricity may be generated.
9. Do not alter, modify or change the the shape of the tab on the metal frame.
10. Do not make extra holes on the printed circuit board, modify its shape or change the positions of components to be attached.

11. Do not damage or modify the pattern writing on the printed circuit board.
12. Absolutely do not modify the zebra rubber strip (conductive rubber) or heat seal connector
13. Except for soldering the interface, do not make any alterations or modifications with a soldering iron.
14. Do not drop, bend or twist LCM.

10.2 Storage

1. Store in an ambient temperature of 5 to 45 °C, and in a relative humidity of 40% to 60%. Don't expose to sunlight or fluorescent light.
2. Storage in a clean environment, free from dust, active gas, and solvent.
3. Store in antistatic container.

11. Inspection Standard

SAMPLING METHOD
SAMPLING PLAN: MIL-STD 105E
CLASS OF AQL: LEVEL II/ SINGLE SAMPLING
MAJOR-0.65% MINOR – 1.5%

QUALITY STANDARD

DEFECT	CRITERIA	TYPE	FIGURE
SHORT CIRCUIT	-	MAJOR	-
MISSING SEGMENT	-	MAJOR	-
UNEVEN / POOR CONTRAST	-	MAJOR	-
CROSS TALK	-	MAJOR	-
PIN HOLE	MAX(a,b) ≤ 1 / 4 W	MINOR	1
EXCESS SEGMENT	MAX(c,d) ≤ 1 / 4 T	MINOR	1
BUBBLES	d* ≥ 0.2 QTY=0	MINOR	2
BLACKS SPOTS	d ≤ 0.3 N.A.** 0.3<d≤0.4 QTY≤1 0.4<d QTY=0	MINOR	2
LINE SCRATCHES	x≥0.7 y≥0.05 QTY=0	MINOR	3
BLACK LINE	x≥0.7 y≥0.05 QTY=0	MINOR	3

*d = MAX (d_1,d_2) ** N. A . = NOT APPLICABLE DEFECT TABLE : B

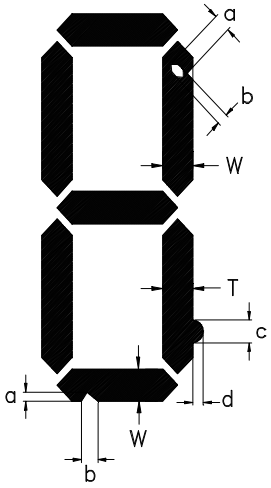
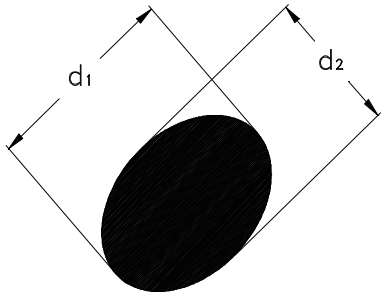
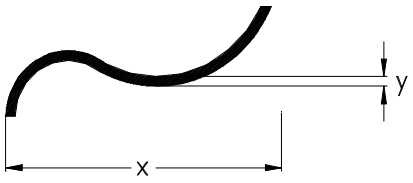


fig . 1



POLARIZER BUBBLES / SPOTS

fig . 2



LINE SCRATCHES / BLACK LINE

QUALITY STANDARD (CONT .)

DEFECT		CRITERIA	TYPE	FIGURE
CHIPS	CONTACT EDGE	e≤1/2T f≤1/3W g≤3.5	MINOR	4
	BOTTOM GLASS	p≤1.0 q≤3.5 r≤1/2T		4
	CORNER	a≤1.5 b≤W		4
	TOP GLASS	a≤3.0 b≤1/3T c≤1/2W		5
GLASS PROTRUSION		a ≤ 1/4 W	MINOR	6
RAINBOW		-	MINOR	-

UNLESS STATE OTHERWISE , ALL UNIT ARE IN MILLIMETER . DEFECT TABLE : B

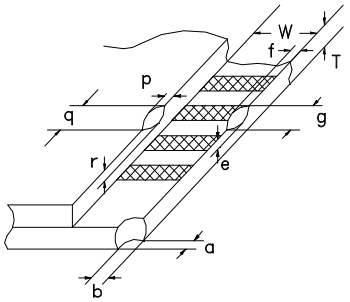


fig . 4

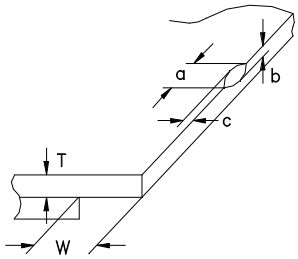
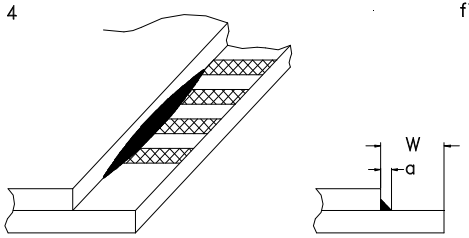


fig . 5



11. Packing (Reference only)

T.B.D

- END -

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