

100-MHz 32-bit RX MCU, on-chip FPU, 165 DMIPS, up to 2-MB flash memory, various communications interfaces including Ethernet MAC, full-speed USB 2.0 host/function/OTG interface, CAN, 10- & 12-bit A/D converters, RTC

Features

RX63N Group products incorporate an Ethernet controller while RX631 Group products do not.

■ 32-bit RX CPU core

- Max. operating frequency: 100 MHz
- Capable of 165 DMIPS in operation at 100 MHz
- Single precision 32-bit IEEE-754 floating point
- Two types of multiply-and-accumulation unit (between memories and between registers)
- 32-bit multiplier (fastest instruction execution takes one CPU clock cycle)
- Divider (fastest instruction execution takes two CPU clock cycles)
- Fast interrupt
- CISC Harvard architecture with 5-stage pipeline
- Variable-length instructions: Ultra-compact code
- Supports the memory protection unit (MPU)
- JTAG and FINE (two-line) debugging interfaces

■ Low-power design and architecture

- Operation from a single 2.7- to 3.6-V supply
- Low power consumption: A product that supports all peripheral functions draws only 500 μ A/MHz.
- RTC is capable of operation from a dedicated power supply (min. operating voltage: 2.3 V).
- Four low-power modes

■ On-chip main flash memory, no wait states

- Supports ROM-less versions and versions with up to 2 Mbytes of ROM (ROMless/256 Kbytes/384 Kbytes/512 Kbytes: RX631 Group only)
- 100-MHz operation, 10-ns read cycle (no wait states)
- 768-Kbyte to 2-Mbyte capacities
- User code is programmable by on-board or off-board programming

■ On-chip data flash memory

- ROM-less or 32 Kbytes of ROM (reprogrammable up to 100,000 times)
- Programming/erasing as background operations (BGOs)

■ On-chip SRAM, no wait states

- 64 Kbytes/128 Kbytes/192 Kbytes/256 Kbytes of SRAM
- For instructions and operands
- Can provide backup on deep software standby

■ DMA

- DMAC: Four channels
- DTC
- EXDMAC: Two channels
- Dedicated DMAC for the Ethernet controller: Single channel

■ Reset and supply management

- Power-on reset (POR)
- Low voltage detection (LVD) with voltage settings

■ Clock functions

- External crystal oscillator or internal PLL for operation at 4 to 16 MHz
- Internal 125-kHz LOCO and 50-MHz HOCO
- 125-kHz clocks for the IWDT

■ Real-time clock

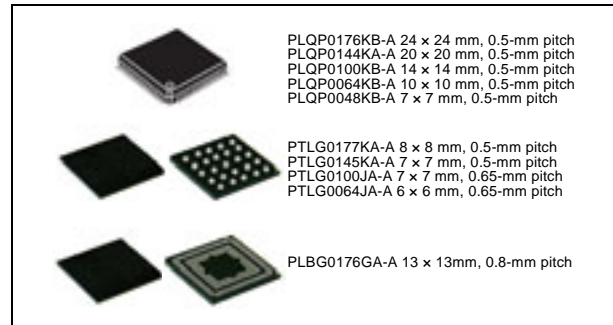
- Adjustment functions (30 seconds, leap year, and error)
- Time capture function
(for capturing times in response to event-signal input on external pins)

■ Independent watchdog timer

- 125-kHz LOCO clock operation

■ Useful functions for IEC60730 compliance

- Oscillation-stoppage detection, frequency measurement, CRC, IWDT, self-diagnostic function for the A/D converter, etc.



■ Various communications interfaces

- Ethernet MAC (1) (not in RX631 Group products)
- Host/function or OTG controller (1) and function controller (1) with full-speed USB 2.0 transfer
- CAN (compliant with ISO11898-1), incorporating 32 mailboxes (up to 3 modules)
- SCI with multiple functionalities (up to 13)
- Choose from among asynchronous mode, clock-synchronous mode, smart-card interface mode, simplified SPI, simplified I2C, and extended serial mode.
- I²C bus interface for transfer at up to 1 Mbps (up to 4)
- RSPI for high-speed transfer (up to 3)
- Parallel data capture unit (PDC) (1) (available for 512 Kbytes/384 Kbytes/256 Kbytes flash memory with 177-pin, 176-pin, 145-pin, and 144-pin)

■ External address space

- Buses for high-speed data transfer (max. operating frequency of 50 MHz)
- 8 CS areas (8 \times 16 Mbytes)
- Multiplexed bus or separate bus are selectable per area.
- 8-, 16-, or 32-bit bus space is selectable per area
- Independent SDRAM area (128 Mbytes)

■ Up to 20 extended-function timers

- 16-bit MTU2: input capture, output compare, PWM waveform output, phase-counting mode (6 channels)
- 16-bit TPU: input capture, output compare, phase-counting mode (12 channels)
- 8-bit TMR (4 channels)
- 16-bit compare-match timers (4 channels)

■ A/D converter for 1-MHz Operation

- Up to 21 \times 12-bit channels, and incorporating 1 sample-and-hold circuit
Up to 8 \times 10-bit channels, and incorporating 1 sample-and-hold circuit
- Addition of results of A/D conversion (in the 12-bit converter)
- Self diagnosis (for the 10-bit converter)

■ 10-bit D/A converter: 2 channels

■ Temperature sensor for measuring temperature within the chip

■ DEU

- AES encryption and decryption functions
- 128/192/256-bit key length
- ECB/CBC mode

■ Register write protection can protect values in important registers against overwriting.

■ Up to 134 pins for general I/O ports

- 5-V tolerance, open drain, input pull-up, switchable driving ability

■ Unique ID

- 16-byte ID code is provided for each chip (only for the G version)

■ Operating temp. range

- D version: -40 to +85°C
- G version: -40 to +105°C

1. Overview

1.1 Outline of Specifications

Table 1.1 lists the specifications in outline, and table 1.2 gives a comparison of the functions of products in different packages.

Table 1.1 is for products with the greatest number of functions, so numbers of peripheral modules and channels will differ in accord with the package. For details, see Table 1.2, Comparison of Functions for Different Packages in the RX63N/RX631 Group.

Table 1.1 Outline of Specifications (1/6)

| Classification | Module/Function | Description |
|---------------------------|--------------------------|---|
| CPU | CPU | <ul style="list-style-type: none"> Maximum operating frequency: 100 MHz 32-bit RX CPU Minimum instruction execution time: One instruction per state (cycle of the system clock) Address space: 4-Gbyte linear Register set of the CPU <ul style="list-style-type: none"> General purpose: Sixteen 32-bit registers Control: Nine 32-bit registers Accumulator: One 64-bit register Basic instructions: 73 Floating-point instructions: 8 DSP instructions: 9 Addressing modes: 10 Data arrangement <ul style="list-style-type: none"> Instructions: Little endian Data: Selectable as little endian or big endian On-chip 32-bit multiplier: 32 x 32 → 64 bits On-chip divider: 32 / 32 → 32 bits Barrel shifter: 32 bits Memory protection unit (MPU) |
| | FPU | <ul style="list-style-type: none"> Single precision (32-bit) floating point Data types and floating-point exceptions in conformance with the IEEE754 standard |
| Memory | ROM | <ul style="list-style-type: none"> Capacity: ROMless, 256 Kbytes, 384 Kbytes, 512 Kbytes, 768 Kbytes, 1 Mbyte, 1.5 Mbytes, 2 Mbytes 100 MHz, no-wait access On-board programming: Four types Off-board programming (parallel programmer mode) (for products with 100 pins or more) |
| | RAM | <ul style="list-style-type: none"> Capacity: 64 Kbytes, 128 Kbytes, 192 Kbytes, 256 Kbytes 100 MHz, no-wait access |
| | E2 data flash | Capacity: 32 Kbytes Programming/erasing: 100,000 times |
| MCU operating modes | | Single-chip mode, on-chip ROM enabled expansion mode, and on-chip ROM disabled expansion mode (software switching) |
| Clock | Clock generation circuit | <ul style="list-style-type: none"> Main clock oscillator, subclock oscillator, low-speed/high-speed on-chip oscillator, PLL frequency synthesizer, and IWDT-dedicated on-chip oscillator Main-clock oscillation stoppage detection Separate frequency-division and multiplication settings for the system clock (ICLK), peripheral module clock (PCLK), FlashIF clock (FCLK) and external bus clock (BCLK) The CPU and other bus masters run in synchronization with the system clock (ICLK): Up to 100 MHz Peripheral modules run in synchronization with the peripheral module clock (PCLK): Up to 50 MHz Flash IF run in synchronization with the flashIF clock (FCLK): Up to 50 MHz Devices connected to the external bus run in synchronization with the external bus clock (BCLK): Up to 50 MHz |
| Reset | | RES# pin reset, power-on reset, voltage-monitoring reset, independent watchdog timer reset, watchdog timer reset, deep software standby reset, and software reset |
| Voltage detection circuit | | When the voltage on VCC passes the voltage detection level (Vdet), an internal reset or internal interrupt is generated. |

Table 1.1 Outline of Specifications (2/6)

| Classification | Module/Function | Description |
|------------------------|----------------------------------|---|
| Low power consumption | Low power consumption facilities | <ul style="list-style-type: none"> • Module stop function • Four low power consumption modes Sleep mode, all-module clock stop mode, software standby mode, and deep software standby mode • Battery backup function |
| Interrupt | Interrupt controller (ICUb) | <ul style="list-style-type: none"> • Peripheral function interrupts: 187 sources • External interrupts: 16 (pins IRQ0 to IRQ15) • Software interrupts: One source • Non-maskable interrupts: 6 sources • Sixteen levels specifiable for the order of priority |
| External bus extension | | <ul style="list-style-type: none"> • The external address space can be divided into nine areas (CS0 to CS7, SDCS), each with independent control of access settings. Capacity of each area: 16 Mbytes (CS0 to CS7), 128 Mbytes (SDCS) A chip-select signal (CS0# to CS7#, SDCS#) can be output for each area. Each area is specifiable as an 8-, 16-, or 32-bit bus space. The data arrangement in each area is selectable as little or big endian (only for data). • SDRAM interface connectable • Bus format: Separate bus, multiplex bus • Wait control • Write buffer facility |
| DMA | DMA controller (DMAC) | <ul style="list-style-type: none"> • 4 channels • Three transfer modes: Normal transfer, repeat transfer, and block transfer • Activation sources: Software trigger, external interrupts, and interrupt requests from peripheral functions |
| | EXDMA controller (EXDMACa) | <ul style="list-style-type: none"> • 2 channels • Four transfer modes: Normal transfer, repeat transfer, block transfer, and cluster transfer • Single-address transfer enabled with the EDAKn signal • Capable of direct data transfer to TFT LCD panels • Activation sources: Software trigger, external DMA requests (EDREQn), and interrupt requests from peripheral functions |
| | Data transfer controller (DTCa) | <ul style="list-style-type: none"> • Three transfer modes: Normal transfer, repeat transfer, and block transfer • Activation sources: External interrupts and interrupt requests from peripheral functions |

Table 1.1 Outline of Specifications (3/6)

| Classification | Module/Function | Description |
|----------------|-------------------|---|
| I/O ports | General I/O ports | <ul style="list-style-type: none"> • I/O ports for the 177-pin TFLGA, 176-pin LFBGA and 176-pin LQFP I/O pins: 133 Input pins: 1 Pull-up resistors: 133 Open-drain outputs: 133 5-V tolerance: 18 • I/O ports for the 145-pin TFLGA and 144-pin LQFP I/O pins: 111 Input pins: 1 Pull-up resistors: 111 Open-drain outputs: 111 5-V tolerance: 18 • I/O ports for the 100-pin TFLGA (in the planning stage) and 100-pin LQFP I/O pins: 78 Input pins: 1 Pull-up resistors: 78 Open-drain outputs: 78 5-V tolerance: 17 • I/O ports for the 64-pin TFLGA I/O pins: 39 Input pin: 1 Pull-up resistors: 39 Open-drain outputs: 39 5-V tolerance: 8 • I/O ports for the 64-pin LQFP I/O pins: 42 Input pin: 1 Pull-up resistors: 42 Open-drain outputs: 42 5-V tolerance: 8 8-bit port switching function • I/O ports for the 48-pin LQFP I/O pins: 30 Input pin: 1 Pull-up resistors: 30 Open-drain outputs: 30 5-V tolerance: 6 8-bit port switching function |

Table 1.1 Outline of Specifications (4/6)

| Classification | Module/Function | Description |
|----------------|---|---|
| Timers | 16-bit timer pulse unit (TPUa) | <ul style="list-style-type: none"> • (16 bits x 6 channels) x 2 unit • Maximum of 16 pulse-input/output possible • Select from among seven or eight counter-input clock signals for each channel • Input capture/output compare function • Output of PWM waveforms in up to 15 phases in PWM mode • Buffered operation and phase-counting mode (two phase encoder input) depending on the channel • Support for cascade-connected operation (32 bits x 2 channels) • PPG output trigger can be generated • Capable of generating conversion start triggers for the A/D converters • Signals from the input capture pins are input via a digital filter • Clock frequency measuring method |
| | Multi-function timer pulse unit 2 (MTU2a) | <ul style="list-style-type: none"> • (16 bits x 6 channels) x 1 unit • Time bases for the 6 x 16-bit timer channels can be provided via up to sixteen pulse-input/output lines and three pulse-input lines • Select from among eight counter-input clock signals for each channel (PCLK/1, PCLK/4, PCLK/16, PCLK/64, MTCLKA, MTCLKB, MTCLKC, MTCLKD) other than channel 5, for which only four signals are available. • Input capture function • 21 output compare/input capture registers • Complementary PWM output mode • Reset synchronous PWM mode • Phase-counting mode • Generation of triggers for A/D converter conversion • Digital filter • Signals from the input capture pins are input via a digital filter • PPG output trigger can be generated • Clock frequency measuring function |
| | Frequency measuring method (MCK) | The MTU or unit 0 TPU module can be used to monitor the main clock, subclock, HOCO clock, LOCO clock, and PLL clock for abnormal frequencies. |
| | Port output enable 2 (POE2a) | Controls the high-impedance state of the MTU's waveform output pins |
| | Programmable pulse generator (PPG) | <ul style="list-style-type: none"> • (4 bits x 4 groups) x 2 units • Pulse output with the MTU2 or TPU output as a trigger • Maximum of 32 pulse-output possible |
| | 8-bit timers (TMR) | <ul style="list-style-type: none"> • (8 bits x 2 channels) x 2 units • Select from among seven internal clock signals (PCLK/1, PCLK/2, PCLK/8, PCLK/32, PCLK/64, PCLK/1024, PCLK/8192) and one external clock signal • Capable of output of pulse trains with desired duty cycles or of PWM signals • The 2 channels of each unit can be cascaded to create a 16-bit timer • Generation of triggers for A/D converter conversion • Capable of generating baud-rate clocks for SCI5, SCI6, and SCI12 |
| | Compare match timer (CMT) | <ul style="list-style-type: none"> • (16 bits x 2 channels) x 2 units • Select from among four internal clock signals (PCLK/8, PCLK/32, PCLK/128, PCLK/512) |
| | Realtime clock (RTCa) | <ul style="list-style-type: none"> • Clock sources: Main clock, subclock • Clock and calendar functions • Interrupt sources: Alarm interrupt, periodic interrupt, and carry interrupt • Battery backup operation • Time-capture facility for three values |
| | Watchdog timer (WDTa) | <ul style="list-style-type: none"> • 14 bits x 1 channel • Select from among 6 counter-input clock signals (PCLK/4, PCLK/64, PCLK/128, PCLK/512, PCLK/2048, PCLK/8192) |
| | Independent watchdog timer (IWDTa) | <ul style="list-style-type: none"> • 14 bits x 1 channel • Counter-input clock: IWDT-dedicated on-chip oscillator • Dedicated clock/1, dedicated clock/16, dedicated clock/32, dedicated clock/64, dedicated clock/128, dedicated clock/256 |

Table 1.1 Outline of Specifications (5/6)

| Classification | Module/Function | Description |
|------------------------|--|---|
| Communication function | Ethernet controller (ETHERC) | <ul style="list-style-type: none"> Input and output of Ethernet/IEEE 802.3 frames Transfer at 10 or 100 Mbps Full- and half-duplex modes MII (Media Independent Interface) or RMII (Reduced Media Independent Interface) as defined in IEEE 802.3u Detection of Magic Packets™*1 or output of a "wake-on-LAN" signal (WOL) Compliance with flow control as defined in IEEE 802.3x standards <p>Note 1. Magic Packet™ is a registered trademark of Advanced Micro Devices, Inc.</p> |
| | DMA controller for Ethernet controller (EDMAC) | <ul style="list-style-type: none"> Alleviation of CPU loads by the descriptor control method Transmission FIFO: 2 Kbytes; Reception FIFO: 2 Kbytes |
| | USB 2.0 host/function module (USBa) | <ul style="list-style-type: none"> Includes a UDC (USB Device Controller) and transceiver for USB 2.0 Host/function module: one port, function module: one port Compliance with the USB 2.0 specification Transfer rate: Full speed (12 Mbps) Self-power mode and bus-power mode are selectable OTG (On the Go) operation is possible Incorporates 2 Kbytes of RAM as a transfer buffer |
| | Serial communications interfaces (SC1c, SC1d) | <ul style="list-style-type: none"> 13 channels (SC1c: 12 channels + SC1d: 1 channel) SC1c <ul style="list-style-type: none"> Serial communications modes: Asynchronous, clock synchronous, and smart-card interface Multi-processor function On-chip baud rate generator allows selection of the desired bit rate Choice of LSB-first or MSB-first transfer Average transfer rate clock can be input from TMR timers for SC15, SC16, and SC112 Simple I²C Simple SPI SC1d (The following functions are added to SC1c) <ul style="list-style-type: none"> Supports the serial communications protocol, which contains the start frame and information frame Supports the LIN format |
| | I ² C bus interfaces (RIIC) | <ul style="list-style-type: none"> 4 channels (one of them is FM+) Communication formats <ul style="list-style-type: none"> I²C bus format/SMBus format Supports the multi-master Max. transfer rate: 1 Mbps (channel 0) |
| | IEBus (IEB) | <ul style="list-style-type: none"> 1 channel Supports protocol control for the IEBus <ul style="list-style-type: none"> Half-duplex asynchronous transfer Multi-master operation Broadcast communications function Two selectable modes, differentiated by transfer rate |
| | CAN module (CAN) | <ul style="list-style-type: none"> 3 channels Compliance with the ISO11898-1 specification (standard frame and extended frame) 32 mailboxes each |
| | Serial peripheral interfaces (SPI) | <ul style="list-style-type: none"> 3 channels RSPI transfer facility <ul style="list-style-type: none"> Using the MOSI (master out, slave in), MISO (master in, slave out), SSL (slave select), and RSPCK (RSPI clock) signals enables serial transfer through SPI operation (four lines) or clock-synchronous operation (three lines) Capable of handling serial transfer as a master or slave Data formats <ul style="list-style-type: none"> Switching between MSB first and LSB first The number of bits in each transfer can be changed to any number of bits from 8 to 16, or to 20, 24, or 32 bits. 128-bit buffers for transmission and reception Up to four frames can be transmitted or received in a single transfer operation (with each frame having up to 32 bits) Buffered structure <ul style="list-style-type: none"> Double buffers for both transmission and reception |

Table 1.1 Outline of Specifications (6/6)

| Classification | Module/Function | Description |
|-------------------------------|----------------------------------|---|
| Communication function | Parallel data capture unit (PDC) | <ul style="list-style-type: none"> 1 channel Communicates with an image sensor or other external I/Os and transfer parallel data such as an image output from those devices to internal RAM or external address spaces (CS space and SDRAM space) through DTC or DMAC. |
| 12-bit A/D converter (S12ADa) | | <ul style="list-style-type: none"> 1 unit (1 unit x 21 channels) 12-bit resolution Conversion time: 1.0 μs per channel (in operation with PCLK at 50 MHz) Operating mode Scan mode (single scan mode or continuous scan mode) Sample-and-hold function Reference voltage generation Three ways to start A/D conversion Conversion can be started by software, a conversion start trigger from a timer (MTU, TPU, or TMR), or an external trigger signal. A/D conversion of the temperature sensor output |
| 10-bit A/D converter (ADb) | | <ul style="list-style-type: none"> 1 unit (1 unit x 8 channels) 10-bit resolution Conversion time: 1.0 μs per channel (in operation with PCLK at 50 MHz) Operating mode Scan mode (single scan mode or continuous scan mode) External amplifier connection mode Sample-and-hold function Three ways to start A/D conversion Conversion can be started by software, a conversion start trigger from a timer (MTU, TPU, or TMR), or an external trigger signal. |
| D/A converter (DAa) | | <ul style="list-style-type: none"> 2 channels 10-bit resolution Output voltage: 0 V to VREFH |
| Temperature sensor | | <ul style="list-style-type: none"> 1 channel Precision: $\pm 1^\circ\text{C}$ The voltage of the temperature is converted into a digital value by the 12-bit A/D converter. |
| CRC calculator (CRC) | | <ul style="list-style-type: none"> CRC code generation for arbitrary amounts of data in 8-bit units Select any of three generating polynomials: $X^8 + X^2 + X + 1$, $X^{16} + X^{15} + X^2 + 1$, or $X^{16} + X^{12} + X^5 + 1$. Generation of CRC codes for use with LSB-first or MSB-first communications is selectable |
| Unique ID | | A 16-byte device-specific ID (only for the G version) |
| Data encryption unit (DEU)*1 | | <ul style="list-style-type: none"> AES encryption and decryption functions 128/192/256-bit key length ECB/CBC mode |
| Operating frequency | | Up to 100 MHz |
| Power supply voltage | | VCC = AVCC0 = VREFH = VCC_USB = 2.7 to 3.6 V, VREFH0 = 2.7 V to AVCC0, V _{BATT} = 2.0 V to 3.6 V (for products with 100 or more pins), V _{BATT} = 2.3 V to 3.6 V (for the 64-pin product) |
| Operating temperature | | D version: -40 to +85°C, G version: -40 to +105°C*2 |
| Package | | 177-pin TFLGA (PTLG0177KA-A) 176-pin LFBGA (PLBG0176GA-A) 176-pin LQFP (PLQP0176KB-A) 145-pin TFLGA (PTLG0145KA-A) 144-pin LQFP (PLQP0144KA-A) 100-pin TFLGA (PTLG0100JA-A) (in the planning stage) 100-pin LQFP (PLQP0100KB-A) 64-pin TFLGA (PTLG0064JA-A) 64-pin LQFP (PLQP0064KB-A) 48-pin LQFP (PLQP0048KB-A) |
| On-chip debugging system | | <ul style="list-style-type: none"> E1 emulator (JTAG and FINE interfaces) E20 emulator (JTAG interface) |

Note 1. Please contact our sales office for more information.

Note 2. Please contact us if you are using a G version.

Table 1.2 Comparison of Functions for Different Packages in the RX63N/RX631 Group

| Functions | | RX63N Group | | | RX631 Group | | | | | |
|--|---|---|---------------------------|---------------|---|---------------------------|-------------------------------|-------------------------------|--------------------|---------------|
| | | 177-pin 176-pin | 145-pin 144-pin | 100-pin | 177-pin 176-pin | 145-pin 144-pin | 100-pin | 64-pin LQFP | 64-pin TFLGA | 48-pin |
| External bus width | External bus width | 32 bits | 16 bits | | 32 bits | 16 bits | | | | Not available |
| | SDRAM area controller | Available | | Not available | Available | | | | | Not available |
| DMA | DMA controller | Ch. 0 to 3 | | | Ch. 0 to 3 | | | | | |
| | EXDMA controller | Ch. 0 and 1 | | | Ch. 0 and 1 | | | | | Not available |
| | Data transfer controller | Available | | | Available | | | | | |
| Timers | 16-bit timer pulse unit | Ch. 0 to 11 | Ch. 0 to 5 | | Ch. 0 to 11 | | | | | Ch. 0 to 5 |
| | Multi-function timer pulse unit 2 | Ch. 0 to 5 | | | Ch. 0 to 5 | | | | | |
| | Port output enable 2 | Available | | | Available | | | | | |
| | Programmable pulse generator | Ch. 0 and 1 | | | Ch. 0 and 1 | | | | | |
| | 8-bit timers | Ch. 0 to 3 | | | Ch. 0 to 3 | | | | | |
| | Compare match timer | Ch. 0 to 3 | | | Ch. 0 to 3 | | | | | |
| | Realtime clock | Available | | | | Available | | | | Not available |
| | Watchdog timer | Available | | | Available | | | | | |
| | Independent watchdog timer | Available | | | Available | | | | | |
| Communication function | Ethernet controller | Available | | | Not available | | | | | |
| | DMA controller for Ethernet controller | Available | | | Not available | | | | | |
| | USB 2.0 host/function module | Ch. 0 and 1 | Ch.0 | | Ch. 0 and 1 | Ch.0 | | Ch. 0 and 1 | Ch.0 | |
| | Serial communications interfaces (SClc) | Ch. 0 to 11 | Ch. 0 to 3, 5, 6, 8 and 9 | | Ch. 0 to 11 | Ch. 0 to 3, 5, 6, 8 and 9 | | Ch. 1, 5, 6, 8 and 9 | Ch. 1, 5, 6, and 8 | |
| | Serial communications interfaces (SCld) | Ch. 12 | | | Ch. 12 | | | | | |
| | I ² C bus interfaces | Ch. 0 to 3 | Ch.0 and 2 | | Ch. 0 to 3 | Ch.0 and 2 | | Ch.2 | | |
| | IEBus | Available | | | Available | | | | | |
| | Serial peripheral interfaces | Ch.0 to 2 | Ch. 0 and 1 | | Ch.0 to 2 | | | Ch. 0 and 1 | | |
| | CAN module | For 1.5 M or more: Ch. 0 to 2, For 1 M or less: Ch. 0 and 1 | Ch. 0 and 1 | | For 1.5 M or more: Ch. 0 to 2, For 1 M or less: Ch. 0 and 1 | Ch. 0 and 1 | | Ch.1 | | |
| | Parallel data capture unit (PDC) | Not available | | | Available | | Not available | | | |
| 12-bit A/D converter (channel) | AN000 to 020 | AN000 to 013 | | AN000 to 020 | AN000 to 013 | | AN000 to 004, 006, 008 to 013 | AN000 to 002, 006, 009 to 012 | | |
| 10-bit A/D converter (channel) | AN0 to 7 | | | AN0 to 7 | | Not available | | | | |
| D/A converter | Ch. 0 and 1 | Ch.1 | | Ch. 0 and 1 | Ch.1 | | Ch.1 | Not available | | |
| Temperature sensor | Available | | | Available | | | | | | |
| CRC calculator | Available | | | Available | | | | | | |
| Unique ID | Available (only for the G version) | | | | | | | | | |
| Off-board programming (parallel programmer mode) | | | | Available | | Not available | | | | |
| Sub-clock oscillator (for low clock loads) | | | | Available | | Not available | | | | |
| Sub-clock oscillator (for standard clock loads) | | | | Available | | Not available | | | | |
| Battery backup function | | | | Available | | Not available | | | | |
| I/O port switching function | Not available | | | Not available | | Available | | | | |

1.2 List of Products

Table 1.3 is a list of products, and Figure 1.1 shows how to read the product part no.

Table 1.3 List of Products (1/8)

| Group | Part No. | Package | ROM Capacity | RAM Capacity | E2 Data Flash | Operating Frequency (Max.) | Operating Temp. Range |
|----------------------|--------------|----------------|--------------|--------------|---------------|----------------------------|-----------------------|
| RX63N (D version) | R5F563NECDLC | PTLG0177KA-A | 2 Mbytes | 128 Kbytes | 32 Kbytes | 100 MHz | -40 to +85°C |
| | R5F563NEDDLC | PTLG0177KA-A | 2 Mbytes | 128 Kbytes | 32 Kbytes | 100 MHz | -40 to +85°C |
| | R5F563NDCDLC | PTLG0177KA-A | 1.5 Mbytes | 128 Kbytes | 32 Kbytes | 100 MHz | -40 to +85°C |
| | R5F563NDDDL | PTLG0177KA-A | 1.5 Mbytes | 128 Kbytes | 32 Kbytes | 100 MHz | -40 to +85°C |
| | R5F563NBCDLC | PTLG0177KA-A | 1 Mbyte | 128 Kbytes | 32 Kbytes | 100 MHz | -40 to +85°C |
| | R5F563NBDDL | PTLG0177KA-A | 1 Mbyte | 128 Kbytes | 32 Kbytes | 100 MHz | -40 to +85°C |
| | R5F563NACDLC | PTLG0177KA-A | 768 Kbytes | 128 Kbytes | 32 Kbytes | 100 MHz | -40 to +85°C |
| | R5F563NADDLC | PTLG0177KA-A | 768 Kbytes | 128 Kbytes | 32 Kbytes | 100 MHz | -40 to +85°C |
| | R5F563NECDBG | PLBG0176GA-A | 2 Mbytes | 128 Kbytes | 32 Kbytes | 100 MHz | -40 to +85°C |
| | R5F563NEDDBG | PLBG0176GA-A | 2 Mbytes | 128 Kbytes | 32 Kbytes | 100 MHz | -40 to +85°C |
| | R5F563NDCDBG | PLBG0176GA-A | 1.5 Mbytes | 128 Kbytes | 32 Kbytes | 100 MHz | -40 to +85°C |
| | R5F563NDDDBG | PLBG0176GA-A | 1.5 Mbytes | 128 Kbytes | 32 Kbytes | 100 MHz | -40 to +85°C |
| | R5F563NBCDBG | PLBG0176GA-A | 1 Mbyte | 128 Kbytes | 32 Kbytes | 100 MHz | -40 to +85°C |
| | R5F563NBDDBG | PLBG0176GA-A | 1 Mbyte | 128 Kbytes | 32 Kbytes | 100 MHz | -40 to +85°C |
| | R5F563NACDBG | PLBG0176GA-A | 768 Kbytes | 128 Kbytes | 32 Kbytes | 100 MHz | -40 to +85°C |
| | R5F563NADDBG | PLBG0176GA-A | 768 Kbytes | 128 Kbytes | 32 Kbytes | 100 MHz | -40 to +85°C |
| | R5F563NFHDFC | PLQP0176KB-A | 2 Mbytes | 256 Kbytes | 32 Kbytes | 100 MHz | -40 to +85°C |
| | R5F563NFDDFC | PLQP0176KB-A | 2 Mbytes | 256 Kbytes | 32 Kbytes | 100 MHz | -40 to +85°C |
| | R5F563NKHDFC | PLQP0176KB-A*1 | 2 Mbytes | 192 Kbytes | 32 Kbytes | 100 MHz | -40 to +85°C |
| | R5F563NKDDFC | PLQP0176KB-A | 2 Mbytes | 192 Kbytes | 32 Kbytes | 100 MHz | -40 to +85°C |
| | R5F563NECDFC | PLQP0176KB-A | 2 Mbytes | 128 Kbytes | 32 Kbytes | 100 MHz | -40 to +85°C |
| | R5F563NEDDFC | PLQP0176KB-A | 2 Mbytes | 128 Kbytes | 32 Kbytes | 100 MHz | -40 to +85°C |
| | R5F563NJHDFC | PLQP0176KB-A*1 | 1.5 Mbytes | 256 Kbytes | 32 Kbytes | 100 MHz | -40 to +85°C |
| | R5F563NJDDFC | PLQP0176KB-A*1 | 1.5 Mbytes | 256 Kbytes | 32 Kbytes | 100 MHz | -40 to +85°C |
| | R5F563NGHDFC | PLQP0176KB-A*1 | 1.5 Mbytes | 192 Kbytes | 32 Kbytes | 100 MHz | -40 to +85°C |
| | R5F563NGDDFC | PLQP0176KB-A*1 | 1.5 Mbytes | 192 Kbytes | 32 Kbytes | 100 MHz | -40 to +85°C |
| | R5F563NDCDFC | PLQP0176KB-A | 1.5 Mbytes | 128 Kbytes | 32 Kbytes | 100 MHz | -40 to +85°C |
| | R5F563NDDDFC | PLQP0176KB-A | 1.5 Mbytes | 128 Kbytes | 32 Kbytes | 100 MHz | -40 to +85°C |
| | R5F563NYHDFC | PLQP0176KB-A | 1 Mbyte | 256 Kbytes | 32 Kbytes | 100 MHz | -40 to +85°C |
| | R5F563NYDDFC | PLQP0176KB-A | 1 Mbyte | 256 Kbytes | 32 Kbytes | 100 MHz | -40 to +85°C |
| | R5F563NWHDFC | PLQP0176KB-A | 1 Mbyte | 192 Kbytes | 32 Kbytes | 100 MHz | -40 to +85°C |
| | R5F563NWDDFC | PLQP0176KB-A | 1 Mbyte | 192 Kbytes | 32 Kbytes | 100 MHz | -40 to +85°C |
| | R5F563NWGDFC | PLQP0176KB-A | 1 Mbyte | 192 Kbytes | 32 Kbytes | 100 MHz | -40 to +85°C |
| | R5F563NWCDFC | PLQP0176KB-A | 1 Mbyte | 192 Kbytes | 32 Kbytes | 100 MHz | -40 to +85°C |
| | R5F563NBCDFC | PLQP0176KB-A | 1 Mbyte | 128 Kbytes | 32 Kbytes | 100 MHz | -40 to +85°C |
| | R5F563NBDDFC | PLQP0176KB-A | 1 Mbyte | 128 Kbytes | 32 Kbytes | 100 MHz | -40 to +85°C |
| | R5F563NACDFC | PLQP0176KB-A | 768 Kbytes | 128 Kbytes | 32 Kbytes | 100 MHz | -40 to +85°C |
| | R5F563NADDFC | PLQP0176KB-A | 768 Kbytes | 128 Kbytes | 32 Kbytes | 100 MHz | -40 to +85°C |
| | R5F563NECDLK | PTLG0145KA-A | 2 Mbytes | 128 Kbytes | 32 Kbytes | 100 MHz | -40 to +85°C |
| | R5F563NEDDLK | PTLG0145KA-A | 2 Mbytes | 128 Kbytes | 32 Kbytes | 100 MHz | -40 to +85°C |
| R5F563NDCDLK | PTLG0145KA-A | 1.5 Mbytes | 128 Kbytes | 32 Kbytes | 100 MHz | -40 to +85°C | |

Table 1.3 List of Products (2/8)

| Group | Part No. | Package | ROM Capacity | RAM Capacity | E2 Data Flash | Operating Frequency (Max.) | Operating Temp. Range |
|----------------------|----------------|----------------|--------------|--------------|---------------|----------------------------|-----------------------|
| RX63N (D version) | R5F563NDDDLK | PTLG0145KA-A | 1.5 Mbytes | 128 Kbytes | 32 Kbytes | 100 MHz | -40 to +85°C |
| | R5F563NBCDLK | PTLG0145KA-A | 1 Mbyte | 128 Kbytes | 32 Kbytes | 100 MHz | -40 to +85°C |
| | R5F563NBDDLK | PTLG0145KA-A | 1 Mbyte | 128 Kbytes | 32 Kbytes | 100 MHz | -40 to +85°C |
| | R5F563NACDLK | PTLG0145KA-A | 768 Kbytes | 128 Kbytes | 32 Kbytes | 100 MHz | -40 to +85°C |
| | R5F563NADDLK | PTLG0145KA-A | 768 Kbytes | 128 Kbytes | 32 Kbytes | 100 MHz | -40 to +85°C |
| | R5F563NFHDFB | PLQP0144KA-A | 2 Mbytes | 256 Kbytes | 32 Kbytes | 100 MHz | -40 to +85°C |
| | R5F563NFDDFB | PLQP0144KA-A | 2 Mbytes | 256 Kbytes | 32 Kbytes | 100 MHz | -40 to +85°C |
| | R5F563NKHDFB | PLQP0144KA-A*1 | 2 Mbytes | 192 Kbytes | 32 Kbytes | 100 MHz | -40 to +85°C |
| | R5F563NKDDFB | PLQP0144KA-A | 2 Mbytes | 192 Kbytes | 32 Kbytes | 100 MHz | -40 to +85°C |
| | R5F563NECDFB | PLQP0144KA-A | 2 Mbytes | 128 Kbytes | 32 Kbytes | 100 MHz | -40 to +85°C |
| | R5F563NEDDFB | PLQP0144KA-A | 2 Mbytes | 128 Kbytes | 32 Kbytes | 100 MHz | -40 to +85°C |
| | R5F563NJHDFB | PLQP0144KA-A*1 | 1.5 Mbytes | 256 Kbytes | 32 Kbytes | 100 MHz | -40 to +85°C |
| | R5F563NJDDFB | PLQP0144KA-A*1 | 1.5 Mbytes | 256 Kbytes | 32 Kbytes | 100 MHz | -40 to +85°C |
| | R5F563NGHDFB | PLQP0144KA-A*1 | 1.5 Mbytes | 192 Kbytes | 32 Kbytes | 100 MHz | -40 to +85°C |
| | R5F563NGDDFB | PLQP0144KA-A*1 | 1.5 Mbytes | 192 Kbytes | 32 Kbytes | 100 MHz | -40 to +85°C |
| | R5F563NDCDFB | PLQP0144KA-A | 1.5 Mbytes | 128 Kbytes | 32 Kbytes | 100 MHz | -40 to +85°C |
| | R5F563NDDDFB | PLQP0144KA-A | 1.5 Mbytes | 128 Kbytes | 32 Kbytes | 100 MHz | -40 to +85°C |
| | R5F563NYHDFB | PLQP0144KA-A | 1 Mbyte | 256 Kbytes | 32 Kbytes | 100 MHz | -40 to +85°C |
| | R5F563NYDDFB | PLQP0144KA-A | 1 Mbyte | 256 Kbytes | 32 Kbytes | 100 MHz | -40 to +85°C |
| | R5F563NWHDFB | PLQP0144KA-A | 1 Mbyte | 192 Kbytes | 32 Kbytes | 100 MHz | -40 to +85°C |
| | R5F563NWDDFB | PLQP0144KA-A | 1 Mbyte | 192 Kbytes | 32 Kbytes | 100 MHz | -40 to +85°C |
| | R5F563NBCDFB | PLQP0144KA-A | 1 Mbyte | 128 Kbytes | 32 Kbytes | 100 MHz | -40 to +85°C |
| | R5F563NBDDFB | PLQP0144KA-A | 1 Mbyte | 128 Kbytes | 32 Kbytes | 100 MHz | -40 to +85°C |
| | R5F563NACDFB | PLQP0144KA-A | 768 Kbytes | 128 Kbytes | 32 Kbytes | 100 MHz | -40 to +85°C |
| | R5F563NADDFB | PLQP0144KA-A | 768 Kbytes | 128 Kbytes | 32 Kbytes | 100 MHz | -40 to +85°C |
| | R5F563NECDLJ | PTLG0100JA-A | 2 Mbytes | 128 Kbytes | 32 Kbytes | 100 MHz | -40 to +85°C |
| | R5F563NEDDLJ | PTLG0100JA-A | 2 Mbytes | 128 Kbytes | 32 Kbytes | 100 MHz | -40 to +85°C |
| | R5F563NDCDLJ | PTLG0100JA-A*1 | 1.5 Mbytes | 128 Kbytes | 32 Kbytes | 100 MHz | -40 to +85°C |
| | R5F563NDDDLJ | PTLG0100JA-A*1 | 1.5 Mbytes | 128 Kbytes | 32 Kbytes | 100 MHz | -40 to +85°C |
| | R5F563NBCDLJ | PTLG0100JA-A | 1 Mbyte | 128 Kbytes | 32 Kbytes | 100 MHz | -40 to +85°C |
| | R5F563NBDDLJ | PTLG0100JA-A | 1 Mbyte | 128 Kbytes | 32 Kbytes | 100 MHz | -40 to +85°C |
| | R5F563NACDLJ | PTLG0100JA-A | 768 Kbytes | 128 Kbytes | 32 Kbytes | 100 MHz | -40 to +85°C |
| | R5F563NADDLJ | PTLG0100JA-A | 768 Kbytes | 128 Kbytes | 32 Kbytes | 100 MHz | -40 to +85°C |
| | R5F563NFHDFP | PLQP0100KB-A | 2 Mbytes | 256 Kbytes | 32 Kbytes | 100 MHz | -40 to +85°C |
| | R5F563NFDDFP | PLQP0100KB-A | 2 Mbytes | 256 Kbytes | 32 Kbytes | 100 MHz | -40 to +85°C |
| | R5F563NKHDFP | PLQP0100KB-A*1 | 2 Mbytes | 192 Kbytes | 32 Kbytes | 100 MHz | -40 to +85°C |
| | R5F563NKDDFP | PLQP0100KB-A | 2 Mbytes | 192 Kbytes | 32 Kbytes | 100 MHz | -40 to +85°C |
| | R5F563NECDFP | PLQP0100KB-A | 2 Mbytes | 128 Kbytes | 32 Kbytes | 100 MHz | -40 to +85°C |
| | R5F563NEDDFP | PLQP0100KB-A | 2 Mbytes | 128 Kbytes | 32 Kbytes | 100 MHz | -40 to +85°C |
| | R5F563NJHDFP | PLQP0100KB-A*1 | 1.5 Mbytes | 256 Kbytes | 32 Kbytes | 100 MHz | -40 to +85°C |
| | R5F563NJDDFP | PLQP0100KB-A*1 | 1.5 Mbytes | 256 Kbytes | 32 Kbytes | 100 MHz | -40 to +85°C |
| | R5F563NGHDFP | PLQP0100KB-A*1 | 1.5 Mbytes | 192 Kbytes | 32 Kbytes | 100 MHz | -40 to +85°C |
| R5F563NGDDFP | PLQP0100KB-A*1 | 1.5 Mbytes | 192 Kbytes | 32 Kbytes | 100 MHz | -40 to +85°C | |
| R5F563NDCDFP | PLQP0100KB-A | 1.5 Mbytes | 128 Kbytes | 32 Kbytes | 100 MHz | -40 to +85°C | |
| R5F563NDDDFP | PLQP0100KB-A | 1.5 Mbytes | 128 Kbytes | 32 Kbytes | 100 MHz | -40 to +85°C | |

Table 1.3 List of Products (3/8)

| Group | Part No. | Package | ROM Capacity | RAM Capacity | E2 Data Flash | Operating Frequency (Max.) | Operating Temp. Range |
|----------------------------|--------------|----------------|--------------|--------------|---------------|----------------------------|-----------------------|
| RX63N (D version) | R5F563NYHDFP | PLQP0100KB-A | 1 Mbyte | 256 Kbytes | 32 Kbytes | 100 MHz | -40 to +85°C |
| | R5F563NYDDFP | PLQP0100KB-A | 1 Mbyte | 256 Kbytes | 32 Kbytes | 100 MHz | -40 to +85°C |
| | R5F563NWHDFP | PLQP0100KB-A | 1 Mbyte | 192 Kbytes | 32 Kbytes | 100 MHz | -40 to +85°C |
| | R5F563NWDDFP | PLQP0100KB-A | 1 Mbyte | 192 Kbytes | 32 Kbytes | 100 MHz | -40 to +85°C |
| | R5F563NWGDFP | PLQP0100KB-A*1 | 1 Mbyte | 192 Kbytes | 32 Kbytes | 100 MHz | -40 to +85°C |
| | R5F563NWCDFP | PLQP0100KB-A*1 | 1 Mbyte | 192 Kbytes | 32 Kbytes | 100 MHz | -40 to +85°C |
| | R5F563NBCDFP | PLQP0100KB-A | 1 Mbyte | 128 Kbytes | 32 Kbytes | 100 MHz | -40 to +85°C |
| | R5F563NBDDFP | PLQP0100KB-A | 1 Mbyte | 128 Kbytes | 32 Kbytes | 100 MHz | -40 to +85°C |
| | R5F563NACDFP | PLQP0100KB-A | 768 Kbytes | 128 Kbytes | 32 Kbytes | 100 MHz | -40 to +85°C |
| R5F563NADDFP | PLQP0100KB-A | 768 Kbytes | 128 Kbytes | 32 Kbytes | 100 MHz | -40 to +85°C | |
| RX63N (G version) *2 | R5F563NFHGFC | PLQP0176KB-A | 2 Mbytes | 256 Kbytes | 32 Kbytes | 100 MHz | -40 to +105°C |
| | R5F563NFDGFC | PLQP0176KB-A | 2 Mbytes | 256 Kbytes | 32 Kbytes | 100 MHz | -40 to +105°C |
| | R5F563NKDGFC | PLQP0176KB-A | 2 Mbytes | 192 Kbytes | 32 Kbytes | 100 MHz | -40 to +105°C |
| | R5F563NEDGFC | PLQP0176KB-A | 2 Mbytes | 128 Kbytes | 32 Kbytes | 100 MHz | -40 to +105°C |
| | R5F563NDDGFC | PLQP0176KB-A | 1.5 Mbytes | 128 Kbytes | 32 Kbytes | 100 MHz | -40 to +105°C |
| | R5F563NYHGFC | PLQP0176KB-A | 1 Mbyte | 256 Kbytes | 32 Kbytes | 100 MHz | -40 to +105°C |
| | R5F563NYDGFC | PLQP0176KB-A | 1 Mbyte | 256 Kbytes | 32 Kbytes | 100 MHz | -40 to +105°C |
| | R5F563NWHGFC | PLQP0176KB-A | 1 Mbyte | 192 Kbytes | 32 Kbytes | 100 MHz | -40 to +105°C |
| | R5F563NWDGFC | PLQP0176KB-A | 1 Mbyte | 192 Kbytes | 32 Kbytes | 100 MHz | -40 to +105°C |
| | R5F563NBDGFC | PLQP0176KB-A | 1 Mbyte | 128 Kbytes | 32 Kbytes | 100 MHz | -40 to +105°C |
| | R5F563NADGFC | PLQP0176KB-A | 768 Kbytes | 128 Kbytes | 32 Kbytes | 100 MHz | -40 to +105°C |
| | R5F563NFHGFB | PLQP0144KA-A | 2 Mbytes | 256 Kbytes | 32 Kbytes | 100 MHz | -40 to +105°C |
| | R5F563NFDGFB | PLQP0144KA-A | 2 Mbytes | 256 Kbytes | 32 Kbytes | 100 MHz | -40 to +105°C |
| | R5F563NKDGFB | PLQP0144KA-A | 2 Mbytes | 192 Kbytes | 32 Kbytes | 100 MHz | -40 to +105°C |
| | R5F563NEDGFB | PLQP0144KA-A | 2 Mbytes | 128 Kbytes | 32 Kbytes | 100 MHz | -40 to +105°C |
| | R5F563NDDGFB | PLQP0144KA-A | 1.5 Mbytes | 128 Kbytes | 32 Kbytes | 100 MHz | -40 to +105°C |
| | R5F563NYHGFB | PLQP0144KA-A | 1 Mbyte | 256 Kbytes | 32 Kbytes | 100 MHz | -40 to +105°C |
| | R5F563NYDGFB | PLQP0144KA-A | 1 Mbyte | 256 Kbytes | 32 Kbytes | 100 MHz | -40 to +105°C |
| | R5F563NWHGFB | PLQP0144KA-A | 1 Mbyte | 192 Kbytes | 32 Kbytes | 100 MHz | -40 to +105°C |
| | R5F563NWDGFB | PLQP0144KA-A | 1 Mbyte | 192 Kbytes | 32 Kbytes | 100 MHz | -40 to +105°C |
| | R5F563NBDGFB | PLQP0144KA-A | 1 Mbyte | 128 Kbytes | 32 Kbytes | 100 MHz | -40 to +105°C |
| | R5F563NADGFB | PLQP0144KA-A | 768 Kbytes | 128 Kbytes | 32 Kbytes | 100 MHz | -40 to +105°C |
| | R5F563NFHGFP | PLQP0100KB-A | 2 Mbytes | 256 Kbytes | 32 Kbytes | 100 MHz | -40 to +105°C |
| | R5F563NFDGFP | PLQP0100KB-A | 2 Mbytes | 256 Kbytes | 32 Kbytes | 100 MHz | -40 to +105°C |
| | R5F563NKDGFP | PLQP0100KB-A | 2 Mbytes | 192 Kbytes | 32 Kbytes | 100 MHz | -40 to +105°C |
| | R5F563NEDGFP | PLQP0100KB-A | 2 Mbytes | 128 Kbytes | 32 Kbytes | 100 MHz | -40 to +105°C |
| | R5F563NDDGFP | PLQP0100KB-A | 1.5 Mbytes | 128 Kbytes | 32 Kbytes | 100 MHz | -40 to +105°C |
| | R5F563NYHGFP | PLQP0100KB-A | 1 Mbyte | 256 Kbytes | 32 Kbytes | 100 MHz | -40 to +105°C |
| | R5F563NYDGFP | PLQP0100KB-A | 1 Mbyte | 256 Kbytes | 32 Kbytes | 100 MHz | -40 to +105°C |
| | R5F563NWHGFP | PLQP0100KB-A | 1 Mbyte | 192 Kbytes | 32 Kbytes | 100 MHz | -40 to +105°C |
| | R5F563NWDGFP | PLQP0100KB-A | 1 Mbyte | 192 Kbytes | 32 Kbytes | 100 MHz | -40 to +105°C |
| | R5F563NBDGFP | PLQP0100KB-A | 1 Mbyte | 128 Kbytes | 32 Kbytes | 100 MHz | -40 to +105°C |
| R5F563NADGFP | PLQP0100KB-A | 768 Kbytes | 128 Kbytes | 32 Kbytes | 100 MHz | -40 to +105°C | |
| RX631 (D version) | R5F5631ECDLC | PTLG0177KA-A | 2 Mbytes | 128 Kbytes | 32 Kbytes | 100 MHz | -40 to +85°C |
| | R5F5631EDDLC | PTLG0177KA-A | 2 Mbytes | 128 Kbytes | 32 Kbytes | 100 MHz | -40 to +85°C |

Table 1.3 List of Products (4/8)

| Group | Part No. | Package | ROM Capacity | RAM Capacity | E2 Data Flash | Operating Frequency (Max.) | Operating Temp. Range |
|----------------------|---------------|----------------|--------------|--------------|---------------|----------------------------|-----------------------|
| RX631 (D version) | R5F5631DCDLC | PTLG0177KA-A | 1.5 Mbytes | 128 Kbytes | 32 Kbytes | 100 MHz | -40 to +85°C |
| | R5F5631DDDLC | PTLG0177KA-A | 1.5 Mbytes | 128 Kbytes | 32 Kbytes | 100 MHz | -40 to +85°C |
| | R5F5631BDDLC | PTLG0177KA-A | 1 Mbyte | 128 Kbytes | 32 Kbytes | 100 MHz | -40 to +85°C |
| | R5F5631BCDLC | PTLG0177KA-A | 1 Mbyte | 128 Kbytes | 32 Kbytes | 100 MHz | -40 to +85°C |
| | R5F5631ACDLC | PTLG0177KA-A | 768 Kbytes | 128 Kbytes | 32 Kbytes | 100 MHz | -40 to +85°C |
| | R5F5631ADDLC | PTLG0177KA-A | 768 Kbytes | 128 Kbytes | 32 Kbytes | 100 MHz | -40 to +85°C |
| | R5F56318CDLC | PTLG0177KA-A | 512 Kbytes | 128 Kbytes | 32 Kbytes | 100 MHz | -40 to +85°C |
| | R5F56318DDLC | PTLG0177KA-A | 512 Kbytes | 128 Kbytes | 32 Kbytes | 100 MHz | -40 to +85°C |
| | R5F56317CDLC | PTLG0177KA-A | 384 Kbytes | 128 Kbytes | 32 Kbytes | 100 MHz | -40 to +85°C |
| | R5F56317DDLC | PTLG0177KA-A | 384 Kbytes | 128 Kbytes | 32 Kbytes | 100 MHz | -40 to +85°C |
| | R5F56316CDLC | PTLG0177KA-A | 256 Kbytes | 128 Kbytes | 32 Kbytes | 100 MHz | -40 to +85°C |
| | R5F56316DDLC | PTLG0177KA-A | 256 Kbytes | 128 Kbytes | 32 Kbytes | 100 MHz | -40 to +85°C |
| | R5F5631ECDDBG | PLBG0176GA-A | 2 Mbytes | 128 Kbytes | 32 Kbytes | 100 MHz | -40 to +85°C |
| | R5F5631EDDBG | PLBG0176GA-A | 2 Mbytes | 128 Kbytes | 32 Kbytes | 100 MHz | -40 to +85°C |
| | R5F5631DCDBG | PLBG0176GA-A | 1.5 Mbytes | 128 Kbytes | 32 Kbytes | 100 MHz | -40 to +85°C |
| | R5F5631DDDBG | PLBG0176GA-A | 1.5 Mbytes | 128 Kbytes | 32 Kbytes | 100 MHz | -40 to +85°C |
| | R5F5631BCDBG | PLBG0176GA-A | 1 Mbyte | 128 Kbytes | 32 Kbytes | 100 MHz | -40 to +85°C |
| | R5F5631BDDBG | PLBG0176GA-A | 1 Mbyte | 128 Kbytes | 32 Kbytes | 100 MHz | -40 to +85°C |
| | R5F5631ACDBG | PLBG0176GA-A | 768 Kbytes | 128 Kbytes | 32 Kbytes | 100 MHz | -40 to +85°C |
| | R5F5631ADDDBG | PLBG0176GA-A | 768 Kbytes | 128 Kbytes | 32 Kbytes | 100 MHz | -40 to +85°C |
| | R5F56318CDBG | PLBG0176GA-A | 512 Kbytes | 128 Kbytes | 32 Kbytes | 100 MHz | -40 to +85°C |
| | R5F56318DDBG | PLBG0176GA-A | 512 Kbytes | 128 Kbytes | 32 Kbytes | 100 MHz | -40 to +85°C |
| | R5F56317CDBG | PLBG0176GA-A | 384 Kbytes | 128 Kbytes | 32 Kbytes | 100 MHz | -40 to +85°C |
| | R5F56317DDBG | PLBG0176GA-A | 384 Kbytes | 128 Kbytes | 32 Kbytes | 100 MHz | -40 to +85°C |
| | R5F56316CDBG | PLBG0176GA-A | 256 Kbytes | 128 Kbytes | 32 Kbytes | 100 MHz | -40 to +85°C |
| | R5F56316DDBG | PLBG0176GA-A | 256 Kbytes | 128 Kbytes | 32 Kbytes | 100 MHz | -40 to +85°C |
| | R5F5631FHDFC | PLQP0176KB-A | 2 Mbytes | 256 Kbytes | 32 Kbytes | 100 MHz | -40 to +85°C |
| | R5F5631FDDFC | PLQP0176KB-A | 2 Mbytes | 256 Kbytes | 32 Kbytes | 100 MHz | -40 to +85°C |
| | R5F5631KHDFC | PLQP0176KB-A*1 | 2 Mbytes | 192 Kbytes | 32 Kbytes | 100 MHz | -40 to +85°C |
| | R5F5631KDDFC | PLQP0176KB-A | 2 Mbytes | 192 Kbytes | 32 Kbytes | 100 MHz | -40 to +85°C |
| | R5F5631ECDFC | PLQP0176KB-A | 2 Mbytes | 128 Kbytes | 32 Kbytes | 100 MHz | -40 to +85°C |
| | R5F5631EDDFC | PLQP0176KB-A | 2 Mbytes | 128 Kbytes | 32 Kbytes | 100 MHz | -40 to +85°C |
| | R5F5631JHDFC | PLQP0176KB-A*1 | 1.5 Mbytes | 256 Kbytes | 32 Kbytes | 100 MHz | -40 to +85°C |
| | R5F5631JDDFC | PLQP0176KB-A*1 | 1.5 Mbytes | 256 Kbytes | 32 Kbytes | 100 MHz | -40 to +85°C |
| | R5F5631GHDFC | PLQP0176KB-A*1 | 1.5 Mbytes | 192 Kbytes | 32 Kbytes | 100 MHz | -40 to +85°C |
| | R5F5631GDDFC | PLQP0176KB-A*1 | 1.5 Mbytes | 192 Kbytes | 32 Kbytes | 100 MHz | -40 to +85°C |
| | R5F5631DCDFC | PLQP0176KB-A | 1.5 Mbytes | 128 Kbytes | 32 Kbytes | 100 MHz | -40 to +85°C |
| | R5F5631DDDFC | PLQP0176KB-A | 1.5 Mbytes | 128 Kbytes | 32 Kbytes | 100 MHz | -40 to +85°C |
| | R5F5631YHDFC | PLQP0176KB-A | 1 Mbyte | 256 Kbytes | 32 Kbytes | 100 MHz | -40 to +85°C |
| | R5F5631YDDFC | PLQP0176KB-A | 1 Mbyte | 256 Kbytes | 32 Kbytes | 100 MHz | -40 to +85°C |
| | R5F5631WHDFC | PLQP0176KB-A | 1 Mbyte | 192 Kbytes | 32 Kbytes | 100 MHz | -40 to +85°C |
| | R5F5631WDDFC | PLQP0176KB-A | 1 Mbyte | 192 Kbytes | 32 Kbytes | 100 MHz | -40 to +85°C |
| R5F5631BCDFC | PLQP0176KB-A | 1 Mbyte | 128 Kbytes | 32 Kbytes | 100 MHz | -40 to +85°C | |
| R5F5631BDDFC | PLQP0176KB-A | 1 Mbyte | 128 Kbytes | 32 Kbytes | 100 MHz | -40 to +85°C | |
| R5F5631ACDFC | PLQP0176KB-A | 768 Kbytes | 128 Kbytes | 32 Kbytes | 100 MHz | -40 to +85°C | |

Table 1.3 List of Products (5/8)

| Group | Part No. | Package | ROM Capacity | RAM Capacity | E2 Data Flash | Operating Frequency (Max.) | Operating Temp. Range |
|----------------------|--------------|----------------|--------------|--------------|---------------|----------------------------|-----------------------|
| RX631 (D version) | R5F5631ADDFC | PLQP0176KB-A | 768 Kbytes | 128 Kbytes | 32 Kbytes | 100 MHz | -40 to +85°C |
| | R5F56318CDFC | PLQP0176KB-A | 512 Kbytes | 128 Kbytes | 32 Kbytes | 100 MHz | -40 to +85°C |
| | R5F56318DDFC | PLQP0176KB-A | 512 Kbytes | 128 Kbytes | 32 Kbytes | 100 MHz | -40 to +85°C |
| | R5F56317CDFC | PLQP0176KB-A | 384 Kbytes | 128 Kbytes | 32 Kbytes | 100 MHz | -40 to +85°C |
| | R5F56317DDFC | PLQP0176KB-A | 384 Kbytes | 128 Kbytes | 32 Kbytes | 100 MHz | -40 to +85°C |
| | R5F56316CDFC | PLQP0176KB-A | 256 Kbytes | 128 Kbytes | 32 Kbytes | 100 MHz | -40 to +85°C |
| | R5F56316DDFC | PLQP0176KB-A | 256 Kbytes | 128 Kbytes | 32 Kbytes | 100 MHz | -40 to +85°C |
| | R5F5631ECDLK | PTLG0145KA-A | 2 Mbytes | 128 Kbytes | 32 Kbytes | 100 MHz | -40 to +85°C |
| | R5F5631EDDLK | PTLG0145KA-A | 2 Mbytes | 128 Kbytes | 32 Kbytes | 100 MHz | -40 to +85°C |
| | R5F5631DCDLK | PTLG0145KA-A | 1.5 Mbytes | 128 Kbytes | 32 Kbytes | 100 MHz | -40 to +85°C |
| | R5F5631DDDLK | PTLG0145KA-A | 1.5 Mbytes | 128 Kbytes | 32 Kbytes | 100 MHz | -40 to +85°C |
| | R5F5631BCDLK | PTLG0145KA-A | 1 Mbyte | 128 Kbytes | 32 Kbytes | 100 MHz | -40 to +85°C |
| | R5F5631BDDLK | PTLG0145KA-A | 1 Mbyte | 128 Kbytes | 32 Kbytes | 100 MHz | -40 to +85°C |
| | R5F5631ACDLK | PTLG0145KA-A | 768 Kbytes | 128 Kbytes | 32 Kbytes | 100 MHz | -40 to +85°C |
| | R5F5631ADDLK | PTLG0145KA-A | 768 Kbytes | 128 Kbytes | 32 Kbytes | 100 MHz | -40 to +85°C |
| | R5F56318CDLK | PTLG0145KA-A | 512 Kbytes | 128 Kbytes | 32 Kbytes | 100 MHz | -40 to +85°C |
| | R5F56318DDLK | PTLG0145KA-A | 512 Kbytes | 128 Kbytes | 32 Kbytes | 100 MHz | -40 to +85°C |
| | R5F56317CDLK | PTLG0145KA-A | 384 Kbytes | 128 Kbytes | 32 Kbytes | 100 MHz | -40 to +85°C |
| | R5F56317DDLK | PTLG0145KA-A | 384 Kbytes | 128 Kbytes | 32 Kbytes | 100 MHz | -40 to +85°C |
| | R5F56316CDLK | PTLG0145KA-A | 256 Kbytes | 128 Kbytes | 32 Kbytes | 100 MHz | -40 to +85°C |
| | R5F56316DDLK | PTLG0145KA-A | 256 Kbytes | 128 Kbytes | 32 Kbytes | 100 MHz | -40 to +85°C |
| | R5F5631FHDFB | PLQP0144KA-A | 2 Mbytes | 256 Kbytes | 32 Kbytes | 100 MHz | -40 to +85°C |
| | R5F5631FDDFB | PLQP0144KA-A | 2 Mbytes | 256 Kbytes | 32 Kbytes | 100 MHz | -40 to +85°C |
| | R5F5631KHDFB | PLQP0144KA-A*1 | 2 Mbytes | 192 Kbytes | 32 Kbytes | 100 MHz | -40 to +85°C |
| | R5F5631KDDFB | PLQP0144KA-A | 2 Mbytes | 192 Kbytes | 32 Kbytes | 100 MHz | -40 to +85°C |
| | R5F5631ECDFB | PLQP0144KA-A | 2 Mbytes | 128 Kbytes | 32 Kbytes | 100 MHz | -40 to +85°C |
| | R5F5631EDDFB | PLQP0144KA-A | 2 Mbytes | 128 Kbytes | 32 Kbytes | 100 MHz | -40 to +85°C |
| | R5F5631JHDFB | PLQP0144KA-A*1 | 1.5 Mbytes | 256 Kbytes | 32 Kbytes | 100 MHz | -40 to +85°C |
| | R5F5631JDDFB | PLQP0144KA-A | 1.5 Mbytes | 256 Kbytes | 32 Kbytes | 100 MHz | -40 to +85°C |
| | R5F5631GHDFB | PLQP0144KA-A*1 | 1.5 Mbytes | 192 Kbytes | 32 Kbytes | 100 MHz | -40 to +85°C |
| | R5F5631GDDFB | PLQP0144KA-A | 1.5 Mbytes | 192 Kbytes | 32 Kbytes | 100 MHz | -40 to +85°C |
| | R5F5631DCDFB | PLQP0144KA-A | 1.5 Mbytes | 128 Kbytes | 32 Kbytes | 100 MHz | -40 to +85°C |
| | R5F5631DDDFB | PLQP0144KA-A | 1.5 Mbytes | 128 Kbytes | 32 Kbytes | 100 MHz | -40 to +85°C |
| | R5F5631YHDFB | PLQP0144KA-A | 1 Mbyte | 256 Kbytes | 32 Kbytes | 100 MHz | -40 to +85°C |
| | R5F5631YDDFB | PLQP0144KA-A | 1 Mbyte | 256 Kbytes | 32 Kbytes | 100 MHz | -40 to +85°C |
| | R5F5631WHDFB | PLQP0144KA-A | 1 Mbyte | 192 Kbytes | 32 Kbytes | 100 MHz | -40 to +85°C |
| | R5F5631WDDFB | PLQP0144KA-A | 1 Mbyte | 192 Kbytes | 32 Kbytes | 100 MHz | -40 to +85°C |
| | R5F5631BCDFB | PLQP0144KA-A | 1 Mbyte | 128 Kbytes | 32 Kbytes | 100 MHz | -40 to +85°C |
| | R5F5631BDDFB | PLQP0144KA-A | 1 Mbyte | 128 Kbytes | 32 Kbytes | 100 MHz | -40 to +85°C |
| | R5F5631ACDFB | PLQP0144KA-A | 768 Kbytes | 128 Kbytes | 32 Kbytes | 100 MHz | -40 to +85°C |
| R5F5631ADDFB | PLQP0144KA-A | 768 Kbytes | 128 Kbytes | 32 Kbytes | 100 MHz | -40 to +85°C | |
| R5F56318CDFB | PLQP0144KA-A | 512 Kbytes | 128 Kbytes | 32 Kbytes | 100 MHz | -40 to +85°C | |
| R5F56318DDFB | PLQP0144KA-A | 512 Kbytes | 128 Kbytes | 32 Kbytes | 100 MHz | -40 to +85°C | |
| R5F56316CDFB | PLQP0144KA-A | 256 Kbytes | 128 Kbytes | 32 Kbytes | 100 MHz | -40 to +85°C | |
| R5F56316DDFB | PLQP0144KA-A | 256 Kbytes | 128 Kbytes | 32 Kbytes | 100 MHz | -40 to +85°C | |

Table 1.3 List of Products (6/8)

| Group | Part No. | Package | ROM Capacity | RAM Capacity | E2 Data Flash | Operating Frequency (Max.) | Operating Temp. Range |
|----------------------|--------------|----------------|--------------|--------------|---------------|----------------------------|-----------------------|
| RX631 (D version) | R5F56317CDFB | PLQP0144KA-A | 384 Kbytes | 128 Kbytes | 32 Kbytes | 100 MHz | -40 to +85°C |
| | R5F56317DDFB | PLQP0144KA-A | 384 Kbytes | 128 Kbytes | 32 Kbytes | 100 MHz | -40 to +85°C |
| | R5F5631ECDLJ | PTLG0100JA-A | 2 Mbytes | 128 Kbytes | 32 Kbytes | 100 MHz | -40 to +85°C |
| | R5F5631EDDLJ | PTLG0100JA-A | 2 Mbytes | 128 Kbytes | 32 Kbytes | 100 MHz | -40 to +85°C |
| | R5F5631DCDLJ | PTLG0100JA-A | 1.5 Mbytes | 128 Kbytes | 32 Kbytes | 100 MHz | -40 to +85°C |
| | R5F5631DDDLJ | PTLG0100JA-A | 1.5 Mbytes | 128 Kbytes | 32 Kbytes | 100 MHz | -40 to +85°C |
| | R5F5631BCDLJ | PTLG0100JA-A | 1 Mbyte | 128 Kbytes | 32 Kbytes | 100 MHz | -40 to +85°C |
| | R5F5631BDDLJ | PTLG0100JA-A | 1 Mbyte | 128 Kbytes | 32 Kbytes | 100 MHz | -40 to +85°C |
| | R5F5631ACDLJ | PTLG0100JA-A | 768 Kbytes | 128 Kbytes | 32 Kbytes | 100 MHz | -40 to +85°C |
| | R5F5631ADDLJ | PTLG0100JA-A | 768 Kbytes | 128 Kbytes | 32 Kbytes | 100 MHz | -40 to +85°C |
| | R5F56318CDLJ | PTLG0100JA-A | 512 Kbytes | 128 Kbytes | 32 Kbytes | 100 MHz | -40 to +85°C |
| | R5F56318DDLJ | PTLG0100JA-A | 512 Kbytes | 128 Kbytes | 32 Kbytes | 100 MHz | -40 to +85°C |
| | R5F56317CDLJ | PTLG0100JA-A | 384 Kbytes | 128 Kbytes | 32 Kbytes | 100 MHz | -40 to +85°C |
| | R5F56317DDLJ | PTLG0100JA-A | 384 Kbytes | 128 Kbytes | 32 Kbytes | 100 MHz | -40 to +85°C |
| | R5F56316CDLJ | PTLG0100JA-A | 256 Kbytes | 128 Kbytes | 32 Kbytes | 100 MHz | -40 to +85°C |
| | R5F56316DDLJ | PTLG0100JA-A | 256 Kbytes | 128 Kbytes | 32 Kbytes | 100 MHz | -40 to +85°C |
| | R5F5631FHDFP | PLQP0100KB-A | 2 Mbytes | 256 Kbytes | 32 Kbytes | 100 MHz | -40 to +85°C |
| | R5F5631FDDFP | PLQP0100KB-A | 2 Mbytes | 256 Kbytes | 32 Kbytes | 100 MHz | -40 to +85°C |
| | R5F5631KHDFP | PLQP0100KB-A*1 | 2 Mbytes | 192 Kbytes | 32 Kbytes | 100 MHz | -40 to +85°C |
| | R5F5631KDDFP | PLQP0100KB-A | 2 Mbytes | 192 Kbytes | 32 Kbytes | 100 MHz | -40 to +85°C |
| | R5F5631ECDFP | PLQP0100KB-A | 2 Mbytes | 128 Kbytes | 32 Kbytes | 100 MHz | -40 to +85°C |
| | R5F5631EDDFP | PLQP0100KB-A | 2 Mbytes | 128 Kbytes | 32 Kbytes | 100 MHz | -40 to +85°C |
| | R5F5631JHDFP | PLQP0100KB-A*1 | 1.5 Mbytes | 256 Kbytes | 32 Kbytes | 100 MHz | -40 to +85°C |
| | R5F5631JDDFP | PLQP0100KB-A | 1.5 Mbytes | 256 Kbytes | 32 Kbytes | 100 MHz | -40 to +85°C |
| | R5F5631GHDFP | PLQP0100KB-A*1 | 1.5 Mbytes | 192 Kbytes | 32 Kbytes | 100 MHz | -40 to +85°C |
| | R5F5631GDDFP | PLQP0100KB-A | 1.5 Mbytes | 192 Kbytes | 32 Kbytes | 100 MHz | -40 to +85°C |
| | R5F5631DCDFP | PLQP0100KB-A | 1.5 Mbytes | 128 Kbytes | 32 Kbytes | 100 MHz | -40 to +85°C |
| | R5F5631DDDFP | PLQP0100KB-A | 1.5 Mbytes | 128 Kbytes | 32 Kbytes | 100 MHz | -40 to +85°C |
| | R5F5631YHDFP | PLQP0100KB-A | 1 Mbyte | 256 Kbytes | 32 Kbytes | 100 MHz | -40 to +85°C |
| | R5F5631YDDFP | PLQP0100KB-A | 1 Mbyte | 256 Kbytes | 32 Kbytes | 100 MHz | -40 to +85°C |
| | R5F5631WHDFP | PLQP0100KB-A | 1 Mbyte | 192 Kbytes | 32 Kbytes | 100 MHz | -40 to +85°C |
| | R5F5631WDDFP | PLQP0100KB-A | 1 Mbyte | 192 Kbytes | 32 Kbytes | 100 MHz | -40 to +85°C |
| | R5F5631BCDFP | PLQP0100KB-A | 1 Mbyte | 128 Kbytes | 32 Kbytes | 100 MHz | -40 to +85°C |
| | R5F5631BDDFP | PLQP0100KB-A | 1 Mbyte | 128 Kbytes | 32 Kbytes | 100 MHz | -40 to +85°C |
| | R5F5631ACDFP | PLQP0100KB-A | 768 Kbytes | 128 Kbytes | 32 Kbytes | 100 MHz | -40 to +85°C |
| | R5F5631ADDFP | PLQP0100KB-A | 768 Kbytes | 128 Kbytes | 32 Kbytes | 100 MHz | -40 to +85°C |
| | R5F56318CDFP | PLQP0100KB-A | 512 Kbytes | 128 Kbytes | 32 Kbytes | 100 MHz | -40 to +85°C |
| | R5F56318DDFP | PLQP0100KB-A | 512 Kbytes | 128 Kbytes | 32 Kbytes | 100 MHz | -40 to +85°C |
| | R5F56317CDFP | PLQP0100KB-A | 384 Kbytes | 128 Kbytes | 32 Kbytes | 100 MHz | -40 to +85°C |
| | R5F56317DDFP | PLQP0100KB-A | 384 Kbytes | 128 Kbytes | 32 Kbytes | 100 MHz | -40 to +85°C |
| R5F56316CDFP | PLQP0100KB-A | 256 Kbytes | 128 Kbytes | 32 Kbytes | 100 MHz | -40 to +85°C | |
| R5F56316DDFP | PLQP0100KB-A | 256 Kbytes | 128 Kbytes | 32 Kbytes | 100 MHz | -40 to +85°C | |
| R5F5631PCDFM | PLQP0064KB-A | 512 Kbytes | 64 Kbytes | 32 Kbytes | 100 MHz | -40 to +85°C | |
| R5F5631PDDFM | PLQP0064KB-A | 512 Kbytes | 64 Kbytes | 32 Kbytes | 100 MHz | -40 to +85°C | |
| R5F5631NCDFM | PLQP0064KB-A | 384 Kbytes | 64 Kbytes | 32 Kbytes | 100 MHz | -40 to +85°C | |

Table 1.3 List of Products (7/8)

| Group | Part No. | Package | ROM Capacity | RAM Capacity | E2 Data Flash | Operating Frequency (Max.) | Operating Temp. Range |
|----------------------------|--------------|----------------|--------------|--------------|---------------|----------------------------|-----------------------|
| RX631 (D version) | R5F5631NDDFM | PLQP0064KB-A | 384 Kbytes | 64 Kbytes | 32 Kbytes | 100 MHz | -40 to +85°C |
| | R5F5631MCDFM | PLQP0064KB-A | 256 Kbytes | 64 Kbytes | 32 Kbytes | 100 MHz | -40 to +85°C |
| | R5F5631MDDFM | PLQP0064KB-A | 256 Kbytes | 64 Kbytes | 32 Kbytes | 100 MHz | -40 to +85°C |
| | R5F5631PCDFL | PLQP0048KB-A | 512 Kbytes | 64 Kbytes | 32 Kbytes | 100 MHz | -40 to +85°C |
| | R5F5631PDDFL | PLQP0048KB-A | 512 Kbytes | 64 Kbytes | 32 Kbytes | 100 MHz | -40 to +85°C |
| | R5F5631NCDL | PLQP0048KB-A | 384 Kbytes | 64 Kbytes | 32 Kbytes | 100 MHz | -40 to +85°C |
| | R5F5631NDDL | PLQP0048KB-A | 384 Kbytes | 64 Kbytes | 32 Kbytes | 100 MHz | -40 to +85°C |
| | R5F5631MCDL | PLQP0048KB-A | 256 Kbytes | 64 Kbytes | 32 Kbytes | 100 MHz | -40 to +85°C |
| | R5F5631MDDL | PLQP0048KB-A | 256 Kbytes | 64 Kbytes | 32 Kbytes | 100 MHz | -40 to +85°C |
| | R5F56318SDLC | PTLG0177KA-A | 512 Kbytes | 128 Kbytes | 32 Kbytes | 100 MHz | -40 to +85°C |
| | R5F56317SDLC | PTLG0177KA-A | 384 Kbytes | 128 Kbytes | 32 Kbytes | 100 MHz | -40 to +85°C |
| | R5F56316SDLC | PTLG0177KA-A | 256 Kbytes | 128 Kbytes | 32 Kbytes | 100 MHz | -40 to +85°C |
| | R5F56318SDBG | PLBG0176GA-A*1 | 512 Kbytes | 128 Kbytes | 32 Kbytes | 100 MHz | -40 to +85°C |
| | R5F56317SDBG | PLBG0176GA-A*1 | 384 Kbytes | 128 Kbytes | 32 Kbytes | 100 MHz | -40 to +85°C |
| | R5F56316SDBG | PLBG0176GA-A*1 | 256 Kbytes | 128 Kbytes | 32 Kbytes | 100 MHz | -40 to +85°C |
| | R5F56318SDFC | PLQP0176KB-A*1 | 512 Kbytes | 128 Kbytes | 32 Kbytes | 100 MHz | -40 to +85°C |
| | R5F56317SDFC | PLQP0176KB-A*1 | 384 Kbytes | 128 Kbytes | 32 Kbytes | 100 MHz | -40 to +85°C |
| | R5F56316SDFC | PLQP0176KB-A*1 | 256 Kbytes | 128 Kbytes | 32 Kbytes | 100 MHz | -40 to +85°C |
| | R5F56318SDLK | PTLG0145KA-A | 512 Kbytes | 128 Kbytes | 32 Kbytes | 100 MHz | -40 to +85°C |
| | R5F56317SDLK | PTLG0145KA-A | 384 Kbytes | 128 Kbytes | 32 Kbytes | 100 MHz | -40 to +85°C |
| | R5F56316SDLK | PTLG0145KA-A | 256 Kbytes | 128 Kbytes | 32 Kbytes | 100 MHz | -40 to +85°C |
| | R5F56318SDFB | PLQP144KA-A*1 | 512 Kbytes | 128 Kbytes | 32 Kbytes | 100 MHz | -40 to +85°C |
| | R5F56317SDFB | PLQP144KA-A*1 | 384 Kbytes | 128 Kbytes | 32 Kbytes | 100 MHz | -40 to +85°C |
| | R5F56316SDFB | PLQP144KA-A*1 | 256 Kbytes | 128 Kbytes | 32 Kbytes | 100 MHz | -40 to +85°C |
| | R5F5631PFDLH | PTLG0064JA-A | 512 Kbytes | 64 Kbytes | 32 Kbytes | 100 MHz | -40 to +85°C |
| | R5F5631MFDLH | PTLG0064JA-A*1 | 256 Kbytes | 64 Kbytes | 32 Kbytes | 100 MHz | -40 to +85°C |
| | R5S56310CDFC | PLQP0176KB-A | 0 bytes | 128 Kbytes | 0 bytes | 100 MHz | -40 to +85°C |
| RX631 (G version) *2 | R5F5631FDGFC | PLQP0176KB-A | 2 Mbytes | 256 Kbytes | 32 Kbytes | 100 MHz | -40 to +105°C |
| | R5F5631KDGFC | PLQP0176KB-A | 2 Mbytes | 192 Kbytes | 32 Kbytes | 100 MHz | -40 to +105°C |
| | R5F5631EDGFC | PLQP0176KB-A | 2 Mbytes | 128 Kbytes | 32 Kbytes | 100 MHz | -40 to +105°C |
| | R5F5631DDGFC | PLQP0176KB-A | 1.5 Mbytes | 128 Kbytes | 32 Kbytes | 100 MHz | -40 to +105°C |
| | R5F5631YDGFC | PLQP0176KB-A | 1 Mbyte | 256 Kbytes | 32 Kbytes | 100 MHz | -40 to +105°C |
| | R5F5631WDGFC | PLQP0176KB-A | 1 Mbyte | 192 Kbytes | 32 Kbytes | 100 MHz | -40 to +105°C |
| | R5F5631BDGFC | PLQP0176KB-A | 1 Mbyte | 128 Kbytes | 32 Kbytes | 100 MHz | -40 to +105°C |
| | R5F5631ADGFC | PLQP0176KB-A | 768 Kbytes | 128 Kbytes | 32 Kbytes | 100 MHz | -40 to +105°C |
| | R5F56318SGFC | PLQP0176KB-A | 512 Kbytes | 128 Kbytes | 32 Kbytes | 100 MHz | -40 to +105°C |
| | R5F56318DGFC | PLQP0176KB-A | 512 Kbytes | 128 Kbytes | 32 Kbytes | 100 MHz | -40 to +105°C |
| | R5F56317SGFC | PLQP0176KB-A | 384 Kbytes | 128 Kbytes | 32 Kbytes | 100 MHz | -40 to +105°C |
| | R5F56317DGFC | PLQP0176KB-A | 384 Kbytes | 128 Kbytes | 32 Kbytes | 100 MHz | -40 to +105°C |
| | R5F56316SGFC | PLQP0176KB-A | 256 Kbytes | 128 Kbytes | 32 Kbytes | 100 MHz | -40 to +105°C |
| | R5F56316DGFC | PLQP0176KB-A | 256 Kbytes | 128 Kbytes | 32 Kbytes | 100 MHz | -40 to +105°C |
| | R5F5631FDGFB | PLQP0144KA-A | 2 Mbytes | 256 Kbytes | 32 Kbytes | 100 MHz | -40 to +105°C |
| | R5F5631KDGFB | PLQP0144KA-A | 2 Mbytes | 192 Kbytes | 32 Kbytes | 100 MHz | -40 to +105°C |
| | R5F5631EDGFB | PLQP0144KA-A | 2 Mbytes | 128 Kbytes | 32 Kbytes | 100 MHz | -40 to +105°C |
| | R5F5631JDGFB | PLQP0144KA-A | 1.5 Mbytes | 256 Kbytes | 32 Kbytes | 100 MHz | -40 to +105°C |

Table 1.3 List of Products (8/8)

| Group | Part No. | Package | ROM Capacity | RAM Capacity | E2 Data Flash | Operating Frequency (Max.) | Operating Temp. Range |
|----------------------------|--------------|--------------|--------------|--------------|---------------|----------------------------|-----------------------|
| RX631 (G version) *2 | R5F5631GDGFB | PLQP0144KA-A | 1.5 Mbytes | 192 Kbytes | 32 Kbytes | 100 MHz | -40 to +105°C |
| | R5F5631DDGFB | PLQP0144KA-A | 1.5 Mbytes | 128 Kbytes | 32 Kbytes | 100 MHz | -40 to +105°C |
| | R5F5631YDGFB | PLQP0144KA-A | 1 Mbyte | 256 Kbytes | 32 Kbytes | 100 MHz | -40 to +105°C |
| | R5F5631WDGFB | PLQP0144KA-A | 1 Mbyte | 192 Kbytes | 32 Kbytes | 100 MHz | -40 to +105°C |
| | R5F5631BDGFB | PLQP0144KA-A | 1 Mbyte | 128 Kbytes | 32 Kbytes | 100 MHz | -40 to +105°C |
| | R5F5631ADGFB | PLQP0144KA-A | 768 Kbytes | 128 Kbytes | 32 Kbytes | 100 MHz | -40 to +105°C |
| | R5F56318SGFB | PLQP0144KA-A | 512 Kbytes | 128 Kbytes | 32 Kbytes | 100 MHz | -40 to +105°C |
| | R5F56318DGFB | PLQP0144KA-A | 512 Kbytes | 128 Kbytes | 32 Kbytes | 100 MHz | -40 to +105°C |
| | R5F56317SGFB | PLQP0144KA-A | 384 Kbytes | 128 Kbytes | 32 Kbytes | 100 MHz | -40 to +105°C |
| | R5F56317DGFB | PLQP0144KA-A | 384 Kbytes | 128 Kbytes | 32 Kbytes | 100 MHz | -40 to +105°C |
| | R5F56316SGFB | PLQP0144KA-A | 256 Kbytes | 128 Kbytes | 32 Kbytes | 100 MHz | -40 to +105°C |
| | R5F56316DGFB | PLQP0144KA-A | 256 Kbytes | 128 Kbytes | 32 Kbytes | 100 MHz | -40 to +105°C |
| | R5F5631FDGFP | PLQP0100KB-A | 2 Mbytes | 256 Kbytes | 32 Kbytes | 100 MHz | -40 to +105°C |
| | R5F5631KDGFP | PLQP0100KB-A | 2 Mbytes | 192 Kbytes | 32 Kbytes | 100 MHz | -40 to +105°C |
| | R5F5631EDGFP | PLQP0100KB-A | 2 Mbytes | 128 Kbytes | 32 Kbytes | 100 MHz | -40 to +105°C |
| | R5F5631JDGFP | PLQP0100KB-A | 1.5 Mbytes | 256 Kbytes | 32 Kbytes | 100 MHz | -40 to +105°C |
| | R5F5631GDGFP | PLQP0100KB-A | 1.5 Mbytes | 192 Kbytes | 32 Kbytes | 100 MHz | -40 to +105°C |
| | R5F5631DDGFP | PLQP0100KB-A | 1.5 Mbytes | 128 Kbytes | 32 Kbytes | 100 MHz | -40 to +105°C |
| | R5F5631YDGFP | PLQP0100KB-A | 1 Mbyte | 256 Kbytes | 32 Kbytes | 100 MHz | -40 to +105°C |
| | R5F5631WDGFP | PLQP0100KB-A | 1 Mbyte | 192 Kbytes | 32 Kbytes | 100 MHz | -40 to +105°C |
| | R5F5631BDGFP | PLQP0100KB-A | 1 Mbyte | 128 Kbytes | 32 Kbytes | 100 MHz | -40 to +105°C |
| | R5F5631ADGFP | PLQP0100KB-A | 768 Kbytes | 128 Kbytes | 32 Kbytes | 100 MHz | -40 to +105°C |
| | R5F56318DGFP | PLQP0100KB-A | 512 Kbytes | 128 Kbytes | 32 Kbytes | 100 MHz | -40 to +105°C |
| | R5F56317DGFP | PLQP0100KB-A | 384 Kbytes | 128 Kbytes | 32 Kbytes | 100 MHz | -40 to +105°C |
| | R5F56316DGFP | PLQP0100KB-A | 256 Kbytes | 128 Kbytes | 32 Kbytes | 100 MHz | -40 to +105°C |
| | R5F5631PDGFM | PLQP0064KB-A | 512 Kbytes | 64 Kbytes | 32 Kbytes | 100 MHz | -40 to +105°C |
| | R5F5631NDGFM | PLQP0064KB-A | 384 Kbytes | 64 Kbytes | 32 Kbytes | 100 MHz | -40 to +105°C |
| | R5F5631MDGFM | PLQP0064KB-A | 256 Kbytes | 64 Kbytes | 32 Kbytes | 100 MHz | -40 to +105°C |
| | R5F5631PDGFL | PLQP0048KB-A | 512 Kbytes | 64 Kbytes | 32 Kbytes | 100 MHz | -40 to +105°C |
| | R5F5631NDGFL | PLQP0048KB-A | 384 Kbytes | 64 Kbytes | 32 Kbytes | 100 MHz | -40 to +105°C |
| | R5F5631MDGFL | PLQP0048KB-A | 256 Kbytes | 64 Kbytes | 32 Kbytes | 100 MHz | -40 to +105°C |

Note 1. In the planning stage

Note 2. The specifications of the temperature sensor calibration and unique ID for G-version products differ from those for other products. For details, see section 45.2.2, Temperature Sensor Calibration Data Registers (TSCDRH, TSCDRL), section 45.3, Using the Temperature Sensor, and section 47.2.22, Unique ID Registers n (UIDRn) (n = 0 to 15) in the User's manual: Hardware.

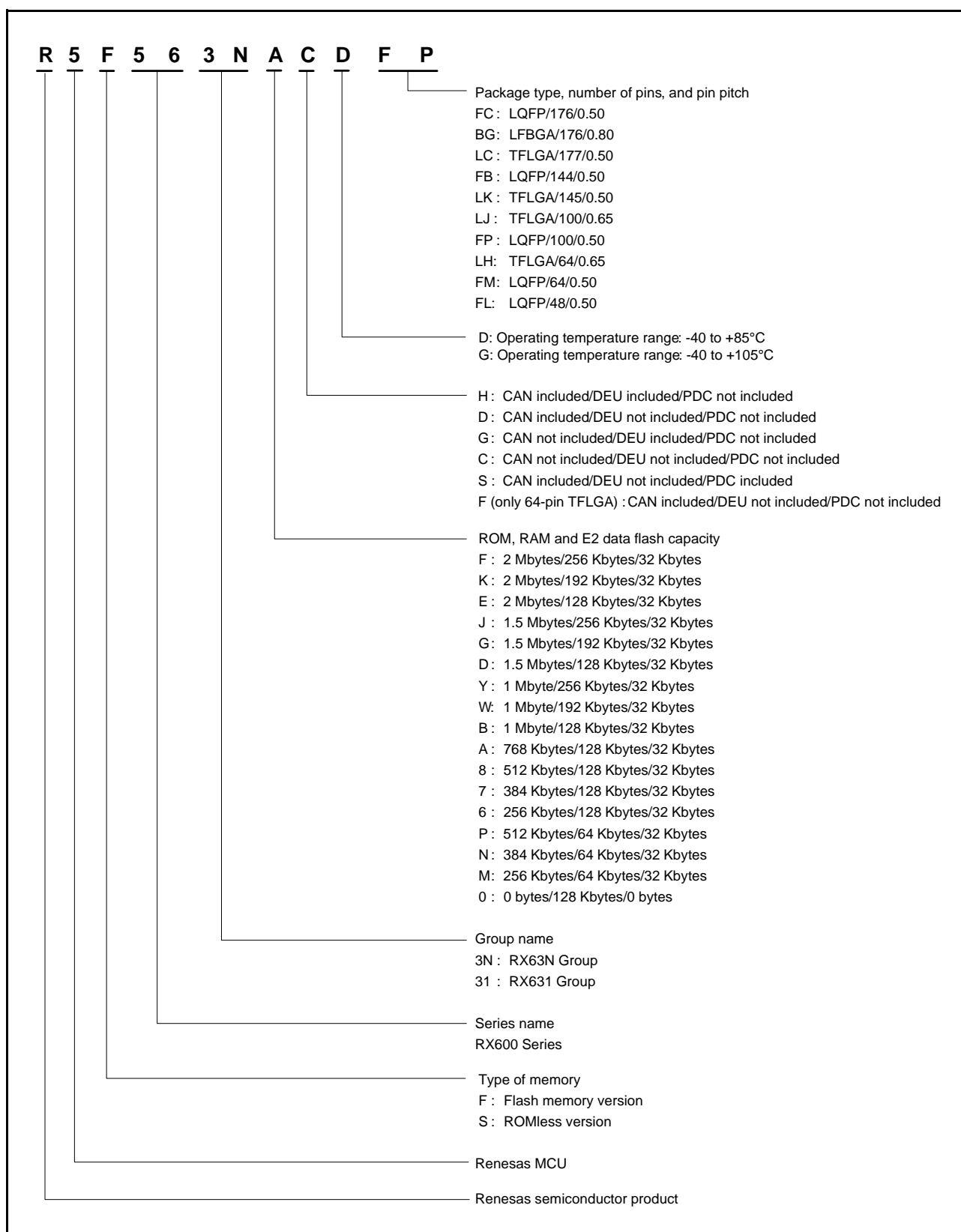


Figure 1.1 How to Read the Product Part No.

1.3 Block Diagram

Figure 1.2 shows a block diagram.

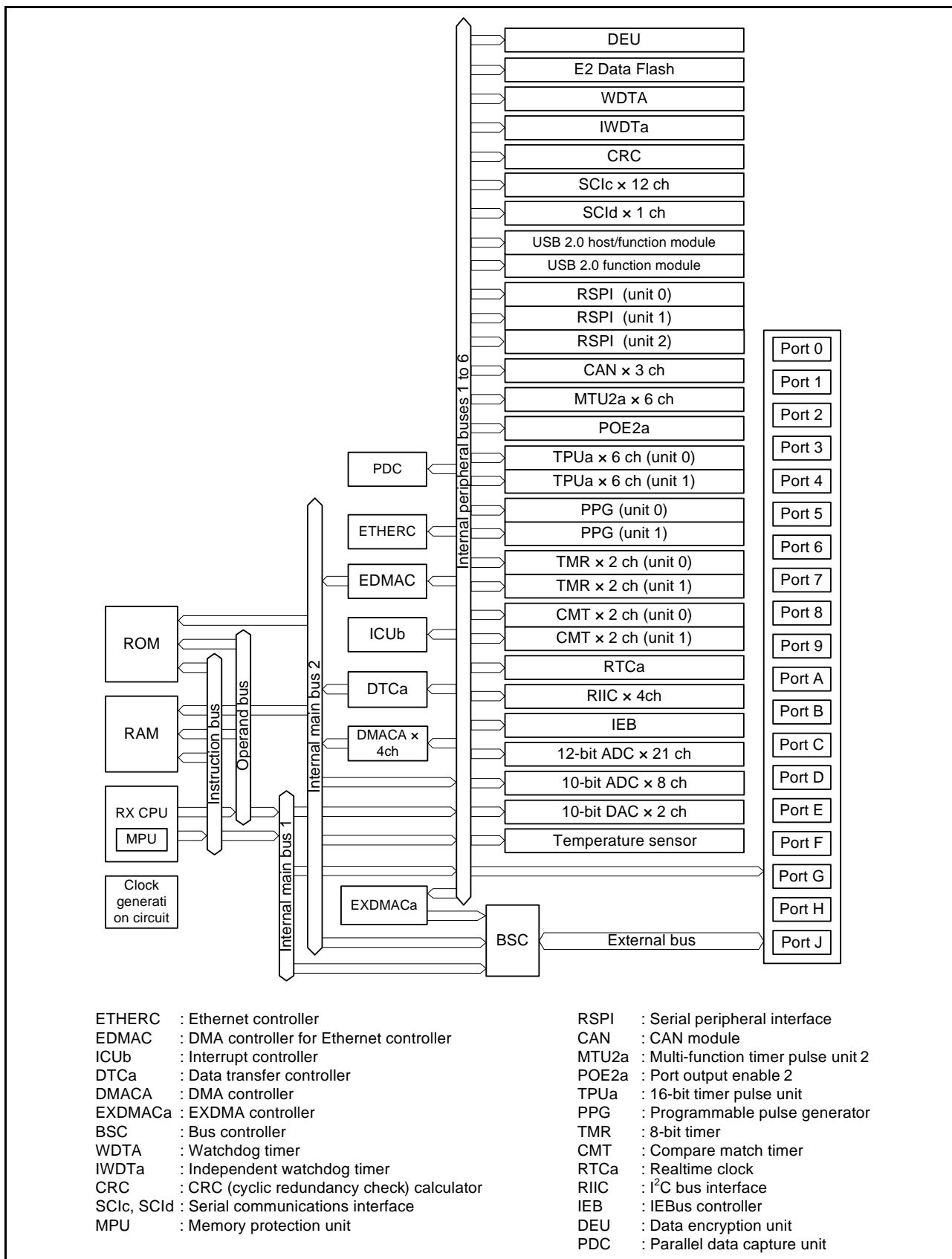


Figure 1.2 Block Diagram

1.4 Pin Functions

Table 1.4 lists the pin functions.

Table 1.4 Pin Functions (1/6)

| Classifications | Pin Name | I/O | Description |
|------------------------|--------------------|--------|---|
| Power supply | VCC | Input | Power supply pin. Connect it to the system power supply. Connect this pin to VSS via a 0.1- μ F capacitor. The capacitor should be placed close to the pin. |
| | VCL | Input | Connect this pin to VSS via a 0.1- μ F capacitor. The capacitor should be placed close to the pin. |
| | VSS | Input | Ground pin. Connect it to the system power supply (0 V). |
| | VBATT | Input | Backup power pin. When the battery backup function is not to be used, connect it to the VCC pin. |
| Clock | XTAL | Output | Pins for a crystal resonator. An external clock signal can be input through the EXTAL pin. |
| | EXTAL | Input | |
| | BCLK | Output | Outputs the external bus clock for external devices. |
| | SDCLK | Output | Outputs the clock dedicated for the SDRAM. |
| | XCOUT | Output | Input/output pins for the subclock oscillator. Connect a crystal resonator between XCOUT and XCIN. |
| | XCIN | Input | |
| Operating mode control | MD | Input | Pins for setting the operating mode. The signal levels on these pins must not be changed during operation. |
| System control | RES# | Input | Reset signal input pin. This LSI enters the reset state when this signal goes low. |
| | EMLE | Input | Input pin for the on-chip emulator enable signal. When the on-chip emulator is used, this pin should be driven high. When not used, it should be driven low. |
| | BSCANP | Input | Boundary scan enable pin. Boundary scan is enabled when this pin goes high. When not used, it should be driven low. |
| On-chip emulator | FINEC | Input | Fine interface clock pin |
| | FINED | I/O | Fine interface pin |
| | TRST# | Input | On-chip emulator or boundary scan pins. When the EMLE pin is driven high, these pins are dedicated for the on-chip emulator. |
| | TMS | Input | |
| | TDI | Input | |
| | TCK | Input | |
| | TDO | Output | |
| | TRCLK | Output | This pin outputs the clock for synchronization with the trace data. |
| | TRSYNC | Output | This pin indicates that output from the TRDATA0 to TRDATA3 pins is valid. |
| | TRDATA0 to TRDATA3 | Output | These pins output the trace information. |
| Address bus | A0 to A23 | Output | Output pins for the address. |
| Data bus | D0 to D31 | I/O | Input and output pins for the bidirectional data bus. |
| Multiplexed bus | A0/D0 to A15/D15 | I/O | Address/data multiplexed bus |

Table 1.4 Pin Functions (2/6)

| Classifications | Pin Name | I/O | Description |
|-----------------------------------|--------------------------------------|-------------------------|--|
| Bus control | RD# | Output | Strobe signal which indicates that reading from the external bus interface space is in progress. |
| | WR# | Output | Strobe signal which indicates that writing to the external bus interface space is in progress, in 1-write strobe mode. |
| | WR0# to WR3# | Output | Strobe signals which indicate that either group of data bus pins (D7 to D0, D15 to D8, D23 to D16, and D31 to D24) is valid in writing to the external bus interface space, in byte strobe mode. |
| | BC0# to BC3# | Output | Strobe signals which indicate that either group of data bus pins (D7 to D0, D15 to D8, D23 to D16, and D31 to D24) is valid in access to the external bus interface space, in 1-write strobe mode. |
| | ALE | Output | Address latch signal when address/data multiplexed bus is selected. |
| | CKE | Output | Output pin for SDRAM clock enable signals. |
| | SDCS# | Output | Output pin for SDRAM chip select signals. |
| | RAS# | Output | Output pin for SDRAM row address strobe signals. |
| | CAS# | Output | Output pin for SDRAM column address strobe signals. |
| | WE# | Output | Output pin for SDRAM write enable signals. |
| | DQM0 to DQM3 | Output | Output pins for SDRAM I/O data mask enable signals. |
| | CS0# to CS7# | Output | Select signals for CS area. |
| | WAIT# | Input | Input pins for wait request signals in access to the external space. |
| | EXDMA controller | EDREQ0, EDREQ1 | |
| EDACK0, EDACK1 | | | Output pins for single address transfer acknowledge signals. |
| Interrupt | NMI | Input | Non-maskable interrupt request signal. |
| | IRQ0 to IRQ15 | Input | Maskable interrupt request signals. |
| Multi-function timer pulse unit 2 | MTIOC0A, MTIOC0B MTIOC0C, MTIOC0D | I/O | The TGRA0 to TGRD0 input capture input/output compare output/PWM output pins. |
| | MTIOC1A, MTIOC1B | I/O | The TGRA1 and TGRB1 input capture input/output compare output/PWM output pins. |
| | MTIOC2A, MTIOC2B | I/O | The TGRA2 and TGRB2 input capture input/output compare output/PWM output pins. |
| | MTIOC3A, MTIOC3B MTIOC3C, MTIOC3D | I/O | The TGRA3 to TGRD3 input capture input/output compare output/PWM output pins. |
| | MTIOC4A, MTIOC4B MTIOC4C, MTIOC4D | I/O | The TGRA4 to TGRD4 input capture input/output compare output/PWM output pins. |
| | MTIC5U, MTIC5V MTIC5W | Input | The TGRU5, TGRV5, and TGRW5 input capture input/dead time compensation input pins. |
| | MTCLKA, MTCLKB MTCLKC, MTCLKD | Input | Input pins for external clock signals. |
| | Port output enable 2 | POE0# to POE3# POE8# | Input |

Table 1.4 Pin Functions (3/6)

| Classifications | Pin Name | I/O | Description |
|--|--|--------|--|
| 16-bit timer pulse unit | TIOCA0, TIOCB0 TIOCC0, TIOCD0 | I/O | The TGRA0 to TGRD0 input capture input/output compare output/PWM output pins. |
| | TIOCA1, TIOCB1 | I/O | The TGRA1 and TGRB1 input capture input/output compare output/PWM output pins. |
| | TIOCA2, TIOCB2 | I/O | The TGRA2 and TGRB2 input capture input/output compare output/PWM output pins. |
| | TIOCA3, TIOCB3 TIOCC3, TIOCD3 | I/O | The TGRA3 to TGRD3 input capture input/output compare output/PWM output pins. |
| | TIOCA4, TIOCB4 | I/O | The TGRA4 and TGRB4 input capture input/output compare output/PWM output pins. |
| | TIOCA5, TIOCB5 | I/O | The TGRA5 and TGRB5 input capture input/output compare output/PWM output pins. |
| | TCLKA, TCLKB TCLKC, TCLKD | Input | Input pins for external clock signals. |
| | TIOCA6, TIOCB6 TIOCC6, TIOCD6 | I/O | The TGRA6 to TGRD6 input capture input/output compare output/PWM output pins. |
| | TIOCA7, TIOCB7 | I/O | The TGRA7 and TGRB7 input capture input/output compare output/PWM output pins. |
| | TIOCA8, TIOCB8 | I/O | The TGRA8 and TGRB8 input capture input/output compare output/PWM output pins. |
| | TIOCA9, TIOCB9 TIOCC9, TIOCD9 | I/O | The TGRA9 to TGRD9 input capture input/output compare output/PWM output pins. |
| | TIOCA10, TIOCB10 | I/O | The TGRA10 and TGRB10 input capture input/output compare output/PWM output pins. |
| | TIOCA11, TIOCB11 | I/O | The TGRA11 and TGRB11 input capture input/output compare output/PWM output pins. |
| | TCLKE, TCLKF TCLKG, TCLKH | Input | Input pins for external clock signals. |
| Programmable pulse generator | PO0 to PO31 | Output | Output pins for the pulse signals. |
| 8-bit timer | TMO0 to TMO3 | Output | Output pins for the compare match signals. |
| | TMCI0 to TMCI3 | Input | Input pins for the external clock signals that drive for the counters. |
| | TMRI0 to TMRI3 | Input | Input pins for the counter-reset signals. |
| Serial communications interface (SC1c) | • Asynchronous mode/clock synchronous mode | | |
| | SCK0 to SCK11 | I/O | Input/output pins for clock signals. |
| | RXD0 to RXD11 | Input | Input pins for data reception. |
| | TXD0 to TXD11 | Output | Output pins for data transmission. |
| | CTS0# to CTS11# | Input | Transmit/receive start control input pins |
| | RTS0# to RTS11# | Output | Transmit/receive start control output pins |
| | • Simple I ² C mode | | |
| | SSCL0 to SSCL11 | I/O | Input/output pins for the I ² C clock |
| | SSDA0 to SSDA11 | I/O | Input/output pins for the I ² C data |
| Serial communications interface (SC1c) | • Simple SPI mode | | |
| | SCK0 to SCK11 | I/O | Input/output pins for the clock |
| | SMISO0 to SMISO11 | I/O | Input/output pins for slave transmit data. |
| | SMOSI0 to SMOSI11 | I/O | Input/output pins for master transmit data. |
| | SS0# to SS11# | Input | Input pins for chip select signals |

Table 1.4 Pin Functions (4/6)

| Classifications | Pin Name | I/O | Description |
|--|--|-------------------------|---|
| Serial communications interface (SCId) | • Asynchronous mode/clock synchronous mode | | |
| | SCK12 | I/O | Input/output pin for clock signals. |
| | RXD12 | Input | Input pin for data reception. |
| | TXD12 | Output | Output pin for data transmission. |
| | CTS12# | Input | Transmit/receive start control input pins |
| | RTS12# | Output | Transmit/receive start control output pins |
| | • Simple I ² C mode | | |
| | SSCL12 | I/O | Input/output pins for the I ² C clock |
| | SSDA12 | I/O | Input/output pins for the I ² C data |
| | • Simple SPI mode | | |
| | SCK12 | I/O | Input/output pins for the clock |
| | SMISO12 | I/O | Input/output pins for slave transmit data. |
| | SMOSI12 | I/O | Input/output pins for master transmit data. |
| | SS12# | Input | Input pins for chip select signals |
| | • Extended serial mode | | |
| | RXDX12 | Input | Input pin for receive data |
| | TXDX12 | Output | Output pin for transmit data |
| | SIOX12 | I/O | Input/output pin for Transmit/receive data |
| | I ² C bus interface | SCL0[FM+], SCL1 to SCL3 | I/O |
| SDA0[FM+], SDA1 to SDA3 | | I/O | Input/output pin for data. Bus can be directly driven by the N-channel open drain output. |
| Ethernet controller | REF50CK | Input | 50-MHz reference clock. This pin inputs reference signals for transmission/reception timings in RMII mode. |
| | RMII_CRS_DV | Input | Indicates that there are carrier detection signals and valid receive data on RMII_RXD1 and RMII_RXD0 in RMII mode. |
| | RMII_TXD0, RMII_TXD1 | Output | 2-bit transmit data in RMII mode. |
| | RMII_RXD0, RMII_RXD1 | Input | 2-bit receive data in RMII mode. |
| | RMII_TXD_EN | Output | Output pin for data transmit enable signals in RMII mode. |
| | RMII_RX_ER | Input | Indicates an error has occurred during reception of data in RMII mode. |
| | ET_CRS | Input | Carrier detection/data reception enable pin. |
| | ET_RX_DV | Input | Indicates that there are valid receive data on ET_ERXD3 to ET_ERXD0. |
| | ET_EXOUT | Output | General-purpose external output pin. |
| | ET_LINKSTA | Input | Inputs link status from the PHY-LSI. |
| | ET_ETXD0 to ET_ETXD3 | Output | 4 bits of MII transmit data. |
| | ET_ERXD0 to ET_ERXD3 | Input | 4 bits of MII receive data. |
| | ET_TX_EN | Output | Transmit enable pin. Indicates that transmit data is ready on ET_ETXD3 to ET_ETXD0. |
| | ET_TX_ER | Output | Transmit error pin. Notifies the PHY_LSI of an error during transmission. |
| | ET_RX_ER | Input | Receive error pin. Recognizes an error during reception. |
| | ET_TX_CLK | Input | Transmit clock pin. This pin inputs reference signals for output timings from ET_TX_EN, ET_ETXD3 to ET_ETXD0, and ET_TX_ER. |
| | ET_RX_CLK | Input | Receive clock pin. This pin inputs reference signals for input timings to ET_RX_DV, ET_ERXD3 to ET_ERXD0, and ET_RX_ER. |
| | ET_COL | Input | Inputs collision detection signals. |
| | ET_WOL | Output | Receives Magic packets. |
| | ET_MDC | Output | Outputs reference clock signals for information transfer via ET_MDIO. |

Table 1.4 Pin Functions (5/6)

| Classifications | Pin Name | I/O | Description |
|----------------------------------|--|--------|---|
| Ethernet controller | ET_MDIO | I/O | Inputs or outputs bidirectional signals for exchange of management information between the RX63N Group and the PHY-LSI. |
| Parallel data capture unit (PDC) | PIXCLK | Input | Parallel data transfer clock |
| | VSYNC | Input | Vertical synchronization signal |
| | HSYNC | Input | Horizontal synchronization signal |
| | PIXD7 to PIXD0 | Input | 8-bit data |
| | PCKO | Output | Outputs parallel data transfer clock signal |
| USB power pins | VCC_USB | Input | Power supply pin. When the USB is not to be used, connect it to the VCC pin. |
| | VSS_USB | Input | Ground pin. When the USB is not to be used, connect it to the VSS pin. |
| USB 2.0 host/function module | USB0_DP, USB1_DP | I/O | Inputs or outputs USB transceiver D+ data. |
| | USB0_DM, USB1_DM | I/O | Inputs or outputs USB transceiver D- data. |
| | USB0_VBUS, USB1_VBUS | Input | Input pins for detection of connection and disconnection of the USB cable. |
| | USB0_EXICEN | Output | Output pin for control the low power of the OTG chip. |
| | USB0_VBUSEN | Output | Supply enable pin of VBUS (5 V) for the OTG chip. |
| | USB0_OVRCURA, USB0_OVRCURB, | Input | Input pin for detection of external over current. |
| | USB0_ID | Input | ID input pin of mini-AB connector at the OTG operation. |
| | USB0_DPUPE, USB1_DPUPE | Output | Pull-up control pins of the D+ signal at the function operation. |
| | USB0_DPRPD | Output | Pull-down control pins of the D+ signal at the host operation. |
| | USB0_DRPD | Output | Pull-down control pins of the D- signal at the host operation. |
| CAN module | CRX0 to CRX2 | Input | Input pin. |
| | CTX0 to CTX2 | Output | Output pin. |
| Serial peripheral interface | RSPCKA, RSPCKB, RSPCKC | I/O | Clock input/output pin. |
| | MOSIA, MOSIB, MOSIC | I/O | Inputs or outputs data output from the master. |
| | MISOA, MISOB, MISOC | I/O | Inputs or outputs data output from the slave. |
| | SSLA0, SSLB0, SSLC0 | I/O | Input or output pins slave selection |
| | SSLA1 to SSLA3, SSLB1 to SSLB3, SSLC1 to SSLC3 | Output | Output pins slave selection |
| | IEBus controller | IERXD | Input |
| IETXD | | Output | Output pin for data transmission. |
| Realtime clock | RTCOUT | Output | Output pin for 1-Hz clock. |
| | RTCIC0 to RTCIC2 | Input | Time capture event input pin |
| 12-bit A/D converter | AN000 to AN020 | Input | Input pins for the analog signals to be processed by the A/D converter. |
| | ADTRG0# | Input | Input pins for the external trigger signals that start the A/D conversion. |
| 10-bit A/D converter | AN0 to AN7 | Input | Input pins for the analog signals to be processed by the A/D converter. |
| | ANEX0 | Output | Extended analog output pin |
| | ANEX1 | Input | Extended analog input pin |
| | ADTRG# | Input | Input pins for the external trigger signals that start the A/D conversion. |
| D/A converter | DA0, DA1 | Output | Output pins for the analog signals to be processed by the D/A converter. |

Table 1.4 Pin Functions (6/6)

| Classifications | Pin Name | I/O | Description |
|---------------------|-----------|----------------------|--|
| Analog power supply | AVCC0 | Input | Analog voltage supply pin for the 12-bit A/D converter. Connect this pin to VCC if the 12-bit A/D converter is not to be used. |
| | AVSS0 | Input | Analog ground pin for the 12-bit A/D converter. Connect this pin to VSS if the 12-bit A/D converter is not to be used. |
| | VREFH0 | Input | Analog reference voltage supply pin for the 12-bit A/D converter. Connect this pin to VCC if the 12-bit A/D converter is not to be used. |
| | VREFL0 | Input | Analog reference ground pin for the 12-bit A/D converter. Connect this pin to VSS if the 12-bit A/D converter is not to be used. |
| | VREFH | Input | Reference voltage input pin for the 10-bit A/D converter and D/A converter. This is used as the analog power supply for the respective modules. Connect this pin to VCC if neither the 10-bit A/D converter nor the D/A converter is in use. |
| | VREFL | Input | Reference ground pin for the 10-bit A/D converter and D/A converter. This is used as the analog ground for the respective modules. Set this pin to the same potential as the VSS pin. |
| | I/O ports | P00 to P03, P05, P07 | I/O |
| P10 to P17 | | I/O | 8-bit input/output pins. |
| P20 to P27 | | I/O | 8-bit input/output pins. |
| P30 to P37 | | I/O | 8-bit input/output pins. (P35 is an input pin) |
| P40 to P47 | | I/O | 8-bit input/output pins. |
| P50 to P57 | | I/O | 8-bit input/output pins. |
| P60 to P67 | | I/O | 8-bit input/output pins. |
| P70 to P77 | | I/O | 8-bit input/output pins. |
| P80 to P87 | | I/O | 8-bit input/output pins. |
| P90 to P97 | | I/O | 8-bit input/output pins. |
| PA0 to PA7 | | I/O | 8-bit input/output pins. |
| PB0 to PB7 | | I/O | 8-bit input/output pins. |
| PC0 to PC7 | | I/O | 8-bit input/output pins. |
| PD0 to PD7 | | I/O | 8-bit input/output pins. |
| PE0 to PE7 | | I/O | 8-bit input/output pins. |
| PF0 to PF5 | | I/O | 6-bit input/output pins. |
| PG0 to PG7 | | I/O | 8-bit input/output pins. |
| PJ3, PJ5 | | I/O | 2-bit input/output pins. |

1.5 Pin Assignments

Figure 1.5 to Figure 1.12 show the pins assignments. Table 1.5 to Table 1.13 show the list of pins and pin functions. Power pins and I/O ports are shown in the pin assignment diagrams.

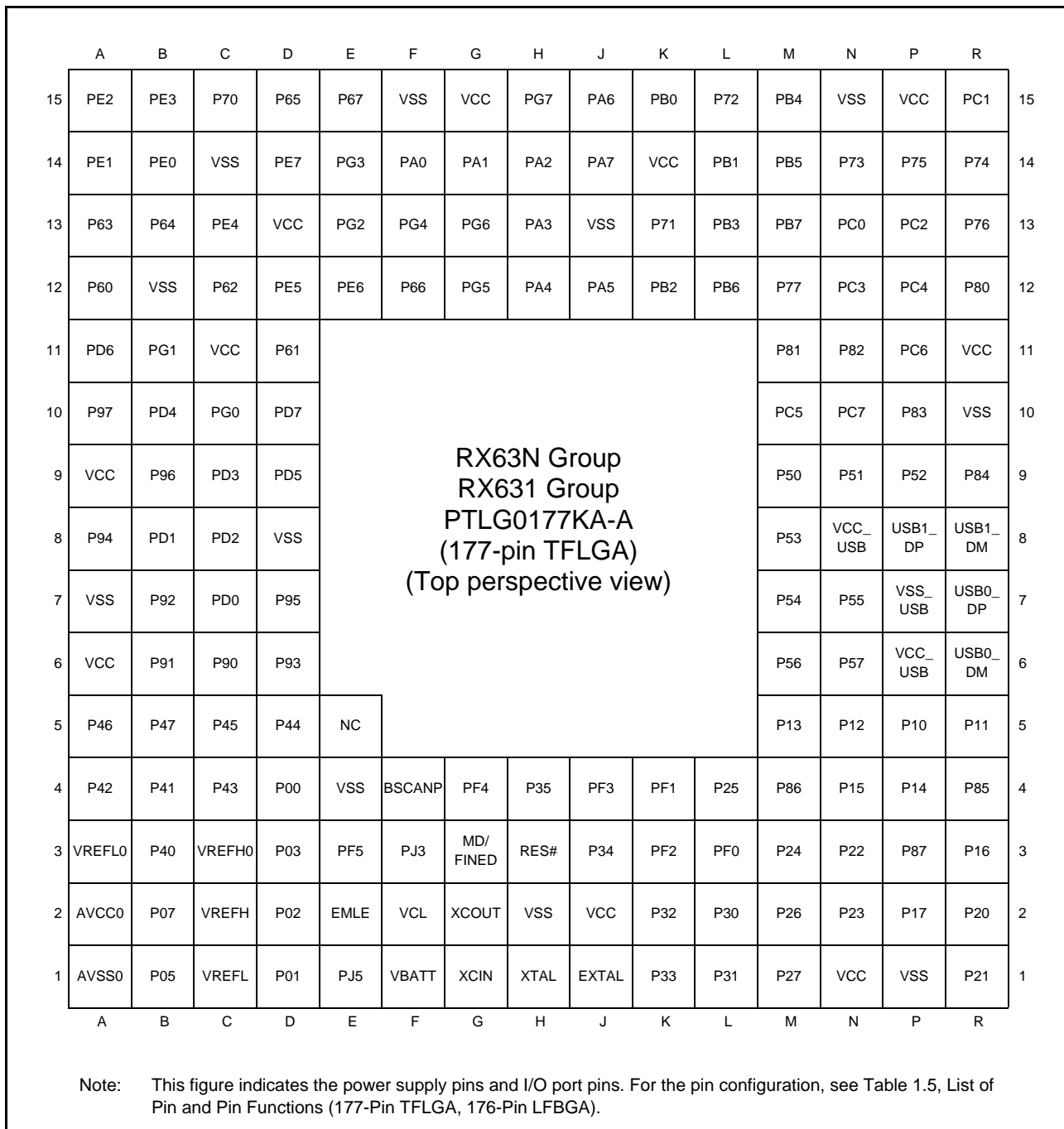


Figure 1.3 Pin Assignment (177-Pin TFLGA)

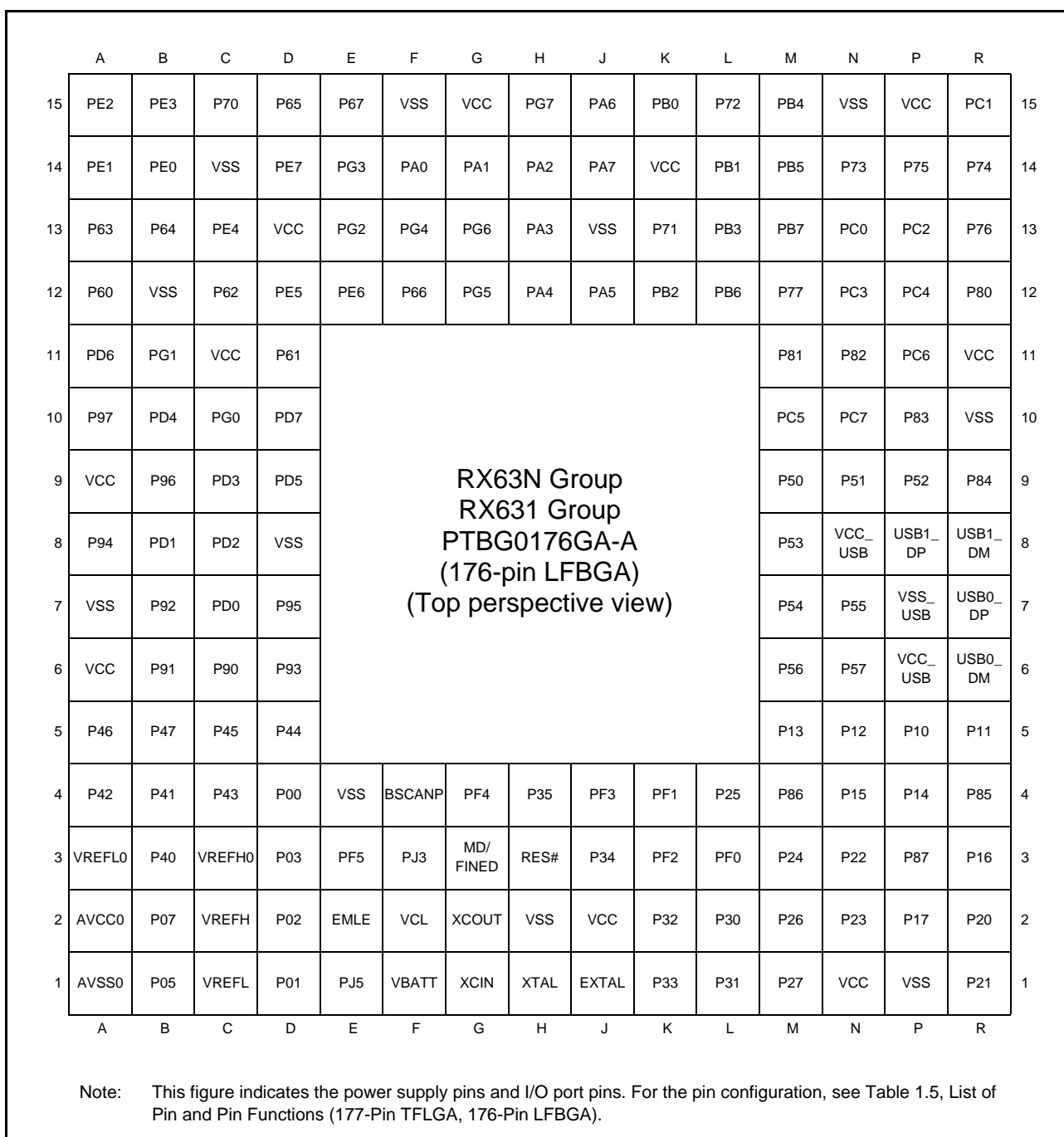


Figure 1.4 Pin Assignment (176-Pin LFBGA)

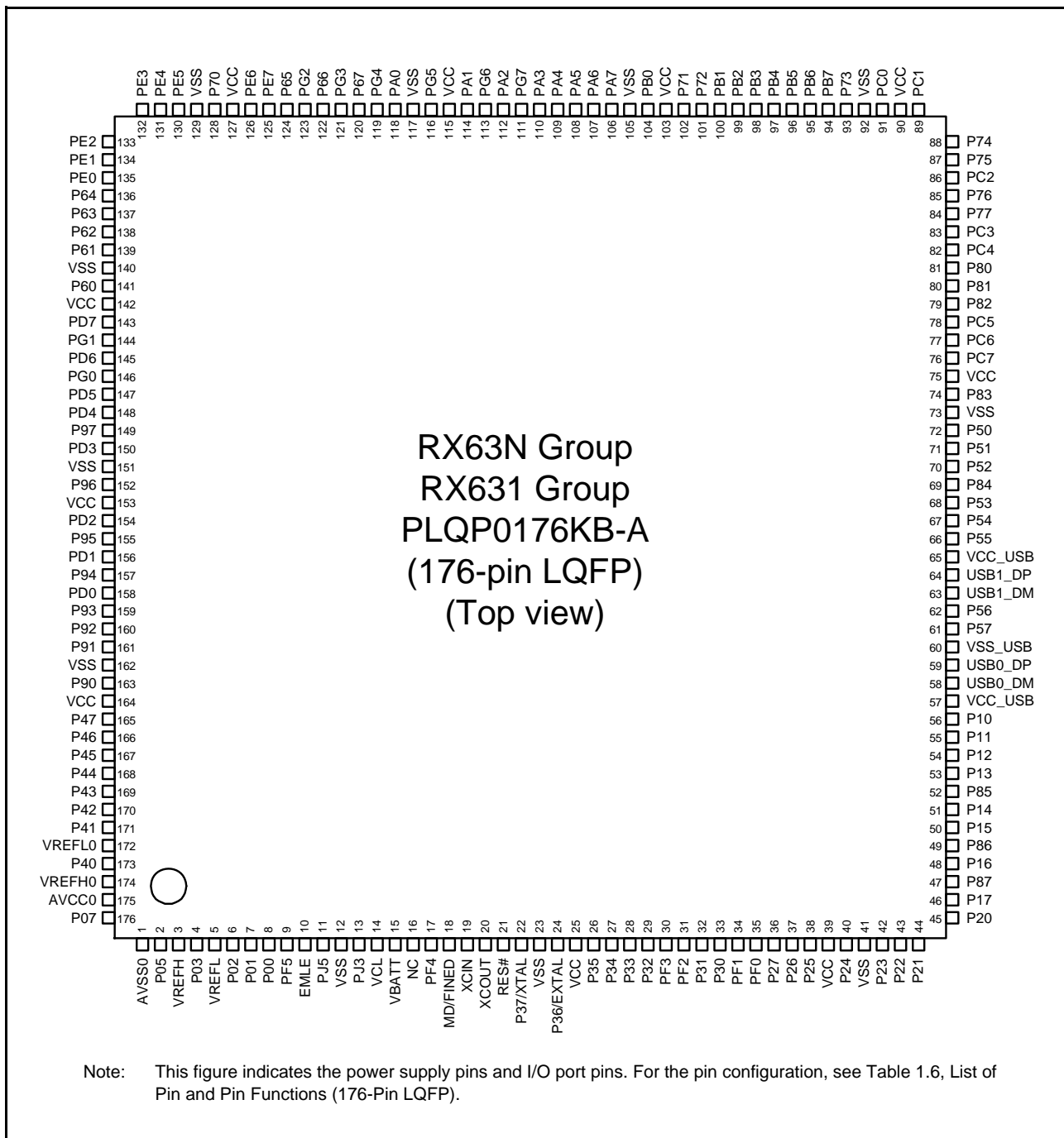


Figure 1.5 Pin Assignment (176-Pin LQFP)

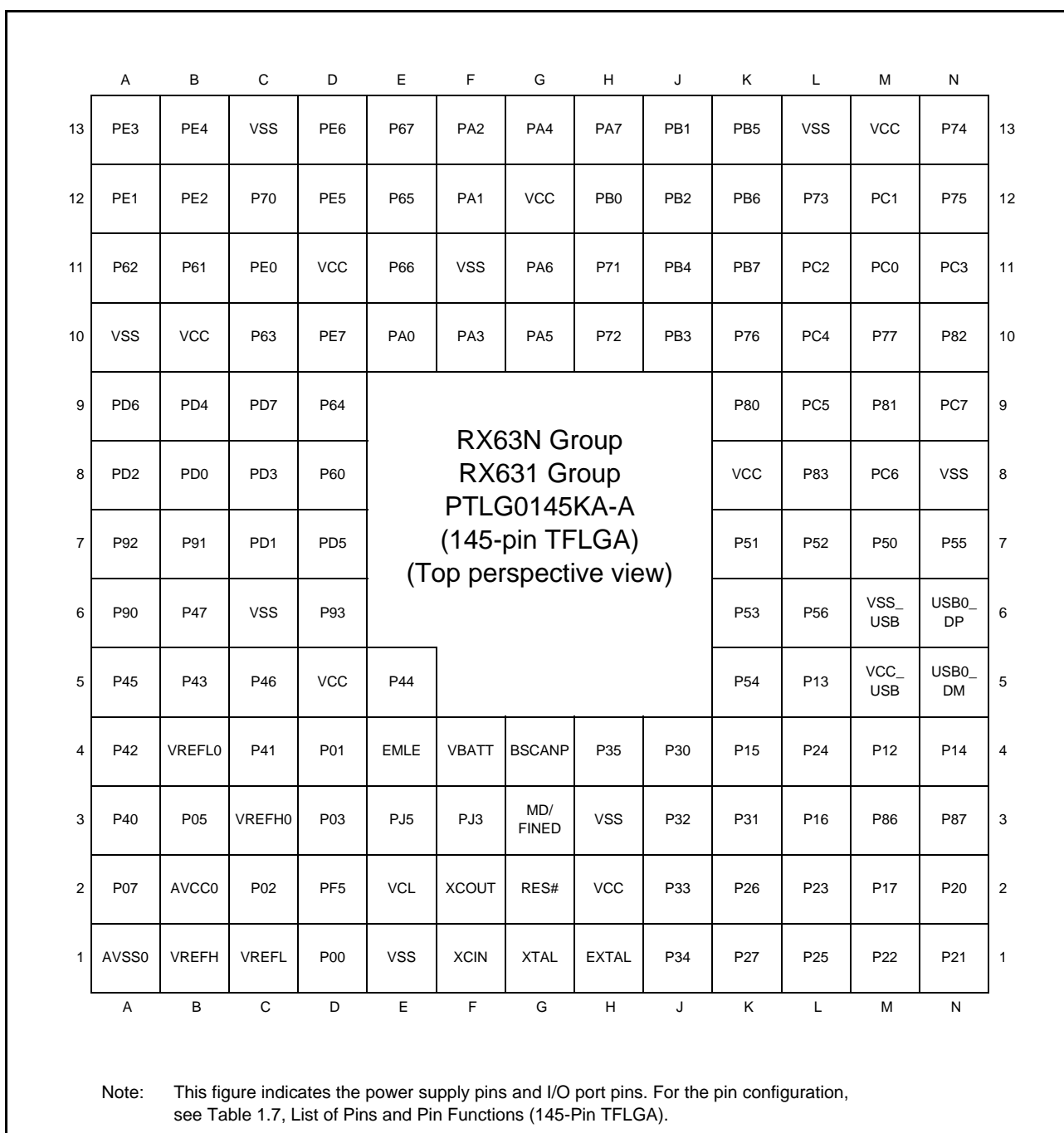


Figure 1.6 Pin Assignment (145-Pin TFLGA)

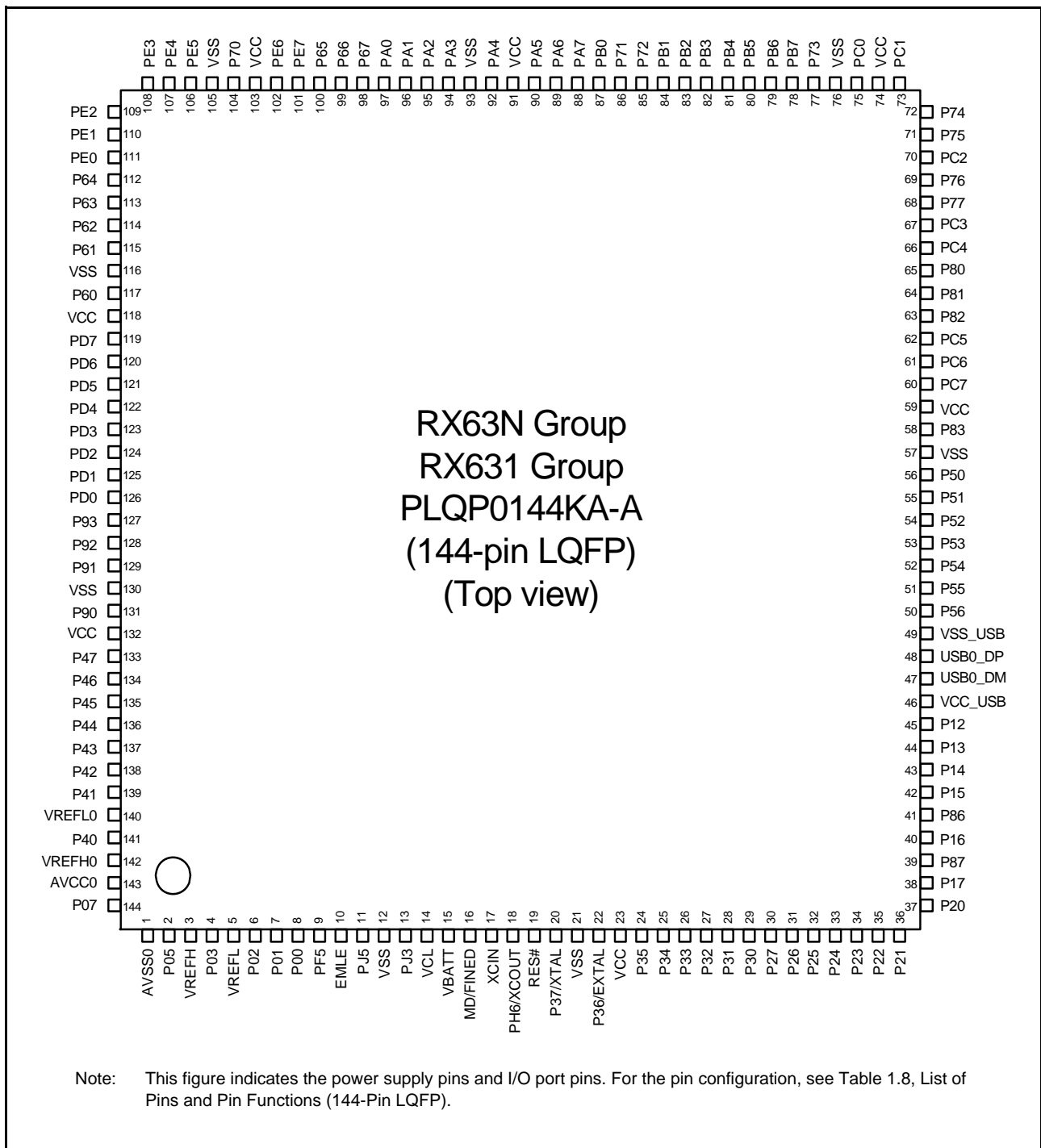


Figure 1.7 Pin Assignment (144-Pin LQFP)

**RX63N Group, RX631 Group
PTLG0100JA-A (100-pin TFLGA)
(Top view)**

| | A | B | C | D | E | F | G | H | J | K | |
|----|--------|-------|--------|--------------|------|-------|-----|-----|-------------|-------------|----|
| 10 | PE2 | PE3 | PE4 | PA0 | PA3 | VSS | VCC | PB7 | PC1 | PC2 | 10 |
| 9 | PE1 | PD7 | PE5 | PA1 | PA5 | PA7 | PB1 | PB6 | PC0 | PC3 | 9 |
| 8 | PE0 | PD6 | PD5 | PE7 | PA4 | PB0 | PB4 | PC6 | PC4 | PC5 | 8 |
| 7 | PD4 | PD3 | PD2 | PE6 | PA6 | PB2 | PB5 | PC7 | P50 | P51 | 7 |
| 6 | PD0 | PD1 | P47 | P46 | PA2 | PB3 | P52 | P54 | VCC_ USB | USB0_ DP | 6 |
| 5 | P43 | P44 | P42 | P45 | P41 | P12 | P53 | P55 | VSS_ USB | USB0_ DM | 5 |
| 4 | VREFL0 | P40 | VREFH0 | VBATT | P34 | P32 | P27 | P15 | P13 | P14 | 4 |
| 3 | P07 | AVCC0 | PJ3 | MD/ FINED | RES# | P35 | P30 | P16 | P17 | P20 | 3 |
| 2 | VREFH | AVSS0 | VREFL | XCOUT | VSS | VCC | P31 | P25 | P21 | P22 | 2 |
| 1 | P05 | EMLE | VCL | XCIN | XTAL | EXTAL | P33 | P26 | P24 | P23 | 1 |
| | A | B | C | D | E | F | G | H | J | K | |

Note: This figure indicates the power supply pins and I/O port pins. For the pin configuration, see Table 1.10, List of Pins and Pin Functions (100-Pin LQFP).

Figure 1.8 Pin Assignment (100-Pin TFLGA)

RX631 Group
PTLG0064JA-A (64-pin TFLGA)
(Top perspective view)

| | A | B | C | D | E | F | G | H | |
|---|--------|-------|----------|-------|-------|-----|---------|---------|---|
| 8 | PE3 | PE4 | PA0 | PA3 | PB0 | PB3 | PB6 | PB7 | 8 |
| 7 | PE2 | PE1 | PE5 | PA1 | VSS | PB5 | PC3 | PC2 | 7 |
| 6 | VREFL | P46 | PE0 | PA4 | VCC | PB1 | PC6 | USB1_DP | 6 |
| 5 | VREFH | P44 | P43 | PA6 | PC4 | P15 | VCC_USB | USB1_DM | 5 |
| 4 | VREFL0 | P42 | P41 | P14 | P16 | PC5 | VSS_USB | USB0_DP | 4 |
| 3 | VREFH0 | P40 | EMLE | P27 | P30 | P31 | VCC_USB | USB0_DM | 3 |
| 2 | AVCC0 | AVSS0 | MD/FINED | RES# | VBATT | P35 | P26 | P17 | 2 |
| 1 | P05 | VCL | XCIN | XCOUT | VSS | VCC | EXTAL | XTAL | 1 |
| | A | B | C | D | E | F | G | H | |

Figure 1.10 Pin Assignment (64-pin TFLGA)

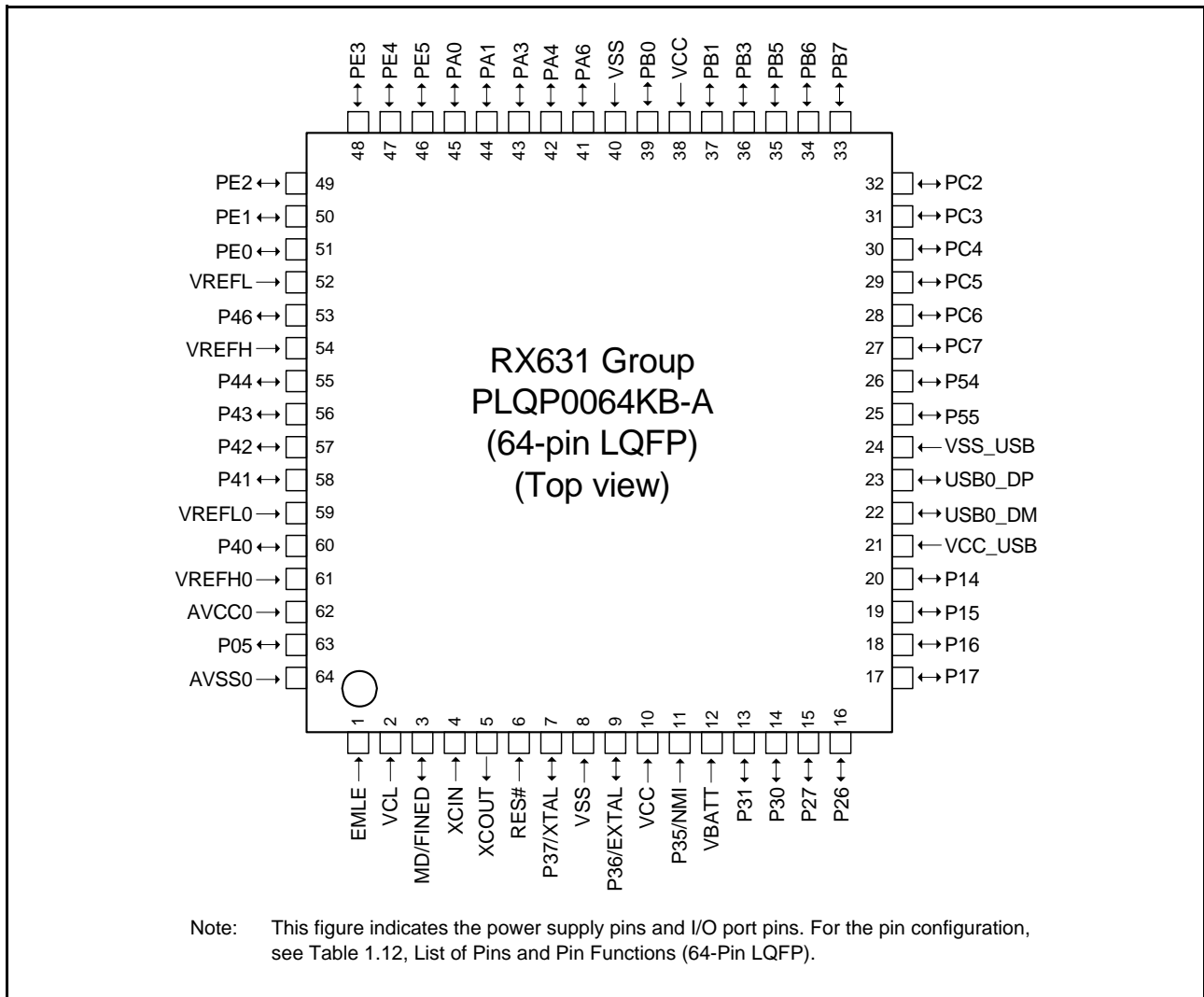


Figure 1.11 Pin Assignment (64-Pin LQFP)

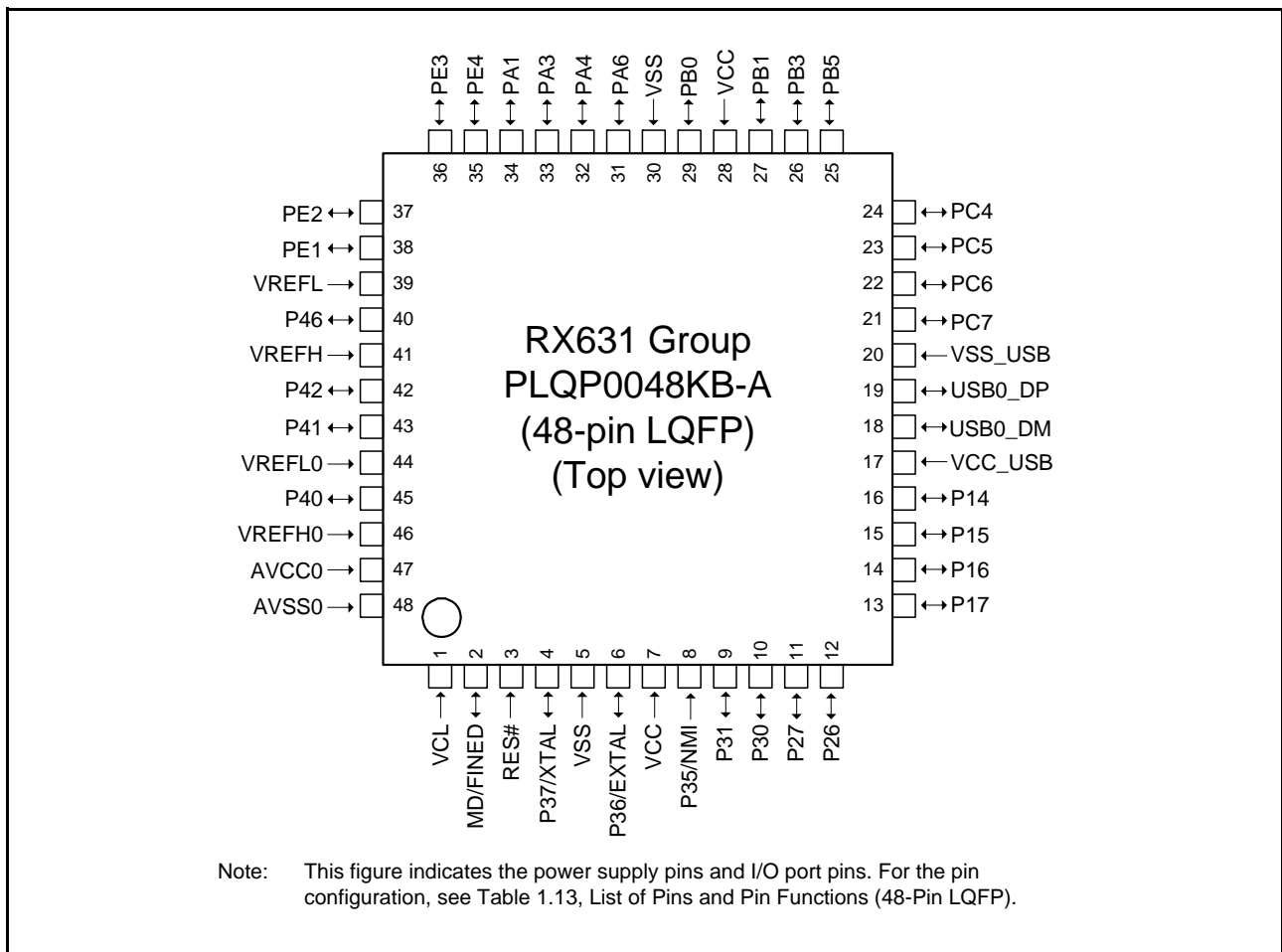


Figure 1.12 Pin Assignment (48-Pin LQFP)

Table 1.5 List of Pin and Pin Functions (177-Pin TFLGA, 176-Pin LFBGA) (1/5)

| Pin Number 177-Pin TFLGA 176-Pin LFBGA | Power Supply Clock System Control | I/O Port | Bus EXDMAC SDRAMC | Timer (MTU, TPU, TMR, PPG, RTC, POE) | Communications (ETHERC, SC1c, SC1d, RSPI, RIIC, CAN, IEB, USB, and PDC) | Interrupt | S12AD, AD, DA |
|--|---|----------|-------------------------|--|--|-----------|------------------|
| A1 | AVSS0 | | | | | | |
| A2 | AVCC0 | | | | | | |
| A3 | VREFLO | | | | | | |
| A4 | | P42 | | | | IRQ10-DS | AN002 |
| A5 | | P46 | | | | IRQ14-DS | AN006 |
| A6 | VCC | | | | | | |
| A7 | VSS | | | | | | |
| A8 | | P94 | A20/D20 | | | | |
| A9 | VCC | | | | | | |
| A10 | | P97 | A23/D23 | | | | |
| A11 | | PD6 | D6[A6/D6] | MTIC5V/POE1# | SSLC2 | IRQ6 | AN6 |
| A12 | | P60 | CS0# | | | | |
| A13 | | P63 | CS3#/CAS# | | | | |
| A14 | | PE1 | D9[A9/D9] | MTIOC4C/TIOCD9/PO18 | TXD12/SMOSI12/ SSDA12/TXD12/ SIOX12/SSLB2/RSPCKB | | ANEX1 |
| A15 | | PE2 | D10[A10/D10] | MTIOC4A/TIOCA9/PO23 | RXD12/SMISO12/ SSCL12/RXD12/SSLB3/ MOSIB | IRQ7-DS | AN0 |
| B1 | | P05 | | | | IRQ13 | DA1 |
| B2 | | P07 | | | | IRQ15 | ADTRG0# |
| B3 | | P40 | | | | IRQ8-DS | AN000 |
| B4 | | P41 | | | | IRQ9-DS | AN001 |
| B5 | | P47 | | | | IRQ15-DS | AN007 |
| B6 | | P91 | A17/D17 | | SCK7 | | AN015 |
| B7 | | P92 | A18/D18 | | RXD7/SMISO7/SSCL7 | | AN016 |
| B8 | | PD1 | D1[A1/D1] | MTIOC4B/TIOCB7/ TCLKG | MOSIC/CTX0 | IRQ1 | AN009 |
| B9 | | P96 | A22/D22 | | | | |
| B10 | | PD4 | D4[A4/D4] | POE3# | SSLC0 | IRQ4 | AN012 |
| B11 | | PG1 | D25 | | | | |
| B12 | VSS | | | | | | |
| B13 | | P64 | CS4#/WE# | | | | |
| B14 | | PE0 | D8[A8/D8] | TIOCC9 | SCK12/SSLB1 | | ANEX0 |
| B15 | | PE3 | D11[A11/D11] | MTIOC4B/TIOCB9/PO26/ POE8# | ET_ERXD3/CTS12#/ RTS12#/SS12#/MISOB | | AN1 |
| C1 | VREFL | | | | | | |
| C2 | VREFH | | | | | | |
| C3 | VREFH0 | | | | | | |
| C4 | | P43 | | | | IRQ11-DS | AN003 |
| C5 | | P45 | | | | IRQ13-DS | AN005 |
| C6 | | P90 | A16/D16 | | TXD7/SMOSI7/SSDA7 | | AN014 |
| C7 | | PD0 | D0[A0/D0] | TIOCA7 | | IRQ0 | AN008 |
| C8 | | PD2 | D2[A2/D2] | MTIOC4D/TIOCA8 | MISOC/CRX0 | IRQ2 | AN010 |
| C9 | | PD3 | D3[A3/D3] | TIOCB8/TCLKH/POE8# | RSPCKC | IRQ3 | AN011 |
| C10 | | PG0 | D24 | | | | |
| C11 | VCC | | | | | | |
| C12 | | P62 | CS2#/RAS# | | | | |
| C13 | | PE4 | D12[A12/D12] | MTIOC4D/MTIOC1A/ TIOCA10/PO28 | ET_ERXD2/SSLB0 | | AN2 |

Table 1.5 List of Pin and Pin Functions (177-Pin TFLGA, 176-Pin LFBGA) (2/5)

| Pin Number 177-Pin TFLGA 176-Pin LFBGA | Power Supply Clock System Control | I/O Port | Bus EXDMAC SDRAMC | Timer (MTU, TPU, TMR, PPG, RTC, POE) | Communications (ETHERC, SC1c, SC1d, RSPI, RIIC, CAN, IEB, USB, and PDC) | Interrupt | S12AD, AD, DA |
|--|---|----------|-------------------------|--|--|-----------|------------------|
| C14 | VSS | | | | | | |
| C15 | SDCLK | P70 | | | | | |
| D1 | | P01 | | TMCI0 | RXD6/SMISO6/SSCL6 | IRQ9 | AN019 |
| D2 | | P02 | | TMCI1 | SCK6 | IRQ10 | AN020 |
| D3 | | P03 | | | | IRQ11 | DA0 |
| D4 | | P00 | | TMRI0 | TXD6/SMOSI6/SSDA6 | IRQ8 | AN018 |
| D5 | | P44 | | | | IRQ12-DS | AN004 |
| D6 | | P93 | A19/D19 | | CTS7#/RTS7#/SS7# | | AN017 |
| D7 | | P95 | A21/D21 | | | | |
| D8 | VSS | | | | | | |
| D9 | | PD5 | D5[A5/D5] | MTIC5W/POE2# | SSLC1 | IRQ5 | AN013 |
| D10 | | PD7 | D7[A7/D7] | MTIC5U/POE0# | SSLC3 | IRQ7 | AN7 |
| D11 | | P61 | CS1#/SDCS# | | | | |
| D12 | | PE5 | D13[A13/D13] | MTIOC4C/MTIOC2B/ TIOCB10 | ET_RX_CLK/REF50CK/ RSPCKB | IRQ5 | AN3 |
| D13 | VCC | | | | | | |
| D14 | | PE7 | D15[A15/D15] | TIOCB11 | MISOB | IRQ7 | AN5 |
| D15 | | P65 | CS5#/CKE | | | | |
| E1 | | PJ5 | | | | | |
| E2 | EMLE | | | | | | |
| E3 | | PF5 | | | | IRQ4 | |
| E4 | VSS | | | | | | |
| E5*1 | NC | | | | | | |
| E12 | | PE6 | D14[A14/D14] | TIOCA11 | MOSIB | IRQ6 | AN4 |
| E13 | TRDATA0 | PG2 | D26 | | | | |
| E14 | TRDATA1 | PG3 | D27 | | | | |
| E15 | | P67 | CS7#/DQM1 | | CRX2*3 | IRQ15 | |
| F1 | VBATT | | | | | | |
| F2 | VCL | | | | | | |
| F3 | | PJ3 | | MTIOC3C | CTS6#/RTS6#/CTS0#/ RTS0#/SS6#/SS0# | | |
| F4 | BSCANP | | | | | | |
| F12 | | P66 | CS6#/DQM0 | | CTX2*3 | | |
| F13 | TRSYNC | PG4 | D28 | | | | |
| F14 | | PA0 | A0/BC0#/DQM2 | MTIOC4A/TIOCA0/PO16 | ET_TX_EN/ RMII_TXD_EN/SSLA1 | | |
| F15 | VSS | | | | | | |
| G1 | XCIN | | | | | | |
| G2 | XCOU | | | | | | |
| G3 | MD/FINED | | | | | | |
| G4 | TRST# | PF4 | | | | | |
| G12 | TRCLK | PG5 | D29 | | | | |
| G13 | TRDATA2 | PG6 | D30 | | | | |
| G14 | | PA1 | A1/DQM3 | MTIOC0B/MTCLKC/ TIOCB0/PO17 | ET_WOL/SCK5/SSLA2 | IRQ11 | |
| G15 | VCC | | | | | | |
| H1 | XTAL | P37 | | | | | |
| H2 | VSS | | | | | | |

Table 1.5 List of Pin and Pin Functions (177-Pin TFLGA, 176-Pin LFBGA) (3/5)

| Pin Number 177-Pin TFLGA 176-Pin LFBGA | Power Supply Clock System Control | I/O Port | Bus EXDMAC SDRAMC | Timer (MTU, TPU, TMR, PPG, RTC, POE) | Communications (ETHERC, SCIC, SCID, RSPI, RIIC, CAN, IEB, USB, and PDC) | Interrupt | S12AD, AD, DA |
|--|---|----------|-------------------------|--|--|-----------|------------------|
| H3 | RES# | | | | | | |
| H4 | | P35 | | | | NMI | |
| H12 | | PA4 | A4 | MTIC5U/MTCLKA/ TIOCA1/TMRI0/PO20 | ET_MDC/TXD5/SMOSI5/ SSDA5/SSLA0 | IRQ5-DS | |
| H13 | | PA3 | A3 | MTIOC0D/MTCLKD/ TIOC0D/TCLKB/PO19 | ET_MDIO/RXD5/SMISO5/ SSCL5 | IRQ6-DS | |
| H14 | | PA2 | A2 | PO18 | RXD5/SMISO5/SSCL5/ SSLA3 | | |
| H15 | TRDATA3 | PG7 | D31 | | | | |
| J1 | EXTAL | P36 | | | | | |
| J2 | VCC | | | | | | |
| J3 | | P34 | | MTIOC0A/TMCI3/PO12/ POE2# | SCK6/SCK0/ USB0_DPRPD | IRQ4 | |
| J4 | TMS | PF3 | | | | | |
| J12 | | PA5 | A5 | TIOCB1/PO21 | ET_LINKSTA/RSPCKA | | |
| J13 | VSS | | | | | | |
| J14 | | PA7 | A7 | TIOCB2/PO23 | ET_WOL/MISOA | | |
| J15 | | PA6 | A6 | MTIC5V/MTCLKB/ TIOCA2/TMCI3/PO22/ POE2# | ET_EXOUT/CTS5#/ RTS5#/SS5#/MOSIA | | |
| K1 | | P33 | | MTIOC0D/TIOC0D/ TMRI3/PO11/POE3# | RXD6/RXD0/SMISO6/ SMISO0/SSCL6/SSCL0/ CRX0/PCKO | IRQ3-DS | |
| K2 | | P32 | | MTIOC0C/TIOCC0/TMO3/ PO10/RTCOU7/RTCIC2 | TXD6/TXD0/SMOSI6/ SMOSI0/SSDA6/SSDA0/ CTX0/USB0_VBUSEN/ VSYNC | IRQ2-DS | |
| K3 | TDI | PF2 | | | RXD1/SMISO1/SSCL1 | | |
| K4 | TCK/FINEC | PF1 | | | SCK1 | | |
| K12 | | PB2 | A10 | TIOCC3/TCLKC/PO26 | ET_RX_CLK/REF50CK/ CTS4#/RTS4#/CTS6#/ RTS6#/SS4#/SS6# | | |
| K13 | | P71 | CS1# | | ET_MDIO | | |
| K14 | VCC | | | | | | |
| K15 | | PB0 | A8 | MTIC5W/TIOCA3/PO24 | ET_ERXD1/RMII_RXD1/ RXD4/RXD6/SMISO4/ SMISO6/SSCL4/SSCL6/ RSPCKA | IRQ12 | |
| L1 | | P31 | | MTIOC4D/TMCI2/PO9/ RTCIC1 | CTS1#/RTS1#/SS1#/ SSLB0/USB0_DPUPE | IRQ1-DS | |
| L2 | | P30 | | MTIOC4B/TMRI3/PO8/ RTCIC0/POE8# | RXD1/SMISO1/SSCL1/ MISOB/USB0_DRPD | IRQ0-DS | |
| L3 | TDO | PF0 | | | TXD1/SMOSI1/SSDA1 | | |
| L4 | | P25 | CS5#/EDACK1 | MTIOC4C/MTCLKB/ TIOCA4/PO5 | RXD3/SMISO3/SSCL3/ USB0_DPRPD/HSYNC | | ADTRG0# |
| L12 | | PB6 | A14 | MTIOC3D/TIOCA5/PO30 | ET_ETXD1/RMII_TXD1/ RXD9/SMISO9/SSCL9 | | |
| L13 | | PB3 | A11 | MTIOC0A/MTIOC4A/ TIOC0D/TCLKD/TMO0/ PO27/POE3# | ET_RX_ER/RMII_RX_ER/ SCK4/SCK6 | | |
| L14 | | PB1 | A9 | MTIOC0C/MTIOC4C/ TIOCB3/TMCI0/PO25 | ET_ERXD0/RMII_RXD0/ TXD4/TXD6/SMOSI4/ SMOSI6/SSDA4/SSDA6 | IRQ4-DS | |
| L15 | | P72 | CS2# | | ET_MDC | | |
| M1 | | P27 | CS7# | MTIOC2B/TMCI3/PO7 | SCK1/RSPCKB | | |

Table 1.5 List of Pin and Pin Functions (177-Pin TFLGA, 176-Pin LFBGA) (4/5)

| Pin Number 177-Pin TFLGA 176-Pin LFBGA | Power Supply Clock System Control | I/O Port | Bus EXDMAC SDRAMC | Timer (MTU, TPU, TMR, PPG, RTC, POE) | Communications (ETHERC, SCIC, SCID, RSPI, RIIC, CAN, IEB, USB, and PDC) | Interrupt | S12AD, AD, DA |
|--|---|----------|----------------------------|---|--|-----------|------------------|
| M2 | | P26 | CS6# | MTIOC2A/TMO1/PO6 | TXD1/CTS3#/RTS3# SMOS11/SS3#/SSDA1/ MOSIB | | |
| M3 | | P24 | CS4#/EDREQ1 | MTIOC4A/MTCLKA/ TIOCB4/TMR1/PO4 | SCK3/USB0_VBUSEN/ PIXCLK | | |
| M4 | | P86 | | TIOCA0 | PIXD1 | | |
| M5 | | P13 | | MTIOC0B/TIOCA5/TMO3/ PO13 | TXD2/SMOS12/SSDA2/ SDA0[FM+] | IRQ3 | ADTRG# |
| M6 | | P56 | WR2#/BC2#/ EDACK1 | MTIOC3C/TIOCA1 | | | |
| M7 | | P54 | ALE/EDACK0 | MTIOC4B/TMC11 | ET_LINKSTA/CTS2#/ RTS2#/SS2#/CTX1 | | |
| M8 | | P53*2 | BCLK | | | | |
| M9 | | P50 | WR0#/WR# | | TXD2/SMOS12/SSDA2/ SSLB1 | | |
| M10 | | PC5 | A21/CS2#/ WAIT# | MTIOC3B/MTCLKD/ TIOCD6/TCLKF/TMR12/ PO29 | ET_ETXD2/SCK8/ RSPCKA | | |
| M11 | | P81 | EDACK0 | MTIOC3D/PO27 | ET_ETXD0/RMIL_TXD0/ RXD10/SMISO10/SSCL10 | | |
| M12 | | P77 | CS7# | PO23 | ET_RX_ER/RMIL_RX_ER/ TXD11/SMOS11/SSDA11 | | |
| M13 | | PB7 | A15 | MTIOC3B/TIOCB5/PO31 | ET_CRS/RMIL_CRS_DV/ TXD9/SMOS9/SSDA9 | | |
| M14 | | PB5 | A13 | MTIOC2A/MTIOC1B/ TIOCB4/TMR11/PO29/ POE1# | ET_ETXD0/RMIL_TXD0/ SCK9 | | |
| M15 | | PB4 | A12 | TIOCA4/PO28 | ET_TX_EN/ RMIL_TXD_EN/CTS9#/ RTS9#/SS9# | | |
| N1 | VCC | | | | | | |
| N2 | | P23 | EDACK0 | MTIOC3D/MTCLKD/ TIOCD3/PO3 | TXD3/CTS0#/RTS0#/ SMOS13/SS0#/SSDA3/ USB0_DPUPE/PIXD7 | | |
| N3 | | P22 | EDREQ0 | MTIOC3B/MTCLKC/ TIOCC3/TMO0/PO2 | SCK0/USB0_DRPD/ PIXD6 | | |
| N4 | | P15 | | MTIOC0B/MTCLKB/ TIOCB2/TCLKB/TMC12/ PO13 | RXD1/SCK3/SMISO1/ SSCL1/CRX1-DS/ USB1_DPUPE/PIXD0 | IRQ5 | |
| N5 | | P12 | | MTIC5U/TMC11 | RXD2/SMISO2/SSCL2/ SCL0[FM+] | IRQ2 | |
| N6 | | P57 | WAIT#/WR3#/ BC3#/EDREQ1 | | | | |
| N7 | | P55 | WAIT#/ EDREQ0 | MTIOC4D/TMO3 | ET_EXOUT/CRX1 | IRQ10 | |
| N8 | VCC_USB | | | | | | |
| N9 | | P51 | WR1#/BC1#/ WAIT# | | SCK2/SSLB2 | | |
| N10 | | PC7 | A23/CS0# | MTIOC3A/MTCLKB/ TIOCB6/TMO2/PO31 | ET_COL/TXD8/SMOS18/ SSDA8/MISOA | IRQ14 | |
| N11 | | P82 | EDREQ1 | MTIOC4A/PO28 | ET_ETXD1/RMIL_TXD1/ TXD10/SMOS10/SSDA10 | | |
| N12 | | PC3 | A19 | MTIOC4D/TCLKB/PO24 | ET_TX_ER/TXD5/ SMOS15/SSDA5/ETXD | | |
| N13 | | PC0 | A16 | MTIOC3C/TCLKC/PO17 | ET_ERXD3/CTS5#/ RTS5#/SS5#/SSLA1/ SCL3 | IRQ14 | |
| N14 | | P73 | CS3# | PO16 | ET_WOL | | |
| N15 | VSS | | | | | | |

Table 1.5 List of Pin and Pin Functions (177-Pin TFLGA, 176-Pin LFBGA) (5/5)

| Pin Number 177-Pin TFLGA 176-Pin LFBGA | Power Supply Clock System Control | I/O Port | Bus EXDMAC SDRAMC | Timer (MTU, TPU, TMR, PPG, RTC, POE) | Communications (ETHERC, SCId, SCId, RSPI, RIIC, CAN, IEB, USB, and PDC) | Interrupt | S12AD, AD, DA |
|--|---|----------|-------------------------|---|--|-----------|------------------|
| P1 | VSS | | | | | | |
| P2 | | P17 | | MTIOC3A/MTIOC3B/ TIOCB0/TCLKD/TMO1/ PO15/POE8# | SCK1/TXD3/SMOSI3/ SSDA3/MISOA/SDA2-DS/ IETXD/USB1_VBUS/ PIXD3 | IRQ7 | ADTRG# |
| P3 | | P87 | | TIOCA2 | PIXD2 | | |
| P4 | | P14 | | MTIOC3A/MTCLKA/ TIOCB5/TCLKA/TMRI2/ PO15 | CTS1#/RTS1#/SS1#/ CTX1/USB0_DPUPE/ USB0_OVRCURA | IRQ4 | |
| P5 | | P10 | | MTIC5W/TMRI3 | | IRQ0 | |
| P6 | VCC_USB | | | | | | |
| P7 | VSS_USB | | | | | | |
| P8 | | | | | USB1_DP | | |
| P9 | | P52 | RD# | | RXD2/SMISO2/SSCL2/ SSLB3 | | |
| P10 | | P83 | EDACK1 | MTIOC4C | ET_CRS/RMII_CRS_DV/ CTS10#/RTS10#/SS10# | | |
| P11 | | PC6 | A22/CS1# | MTIOC3C/MTCLKA/ TIOCA6/TMC12/PO30 | ET_ETXD3/RXD8/ SMISO8/SSCL8/MOSIA | IRQ13 | |
| P12 | | PC4 | A20/CS3# | MTIOC3D/MTCLKC/ TIOCC6/TCLKE/TMC11/ PO25/POE0# | ET_TX_CLK/SCK5/ CTS8#/RTS8#/SS8#/ SSLA0 | | |
| P13 | | PC2 | A18 | MTIOC4B/TCLKA/PO21 | ET_RX_DV/RXD5/ SMISO5/SSCL5/SSLA3/ IERXD | | |
| P14 | | P75 | CS5# | PO20 | ET_ERXD0/RMII_RXD0/ SCK11 | | |
| P15 | VCC | | | | | | |
| R1 | | P21 | | MTIOC1B/TIOCA3/ TMC10/PO1 | RXD0/SMISO0/SSCL0/ SCL1/USB0_EXICEN/ PIXD5 | IRQ9 | |
| R2 | | P20 | | MTIOC1A/TIOCB3/ TMRI0/PO0 | TXD0/SMOSI0/SSDA0/ SDA1/USB0_ID/PIXD4 | IRQ8 | |
| R3 | | P16 | | MTIOC3C/MTIOC3D/ TIOCB1/TCLKC/TMO2/ PO14/RTCOUT | TXD1/RXD3/SMOSI1/ SMISO3/SSDA1/SSCL3/ MOSIA/SCL2-DS/IERXD/ USB0_VBUS/ USB0_VBUSEN/ USB0_OVRCURB | IRQ6 | ADTRG0# |
| R4 | | P85 | | | | | |
| R5 | | P11 | | MTIC5V/TMC13 | SCK2 | IRQ1 | |
| R6 | | | | | USB0_DM | | |
| R7 | | | | | USB0_DP | | |
| R8 | | | | | USB1_DM | | |
| R9 | | P84 | | | | | |
| R10 | VSS | | | | | | |
| R11 | VCC | | | | | | |
| R12 | | P80 | EDREQ0 | MTIOC3B/PO26 | ET_TX_EN/ RMII_TXD_EN/SCK10 | | |
| R13 | | P76 | CS6# | PO22 | ET_RX_CLK/REF50CK/ RXD11/SMISO11/SSCL11 | | |
| R14 | | P74 | CS4# | PO19 | ET_ERXD1/RMII_RXD1/ CTS11#/RTS11#/SS11# | | |
| R15 | | PC1 | A17 | MTIOC3A/TCLKD/PO18 | ET_ERXD2/SCK5/SSLA2/ SDA3 | IRQ12 | |

Note 1. 176-pin LFBGA does not have E5 pin

Note 2. The BCLK function is multiplexed with the I/O port function for pin P53, so the port function is not available if the external bus is enabled.

Note 3. Enabled only for the ROM capacity: 2 Mbytes/1.5 Mbytes

Table 1.6 List of Pin and Pin Functions (176-Pin LQFP) (1/5)

| Pin Number | Power Supply Clock System Control | I/O Port | Bus EXDMAC SDRAMC | Timer (MTU, TPU, TMR, PPG, RTC, POE) | Communications (ETHERC, SCIC, SCID, RSPI, RIIC, CAN, IEB, USB, and PDC) | Interrupt | S12AD, AD, DA |
|------------|---|----------|-------------------------|--|--|-----------|------------------|
| 1 | AVSS0 | | | | | | |
| 2 | | P05 | | | | IRQ13 | DA1 |
| 3 | VREFH | | | | | | |
| 4 | | P03 | | | | IRQ11 | DA0 |
| 5 | VREFL | | | | | | |
| 6 | | P02 | | TMC1 | SCK6 | IRQ10 | AN020 |
| 7 | | P01 | | TMC10 | RXD6/SMISO6/SSCL6 | IRQ9 | AN019 |
| 8 | | P00 | | TMR10 | TXD6/SMOSI6/SSDA6 | IRQ8 | AN018 |
| 9 | | PF5 | | | | IRQ4 | |
| 10 | EMLE | | | | | | |
| 11 | | PJ5 | | | | | |
| 12 | VSS | | | | | | |
| 13 | | PJ3 | | MTIOC3C | CTS6#/RTS6#/CTS0#/ RTS0#/SS6#/SS0# | | |
| 14 | VCL | | | | | | |
| 15 | VBATT | | | | | | |
| 16 | NC | | | | | | |
| 17 | TRST# | PF4 | | | | | |
| 18 | MD/FINED | | | | | | |
| 19 | XCIN | | | | | | |
| 20 | XCOUT | | | | | | |
| 21 | RES# | | | | | | |
| 22 | XTAL | P37 | | | | | |
| 23 | VSS | | | | | | |
| 24 | EXTAL | P36 | | | | | |
| 25 | VCC | | | | | | |
| 26 | | P35 | | | | NMI | |
| 27 | | P34 | | MTIOC0A/TMC13/PO12/ POE2# | SCK6/SCK0/ USB0_DPRPD | IRQ4 | |
| 28 | | P33 | | MTIOC0D/TIOC0D0/ TMR13/PO11/POE3# | RXD6/RXD0/SMISO6/ SMISO0/SSCL6/SSCL0/ CRX0/PCKO | IRQ3-DS | |
| 29 | | P32 | | MTIOC0C/TIOCC0/TMO3/ PO10/RTCOU/RTCIC2 | TXD6/TXD0/SMOSI6/ SMOSI0/SSDA6/SSDA0/ CTX0/USB0_VBUSEN/ VSYNC | IRQ2-DS | |
| 30 | TMS | PF3 | | | | | |
| 31 | TDI | PF2 | | | RXD1/SMISO1/SSCL1 | | |
| 32 | | P31 | | MTIOC4D/TMC12/PO9/ RTCIC1 | CTS1#/RTS1#/SS1#/ SSLB0/USB0_DPUPE | IRQ1-DS | |
| 33 | | P30 | | MTIOC4B/TMR13/PO8/ RTCIC0/POE8# | RXD1/SMISO1/SSCL1/ MISOB/USB0_DRPD | IRQ0-DS | |
| 34 | TCK/FINEC | PF1 | | | SCK1 | | |
| 35 | TDO | PF0 | | | TXD1/SMOSI1/SSDA1 | | |
| 36 | | P27 | CS7# | MTIOC2B/TMC13/PO7 | SCK1/RSPCKB | | |
| 37 | | P26 | CS6# | MTIOC2A/TMO1/PO6 | TXD1/CTS3#/RTS3# SMOSI1/SS3#/SSDA1/ MOSIB | | |
| 38 | | P25 | CS5#/EDACK1 | MTIOC4C/MTCLKB/ TIOCA4/PO5 | RXD3/SMISO3/SSCL3/ USB0_DPRPD/HSYNC | | ADTRG0# |
| 39 | VCC | | | | | | |
| 40 | | P24 | CS4#/EDREQ1 | MTIOC4A/MTCLKA/ TIOCB4/TMR11/PO4 | SCK3/USB0_VBUSEN/ PIXCLK | | |

Table 1.6 List of Pin and Pin Functions (176-Pin LQFP) (2/5)

| Pin Number | Power Supply Clock System Control | I/O Port | Bus EXDMAC SDRAMC | Timer (MTU, TPU, TMR, PPG, RTC, POE) | Communications (ETHERC, SC1c, SC1d, RSPI, RIIC, CAN, IEB, USB, and PDC) | Interrupt | S12AD, AD, DA |
|------------|---|----------|----------------------------|---|--|-----------|------------------|
| 41 | VSS | | | | | | |
| 42 | | P23 | EDACK0 | MTIOC3D/MTCLKD/ TIOCD3/PO3 | TXD3/CTS0#/RTS0#/ SMOSI3/SS0#/SSDA3/ USB0_DPUPE/PIXD7 | | |
| 43 | | P22 | EDREQ0 | MTIOC3B/MTCLKC/ TIOCC3/TMO0/PO2 | SCK0/USB0_DRPD/ PIXD6 | | |
| 44 | | P21 | | MTIOC1B/TIOCA3/ TMC10/PO1 | RXD0/SMISO0/SSCL0/ SCL1/USB0_EXICEN/ PIXD5 | IRQ9 | |
| 45 | | P20 | | MTIOC1A/TIOCB3/ TMR10/PO0 | TXD0/SMOSI0/SSDA0/ SDA1/USB0_ID/PIXD4 | IRQ8 | |
| 46 | | P17 | | MTIOC3A/MTIOC3B/ TIOCB0/TCLKD/TMO1/ PO15/POE8# | SCK1/TXD3/SMOSI3/ SSDA3/MISOA/SDA2-DS/ IETXD/USB1_VBUS/ PIXD3 | IRQ7 | ADTRG# |
| 47 | | P87 | | TIOCA2 | PIXD2 | | |
| 48 | | P16 | | MTIOC3C/MTIOC3D/ TIOCB1/TCLKC/TMO2/ PO14/RTCOUT | TXD1/RXD3/SMOSI1/ SMISO3/SSDA1/SSCL3/ MOSIA/SCL2-DS/IERXD/ USB0_VBUS/ USB0_VBUSEN/ USB0_OVRCURB | IRQ6 | ADTRG0# |
| 49 | | P86 | | TIOCA0 | PIXD1 | | |
| 50 | | P15 | | MTIOC0B/MTCLKB/ TIOCB2/TCLKB/TMC12/ PO13 | RXD1/SCK3/SMISO1/ SSCL1/CRX1-DS/ USB1_DPUPE/PIXD0 | IRQ5 | |
| 51 | | P14 | | MTIOC3A/MTCLKA/ TIOCB5/TCLKA/TMR12/ PO15 | CTS1#/RTS1#/#SS1#/ CTX1/USB0_DPUPE/ USB0_OVRCURA | IRQ4 | |
| 52 | | P85 | | | | | |
| 53 | | P13 | | MTIOC0B/TIOCA5/TMO3/ PO13 | TXD2/SMOSI2/SSDA2/ SDA0[FM+] | IRQ3 | ADTRG# |
| 54 | | P12 | | MTIC5U/TMC11 | RXD2/SMISO2/SSCL2/ SCL0[FM+] | IRQ2 | |
| 55 | | P11 | | MTIC5V/TMC13 | SCK2 | IRQ1 | |
| 56 | | P10 | | MTIC5W/TMR13 | | IRQ0 | |
| 57 | VCC_USB | | | | | | |
| 58 | | | | | USB0_DM | | |
| 59 | | | | | USB0_DP | | |
| 60 | VSS_USB | | | | | | |
| 61 | | P57 | WAIT#/WR3#/ BC3#/EDREQ1 | | | | |
| 62 | | P56 | WR2#/BC2#/ EDACK1 | MTIOC3C/TIOCA1 | | | |
| 63 | | | | | USB1_DM | | |
| 64 | | | | | USB1_DP | | |
| 65 | VCC_USB | | | | | | |
| 66 | | P55 | WAIT#/ EDREQ0 | MTIOC4D/TMO3 | ET_EXOUT/CRX1 | IRQ10 | |
| 67 | | P54 | ALE/EDACK0 | MTIOC4B/TMC11 | ET_LINKSTA/CTS2#/ RTS2#/SS2#/CTX1 | | |
| 68 | | P53*1 | BCLK | | | | |
| 69 | | P84 | | | | | |
| 70 | | P52 | RD# | | RXD2/SMISO2/SSCL2/ SSLB3 | | |
| 71 | | P51 | WR1#/BC1#/ WAIT# | | SCK2/SSLB2 | | |

Table 1.6 List of Pin and Pin Functions (176-Pin LQFP) (3/5)

| Pin Number | Power Supply Clock System Control | I/O Port | Bus EXDMAC SDRAMC | Timer (MTU, TPU, TMR, PPG, RTC, POE) | Communications (ETHERC, SC1c, SC1d, RSPI, RIIC, CAN, IEB, USB, and PDC) | Interrupt | S12AD, AD, DA |
|------------|---|----------|-------------------------|--|--|-----------|------------------|
| 72 | | P50 | WR0#/WR# | | TXD2/SMOSI2/SSDA2/ SSLB1 | | |
| 73 | VSS | | | | | | |
| 74 | | P83 | EDACK1 | MTIOC4C | ET_CRS/RMII_CRS_DV/ CTS10#/RTS10#/SS10# | | |
| 75 | VCC | | | | | | |
| 76 | | PC7 | A23/CS0# | MTIOC3A/MTCLKB/ TIOCB6/TMO2/PO31 | ET_COL/TXD8/SMOSI8/ SSDA8/MISOA | IRQ14 | |
| 77 | | PC6 | A22/CS1# | MTIOC3C/MTCLKA/ TIOCA6/TMCI2/PO30 | ET_ETXD3/RXD8/ SMISO8/SSCL8/MOSIA | IRQ13 | |
| 78 | | PC5 | A21/CS2#/ WAIT# | MTIOC3B/MTCLKD/ TIOCD6/TCLKF/TMRI2/ PO29 | ET_ETXD2/SCK8/ RSPCKA | | |
| 79 | | P82 | EDREQ1 | MTIOC4A/PO28 | ET_ETXD1/RMII_TXD1/ TXD10/SMOSI10/SSDA10 | | |
| 80 | | P81 | EDACK0 | MTIOC3D/PO27 | ET_ETXD0/RMII_TXD0/ RXD10/SMISO10/SSCL10 | | |
| 81 | | P80 | EDREQ0 | MTIOC3B/PO26 | ET_TX_EN/ RMII_TXD_EN/SCK10 | | |
| 82 | | PC4 | A20/CS3# | MTIOC3D/MTCLKC/ TIOCC6/TCLKE/TMCI1/ PO25/POE0# | ET_TX_CLK/SCK5/ CTS8#/RTS8#/SS8#/ SSLA0 | | |
| 83 | | PC3 | A19 | MTIOC4D/TCLKB/PO24 | ET_TX_ER/TXD5/ SMOSI5/SSDA5/ETXD | | |
| 84 | | P77 | CS7# | PO23 | ET_RX_ER/RMII_RX_ER/ TXD11/SMOSI11/SSDA11 | | |
| 85 | | P76 | CS6# | PO22 | ET_RX_CLK/REF50CK/ RXD11/SMISO11/SSCL11 | | |
| 86 | | PC2 | A18 | MTIOC4B/TCLKA/PO21 | ET_RX_DV/RXD5/ SMISO5/SSCL5/SSLA3/ IERXD | | |
| 87 | | P75 | CS5# | PO20 | ET_ERXD0/RMII_RXD0/ SCK11 | | |
| 88 | | P74 | CS4# | PO19 | ET_ERXD1/RMII_RXD1/ CTS11#/RTS11#/SS11# | | |
| 89 | | PC1 | A17 | MTIOC3A/TCLKD/PO18 | ET_ERXD2/SCK5/SSLA2/ SDA3 | IRQ12 | |
| 90 | VCC | | | | | | |
| 91 | | PC0 | A16 | MTIOC3C/TCLKC/PO17 | ET_ERXD3/CTS5#/ RTS5#/SS5#/SSLA1/ SCL3 | IRQ14 | |
| 92 | VSS | | | | | | |
| 93 | | P73 | CS3# | PO16 | ET_WOL | | |
| 94 | | PB7 | A15 | MTIOC3B/TIOCB5/PO31 | ET_CRS/RMII_CRS_DV/ TXD9/SMOSI9/SSDA9 | | |
| 95 | | PB6 | A14 | MTIOC3D/TIOCA5/PO30 | ET_ETXD1/RMII_TXD1/ RXD9/SMISO9/SSCL9 | | |
| 96 | | PB5 | A13 | MTIOC2A/MTIOC1B/ TIOCB4/TMRI1/PO29/ POE1# | ET_ETXD0/RMII_TXD0/ SCK9 | | |
| 97 | | PB4 | A12 | TIOCA4/PO28 | ET_TX_EN/ RMII_TXD_EN/CTS9#/ RTS9#/SS9# | | |
| 98 | | PB3 | A11 | MTIOC0A/MTIOC4A/ TIOCD3/TCLKD/TMO0/ PO27/POE3# | ET_RX_ER/RMII_RX_ER/ SCK4/SCK6 | | |
| 99 | | PB2 | A10 | TIOCC3/TCLKC/PO26 | ET_RX_CLK/REF50CK/ CTS4#/RTS4#/CTS6#/ RTS6#/SS4#/SS6# | | |

Table 1.6 List of Pin and Pin Functions (176-Pin LQFP) (4/5)

| Pin Number | Power Supply Clock System Control | I/O Port | Bus EXDMAC SDRAMC | Timer (MTU, TPU, TMR, PPG, RTC, POE) | Communications (ETHERC, SCIC, SCID, RSPI, RIIC, CAN, IEB, USB, and PDC) | Interrupt | S12AD, AD, DA |
|------------|---|----------|-------------------------|---|--|-----------|------------------|
| 100 | | PB1 | A9 | MTIOC0C/MTIOC4C/ TIOCB3/TMCI0/PO25 | ET_ERXD0/RMII_RXD0/ TXD4/TXD6/SMOSI4/ SMOSI6/SSDA4/SSDA6 | IRQ4-DS | |
| 101 | | P72 | CS2# | | ET_MDC | | |
| 102 | | P71 | CS1# | | ET_MDIO | | |
| 103 | VCC | | | | | | |
| 104 | | PB0 | A8 | MTIC5W/TIOCA3/PO24 | ET_ERXD1/RMII_RXD1/ RXD4/RXD6/SMISO4/ SMISO6/SSCL4/SSCL6/ RSPCKA | IRQ12 | |
| 105 | VSS | | | | | | |
| 106 | | PA7 | A7 | TIOCB2/PO23 | ET_WOL/MISOA | | |
| 107 | | PA6 | A6 | MTIC5V/MTCLKB/ TIOCA2/TMCI3/PO22/ POE2# | ET_EXOUT/CTS5#/ RTS5#/SS5#/MOSIA | | |
| 108 | | PA5 | A5 | TIOCB1/PO21 | ET_LINKSTA/RSPCKA | | |
| 109 | | PA4 | A4 | MTIC5U/MTCLKA/ TIOCA1/TMRI0/PO20 | ET_MDC/TXD5/SMOSI5/ SSDA5/SSLA0 | IRQ5-DS | |
| 110 | | PA3 | A3 | MTIOC0D/MTCLKD/ TIOCD0/TCLKB/PO19 | ET_MDIO/RXD5/SMISO5/ SSCL5 | IRQ6-DS | |
| 111 | TRDATA3 | PG7 | D31 | | | | |
| 112 | | PA2 | A2 | PO18 | RXD5/SMISO5/SSCL5/ SSLA3 | | |
| 113 | TRDATA2 | PG6 | D30 | | | | |
| 114 | | PA1 | A1/DQM3 | MTIOC0B/MTCLKC/ TIOCB0/PO17 | ET_WOL/SCK5/SSLA2 | IRQ11 | |
| 115 | VCC | | | | | | |
| 116 | TRCLK | PG5 | D29 | | | | |
| 117 | VSS | | | | | | |
| 118 | | PA0 | A0/BC0#/DQM2 | MTIOC4A/TIOCA0/PO16 | ET_TX_EN/ RMII_TXD_EN/SSLA1 | | |
| 119 | TRSYNC | PG4 | D28 | | | | |
| 120 | | P67 | CS7#/DQM1 | | CRX2*2 | IRQ15 | |
| 121 | TRDATA1 | PG3 | D27 | | | | |
| 122 | | P66 | CS6#/DQM0 | | CTX2*2 | | |
| 123 | TRDATA0 | PG2 | D26 | | | | |
| 124 | | P65 | CS5#/CKE | | | | |
| 125 | | PE7 | D15[A15/D15] | TIOCB11 | MISOB | IRQ7 | AN5 |
| 126 | | PE6 | D14[A14/D14] | TIOCA11 | MOSIB | IRQ6 | AN4 |
| 127 | VCC | | | | | | |
| 128 | SDCLK | P70 | | | | | |
| 129 | VSS | | | | | | |
| 130 | | PE5 | D13[A13/D13] | MTIOC4C/MTIOC2B/ TIOCB10 | ET_RX_CLK/REF50CK/ RSPCKB | IRQ5 | AN3 |
| 131 | | PE4 | D12[A12/D12] | MTIOC4D/MTIOC1A/ TIOCA10/PO28 | ET_ERXD2/SSLB0 | | AN2 |
| 132 | | PE3 | D11[A11/D11] | MTIOC4B/TIOCB9/PO26/ POE8# | ET_ERXD3/CTS12#/ RTS12#/SS12#/MISOB | | AN1 |
| 133 | | PE2 | D10[A10/D10] | MTIOC4A/TIOCA9/PO23 | RXD12/SMISO12/ SSCL12/RXD12/SSLB3/ MOSIB | IRQ7-DS | AN0 |
| 134 | | PE1 | D9[A9/D9] | MTIOC4C/TIOCD9/PO18 | TXD12/SMOSI12/ SSDA12/TXD12/ SIOX12/SSLB2/RSPCKB | | ANEX1 |
| 135 | | PE0 | D8[A8/D8] | TIOCC9 | SCK12/SSLB1 | | ANEX0 |

Table 1.6 List of Pin and Pin Functions (176-Pin LQFP) (5/5)

| Pin Number 176-Pin LQFP | Power Supply Clock System Control | I/O Port | Bus EXDMAC SDRAMC | Timer (MTU, TPU, TMR, PPG, RTC, POE) | Communications (ETHERC, SCIC, SCID, RSPI, RIIC, CAN, IEB, USB, and PDC) | Interrupt | S12AD, AD, DA |
|-------------------------------|---|----------|-------------------------|--|--|-----------|------------------|
| 136 | | P64 | CS4#/WE# | | | | |
| 137 | | P63 | CS3#/CAS# | | | | |
| 138 | | P62 | CS2#/RAS# | | | | |
| 139 | | P61 | CS1#/SDCS# | | | | |
| 140 | VSS | | | | | | |
| 141 | | P60 | CS0# | | | | |
| 142 | VCC | | | | | | |
| 143 | | PD7 | D7[A7/D7] | MTIC5U/POE0# | SSLC3 | IRQ7 | AN7 |
| 144 | | PG1 | D25 | | | | |
| 145 | | PD6 | D6[A6/D6] | MTIC5V/POE1# | SSLC2 | IRQ6 | AN6 |
| 146 | | PG0 | D24 | | | | |
| 147 | | PD5 | D5[A5/D5] | MTIC5W/POE2# | SSLC1 | IRQ5 | AN013 |
| 148 | | PD4 | D4[A4/D4] | POE3# | SSLC0 | IRQ4 | AN012 |
| 149 | | P97 | A23/D23 | | | | |
| 150 | | PD3 | D3[A3/D3] | TIOCB8/TCLKH/POE8# | RSPCKC | IRQ3 | AN011 |
| 151 | VSS | | | | | | |
| 152 | | P96 | A22/D22 | | | | |
| 153 | VCC | | | | | | |
| 154 | | PD2 | D2[A2/D2] | MTIOC4D/TIOCA8 | MISOC/CRX0 | IRQ2 | AN010 |
| 155 | | P95 | A21/D21 | | | | |
| 156 | | PD1 | D1[A1/D1] | MTIOC4B/TIOCB7/ TCLKG | MOSIC/CTX0 | IRQ1 | AN009 |
| 157 | | P94 | A20/D20 | | | | |
| 158 | | PD0 | D0[A0/D0] | TIOCA7 | | IRQ0 | AN008 |
| 159 | | P93 | A19/D19 | | CTS7#/RTS7#/SS7# | | AN017 |
| 160 | | P92 | A18/D18 | | RXD7/SMISO7/SSCL7 | | AN016 |
| 161 | | P91 | A17/D17 | | SCK7 | | AN015 |
| 162 | VSS | | | | | | |
| 163 | | P90 | A16/D16 | | TXD7/SMOSI7/SSDA7 | | AN014 |
| 164 | VCC | | | | | | |
| 165 | | P47 | | | | IRQ15-DS | AN007 |
| 166 | | P46 | | | | IRQ14-DS | AN006 |
| 167 | | P45 | | | | IRQ13-DS | AN005 |
| 168 | | P44 | | | | IRQ12-DS | AN004 |
| 169 | | P43 | | | | IRQ11-DS | AN003 |
| 170 | | P42 | | | | IRQ10-DS | AN002 |
| 171 | | P41 | | | | IRQ9-DS | AN001 |
| 172 | VREFLO | | | | | | |
| 173 | | P40 | | | | IRQ8-DS | AN000 |
| 174 | VREFH0 | | | | | | |
| 175 | AVCC0 | | | | | | |
| 176 | | P07 | | | | IRQ15 | ADTRG0# |

Note 1. The BCLK function is multiplexed with the I/O port function for pin P53, so the port function is not available if the external bus is enabled.

Note 2. Enabled only for the ROM capacity: 2 Mbytes/1.5 Mbytes

Table 1.7 List of Pins and Pin Functions (145-Pin TFLGA) (1/5)

| Pin No. 145-pin TFLGA | Power Supply Clock System Control | I/O Port | Bus EXDMAC SDRAMC | Timers (MTU, TPU, TMR, PPG, RTC, POE) | Communications (ETHERC, SClc, SClD, RSPI, RIIC, CAN, IEB, USB, and PDC) | Interrupt | S12AD AD DA |
|-----------------------------|---|----------|-------------------------|---|--|-----------|-------------------|
| A1 | AVSS0 | | | | | | |
| A2 | | P07 | | | | IRQ15 | ADTRG0# |
| A3 | | P40 | | | | IRQ8-DS | AN000 |
| A4 | | P42 | | | | IRQ10-DS | AN002 |
| A5 | | P45 | | | | IRQ13-DS | AN005 |
| A6 | | P90 | A16 | | TXD7/SMOSI7/SSDA7 | | AN014 |
| A7 | | P92 | A18 | | RXD7/SMISO7/SSCL7 | | AN016 |
| A8 | | PD2 | D2[A2/D2] | MTIOC4D/TIOCA8 | MISOC/CRX0 | IRQ2 | AN010 |
| A9 | | PD6 | D6[A6/D6] | MTIC5V/POE1# | SSLC2 | IRQ6 | AN6 |
| A10 | VSS | | | | | | |
| A11 | | P62 | CS2#/RAS# | | | | |
| A12 | | PE1 | D9[A9/D9] | MTIOC4C/TIOCD9/ PO18 | TXD12/SMOSI12/SSDA12/ TXDX12/SIOX12/SSLB2/ RSPCKB | | ANEX1 |
| A13 | | PE3 | D11[A11/D11] | MTIOC4B/TIOCB9/ PO26/POE8# | CTS12#/RTS12#/SS12#/ MISOB/ET_ERXD3 | | AN1 |
| B1 | VREFH | | | | | | |
| B2 | AVCC0 | | | | | | |
| B3 | | P05 | | | | IRQ13 | DA1 |
| B4 | VREFL0 | | | | | | |
| B5 | | P43 | | | | IRQ11-DS | AN003 |
| B6 | | P47 | | | | IRQ15-DS | AN007 |
| B7 | | P91 | A17 | | SCK7 | | AN015 |
| B8 | | PD0 | D0[A0/D0] | TIOCA7 | | IRQ0 | AN008 |
| B9 | | PD4 | D4[A4/D4] | POE3# | SSLC0 | IRQ4 | AN012 |
| B10 | VCC | | | | | | |
| B11 | | P61 | CS1#/SDCS# | | | | |
| B12 | | PE2 | D10[A10/D10] | MTIOC4A/TIOCA9/ PO23 | RXD12/SMISO12/SSCL12/ RXDX12/SSLB3/MOSIB | IRQ7-DS | AN0 |
| B13 | | PE4 | D12[A12/D12] | MTIOC4D/MTIOC1A/ TIOCA10/PO28 | SSLB0/ET_ERXD2 | | AN2 |
| C1 | VREFL | | | | | | |
| C2 | | P02 | | TMC11 | SCK6 | IRQ10 | AN020 |
| C3 | VREFH0 | | | | | | |
| C4 | | P41 | | | | IRQ9-DS | AN001 |
| C5 | | P46 | | | | IRQ14-DS | AN006 |
| C6 | VSS | | | | | | |
| C7 | | PD1 | D1[A1/D1] | MTIOC4B/TIOCB7/ TCLKG | MOSIC/CTX0 | IRQ1 | AN009 |
| C8 | | PD3 | D3[A3/D3] | TIOCB8/TCLKH/POE8# | RSPCKC | IRQ3 | AN011 |
| C9 | | PD7 | D7[A7/D7] | MTIC5U/POE0# | SSLC3 | IRQ7 | AN7 |
| C10 | | P63 | CS3#/CAS# | | | | |
| C11 | | PE0 | D8[A8/D8] | TIOCC9 | SCK12/SSLB1 | | ANEX0 |
| C12 | SDCLK | P70 | | | | | |
| C13 | VSS | | | | | | |
| D1 | | P00 | | TMRI0 | TXD6/SMOSI6/SSDA6 | IRQ8 | AN018 |
| D2 | | PF5 | | | | IRQ4 | |
| D3 | | P03 | | | | IRQ11 | DA0 |
| D4 | | P01 | | TMC10 | RXD6/SMISO6/SSCL6 | IRQ9 | AN019 |

Table 1.7 List of Pins and Pin Functions (145-Pin TFLGA) (2/5)

| Pin No. 145-pin TFLGA | Power Supply Clock System Control | I/O Port | Bus EXDMAC SDRAMC | Timers (MTU, TPU, TMR, PPG, RTC, POE) | Communications (ETHERC, SClc, SClD, RSPI, RIIC, CAN, IEB, USB, and PDC) | Interrupt | S12AD AD DA |
|-----------------------------|---|----------|-------------------------|---|--|-----------|-------------------|
| D5 | VCC | | | | | | |
| D6 | | P93 | A19 | | CTS7#/RTS7#/SS7# | | AN017 |
| D7 | | PD5 | D5[A5/D5] | MTIC5W/POE2# | SSLC1 | IRQ5 | AN013 |
| D8 | | P60 | CS0# | | | | |
| D9 | | P64 | CS4#/WE# | | | | |
| D10 | | PE7 | D15[A15/D15] | TIOCB11 | MISOB | IRQ7 | AN5 |
| D11 | VCC | | | | | | |
| D12 | | PE5 | D13[A13/D13] | MTIOC4C/MTIOC2B/ TIOCB10 | RSPCKB/ET_RX_CLK/ REF50CK | IRQ5 | AN3 |
| D13 | | PE6 | D14[A14/D14] | TIOCA11 | MOSIB | IRQ6 | AN4 |
| E1 | VSS | | | | | | |
| E2 | VCL | | | | | | |
| E3 | | PJ5 | | | | | |
| E4 | EMLE | | | | | | |
| E5 | | P44 | | | | IRQ12-DS | AN004 |
| E10 | | PA0 | A0/BC0# | MTIOC4A/TIOCA0/ PO16 | SSLA1/ET_TX_EN/ RMII_TXD_EN | | |
| E11 | | P66 | CS6#/DQM0 | | CTX2*2 | | |
| E12 | | P65 | CS5#/CKE | | | | |
| E13 | | P67 | CS7#/DQM1 | | CRX2*2 | IRQ15 | |
| F1 | XCIN | | | | | | |
| F2 | XCOUT | | | | | | |
| F3 | | PJ3 | | MTIOC3C | CTS6#/RTS6#/CTS0#/ RTS0#/SS6#/SS0# | | |
| F4 | VBATT | | | | | | |
| F10 | | PA3 | A3 | MTIOC0D/MTCLKD/ TIOC0D/TCLKB/PO19 | RXD5/SMISO5/SSCL5/ ET_MDIO | IRQ6-DS | |
| F11 | VSS | | | | | | |
| F12 | | PA1 | A1 | MTIOC0B/MTCLKC/ TIOCB0/PO17 | SCK5/SSLA2/ET_WOL | IRQ11 | |
| F13 | | PA2 | A2 | PO18 | RXD5/SMISO5/SSCL5/ SSLA3 | | |
| G1 | XTAL | P37 | | | | | |
| G2 | RES# | | | | | | |
| G3 | MD/FINED | | | | | | |
| G4 | BSCANP | | | | | | |
| G10 | | PA5 | A5 | TIOCB1/PO21 | RSPCKA/ET_LINKSTA | | |
| G11 | | PA6 | A6 | MTIC5V/MTCLKB/ TIOCA2/TMCI3/PO22/ POE2# | CTS5#/RTS5#/SS5# MOSIA/ET_EXOUT | | |
| G12 | VCC | | | | | | |
| G13 | | PA4 | A4 | MTIC5U/MTCLKA/ TIOCA1/TMRI0/PO20 | TXD5/SMOSI5/SSDA5/ SSLA0/ET_MDC | IRQ5-DS | |
| H1 | EXTAL | P36 | | | | | |
| H2 | VCC | | | | | | |
| H3 | VSS | | | | | | |
| H4 | | P35 | | | | NMI | |
| H10 | | P72 | CS2# | | ET_MDC | | |
| H11 | | P71 | CS1# | | ET_MDIO | | |

Table 1.7 List of Pins and Pin Functions (145-Pin TFLGA) (3/5)

| Pin No. 145-pin TFLGA | Power Supply Clock System Control | I/O Port | Bus EXDMAC SDRAMC | Timers (MTU, TPU, TMR, PPG, RTC, POE) | Communications (ETHERC, SClc, SClD, RSPI, RIIC, CAN, IEB, USB, and PDC) | Interrupt | S12AD AD DA |
|-----------------------------|---|----------|-------------------------|--|--|-----------|-------------------|
| H12 | | PB0 | A8 | MTI0C5W/TIOCA3/PO24 | RXD4/RXD6/SMISO4/ SMISO6/SSCL4/SSCL6/ RSPCKA/T_ERXD1/ RMII_RXD1 | IRQ12 | |
| H13 | | PA7 | A7 | TIOCB2/PO23 | MISOA/ET_WOL | | |
| J1 | TRST# | P34 | | MTI0C0A/TMCI3/PO12/ POE2# | SCK6/SCK0/ USB0_DPRPD | IRQ4 | |
| J2 | | P33 | | MTI0C0D/TIOCD0/ TMR13/PO11/POE3# | RXD6/RXD0/SMISO6/ SMISO0/SSCL6/SSCL0/ CRX0/PCKO | IRQ3-DS | |
| J3 | | P32 | | MTI0C0C/TIOCC0/ TMO3/PO10/RTCOU/ RTCIC2 | TXD6/TXD0/SMOSI6/ SMOSI0/SSDA6/SSDA0/ CTX0/USB0_VBUSEN/ VSYNC | IRQ2-DS | |
| J4 | TDI | P30 | | MTI0C4B/TMR13/PO8/ RTCIC0/POE8# | RXD1/SMISO1/SSCL1/ MISOB/USB0_DRPD | IRQ0-DS | |
| J10 | | PB3 | A11 | MTI0C0A/MTI0C4A/ TIOCD3/TCLKD/TMO0/ PO27/POE3# | SCK4/SCK6/ET_RX_ER/ RMII_RX_ER | | |
| J11 | | PB4 | A12 | TIOCA4/PO28 | CTS9#/RTS9#/SS9#/ ET_TX_EN/RMII_TXD_EN | | |
| J12 | | PB2 | A10 | TIOCC3/TCLKC/PO26 | CTS4#/RTS4#/CTS6#/ RTS6#/SS4#/SS6#/ ET_RX_CLK/REF50CK | | |
| J13 | | PB1 | A9 | MTI0C0C/MTI0C4C/ TIOCB3/TMCI0/PO25 | TXD4/TXD6/SMOSI4/ SMOSI6/SSDA4/SSDA6/ ET_ERXD0/RMII_RXD0 | IRQ4-DS | |
| K1 | TCK/FINEC | P27 | CS7# | MTI0C2B/TMCI3/PO7 | SCK1/RSPCKB | | |
| K2 | TDO | P26 | CS6# | MTI0C2A/TMO1/PO6 | TXD1/CTS3#/RTS3#/ SMOSI1/SS3#/SSDA1/ MOSIB | | |
| K3 | TMS | P31 | | MTI0C4D/TMCI2/PO9/ RTCIC1 | CTS1#/RTS1#/SS1#/ SSLB0/USB0_DPUPE | IRQ1-DS | |
| K4 | | P15 | | MTI0C0B/MTCLKB/ TIOCB2/TCLKB/TMCI2/ PO13 | RXD1/SCK3/SMISO1/ SSCL1/CRX1-DS/PIXD0 | IRQ5 | |
| K5 | TRDATA2 | P54 | ALE/EDACK0 | MTI0C4B/TMCI1 | CTS2#/RTS2#/SS2#/ CTX1/ET_LINKSTA | | |
| K6 | | P53*1 | BCLK | | | | |
| K7 | | P51 | WR1#/BC1#/ WAIT# | | SCK2/SSLB2 | | |
| K8 | VCC | | | | | | |
| K9 | TRDATA0 | P80 | EDREQ0 | MTI0C3B/PO26 | SCK10/ET_TX_EN/ RMII_TXD_EN | | |
| K10 | | P76 | CS6# | PO22 | RXD11/SMISO11/SSCL11/ ET_RX_CLK/REF50CK | | |
| K11 | | PB7 | A15 | MTI0C3B/TIOCB5/ PO31 | TXD9/SMOSI9/SSDA9/ ET_CRS/RMII_CRS_DV | | |
| K12 | | PB6 | A14 | MTI0C3D/TIOCA5/ PO30 | RXD9/SMISO9/SSCL9/ ET_ETXD1/RMII_TXD1 | | |
| K13 | | PB5 | A13 | MTI0C2A/MTI0C1B/ TIOCB4/TMR11/PO29/ POE1# | SCK9/ET_ETXD0/ RMII_TXD0 | | |
| L1 | | P25 | CS5#/EDACK1 | MTI0C4C/MTCLKB/ TIOCA4/PO5 | RXD3/SMISO3/SSCL3/ USB0_DPRPD/HSYNC | | ADTRG0# |
| L2 | | P23 | EDACK0 | MTI0C3D/MTCLKD/ TIOCD3/PO3 | TXD3/CTS0#/RTS0#/ SMOSI3/SS0#/SSDA3/ USB0_DPUPE/PIXD7 | | |

Table 1.7 List of Pins and Pin Functions (145-Pin TFLGA) (4/5)

| Pin No. 145-pin TFLGA | Power Supply Clock System Control | I/O Port | Bus EXDMAC SDRAMC | Timers (MTU, TPU, TMR, PPG, RTC, POE) | Communications (ETHERC, SClc, SClD, RSPI, RIIC, CAN, IEB, USB, and PDC) | Interrupt | S12AD AD DA |
|-----------------------------|---|----------|-------------------------|--|---|-----------|-------------------|
| L3 | | P16 | | MTIOC3C/MTIOC3D/ TIOCB1/TCLKC/TMO2/ PO14/RTCOU | TXD1/RXD3/SMOSI1/ SMISO3/SSDA1/SSCL3/ MOSIA/SCL2-DS/IERXD/ USB0_VBUS/ USB0_VBUSE/ USB0_OVRCURB | IRQ6 | ADTRG0# |
| L4 | | P24 | CS4#/EDREQ1 | MTIOC4A/MTCLKA/ TIOCB4/TMRI1/PO4 | SCK3/USB0_VBUSE/ PIXCLK | | |
| L5 | | P13 | | MTIOC0B/TIOCA5/ TMO3/PO13 | TXD2/SMOSI2/SSDA2/ SDA0[FM+] | IRQ3 | ADTRG# |
| L6 | | P56 | EDACK1 | MTIOC3C/TIOCA1 | | | |
| L7 | | P52 | RD# | | RXD2/SMISO2/SSCL2/ SSLB3 | | |
| L8 | TRCLK | P83 | EDACK1 | MTIOC4C | CTS10#/RTS10#/SS10#/ ET_CRS/RMII_CRS_DV | | |
| L9 | | PC5 | A21/CS2#/ WAIT# | MTIOC3B/MTCLKD/ TIOCD6/TCLKF/TMRI2/ PO29 | SCK8/RSPCKA/ ET_ETXD2 | | |
| L10 | | PC4 | A20/CS3# | MTIOC3D/MTCLKC/ TIOCC6/TCLKE/TMC11/ PO25/POE0# | SCK5/CTS8#/RTS8#/ SS8#/SSLA0/ET_TX_CLK | | |
| L11 | | PC2 | A18 | MTIOC4B/TCLKA/PO21 | RXD5/SMISO5/SSCL5/ SSLA3/IERXD/ET_RX_DV | | |
| L12 | | P73 | CS3# | PO16 | ET_WOL | | |
| L13 | VSS | | | | | | |
| M1 | | P22 | EDREQ0 | MTIOC3B/MTCLKC/ TIOCC3/TMO0/PO2 | SCK0/USB0_DRPD/PIXD6 | | |
| M2 | | P17 | | MTIOC3A/MTIOC3B/ TIOCB0/TCLKD/TMO1/ PO15/POE8# | SCK1/TXD3/SMOSI3/ SSDA3/MISOA/SDA2-DS/ IETXD/PIXD3 | IRQ7 | ADTRG# |
| M3 | | P86 | | TIOCA0 | PIXD1 | | |
| M4 | | P12 | | TMC11 | RXD2/SMISO2/SSCL2/ SCL0[FM+] | IRQ2 | |
| M5 | VCC_USB | | | | | | |
| M6 | VSS_USB | | | | | | |
| M7 | | P50 | WR0#/WR# | | TXD2/SMOSI2/SSDA2/ SSLB1 | | |
| M8 | | PC6 | A22/CS1# | MTIOC3C/MTCLKA/ TIOCA6/TMC12/PO30 | RXD8/SMISO8/SSCL8/ MOSIA/ET_ETXD3 | IRQ13 | |
| M9 | TRDATA1 | P81 | EDACK0 | MTIOC3D/PO27 | RXD10/SMISO10/SSCL10/ ET_ETXD0/RMII_TXD0 | | |
| M10 | | P77 | CS7# | PO23 | TXD11/SMOSI11/SSDA11/ ET_RX_ER/RMII_RX_ER | | |
| M11 | | PC0 | A16 | MTIOC3C/TCLKC/PO17 | CTS5#/RTS5#/SS5#/ SSLA1/SCL3/ET_ERXD3 | IRQ14 | |
| M12 | | PC1 | A17 | MTIOC3A/TCLKD/PO18 | SCK5/SSLA2/SDA3/ ET_ERXD2 | IRQ12 | |
| M13 | VCC | | | | | | |
| N1 | | P21 | | MTIOC1B/TIOCA3/ TMC10/PO1 | RXD0/SMISO0/SSCL0/ SCL1/USB0_EXICEN/ PIXD5 | IRQ9 | |
| N2 | | P20 | | MTIOC1A/TIOCB3/ TMRI0/PO0 | TXD0/SMOSI0/SSDA0/ SDA1/USB0_ID/PIXD4 | IRQ8 | |
| N3 | | P87 | | TIOCA2 | PIXD2 | | |
| N4 | | P14 | | MTIOC3A/MTCLKA/ TIOCB5/TCLKA/TMRI2/ PO15 | CTS1#/RTS1#/SS1#/ CTX1/USB0_DPUPE/ USB0_OVRCURA | IRQ4 | |
| N5 | | | | | USB0_DM | | |
| N6 | | | | | USB0_DP | | |

Table 1.7 List of Pins and Pin Functions (145-Pin TFLGA) (5/5)

| Pin No. 145-pin TFLGA | Power Supply Clock System Control | I/O Port | Bus EXDMAC SDRAMC | Timers (MTU, TPU, TMR, PPG, RTC, POE) | Communications (ETHERC, SC1c, SC1d, RSPI, RIIC, CAN, IEB, USB, and PDC) | Interrupt | S12AD AD DA |
|-----------------------------|---|----------|-------------------------|---|--|-----------|-------------------|
| N7 | TRDATA3 | P55 | WAIT#/ EDREQ0 | MTIOC4D/TMO3 | CRX1/ET_EXOUT | IRQ10 | |
| N8 | VSS | | | | | | |
| N9 | | PC7 | A23/CS0# | MTIOC3A/MTCLKB/ TIOCB6/TMO2/PO31 | TXD8/SMOSI8/SSDA8/ MISOA/ET_COL | IRQ14 | |
| N10 | TRSYNC | P82 | EDREQ1 | MTIOC4A/PO28 | TXD10/SMOSI10/SSDA10/ ET_ETXD1/RMII_TXD1 | | |
| N11 | | PC3 | A19 | MTIOC4D/TCLKB/PO24 | TXD5/SMOSI5/SSDA5/ IETXD/ET_TX_ER | | |
| N12 | | P75 | CS5# | PO20 | SCK11/ET_ERXD0/ RMII_RXD0 | | |
| N13 | | P74 | CS4# | PO19 | CTS11#/RTS11#/SS11#/ ET_ERXD1/RMII_RXD1 | | |

Note 1. The BCLK function is multiplexed with the I/O port function for pin P53, so the port function is not available if the external bus is enabled.

Note 2. Enabled only for the ROM capacity: 2 Mbytes/1.5 Mbytes

Table 1.8 List of Pins and Pin Functions (144-Pin LQFP) (1/5)

| Pin No. 144-pin LQFP | Power Supply Clock System Control | I/O Port | Bus EXDMAC SDRAMC | Timers (MTU, TPU, TMR, PPG, RTC, POE) | Communications (ETHERC, SClc, SClD, RSPI, RIIC, CAN, IEB, USB, and PDC) | Interrupt | S12AD AD DA |
|----------------------------|---|----------|-------------------------|--|--|-----------|-------------------|
| 1 | AVSS0 | | | | | | |
| 2 | | P05 | | | | IRQ13 | DA1 |
| 3 | VREFH | | | | | | |
| 4 | | P03 | | | | IRQ11 | DA0 |
| 5 | VREFL | | | | | | |
| 6 | | P02 | | TMC11 | SCK6 | IRQ10 | AN020 |
| 7 | | P01 | | TMC10 | RXD6/SMISO6/SSCL6 | IRQ9 | AN019 |
| 8 | | P00 | | TMR10 | TXD6/SMOSI6/SSDA6 | IRQ8 | AN018 |
| 9 | | PF5 | | | | IRQ4 | |
| 10 | EMLE | | | | | | |
| 11 | | PJ5 | | | | | |
| 12 | VSS | | | | | | |
| 13 | | PJ3 | | MTIOC3C | CTS6#/RTS6#/CTS0/ RTS0#/SS6#/SS0# | | |
| 14 | VCL | | | | | | |
| 15 | VBATT | | | | | | |
| 16 | MD/FINED | | | | | | |
| 17 | XCIN | | | | | | |
| 18 | XCOUT | | | | | | |
| 19 | RES# | | | | | | |
| 20 | XTAL | P37 | | | | | |
| 21 | VSS | | | | | | |
| 22 | EXTAL | P36 | | | | | |
| 23 | VCC | | | | | | |
| 24 | | P35 | | | | NMI | |
| 25 | TRST# | P34 | | MTIOC0A/TMC13/ PO12/POE2# | SCK6/SCK0/ USB0_DPRPD | IRQ4 | |
| 26 | | P33 | | MTIOC0D/TIOC0D/ TMR13/PO11/POE3# | RXD6/RXD0/SMISO6/ SMISO0/SSCL6/ SSCL0/CRX0/PCKO | IRQ3-DS | |
| 27 | | P32 | | MTIOC0C/TIOC0C/ TMO3/PO10/RTCOUT/ RTCIC2 | TXD6/TXD0/SMOSI6/ SMOSI0/SSDA6/ SSDA0/CTX0/ USB0_VBUSEN/ VSYNC | IRQ2-DS | |
| 28 | TMS | P31 | | MTIOC4D/TMC12/PO9/ RTCIC1 | CTS1#/RTS1#/SS1#/ SSLB0/USB0_DPUPE | IRQ1-DS | |
| 29 | TDI | P30 | | MTIOC4B/TMR13/PO8/ RTCIC0/POE8# | RXD1/SMISO1/SSCL1/ MISOB/USB0_DRPD | IRQ0-DS | |
| 30 | TCK/FINEC | P27 | CS7# | MTIOC2B/TMC13/PO7 | SCK1/RSPCKB | | |
| 31 | TDO | P26 | CS6# | MTIOC2A/TMO1/PO6 | TXD1/CTS3#/RTS3#/ SMOSI1/SS3#/SSDA1/ MOSIB | | |
| 32 | | P25 | CS5#/EDACK1 | MTIOC4C/MTCLKB/ TIOCA4/PO5 | RXD3/SMISO3/SSCL3/ USB0_DPRPD/HSYNC | | ADTRG0# |
| 33 | | P24 | CS4#/EDREQ1 | MTIOC4A/MTCLKA/ TIOCB4/TMR11/PO4 | SCK3/USB0_VBUSEN/ PIXCLK | | |
| 34 | | P23 | EDACK0 | MTIOC3D/MTCLKD/ TIOC3D/PO3 | TXD3/CTS0#/RTS0#/ SMOSI3/SS0#/SSDA3/ USB0_DPUPE/PIXD7 | | |
| 35 | | P22 | EDREQ0 | MTIOC3B/MTCLKC/ TIOC3B/TMO0/PO2 | SCK0/USB0_DRPD/ PIXD6 | | |

Table 1.8 List of Pins and Pin Functions (144-Pin LQFP) (2/5)

| Pin No. | Power Supply Clock System Control | I/O Port | Bus EXDMAC SDRAMC | Timers (MTU, TPU, TMR, PPG, RTC, POE) | Communications (ETHERC, SClc, SClD, RSPI, RIIC, CAN, IEB, USB, and PDC) | Interrupt | S12AD AD DA |
|---------|---|----------|-------------------------|---|--|-----------|-------------------|
| 36 | | P21 | | MTIOC1B/TIOCA3/ TMC10/PO1 | RXD0/SMISO0/SSCL0/ SCL1/USB0_EXICEN/ PIXD5 | IRQ9 | |
| 37 | | P20 | | MTIOC1A/TIOCB3/ TMR10/PO0 | TXD0/SMOSI0/SSDA0/ SDA1/USB0_ID/PIXD4 | IRQ8 | |
| 38 | | P17 | | MTIOC3A/MTIOC3B/ TIOCB0/TCLKD/TMO1/ PO15/POE8# | SCK1/TXD3/SMOSI3/ SSDA3/MISOA/SDA2- DS/IETXD/PIXD3 | IRQ7 | ADTRG# |
| 39 | | P87 | | TIOCA2 | PIXD2 | | |
| 40 | | P16 | | MTIOC3C/MTIOC3D/ TIOCB1/TCLKC/TMO2/ PO14/RTCOUT | TXD1/RXD3/SMOSI1/ SMISO3/SSDA1/ SSCL3/MOSIA/SCL2- DS/IERXD/ USB0_VBUS/ USB0_VBUSEN/ USB0_OVRCURB | IRQ6 | ADTRG0# |
| 41 | | P86 | | TIOCA0 | PIXD1 | | |
| 42 | | P15 | | MTIOC0B/MTCLKB/ TIOCB2/TCLKB/ TMC12/PO13 | RXD1/SCK3/SMISO1/ SSCL1/CRX1-DS/ PIXD0 | IRQ5 | |
| 43 | | P14 | | MTIOC3A/MTCLKA/ TIOCB5/TCLKA/ TMR12/PO15 | CTS1#/RTS1#/SS1#/ CTX1/USB0_DPUPE/ USB0_OVRCURA | IRQ4 | |
| 44 | | P13 | | MTIOC0B/TIOCA5/ TMO3/PO13 | TXD2/SMOSI2/SSDA2/ SDA0[FM+] | IRQ3 | ADTRG# |
| 45 | | P12 | | TMC11 | RXD2/SMISO2/SSCL2/ SCL0[FM+] | IRQ2 | |
| 46 | VCC_USB | | | | | | |
| 47 | | | | | USB0_DM | | |
| 48 | | | | | USB0_DP | | |
| 49 | VSS_USB | | | | | | |
| 50 | | P56 | EDACK1 | MTIOC3C/TIOCA1 | | | |
| 51 | TRDATA3 | P55 | WAIT#/ EDREQ0 | MTIOC4D/TMO3 | CRX1/ET_EXOUT | IRQ10 | |
| 52 | TRDATA2 | P54 | ALE/EDACK0 | MTIOC4B/TMC11 | CTS2#/RTS2#/SS2#/ CTX1/ET_LINKSTA | | |
| 53 | | P53*1 | BCLK | | | | |
| 54 | | P52 | RD# | | RXD2/SMISO2/SSCL2/ SSLB3 | | |
| 55 | | P51 | WR1#/BC1#/ WAIT# | | SCK2/SSLB2 | | |
| 56 | | P50 | WRO#/WR# | | TXD2/SMOSI2/SSDA2/ SSLB1 | | |
| 57 | VSS | | | | | | |
| 58 | TRCLK | P83 | EDACK1 | MTIOC4C | CTS10#/RTS10#/ SS10#/ET_CRS/ RMII_CRS_DV | | |
| 59 | VCC | | | | | | |
| 60 | | PC7 | A23/CS0# | MTIOC3A/MTCLKB/ TIOCB6/TMO2/PO31 | TXD8/SMOSI8/SSDA8/ MISOA/ET_COL | IRQ14 | |
| 61 | | PC6 | A22/CS1# | MTIOC3C/MTCLKA/ TIOCA6/TMC12/PO30 | RXD8/SMISO8/SSCL8/ MOSIA/ET_ETXD3 | IRQ13 | |
| 62 | | PC5 | A21/CS2#/ WAIT# | MTIOC3B/MTCLKD/ TIOCD6/TCLKF/ TMR12/PO29 | SCK8/RSPCKA/ ET_ETXD2 | | |
| 63 | TRSYNC | P82 | EDREQ1 | MTIOC4A/PO28 | TXD10/SMOSI10/ SSDA10/ET_ETXD1/ RMII_TXD1 | | |

Table 1.8 List of Pins and Pin Functions (144-Pin LQFP) (3/5)

| Pin No. | Power Supply Clock System Control | I/O Port | Bus EXDMAC SDRAMC | Timers (MTU, TPU, TMR, PPG, RTC, POE) | Communications (ETHERC, SClc, SClD, RSPI, RIIC, CAN, IEB, USB, and PDC) | Interrupt | S12AD AD DA |
|---------|---|----------|-------------------------|--|--|-----------|-------------------|
| 64 | TRDATA1 | P81 | EDACK0 | MTIOC3D/PO27 | RXD10/SMISO10/ SSCL10/ET_ETXD0/ RMII_TXD0 | | |
| 65 | TRDATA0 | P80 | EDREQ0 | MTIOC3B/PO26 | SCK10/ET_TX_EN/ RMII_TXD_EN | | |
| 66 | | PC4 | A20/CS3# | MTIOC3D/MTCLKC/ TIOCC6/TCLKE/ TMCI1/PO25/POE0# | SCK5/CTS8#/RTS8#/ SS8#/SSLA0/ ET_TX_CLK | | |
| 67 | | PC3 | A19 | MTIOC4D/TCLKB/ PO24 | TXD5/SMOSI5/SSDA5/ IETXD/ET_TX_ER | | |
| 68 | | P77 | CS7# | PO23 | TXD11/SMOSI11/ SSDA11/ET_RX_ER/ RMII_RX_ER | | |
| 69 | | P76 | CS6# | PO22 | RXD11/SMISO11/ SSCL11/ET_RX_CLK/ REF50CK | | |
| 70 | | PC2 | A18 | MTIOC4B/TCLKA/ PO21 | RXD5/SMISO5/SSCL5/ SSLA3/IERXD/ ET_RX_DV | | |
| 71 | | P75 | CS5# | PO20 | SCK11/ET_ERXD0/ RMII_RXD0 | | |
| 72 | | P74 | CS4# | PO19 | CTS11#/RTS11#/ SS11#/ET_ERXD1/ RMII_RXD1 | | |
| 73 | | PC1 | A17 | MTIOC3A/TCLKD/ PO18 | SCK5/SSLA2/SDA3/ ET_ERXD2 | IRQ12 | |
| 74 | VCC | | | | | | |
| 75 | | PC0 | A16 | MTIOC3C/TCLKC/ PO17 | CTS5#/RTS5#/SS5#/ SSLA1/SCL3/ ET_ERXD3 | IRQ14 | |
| 76 | VSS | | | | | | |
| 77 | | P73 | CS3# | PO16 | ET_WOL | | |
| 78 | | PB7 | A15 | MTIOC3B/TIOCB5/ PO31 | TXD9/SMOSI9/SSDA9/ ET_CRS/ RMII_CRS_DV | | |
| 79 | | PB6 | A14 | MTIOC3D/TIOCA5/ PO30 | RXD9/SMISO9/SSCL9/ ET_ETXD1/RMII_TXD1 | | |
| 80 | | PB5 | A13 | MTIOC2A/MTIOC1B/ TIOCB4/TMR11/PO29/ POE1# | SCK9/ET_ETXD0/ RMII_TXD0 | | |
| 81 | | PB4 | A12 | TIOCA4/PO28 | CTS9#/RTS9#/SS9#/ ET_TX_EN/ RMII_TXD_EN | | |
| 82 | | PB3 | A11 | MTIOC0A/MTIOC4A/ TIOC3/TCLKD/TMO0/ PO27/POE3# | SCK4/SCK6/ ET_RX_ER/ RMII_RX_ER | | |
| 83 | | PB2 | A10 | TIOCC3/TCLKC/PO26 | CTS4#/RTS4#/CTS6#/ RTS6#/SS4#/SS6#/ ET_RX_CLK/REF50CK | | |
| 84 | | PB1 | A9 | MTIOC0C/MTIOC4C/ TIOCB3/TMCI0/PO25 | TXD4/TXD6/SMOSI4/ SMOSI6/SSDA4/ SSDA6/ET_ERXD0/ RMII_RXD0 | IRQ4-DS | |
| 85 | | P72 | CS2# | | ET_MDC | | |
| 86 | | P71 | CS1# | | ET_MDIO | | |
| 87 | | PB0 | A8 | MTIC5W/TIOCA3/ PO24 | RXD4/RXD6/SMISO4/ SMISO6/SSCL4/ SSCL6/RSPCKA/ T_ERXD1/RMII_RXD1 | IRQ12 | |
| 88 | | PA7 | A7 | TIOCB2/PO23 | MISOA/ET_WOL | | |

Table 1.8 List of Pins and Pin Functions (144-Pin LQFP) (4/5)

| Pin No. 144-pin LQFP | Power Supply Clock System Control | I/O Port | Bus EXDMAC SDRAMC | Timers (MTU, TPU, TMR, PPG, RTC, POE) | Communications (ETHERC, SCIC, SCID, RSPI, RIIC, CAN, IEB, USB, and PDC) | Interrupt | S12AD AD DA |
|----------------------------|---|----------|-------------------------|---|--|-----------|-------------------|
| 89 | | PA6 | A6 | MTIC5V/MTCLKB/ TIOCA2/TMC13/PO22/ POE2# | CTS5#/RTS5#/SS5# MOSIA/ET_EXOUT | | |
| 90 | | PA5 | A5 | TIOCB1/PO21 | RSPCKA/ET_LINKSTA | | |
| 91 | VCC | | | | | | |
| 92 | | PA4 | A4 | MTIC5U/MTCLKA/ TIOCA1/TMRI0/PO20 | TXD5/SMISO5/SSDA5/ SSLA0/ET_MDC | IRQ5-DS | |
| 93 | VSS | | | | | | |
| 94 | | PA3 | A3 | MTIOC0D/MTCLKD/ TIOC0D/TCLKB/PO19 | RXD5/SMISO5/SSCL5/ ET_MDIO | IRQ6-DS | |
| 95 | | PA2 | A2 | PO18 | RXD5/SMISO5/SSCL5/ SSLA3 | | |
| 96 | | PA1 | A1 | MTIOC0B/MTCLKC/ TIOCB0/PO17 | SCK5/SSLA2/ET_WOL | IRQ11 | |
| 97 | | PA0 | A0/BC0# | MTIOC4A/TIOCA0/ PO16 | SSLA1/ET_TX_EN/ RMIL_TXD_EN | | |
| 98 | | P67 | CS7#/DQM1 | | CRX2*2 | IRQ15 | |
| 99 | | P66 | CS6#/DQM0 | | CTX2*2 | | |
| 100 | | P65 | CS5#/CKE | | | | |
| 101 | | PE7 | D15[A15/D15] | TIOCB11 | MISOB | IRQ7 | AN5 |
| 102 | | PE6 | D14[A14/D14] | TIOCA11 | MOSIB | IRQ6 | AN4 |
| 103 | VCC | | | | | | |
| 104 | SDCLK | P70 | | | | | |
| 105 | VSS | | | | | | |
| 106 | | PE5 | D13[A13/D13] | MTIOC4C/MTIOC2B/ TIOCB10 | RSPCKB/ET_RX_CLK/ REF50CK | IRQ5 | AN3 |
| 107 | | PE4 | D12[A12/D12] | MTIOC4D/MTIOC1A/ TIOCA10/PO28 | SSLB0/ET_ERXD2 | | AN2 |
| 108 | | PE3 | D11[A11/D11] | MTIOC4B/TIOCB9/ PO26/POE8# | CTS12#/RTS12#/ SS12#/MISOB/ ET_ERXD3 | | AN1 |
| 109 | | PE2 | D10[A10/D10] | MTIOC4A/TIOCA9/ PO23 | RXD12/SMISO12/ SSCL12/RXDX12/ SSLB3/MOSIB | IRQ7-DS | AN0 |
| 110 | | PE1 | D9[A9/D9] | MTIOC4C/TIOC9/ PO18 | TXD12/SMOSI12/ SSDA12/TXDX12/ SIOX12/SSLB2/ RSPCKB | | ANEX1 |
| 111 | | PE0 | D8[A8/D8] | TIOCC9 | SCK12/SSLB1 | | ANEX0 |
| 112 | | P64 | CS4#/WE# | | | | |
| 113 | | P63 | CS3#/CAS# | | | | |
| 114 | | P62 | CS2#/RAS# | | | | |
| 115 | | P61 | CS1#/SDCS# | | | | |
| 116 | VSS | | | | | | |
| 117 | | P60 | CS0# | | | | |
| 118 | VCC | | | | | | |
| 119 | | PD7 | D7[A7/D7] | MTIC5U/POE0# | SSLC3 | IRQ7 | AN7 |
| 120 | | PD6 | D6[A6/D6] | MTIC5V/POE1# | SSLC2 | IRQ6 | AN6 |
| 121 | | PD5 | D5[A5/D5] | MTIC5W/POE2# | SSLC1 | IRQ5 | AN013 |
| 122 | | PD4 | D4[A4/D4] | POE3# | SSLC0 | IRQ4 | AN012 |
| 123 | | PD3 | D3[A3/D3] | TIOCB8/TCLKH/ POE8# | RSPCKC | IRQ3 | AN011 |
| 124 | | PD2 | D2[A2/D2] | MTIOC4D/TIOCA8 | MISOC/CRX0 | IRQ2 | AN010 |

Table 1.8 List of Pins and Pin Functions (144-Pin LQFP) (5/5)

| Pin No. 144-pin LQFP | Power Supply Clock System Control | I/O Port | Bus EXDMAC SDRAMC | Timers (MTU, TPU, TMR, PPG, RTC, POE) | Communications (ETHERC, SC1c, SC1d, RSPI, RIIC, CAN, IEB, USB, and PDC) | Interrupt | S12AD AD DA |
|----------------------------|---|----------|-------------------------|---|--|-----------|-------------------|
| 125 | | PD1 | D1[A1/D1] | MTIOC4B/TIOCB7/ TCLKG | MOSIC/CTX0 | IRQ1 | AN009 |
| 126 | | PD0 | D0[A0/D0] | TIOCA7 | | IRQ0 | AN008 |
| 127 | | P93 | A19 | | CTS7#/RTS7#/SS7# | | AN017 |
| 128 | | P92 | A18 | | RXD7/SMISO7/SSCL7 | | AN016 |
| 129 | | P91 | A17 | | SCK7 | | AN015 |
| 130 | VSS | | | | | | |
| 131 | | P90 | A16 | | TXD7/SMOSI7/SSDA7 | | AN014 |
| 132 | VCC | | | | | | |
| 133 | | P47 | | | | IRQ15-DS | AN007 |
| 134 | | P46 | | | | IRQ14-DS | AN006 |
| 135 | | P45 | | | | IRQ13-DS | AN005 |
| 136 | | P44 | | | | IRQ12-DS | AN004 |
| 137 | | P43 | | | | IRQ11-DS | AN003 |
| 138 | | P42 | | | | IRQ10-DS | AN002 |
| 139 | | P41 | | | | IRQ9-DS | AN001 |
| 140 | VREFLO | | | | | | |
| 141 | | P40 | | | | IRQ8-DS | AN000 |
| 142 | VREFH0 | | | | | | |
| 143 | AVCC0 | | | | | | |
| 144 | | P07 | | | | IRQ15 | ADTRG0# |

Note 1. The BCLK function is multiplexed with the I/O port function for pin P53, so the port function is not available if the external bus is enabled.

Note 2. Enabled only for the ROM capacity: 2 Mbytes/1.5 Mbytes

Table 1.9 List of Pins and Pin Functions (100-Pin TFLGA) (1/5)

| Pin No. 100-pin TFLGA | Power Supply Clock System Control | I/O Port | Bus EXDMAC | Timers (MTU, TPU, TMR, PPG, RTC, POE) | Communications (ETHERC, SClc, SCId, RSPI, RIIC, CAN, IEB, USB) | Interrupt | S12AD AD DA |
|-----------------------------|--|----------|---------------|--|---|-----------|-------------------|
| A1 | | P05 | | | | IRQ13 | DA1 |
| A2 | VREFH | | | | | | |
| A3 | | P07 | | | | IRQ15 | ADTRG0# |
| A4 | VREFL0 | | | | | | |
| A5 | | P43 | | | | IRQ11-DS | AN003 |
| A6 | | PD0 | D0[A0/D0] | | | IRQ0 | AN008 |
| A7 | | PD4 | D4[A4/D4] | POE3# | | IRQ4 | AN012 |
| A8 | | PE0 | D8[A8/D8] | | SCK12/SSLB1 | | ANEX0 |
| A9 | | PE1 | D9[A9/D9] | MTIOC4C/ PO18 | TXD12/SMOSI12/ SSDA12/TXDX12/ SIOX12/SSLB2/ RSPCKB | | ANEX1 |
| A10 | | PE2 | D10[A10/D10] | MTIOC4A/ PO23 | RXD12/SMISO12/ SSCL12/RXDX12/ SSLB3/MOSIB | IRQ7-DS | AN0 |
| B1 | EMLE | | | | | | |
| B2 | AVSS0 | | | | | | |
| B3 | AVCC0 | | | | | | |
| B4 | | P40 | | | | IRQ8-DS | AN000 |
| B5 | | P44 | | | | IRQ12-DS | AN004 |
| B6 | | PD1 | D1[A1/D1] | MTIOC4B | CTX0*1 | IRQ1 | AN009 |
| B7 | | PD3 | D3[A3/D3] | POE8# | | IRQ3 | AN011 |
| B8 | | PD6 | D6[A6/D6] | MTIC5V/ POE1# | | IRQ6 | AN6 |
| B9 | | PD7 | D7[A7/D7] | MTIC5U/ POE0# | | IRQ7 | AN7 |
| B10 | | PE3 | D11[A11/D11] | MTIOC4B/ PO26/POE8# | CTS12#/RTS12#/ SS12#/MISOB/ ET_ERXD3 | | AN1 |
| C1 | VCL | | | | | | |
| C2 | VREFL | | | | | | |
| C3 | | PJ3 | | MTIOC3C | CTS6#/RTS6#/ CTS0#/RTS0#/ SS6#/SS0# | | |
| C4 | VREFH0 | | | | | | |
| C5 | | P42 | | | | IRQ10-DS | AN002 |
| C6 | | P47 | | | | IRQ15-DS | AN007 |
| C7 | | PD2 | D2[A2/D2] | MTIOC4D | CRX0*1 | IRQ2 | AN010 |
| C8 | | PD5 | D5[A5/D5] | MTIC5W/ POE2# | | IRQ5 | AN013 |
| C9 | | PE5 | D13[A13/D13] | MTIOC4C/ MTIOC2B | RSPCKB/ ET_RX_CLK/ REF50CK | IRQ5 | AN3 |
| C10 | | PE4 | D12[A12/D12] | MTIOC4D/ MTIOC1A/ PO28 | SSLB0/ET_ERXD2 | | AN2 |
| D1 | XCIN | | | | | | |

Table 1.9 List of Pins and Pin Functions (100-Pin TFLGA) (2/5)

| Pin No. 100-pin TFLGA | Power Supply Clock System Control | I/O Port | Bus EXDMAC | Timers (MTU, TPU, TMR, PPG, RTC, POE) | Communications (ETHERC, SC1c, SC1d, RSPI, RIIC, CAN, IEB, USB) | Interrupt | S12AD AD DA |
|-----------------------------|--|----------|---------------|---|---|-----------|-------------------|
| D2 | XCOUT | | | | | | |
| D3 | MD/FINED | | | | | | |
| D4 | VBATT | | | | | | |
| D5 | | P45 | | | | IRQ13-DS | AN005 |
| D6 | | P46 | | | | IRQ14-DS | AN006 |
| D7 | | PE6 | D14[A14/D14] | | MOSIB | IRQ6 | AN4 |
| D8 | | PE7 | D15[A15/D15] | | MISOB | IRQ7 | AN5 |
| D9 | | PA1 | A1 | MTIOC0B/ MTCLKC/ TIOC0B/PO17 | SCK5/SSLA2/ ET_WOL | IRQ11 | |
| D10 | | PA0 | A0/BC0# | MTIOC4A/ TIOCA0/PO16 | SSLA1/ET_TX_EN/ RMII_TXD_EN | | |
| E1 | XTAL | P37 | | | | | |
| E2 | VSS | | | | | | |
| E3 | RES# | | | | | | |
| E4 | TRST# | P34 | | MTIOC0A/ TMCI3/PO12/ POE2# | SCK6/SCK0/ USB0_DPRPD | IRQ4 | |
| E5 | | P41 | | | | IRQ9-DS | AN001 |
| E6 | | PA2 | A2 | PO18 | RXD5/SMISO5/ SSCL5/SSLA3 | | |
| E7 | | PA6 | A6 | MTIC5V/ MTCLKB/ TIOCA2/ TMCI3/PO22/ POE2# | CTS5#/RTS5#/ SS5#/MOSIA/ ET_EXOUT | | |
| E8 | | PA4 | A4 | MTIC5U/ MTCLKA/ TIOCA1/ TMRI0/PO20 | TXD5/SMOSI5/ SSDA5/SSLA0/ ET_MDC | IRQ5-DS | |
| E9 | | PA5 | A5 | TIOC0B1/PO21 | RSPCKA/ ET_LINKSTA | | |
| E10 | | PA3 | A3 | MTIOC0D/ MTCLKD/ TIOC0D/ TCLKB/PO19 | RXD5/SMISO5/ SSCL5/ET_MDIO | IRQ6-DS | |
| F1 | EXTAL | P36 | | | | | |
| F2 | VCC | | | | | | |
| F3 | | P35 | | | | NMI | |
| F4 | | P32 | | MTIOC0C/ TIOCC0/TMO3/ PO10/ RTCOUT/ RTCIC2 | TXD6/TXD0/ SMOSI6/SMOSI0/ SSDA6/SSDA0/ CTX0*1/ USB0_VBUSEN | IRQ2-DS | |
| F5 | | P12 | | TMCI1 | RXD2/SMISO2/ SSCL2/SCL0[FM+] | IRQ2 | |
| F6 | | PB3 | A11 | MTIOC0A/ MTIOC4A/ TIOC0D3/ TCLKD/TMO0/ PO27/POE3# | SCK6/ET_RX_ER/ RMII_RX_ER | | |

Table 1.9 List of Pins and Pin Functions (100-Pin TFLGA) (3/5)

| Pin No. 100-pin TFLGA | Power Supply Clock System Control | I/O Port | Bus EXDMAC | Timers (MTU, TPU, TMR, PPG, RTC, POE) | Communications (ETHERC, SC1c, SC1d, RSPI, RIIC, CAN, IEB, USB) | Interrupt | S12AD AD DA |
|-----------------------------|--|----------|-----------------|---|--|-----------|-------------------|
| F7 | | PB2 | A10 | TIOCC3/ TCLKC/PO26 | CTS6#/RTS6#/ SS6#/ET_RX_CLK/ REF50CK | | |
| F8 | | PB0 | A8 | MTIC5W/ TIOCA3/PO24 | RXD6/SMISO6/ SSCL6/RSPCKA/ ET_ERXD1/ RMII_RXD1 | IRQ12 | |
| F9 | | PA7 | A7 | TIOCB2/PO23 | MISOA/ET_WOL | | |
| F10 | VSS | | | | | | |
| G1 | | P33 | | MTIOC0D/ TIOC0D/ TMRI3/PO11/ POE3# | RXD6/RXD0/ SMISO6/SMISO0/ SSCL6/SSCL0/ CRX0*1 | IRQ3-DS | |
| G2 | TMS | P31 | | MTIOC4D/ TMC12/PO9/ RTCIC1 | CTS1#/RTS1#/ SS1#/SSLB0/ USB0_DPUPE | IRQ1-DS | |
| G3 | TDI | P30 | | MTIOC4B/ TMRI3/PO8/ RTCIC0/POE8# | RXD1/SMISO1/ SSCL1/MISOB/ USB0_DRPD | IRQ0-DS | |
| G4 | TCK/FINEC | P27 | CS7# | MTIOC2B/ TMCI3/PO7 | SCK1/RSPCKB | | |
| G5 | BCLK | P53*2 | | | | | |
| G6 | | P52 | RD# | | RXD2/SMISO2/ SSCL2/SSLB3 | | |
| G7 | | PB5 | A13 | MTIOC2A/ MTIOC1B/ TIOCB4/ TMRI1/PO29/ POE1# | SCK9/ET_ETXD0/ RMII_TXD0 | | |
| G8 | | PB4 | A12 | TIOCA4/PO28 | CTS9#/RTS9#/ SS9#/ET_TX_EN/ RMII_TXD_EN | | |
| G9 | | PB1 | A9 | MTIOC0C/ MTIOC4C/ TIOCB3/ TMCI0/PO25 | TXD6/SMOSI6/ SSDA6/ET_ERXD0/ RMII_RXD0 | IRQ4-DS | |
| G10 | VCC | | | | | | |
| H1 | TDO | P26 | CS6# | MTIOC2A/ TMO1/PO6 | TXD1/CTS3#/ RTS3#/SMOSI1/ SS3#/SSDA1/ MOSIB | | |
| H2 | | P25 | CS5#/ EDACK1 | MTIOC4C/ MTCLKB/ TIOCA4/PO5 | RXD3/SMISO3/ SSCL3/ USB0_DPRPD | | ADTRG0# |
| H3 | | P16 | | MTIOC3C/ MTIOC3D/ TIOCB1/ TCLKC/TMO2/ PO14/RTCOUT | TXD1/RXD3/ SMOSI1/SMISO3/ SSDA1/SSCL3/ MOSIA/SCL2-DS/ IERXD/ USB0_VBUS/ USB0_VBUSEN/ USB0_OVRCURB | IRQ6 | ADTRG0# |

Table 1.9 List of Pins and Pin Functions (100-Pin TFLGA) (4/5)

| Pin No. 100-pin TFLGA | Power Supply Clock System Control | I/O Port | Bus EXDMAC | Timers (MTU, TPU, TMR, PPG, RTC, POE) | Communications (ETHERC, SC1c, SC1d, RSPI, RIIC, CAN, IEB, USB) | Interrupt | S12AD AD DA |
|-----------------------------|--|----------|------------------|--|---|-----------|-------------------|
| H4 | | P15 | | MTIOC0B/ MTCLKB/ TIOCB2/ TCLKB/TMC12/ PO13 | RXD1/SCK3/ SMISO1/SSCL1/ CRX1-DS | IRQ5 | |
| H5 | | P55 | WAIT#/ EDREQ0 | MTIOC4D/ TMO3 | CRX1/ET_EXOUT | IRQ10 | |
| H6 | | P54 | ALE/EDACK0 | MTIOC4B/ TMC11 | CTS2#/RTS2#/ SS2#/CTX1/ ET_LINKSTA | | |
| H7 | | PC7 | A23/CS0# | MTIOC3A/ MTCLKB/ TMO2/PO31 | TXD8/SMOSI8/ SSDA8/MISOA/ ET_COL | IRQ14 | |
| H8 | | PC6 | A22/CS1# | MTIOC3C/ MTCLKA/ TMC12/PO30 | RXD8/SMISO8/ SSCL8/MOSIA/ ET_ETXD3 | IRQ13 | |
| H9 | | PB6 | A14 | MTIOC3D/ TIOCA5/PO30 | RXD9/SMISO9/ SSCL9/ET_ETXD1/ RMII_TXD1 | | |
| H10 | | PB7 | A15 | MTIOC3B/ TIOCB5/PO31 | TXD9/SMOSI9/ SSDA9/ET_CRS/ RMII_CRS_DV | | |
| J1 | | P24 | CS4#/ EDREQ1 | MTIOC4A/ MTCLKA/ TIOCB4/ TMR11/PO4 | SCK3/ USB0_VBUSEN | | |
| J2 | | P21 | | MTIOC1B/ TIOCA3/ TMC10/PO1 | RXD0/SMISO0/ SSCL0/ USB0_EXICEN | IRQ9 | |
| J3 | | P17 | | MTIOC3A/ MTIOC3B/ TIOCB0/ TCLKD/TMO1/ PO15/POE8# | SCK1/TXD3/ SMOSI3/SSDA3/ MISOA/SDA2-DS/ IETXD | IRQ7 | ADTRG# |
| J4 | | P13 | | MTIOC0B/ TIOCA5/TMO3/ PO13 | TXD2/SMOSI2/ SSDA2/SDA0[FM+] | IRQ3 | ADTRG# |
| J5 | VSS_USB | | | | | | |
| J6 | VCC_USB | | | | | | |
| J7 | | P50 | WR0#/WR# | | TXD2/SMOSI2/ SSDA2/SSLB1 | | |
| J8 | | PC4 | A20/CS3# | MTIOC3D/ MTCLKC/ TMC11/PO25/ POE0# | SCK5/CTS8#/ RTS8#/SS8#/ SSLA0/ET_TX_CLK | | |
| J9 | | PC0 | A16 | MTIOC3C/ TCLKC/PO17 | CTS5#/RTS5#/ SS5#/SSLA1/ ET_ERXD3 | IRQ14 | |
| J10 | | PC1 | A17 | MTIOC3A/ TCLKD/PO18 | SCK5/SSLA2/ ET_ERXD2 | IRQ12 | |
| K1 | | P23 | EDACK0 | MTIOC3D/ MTCLKD/ TIOCD3/PO3 | TXD3/CTS0#/ RTS0#/SMOSI3/ SS0#/SSDA3/ USB0_DPUPE | | |

Table 1.9 List of Pins and Pin Functions (100-Pin TFLGA) (5/5)

| Pin No. 100-pin TFLGA | Power Supply Clock System Control | I/O Port | Bus EXDMAC | Timers (MTU, TPU, TMR, PPG, RTC, POE) | Communications (ETHERC, SCId, SCId, RSPI, RIIC, CAN, IEB, USB) | Interrupt | S12AD AD DA |
|-----------------------------|--|----------|---------------------|--|---|-----------|-------------------|
| K2 | | P22 | EDREQ0 | MTIOC3B/ MTCLKC/ TIOCC3/TMO0/ PO2 | SCK0/USB0_DRPD | | |
| K3 | | P20 | | MTIOC1A/ TIOCB3/ TMRI0/PO0 | TXD0/SMOSI0/ SSDA0/USB0_ID | IRQ8 | |
| K4 | | P14 | | MTIOC3A/ MTCLKA/ TIOCB5/ TCLKA/TMRI2/ PO15 | CTS1#/RTS1#/ SS1#/CTX1/ USB0_DPUPE/ USB0_OVRCURA | IRQ4 | |
| K5 | | | | | USB0_DM | | |
| K6 | | | | | USB0_DP | | |
| K7 | | P51 | WR1#/BC1#/ WAIT# | | SCK2/SSLB2 | | |
| K8 | | PC5 | A21/CS2#/ WAIT# | MTIOC3B/ MTCLKD/ TMRI2/PO29 | SCK8/RSPCKA/ ET_ETXD2 | | |
| K9 | | PC3 | A19 | MTIOC4D/ TCLKB/PO24 | TXD5/SMOSI5/ SSDA5/IETXD/ ET_TX_ER | | |
| K10 | | PC2 | A18 | MTIOC4B/ TCLKA/PO21 | RXD5/SMISO5/ SSCL5/SSLA3/ IERXD/ET_RX_DV | | |

Note 1. Enabled only for the ROM capacity of 768 Kbytes or more.

Note 2. The BCLK function is multiplexed with the I/O port function for pin P53, so the port function is not available if the external bus is enabled.

Table 1.10 List of Pins and Pin Functions (100-Pin LQFP) (1/4)

| Pin No. | Power Supply Clock System Control | I/O Port | Bus EXDMAC | Timers (MTU, TPU, TMR, PPG, RTC, POE) | Communications (ETHERC, SClc, SClD, RSPI, RIIC, CAN, IEB, USB) | Interrupt | S12AD AD DA |
|---------|---|----------|---------------|---|--|-----------|-------------------|
| 1 | VREFH | | | | | | |
| 2 | EMLE | | | | | | |
| 3 | VREFL | | | | | | |
| 4 | | PJ3 | | MTIOC3C | CTS6#/RTS6#/CTS0#/ RTS0#/SS6#/SS0# | | |
| 5 | VCL | | | | | | |
| 6 | VBATT | | | | | | |
| 7 | MD/FINED | | | | | | |
| 8 | XCIN | | | | | | |
| 9 | XCOUT | | | | | | |
| 10 | RES# | | | | | | |
| 11 | XTAL | P37 | | | | | |
| 12 | VSS | | | | | | |
| 13 | EXTAL | P36 | | | | | |
| 14 | VCC | | | | | | |
| 15 | | P35 | | | | NMI | |
| 16 | TRST# | P34 | | MTIOC0A/TMC13/ PO12/POE2# | SCK6/SCK0/ USB0_DPRPD | IRQ4 | |
| 17 | | P33 | | MTIOC0D/TIOC0D/ TMR13/PO11/POE3# | RXD6/RXD0/SMISO6/ SMISO0/SSCL6/ SSCL0/CRX0*1 | IRQ3-DS | |
| 18 | | P32 | | MTIOC0C/TIOCC0/ TMO3/PO10/RTCOUT/ RTCIC2 | TXD6/TXD0/SMOSI6/ SMOSI0/SSDA6/ SSDA0/CTX0*1/ USB0_VBUSEN | IRQ2-DS | |
| 19 | TMS | P31 | | MTIOC4D/TMC12/PO9/ RTCIC1 | CTS1#/RTS1#/SS1#/ SSLB0/USB0_DPUPE | IRQ1-DS | |
| 20 | TDI | P30 | | MTIOC4B/TMR13/PO8/ RTCIC0/POE8# | RXD1/SMISO1/SSCL1/ MISOB/USB0_DRPD | IRQ0-DS | |
| 21 | TCK/FINEC | P27 | CS7# | MTIOC2B/TMC13/PO7 | SCK1/RSPCKB | | |
| 22 | TDO | P26 | CS6# | MTIOC2A/TMO1/PO6 | TXD1/CTS3#/RTS3#/ SMOSI1/SS3#/SSDA1/ MOSIB | | |
| 23 | | P25 | CS5#/EDACK1 | MTIOC4C/MTCLKB/ TIOCA4/PO5 | RXD3/SMISO3/SSCL3/ USB0_DPRPD | | ADTRG0# |
| 24 | | P24 | CS4#/EDREQ1 | MTIOC4A/MTCLKA/ TIOCB4/TMR11/PO4 | SCK3/USB0_VBUSEN | | |
| 25 | | P23 | EDACK0 | MTIOC3D/MTCLKD/ TIOC3D/PO3 | TXD3/CTS0#/RTS0#/ SMOSI3/SS0#/SSDA3/ USB0_DPUPE | | |
| 26 | | P22 | EDREQ0 | MTIOC3B/MTCLKC/ TIOCC3/TMO0/PO2 | SCK0/USB0_DRPD | | |
| 27 | | P21 | | MTIOC1B/TIOCA3/ TMC10/PO1 | RXD0/SMISO0/SSCL0/ USB0_EXICEN | IRQ9 | |
| 28 | | P20 | | MTIOC1A/TIOCB3/ TMR10/PO0 | TXD0/SMOSI0/SSDA0/ USB0_ID | IRQ8 | |
| 29 | | P17 | | MTIOC3A/MTIOC3B/ TIOCB0/TCLKD/TMO1/ PO15/POE8# | SCK1/TXD3/SMOSI3/ SSDA3/MISOA/SDA2- DS/IETXD | IRQ7 | ADTRG# |
| 30 | | P16 | | MTIOC3C/MTIOC3D/ TIOCB1/TCLKC/TMO2/ PO14/RTCOUT | TXD1/RXD3/SMOSI1/ SMISO3/SSDA1/ SSCL3/MOSIA/SCL2- DS/IERXD/ USB0_VBUS/ USB0_VBUSEN/ USB0_OVRCURB | IRQ6 | ADTRG0# |

Table 1.10 List of Pins and Pin Functions (100-Pin LQFP) (2/4)

| Pin No. | Power Supply Clock System Control | I/O Port | Bus EXDMAC | Timers (MTU, TPU, TMR, PPG, RTC, POE) | Communications (ETHERC, SClc, SClD, RSPI, RIIC, CAN, IEB, USB) | Interrupt | S12AD AD DA |
|---------|---|----------|---------------------|--|---|-----------|-------------------|
| 31 | | P15 | | MTIOC0B/MTCLKB/ TIOCB2/TCLKB/TMC12/ PO13 | RXD1/SCK3/SMISO1/ SSCL1/CRX1-DS | IRQ5 | |
| 32 | | P14 | | MTIOC3A/MTCLKA/ TIOCB5/TCLKA/TMR12/ PO15 | CTS1#/RTS1#/SS1#/ CTX1/USB0_DPUPE/ USB0_OVRCURA | IRQ4 | |
| 33 | | P13 | | MTIOC0B/TIOCA5/ TMO3/PO13 | TXD2/SMOSI2/SSDA2/ SDA0[FM+] | IRQ3 | ADTRG# |
| 34 | | P12 | | TMC1 | RXD2/SMISO2/SSCL2/ SCL0[FM+] | IRQ2 | |
| 35 | VCC_USB | | | | | | |
| 36 | | | | | USB0_DM | | |
| 37 | | | | | USB0_DP | | |
| 38 | VSS_USB | | | | | | |
| 39 | | P55 | WAIT#/ EDREQ0 | MTIOC4D/TMO3 | CRX1/ET_EXOUT | IRQ10 | |
| 40 | | P54 | ALE/EDACK0 | MTIOC4B/TMC1 | CTS2#/RTS2#/SS2#/ CTX1/ET_LINKSTA | | |
| 41 | | P53*2 | BCLK | | | | |
| 42 | | P52 | RD# | | RXD2/SMISO2/SSCL2/ SSLB3 | | |
| 43 | | P51 | WR1#/BC1#/ WAIT# | | SCK2/SSLB2 | | |
| 44 | | P50 | WR0#/WR# | | TXD2/SMOSI2/SSDA2/ SSLB1 | | |
| 45 | | PC7 | A23/CS0# | MTIOC3A/MTCLKB/ TMO2/PO31 | TXD8/SMOSI8/SSDA8/ MISOA/ET_COL | IRQ14 | |
| 46 | | PC6 | A22/CS1# | MTIOC3C/MTCLKA/ TMC12/PO30 | RXD8/SMISO8/SSL8/ MOSIA/ET_ETXD3 | IRQ13 | |
| 47 | | PC5 | A21/CS2#/ WAIT# | MTIOC3B/MTCLKD/ TMR12/PO29 | SCK8/RSPCKA/ ET_ETXD2 | | |
| 48 | | PC4 | A20/CS3# | MTIOC3D/MTCLKC/ TMC11/PO25/POE0# | SCK5/CTS8#/RTS8#/ SS8#/SSLA0/ ET_TX_CLK | | |
| 49 | | PC3 | A19 | MTIOC4D/TCLKB/ PO24 | TXD5/SMOSI5/SSDA5/ IETXD/ET_TX_ER | | |
| 50 | | PC2 | A18 | MTIOC4B/TCLKA/PO21 | RXD5/SMISO5/SSCL5/ SSLA3/IERXD/ ET_RX_DV | | |
| 51 | | PC1 | A17 | MTIOC3A/TCLKD/ PO18 | SCK5/SSLA2/ ET_ERXD2 | IRQ12 | |
| 52 | | PC0 | A16 | MTIOC3C/TCLKC/ PO17 | CTS5#/RTS5#/SS5#/ SSLA1/ET_ERXD3 | IRQ14 | |
| 53 | | PB7 | A15 | MTIOC3B/TIOCB5/ PO31 | TXD9/SMOSI9/SSDA9/ ET_CRS/ RMII_CRS_DV | | |
| 54 | | PB6 | A14 | MTIOC3D/TIOCA5/ PO30 | RXD9/SMISO9/SSCL9/ ET_ETXD1/RMII_TXD1 | | |
| 55 | | PB5 | A13 | MTIOC2A/MTIOC1B/ TIOCB4/TMR11/PO29/ POE1# | SCK9/ET_ETXD0/ RMII_TXD0 | | |
| 56 | | PB4 | A12 | TIOCA4/PO28 | CTS9#/RTS9#/SS9#/ ET_TX_EN/ RMII_TXD_EN | | |
| 57 | | PB3 | A11 | MTIOC0A/MTIOC4A/ TIOCD3/TCLKD/TMO0/ PO27/POE3# | SCK6/ET_RX_ER/ RMII_RX_ER | | |
| 58 | | PB2 | A10 | TIOCC3/TCLKC/PO26 | CTS6#/RTS6#/SS6#/ ET_RX_CLK/REF50CK | | |

Table 1.10 List of Pins and Pin Functions (100-Pin LQFP) (3/4)

| Pin No. | Power Supply Clock System Control | I/O Port | Bus EXDMAC | Timers (MTU, TPU, TMR, PPG, RTC, POE) | Communications (ETHERC, SC1c, SC1d, RSPI, RIIC, CAN, IEB, USB) | Interrupt | S12AD AD DA |
|---------|---|----------|---------------|---|---|-----------|-------------------|
| 59 | | PB1 | A9 | MTIOC0C/MTIOC4C/ TIOCB3/TMC10/PO25 | TXD6/SMOSI6/SSDA6/ ET_ERXD0/ RMII_RXD0 | IRQ4-DS | |
| 60 | VCC | | | | | | |
| 61 | | PB0 | A8 | MTIC5W/TIOCA3/PO24 | RXD6/SMISO6/SSCL6/ RSPCKA/ET_ERXD1/ RMII_RXD1 | IRQ12 | |
| 62 | VSS | | | | | | |
| 63 | | PA7 | A7 | TIOCB2/PO23 | MISOA/ET_WOL | | |
| 64 | | PA6 | A6 | MTIC5V/MTCLKB/ TIOCA2/TMC13/PO22/ POE2# | CTS5#/RTS5#/SS5#/ MOSIA/ET_EXOUT | | |
| 65 | | PA5 | A5 | TIOCB1/PO21 | RSPCKA/ET_LINKSTA | | |
| 66 | | PA4 | A4 | MTIC5U/MTCLKA/ TIOCA1/TMRI0/PO20 | TXD5/SMOSI5/SSDA5/ SSLA0/ET_MDC | IRQ5-DS | |
| 67 | | PA3 | A3 | MTIOC0D/MTCLKD/ TIOC0D/TCLKB/PO19 | RXD5/SMISO5/SSCL5/ ET_MDIO | IRQ6-DS | |
| 68 | | PA2 | A2 | PO18 | RXD5/SMISO5/SSCL5/ SSLA3 | | |
| 69 | | PA1 | A1 | MTIOC0B/MTCLKC/ TIOCB0/PO17 | SCK5/SSLA2/ET_WOL | IRQ11 | |
| 70 | | PA0 | A0/BC0# | MTIOC4A/TIOCA0/ PO16 | SSLA1/ET_TX_EN/ RMII_TXD_EN | | |
| 71 | | PE7 | D15[A15/D15] | | MISOB | IRQ7 | AN5 |
| 72 | | PE6 | D14[A14/D14] | | MOSIB | IRQ6 | AN4 |
| 73 | | PE5 | D13[A13/D13] | MTIOC4C/MTIOC2B | RSPCKB/ET_RX_CLK/ REF50CK | IRQ5 | AN3 |
| 74 | | PE4 | D12[A12/D12] | MTIOC4D/MTIOC1A/ PO28 | SSLB0/ET_ERXD2 | | AN2 |
| 75 | | PE3 | D11[A11/D11] | MTIOC4B/PO26/POE8# | CTS12#/RTS12#/ SS12#/MISOB/ ET_ERXD3 | | AN1 |
| 76 | | PE2 | D10[A10/D10] | MTIOC4A/PO23 | RXD12/SMISO12/ SSCL12/RXD12/ SSLB3/MOSIB | IRQ7-DS | AN0 |
| 77 | | PE1 | D9[A9/D9] | MTIOC4C/PO18 | TXD12/SMOSI12/ SSDA12/TXD12/ SIOX12/SSLB2/ RSPCKB | | ANEX1 |
| 78 | | PE0 | D8[A8/D8] | | SCK12/SSLB1 | | ANEX0 |
| 79 | | PD7 | D7[A7/D7] | MTIC5U/POE0# | | IRQ7 | AN7 |
| 80 | | PD6 | D6[A6/D6] | MTIC5V/POE1# | | IRQ6 | AN6 |
| 81 | | PD5 | D5[A5/D5] | MTIC5W/POE2# | | IRQ5 | AN013 |
| 82 | | PD4 | D4[A4/D4] | POE3# | | IRQ4 | AN012 |
| 83 | | PD3 | D3[A3/D3] | POE8# | | IRQ3 | AN011 |
| 84 | | PD2 | D2[A2/D2] | MTIOC4D | CRX0*1 | IRQ2 | AN010 |
| 85 | | PD1 | D1[A1/D1] | MTIOC4B | CTX0*1 | IRQ1 | AN009 |
| 86 | | PD0 | D0[A0/D0] | | | IRQ0 | AN008 |
| 87 | | P47 | | | | IRQ15-DS | AN007 |
| 88 | | P46 | | | | IRQ14-DS | AN006 |
| 89 | | P45 | | | | IRQ13-DS | AN005 |
| 90 | | P44 | | | | IRQ12-DS | AN004 |
| 91 | | P43 | | | | IRQ11-DS | AN003 |
| 92 | | P42 | | | | IRQ10-DS | AN002 |
| 93 | | P41 | | | | IRQ9-DS | AN001 |

Table 1.10 List of Pins and Pin Functions (100-Pin LQFP) (4/4)

| Pin No. 100-pin LQFP | Power Supply Clock System Control | I/O Port | Bus EXDMAC | Timers (MTU, TPU, TMR, PPG, RTC, POE) | Communications (ETHERC, SC1c, SC1d, RSPI, RIIC, CAN, IEB, USB) | Interrupt | S12AD AD DA |
|----------------------------|---|----------|---------------|---|---|-----------|-------------------|
| 94 | VREFL0 | | | | | | |
| 95 | | P40 | | | | IRQ8-DS | AN000 |
| 96 | VREFH0 | | | | | | |
| 97 | AVCC0 | | | | | | |
| 98 | | P07 | | | | IRQ15 | ADTRG0# |
| 99 | AVSS0 | | | | | | |
| 100 | | P05 | | | | IRQ13 | DA1 |

Note 1. Enabled only for the ROM capacity of 768 Kbytes or more

Note 2. The BCLK function is multiplexed with the I/O port function for pin P53, so the port function is not available if the external bus is enabled.

Table 1.11 List of Pins and Pin Functions (64-Pin TFLGA) (1/2)

| Pin No. 64-pin TFLGA | Power Supply Clock System Control | I/O Port | Timers (MTU2a, TPUa, TMR, PPG, RTCa, POE2a) | Communications (SClC, SClD, RSPI, RIIC, CAN, IEB, USB) | Interrupt | S12ADa, DAa |
|----------------------------|---|----------|---|--|-----------|-------------|
| A1 | | P05 | | | IRQ13 | DA1 |
| A2 | AVCC0 | | | | | |
| A3 | VREFH0 | | | | | |
| A4 | VREFL0 | | | | | |
| A5 | VREFH | | | | | |
| A6 | VREFL | | | | | |
| A7 | | PE2 | MTIOC4A/PO23 | RXD12/SMISO12/SSCL12/ RXDX12/SSLB3/MOSIB | IRQ7-DS | AN010 |
| A8 | | PE3 | MTIOC4B/PO26/POE8# | CTS12#/RTS12#/SS12#/ MISOB | | AN011 |
| B1 | VCL | | | | | |
| B2 | AVSS0 | | | | | |
| B3 | | P40 | | | IRQ8-DS | AN000 |
| B4 | | P42 | | | IRQ10-DS | AN002 |
| B5 | | P44 | | | IRQ12-DS | AN004 |
| B6 | | P46 | | | IRQ14-DS | AN006 |
| B7 | | PE1 | MTIOC4C/PO18 | TXD12/SMOS12/SSDA12/ TXDX12/SIOX12/SSLB2/ RSPCKB | | AN009 |
| B8 | | PE4 | MTIOC4D/MTIOC1A/PO28 | SSLB0 | | AN012 |
| C1 | XCIN | | | | | |
| C2 | MD/FINED | | | | | |
| C3 | EMLE | | | | | |
| C4 | | P41 | | | IRQ9-DS | AN001 |
| C5 | | P43 | | | IRQ11-DS | AN003 |
| C6 | | PE0 | | SCK12/SSLB1 | | AN008 |
| C7 | | PE5 | MTIOC4C/MTIOC2B | RSPCKB | IRQ5 | AN013 |
| C8 | | PA0 | MTIOC4A/TIOCA0/PO16 | SSLA1 | | |
| D1 | XCOUT | | | | | |
| D2 | RES# | | | | | |
| D3 | TCK FINEC | P27 | MTIOC2B/TMCI3 | SCK1/RSPCKB | | |
| D4 | | P14 | MTIOC3A/MTCLKA/ TIOCB5/TCLKA/TMRI2 | CTS1#/RTS1#/SS1#/CTX1/ USB0_DPUPE/ USB0_OVRCURA | IRQ4 | |
| D5 | | PA6 | MTIC5V/MTCLKB/TIOCA2/ TMCI3/PO22/POE2# | CTS5#/RTS5#/SS5#/ MOSIA | | |
| D6 | | PA4 | MTIC5U/MTCLKA/TIOCA1/ TMRI0/PO20 | TXD5/SMOS15/SSDA5/ SSLA0 | IRQ5-DS | |
| D7 | | PA1 | MTIOC0B/MTCLKC/ TIOCB0/PO17 | SCK5/SSLA2/SCL2 | IRQ11 | |
| D8 | | PA3 | MTIOC0D/MTCLKD/ TIOCD0/TCLKB/PO19 | RXD5/SMISO5/SSCL5/ SDA2 | IRQ6-DS | |
| E1 | VSS | | | | | |
| E2 | VBATT | | | | | |
| E3 | TDI | P30 | MTIOC4B/TMRI3/POE8#/ RTIC0 | RXD1/SMISO1/SSCL1/ MISOB/USB0_DRPD | IRQ0-DS | |

Table 1.11 List of Pins and Pin Functions (64-Pin TFLGA) (2/2)

| Pin No. 64-pin TFLGA | Power Supply Clock System Control | I/O Port | Timers (MTU2a, TPUa, TMR, PPG, RTCa, POE2a) | Communications (SClC, SCId, RSPI, RIIC, CAN, IEB, USB) | Interrupt | S12ADa, DAa |
|----------------------------|---|----------|---|--|-----------|-------------|
| E4 | TMS | P16 | MTIOC3C/MTIOC3D/ TIOCB1/TCLKC/TMO2/ RTCOUT | TXD1/SMOSI1/SSDA1/ MOSIA/SCL2-DS/IERXD/ USB0_VBUS/ USB0_VBUSEN/ USB0_OVRCURB | IRQ6 | ADTRG0# |
| E5 | | PC4 | MTIOC3D/MTCLKC/TMC11/ PO25/POE0# | SCK5/SSLA0/ USB0_DPRPD | | |
| E6 | VCC | | | | | |
| E7 | VSS | | | | | |
| E8 | | PB0 | MTIC5W/TIOCA3/PO24 | RXD6/SMISO6/SSCL6/ RSPCKA | IRQ12 | |
| F1 | VCC | | | | | |
| F2 | | P35 | | | NMI | |
| F3 | | P31 | MTIOC4D/TMC12/RTCIC1 | CTS1#/RTS1#/SS1#/ SSLB0/USB0_DPUPE | IRQ1-DS | |
| F4 | | PC5 | MTIOC3B/MTCLKD/TMR12/ PO29 | RSPCKA/USB0_ID | | |
| F5 | | P15 | MTIOC0B/MTCLKB/ TIOCB2/TCLKB/TMC12 | RXD1/SMISO1/SSCL1/ CRX1-DS/USB1_DPUPE | IRQ5 | |
| F6 | | PB1 | MTIOC0C/MTIOC4C/ TIOCB3/TMC10/PO25 | TXD6/SMOSI6/SSDA6 | IRQ4-DS | |
| F7 | | PB5 | MTIOC2A/MTIOC1B/ TIOCB4/TMR11/PO29/ POE1# | SCK9 | | |
| F8 | | PB3 | MTIOC0A/MTIOC4A/ TIOC3/TCLKD/TMO0/ PO27/POE3# | SCK6 | | |
| G1 | EXTAL | P36 | | | | |
| G2 | TDO | P26 | MTIOC2A/TMO1 | TXD1/SMOSI1/SSDA1/ MOSIB/USB0_VBUSEN | | |
| G3 | VCC_USB | | | | | |
| G4 | VSS_USB | | | | | |
| G5 | VCC_USB | | | | | |
| G6 | | PC6 | MTIOC3C/MTCLKA/TMC12/ PO30 | MOSIA/USB0_EXICEN | IRQ13 | |
| G7 | | PC3 | MTIOC4D/TCLKB/PO24 | TXD5/SMOSI5/SSDA5/ SDA2/IETXD | | |
| G8 | | PB6 | MTIOC3D/TIOCA5/PO30 | RXD9/SMISO9/SSCL9 | | |
| H1 | XTAL | P37 | | | | |
| H2 | TRST# | P17 | MTIOC3A/MTIOC3B/ TIOCB0/TCLKD/TMO1/ POE8# | SCK1/MISOA/SDA2-DS/ IETXD/USB1_VBUS | IRQ7 | |
| H3 | | | | USB0_DM | | |
| H4 | | | | USB0_DP | | |
| H5 | | | | USB1_DM | | |
| H6 | | | | USB1_DP | | |
| H7 | | PC2 | MTIOC4B/TCLKA/PO21 | RXD5/SMISO5/SSCL5/ SSLA3/SCL2/IERXD | | |
| H8 | | PB7 | MTIOC3B/TIOCB5/PO31 | TXD9/SMOSI9/SSDA9 | | |

Table 1.12 List of Pins and Pin Functions (64-Pin LQFP) (1/3)

| Pin Number 64-Pin LQFP | Power Supply Clock System Control | I/O Port | Timer (MTU2a, TPUa, TMR, PPG, RTCa, POE2a) | Timer Communications (SClC, SClD, RSPI, RIIC, CAN, IEB, USB) | Interrupt | S12ADa, DAa |
|------------------------------|---|----------|---|--|-----------|-------------|
| 1 | EMLE | | | | | |
| 2 | VCL | | | | | |
| 3 | MD/FINED | | | | | |
| 4 | XCIN | | | | | |
| 5 | XCOUT | | | | | |
| 6 | RES# | | | | | |
| 7 | XTAL | P37 | | | | |
| 8 | VSS | | | | | |
| 9 | EXTAL | P36 | | | | |
| 10 | VCC | | | | | |
| 11 | | P35 | | | NMI | |
| 12 | VBATT | | | | | |
| 13 | | P31 | MTIOC4D/TMC12/PO9/ RTCIC1 | CTS1#/RTS1#/SS1#/ SSLB0/USB0_DPUPE | IRQ1-DS | |
| 14 | TDI | P30 | MTIOC4B/TMRI3/PO8/ POE8#/RTCIC0 | RXD1/SMISO1/SSCL1/ MISOB/USB0_DRPD | IRQ0-DS | |
| 15 | TCK/FINEC | P27 | MTIOC2B/TMC13/PO7 | SCK1/RSPCKB | | |
| 16 | TDO | P26 | MTIOC2A/TMO1/PO6 | TXD1/SMOSI1/SSDA1/ MOSIB/USB0_VBUSEN | | |
| 17 | TRST# | P17 | MTIOC3A/MTIOC3B/ TIOCB0/TCLKD/TMO1/ PO15/POE8# | SCK1/MISOA/ SDA2-DS/IETXD | IRQ7 | |
| 18 | TMS | P16 | MTIOC3C/MTIOC3D/ TIOCB1/TCLKC/TMO2/ PO14/RTCOUT | TXD1/SMOSI1/SSDA1/ MOSIA/SCL2-DS/IERXD/ USB0_VBUS/ USB0_VBUSEN/ USB0_OVRCURB | IRQ6 | ADTRG0# |
| 19 | | P15 | MTIOC0B/MTCLKB/ TIOCB2/TCLKB/TMC12/ PO13 | RXD1/SMISO1/SSCL1/ CRX1-DS | IRQ5 | |
| 20 | | P14 | MTIOC3A/MTCLKA/ TIOCB5/TCLKA/TMRI2/ PO15 | CTS1#/RTS1#/SS1#/ CTX1/USB0_DPUPE/ USB0_OVRCURA | IRQ4 | |
| 21 | VCC_USB | | | | | |
| 22 | | | | USB0_DM | | |
| 23 | | | | USB0_DP | | |
| 24 | VSS_USB | | | | | |
| 25 | | P55 | MTIOC4D/TMO3 | CRX1 | IRQ10 | |
| 26 | | P54 | MTIOC4B/TMC11 | CTX1 | | |
| 27 | | PC7 | MTIOC3A/ MTCLKB/TMO2 /PO31 | TXD8/SMOSI8/SSDA8/ MISOA | IRQ14 | |
| 28 | | PC6 | MTIOC3C/MTCLKA/ TMC12/PO30 | RXD8/SMISO8/SSCL8/ MOSIA/USB0_EXICEN | IRQ13 | |
| 29 | | PC5 | MTIOC3B/MTCLKD/ TMRI2/PO29 | SCK8/RSPCKA/USB0_ID | | |
| 30 | | PC4 | MTIOC3D/MTCLKC/ TMC11/PO25/POE0# | SCK5/CTS8#/RTS8#/SS8#/ SSLA0/USB0_DPRPD | | |
| 31 | | PC3 | MTIOC4D/TCLKB/ PO24 | TXD5/SMOSI5/SSDA5/ IETXD | | |

Table 1.12 List of Pins and Pin Functions (64-Pin LQFP) (2/3)

| Pin Number 64-Pin LQFP | Power Supply Clock System Control | I/O Port | Timer (MTU2a, TPUa, TMR, PPG, RTCa, POE2a) | Timer Communications (SClC, SClD, RSPI, RIIC, CAN, IEB, USB) | Interrupt | S12ADa, DAa |
|------------------------------|---|-------------|--|---|-----------|-------------|
| 32 | | PC2 | MTIOC4B/TCLKA/ PO21 | RXD5/SMISO5/SSCL5/ SSLA3/IERXD | | |
| 33 | | PB7/ PC1 | MTIOC3B/TIOCB5/ PO31 | TXD9/SMOSI9/SSDA9 | | |
| 34 | | PB6/ PC0 | MTIOC3D/TIOCA5/ PO30 | RXD9/SMISO9/SSCL9 | | |
| 35 | | PB5 | MTIOC2A/MTIOC1B/ TIOCB4/TMR11/PO29/ POE1# | SCK9 | | |
| 36 | | PB3 | MTIOC0A/MTIOC4A/ TIOCD3/TCLKD/TMO0/ PO27/POE3# | SCK6 | | |
| 37 | | PB1 | MTIOC0C/MTIOC4C/ TIOCB3/TMCI0/PO25 | TXD6/SMOSI6/SSDA6 | IRQ4-DS | |
| 38 | VCC | | | | | |
| 39 | | PB0 | MTIC5W/TIOCA3/PO24 | RXD6/SMISO6/SSCL6/ RSPCKA | IRQ12 | |
| 40 | VSS | | | | | |
| 41 | | PA6 | MTIC5V/MTCLKB/ TIOCA2/TMCI3/PO22/ POE2# | CTS5#/RTS5#/SS5#/ MOSIA | | |
| 42 | | PA4 | MTIC5U/MTCLKA/ TIOCA1/TMR10/PO20 | TXD5/SMOSI5/SSDA5/ SSLA0 | IRQ5-DS | |
| 43 | | PA3 | MTIOC0D/MTCLKD/ TIOCD0/TCLKB/PO19 | RXD5/SMISO5/SSCL5 | IRQ6-DS | |
| 44 | | PA1 | MTIOC0B/MTCLKC/ TIOCB0/PO17 | SCK5/SSLA2/SCL2 | IRQ11 | |
| 45 | | PA0 | MTIOC4A/TIOCA0/ PO16 | SSLA1 | | |
| 46 | | PE5 | MTIOC4C/MTIOC2B | RSPCKB | IRQ5 | AN013 |
| 47 | | PE4 | MTIOC4D/MTIOC1A/ PO28 | SSLB0 | | AN012 |
| 48 | | PE3 | MTIOC4B/PO26/POE8# | CTS12#/RTS12#/ SS12#/MISOB | | AN011 |
| 49 | | PE2 | MTIOC4A/PO23 | RXD12/SMISO12/ SSCL12/RXDX12/ SSLB3/MOSIB | IRQ7-DS | AN010 |
| 50 | | PE1 | MTIOC4C/PO18 | TXD12/SMOSI12/SSDA12/ TXDX12/SIOX12/SSLB2/ RSPCKB | | AN009 |
| 51 | | PE0 | | SCK12/SSLB1 | | AN008 |
| 52 | VREFL | | | | | |
| 53 | | P46 | | | IRQ14-DS | AN006 |
| 54 | VREFH | | | | | |
| 55 | | P44 | | | IRQ12-DS | AN004 |
| 56 | | P43 | | | IRQ11-DS | AN003 |
| 57 | | P42 | | | IRQ10-DS | AN002 |
| 58 | | P41 | | | IRQ9-DS | AN001 |
| 59 | VREFL0 | | | | | |
| 60 | | P40 | | | IRQ8-DS | AN000 |

Table 1.12 List of Pins and Pin Functions (64-Pin LQFP) (3/3)

| Pin Number 64-Pin LQFP | Power Supply Clock System Control | I/O Port | Timer (MTU2a, TPUa, TMR, PPG, RTCa, POE2a) | Timer Communications (SC1c, SC1d, RSPI, RIIC, CAN, IEB, USB) | Interrupt | S12ADa, DAa |
|---------------------------|---|----------|--|---|-----------|-------------|
| 61 | VREFH0 | | | | | |
| 62 | AVCC0 | | | | | |
| 63 | | P05 | | | IRQ13 | DA1 |
| 64 | AVSS0 | | | | | |

Table 1.13 List of Pins and Pin Functions (48-Pin LQFP) (1/2)

| Pin Number 48-Pin LQFP | Power Supply Clock System Control | I/O Port | Timer (MTU2a, TPUa, TMR, PPG, POE2a) | Communications (SC1c, SC1d, RSPI, RIIC, CAN, IEB, USB) | Interrupt | S12ADa, DAa |
|------------------------------|---|-------------|--|--|-----------|-------------|
| 1 | VCL | | | | | |
| 2 | MD/FINED | | | | | |
| 3 | RES# | | | | | |
| 4 | XTAL | P37 | | | | |
| 5 | VSS | | | | | |
| 6 | EXTAL | P36 | | | | |
| 7 | VCC | | | | | |
| 8 | | P35 | | | NMI | |
| 9 | | P31 | MTIOC4D/TMCI2/PO9 | CTS1#/RTS1#/SS1#/ SSLB0/USB0_DPUPE | IRQ1-DS | |
| 10 | | P30 | MTIOC4B/TMRI3/PO8/ POE8# | RXD1/SMISO1/SSCL1/ MISOB/USB0_DRPD | IRQ0-DS | |
| 11 | FINEC | P27 | MTIOC2B/TMCI3/PO7 | SCK1/RSPCKB | | |
| 12 | | P26 | MTIOC2A/TMO1/PO6 | TXD1/SMOSI1/SSDA1/ MOSIB/USB0_VBUSEN | | |
| 13 | | P17 | MTIOC3A/MTIOC3B/ TIOCB0/TCLKD/TMO1/ PO15/POE8# | SCK1/MISOA/SDA2-DS/ IETXD | IRQ7 | |
| 14 | | P16 | MTIOC3C/MTIOC3D/ TIOCB1/TCLKC/TMO2/ PO14 | TXD1/SMOSI1/SSDA1/ MOSIA/SCL2-DS/IERXD/ USB0_VBUS/ USB0_VBUSEN/ USB0_OVRCURB | IRQ6 | ADTRG0# |
| 15 | | P15 | MTIOC0B/MTCLKB/ TIOCB2/TCLKB/TMCI2/ PO13 | RXD1/SMISO1/SSCL1/ CRX1-DS | IRQ5 | |
| 16 | | P14 | MTIOC3A/MTCLKA/ TIOCB5/TCLKA/TMRI2/ PO15 | CTS1#/RTS1#/SS1#/ CTX1/USB0_DPUPE/ USB0_OVRCURA | IRQ4 | |
| 17 | VCC_USB | | | | | |
| 18 | | | | USB0_DM | | |
| 19 | | | | USB0_DP | | |
| 20 | VSS_USB | | | | | |
| 21 | | PC7 | MTIOC3A/MTCLKB/ TMO2 /PO31 | TXD8/SMOSI8/SSDA8/ MISOA | IRQ14 | |
| 22 | | PC6 | MTIOC3C/MTCLKA/ TMCI2/PO30 | RXD8/SMISO8/SSCL8/ MOSIA/USB0_EXICEN | IRQ13 | |
| 23 | | PC5 | MTIOC3B/MTCLKD/ TMRI2/PO29 | SCK8/RSPCKA/USB0_ID | | |
| 24 | | PC4 | MTIOC3D/MTCLKC/ TMC11/PO25/POE0# | SCK5/CTS8#/RTS8#/SS8#/ /SSLA0/ USB0_DPRPD | | |
| 25 | | PB5/ PC3 | MTIOC2A/MTIOC1B/ TIOCB4/TMRI1/PO29/ POE1# | | | |
| 26 | | PB3/ PC2 | MTIOC0A/MTIOC4A/ TIOCD3/TCLKD/TMO0/ PO27/POE3# | SCK6 | | |
| 27 | | PB1/ PC1 | MTIOC0C/MTIOC4C/ TIOCB3/TMCI0/PO25 | TXD6/SMOSI6/SSDA6 | IRQ4-DS | |
| 28 | VCC | | | | | |

Table 1.13 List of Pins and Pin Functions (48-Pin LQFP) (2/2)

| Pin Number 48-Pin LQFP | Power Supply Clock System Control | I/O Port | Timer (MTU2a, TPUa, TMR, PPG, POE2a) | Communications (SC1c, SC1d, RSPI, RIIC, CAN, IEB, USB) | Interrupt | S12ADa, DAa |
|------------------------------|---|-------------|--|--|-----------|-------------|
| 29 | | PB0/ PC0 | MTIC5W/TIOCA3/PO24 | RXD6/SMISO6/SSCL6/ RSPCKA | IRQ12 | |
| 30 | VSS | | | | | |
| 31 | | PA6 | MTIC5V/MTCLKB/TIOCA2/ TMC13/PO22/POE2# | CTS5#/RTS5#/SS5#/ MOSIA | | |
| 32 | | PA4 | MTIC5U/MTCLKA/ TIOCA1/TMRI0/PO20 | TXD5/SMOSI5/SSDA5/ SSLA0 | IRQ5-DS | |
| 33 | | PA3 | MTIOC0D/MTCLKD/ TIOC0D/TCLKB/PO19 | RXD5/SMISO5/SSCL5 | IRQ6-DS | |
| 34 | | PA1 | MTIOC0B/MTCLKC/ TIOCB0/PO17 | SCK5/SSLA2 | IRQ11 | |
| 35 | | PE4 | MTIOC4D/MTIOC1A/ PO28 | SSLB0 | | AN012 |
| 36 | | PE3 | MTIOC4B/PO26/POE8# | CTS12#/RTS12#/SS12#/ MISOB | | AN011 |
| 37 | | PE2 | MTIOC4A/PO23 | RXD12/SMISO12/SSCL12/ RXDX12/ SSLB3/MOSIB | IRQ7-DS | AN010 |
| 38 | | PE1 | MTIOC4C/PO18 | TXD12/SMISO12/SSDA12/ TXDX12/SIOX12/SSLB2/ RSPCKB | | AN009 |
| 39 | VREFL | | | | | |
| 40 | | P46 | | | IRQ14-DS | AN006 |
| 41 | VREFH | | | | | |
| 42 | | P42 | | | IRQ10-DS | AN002 |
| 43 | | P41 | | | IRQ9-DS | AN001 |
| 44 | VREFL0 | | | | | |
| 45 | | P40 | | | IRQ8-DS | AN000 |
| 46 | VREFH0 | | | | | |
| 47 | AVCC0 | | | | | |
| 48 | AVSS0 | | | | | |

2. CPU

The RX CPU has sixteen general-purpose registers, nine control registers, and one accumulator used for DSP instructions.

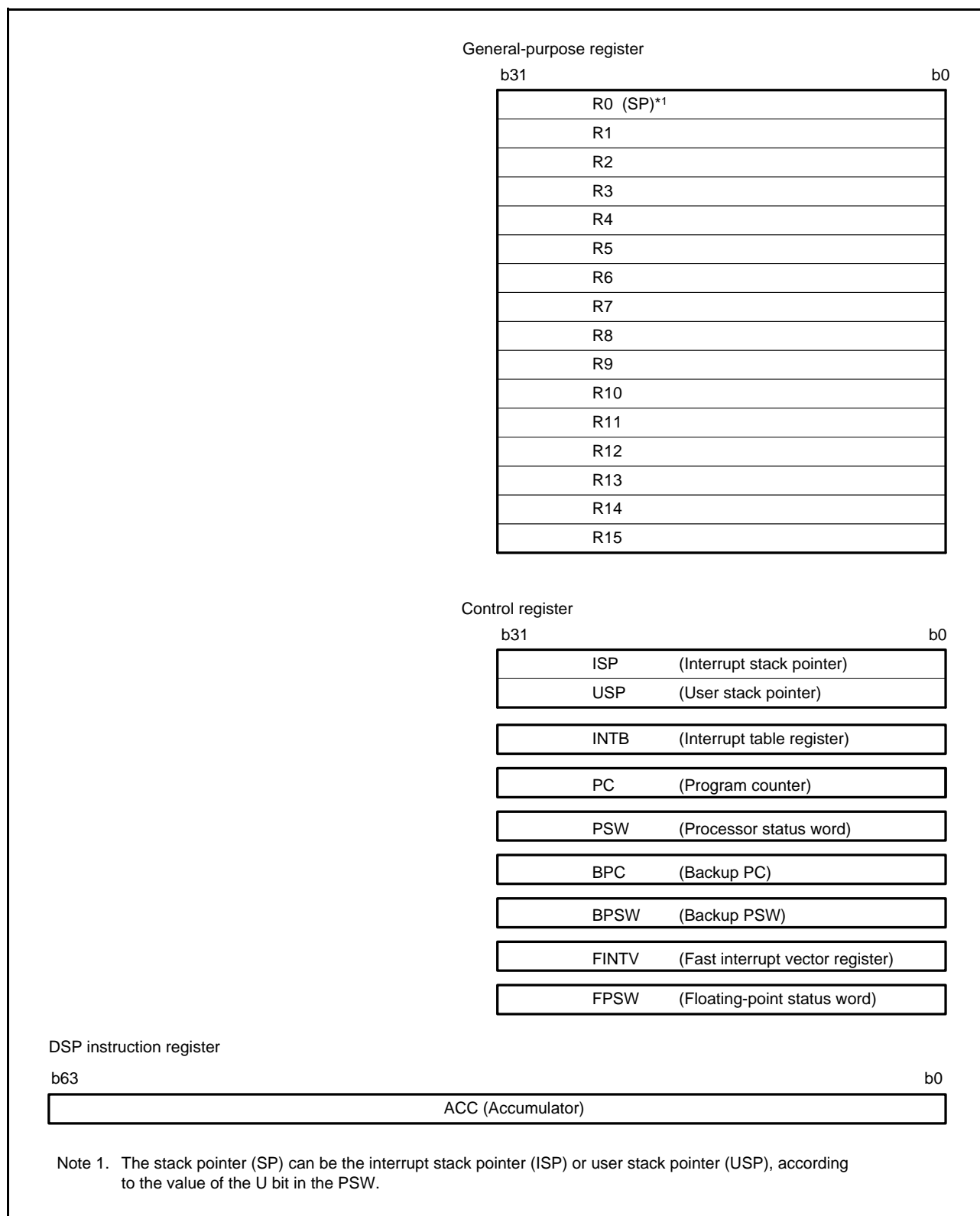


Figure 2.1 Register Set of the CPU

2.1 General-Purpose Registers (R0 to R15)

This CPU has sixteen general-purpose registers (R0 to R15). R1 to R15 can be used as data registers or address registers. R0, a general-purpose register, also functions as the stack pointer (SP).

The stack pointer is switched to operate as the interrupt stack pointer (ISP) or user stack pointer (USP) by the value of the stack pointer select bit (U) in the processor status word (PSW).

2.2 Control Registers

(1) Interrupt Stack Pointer (ISP)/User Stack Pointer (USP)

The stack pointer (SP) can be either of two types, the interrupt stack pointer (ISP) or the user stack pointer (USP). Whether the stack pointer operates as the ISP or USP depends on the value of the stack pointer select bit (U) in the processor status word (PSW).

Set the ISP or USP to a multiple of four, as this reduces the numbers of cycles required to execute interrupt sequences and instructions entailing stack manipulation.

(2) Interrupt Table Register (INTB)

The interrupt table register (INTB) specifies the address where the relocatable vector table starts.

(3) Program Counter (PC)

The program counter (PC) indicates the address of the instruction being executed.

(4) Processor Status Word (PSW)

The processor status word (PSW) indicates the results of instruction execution or the state of the CPU.

(5) Backup PC (BPC)

The backup PC (BPC) is provided to speed up response to interrupts.

After a fast interrupt has been generated, the contents of the program counter (PC) are saved in the BPC register.

(6) Backup PSW (BPSW)

The backup PSW (BPSW) is provided to speed up response to interrupts.

After a fast interrupt has been generated, the contents of the processor status word (PSW) are saved in the BPSW. The allocation of bits in the BPSW corresponds to that in the PSW.

(7) Fast Interrupt Vector Register (FINTV)

The fast interrupt vector register (FINTV) is provided to speed up response to interrupts.

The FINTV register specifies a branch destination address when a fast interrupt has been generated.

(8) Floating-Point Status Word (FPSW)

The floating-point status word (FPSW) indicates the results of floating-point operations.

When an exception handling enable bit (Ej) enables the exception handling (Ej = 1), the exception cause can be identified by checking the corresponding Cj flag in the exception handling routine. If the exception handling is masked (Ej = 0), the occurrence of exception can be checked by reading the Fj flag at the end of a series of processing. Once the Fj flag has been set to 1, this value is retained until it is cleared to 0 by software (j = X, U, Z, O, or V).

2.3 Register Associated with DSP Instructions

(1) Accumulator (ACC)

The accumulator (ACC) is a 64-bit register used for DSP instructions. The accumulator is also used for the multiply and multiply-and-accumulate instructions; EMUL, EMULU, FMUL, MUL, and RMPA, in which case the prior value in the accumulator is modified by execution of the instruction.

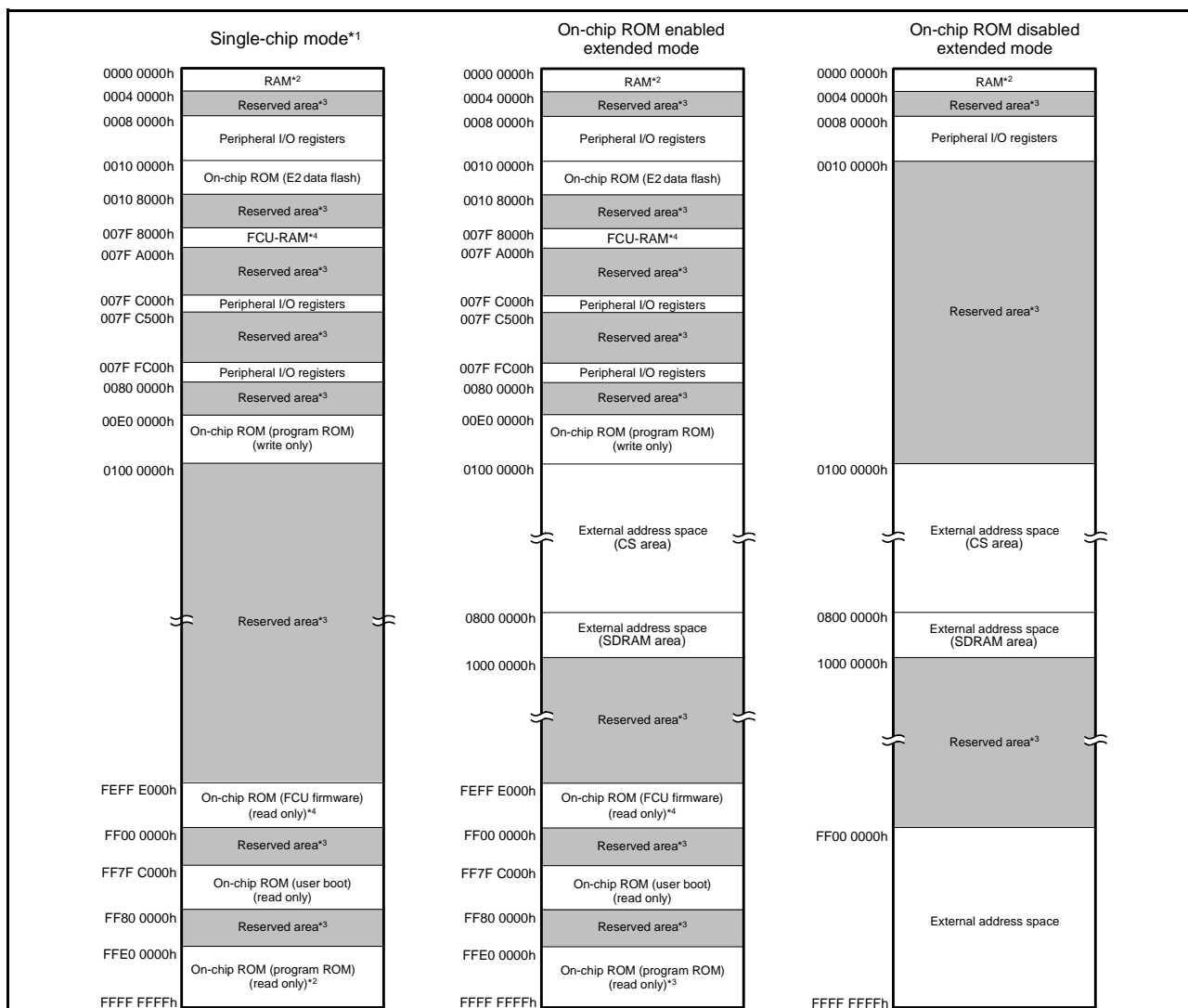
Use the MVTACHI and MVTACLO instructions for writing to the accumulator. The MVTACHI and MVTACLO instructions write data to the higher-order 32 bits (bits 63 to 32) and the lower-order 32 bits (bits 31 to 0), respectively. Use the MVFACHI and MVFACMI instructions for reading data from the accumulator. The MVFACHI and MVFACMI instructions read data from the higher-order 32 bits (bits 63 to 32) and the middle 32 bits (bits 47 to 16), respectively.

3. Address Space

3.1 Address Space

This LSI has a 4-Gbyte address space, consisting of the range of addresses from 0000 0000h to FFFF FFFFh. That is, linear access to an address space of up to 4 Gbytes is possible, and this contains both program and data areas.

Figure 3.1 shows the memory maps in the respective operating modes. Accessible areas will differ according to the operating mode and states of control bits.



Note 1. The address space in boot mode and user boot mode/USB boot mode is the same as the address space in single-chip mode.
 Note 2. The capacity of ROM/RAM differs depending on the products.

| ROM (byt) | | | RAM (byt) | |
|-----------|----------------------------|--------------------------------|-----------|--------------------------|
| Capacity | Address (for reading only) | Address (for programming only) | Capacity | Address |
| 2 M | FFE0 0000h to FFFF FFFFh | 00E0 0000h to 00FF FFFFh | 256 K | 0000 0000h to 0003 FFFFh |
| | | | 192 K | 0000 0000h to 0002 FFFFh |
| | | | 128 K | 0000 0000h to 0001 FFFFh |
| 1.5 M | FFE8 0000h to FFFF FFFFh | 00E8 0000h to 00FF FFFFh | 256 K | 0000 0000h to 0003 FFFFh |
| | | | 192 K | 0000 0000h to 0002 FFFFh |
| | | | 128 K | 0000 0000h to 0001 FFFFh |
| 1 M | FFF0 0000h to FFFF FFFFh | 00F0 0000h to 00FF FFFFh | 256 K | 0000 0000h to 0003 FFFFh |
| | | | 192 K | 0000 0000h to 0002 FFFFh |
| | | | 128 K | 0000 0000h to 0001 FFFFh |
| 768 K | FFF4 0000h to FFFF FFFFh | 00F4 0000h to 00FF FFFFh | 64K | 0000 0000h to 0000 FFFFh |
| 512K | FFF8 0000h to FFFF FFFFh | 00F8 0000h to 00FF FFFFh | | |
| 384K | FFFA 0000h to FFFF FFFFh | 00FA 0000h to 00FF FFFFh | | |
| 256K | FFFC 0000h to FFFF FFFFh | 00FC 0000h to 00FF FFFFh | | |
| 512K | FFF8 0000h to FFFF FFFFh | 00F8 0000h to 00FF FFFFh | | |
| 384K | FFFA 0000h to FFFF FFFFh | 00FA 0000h to 00FF FFFFh | | |
| 256K | FFFC 0000h to FFFF FFFFh | 00FC 0000h to 00FF FFFFh | | |

Note: See Table 1.3, List of Products, for the product type name.

Note 3. Reserved areas should not be accessed.
 Note 4. For details on the FCU, see section 47, Flash Memory in the User's manual: Hardware.

Figure 3.1 Memory Map in Each Operating Mode

3.2 External Address Space

The external address space is classified into CS areas (CS0 to CS7) and SDRAM area (SDCS). CS areas can be divided into up to eight areas (CS0 to CS7) corresponding to the CSn# signal to be output from the CSn# pin.

Figure 3.2 shows the address ranges corresponding to the individual CS areas (CS0 to CS7) and SDRAM area (SDCS) in on-chip ROM disabled extended mode.

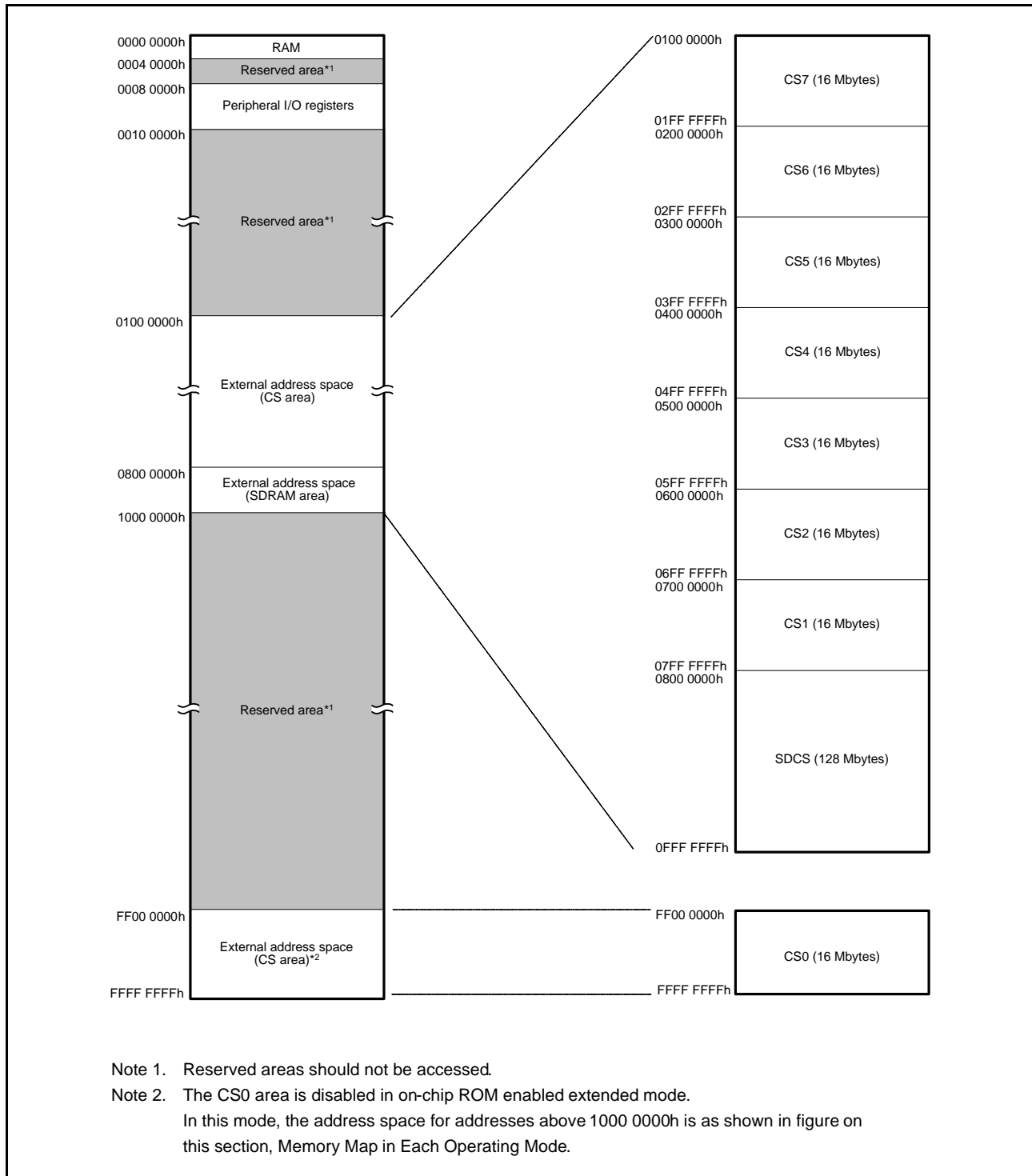


Figure 3.2 Correspondence between External Address Spaces and CS Areas (In On-Chip ROM Disabled Extended Mode)

4. I/O Registers

This section gives information on the on-chip I/O register addresses. The information is given as shown below. Notes on writing to registers are also given at the end.

(1) I/O register addresses (address order)

- Registers are listed from the lower allocation addresses.
- Registers are classified according to module symbols.
- The number of access cycles indicates the number of cycles based on the specified reference clock.
- Among the internal I/O register area, addresses not listed in the list of registers are reserved. Reserved addresses must not be accessed. Do not access these addresses; otherwise, the operation when accessing these bits and subsequent operations cannot be guaranteed.

(2) Notes on writing to I/O registers

When writing to an I/O register, the CPU starts executing the subsequent instruction before completing I/O register write. This may cause the subsequent instruction to be executed before the post-update I/O register value is reflected on the operation.

As described in the following examples, special care is required for the cases in which the subsequent instruction must be executed after the post-update I/O register value is actually reflected.

[Examples of cases requiring special care]

- The subsequent instruction must be executed while an interrupt request is disabled with the IENj bit in IERN of the ICU (interrupt request enable bit) cleared to 0.
- A WAIT instruction is executed immediately after the preprocessing for causing a transition to the low power consumption state.

In the above cases, after writing to an I/O register, wait until the write operation is completed using the following procedure and then execute the subsequent instruction.

- Write to an I/O register.
- Read the value from the I/O register to a general register.
- Execute the operation using the value read.
- Execute the subsequent instruction.

[Instruction examples]

- Byte-size I/O registers

```
MOV.L #SFR_ADDR, R1
MOV.B #SFR_DATA, [R1]
CMP [R1].UB, R1
;; Next process
```

- Word-size I/O registers

```
MOV.L #SFR_ADDR, R1
MOV.W #SFR_DATA, [R1]
CMP [R1].W, R1
;; Next process
```

- Longword-size I/O registers

```
MOV.L #SFR_ADDR, R1
MOV.L #SFR_DATA, [R1]
CMP [R1].L, R1
;; Next process
```

If multiple registers are written to and a subsequent instruction should be executed after the write operations are entirely completed, only read the I/O register that was last written to and execute the operation using the value; it is not necessary to read or execute operation for all the registers that were written to.

(3) Number of Access Cycles to I/O Registers

For the number of I/O register access cycles, refer to Table 4.1, List of I/O Registers (Address Order). The number of access cycles to I/O registers is obtained by following equation.*1

$$\begin{aligned} \text{Number of access cycles to I/O registers} = & \text{Number of bus cycles for internal main bus 1} + \\ & \text{Number of divided clock synchronization cycles} + \\ & \text{Number of bus cycles for internal peripheral busses 1 to 6} \end{aligned}$$

The number of bus cycles of internal peripheral bus 1 to 6 differs according to the register to be accessed. When peripheral functions connected to internal peripheral bus 2 to 6 or registers for the external bus control unit (except for bus error related registers) are accessed, the number of divided clock synchronization cycles is added.

The number of divided clock synchronization cycles differs depending on the frequency ratio between ICLK and PCLK (or FCLK, BCLK) or bus access timing.

In the peripheral function unit, when the frequency ratio of ICLK is equal to or greater than that of PCLK (or FCLK), the sum of the number of bus cycles for internal main bus 1 and the number of the divided clock synchronization cycles will be one cycle of PCLK (or FCLK) at a maximum. Therefore, one PCLK (or FCLK) has been added to the number of access states shown in Table 4.1.

When the frequency ratio of ICLK is lower than that of PCLK (or FCLK), the subsequent bus access is started from the ICLK cycle following the completion of the access to the peripheral functions. Therefore, the access cycles are described on an ICLK basis.

In the external bus control unit, the sum of the number of bus cycles for internal main bus 1 and the number of divided clock synchronization cycles will be one cycle of BCLK at a maximum. Therefore, one BCLK is added to the number of access cycles shown in Table 4.1.

Note 1. This applies to the number of cycles when the access from the CPU does not conflict with the instruction fetching to the external memory or bus access from the different bus master (DMAC or DTC).

(4) Restrictions in Relation to RMPA and String-Manipulation Instructions

The allocation of data to be handled by RMPA or string-manipulation instructions to I/O registers is prohibited, and operation is not guaranteed if this restriction is not observed.

4.1 I/O Register Addresses (Address Order)

Table 4.1 List of I/O Registers (Address Order) (1/50)

| Address | Module Symbol | Register Name | Register Symbol | Number of Bits | Access Size | Number of Access States | | Related Function | |
|------------|---------------|--|-----------------|----------------|-------------|-------------------------|-----------|------------------------------------|-----------------------|
| | | | | | | ICLK≥PCLK | ICLK<PCLK | | |
| 0008 0000h | SYSTEM | Mode monitor register | MDMONR | 16 | 16 | 3 | ICLK | Operating Modes | |
| 0008 0002h | SYSTEM | Mode status register | MDSR | 16 | 16 | 3 | ICLK | | |
| 0008 0006h | SYSTEM | System control register 0 | SYSCR0 | 16 | 16 | 3 | ICLK | | |
| 0008 0008h | SYSTEM | System control register 1 | SYSCR1 | 16 | 16 | 3 | ICLK | | |
| 0008 000Ch | SYSTEM | Standby control register | SBYCR | 16 | 16 | 3 | ICLK | Low Power Consumption | |
| 0008 0010h | SYSTEM | Module stop control register A | MSTPCRA | 32 | 32 | 3 | ICLK | | |
| 0008 0014h | SYSTEM | Module stop control register B | MSTPCRB | 32 | 32 | 3 | ICLK | | |
| 0008 0018h | SYSTEM | Module stop control register C | MSTPCRC | 32 | 32 | 3 | ICLK | | |
| 0008 001Ch | SYSTEM | Module stop control register D | MSTPCRD | 32 | 32 | 3 | ICLK | | |
| 0008 0020h | SYSTEM | System clock control register | SCKCR | 32 | 32 | 3 | ICLK | Clock Generation Circuit | |
| 0008 0024h | SYSTEM | System clock control register 2 | SCKCR2 | 16 | 16 | 3 | ICLK | | |
| 0008 0026h | SYSTEM | System clock control register 3 | SCKCR3 | 16 | 16 | 3 | ICLK | | |
| 0008 0028h | SYSTEM | PLL control register | PLLCR | 16 | 16 | 3 | ICLK | | |
| 0008 002Ah | SYSTEM | PLL control register 2 | PLLCR2 | 8 | 8 | 3 | ICLK | | |
| 0008 0030h | SYSTEM | External bus clock control register | BCKCR | 8 | 8 | 3 | ICLK | | |
| 0008 0032h | SYSTEM | Main clock oscillator control register | MOSCCR | 8 | 8 | 3 | ICLK | | |
| 0008 0033h | SYSTEM | Sub-clock oscillator control register | SOSCCR | 8 | 8 | 3 | ICLK | | |
| 0008 0034h | SYSTEM | Low-speed on-chip oscillator control register | LOCOCR | 8 | 8 | 3 | ICLK | | |
| 0008 0035h | SYSTEM | IWDT-dedicated on-chip oscillator control register | ILOCOCR | 8 | 8 | 3 | ICLK | | |
| 0008 0036h | SYSTEM | High-speed on-chip oscillator control register | HOCOCR | 8 | 8 | 3 | ICLK | | |
| 0008 0040h | SYSTEM | Oscillation stop detection control register | OSTDCR | 8 | 8 | 3 | ICLK | | |
| 0008 0041h | SYSTEM | Oscillation stop detection status register | OSTDSR | 8 | 8 | 3 | ICLK | | |
| 0008 00A0h | SYSTEM | Operating power control register | OPCCR | 8 | 8 | 3 | ICLK | | Low Power Consumption |
| 0008 00A1h | SYSTEM | Sleep mode return clock source switching register | RSTCKCR | 8 | 8 | 3 | ICLK | | |
| 0008 00A2h | SYSTEM | Main clock oscillator wait control register | MOSCWTCR | 8 | 8 | 3 | ICLK | | |
| 0008 00A3h | SYSTEM | Sub-clock oscillator wait control register | SOSCWTCR | 8 | 8 | 3 | ICLK | | |
| 0008 00A6h | SYSTEM | PLL wait control register | PLLWTCR | 8 | 8 | 3 | ICLK | | |
| 0008 00C0h | SYSTEM | Reset status register 2 | RSTSR2 | 8 | 8 | 3 | ICLK | Resets | |
| 0008 00C2h | SYSTEM | Software reset register | SWRR | 16 | 16 | 3 | ICLK | | |
| 0008 00E0h | SYSTEM | Voltage monitoring 1 circuit control register 1 | LVD1CR1 | 8 | 8 | 3 | ICLK | LVDA | |
| 0008 00E1h | SYSTEM | Voltage monitoring 1 circuit status register | LVD1SR | 8 | 8 | 3 | ICLK | | |
| 0008 00E2h | SYSTEM | Voltage monitoring 2 circuit control register 1 | LVD2CR1 | 8 | 8 | 3 | ICLK | | |
| 0008 00E3h | SYSTEM | Voltage monitoring 2 circuit status register | LVD2SR | 8 | 8 | 3 | ICLK | | |
| 0008 03FEh | SYSTEM | Protect register | PRCR | 16 | 16 | 3 | ICLK | Register Write Protection Function | |
| 0008 1300h | BSC | Bus error status clear register | BERCLR | 8 | 8 | 2 | ICLK | Buses | |
| 0008 1304h | BSC | Bus error monitoring enable register | BEREN | 8 | 8 | 2 | ICLK | | |
| 0008 1308h | BSC | Bus error status register 1 | BERSR1 | 8 | 8 | 2 | ICLK | | |
| 0008 130Ah | BSC | Bus error status register 2 | BERSR2 | 16 | 16 | 2 | ICLK | | |
| 0008 1310h | BSC | Bus priority control register | BUSPRI | 16 | 16 | 2 | ICLK | | |
| 0008 2000h | DMAC0 | DMA source address register | DMSAR | 32 | 32 | 2 | ICLK | DMACA | |
| 0008 2004h | DMAC0 | DMA destination address register | DMDAR | 32 | 32 | 2 | ICLK | | |
| 0008 2008h | DMAC0 | DMA transfer count register | DMCRA | 32 | 32 | 2 | ICLK | | |
| 0008 200Ch | DMAC0 | DMA block transfer count register | DMCRB | 16 | 16 | 2 | ICLK | | |
| 0008 2010h | DMAC0 | DMA transfer mode register | DMTMD | 16 | 16 | 2 | ICLK | | |
| 0008 2013h | DMAC0 | DMA interrupt setting register | DMINT | 8 | 8 | 2 | ICLK | | |
| 0008 2014h | DMAC0 | DMA address mode register | DMAMD | 16 | 16 | 2 | ICLK | | |
| 0008 2018h | DMAC0 | DMA offset register | DMOFR | 32 | 32 | 2 | ICLK | | |

Table 4.1 List of I/O Registers (Address Order) (2/50)

| Address | Module Symbol | Register Name | Register Symbol | Number of Bits | Access Size | Number of Access States | | Related Function |
|------------|---------------|---|-----------------|----------------|-------------|-------------------------|-----------|------------------|
| | | | | | | ICLK≥PCLK | ICLK<PCLK | |
| 0008 201Ch | DMAC0 | DMA transfer enable register | DMCNT | 8 | 8 | 2 | ICLK | DMACA |
| 0008 201Dh | DMAC0 | DMA software start register | DMREQ | 8 | 8 | 2 | ICLK | DMACA |
| 0008 201Eh | DMAC0 | DMA status register | DMSTS | 8 | 8 | 2 | ICLK | DMACA |
| 0008 201Fh | DMAC0 | DMA activation source flag control register | DMCSL | 8 | 8 | 2 | ICLK | DMACA |
| 0008 2040h | DMAC1 | DMA source address register | DMSAR | 32 | 32 | 2 | ICLK | DMACA |
| 0008 2044h | DMAC1 | DMA destination address register | DMDAR | 32 | 32 | 2 | ICLK | DMACA |
| 0008 2048h | DMAC1 | DMA transfer count register | DMCRA | 32 | 32 | 2 | ICLK | DMACA |
| 0008 204Ch | DMAC1 | DMA block transfer count register | DMCRB | 16 | 16 | 2 | ICLK | DMACA |
| 0008 2050h | DMAC1 | DMA transfer mode register | DMTMD | 16 | 16 | 2 | ICLK | DMACA |
| 0008 2053h | DMAC1 | DMA interrupt setting register | DMINT | 8 | 8 | 2 | ICLK | DMACA |
| 0008 2054h | DMAC1 | DMA address mode register | DMAMD | 16 | 16 | 2 | ICLK | DMACA |
| 0008 205Ch | DMAC1 | DMA transfer enable register | DMCNT | 8 | 8 | 2 | ICLK | DMACA |
| 0008 205Dh | DMAC1 | DMA software start register | DMREQ | 8 | 8 | 2 | ICLK | DMACA |
| 0008 205Eh | DMAC1 | DMA status register | DMSTS | 8 | 8 | 2 | ICLK | DMACA |
| 0008 205Fh | DMAC1 | DMA activation source flag control register | DMCSL | 8 | 8 | 2 | ICLK | DMACA |
| 0008 2080h | DMAC2 | DMA source address register | DMSAR | 32 | 32 | 2 | ICLK | DMACA |
| 0008 2084h | DMAC2 | DMA destination address register | DMDAR | 32 | 32 | 2 | ICLK | DMACA |
| 0008 2088h | DMAC2 | DMA transfer count register | DMCRA | 32 | 32 | 2 | ICLK | DMACA |
| 0008 208Ch | DMAC2 | DMA block transfer count register | DMCRB | 16 | 16 | 2 | ICLK | DMACA |
| 0008 2090h | DMAC2 | DMA transfer mode register | DMTMD | 16 | 16 | 2 | ICLK | DMACA |
| 0008 2093h | DMAC2 | DMA interrupt setting register | DMINT | 8 | 8 | 2 | ICLK | DMACA |
| 0008 2094h | DMAC2 | DMA address mode register | DMAMD | 16 | 16 | 2 | ICLK | DMACA |
| 0008 209Ch | DMAC2 | DMA transfer enable register | DMCNT | 8 | 8 | 2 | ICLK | DMACA |
| 0008 209Dh | DMAC2 | DMA software start register | DMREQ | 8 | 8 | 2 | ICLK | DMACA |
| 0008 209Eh | DMAC2 | DMA status register | DMSTS | 8 | 8 | 2 | ICLK | DMACA |
| 0008 209Fh | DMAC2 | DMA activation source flag control register | DMCSL | 8 | 8 | 2 | ICLK | DMACA |
| 0008 20C0h | DMAC3 | DMA source address register | DMSAR | 32 | 32 | 2 | ICLK | DMACA |
| 0008 20C4h | DMAC3 | DMA destination address register | DMDAR | 32 | 32 | 2 | ICLK | DMACA |
| 0008 20C8h | DMAC3 | DMA transfer count register | DMCRA | 32 | 32 | 2 | ICLK | DMACA |
| 0008 20CCh | DMAC3 | DMA block transfer count register | DMCRB | 16 | 16 | 2 | ICLK | DMACA |
| 0008 20D0h | DMAC3 | DMA transfer mode register | DMTMD | 16 | 16 | 2 | ICLK | DMACA |
| 0008 20D3h | DMAC3 | DMA interrupt setting register | DMINT | 8 | 8 | 2 | ICLK | DMACA |
| 0008 20D4h | DMAC3 | DMA address mode register | DMAMD | 16 | 16 | 2 | ICLK | DMACA |
| 0008 20DCh | DMAC3 | DMA transfer enable register | DMCNT | 8 | 8 | 2 | ICLK | DMACA |
| 0008 20DDh | DMAC3 | DMA software start register | DMREQ | 8 | 8 | 2 | ICLK | DMACA |
| 0008 20DEh | DMAC3 | DMA status register | DMSTS | 8 | 8 | 2 | ICLK | DMACA |
| 0008 20DFh | DMAC3 | DMA activation source flag control register | DMCSL | 8 | 8 | 2 | ICLK | DMACA |
| 0008 2200h | DMAC | DMACA module activation register | DMAST | 8 | 8 | 2 | ICLK | DMACA |
| 0008 2400h | DTC | DTC control register | DTCCR | 8 | 8 | 2 | ICLK | DTCa |
| 0008 2404h | DTC | DTC vector base register | DTCVBR | 32 | 32 | 2 | ICLK | DTCa |
| 0008 2408h | DTC | DTC address mode register | DTCADMOD | 8 | 8 | 2 | ICLK | DTCa |
| 0008 240Ch | DTC | DTC module start register | DTCST | 8 | 8 | 2 | ICLK | DTCa |
| 0008 240Eh | DTC | DTC status register | DTCSTS | 16 | 16 | 2 | ICLK | DTCa |
| 0008 2800h | EXDMAC0 | EXDMA source address register | EDMSAR | 32 | 32 | 1, 2 | BCLK | EXDMACa |
| 0008 2804h | EXDMAC0 | EXDMA destination address register | EDMDAR | 32 | 32 | 1, 2 | BCLK | EXDMACa |
| 0008 2808h | EXDMAC0 | EXDMA transfer count register | EDMCRA | 32 | 32 | 1, 2 | BCLK | EXDMACa |
| 0008 280Ch | EXDMAC0 | EXDMA block transfer count register | EDMCRB | 16 | 16 | 1, 2 | BCLK | EXDMACa |
| 0008 2810h | EXDMAC0 | EXDMA transfer mode register | EDMTMD | 16 | 16 | 1, 2 | BCLK | EXDMACa |
| 0008 2812h | EXDMAC0 | EXDMA output setting register | EDMOMD | 8 | 8 | 1, 2 | BCLK | EXDMACa |
| 0008 2813h | EXDMAC0 | EXDMA interrupt setting register | EDMINT | 8 | 8 | 1, 2 | BCLK | EXDMACa |
| 0008 2814h | EXDMAC0 | EXDMA address mode register | EDMAMD | 32 | 32 | 1, 2 | BCLK | EXDMACa |

Table 4.1 List of I/O Registers (Address Order) (3/50)

| Address | Module Symbol | Register Name | Register Symbol | Number of Bits | Access Size | Number of Access States | | Related Function |
|------------|---------------|--|-----------------|----------------|-------------|-------------------------|-----------|------------------|
| | | | | | | ICLK≥PCLK | ICLK<PCLK | |
| 0008 2818h | EXDMAC0 | EXDMA offset register | EDMOFR | 32 | 32 | 1, 2 | BCLK | EXDMACa |
| 0008 281Ch | EXDMAC0 | EXDMA transfer enable register | EDMCNT | 8 | 8 | 1, 2 | BCLK | |
| 0008 281Dh | EXDMAC0 | EXDMA software start register | EDMREQ | 8 | 8 | 1, 2 | BCLK | |
| 0008 281Eh | EXDMAC0 | EXDMA status register | EDMSTS | 8 | 8 | 1, 2 | BCLK | |
| 0008 2820h | EXDMAC0 | EXDMA external request sense mode register | EDMRMD | 8 | 8 | 1, 2 | BCLK | |
| 0008 2821h | EXDMAC0 | EXDMA external request flag register | EDMERF | 8 | 8 | 1, 2 | BCLK | |
| 0008 2822h | EXDMAC0 | EXDMA peripheral request flag register | EDMPRF | 8 | 8 | 1, 2 | BCLK | |
| 0008 2840h | EXDMAC1 | EXDMA source address register | EDMSAR | 32 | 32 | 1, 2 | BCLK | |
| 0008 2844h | EXDMAC1 | EXDMA destination address register | EDMDAR | 32 | 32 | 1, 2 | BCLK | |
| 0008 2848h | EXDMAC1 | EXDMA transfer count register | EDMCRA | 32 | 32 | 1, 2 | BCLK | |
| 0008 284Ch | EXDMAC1 | EXDMA block transfer count register | EDMCRB | 16 | 16 | 1, 2 | BCLK | |
| 0008 2850h | EXDMAC1 | EXDMA transfer mode register | EDMTMD | 16 | 16 | 1, 2 | BCLK | |
| 0008 2852h | EXDMAC1 | EXDMA output setting register | EDMOMD | 8 | 8 | 1, 2 | BCLK | |
| 0008 2853h | EXDMAC1 | EXDMA interrupt setting register | EDMINT | 8 | 8 | 1, 2 | BCLK | |
| 0008 2854h | EXDMAC1 | EXDMA address mode register | EDMAMD | 32 | 32 | 1, 2 | BCLK | |
| 0008 285Ch | EXDMAC1 | EXDMA transfer enable register | EDMCNT | 8 | 8 | 1, 2 | BCLK | |
| 0008 285Dh | EXDMAC1 | EXDMA software start register | EDMREQ | 8 | 8 | 1, 2 | BCLK | |
| 0008 285Eh | EXDMAC1 | EXDMA status register | EDMSTS | 8 | 8 | 1, 2 | BCLK | |
| 0008 2860h | EXDMAC1 | EXDMA external request sense mode register | EDMRMD | 8 | 8 | 1, 2 | BCLK | |
| 0008 2861h | EXDMAC1 | EXDMA external request flag register | EDMERF | 8 | 8 | 1, 2 | BCLK | |
| 0008 2862h | EXDMAC1 | EXDMA peripheral request flag register | EDMPRF | 8 | 8 | 1, 2 | BCLK | |
| 0008 2A00h | EXDMAC | EXDMA module start register | EDMAST | 8 | 8 | 1, 2 | BCLK | |
| 0008 2BE0h | EXDMAC | Cluster buffer register 0 | CLSBR0 | 32 | 32 | 1, 2 | BCLK | |
| 0008 2BE4h | EXDMAC | Cluster buffer register 1 | CLSBR1 | 32 | 32 | 1, 2 | BCLK | |
| 0008 2BE8h | EXDMAC | Cluster buffer register 2 | CLSBR2 | 32 | 32 | 1, 2 | BCLK | |
| 0008 2BECh | EXDMAC | Cluster buffer register 3 | CLSBR3 | 32 | 32 | 1, 2 | BCLK | |
| 0008 2BF0h | EXDMAC | Cluster buffer register 4 | CLSBR4 | 32 | 32 | 1, 2 | BCLK | |
| 0008 2BF4h | EXDMAC | Cluster buffer register 5 | CLSBR5 | 32 | 32 | 1, 2 | BCLK | |
| 0008 2BF8h | EXDMAC | Cluster buffer register 6 | CLSBR6 | 32 | 32 | 1, 2 | BCLK | |
| 0008 2BFCh | EXDMAC | Cluster buffer register 7 | CLSBR7 | 32 | 32 | 1, 2 | BCLK | |
| 0008 3002h | BSC | CS0 mode register | CS0MOD | 16 | 16 | 1, 2 | BCLK | Buses |
| 0008 3004h | BSC | CS0 wait control register 1 | CS0WCR1 | 32 | 32 | 1, 2 | BCLK | |
| 0008 3008h | BSC | CS0 wait control register 2 | CS0WCR2 | 32 | 32 | 1, 2 | BCLK | |
| 0008 3012h | BSC | CS1 mode register | CS1MOD | 16 | 16 | 1, 2 | BCLK | |
| 0008 3014h | BSC | CS1 wait control register 1 | CS1WCR1 | 32 | 32 | 1, 2 | BCLK | |
| 0008 3018h | BSC | CS1 wait control register 2 | CS1WCR2 | 32 | 32 | 1, 2 | BCLK | |
| 0008 3022h | BSC | CS2 mode register | CS2MOD | 16 | 16 | 1, 2 | BCLK | |
| 0008 3024h | BSC | CS2 wait control register 1 | CS2WCR1 | 32 | 32 | 1, 2 | BCLK | |
| 0008 3028h | BSC | CS2 wait control register 2 | CS2WCR2 | 32 | 32 | 1, 2 | BCLK | |
| 0008 3032h | BSC | CS3 mode register | CS3MOD | 16 | 16 | 1, 2 | BCLK | |
| 0008 3034h | BSC | CS3 wait control register 1 | CS3WCR1 | 32 | 32 | 1, 2 | BCLK | |
| 0008 3038h | BSC | CS3 wait control register 2 | CS3WCR2 | 32 | 32 | 1, 2 | BCLK | |
| 0008 3042h | BSC | CS4 mode register | CS4MOD | 16 | 16 | 1, 2 | BCLK | |
| 0008 3044h | BSC | CS4 wait control register 1 | CS4WCR1 | 32 | 32 | 1, 2 | BCLK | |
| 0008 3048h | BSC | CS4 wait control register 2 | CS4WCR2 | 32 | 32 | 1, 2 | BCLK | |
| 0008 3052h | BSC | CS5 mode register | CS5MOD | 16 | 16 | 1, 2 | BCLK | |
| 0008 3054h | BSC | CS5 wait control register 1 | CS5WCR1 | 32 | 32 | 1, 2 | BCLK | |
| 0008 3058h | BSC | CS5 wait control register 2 | CS5WCR2 | 32 | 32 | 1, 2 | BCLK | |
| 0008 3062h | BSC | CS6 mode register | CS6MOD | 16 | 16 | 1, 2 | BCLK | |
| 0008 3064h | BSC | CS6 wait control register 1 | CS6WCR1 | 32 | 32 | 1, 2 | BCLK | |
| 0008 3068h | BSC | CS6 wait control register 2 | CS6WCR2 | 32 | 32 | 1, 2 | BCLK | |

Table 4.1 List of I/O Registers (Address Order) (4/50)

| Address | Module Symbol | Register Name | Register Symbol | Number of Bits | Access Size | Number of Access States | | Related Function |
|------------|---------------|--|-----------------|----------------|-------------|-------------------------|-----------|------------------|
| | | | | | | ICLK \geq PCLK | ICLK<PCLK | |
| 0008 3072h | BSC | CS7 mode register | CS7MOD | 16 | 16 | 1, 2 BCLK | | Buses |
| 0008 3074h | BSC | CS7 wait control register 1 | CS7WCR1 | 32 | 32 | 1, 2 BCLK | | |
| 0008 3078h | BSC | CS7 wait control register 2 | CS7WCR2 | 32 | 32 | 1, 2 BCLK | | |
| 0008 3802h | BSC | CS0 control register | CS0CR | 16 | 16 | 1, 2 BCLK | | |
| 0008 380Ah | BSC | CS0 recovery cycle register | CS0REC | 16 | 16 | 1, 2 BCLK | | |
| 0008 3812h | BSC | CS1 control register | CS1CR | 16 | 16 | 1, 2 BCLK | | |
| 0008 381Ah | BSC | CS1 recovery cycle register | CS1REC | 16 | 16 | 1, 2 BCLK | | |
| 0008 3822h | BSC | CS2 control register | CS2CR | 16 | 16 | 1, 2 BCLK | | |
| 0008 382Ah | BSC | CS2 recovery cycle register | CS2REC | 16 | 16 | 1, 2 BCLK | | |
| 0008 3832h | BSC | CS3 control register | CS3CR | 16 | 16 | 1, 2 BCLK | | |
| 0008 383Ah | BSC | CS3 recovery cycle register | CS3REC | 16 | 16 | 1, 2 BCLK | | |
| 0008 3842h | BSC | CS4 control register | CS4CR | 16 | 16 | 1, 2 BCLK | | |
| 0008 384Ah | BSC | CS4 recovery cycle register | CS4REC | 16 | 16 | 1, 2 BCLK | | |
| 0008 3852h | BSC | CS5 control register | CS5CR | 16 | 16 | 1, 2 BCLK | | |
| 0008 385Ah | BSC | CS5 recovery cycle register | CS5REC | 16 | 16 | 1, 2 BCLK | | |
| 0008 3862h | BSC | CS6 control register | CS6CR | 16 | 16 | 1, 2 BCLK | | |
| 0008 386Ah | BSC | CS6 recovery cycle register | CS6REC | 16 | 16 | 1, 2 BCLK | | |
| 0008 3872h | BSC | CS7 control register | CS7CR | 16 | 16 | 1, 2 BCLK | | |
| 0008 387Ah | BSC | CS7 recovery cycle register | CS7REC | 16 | 16 | 1, 2 BCLK | | |
| 0008 3880h | BSC | CS recovery cycle insertion enable register | CSRECEN | 16 | 16 | 1, 2 BCLK | | |
| 0008 3C00h | BSC | SDC control register | SDCCR | 8 | 8 | 1, 2 BCLK | | |
| 0008 3C01h | BSC | SDC mode register | SDCMOD | 8 | 8 | 1, 2 BCLK | | |
| 0008 3C02h | BSC | SDRAM access mode register | SDAMOD | 8 | 8 | 1, 2 BCLK | | |
| 0008 3C10h | BSC | SDRAM self-refresh control register | SDSELF | 8 | 8 | 1, 2 BCLK | | |
| 0008 3C14h | BSC | SDRAM refresh control register | SDRFCR | 16 | 16 | 1, 2 BCLK | | |
| 0008 3C16h | BSC | SDRAM auto-refresh control register | SDRFEN | 8 | 8 | 1, 2 BCLK | | |
| 0008 3C20h | BSC | SDRAM initialization sequence control register | SDICR | 8 | 8 | 1, 2 BCLK | | |
| 0008 3C24h | BSC | SDRAM initialization register | SDIR | 16 | 16 | 1, 2 BCLK | | |
| 0008 3C40h | BSC | SDRAM address register | SDADR | 8 | 8 | 1, 2 BCLK | | |
| 0008 3C44h | BSC | SDRAM timing register | SDTR | 32 | 32 | 1, 2 BCLK | | |
| 0008 3C48h | BSC | SDRAM mode register | SDMOD | 16 | 16 | 1, 2 BCLK | | |
| 0008 3C50h | BSC | SDRAM status register | SDSR | 8 | 8 | 1, 2 BCLK | | |
| 0008 6400h | MPU | Region-0 start page number register | RSPAGE0 | 32 | 32 | 1 ICLK | | |
| 0008 6404h | MPU | Region-0 end page number register | REPAGE0 | 32 | 32 | 1 ICLK | | |
| 0008 6408h | MPU | Region-1 start page number register | RSPAGE1 | 32 | 32 | 1 ICLK | | |
| 0008 640Ch | MPU | Region-1 end page number register | REPAGE1 | 32 | 32 | 1 ICLK | | |
| 0008 6410h | MPU | Region-2 start page number register | RSPAGE2 | 32 | 32 | 1 ICLK | | |
| 0008 6414h | MPU | Region-2 end page number register | REPAGE2 | 32 | 32 | 1 ICLK | | |
| 0008 6418h | MPU | Region-3 start page number register | RSPAGE3 | 32 | 32 | 1 ICLK | | |
| 0008 641Ch | MPU | Region-3 end page number register | REPAGE3 | 32 | 32 | 1 ICLK | | |
| 0008 6420h | MPU | Region-4 start page number register | RSPAGE4 | 32 | 32 | 1 ICLK | | |
| 0008 6424h | MPU | Region-4 end page number register | REPAGE4 | 32 | 32 | 1 ICLK | | |
| 0008 6428h | MPU | Region-5 start page number register | RSPAGE5 | 32 | 32 | 1 ICLK | | |
| 0008 642Ch | MPU | Region-5 end page number register | REPAGE5 | 32 | 32 | 1 ICLK | | |
| 0008 6430h | MPU | Region-6 start page number register | RSPAGE6 | 32 | 32 | 1 ICLK | | |
| 0008 6434h | MPU | Region-6 end page number register | REPAGE6 | 32 | 32 | 1 ICLK | | |
| 0008 6438h | MPU | Region-7 start page number register | RSPAGE7 | 32 | 32 | 1 ICLK | | |
| 0008 643Ch | MPU | Region-7 end page number register | REPAGE7 | 32 | 32 | 1 ICLK | | |
| 0008 6500h | MPU | Memory-protection enable register | MPEN | 32 | 32 | 1 ICLK | | |
| 0008 6504h | MPU | Background access control register | MPBAC | 32 | 32 | 1 ICLK | | |
| 0008 6508h | MPU | Memory-protection error status-clearing register | MPECLR | 32 | 32 | 1 ICLK | | |

Table 4.1 List of I/O Registers (Address Order) (5/50)

| Address | Module Symbol | Register Name | Register Symbol | Number of Bits | Access Size | Number of Access States | | Related Function |
|------------|---------------|---|-----------------|----------------|-------------|-------------------------|-----------|------------------|
| | | | | | | ICLK≥PCLK | ICLK<PCLK | |
| 0008 650Ch | MPU | Memory-protection error status register | MPESTS | 32 | 32 | 1 | ICLK | MPU |
| 0008 6514h | MPU | Data memory-protection error address register | MPDEA | 32 | 32 | 1 | ICLK | |
| 0008 6520h | MPU | Region search address register | MPSA | 32 | 32 | 1 | ICLK | |
| 0008 6524h | MPU | Region search operation register | MPOPS | 16 | 16 | 1 | ICLK | |
| 0008 6526h | MPU | Region invalidation operation register | MPOPI | 16 | 16 | 1 | ICLK | |
| 0008 6528h | MPU | Instruction-hit region register | MHITI | 32 | 32 | 1 | ICLK | |
| 0008 652Ch | MPU | Data-hit region register | MHITD | 32 | 32 | 1 | ICLK | |
| 0008 7010h | ICU | Interrupt request register 016 | IR016 | 8 | 8 | 2 | ICLK | ICUb |
| 0008 7015h | ICU | Interrupt request register 021 | IR021 | 8 | 8 | 2 | ICLK | |
| 0008 7017h | ICU | Interrupt request register 023 | IR023 | 8 | 8 | 2 | ICLK | |
| 0008 701Bh | ICU | Interrupt request register 027 | IR027 | 8 | 8 | 2 | ICLK | |
| 0008 701Ch | ICU | Interrupt request register 028 | IR028 | 8 | 8 | 2 | ICLK | |
| 0008 701Dh | ICU | Interrupt request register 029 | IR029 | 8 | 8 | 2 | ICLK | |
| 0008 701Eh | ICU | Interrupt request register 030 | IR030 | 8 | 8 | 2 | ICLK | |
| 0008 701Fh | ICU | Interrupt request register 031 | IR031 | 8 | 8 | 2 | ICLK | |
| 0008 7020h | ICU | Interrupt request register 032 | IR032 | 8 | 8 | 2 | ICLK | |
| 0008 7021h | ICU | Interrupt request register 033 | IR033 | 8 | 8 | 2 | ICLK | |
| 0008 7022h | ICU | Interrupt request register 034 | IR034 | 8 | 8 | 2 | ICLK | |
| 0008 7023h | ICU | Interrupt request register 035 | IR035 | 8 | 8 | 2 | ICLK | |
| 0008 7024h | ICU | Interrupt request register 036 | IR036 | 8 | 8 | 2 | ICLK | |
| 0008 7025h | ICU | Interrupt request register 037 | IR037 | 8 | 8 | 2 | ICLK | |
| 0008 7026h | ICU | Interrupt request register 038 | IR038 | 8 | 8 | 2 | ICLK | |
| 0008 7027h | ICU | Interrupt request register 039 | IR039 | 8 | 8 | 2 | ICLK | |
| 0008 7028h | ICU | Interrupt request register 040 | IR040 | 8 | 8 | 2 | ICLK | |
| 0008 7029h | ICU | Interrupt request register 041 | IR041 | 8 | 8 | 2 | ICLK | |
| 0008 702Ah | ICU | Interrupt request register 042 | IR042 | 8 | 8 | 2 | ICLK | |
| 0008 702Bh | ICU | Interrupt request register 043 | IR043 | 8 | 8 | 2 | ICLK | |
| 0008 702Ch | ICU | Interrupt request register 044 | IR044 | 8 | 8 | 2 | ICLK | |
| 0008 702Dh | ICU | Interrupt request register 045 | IR045 | 8 | 8 | 2 | ICLK | |
| 0008 702Eh | ICU | Interrupt request register 046 | IR046 | 8 | 8 | 2 | ICLK | |
| 0008 702Fh | ICU | Interrupt request register 047 | IR047 | 8 | 8 | 2 | ICLK | |
| 0008 7030h | ICU | Interrupt request register 048 | IR048 | 8 | 8 | 2 | ICLK | |
| 0008 7031h | ICU | Interrupt request register 049 | IR049 | 8 | 8 | 2 | ICLK | |
| 0008 7032h | ICU | Interrupt request register 050 | IR050 | 8 | 8 | 2 | ICLK | |
| 0008 7033h | ICU | Interrupt request register 051 | IR051 | 8 | 8 | 2 | ICLK | |
| 0008 7034h | ICU | Interrupt request register 052 | IR052 | 8 | 8 | 2 | ICLK | |
| 0008 7035h | ICU | Interrupt request register 053 | IR053 | 8 | 8 | 2 | ICLK | |
| 0008 7036h | ICU | Interrupt request register 054 | IR054 | 8 | 8 | 2 | ICLK | |
| 0008 7037h | ICU | Interrupt request register 055 | IR055 | 8 | 8 | 2 | ICLK | |
| 0008 7038h | ICU | Interrupt request register 056 | IR056 | 8 | 8 | 2 | ICLK | |
| 0008 7039h | ICU | Interrupt request register 057 | IR057 | 8 | 8 | 2 | ICLK | |
| 0008 703Ah | ICU | Interrupt request register 058 | IR058 | 8 | 8 | 2 | ICLK | |
| 0008 703Bh | ICU | Interrupt request register 059 | IR059 | 8 | 8 | 2 | ICLK | |
| 0008 703Eh | ICU | Interrupt request register 062 | IR062 | 8 | 8 | 2 | ICLK | |
| 0008 7040h | ICU | Interrupt request register 064 | IR064 | 8 | 8 | 2 | ICLK | |
| 0008 7041h | ICU | Interrupt request register 065 | IR065 | 8 | 8 | 2 | ICLK | |
| 0008 7042h | ICU | Interrupt request register 066 | IR066 | 8 | 8 | 2 | ICLK | |
| 0008 7043h | ICU | Interrupt request register 067 | IR067 | 8 | 8 | 2 | ICLK | |
| 0008 7044h | ICU | Interrupt request register 068 | IR068 | 8 | 8 | 2 | ICLK | |
| 0008 7045h | ICU | Interrupt request register 069 | IR069 | 8 | 8 | 2 | ICLK | |
| 0008 7046h | ICU | Interrupt request register 070 | IR070 | 8 | 8 | 2 | ICLK | |

Table 4.1 List of I/O Registers (Address Order) (6/50)

| Address | Module Symbol | Register Name | Register Symbol | Number of Bits | Access Size | Number of Access States | | Related Function |
|------------|---------------|--------------------------------|-----------------|----------------|-------------|-------------------------|-----------|------------------|
| | | | | | | ICLK \geq PCLK | ICLK<PCLK | |
| 0008 7047h | ICU | Interrupt request register 071 | IR071 | 8 | 8 | 2 | ICLK | ICUb |
| 0008 7048h | ICU | Interrupt request register 072 | IR072 | 8 | 8 | 2 | ICLK | |
| 0008 7049h | ICU | Interrupt request register 073 | IR073 | 8 | 8 | 2 | ICLK | |
| 0008 704Ah | ICU | Interrupt request register 074 | IR074 | 8 | 8 | 2 | ICLK | |
| 0008 704Bh | ICU | Interrupt request register 075 | IR075 | 8 | 8 | 2 | ICLK | |
| 0008 704Ch | ICU | Interrupt request register 076 | IR076 | 8 | 8 | 2 | ICLK | |
| 0008 704Dh | ICU | Interrupt request register 077 | IR077 | 8 | 8 | 2 | ICLK | |
| 0008 704Eh | ICU | Interrupt request register 078 | IR078 | 8 | 8 | 2 | ICLK | |
| 0008 704Fh | ICU | Interrupt request register 079 | IR079 | 8 | 8 | 2 | ICLK | |
| 0008 705Ah | ICU | Interrupt request register 090 | IR090 | 8 | 8 | 2 | ICLK | |
| 0008 705Bh | ICU | Interrupt request register 091 | IR091 | 8 | 8 | 2 | ICLK | |
| 0008 705Ch | ICU | Interrupt request register 092 | IR092 | 8 | 8 | 2 | ICLK | |
| 0008 705Dh | ICU | Interrupt request register 093 | IR093 | 8 | 8 | 2 | ICLK | |
| 0008 7062h | ICU | Interrupt request register 098 | IR098 | 8 | 8 | 2 | ICLK | |
| 0008 7066h | ICU | Interrupt request register 102 | IR102 | 8 | 8 | 2 | ICLK | |
| 0008 706Ah | ICU | Interrupt request register 106 | IR106 | 8 | 8 | 2 | ICLK | |
| 0008 706Bh | ICU | Interrupt request register 107 | IR107 | 8 | 8 | 2 | ICLK | |
| 0008 706Ch | ICU | Interrupt request register 108 | IR108 | 8 | 8 | 2 | ICLK | |
| 0008 706Dh | ICU | Interrupt request register 109 | IR109 | 8 | 8 | 2 | ICLK | |
| 0008 706Eh | ICU | Interrupt request register 110 | IR110 | 8 | 8 | 2 | ICLK | |
| 0008 706Fh | ICU | Interrupt request register 111 | IR111 | 8 | 8 | 2 | ICLK | |
| 0008 7070h | ICU | Interrupt request register 112 | IR112 | 8 | 8 | 2 | ICLK | |
| 0008 7072h | ICU | Interrupt request register 114 | IR114 | 8 | 8 | 2 | ICLK | |
| 0008 707Ah | ICU | Interrupt request register 122 | IR122 | 8 | 8 | 2 | ICLK | |
| 0008 707Bh | ICU | Interrupt request register 123 | IR123 | 8 | 8 | 2 | ICLK | |
| 0008 707Ch | ICU | Interrupt request register 124 | IR124 | 8 | 8 | 2 | ICLK | |
| 0008 707Dh | ICU | Interrupt request register 125 | IR125 | 8 | 8 | 2 | ICLK | |
| 0008 707Eh | ICU | Interrupt request register 126 | IR126 | 8 | 8 | 2 | ICLK | |
| 0008 707Fh | ICU | Interrupt request register 127 | IR127 | 8 | 8 | 2 | ICLK | |
| 0008 7080h | ICU | Interrupt request register 128 | IR128 | 8 | 8 | 2 | ICLK | |
| 0008 7081h | ICU | Interrupt request register 129 | IR129 | 8 | 8 | 2 | ICLK | |
| 0008 7082h | ICU | Interrupt request register 130 | IR130 | 8 | 8 | 2 | ICLK | |
| 0008 7083h | ICU | Interrupt request register 131 | IR131 | 8 | 8 | 2 | ICLK | |
| 0008 7084h | ICU | Interrupt request register 132 | IR132 | 8 | 8 | 2 | ICLK | |
| 0008 7085h | ICU | Interrupt request register 133 | IR133 | 8 | 8 | 2 | ICLK | |
| 0008 7086h | ICU | Interrupt request register 134 | IR134 | 8 | 8 | 2 | ICLK | |
| 0008 7087h | ICU | Interrupt request register 135 | IR135 | 8 | 8 | 2 | ICLK | |
| 0008 7088h | ICU | Interrupt request register 136 | IR136 | 8 | 8 | 2 | ICLK | |
| 0008 7089h | ICU | Interrupt request register 137 | IR137 | 8 | 8 | 2 | ICLK | |
| 0008 708Ah | ICU | Interrupt request register 138 | IR138 | 8 | 8 | 2 | ICLK | |
| 0008 708Bh | ICU | Interrupt request register 139 | IR139 | 8 | 8 | 2 | ICLK | |
| 0008 708Ch | ICU | Interrupt request register 140 | IR140 | 8 | 8 | 2 | ICLK | |
| 0008 708Dh | ICU | Interrupt request register 141 | IR141 | 8 | 8 | 2 | ICLK | |
| 0008 708Eh | ICU | Interrupt request register 142 | IR142 | 8 | 8 | 2 | ICLK | |
| 0008 708Fh | ICU | Interrupt request register 143 | IR143 | 8 | 8 | 2 | ICLK | |
| 0008 7090h | ICU | Interrupt request register 144 | IR144 | 8 | 8 | 2 | ICLK | |
| 0008 7091h | ICU | Interrupt request register 145 | IR145 | 8 | 8 | 2 | ICLK | |
| 0008 7092h | ICU | Interrupt request register 146 | IR146 | 8 | 8 | 2 | ICLK | |
| 0008 7093h | ICU | Interrupt request register 147 | IR147 | 8 | 8 | 2 | ICLK | |
| 0008 7094h | ICU | Interrupt request register 148 | IR148 | 8 | 8 | 2 | ICLK | |
| 0008 7095h | ICU | Interrupt request register 149 | IR149 | 8 | 8 | 2 | ICLK | |

Table 4.1 List of I/O Registers (Address Order) (7/50)

| Address | Module Symbol | Register Name | Register Symbol | Number of Bits | Access Size | Number of Access States | | Related Function |
|------------|---------------|--------------------------------|-----------------|----------------|-------------|-------------------------|-----------|------------------|
| | | | | | | ICLK≥PCLK | ICLK<PCLK | |
| 0008 7096h | ICU | Interrupt request register 150 | IR150 | 8 | 8 | 2 | ICLK | ICUb |
| 0008 7097h | ICU | Interrupt request register 151 | IR151 | 8 | 8 | 2 | ICLK | |
| 0008 7098h | ICU | Interrupt request register 152 | IR152 | 8 | 8 | 2 | ICLK | |
| 0008 7099h | ICU | Interrupt request register 153 | IR153 | 8 | 8 | 2 | ICLK | |
| 0008 709Ah | ICU | Interrupt request register 154 | IR154 | 8 | 8 | 2 | ICLK | |
| 0008 709Bh | ICU | Interrupt request register 155 | IR155 | 8 | 8 | 2 | ICLK | |
| 0008 709Ch | ICU | Interrupt request register 156 | IR156 | 8 | 8 | 2 | ICLK | |
| 0008 709Dh | ICU | Interrupt request register 157 | IR157 | 8 | 8 | 2 | ICLK | |
| 0008 709Eh | ICU | Interrupt request register 158 | IR158 | 8 | 8 | 2 | ICLK | |
| 0008 709Fh | ICU | Interrupt request register 159 | IR159 | 8 | 8 | 2 | ICLK | |
| 0008 70A0h | ICU | Interrupt request register 160 | IR160 | 8 | 8 | 2 | ICLK | |
| 0008 70A1h | ICU | Interrupt request register 161 | IR161 | 8 | 8 | 2 | ICLK | |
| 0008 70A2h | ICU | Interrupt request register 162 | IR162 | 8 | 8 | 2 | ICLK | |
| 0008 70A3h | ICU | Interrupt request register 163 | IR163 | 8 | 8 | 2 | ICLK | |
| 0008 70A4h | ICU | Interrupt request register 164 | IR164 | 8 | 8 | 2 | ICLK | |
| 0008 70A5h | ICU | Interrupt request register 165 | IR165 | 8 | 8 | 2 | ICLK | |
| 0008 70A6h | ICU | Interrupt request register 166 | IR166 | 8 | 8 | 2 | ICLK | |
| 0008 70A7h | ICU | Interrupt request register 167 | IR167 | 8 | 8 | 2 | ICLK | |
| 0008 70AAh | ICU | Interrupt request register 170 | IR170 | 8 | 8 | 2 | ICLK | |
| 0008 70ABh | ICU | Interrupt request register 171 | IR171 | 8 | 8 | 2 | ICLK | |
| 0008 70ACh | ICU | Interrupt request register 172 | IR172 | 8 | 8 | 2 | ICLK | |
| 0008 70ADh | ICU | Interrupt request register 173 | IR173 | 8 | 8 | 2 | ICLK | |
| 0008 70AEh | ICU | Interrupt request register 174 | IR174 | 8 | 8 | 2 | ICLK | |
| 0008 70AFh | ICU | Interrupt request register 175 | IR175 | 8 | 8 | 2 | ICLK | |
| 0008 70B0h | ICU | Interrupt request register 176 | IR176 | 8 | 8 | 2 | ICLK | |
| 0008 70B1h | ICU | Interrupt request register 177 | IR177 | 8 | 8 | 2 | ICLK | |
| 0008 70B2h | ICU | Interrupt request register 178 | IR178 | 8 | 8 | 2 | ICLK | |
| 0008 70B3h | ICU | Interrupt request register 179 | IR179 | 8 | 8 | 2 | ICLK | |
| 0008 70B4h | ICU | Interrupt request register 180 | IR180 | 8 | 8 | 2 | ICLK | |
| 0008 70B5h | ICU | Interrupt request register 181 | IR181 | 8 | 8 | 2 | ICLK | |
| 0008 70B6h | ICU | Interrupt request register 182 | IR182 | 8 | 8 | 2 | ICLK | |
| 0008 70B7h | ICU | Interrupt request register 183 | IR183 | 8 | 8 | 2 | ICLK | |
| 0008 70B8h | ICU | Interrupt request register 184 | IR184 | 8 | 8 | 2 | ICLK | |
| 0008 70B9h | ICU | Interrupt request register 185 | IR185 | 8 | 8 | 2 | ICLK | |
| 0008 70BAh | ICU | Interrupt request register 186 | IR186 | 8 | 8 | 2 | ICLK | |
| 0008 70BBh | ICU | Interrupt request register 187 | IR187 | 8 | 8 | 2 | ICLK | |
| 0008 70BCh | ICU | Interrupt request register 188 | IR188 | 8 | 8 | 2 | ICLK | |
| 0008 70BDh | ICU | Interrupt request register 189 | IR189 | 8 | 8 | 2 | ICLK | |
| 0008 70BEh | ICU | Interrupt request register 190 | IR190 | 8 | 8 | 2 | ICLK | |
| 0008 70BFh | ICU | Interrupt request register 191 | IR191 | 8 | 8 | 2 | ICLK | |
| 0008 70C0h | ICU | Interrupt request register 192 | IR192 | 8 | 8 | 2 | ICLK | |
| 0008 70C1h | ICU | Interrupt request register 193 | IR193 | 8 | 8 | 2 | ICLK | |
| 0008 70C2h | ICU | Interrupt request register 194 | IR194 | 8 | 8 | 2 | ICLK | |
| 0008 70C3h | ICU | Interrupt request register 195 | IR195 | 8 | 8 | 2 | ICLK | |
| 0008 70C4h | ICU | Interrupt request register 196 | IR196 | 8 | 8 | 2 | ICLK | |
| 0008 70C5h | ICU | Interrupt request register 197 | IR197 | 8 | 8 | 2 | ICLK | |
| 0008 70C6h | ICU | Interrupt request register 198 | IR198 | 8 | 8 | 2 | ICLK | |
| 0008 70C7h | ICU | Interrupt request register 199 | IR199 | 8 | 8 | 2 | ICLK | |
| 0008 70C8h | ICU | Interrupt request register 200 | IR200 | 8 | 8 | 2 | ICLK | |
| 0008 70C9h | ICU | Interrupt request register 201 | IR201 | 8 | 8 | 2 | ICLK | |
| 0008 70CAh | ICU | Interrupt request register 202 | IR202 | 8 | 8 | 2 | ICLK | |

Table 4.1 List of I/O Registers (Address Order) (8/50)

| Address | Module Symbol | Register Name | Register Symbol | Number of Bits | Access Size | Number of Access States | | Related Function |
|------------|---------------|------------------------------------|-----------------|----------------|-------------|-------------------------|-----------|------------------|
| | | | | | | ICLK≥PCLK | ICLK<PCLK | |
| 0008 70CBh | ICU | Interrupt request register 203 | IR203 | 8 | 8 | 2 | ICLK | ICUb |
| 0008 70D6h | ICU | Interrupt request register 214 | IR214 | 8 | 8 | 2 | ICLK | |
| 0008 70D7h | ICU | Interrupt request register 215 | IR215 | 8 | 8 | 2 | ICLK | |
| 0008 70D8h | ICU | Interrupt request register 216 | IR216 | 8 | 8 | 2 | ICLK | |
| 0008 70D9h | ICU | Interrupt request register 217 | IR217 | 8 | 8 | 2 | ICLK | |
| 0008 70DAh | ICU | Interrupt request register 218 | IR218 | 8 | 8 | 2 | ICLK | |
| 0008 70DBh | ICU | Interrupt request register 219 | IR219 | 8 | 8 | 2 | ICLK | |
| 0008 70DCh | ICU | Interrupt request register 220 | IR220 | 8 | 8 | 2 | ICLK | |
| 0008 70DDh | ICU | Interrupt request register 221 | IR221 | 8 | 8 | 2 | ICLK | |
| 0008 70DEh | ICU | Interrupt request register 222 | IR222 | 8 | 8 | 2 | ICLK | |
| 0008 70DFh | ICU | Interrupt request register 223 | IR223 | 8 | 8 | 2 | ICLK | |
| 0008 70E0h | ICU | Interrupt request register 224 | IR224 | 8 | 8 | 2 | ICLK | |
| 0008 70E1h | ICU | Interrupt request register 225 | IR225 | 8 | 8 | 2 | ICLK | |
| 0008 70E2h | ICU | Interrupt request register 226 | IR226 | 8 | 8 | 2 | ICLK | |
| 0008 70E3h | ICU | Interrupt request register 227 | IR227 | 8 | 8 | 2 | ICLK | |
| 0008 70E4h | ICU | Interrupt request register 228 | IR228 | 8 | 8 | 2 | ICLK | |
| 0008 70E5h | ICU | Interrupt request register 229 | IR229 | 8 | 8 | 2 | ICLK | |
| 0008 70E6h | ICU | Interrupt request register 230 | IR230 | 8 | 8 | 2 | ICLK | |
| 0008 70E7h | ICU | Interrupt request register 231 | IR231 | 8 | 8 | 2 | ICLK | |
| 0008 70E8h | ICU | Interrupt request register 232 | IR232 | 8 | 8 | 2 | ICLK | |
| 0008 70E9h | ICU | Interrupt request register 233 | IR233 | 8 | 8 | 2 | ICLK | |
| 0008 70EAh | ICU | Interrupt request register 234 | IR234 | 8 | 8 | 2 | ICLK | |
| 0008 70EBh | ICU | Interrupt request register 235 | IR235 | 8 | 8 | 2 | ICLK | |
| 0008 70ECh | ICU | Interrupt request register 236 | IR236 | 8 | 8 | 2 | ICLK | |
| 0008 70EDh | ICU | Interrupt request register 237 | IR237 | 8 | 8 | 2 | ICLK | |
| 0008 70EEh | ICU | Interrupt request register 238 | IR238 | 8 | 8 | 2 | ICLK | |
| 0008 70EFh | ICU | Interrupt request register 239 | IR239 | 8 | 8 | 2 | ICLK | |
| 0008 70F0h | ICU | Interrupt request register 240 | IR240 | 8 | 8 | 2 | ICLK | |
| 0008 70F1h | ICU | Interrupt request register 241 | IR241 | 8 | 8 | 2 | ICLK | |
| 0008 70F2h | ICU | Interrupt request register 242 | IR242 | 8 | 8 | 2 | ICLK | |
| 0008 70F3h | ICU | Interrupt request register 243 | IR243 | 8 | 8 | 2 | ICLK | |
| 0008 70F4h | ICU | Interrupt request register 244 | IR244 | 8 | 8 | 2 | ICLK | |
| 0008 70F5h | ICU | Interrupt request register 245 | IR245 | 8 | 8 | 2 | ICLK | |
| 0008 70F6h | ICU | Interrupt request register 246 | IR246 | 8 | 8 | 2 | ICLK | |
| 0008 70F7h | ICU | Interrupt request register 247 | IR247 | 8 | 8 | 2 | ICLK | |
| 0008 70F8h | ICU | Interrupt request register 248 | IR248 | 8 | 8 | 2 | ICLK | |
| 0008 70F9h | ICU | Interrupt request register 249 | IR249 | 8 | 8 | 2 | ICLK | |
| 0008 70FAh | ICU | Interrupt request register 250 | IR250 | 8 | 8 | 2 | ICLK | |
| 0008 70FBh | ICU | Interrupt request register 251 | IR251 | 8 | 8 | 2 | ICLK | |
| 0008 70FCh | ICU | Interrupt request register 252 | IR252 | 8 | 8 | 2 | ICLK | |
| 0008 70FDh | ICU | Interrupt request register 253 | IR253 | 8 | 8 | 2 | ICLK | |
| 0008 711Bh | ICU | DTC activation enable register 027 | DTCER027 | 8 | 8 | 2 | ICLK | |
| 0008 711Ch | ICU | DTC activation enable register 028 | DTCER028 | 8 | 8 | 2 | ICLK | |
| 0008 711Dh | ICU | DTC activation enable register 029 | DTCER029 | 8 | 8 | 2 | ICLK | |
| 0008 711Eh | ICU | DTC activation enable register 030 | DTCER030 | 8 | 8 | 2 | ICLK | |
| 0008 711Fh | ICU | DTC activation enable register 031 | DTCER031 | 8 | 8 | 2 | ICLK | |
| 0008 7121h | ICU | DTC activation enable register 033 | DTCER033 | 8 | 8 | 2 | ICLK | |
| 0008 7122h | ICU | DTC activation enable register 034 | DTCER034 | 8 | 8 | 2 | ICLK | |
| 0008 7124h | ICU | DTC activation enable register 036 | DTCER036 | 8 | 8 | 2 | ICLK | |
| 0008 7125h | ICU | DTC activation enable register 037 | DTCER037 | 8 | 8 | 2 | ICLK | |
| 0008 7127h | ICU | DTC activation enable register 039 | DTCER039 | 8 | 8 | 2 | ICLK | |

Table 4.1 List of I/O Registers (Address Order) (9/50)

| Address | Module Symbol | Register Name | Register Symbol | Number of Bits | Access Size | Number of Access States | | Related Function |
|------------|---------------|------------------------------------|-----------------|----------------|-------------|-------------------------|-----------|------------------|
| | | | | | | ICLK≥PCLK | ICLK<PCLK | |
| 0008 7128h | ICU | DTC activation enable register 040 | DTCER040 | 8 | 8 | 2 | ICLK | ICUb |
| 0008 712Ah | ICU | DTC activation enable register 042 | DTCER042 | 8 | 8 | 2 | ICLK | |
| 0008 712Bh | ICU | DTC activation enable register 043 | DTCER043 | 8 | 8 | 2 | ICLK | |
| 0008 712Dh | ICU | DTC activation enable register 045 | DTCER045 | 8 | 8 | 2 | ICLK | |
| 0008 712Eh | ICU | DTC activation enable register 046 | DTCER046 | 8 | 8 | 2 | ICLK | |
| 0008 7140h | ICU | DTC activation enable register 064 | DTCER064 | 8 | 8 | 2 | ICLK | |
| 0008 7141h | ICU | DTC activation enable register 065 | DTCER065 | 8 | 8 | 2 | ICLK | |
| 0008 7142h | ICU | DTC activation enable register 066 | DTCER066 | 8 | 8 | 2 | ICLK | |
| 0008 7143h | ICU | DTC activation enable register 067 | DTCER067 | 8 | 8 | 2 | ICLK | |
| 0008 7144h | ICU | DTC activation enable register 068 | DTCER068 | 8 | 8 | 2 | ICLK | |
| 0008 7145h | ICU | DTC activation enable register 069 | DTCER069 | 8 | 8 | 2 | ICLK | |
| 0008 7146h | ICU | DTC activation enable register 070 | DTCER070 | 8 | 8 | 2 | ICLK | |
| 0008 7147h | ICU | DTC activation enable register 071 | DTCER071 | 8 | 8 | 2 | ICLK | |
| 0008 7148h | ICU | DTC activation enable register 072 | DTCER072 | 8 | 8 | 2 | ICLK | |
| 0008 7149h | ICU | DTC activation enable register 073 | DTCER073 | 8 | 8 | 2 | ICLK | |
| 0008 714Ah | ICU | DTC activation enable register 074 | DTCER074 | 8 | 8 | 2 | ICLK | |
| 0008 714Bh | ICU | DTC activation enable register 075 | DTCER075 | 8 | 8 | 2 | ICLK | |
| 0008 714Ch | ICU | DTC activation enable register 076 | DTCER076 | 8 | 8 | 2 | ICLK | |
| 0008 714Dh | ICU | DTC activation enable register 077 | DTCER077 | 8 | 8 | 2 | ICLK | |
| 0008 714Eh | ICU | DTC activation enable register 078 | DTCER078 | 8 | 8 | 2 | ICLK | |
| 0008 714Fh | ICU | DTC activation enable register 079 | DTCER079 | 8 | 8 | 2 | ICLK | |
| 0008 7162h | ICU | DTC activation enable register 098 | DTCER098 | 8 | 8 | 2 | ICLK | |
| 0008 7166h | ICU | DTC activation enable register 102 | DTCER102 | 8 | 8 | 2 | ICLK | |
| 0008 717Eh | ICU | DTC activation enable register 126 | DTCER126 | 8 | 8 | 2 | ICLK | |
| 0008 717Fh | ICU | DTC activation enable register 127 | DTCER127 | 8 | 8 | 2 | ICLK | |
| 0008 7180h | ICU | DTC activation enable register 128 | DTCER128 | 8 | 8 | 2 | ICLK | |
| 0008 7181h | ICU | DTC activation enable register 129 | DTCER129 | 8 | 8 | 2 | ICLK | |
| 0008 7182h | ICU | DTC activation enable register 130 | DTCER130 | 8 | 8 | 2 | ICLK | |
| 0008 7183h | ICU | DTC activation enable register 131 | DTCER131 | 8 | 8 | 2 | ICLK | |
| 0008 7184h | ICU | DTC activation enable register 132 | DTCER132 | 8 | 8 | 2 | ICLK | |
| 0008 7185h | ICU | DTC activation enable register 133 | DTCER133 | 8 | 8 | 2 | ICLK | |
| 0008 7186h | ICU | DTC activation enable register 134 | DTCER134 | 8 | 8 | 2 | ICLK | |
| 0008 7187h | ICU | DTC activation enable register 135 | DTCER135 | 8 | 8 | 2 | ICLK | |
| 0008 7188h | ICU | DTC activation enable register 136 | DTCER136 | 8 | 8 | 2 | ICLK | |
| 0008 7189h | ICU | DTC activation enable register 137 | DTCER137 | 8 | 8 | 2 | ICLK | |
| 0008 718Ah | ICU | DTC activation enable register 138 | DTCER138 | 8 | 8 | 2 | ICLK | |
| 0008 718Bh | ICU | DTC activation enable register 139 | DTCER139 | 8 | 8 | 2 | ICLK | |
| 0008 718Ch | ICU | DTC activation enable register 140 | DTCER140 | 8 | 8 | 2 | ICLK | |
| 0008 718Dh | ICU | DTC activation enable register 141 | DTCER141 | 8 | 8 | 2 | ICLK | |
| 0008 718Eh | ICU | DTC activation enable register 142 | DTCER142 | 8 | 8 | 2 | ICLK | |
| 0008 718Fh | ICU | DTC activation enable register 143 | DTCER143 | 8 | 8 | 2 | ICLK | |
| 0008 7190h | ICU | DTC activation enable register 144 | DTCER144 | 8 | 8 | 2 | ICLK | |
| 0008 7191h | ICU | DTC activation enable register 145 | DTCER145 | 8 | 8 | 2 | ICLK | |
| 0008 7194h | ICU | DTC activation enable register 148 | DTCER148 | 8 | 8 | 2 | ICLK | |
| 0008 7195h | ICU | DTC activation enable register 149 | DTCER149 | 8 | 8 | 2 | ICLK | |
| 0008 7196h | ICU | DTC activation enable register 150 | DTCER150 | 8 | 8 | 2 | ICLK | |
| 0008 7197h | ICU | DTC activation enable register 151 | DTCER151 | 8 | 8 | 2 | ICLK | |
| 0008 7198h | ICU | DTC activation enable register 152 | DTCER152 | 8 | 8 | 2 | ICLK | |
| 0008 7199h | ICU | DTC activation enable register 153 | DTCER153 | 8 | 8 | 2 | ICLK | |
| 0008 719Ah | ICU | DTC activation enable register 154 | DTCER154 | 8 | 8 | 2 | ICLK | |
| 0008 719Bh | ICU | DTC activation enable register 155 | DTCER155 | 8 | 8 | 2 | ICLK | |

Table 4.1 List of I/O Registers (Address Order) (10/50)

| Address | Module Symbol | Register Name | Register Symbol | Number of Bits | Access Size | Number of Access States | | Related Function |
|------------|---------------|------------------------------------|-----------------|----------------|-------------|-------------------------|-----------|------------------|
| | | | | | | ICLK≥PCLK | ICLK<PCLK | |
| 0008 719Ch | ICU | DTC activation enable register 156 | DTCER156 | 8 | 8 | 2 | ICLK | ICUb |
| 0008 719Dh | ICU | DTC activation enable register 157 | DTCER157 | 8 | 8 | 2 | ICLK | |
| 0008 719Eh | ICU | DTC activation enable register 158 | DTCER158 | 8 | 8 | 2 | ICLK | |
| 0008 719Fh | ICU | DTC activation enable register 159 | DTCER159 | 8 | 8 | 2 | ICLK | |
| 0008 71A0h | ICU | DTC activation enable register 160 | DTCER160 | 8 | 8 | 2 | ICLK | |
| 0008 71A1h | ICU | DTC activation enable register 161 | DTCER161 | 8 | 8 | 2 | ICLK | |
| 0008 71A2h | ICU | DTC activation enable register 162 | DTCER162 | 8 | 8 | 2 | ICLK | |
| 0008 71A3h | ICU | DTC activation enable register 163 | DTCER163 | 8 | 8 | 2 | ICLK | |
| 0008 71A4h | ICU | DTC activation enable register 164 | DTCER164 | 8 | 8 | 2 | ICLK | |
| 0008 71A5h | ICU | DTC activation enable register 165 | DTCER165 | 8 | 8 | 2 | ICLK | |
| 0008 71AAh | ICU | DTC activation enable register 170 | DTCER170 | 8 | 8 | 2 | ICLK | |
| 0008 71ABh | ICU | DTC activation enable register 171 | DTCER171 | 8 | 8 | 2 | ICLK | |
| 0008 71ADh | ICU | DTC activation enable register 173 | DTCER173 | 8 | 8 | 2 | ICLK | |
| 0008 71AEh | ICU | DTC activation enable register 174 | DTCER174 | 8 | 8 | 2 | ICLK | |
| 0008 71B0h | ICU | DTC activation enable register 176 | DTCER176 | 8 | 8 | 2 | ICLK | |
| 0008 71B1h | ICU | DTC activation enable register 177 | DTCER177 | 8 | 8 | 2 | ICLK | |
| 0008 71B3h | ICU | DTC activation enable register 179 | DTCER179 | 8 | 8 | 2 | ICLK | |
| 0008 71B4h | ICU | DTC activation enable register 180 | DTCER180 | 8 | 8 | 2 | ICLK | |
| 0008 71B7h | ICU | DTC activation enable register 183 | DTCER183 | 8 | 8 | 2 | ICLK | |
| 0008 71B8h | ICU | DTC activation enable register 184 | DTCER184 | 8 | 8 | 2 | ICLK | |
| 0008 71BBh | ICU | DTC activation enable register 187 | DTCER187 | 8 | 8 | 2 | ICLK | |
| 0008 71BCh | ICU | DTC activation enable register 188 | DTCER188 | 8 | 8 | 2 | ICLK | |
| 0008 71BFh | ICU | DTC activation enable register 191 | DTCER191 | 8 | 8 | 2 | ICLK | |
| 0008 71C0h | ICU | DTC activation enable register 192 | DTCER192 | 8 | 8 | 2 | ICLK | |
| 0008 71C3h | ICU | DTC activation enable register 195 | DTCER195 | 8 | 8 | 2 | ICLK | |
| 0008 71C4h | ICU | DTC activation enable register 196 | DTCER196 | 8 | 8 | 2 | ICLK | |
| 0008 71C6h | ICU | DTC activation enable register 198 | DTCER198 | 8 | 8 | 2 | ICLK | |
| 0008 71C7h | ICU | DTC activation enable register 199 | DTCER199 | 8 | 8 | 2 | ICLK | |
| 0008 71C8h | ICU | DTC activation enable register 200 | DTCER200 | 8 | 8 | 2 | ICLK | |
| 0008 71C9h | ICU | DTC activation enable register 201 | DTCER201 | 8 | 8 | 2 | ICLK | |
| 0008 71CAh | ICU | DTC activation enable register 202 | DTCER202 | 8 | 8 | 2 | ICLK | |
| 0008 71CBh | ICU | DTC activation enable register 203 | DTCER203 | 8 | 8 | 2 | ICLK | |
| 0008 71CEh | ICU | DTC activation enable register 206 | DTCER206 | 8 | 8 | 2 | ICLK | |
| 0008 71CFh | ICU | DTC activation enable register 207 | DTCER207 | 8 | 8 | 2 | ICLK | |
| 0008 71D0h | ICU | DTC activation enable register 208 | DTCER208 | 8 | 8 | 2 | ICLK | |
| 0008 71D6h | ICU | DTC activation enable register 214 | DTCER214 | 8 | 8 | 2 | ICLK | |
| 0008 71D7h | ICU | DTC activation enable register 215 | DTCER215 | 8 | 8 | 2 | ICLK | |
| 0008 71D9h | ICU | DTC activation enable register 217 | DTCER217 | 8 | 8 | 2 | ICLK | |
| 0008 71DAh | ICU | DTC activation enable register 218 | DTCER218 | 8 | 8 | 2 | ICLK | |
| 0008 71DCh | ICU | DTC activation enable register 220 | DTCER220 | 8 | 8 | 2 | ICLK | |
| 0008 71DDh | ICU | DTC activation enable register 221 | DTCER221 | 8 | 8 | 2 | ICLK | |
| 0008 71DFh | ICU | DTC activation enable register 223 | DTCER223 | 8 | 8 | 2 | ICLK | |
| 0008 71E0h | ICU | DTC activation enable register 224 | DTCER224 | 8 | 8 | 2 | ICLK | |
| 0008 71E2h | ICU | DTC activation enable register 226 | DTCER226 | 8 | 8 | 2 | ICLK | |
| 0008 71E3h | ICU | DTC activation enable register 227 | DTCER227 | 8 | 8 | 2 | ICLK | |
| 0008 71E5h | ICU | DTC activation enable register 229 | DTCER229 | 8 | 8 | 2 | ICLK | |
| 0008 71E6h | ICU | DTC activation enable register 230 | DTCER230 | 8 | 8 | 2 | ICLK | |
| 0008 71E8h | ICU | DTC activation enable register 232 | DTCER232 | 8 | 8 | 2 | ICLK | |
| 0008 71E9h | ICU | DTC activation enable register 233 | DTCER233 | 8 | 8 | 2 | ICLK | |
| 0008 71EBh | ICU | DTC activation enable register 235 | DTCER235 | 8 | 8 | 2 | ICLK | |
| 0008 71ECh | ICU | DTC activation enable register 236 | DTCER236 | 8 | 8 | 2 | ICLK | |

Table 4.1 List of I/O Registers (Address Order) (11/50)

| Address | Module Symbol | Register Name | Register Symbol | Number of Bits | Access Size | Number of Access States | | Related Function |
|------------|---------------|--|-----------------|----------------|-------------|-------------------------|-----------|------------------|
| | | | | | | ICLK≥PCLK | ICLK<PCLK | |
| 0008 71EEh | ICU | DTC activation enable register 238 | DTCER238 | 8 | 8 | 2 | ICLK | ICUb |
| 0008 71EFh | ICU | DTC activation enable register 239 | DTCER239 | 8 | 8 | 2 | ICLK | |
| 0008 71F1h | ICU | DTC activation enable register 241 | DTCER241 | 8 | 8 | 2 | ICLK | |
| 0008 71F2h | ICU | DTC activation enable register 242 | DTCER242 | 8 | 8 | 2 | ICLK | |
| 0008 71F4h | ICU | DTC activation enable register 244 | DTCER244 | 8 | 8 | 2 | ICLK | |
| 0008 71F5h | ICU | DTC activation enable register 245 | DTCER245 | 8 | 8 | 2 | ICLK | |
| 0008 71F7h | ICU | DTC activation enable register 247 | DTCER247 | 8 | 8 | 2 | ICLK | |
| 0008 71F8h | ICU | DTC activation enable register 248 | DTCER248 | 8 | 8 | 2 | ICLK | |
| 0008 71FAh | ICU | DTC activation enable register 250 | DTCER250 | 8 | 8 | 2 | ICLK | |
| 0008 71FBh | ICU | DTC activation enable register 251 | DTCER251 | 8 | 8 | 2 | ICLK | |
| 0008 7202h | ICU | Interrupt request enable register 02 | IER02 | 8 | 8 | 2 | ICLK | |
| 0008 7203h | ICU | Interrupt request enable register 03 | IER03 | 8 | 8 | 2 | ICLK | |
| 0008 7204h | ICU | Interrupt request enable register 04 | IER04 | 8 | 8 | 2 | ICLK | |
| 0008 7205h | ICU | Interrupt request enable register 05 | IER05 | 8 | 8 | 2 | ICLK | |
| 0008 7206h | ICU | Interrupt request enable register 06 | IER06 | 8 | 8 | 2 | ICLK | |
| 0008 7207h | ICU | Interrupt request enable register 07 | IER07 | 8 | 8 | 2 | ICLK | |
| 0008 7208h | ICU | Interrupt request enable register 08 | IER08 | 8 | 8 | 2 | ICLK | |
| 0008 7209h | ICU | Interrupt request enable register 09 | IER09 | 8 | 8 | 2 | ICLK | |
| 0008 720Bh | ICU | Interrupt request enable register 0B | IER0B | 8 | 8 | 2 | ICLK | |
| 0008 720Ch | ICU | Interrupt request enable register 0C | IER0C | 8 | 8 | 2 | ICLK | |
| 0008 720Dh | ICU | Interrupt request enable register 0D | IER0D | 8 | 8 | 2 | ICLK | |
| 0008 720Eh | ICU | Interrupt request enable register 0E | IER0E | 8 | 8 | 2 | ICLK | |
| 0008 720Fh | ICU | Interrupt request enable register 0F | IER0F | 8 | 8 | 2 | ICLK | |
| 0008 7210h | ICU | Interrupt request enable register 10 | IER10 | 8 | 8 | 2 | ICLK | |
| 0008 7211h | ICU | Interrupt request enable register 11 | IER11 | 8 | 8 | 2 | ICLK | |
| 0008 7212h | ICU | Interrupt request enable register 12 | IER12 | 8 | 8 | 2 | ICLK | |
| 0008 7213h | ICU | Interrupt request enable register 13 | IER13 | 8 | 8 | 2 | ICLK | |
| 0008 7214h | ICU | Interrupt request enable register 14 | IER14 | 8 | 8 | 2 | ICLK | |
| 0008 7215h | ICU | Interrupt request enable register 15 | IER15 | 8 | 8 | 2 | ICLK | |
| 0008 7216h | ICU | Interrupt request enable register 16 | IER16 | 8 | 8 | 2 | ICLK | |
| 0008 7217h | ICU | Interrupt request enable register 17 | IER17 | 8 | 8 | 2 | ICLK | |
| 0008 7218h | ICU | Interrupt request enable register 18 | IER18 | 8 | 8 | 2 | ICLK | |
| 0008 7219h | ICU | Interrupt request enable register 19 | IER19 | 8 | 8 | 2 | ICLK | |
| 0008 721Ah | ICU | Interrupt request enable register 1A | IER1A | 8 | 8 | 2 | ICLK | |
| 0008 721Bh | ICU | Interrupt request enable register 1B | IER1B | 8 | 8 | 2 | ICLK | |
| 0008 721Ch | ICU | Interrupt request enable register 1C | IER1C | 8 | 8 | 2 | ICLK | |
| 0008 721Dh | ICU | Interrupt request enable register 1D | IER1D | 8 | 8 | 2 | ICLK | |
| 0008 721Eh | ICU | Interrupt request enable register 1E | IER1E | 8 | 8 | 2 | ICLK | |
| 0008 721Fh | ICU | Interrupt request enable register 1F | IER1F | 8 | 8 | 2 | ICLK | |
| 0008 72E0h | ICU | Software interrupt activation register | SWINTR | 8 | 8 | 2 | ICLK | |
| 0008 72F0h | ICU | Fast interrupt set register | FIR | 16 | 16 | 2 | ICLK | |
| 0008 7300h | ICU | Interrupt source priority register 000 | IPR000 | 8 | 8 | 2 | ICLK | |
| 0008 7301h | ICU | Interrupt source priority register 001 | IPR001 | 8 | 8 | 2 | ICLK | |
| 0008 7302h | ICU | Interrupt source priority register 002 | IPR002 | 8 | 8 | 2 | ICLK | |
| 0008 7303h | ICU | Interrupt source priority register 003 | IPR003 | 8 | 8 | 2 | ICLK | |
| 0008 7304h | ICU | Interrupt source priority register 004 | IPR004 | 8 | 8 | 2 | ICLK | |
| 0008 7305h | ICU | Interrupt source priority register 005 | IPR005 | 8 | 8 | 2 | ICLK | |
| 0008 7306h | ICU | Interrupt source priority register 006 | IPR006 | 8 | 8 | 2 | ICLK | |
| 0008 7307h | ICU | Interrupt source priority register 007 | IPR007 | 8 | 8 | 2 | ICLK | |
| 0008 7320h | ICU | Interrupt source priority register 032 | IPR032 | 8 | 8 | 2 | ICLK | |
| 0008 7321h | ICU | Interrupt source priority register 033 | IPR033 | 8 | 8 | 2 | ICLK | |

Table 4.1 List of I/O Registers (Address Order) (12/50)

| Address | Module Symbol | Register Name | Register Symbol | Number of Bits | Access Size | Number of Access States | | Related Function |
|------------|---------------|--|-----------------|----------------|-------------|-------------------------|-----------|------------------|
| | | | | | | ICLK≥PCLK | ICLK<PCLK | |
| 0008 7322h | ICU | Interrupt source priority register 034 | IPR034 | 8 | 8 | 2 | ICLK | ICUb |
| 0008 7323h | ICU | Interrupt source priority register 035 | IPR035 | 8 | 8 | 2 | ICLK | |
| 0008 7324h | ICU | Interrupt source priority register 036 | IPR036 | 8 | 8 | 2 | ICLK | |
| 0008 7325h | ICU | Interrupt source priority register 037 | IPR037 | 8 | 8 | 2 | ICLK | |
| 0008 7326h | ICU | Interrupt source priority register 038 | IPR038 | 8 | 8 | 2 | ICLK | |
| 0008 7327h | ICU | Interrupt source priority register 039 | IPR039 | 8 | 8 | 2 | ICLK | |
| 0008 732Ah | ICU | Interrupt source priority register 042 | IPR042 | 8 | 8 | 2 | ICLK | |
| 0008 732Dh | ICU | Interrupt source priority register 045 | IPR045 | 8 | 8 | 2 | ICLK | |
| 0008 7330h | ICU | Interrupt source priority register 048 | IPR048 | 8 | 8 | 2 | ICLK | |
| 0008 7334h | ICU | Interrupt source priority register 052 | IPR052 | 8 | 8 | 2 | ICLK | |
| 0008 7338h | ICU | Interrupt source priority register 056 | IPR056 | 8 | 8 | 2 | ICLK | |
| 0008 733Eh | ICU | Interrupt source priority register 062 | IPR062 | 8 | 8 | 2 | ICLK | |
| 0008 7340h | ICU | Interrupt source priority register 064 | IPR064 | 8 | 8 | 2 | ICLK | |
| 0008 7341h | ICU | Interrupt source priority register 065 | IPR065 | 8 | 8 | 2 | ICLK | |
| 0008 7342h | ICU | Interrupt source priority register 066 | IPR066 | 8 | 8 | 2 | ICLK | |
| 0008 7343h | ICU | Interrupt source priority register 067 | IPR067 | 8 | 8 | 2 | ICLK | |
| 0008 7344h | ICU | Interrupt source priority register 068 | IPR068 | 8 | 8 | 2 | ICLK | |
| 0008 7345h | ICU | Interrupt source priority register 069 | IPR069 | 8 | 8 | 2 | ICLK | |
| 0008 7346h | ICU | Interrupt source priority register 070 | IPR070 | 8 | 8 | 2 | ICLK | |
| 0008 7347h | ICU | Interrupt source priority register 071 | IPR071 | 8 | 8 | 2 | ICLK | |
| 0008 7348h | ICU | Interrupt source priority register 072 | IPR072 | 8 | 8 | 2 | ICLK | |
| 0008 7349h | ICU | Interrupt source priority register 073 | IPR073 | 8 | 8 | 2 | ICLK | |
| 0008 734Ah | ICU | Interrupt source priority register 074 | IPR074 | 8 | 8 | 2 | ICLK | |
| 0008 734Bh | ICU | Interrupt source priority register 075 | IPR075 | 8 | 8 | 2 | ICLK | |
| 0008 734Ch | ICU | Interrupt source priority register 076 | IPR076 | 8 | 8 | 2 | ICLK | |
| 0008 734Dh | ICU | Interrupt source priority register 077 | IPR077 | 8 | 8 | 2 | ICLK | |
| 0008 734Eh | ICU | Interrupt source priority register 078 | IPR078 | 8 | 8 | 2 | ICLK | |
| 0008 734Fh | ICU | Interrupt source priority register 079 | IPR079 | 8 | 8 | 2 | ICLK | |
| 0008 735Ah | ICU | Interrupt source priority register 090 | IPR090 | 8 | 8 | 2 | ICLK | |
| 0008 735Bh | ICU | Interrupt source priority register 091 | IPR091 | 8 | 8 | 2 | ICLK | |
| 0008 735Ch | ICU | Interrupt source priority register 092 | IPR092 | 8 | 8 | 2 | ICLK | |
| 0008 735Dh | ICU | Interrupt source priority register 093 | IPR093 | 8 | 8 | 2 | ICLK | |
| 0008 7362h | ICU | Interrupt source priority register 098 | IPR098 | 8 | 8 | 2 | ICLK | |
| 0008 7366h | ICU | Interrupt source priority register 102 | IPR102 | 8 | 8 | 2 | ICLK | |
| 0008 736Ah | ICU | Interrupt source priority register 106 | IPR106 | 8 | 8 | 2 | ICLK | |
| 0008 736Bh | ICU | Interrupt source priority register 107 | IPR107 | 8 | 8 | 2 | ICLK | |
| 0008 736Ch | ICU | Interrupt source priority register 108 | IPR108 | 8 | 8 | 2 | ICLK | |
| 0008 736Dh | ICU | Interrupt source priority register 109 | IPR109 | 8 | 8 | 2 | ICLK | |
| 0008 736Eh | ICU | Interrupt source priority register 110 | IPR110 | 8 | 8 | 2 | ICLK | |
| 0008 736Fh | ICU | Interrupt source priority register 111 | IPR111 | 8 | 8 | 2 | ICLK | |
| 0008 7370h | ICU | Interrupt source priority register 112 | IPR112 | 8 | 8 | 2 | ICLK | |
| 0008 7372h | ICU | Interrupt source priority register 114 | IPR114 | 8 | 8 | 2 | ICLK | |
| 0008 737Ah | ICU | Interrupt source priority register 122 | IPR122 | 8 | 8 | 2 | ICLK | |
| 0008 737Eh | ICU | Interrupt source priority register 126 | IPR126 | 8 | 8 | 2 | ICLK | |
| 0008 7382h | ICU | Interrupt source priority register 130 | IPR130 | 8 | 8 | 2 | ICLK | |
| 0008 7384h | ICU | Interrupt source priority register 132 | IPR132 | 8 | 8 | 2 | ICLK | |
| 0008 7386h | ICU | Interrupt source priority register 134 | IPR134 | 8 | 8 | 2 | ICLK | |
| 0008 738Ah | ICU | Interrupt source priority register 138 | IPR138 | 8 | 8 | 2 | ICLK | |
| 0008 738Ch | ICU | Interrupt source priority register 140 | IPR140 | 8 | 8 | 2 | ICLK | |
| 0008 738Eh | ICU | Interrupt source priority register 142 | IPR142 | 8 | 8 | 2 | ICLK | |
| 0008 7392h | ICU | Interrupt source priority register 146 | IPR146 | 8 | 8 | 2 | ICLK | |

Table 4.1 List of I/O Registers (Address Order) (13/50)

| Address | Module Symbol | Register Name | Register Symbol | Number of Bits | Access Size | Number of Access States | | Related Function |
|------------|---------------|--|-----------------|----------------|-------------|-------------------------|-----------|------------------|
| | | | | | | ICLK≥PCLK | ICLK<PCLK | |
| 0008 7394h | ICU | Interrupt source priority register 148 | IPR148 | 8 | 8 | 2 | ICLK | ICUb |
| 0008 7396h | ICU | Interrupt source priority register 150 | IPR150 | 8 | 8 | 2 | ICLK | |
| 0008 7398h | ICU | Interrupt source priority register 152 | IPR152 | 8 | 8 | 2 | ICLK | |
| 0008 739Ch | ICU | Interrupt source priority register 156 | IPR156 | 8 | 8 | 2 | ICLK | |
| 0008 73A0h | ICU | Interrupt source priority register 160 | IPR160 | 8 | 8 | 2 | ICLK | |
| 0008 73A1h | ICU | Interrupt source priority register 161 | IPR161 | 8 | 8 | 2 | ICLK | |
| 0008 73A4h | ICU | Interrupt source priority register 164 | IPR164 | 8 | 8 | 2 | ICLK | |
| 0008 73A6h | ICU | Interrupt source priority register 166 | IPR166 | 8 | 8 | 2 | ICLK | |
| 0008 73AAh | ICU | Interrupt source priority register 170 | IPR170 | 8 | 8 | 2 | ICLK | |
| 0008 73ADh | ICU | Interrupt source priority register 173 | IPR173 | 8 | 8 | 2 | ICLK | |
| 0008 73B0h | ICU | Interrupt source priority register 176 | IPR176 | 8 | 8 | 2 | ICLK | |
| 0008 73B3h | ICU | Interrupt source priority register 179 | IPR179 | 8 | 8 | 2 | ICLK | |
| 0008 73B6h | ICU | Interrupt source priority register 182 | IPR182 | 8 | 8 | 2 | ICLK | |
| 0008 73B7h | ICU | Interrupt source priority register 183 | IPR183 | 8 | 8 | 2 | ICLK | |
| 0008 73B8h | ICU | Interrupt source priority register 184 | IPR184 | 8 | 8 | 2 | ICLK | |
| 0008 73B9h | ICU | Interrupt source priority register 185 | IPR185 | 8 | 8 | 2 | ICLK | |
| 0008 73BAh | ICU | Interrupt source priority register 186 | IPR186 | 8 | 8 | 2 | ICLK | |
| 0008 73BBh | ICU | Interrupt source priority register 187 | IPR187 | 8 | 8 | 2 | ICLK | |
| 0008 73BCh | ICU | Interrupt source priority register 188 | IPR188 | 8 | 8 | 2 | ICLK | |
| 0008 73BDh | ICU | Interrupt source priority register 189 | IPR189 | 8 | 8 | 2 | ICLK | |
| 0008 73BEh | ICU | Interrupt source priority register 190 | IPR190 | 8 | 8 | 2 | ICLK | |
| 0008 73BFh | ICU | Interrupt source priority register 191 | IPR191 | 8 | 8 | 2 | ICLK | |
| 0008 73C0h | ICU | Interrupt source priority register 192 | IPR192 | 8 | 8 | 2 | ICLK | |
| 0008 73C1h | ICU | Interrupt source priority register 193 | IPR193 | 8 | 8 | 2 | ICLK | |
| 0008 73C2h | ICU | Interrupt source priority register 194 | IPR194 | 8 | 8 | 2 | ICLK | |
| 0008 73C3h | ICU | Interrupt source priority register 195 | IPR195 | 8 | 8 | 2 | ICLK | |
| 0008 73C4h | ICU | Interrupt source priority register 196 | IPR196 | 8 | 8 | 2 | ICLK | |
| 0008 73C5h | ICU | Interrupt source priority register 197 | IPR197 | 8 | 8 | 2 | ICLK | |
| 0008 73C6h | ICU | Interrupt source priority register 198 | IPR198 | 8 | 8 | 2 | ICLK | |
| 0008 73C7h | ICU | Interrupt source priority register 199 | IPR199 | 8 | 8 | 2 | ICLK | |
| 0008 73C8h | ICU | Interrupt source priority register 200 | IPR200 | 8 | 8 | 2 | ICLK | |
| 0008 73C9h | ICU | Interrupt source priority register 201 | IPR201 | 8 | 8 | 2 | ICLK | |
| 0008 73CAh | ICU | Interrupt source priority register 202 | IPR202 | 8 | 8 | 2 | ICLK | |
| 0008 73CBh | ICU | Interrupt source priority register 203 | IPR203 | 8 | 8 | 2 | ICLK | |
| 0008 73CEh | ICU | Interrupt source priority register 206 | IPR206 | 8 | 8 | 2 | ICLK | |
| 0008 73CFh | ICU | Interrupt source priority register 207 | IPR207 | 8 | 8 | 2 | ICLK | |
| 0008 73D0h | ICU | Interrupt source priority register 208 | IPR208 | 8 | 8 | 2 | ICLK | |
| 0008 73D6h | ICU | Interrupt source priority register 214 | IPR214 | 8 | 8 | 2 | ICLK | |
| 0008 73D9h | ICU | Interrupt source priority register 217 | IPR217 | 8 | 8 | 2 | ICLK | |
| 0008 73DCh | ICU | Interrupt source priority register 220 | IPR220 | 8 | 8 | 2 | ICLK | |
| 0008 73DFh | ICU | Interrupt source priority register 223 | IPR223 | 8 | 8 | 2 | ICLK | |
| 0008 73E2h | ICU | Interrupt source priority register 226 | IPR226 | 8 | 8 | 2 | ICLK | |
| 0008 73E5h | ICU | Interrupt source priority register 229 | IPR229 | 8 | 8 | 2 | ICLK | |
| 0008 73E8h | ICU | Interrupt source priority register 232 | IPR232 | 8 | 8 | 2 | ICLK | |
| 0008 73EBh | ICU | Interrupt source priority register 235 | IPR235 | 8 | 8 | 2 | ICLK | |
| 0008 73EEh | ICU | Interrupt source priority register 238 | IPR238 | 8 | 8 | 2 | ICLK | |
| 0008 73F1h | ICU | Interrupt source priority register 241 | IPR241 | 8 | 8 | 2 | ICLK | |
| 0008 73F4h | ICU | Interrupt source priority register 244 | IPR244 | 8 | 8 | 2 | ICLK | |
| 0008 73F7h | ICU | Interrupt source priority register 247 | IPR247 | 8 | 8 | 2 | ICLK | |
| 0008 73FAh | ICU | Interrupt source priority register 250 | IPR250 | 8 | 8 | 2 | ICLK | |
| 0008 73FDh | ICU | Interrupt source priority register 253 | IPR253 | 8 | 8 | 2 | ICLK | |

Table 4.1 List of I/O Registers (Address Order) (14/50)

| Address | Module Symbol | Register Name | Register Symbol | Number of Bits | Access Size | Number of Access States | | Related Function | |
|------------|---------------|--|-----------------|----------------|-------------|-------------------------|-----------|------------------|-----|
| | | | | | | ICLK≥PCLK | ICLK<PCLK | | |
| 0008 7400h | ICU | DMAC activation request select register 0 | DMRSR0 | 8 | 8 | 2 ICLK | | ICUb | |
| 0008 7404h | ICU | DMAC activation request select register 1 | DMRSR1 | 8 | 8 | 2 ICLK | | | |
| 0008 7408h | ICU | DMAC activation request select register 2 | DMRSR2 | 8 | 8 | 2 ICLK | | | |
| 0008 740Ch | ICU | DMAC activation request select register 3 | DMRSR3 | 8 | 8 | 2 ICLK | | | |
| 0008 7500h | ICU | IRQ control register 0 | IRQCR0 | 8 | 8 | 2 ICLK | | | |
| 0008 7501h | ICU | IRQ control register 1 | IRQCR1 | 8 | 8 | 2 ICLK | | | |
| 0008 7502h | ICU | IRQ control register 2 | IRQCR2 | 8 | 8 | 2 ICLK | | | |
| 0008 7503h | ICU | IRQ control register 3 | IRQCR3 | 8 | 8 | 2 ICLK | | | |
| 0008 7504h | ICU | IRQ control register 4 | IRQCR4 | 8 | 8 | 2 ICLK | | | |
| 0008 7505h | ICU | IRQ control register 5 | IRQCR5 | 8 | 8 | 2 ICLK | | | |
| 0008 7506h | ICU | IRQ control register 6 | IRQCR6 | 8 | 8 | 2 ICLK | | | |
| 0008 7507h | ICU | IRQ control register 7 | IRQCR7 | 8 | 8 | 2 ICLK | | | |
| 0008 7508h | ICU | IRQ control register 8 | IRQCR8 | 8 | 8 | 2 ICLK | | | |
| 0008 7509h | ICU | IRQ control register 9 | IRQCR9 | 8 | 8 | 2 ICLK | | | |
| 0008 750Ah | ICU | IRQ control register 10 | IRQCR10 | 8 | 8 | 2 ICLK | | | |
| 0008 750Bh | ICU | IRQ control register 11 | IRQCR11 | 8 | 8 | 2 ICLK | | | |
| 0008 750Ch | ICU | IRQ control register 12 | IRQCR12 | 8 | 8 | 2 ICLK | | | |
| 0008 750Dh | ICU | IRQ control register 13 | IRQCR13 | 8 | 8 | 2 ICLK | | | |
| 0008 750Eh | ICU | IRQ control register 14 | IRQCR14 | 8 | 8 | 2 ICLK | | | |
| 0008 750Fh | ICU | IRQ control register 15 | IRQCR15 | 8 | 8 | 2 ICLK | | | |
| 0008 7510h | ICU | IRQ pin digital filter enable register 0 | IRQFLTE0 | 8 | 8 | 2 ICLK | | | |
| 0008 7511h | ICU | IRQ pin digital filter enable register 1 | IRQFLTE1 | 8 | 8 | 2 ICLK | | | |
| 0008 7514h | ICU | IRQ pin digital filter setting register 0 | IRQFLTC0 | 16 | 16 | 2 ICLK | | | |
| 0008 7516h | ICU | IRQ pin digital filter setting register 1 | IRQFLTC1 | 16 | 16 | 2 ICLK | | | |
| 0008 7580h | ICU | Non-maskable interrupt status register | NMISR | 8 | 8 | 2 ICLK | | | |
| 0008 7581h | ICU | Non-maskable interrupt enable register | NMIER | 8 | 8 | 2 ICLK | | | |
| 0008 7582h | ICU | Non-maskable interrupt status clear register | NMICLR | 8 | 8 | 2 ICLK | | | |
| 0008 7583h | ICU | NMI pin interrupt control register | NMICR | 8 | 8 | 2 ICLK | | | |
| 0008 7590h | ICU | NMI pin digital filter enable register | NMIFLTE | 8 | 8 | 2 ICLK | | | |
| 0008 7594h | ICU | NMI pin digital filter setting register | NMIFLTC | 16 | 16 | 2 ICLK | | | |
| 0008 8000h | CMT | Compare match timer start register 0 | CMSTR0 | 16 | 16 | 2, 3 PCLKB | 2 ICLK | | CMT |
| 0008 8002h | CMT0 | Compare match timer control register | CMCR | 16 | 16 | 2, 3 PCLKB | 2 ICLK | | |
| 0008 8004h | CMT0 | Compare match timer counter | CMCNT | 16 | 16 | 2, 3 PCLKB | 2 ICLK | | |
| 0008 8006h | CMT0 | Compare match timer constant register | CMCOR | 16 | 16 | 2, 3 PCLKB | 2 ICLK | | |
| 0008 8008h | CMT1 | Compare match timer control register | CMCR | 16 | 16 | 2, 3 PCLKB | 2 ICLK | | |
| 0008 800Ah | CMT1 | Compare match timer counter | CMCNT | 16 | 16 | 2, 3 PCLKB | 2 ICLK | | |
| 0008 800Ch | CMT1 | Compare match timer constant register | CMCOR | 16 | 16 | 2, 3 PCLKB | 2 ICLK | | |
| 0008 8010h | CMT | Compare match timer start register 1 | CMSTR1 | 16 | 16 | 2, 3 PCLKB | 2 ICLK | | |
| 0008 8012h | CMT2 | Compare match timer control register | CMCR | 16 | 16 | 2, 3 PCLKB | 2 ICLK | | |
| 0008 8014h | CMT2 | Compare match timer counter | CMCNT | 16 | 16 | 2, 3 PCLKB | 2 ICLK | | |
| 0008 8016h | CMT2 | Compare match timer constant register | CMCOR | 16 | 16 | 2, 3 PCLKB | 2 ICLK | | |
| 0008 8018h | CMT3 | Compare match timer control register | CMCR | 16 | 16 | 2, 3 PCLKB | 2 ICLK | | |
| 0008 801Ah | CMT3 | Compare match timer counter | CMCNT | 16 | 16 | 2, 3 PCLKB | 2 ICLK | | |
| 0008 801Ch | CMT3 | Compare match timer constant register | CMCOR | 16 | 16 | 2, 3 PCLKB | 2 ICLK | | |
| 0008 8020h | WDT | WDT refresh register | WDTRR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | WDTA | |
| 0008 8022h | WDT | WDT control register | WDTCR | 16 | 16 | 2, 3 PCLKB | 2 ICLK | | |
| 0008 8024h | WDT | WDT status register | WDTSR | 16 | 16 | 2, 3 PCLKB | 2 ICLK | | |
| 0008 8026h | WDT | WDT reset control register | WDTRCR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | | |
| 0008 8030h | IWDT | IWDT refresh register | IWDTRR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | | |
| 0008 8032h | IWDT | IWDT control register | IWDTCR | 16 | 16 | 2, 3 PCLKB | 2 ICLK | | |
| 0008 8034h | IWDT | IWDT status register | IWDTSR | 16 | 16 | 2, 3 PCLKB | 2 ICLK | | |

Table 4.1 List of I/O Registers (Address Order) (15/50)

| Address | Module Symbol | Register Name | Register Symbol | Number of Bits | Access Size | Number of Access States | | Related Function |
|------------|---------------|--|-----------------|----------------|-------------|-------------------------|-----------|------------------|
| | | | | | | ICLK>PCLK | ICLK<PCLK | |
| 0008 8036h | IWDT | IWDT reset control register | IWDTRCR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | IWDTa |
| 0008 8038h | IWDT | IWDT count stop control register | IWDTCSTPR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 80C0h | DA | D/A data register 0 | DADR0 | 16 | 16 | 2, 3 PCLKB | 2 ICLK | DAa |
| 0008 80C2h | DA | D/A data register 1 | DADR1 | 16 | 16 | 2, 3 PCLKB | 2 ICLK | |
| 0008 80C4h | DA | D/A control register | DACR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 80C5h | DA | DADRm format select register | DADPR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 80C6h | DA | D/A A/D synchronous start control register | DAADSCR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 8100h | TPUA | Timer start register | TSTR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 8101h | TPUA | Timer synchronous register | TSYR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 8108h | TPU0 | Noise filter control register | NFCR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 8109h | TPU1 | Noise filter control register | NFCR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 810Ah | TPU2 | Noise filter control register | NFCR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 810Bh | TPU3 | Noise filter control register | NFCR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 810Ch | TPU4 | Noise filter control register | NFCR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 810Dh | TPU5 | Noise filter control register | NFCR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 8110h | TPU0 | Timer control register | TCR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 8111h | TPU0 | Timer mode register | TMDR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 8112h | TPU0 | Timer I/O control register H | TIORH | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 8113h | TPU0 | Timer I/O control register L | TIORL | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 8114h | TPU0 | Timer interrupt enable register | TIER | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 8115h | TPU0 | Timer status register | TSR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 8116h | TPU0 | Timer counter | TCNT | 16 | 16 | 2, 3 PCLKB | 2 ICLK | |
| 0008 8118h | TPU0 | Timer general register A | TGRA | 16 | 16 | 2, 3 PCLKB | 2 ICLK | |
| 0008 811Ah | TPU0 | Timer general register B | TGRB | 16 | 16 | 2, 3 PCLKB | 2 ICLK | |
| 0008 811Ch | TPU0 | Timer general register C | TGRC | 16 | 16 | 2, 3 PCLKB | 2 ICLK | |
| 0008 811Eh | TPU0 | Timer general register D | TGRD | 16 | 16 | 2, 3 PCLKB | 2 ICLK | |
| 0008 8120h | TPU1 | Timer control register | TCR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 8121h | TPU1 | Timer mode register | TMDR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 8122h | TPU1 | Timer I/O control register | TIOR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 8124h | TPU1 | Timer interrupt enable register | TIER | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 8125h | TPU1 | Timer status register | TSR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 8126h | TPU1 | Timer counter | TCNT | 16 | 16 | 2, 3 PCLKB | 2 ICLK | |
| 0008 8128h | TPU1 | Timer general register A | TGRA | 16 | 16 | 2, 3 PCLKB | 2 ICLK | |
| 0008 812Ah | TPU1 | Timer general register B | TGRB | 16 | 16 | 2, 3 PCLKB | 2 ICLK | |
| 0008 8130h | TPU2 | Timer control register | TCR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 8131h | TPU2 | Timer mode register | TMDR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 8132h | TPU2 | Timer I/O control register | TIOR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 8134h | TPU2 | Timer interrupt enable register | TIER | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 8135h | TPU2 | Timer status register | TSR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 8136h | TPU2 | Timer counter | TCNT | 16 | 16 | 2, 3 PCLKB | 2 ICLK | |
| 0008 8138h | TPU2 | Timer general register A | TGRA | 16 | 16 | 2, 3 PCLKB | 2 ICLK | |
| 0008 813Ah | TPU2 | Timer general register B | TGRB | 16 | 16 | 2, 3 PCLKB | 2 ICLK | |
| 0008 8140h | TPU3 | Timer control register | TCR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 8141h | TPU3 | Timer mode register | TMDR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 8142h | TPU3 | Timer I/O control register H | TIORH | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 8143h | TPU3 | Timer I/O control register L | TIORL | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 8144h | TPU3 | Timer interrupt enable register | TIER | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 8145h | TPU3 | Timer status register | TSR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 8146h | TPU3 | Timer counter | TCNT | 16 | 16 | 2, 3 PCLKB | 2 ICLK | |
| 0008 8148h | TPU3 | Timer general register A | TGRA | 16 | 16 | 2, 3 PCLKB | 2 ICLK | |
| 0008 814Ah | TPU3 | Timer general register B | TGRB | 16 | 16 | 2, 3 PCLKB | 2 ICLK | |

Table 4.1 List of I/O Registers (Address Order) (16/50)

| Address | Module Symbol | Register Name | Register Symbol | Number of Bits | Access Size | Number of Access States | | Related Function |
|------------|---------------|---------------------------------|-----------------|----------------|-------------|-------------------------|-----------|------------------|
| | | | | | | ICLK>PCLK | ICLK<PCLK | |
| 0008 814Ch | TPU3 | Timer general register C | TGRC | 16 | 16 | 2, 3 PCLKB | 2 ICLK | TPUa |
| 0008 814Eh | TPU3 | Timer general register D | TGRD | 16 | 16 | 2, 3 PCLKB | 2 ICLK | |
| 0008 8150h | TPU4 | Timer control register | TCR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 8151h | TPU4 | Timer mode register | TMDR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 8152h | TPU4 | Timer I/O control register | TIOR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 8154h | TPU4 | Timer interrupt enable register | TIER | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 8155h | TPU4 | Timer status register | TSR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 8156h | TPU4 | Timer counter | TCNT | 16 | 16 | 2, 3 PCLKB | 2 ICLK | |
| 0008 8158h | TPU4 | Timer general register A | TGRA | 16 | 16 | 2, 3 PCLKB | 2 ICLK | |
| 0008 815Ah | TPU4 | Timer general register B | TGRB | 16 | 16 | 2, 3 PCLKB | 2 ICLK | |
| 0008 8160h | TPU5 | Timer control register | TCR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 8161h | TPU5 | Timer mode register | TMDR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 8162h | TPU5 | Timer I/O control register | TIOR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 8164h | TPU5 | Timer interrupt enable register | TIER | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 8165h | TPU5 | Timer status register | TSR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 8166h | TPU5 | Timer counter | TCNT | 16 | 16 | 2, 3 PCLKB | 2 ICLK | |
| 0008 8168h | TPU5 | Timer general register A | TGRA | 16 | 16 | 2, 3 PCLKB | 2 ICLK | |
| 0008 816Ah | TPU5 | Timer general register B | TGRB | 16 | 16 | 2, 3 PCLKB | 2 ICLK | |
| 0008 8170h | TPUB | Timer start register | TSTR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 8171h | TPUB | Timer synchronous register | TSYR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 8178h | TPU6 | Noise filter control register | NFCR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 8179h | TPU7 | Noise filter control register | NFCR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 817Ah | TPU8 | Noise filter control register | NFCR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 817Bh | TPU9 | Noise filter control register | NFCR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 817Ch | TPU10 | Noise filter control register | NFCR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 817Dh | TPU11 | Noise filter control register | NFCR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 8180h | TPU6 | Timer control register | TCR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 8181h | TPU6 | Timer mode register | TMDR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 8182h | TPU6 | Timer I/O control register H | TIORH | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 8183h | TPU6 | Timer I/O control register L | TIORL | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 8184h | TPU6 | Timer interrupt enable register | TIER | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 8185h | TPU6 | Timer status register | TSR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 8186h | TPU6 | Timer counter | TCNT | 16 | 16 | 2, 3 PCLKB | 2 ICLK | |
| 0008 8188h | TPU6 | Timer general register A | TGRA | 16 | 16 | 2, 3 PCLKB | 2 ICLK | |
| 0008 818Ah | TPU6 | Timer general register B | TGRB | 16 | 16 | 2, 3 PCLKB | 2 ICLK | |
| 0008 818Ch | TPU6 | Timer general register C | TGRC | 16 | 16 | 2, 3 PCLKB | 2 ICLK | |
| 0008 818Eh | TPU6 | Timer general register D | TGRD | 16 | 16 | 2, 3 PCLKB | 2 ICLK | |
| 0008 8190h | TPU7 | Timer control register | TCR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 8191h | TPU7 | Timer mode register | TMDR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 8192h | TPU7 | Timer I/O control register | TIOR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 8194h | TPU7 | Timer interrupt enable register | TIER | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 8195h | TPU7 | Timer status register | TSR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 8196h | TPU7 | Timer counter | TCNT | 16 | 16 | 2, 3 PCLKB | 2 ICLK | |
| 0008 8198h | TPU7 | Timer general register A | TGRA | 16 | 16 | 2, 3 PCLKB | 2 ICLK | |
| 0008 819Ah | TPU7 | Timer general register B | TGRB | 16 | 16 | 2, 3 PCLKB | 2 ICLK | |
| 0008 81A0h | TPU8 | Timer control register | TCR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 81A1h | TPU8 | Timer mode register | TMDR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 81A2h | TPU8 | Timer I/O control register | TIOR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 81A4h | TPU8 | Timer interrupt enable register | TIER | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 81A5h | TPU8 | Timer status register | TSR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 81A6h | TPU8 | Timer counter | TCNT | 16 | 16 | 2, 3 PCLKB | 2 ICLK | |

Table 4.1 List of I/O Registers (Address Order) (17/50)

| Address | Module Symbol | Register Name | Register Symbol | Number of Bits | Access Size | Number of Access States | | Related Function | |
|--------------------------|---------------|---------------------------------|-----------------|----------------|-------------|-------------------------|-----------|------------------|-----|
| | | | | | | ICLK>PCLK | ICLK<PCLK | | |
| 0008 81A8h | TPU8 | Timer general register A | TGRA | 16 | 16 | 2, 3 PCLKB | 2 ICLK | TPUa | |
| 0008 81AAh | TPU8 | Timer general register B | TGRB | 16 | 16 | 2, 3 PCLKB | 2 ICLK | | |
| 0008 81B0h | TPU9 | Timer control register | TCR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | | |
| 0008 81B1h | TPU9 | Timer mode register | TMDR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | | |
| 0008 81B2h | TPU9 | Timer I/O control register H | TIORH | 8 | 8 | 2, 3 PCLKB | 2 ICLK | | |
| 0008 81B3h | TPU9 | Timer I/O control register L | TIORL | 8 | 8 | 2, 3 PCLKB | 2 ICLK | | |
| 0008 81B4h | TPU9 | Timer interrupt enable register | TIER | 8 | 8 | 2, 3 PCLKB | 2 ICLK | | |
| 0008 81B5h | TPU9 | Timer status register | TSR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | | |
| 0008 81B6h | TPU9 | Timer counter | TCNT | 16 | 16 | 2, 3 PCLKB | 2 ICLK | | |
| 0008 81B8h | TPU9 | Timer general register A | TGRA | 16 | 16 | 2, 3 PCLKB | 2 ICLK | | |
| 0008 81BAh | TPU9 | Timer general register B | TGRB | 16 | 16 | 2, 3 PCLKB | 2 ICLK | | |
| 0008 81BCh | TPU9 | Timer general register C | TGRC | 16 | 16 | 2, 3 PCLKB | 2 ICLK | | |
| 0008 81BEh | TPU9 | Timer general register D | TGRD | 16 | 16 | 2, 3 PCLKB | 2 ICLK | | |
| 0008 81C0h | TPU10 | Timer control register | TCR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | | |
| 0008 81C1h | TPU10 | Timer mode register | TMDR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | | |
| 0008 81C2h | TPU10 | Timer I/O control register | TIOR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | | |
| 0008 81C4h | TPU10 | Timer interrupt enable register | TIER | 8 | 8 | 2, 3 PCLKB | 2 ICLK | | |
| 0008 81C5h | TPU10 | Timer status register | TSR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | | |
| 0008 81C6h | TPU10 | Timer counter | TCNT | 16 | 16 | 2, 3 PCLKB | 2 ICLK | | |
| 0008 81C8h | TPU10 | Timer general register A | TGRA | 16 | 16 | 2, 3 PCLKB | 2 ICLK | | |
| 0008 81CAh | TPU10 | Timer general register B | TGRB | 16 | 16 | 2, 3 PCLKB | 2 ICLK | | |
| 0008 81D0h | TPU11 | Timer control register | TCR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | | |
| 0008 81D1h | TPU11 | Timer mode register | TMDR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | | |
| 0008 81D2h | TPU11 | Timer I/O control register | TIOR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | | |
| 0008 81D4h | TPU11 | Timer interrupt enable register | TIER | 8 | 8 | 2, 3 PCLKB | 2 ICLK | | |
| 0008 81D5h | TPU11 | Timer status register | TSR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | | |
| 0008 81D6h | TPU11 | Timer counter | TCNT | 16 | 16 | 2, 3 PCLKB | 2 ICLK | | |
| 0008 81D8h | TPU11 | Timer general register A | TGRA | 16 | 16 | 2, 3 PCLKB | 2 ICLK | | |
| 0008 81DAh | TPU11 | Timer general register B | TGRB | 16 | 16 | 2, 3 PCLKB | 2 ICLK | | |
| 0008 81E6h | PPG0 | PPG output control register | PCR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | PPG | |
| 0008 81E7h | PPG0 | PPG output mode register | PMR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | | |
| 0008 81E8h | PPG0 | Next data enable register H | NDERH | 8 | 8 | 2, 3 PCLKB | 2 ICLK | | |
| 0008 81E9h | PPG0 | Next data enable register L | NDERL | 8 | 8 | 2, 3 PCLKB | 2 ICLK | | |
| 0008 81EAh | PPG0 | Output data register H | PODRH | 8 | 8 | 2, 3 PCLKB | 2 ICLK | | |
| 0008 81EBh | PPG0 | Output data register L | PODRL | 8 | 8 | 2, 3 PCLKB | 2 ICLK | | |
| 0008 81ECh ^{*1} | PPG0 | Next data register H | NDRH | 8 | 8 | 2, 3 PCLKB | 2 ICLK | | |
| 0008 81EDh ^{*2} | PPG0 | Next data register L | NDRL | 8 | 8 | 2, 3 PCLKB | 2 ICLK | | |
| 0008 81EEh ^{*1} | PPG0 | Next data register H | NDRH2 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | | |
| 0008 81EFh ^{*2} | PPG0 | Next data register L | NDRL2 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | | |
| 0008 81F0h | PPG1 | PPG trigger select register | PTRSLR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | | |
| 0008 81F6h | PPG1 | PPG output control register | PCR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | | |
| 0008 81F7h | PPG1 | PPG output mode register | PMR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | | |
| 0008 81F8h | PPG1 | Next data enable register H | NDERH | 8 | 8 | 2, 3 PCLKB | 2 ICLK | | |
| 0008 81F9h | PPG1 | Next data enable register L | NDERL | 8 | 8 | 2, 3 PCLKB | 2 ICLK | | |
| 0008 81FAh | PPG1 | Output data register H | PODRH | 8 | 8 | 2, 3 PCLKB | 2 ICLK | | |
| 0008 81FBh | PPG1 | Output data register L | PODRL | 8 | 8 | 2, 3 PCLKB | 2 ICLK | | |
| 0008 81FCh ^{*3} | PPG1 | Next data register H | NDRH | 8 | 8 | 2, 3 PCLKB | 2 ICLK | | |
| 0008 81FDh ^{*4} | PPG1 | Next data register L | NDRL | 8 | 8 | 2, 3 PCLKB | 2 ICLK | | |
| 0008 81FEh ^{*3} | PPG1 | Next data register H | NDRH2 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | | PPG |
| 0008 81FFh ^{*4} | PPG1 | Next data register L | NDRL2 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | | |

Table 4.1 List of I/O Registers (Address Order) (18/50)

| Address | Module Symbol | Register Name | Register Symbol | Number of Bits | Access Size | Number of Access States | | Related Function | |
|------------|---------------|---|-----------------|----------------|----------------|-------------------------|-----------|------------------|------|
| | | | | | | ICLK≥PCLK | ICLK<PCLK | | |
| 0008 8200h | TMR0 | Timer control register | TCR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | TMR | |
| 0008 8201h | TMR1 | Timer control register | TCR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | | |
| 0008 8202h | TMR0 | Timer control/status register | TCSR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | | |
| 0008 8203h | TMR1 | Timer control/status register | TCSR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | | |
| 0008 8204h | TMR0 | Time constant register A | TCORA | 8 | 8 | 2, 3 PCLKB | 2 ICLK | | |
| 0008 8205h | TMR1 | Time constant register A | TCORA | 8 | 8 ⁵ | 2, 3 PCLKB | 2 ICLK | | |
| 0008 8206h | TMR0 | Time constant register B | TCORB | 8 | 8 | 2, 3 PCLKB | 2 ICLK | | |
| 0008 8207h | TMR1 | Time constant register B | TCORB | 8 | 8 ⁵ | 2, 3 PCLKB | 2 ICLK | | |
| 0008 8208h | TMR0 | Timer counter | TCNT | 8 | 8 | 2, 3 PCLKB | 2 ICLK | | |
| 0008 8209h | TMR1 | Timer counter | TCNT | 8 | 8 ⁵ | 2, 3 PCLKB | 2 ICLK | | |
| 0008 820Ah | TMR0 | Timer counter control register | TCCR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | | |
| 0008 820Bh | TMR1 | Timer counter control register | TCCR | 8 | 8 ⁵ | 2, 3 PCLKB | 2 ICLK | | |
| 0008 8210h | TMR2 | Timer control register | TCR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | | |
| 0008 8211h | TMR3 | Timer control register | TCR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | | |
| 0008 8212h | TMR2 | Timer control/status register | TCSR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | | |
| 0008 8213h | TMR3 | Timer control/status register | TCSR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | | |
| 0008 8214h | TMR2 | Time constant register A | TCORA | 8 | 8 | 2, 3 PCLKB | 2 ICLK | | |
| 0008 8215h | TMR3 | Time constant register A | TCORA | 8 | 8 ⁵ | 2, 3 PCLKB | 2 ICLK | | |
| 0008 8216h | TMR2 | Time constant register B | TCORB | 8 | 8 | 2, 3 PCLKB | 2 ICLK | | |
| 0008 8217h | TMR3 | Time constant register B | TCORB | 8 | 8 | 2, 3 PCLKB | 2 ICLK | | |
| 0008 8218h | TMR2 | Timer counter | TCNT | 8 | 8 | 2, 3 PCLKB | 2 ICLK | | |
| 0008 8219h | TMR3 | Timer counter | TCNT | 8 | 8 ⁵ | 2, 3 PCLKB | 2 ICLK | | |
| 0008 821Ah | TMR2 | Timer counter control register | TCCR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | | |
| 0008 821Bh | TMR3 | Timer counter control register | TCCR | 8 | 8 ⁵ | 2, 3 PCLKB | 2 ICLK | | |
| 0008 8280h | CRC | CRC control register | CRCCR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | | CRC |
| 0008 8281h | CRC | CRC data input register | CRCDIR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | | |
| 0008 8282h | CRC | CRC data output register | CRCDOR | 16 | 16 | 2, 3 PCLKB | 2 ICLK | | |
| 0008 8300h | RIIC0 | I ² C bus control register 1 | ICCR1 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | | RIIC |
| 0008 8301h | RIIC0 | I ² C bus control register 2 | ICCR2 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | | |
| 0008 8302h | RIIC0 | I ² C bus mode register 1 | ICMR1 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | | |
| 0008 8303h | RIIC0 | I ² C bus mode register 2 | ICMR2 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | | |
| 0008 8304h | RIIC0 | I ² C bus mode register 3 | ICMR3 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | | |
| 0008 8305h | RIIC0 | I ² C bus function enable register | ICFER | 8 | 8 | 2, 3 PCLKB | 2 ICLK | | |
| 0008 8306h | RIIC0 | I ² C bus status enable register | ICSER | 8 | 8 | 2, 3 PCLKB | 2 ICLK | | |
| 0008 8307h | RIIC0 | I ² C bus interrupt enable register | ICIER | 8 | 8 | 2, 3 PCLKB | 2 ICLK | | |
| 0008 8308h | RIIC0 | I ² C bus status register 1 | ICSR1 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | | |
| 0008 8309h | RIIC0 | I ² C bus status register 2 | ICSR2 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | | |
| 0008 830Ah | RIIC0 | Slave address register L0 | SARL0 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | | |
| 0008 830Ah | RIIC0 | Timeout Internal Counter L | TMOCNTL | 8 | 8 | 2, 3 PCLKB | 2 ICLK | | |
| 0008 830Bh | RIIC0 | Slave address register U0 | SARU0 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | | |
| 0008 830Bh | RIIC0 | Timeout Internal Counter U | TMOCNTU | 8 | 8 | 2, 3 PCLKB | 2 ICLK | | |
| 0008 830Ch | RIIC0 | Slave address register L1 | SARL1 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | | |
| 0008 830Dh | RIIC0 | Slave address register U1 | SARU1 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | | |
| 0008 830Eh | RIIC0 | Slave address register L2 | SARL2 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | | |
| 0008 830Fh | RIIC0 | Slave address register U2 | SARU2 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | | |
| 0008 8310h | RIIC0 | I ² C bus bit rate low-level register | ICBRL | 8 | 8 | 2, 3 PCLKB | 2 ICLK | | |
| 0008 8311h | RIIC0 | I ² C bus bit rate high-level register | ICBRH | 8 | 8 | 2, 3 PCLKB | 2 ICLK | | |
| 0008 8312h | RIIC0 | I ² C bus transmit data register | ICDRT | 8 | 8 | 2, 3 PCLKB | 2 ICLK | | |

Table 4.1 List of I/O Registers (Address Order) (19/50)

| Address | Module Symbol | Register Name | Register Symbol | Number of Bits | Access Size | Number of Access States | | Related Function |
|------------|---------------|---|-----------------|----------------|-------------|-------------------------|---------------|------------------|
| | | | | | | ICLK \geq PCLK | ICLK $<$ PCLK | |
| 0008 8313h | RIIC0 | I ² C bus receive data register | ICDRR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | RIIC |
| 0008 8320h | RIIC1 | I ² C bus control register 1 | ICCR1 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 8321h | RIIC1 | I ² C bus control register 2 | ICCR2 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 8322h | RIIC1 | I ² C bus mode register 1 | ICMR1 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 8323h | RIIC1 | I ² C bus mode register 2 | ICMR2 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 8324h | RIIC1 | I ² C bus mode register 3 | ICMR3 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 8325h | RIIC1 | I ² C bus function enable register | ICFER | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 8326h | RIIC1 | I ² C bus status enable register | ICSER | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 8327h | RIIC1 | I ² C bus interrupt enable register | ICIER | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 8328h | RIIC1 | I ² C bus status register 1 | ICSR1 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 8329h | RIIC1 | I ² C bus status register 2 | ICSR2 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 832Ah | RIIC1 | Slave address register L0 | SARL0 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 832Ah | RIIC1 | Timeout Internal Counter L | TMOCNTL | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 832Bh | RIIC1 | Slave address register U0 | SARU0 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 832Bh | RIIC1 | Timeout Internal Counter U | TMOCNTU | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 832Ch | RIIC1 | Slave address register L1 | SARL1 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 832Dh | RIIC1 | Slave address register U1 | SARU1 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 832Eh | RIIC1 | Slave address register L2 | SARL2 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 832Fh | RIIC1 | Slave address register U2 | SARU2 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 8330h | RIIC1 | I ² C bus bit rate low-level register | ICBRL | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 8331h | RIIC1 | I ² C bus bit rate high-level register | ICBRH | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 8332h | RIIC1 | I ² C bus transmit data register | ICDRT | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 8333h | RIIC1 | I ² C bus receive data register | ICDRR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 8340h | RIIC2 | I ² C bus control register 1 | ICCR1 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 8341h | RIIC2 | I ² C bus control register 2 | ICCR2 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 8342h | RIIC2 | I ² C bus mode register 1 | ICMR1 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 8343h | RIIC2 | I ² C bus mode register 2 | ICMR2 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 8344h | RIIC2 | I ² C bus mode register 3 | ICMR3 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 8345h | RIIC2 | I ² C bus function enable register | ICFER | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 8346h | RIIC2 | I ² C bus status enable register | ICSER | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 8347h | RIIC2 | I ² C bus interrupt enable register | ICIER | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 8348h | RIIC2 | I ² C bus status register 1 | ICSR1 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 8349h | RIIC2 | I ² C bus status register 2 | ICSR2 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 834Ah | RIIC2 | Slave address register L0 | SARL0 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 834Bh | RIIC2 | Slave address register U0 | SARU0 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 834Ch | RIIC2 | Slave address register L1 | SARL1 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 834Dh | RIIC2 | Slave address register U1 | SARU1 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 834Eh | RIIC2 | Slave address register L2 | SARL2 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 834Fh | RIIC2 | Slave address register U2 | SARU2 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 8350h | RIIC2 | I ² C bus bit rate low-level register | ICBRL | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 8351h | RIIC2 | I ² C bus bit rate high-level register | ICBRH | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 8352h | RIIC2 | I ² C bus transmit data register | ICDRT | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 8353h | RIIC2 | I ² C bus receive data register | ICDRR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 8360h | RIIC3 | I ² C bus control register 1 | ICCR1 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 8361h | RIIC3 | I ² C bus control register 2 | ICCR2 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 8362h | RIIC3 | I ² C bus mode register 1 | ICMR1 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 8363h | RIIC3 | I ² C bus mode register 2 | ICMR2 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 8364h | RIIC3 | I ² C bus mode register 3 | ICMR3 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 8365h | RIIC3 | I ² C bus function enable register | ICFER | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 8366h | RIIC3 | I ² C bus status enable register | ICSER | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 8367h | RIIC3 | I ² C bus interrupt enable register | ICIER | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |

Table 4.1 List of I/O Registers (Address Order) (20/50)

| Address | Module Symbol | Register Name | Register Symbol | Number of Bits | Access Size | Number of Access States | | Related Function |
|------------|---------------|---|-----------------|----------------|-------------|-------------------------|-----------|------------------|
| | | | | | | ICLK≥PCLK | ICLK<PCLK | |
| 0008 8368h | RIIC3 | I ² C bus status register 1 | ICSR1 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | RSPI |
| 0008 8369h | RIIC3 | I ² C bus status register 2 | ICSR2 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 836Ah | RIIC3 | Slave address register L0 | SARL0 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 836Bh | RIIC3 | Slave address register U0 | SARU0 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 836Ch | RIIC3 | Slave address register L1 | SARL1 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 836Dh | RIIC3 | Slave address register U1 | SARU1 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 836Eh | RIIC3 | Slave address register L2 | SARL2 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 836Fh | RIIC3 | Slave address register U2 | SARU2 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 8370h | RIIC3 | I ² C bus bit rate low-level register | ICBRL | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 8371h | RIIC3 | I ² C bus bit rate high-level register | ICBRH | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 8372h | RIIC3 | I ² C bus transmit data register | ICDRT | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 8373h | RIIC3 | I ² C bus receive data register | ICDRR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 8380h | RSPI0 | RSPI control register | SPCR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 8381h | RSPI0 | RSPI slave select polarity register | SSLP | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 8382h | RSPI0 | RSPI pin control register | SPPCR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 8383h | RSPI0 | RSPI status register | SPSR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 8384h | RSPI0 | RSPI data register | SPDR | 32 | 16, 32 | 2, 3 PCLKB | 2 ICLK | |
| 0008 8388h | RSPI0 | RSPI sequence control register | SPSCR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 8389h | RSPI0 | RSPI sequence status register | SPSSR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 838Ah | RSPI0 | RSPI bit rate register | SPBR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 838Bh | RSPI0 | RSPI data control register | SPDCR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 838Ch | RSPI0 | RSPI clock delay register | SPCKD | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 838Dh | RSPI0 | RSPI slave select negation delay register | SSLND | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 838Eh | RSPI0 | RSPI next-access delay register | SPND | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 838Fh | RSPI0 | RSPI control register 2 | SPCR2 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 8390h | RSPI0 | RSPI command register 0 | SPCMD0 | 16 | 16 | 2, 3 PCLKB | 2 ICLK | |
| 0008 8392h | RSPI0 | RSPI command register 1 | SPCMD1 | 16 | 16 | 2, 3 PCLKB | 2 ICLK | |
| 0008 8394h | RSPI0 | RSPI command register 2 | SPCMD2 | 16 | 16 | 2, 3 PCLKB | 2 ICLK | |
| 0008 8396h | RSPI0 | RSPI command register 3 | SPCMD3 | 16 | 16 | 2, 3 PCLKB | 2 ICLK | |
| 0008 8398h | RSPI0 | RSPI command register 4 | SPCMD4 | 16 | 16 | 2, 3 PCLKB | 2 ICLK | |
| 0008 839Ah | RSPI0 | RSPI command register 5 | SPCMD5 | 16 | 16 | 2, 3 PCLKB | 2 ICLK | |
| 0008 839Ch | RSPI0 | RSPI command register 6 | SPCMD6 | 16 | 16 | 2, 3 PCLKB | 2 ICLK | |
| 0008 839Eh | RSPI0 | RSPI command register 7 | SPCMD7 | 16 | 16 | 2, 3 PCLKB | 2 ICLK | |
| 0008 83A0h | RSPI1 | RSPI control register | SPCR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 83A1h | RSPI1 | RSPI slave select polarity register | SSLP | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 83A2h | RSPI1 | RSPI pin control register | SPPCR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 83A3h | RSPI1 | RSPI status register | SPSR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 83A4h | RSPI1 | RSPI data register | SPDR | 32 | 16, 32 | 2, 3 PCLKB | 2 ICLK | |
| 0008 83A8h | RSPI1 | RSPI sequence control register | SPSCR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 83A9h | RSPI1 | RSPI sequence status register | SPSSR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 83AAh | RSPI1 | RSPI bit rate register | SPBR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 83ABh | RSPI1 | RSPI data control register | SPDCR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 83ACh | RSPI1 | RSPI clock delay register | SPCKD | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 83ADh | RSPI1 | RSPI slave select negation delay register | SSLND | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 83AEh | RSPI1 | RSPI next-access delay register | SPND | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 83AFh | RSPI1 | RSPI control register 2 | SPCR2 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 83B0h | RSPI1 | RSPI command register 0 | SPCMD0 | 16 | 16 | 2, 3 PCLKB | 2 ICLK | |
| 0008 83B2h | RSPI1 | RSPI command register 1 | SPCMD1 | 16 | 16 | 2, 3 PCLKB | 2 ICLK | |
| 0008 83B4h | RSPI1 | RSPI command register 2 | SPCMD2 | 16 | 16 | 2, 3 PCLKB | 2 ICLK | |
| 0008 83B6h | RSPI1 | RSPI command register 3 | SPCMD3 | 16 | 16 | 2, 3 PCLKB | 2 ICLK | |
| 0008 83B8h | RSPI1 | RSPI command register 4 | SPCMD4 | 16 | 16 | 2, 3 PCLKB | 2 ICLK | |

Table 4.1 List of I/O Registers (Address Order) (21/50)

| Address | Module Symbol | Register Name | Register Symbol | Number of Bits | Access Size | Number of Access States | | Related Function |
|------------|---------------|---|-----------------|----------------|-------------|-------------------------|-----------|------------------|
| | | | | | | ICLK>PCLK | ICLK<PCLK | |
| 0008 83BAh | RSPI1 | RSPI command register 5 | SPCMD5 | 16 | 16 | 2, 3 PCLKB | 2 ICLK | RSPI |
| 0008 83BCh | RSPI1 | RSPI command register 6 | SPCMD6 | 16 | 16 | 2, 3 PCLKB | 2 ICLK | |
| 0008 83BEh | RSPI1 | RSPI command register 7 | SPCMD7 | 16 | 16 | 2, 3 PCLKB | 2 ICLK | |
| 0008 83C0h | RSPI2 | RSPI control register | SPCR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 83C1h | RSPI2 | RSPI slave select polarity register | SSLP | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 83C2h | RSPI2 | RSPI pin control register | SPPCR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 83C3h | RSPI2 | RSPI status register | SPSR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 83C4h | RSPI2 | RSPI data register | SPDR | 32 | 16, 32 | 2, 3 PCLKB | 2 ICLK | |
| 0008 83C8h | RSPI2 | RSPI sequence control register | SPSCR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 83C9h | RSPI2 | RSPI sequence status register | SPSSR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 83CAh | RSPI2 | RSPI bit rate register | SPBR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 83CBh | RSPI2 | RSPI data control register | SPDCR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 83CCh | RSPI2 | RSPI clock delay register | SPCKD | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 83CDh | RSPI2 | RSPI slave select negation delay register | SSLND | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 83CEh | RSPI2 | RSPI next-access delay register | SPND | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 83CFh | RSPI2 | RSPI control register 2 | SPCR2 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 83D0h | RSPI2 | RSPI command register 0 | SPCMD0 | 16 | 16 | 2, 3 PCLKB | 2 ICLK | |
| 0008 83D2h | RSPI2 | RSPI command register 1 | SPCMD1 | 16 | 16 | 2, 3 PCLKB | 2 ICLK | |
| 0008 83D4h | RSPI2 | RSPI command register 2 | SPCMD2 | 16 | 16 | 2, 3 PCLKB | 2 ICLK | |
| 0008 83D6h | RSPI2 | RSPI command register 3 | SPCMD3 | 16 | 16 | 2, 3 PCLKB | 2 ICLK | |
| 0008 83D8h | RSPI2 | RSPI command register 4 | SPCMD4 | 16 | 16 | 2, 3 PCLKB | 2 ICLK | |
| 0008 83DAh | RSPI2 | RSPI command register 5 | SPCMD5 | 16 | 16 | 2, 3 PCLKB | 2 ICLK | |
| 0008 83DCh | RSPI2 | RSPI command register 6 | SPCMD6 | 16 | 16 | 2, 3 PCLKB | 2 ICLK | |
| 0008 83DEh | RSPI2 | RSPI command register 7 | SPCMD7 | 16 | 16 | 2, 3 PCLKB | 2 ICLK | |
| 0008 8600h | MTU3 | Timer control register | TCR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | MTU2a |
| 0008 8601h | MTU4 | Timer control register | TCR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 8602h | MTU3 | Timer mode register | TMDR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 8603h | MTU4 | Timer mode register | TMDR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 8604h | MTU3 | Timer I/O control register H | TIORH | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 8605h | MTU3 | Timer I/O control register L | TIORL | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 8606h | MTU4 | Timer I/O control register H | TIORH | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 8607h | MTU4 | Timer I/O control register L | TIORL | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 8608h | MTU3 | Timer interrupt enable register | TIER | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 8609h | MTU4 | Timer interrupt enable register | TIER | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 860Ah | MTU | Timer output master enable register | TOER | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 860Dh | MTU | Timer gate control register | TGCR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 860Eh | MTU | Timer output control register 1 | TOCR1 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 860Fh | MTU | Timer output control register 2 | TOCR2 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 8610h | MTU3 | Timer counter | TCNT | 16 | 16 | 2, 3 PCLKB | 2 ICLK | |
| 0008 8612h | MTU4 | Timer counter | TCNT | 16 | 16 | 2, 3 PCLKB | 2 ICLK | |
| 0008 8614h | MTU | Timer cycle data register | TCDR | 16 | 16 | 2, 3 PCLKB | 2 ICLK | |
| 0008 8616h | MTU | Timer dead time data register | TDDR | 16 | 16 | 2, 3 PCLKB | 2 ICLK | |
| 0008 8618h | MTU3 | Timer general register A | TGRA | 16 | 16 | 2, 3 PCLKB | 2 ICLK | |
| 0008 861Ah | MTU3 | Timer general register B | TGRB | 16 | 16 | 2, 3 PCLKB | 2 ICLK | |
| 0008 861Ch | MTU4 | Timer general register A | TGRA | 16 | 16 | 2, 3 PCLKB | 2 ICLK | |
| 0008 861Eh | MTU4 | Timer general register B | TGRB | 16 | 16 | 2, 3 PCLKB | 2 ICLK | |
| 0008 8620h | MTU | Timer subcounter | TCNTS | 16 | 16 | 2, 3 PCLKB | 2 ICLK | |
| 0008 8622h | MTU | Timer cycle buffer register | TGBR | 16 | 16 | 2, 3 PCLKB | 2 ICLK | |
| 0008 8624h | MTU3 | Timer general register C | TGRC | 16 | 16 | 2, 3 PCLKB | 2 ICLK | |
| 0008 8626h | MTU3 | Timer general register D | TGRD | 16 | 16 | 2, 3 PCLKB | 2 ICLK | |
| 0008 8628h | MTU4 | Timer general register C | TGRC | 16 | 16 | 2, 3 PCLKB | 2 ICLK | |

Table 4.1 List of I/O Registers (Address Order) (22/50)

| Address | Module Symbol | Register Name | Register Symbol | Number of Bits | Access Size | Number of Access States | | Related Function |
|------------|---------------|---|-----------------|----------------|-------------|-------------------------|-----------|------------------|
| | | | | | | ICLK \geq PCLK | ICLK<PCLK | |
| 0008 862Ah | MTU4 | Timer general register D | TGRD | 16 | 16 | 2, 3 PCLKB | 2 ICLK | MTU2a |
| 0008 862Ch | MTU3 | Timer status register | TSR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 862Dh | MTU4 | Timer status register | TSR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 8630h | MTU | Timer interrupt skipping set register | TITCR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 8631h | MTU | Timer interrupt skipping counter | TITCNT | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 8632h | MTU | Timer buffer transfer set register | TBTER | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 8634h | MTU | Timer dead time enable register | TDER | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 8636h | MTU | Timer output level buffer register | TOLBR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 8638h | MTU3 | Timer buffer operation transfer mode register | TBTM | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 8639h | MTU4 | Timer buffer operation transfer mode register | TBTM | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 8640h | MTU4 | Timer A/D converter start request control register | TADCR | 16 | 16 | 2, 3 PCLKB | 2 ICLK | |
| 0008 8644h | MTU4 | Timer A/D converter start request cycle set register A | TADCORA | 16 | 16 | 2, 3 PCLKB | 2 ICLK | |
| 0008 8646h | MTU4 | Timer A/D converter start request cycle set register B | TADCORB | 16 | 16 | 2, 3 PCLKB | 2 ICLK | |
| 0008 8648h | MTU4 | Timer A/D converter start request cycle set buffer register A | TADCOBRA | 16 | 16 | 2, 3 PCLKB | 2 ICLK | |
| 0008 864Ah | MTU4 | Timer A/D converter start request cycle set buffer register B | TADCOBRB | 16 | 16 | 2, 3 PCLKB | 2 ICLK | |
| 0008 8660h | MTU | Timer waveform control register | TWCR | 8 | 8, 16 | 2, 3 PCLKB | 2 ICLK | |
| 0008 8680h | MTU | Timer start register | TSTR | 8 | 8, 16 | 2, 3 PCLKB | 2 ICLK | |
| 0008 8681h | MTU | Timer synchronous register | TSYR | 8 | 8, 16 | 2, 3 PCLKB | 2 ICLK | |
| 0008 8684h | MTU | Timer read/write enable register | TRWER | 8 | 8, 16 | 2, 3 PCLKB | 2 ICLK | |
| 0008 8690h | MTU0 | Noise filter control register | NFCR | 8 | 8, 16 | 2, 3 PCLKB | 2 ICLK | |
| 0008 8691h | MTU1 | Noise filter control register | NFCR | 8 | 8, 16 | 2, 3 PCLKB | 2 ICLK | |
| 0008 8692h | MTU2 | Noise filter control register | NFCR | 8 | 8, 16 | 2, 3 PCLKB | 2 ICLK | |
| 0008 8693h | MTU3 | Noise filter control register | NFCR | 8 | 8, 16 | 2, 3 PCLKB | 2 ICLK | |
| 0008 8694h | MTU4 | Noise filter control register | NFCR | 8 | 8, 16 | 2, 3 PCLKB | 2 ICLK | |
| 0008 8695h | MTU5 | Noise filter control register | NFCR | 8 | 8, 16 | 2, 3 PCLKB | 2 ICLK | |
| 0008 8700h | MTU0 | Timer control register | TCR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 8701h | MTU0 | Timer mode register | TMDR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 8702h | MTU0 | Timer I/O control register H | TIORH | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 8703h | MTU0 | Timer I/O control register L | TIORL | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 8704h | MTU0 | Timer interrupt enable register | TIER | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 8705h | MTU0 | Timer status register | TSR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 8706h | MTU0 | Timer counter | TGNT | 16 | 16 | 2, 3 PCLKB | 2 ICLK | |
| 0008 8708h | MTU0 | Timer general register A | TGRA | 16 | 16 | 2, 3 PCLKB | 2 ICLK | |
| 0008 870Ah | MTU0 | Timer general register B | TGRB | 16 | 16 | 2, 3 PCLKB | 2 ICLK | |
| 0008 870Ch | MTU0 | Timer general register C | TGRC | 16 | 16 | 2, 3 PCLKB | 2 ICLK | |
| 0008 870Eh | MTU0 | Timer general register D | TGRD | 16 | 16 | 2, 3 PCLKB | 2 ICLK | |
| 0008 8720h | MTU0 | Timer general register E | TGRE | 16 | 16 | 2, 3 PCLKB | 2 ICLK | |
| 0008 8722h | MTU0 | Timer general register F | TGRF | 16 | 16 | 2, 3 PCLKB | 2 ICLK | |
| 0008 8724h | MTU0 | Timer interrupt enable register2 | TIER2 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 8726h | MTU0 | Timer buffer operation transfer mode register | TBTM | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 8780h | MTU1 | Timer control register | TCR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 8781h | MTU1 | Timer mode register | TMDR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 8782h | MTU1 | Timer I/O control register | TIOR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 8784h | MTU1 | Timer interrupt enable register | TIER | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 8785h | MTU1 | Timer status register | TSR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 8786h | MTU1 | Timer counter | TCNT | 16 | 16 | 2, 3 PCLKB | 2 ICLK | |
| 0008 8788h | MTU1 | Timer general register A | TGRA | 16 | 16 | 2, 3 PCLKB | 2 ICLK | |
| 0008 878Ah | MTU1 | Timer general register B | TGRB | 16 | 16 | 2, 3 PCLKB | 2 ICLK | |
| 0008 8790h | MTU1 | Timer input capture control register | TICCR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |

Table 4.1 List of I/O Registers (Address Order) (23/50)

| Address | Module Symbol | Register Name | Register Symbol | Number of Bits | Access Size | Number of Access States | | Related Function |
|------------|---------------|---|-----------------|----------------|-------------|-------------------------|-----------|------------------|
| | | | | | | ICLK>PCLK | ICLK<PCLK | |
| 0008 8800h | MTU2 | Timer control register | TCR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | MTU2a |
| 0008 8801h | MTU2 | Timer mode register | TMDR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 8802h | MTU2 | Timer I/O control register | TIOR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 8804h | MTU2 | Timer interrupt enable register | TIER | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 8805h | MTU2 | Timer status register | TSR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 8806h | MTU2 | Timer counter | TCNT | 16 | 16 | 2, 3 PCLKB | 2 ICLK | |
| 0008 8808h | MTU2 | Timer general register A | TGRA | 16 | 16 | 2, 3 PCLKB | 2 ICLK | |
| 0008 880Ah | MTU2 | Timer general register B | TGRB | 16 | 16 | 2, 3 PCLKB | 2 ICLK | |
| 0008 8880h | MTU5 | Timer counter U | TCNTU | 16 | 16 | 2, 3 PCLKB | 2 ICLK | |
| 0008 8882h | MTU5 | Timer general register U | TGRU | 16 | 16 | 2, 3 PCLKB | 2 ICLK | |
| 0008 8884h | MTU5 | Timer control register U | TCRU | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 8886h | MTU5 | Timer I/O control register U | TIORU | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 8890h | MTU5 | Timer counter V | TCNTV | 16 | 16 | 2, 3 PCLKB | 2 ICLK | |
| 0008 8892h | MTU5 | Timer general register V | TGRV | 16 | 16 | 2, 3 PCLKB | 2 ICLK | |
| 0008 8894h | MTU5 | Timer control register V | TCRV | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 8896h | MTU5 | Timer I/O control register V | TIORV | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 88A0h | MTU5 | Timer counter W | TCNTW | 16 | 16 | 2, 3 PCLKB | 2 ICLK | |
| 0008 88A2h | MTU5 | Timer general register W | TGRW | 16 | 16 | 2, 3 PCLKB | 2 ICLK | |
| 0008 88A4h | MTU5 | Timer control register W | TCRW | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 88A6h | MTU5 | Timer I/O control register W | TIORW | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 88B2h | MTU5 | Timer interrupt enable register | TIER | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 88B4h | MTU5 | Timer start register | TSTR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 88B6h | MTU5 | Timer compare match clear register | TCNTCMPCLR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 8900h | POE | Input level control/status register 1 | ICSR1 | 16 | 16 | 2, 3 PCLKB | 2 ICLK | POE2a |
| 0008 8902h | POE | Output level control/status register 1 | OCSR1 | 16 | 16 | 2, 3 PCLKB | 2 ICLK | |
| 0008 8908h | POE | Input level control/status register 2 | ICSR2 | 16 | 16 | 2, 3 PCLKB | 2 ICLK | |
| 0008 890Ah | POE | Software port output enable register | SPOER | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 890Bh | POE | Port output enable control register 1 | POECR1 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 890Ch | POE | Port output enable control register 2 | POECR2 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 890Eh | POE | Input level control/status register 3 | ICSR3 | 16 | 16 | 2, 3 PCLKB | 2 ICLK | |
| 0008 9000h | S12AD | A/D control register | ADCSR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | S12ADa |
| 0008 9004h | S12AD | A/D channel select register 0 | ADANS0 | 16 | 16 | 2, 3 PCLKB | 2 ICLK | |
| 0008 9006h | S12AD | A/D channel select register 1 | ADANS1 | 16 | 16 | 2, 3 PCLKB | 2 ICLK | |
| 0008 9008h | S12AD | A/D-converted value addition mode select register 0 | ADADS0 | 16 | 16 | 2, 3 PCLKB | 2 ICLK | |
| 0008 900Ah | S12AD | A/D-converted value addition mode select register 1 | ADADS1 | 16 | 16 | 2, 3 PCLKB | 2 ICLK | |
| 0008 900Ch | S12AD | A/D-converted value addition count select register | ADADC | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 900Eh | S12AD | A/D control extended register | ADCER | 16 | 16 | 2, 3 PCLKB | 2 ICLK | |
| 0008 9010h | S12AD | A/D start trigger select register | ADSTRGR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 9012h | S12AD | A/D conversion extended input control register | ADEXICR | 16 | 16 | 2, 3 PCLKB | 2 ICLK | |
| 0008 901Ah | S12AD | A/D temperature sensor data register | ADTSR | 16 | 16 | 2, 3 PCLKB | 2 ICLK | |
| 0008 901Ch | S12AD | A/D internal reference voltage data register | ADOCDR | 16 | 16 | 2, 3 PCLKB | 2 ICLK | |
| 0008 9020h | S12AD | A/D data register 0 | ADDR0 | 16 | 16 | 2, 3 PCLKB | 2 ICLK | |
| 0008 9022h | S12AD | A/D data register 1 | ADDR1 | 16 | 16 | 2, 3 PCLKB | 2 ICLK | |
| 0008 9024h | S12AD | A/D data register 2 | ADDR2 | 16 | 16 | 2, 3 PCLKB | 2 ICLK | |
| 0008 9026h | S12AD | A/D data register 3 | ADDR3 | 16 | 16 | 2, 3 PCLKB | 2 ICLK | |
| 0008 9028h | S12AD | A/D data register 4 | ADDR4 | 16 | 16 | 2, 3 PCLKB | 2 ICLK | |
| 0008 902Ah | S12AD | A/D data register 5 | ADDR5 | 16 | 16 | 2, 3 PCLKB | 2 ICLK | |
| 0008 902Ch | S12AD | A/D data register 6 | ADDR6 | 16 | 16 | 2, 3 PCLKB | 2 ICLK | |
| 0008 902Eh | S12AD | A/D data register 7 | ADDR7 | 16 | 16 | 2, 3 PCLKB | 2 ICLK | |
| 0008 9030h | S12AD | A/D data register 8 | ADDR8 | 16 | 16 | 2, 3 PCLKB | 2 ICLK | |
| 0008 9032h | S12AD | A/D data register 9 | ADDR9 | 16 | 16 | 2, 3 PCLKB | 2 ICLK | |

Table 4.1 List of I/O Registers (Address Order) (24/50)

| Address | Module Symbol | Register Name | Register Symbol | Number of Bits | Access Size | Number of Access States | | Related Function | |
|------------|---------------|----------------------------------|-----------------|----------------|-------------|-------------------------|-----------|------------------|-----|
| | | | | | | ICLK>PCLK | ICLK<PCLK | | |
| 0008 9034h | S12AD | A/D data register 10 | ADDR10 | 16 | 16 | 2, 3 PCLKB | 2 ICLK | S12ADa | |
| 0008 9036h | S12AD | A/D data register 11 | ADDR11 | 16 | 16 | 2, 3 PCLKB | 2 ICLK | | |
| 0008 9038h | S12AD | A/D data register 12 | ADDR12 | 16 | 16 | 2, 3 PCLKB | 2 ICLK | | |
| 0008 903Ah | S12AD | A/D data register 13 | ADDR13 | 16 | 16 | 2, 3 PCLKB | 2 ICLK | | |
| 0008 903Ch | S12AD | A/D data register 14 | ADDR14 | 16 | 16 | 2, 3 PCLKB | 2 ICLK | | |
| 0008 903Eh | S12AD | A/D data register 15 | ADDR15 | 16 | 16 | 2, 3 PCLKB | 2 ICLK | | |
| 0008 9040h | S12AD | A/D data register 16 | ADDR16 | 16 | 16 | 2, 3 PCLKB | 2 ICLK | | |
| 0008 9042h | S12AD | A/D data register 17 | ADDR17 | 16 | 16 | 2, 3 PCLKB | 2 ICLK | | |
| 0008 9044h | S12AD | A/D data register 18 | ADDR18 | 16 | 16 | 2, 3 PCLKB | 2 ICLK | | |
| 0008 9046h | S12AD | A/D data register 19 | ADDR19 | 16 | 16 | 2, 3 PCLKB | 2 ICLK | | |
| 0008 9048h | S12AD | A/D data register 20 | ADDR20 | 16 | 16 | 2, 3 PCLKB | 2 ICLK | | |
| 0008 9060h | S12AD | A/D sampling state register01 | ADSSTR01 | 16 | 16 | 2, 3 PCLKB | 2 ICLK | | |
| 0008 9070h | S12AD | A/D sampling state register 23 | ADSSTR23 | 16 | 16 | 2, 3 PCLKB | 2 ICLK | | |
| 0008 9800h | AD | A/D data register A | ADDRA | 16 | 16 | 2, 3 PCLKB | 2 ICLK | | ADb |
| 0008 9802h | AD | A/D data register B | ADDRB | 16 | 16 | 2, 3 PCLKB | 2 ICLK | | |
| 0008 9804h | AD | A/D data register C | ADDRC | 16 | 16 | 2, 3 PCLKB | 2 ICLK | | |
| 0008 9806h | AD | A/D data register D | ADDRD | 16 | 16 | 2, 3 PCLKB | 2 ICLK | | |
| 0008 9808h | AD | A/D data register E | ADDRE | 16 | 16 | 2, 3 PCLKB | 2 ICLK | | |
| 0008 980Ah | AD | A/D data register F | ADDRF | 16 | 16 | 2, 3 PCLKB | 2 ICLK | | |
| 0008 980Ch | AD | A/D data register G | ADDRG | 16 | 16 | 2, 3 PCLKB | 2 ICLK | | |
| 0008 980Eh | AD | A/D data register H | ADDRH | 16 | 16 | 2, 3 PCLKB | 2 ICLK | | |
| 0008 9810h | AD | A/D control/status register | ADCSR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | | |
| 0008 9811h | AD | A/D control register | ADCR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | | |
| 0008 9812h | AD | A/D control register 2 | ADCR2 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | | |
| 0008 9813h | AD | A/D sampling state register | ADSSTR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | | |
| 0008 981Fh | AD | A/D self-diagnostic register | ADDIAGR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | | |
| 0008 A000h | SCI0 | Serial mode register | SMR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | SC1c, SC1d | |
| 0008 A001h | SCI0 | Bit rate register | BRR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | | |
| 0008 A002h | SCI0 | Serial control register | SCR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | | |
| 0008 A003h | SCI0 | Transmit data register | TDR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | | |
| 0008 A004h | SCI0 | Serial status register | SSR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | | |
| 0008 A005h | SCI0 | Receive data register | RDR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | | |
| 0008 A006h | SCI0 | Smart card mode register | SCMR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | | |
| 0008 A007h | SCI0 | Serial extended mode register | SEMR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | | |
| 0008 A008h | SCI0 | Noise filter setting register | SNFR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | | |
| 0008 A009h | SCI0 | I ² C mode register 1 | SIMR1 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | | |
| 0008 A00Ah | SCI0 | I ² C mode register 2 | SIMR2 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | | |
| 0008 A00Bh | SCI0 | I ² C mode register 3 | SIMR3 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | | |
| 0008 A00Ch | SCI0 | I ² C status register | SISR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | | |
| 0008 A00Dh | SCI0 | SPI mode register | SPMR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | | |
| 0008 A020h | SCI1 | Serial mode register | SMR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | | |
| 0008 A021h | SCI1 | Bit rate register | BRR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | | |
| 0008 A022h | SCI1 | Serial control register | SCR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | | |
| 0008 A023h | SCI1 | Transmit data register | TDR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | | |
| 0008 A024h | SCI1 | Serial status register | SSR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | | |
| 0008 A025h | SCI1 | Receive data register | RDR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | | |
| 0008 A026h | SCI1 | Smart card mode register | SCMR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | | |
| 0008 A027h | SCI1 | Serial extended mode register | SEMR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | | |
| 0008 A028h | SCI1 | Noise filter setting register | SNFR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | | |
| 0008 A029h | SCI1 | I ² C mode register 1 | SIMR1 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | | |
| 0008 A02Ah | SCI1 | I ² C mode register 2 | SIMR2 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | | |

Table 4.1 List of I/O Registers (Address Order) (25/50)

| Address | Module Symbol | Register Name | Register Symbol | Number of Bits | Access Size | Number of Access States | | Related Function |
|------------|---------------|----------------------------------|-----------------|----------------|-------------|-------------------------|-----------|------------------|
| | | | | | | ICLK>PCLK | ICLK<PCLK | |
| 0008 A02Bh | SCI1 | I ² C mode register 3 | SIMR3 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | SCIc, SCId |
| 0008 A02Ch | SCI1 | I ² C status register | SISR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 A02Dh | SCI1 | SPI mode register | SPMR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 A040h | SCI2 | Serial mode register | SMR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 A041h | SCI2 | Bit rate register | BRR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 A042h | SCI2 | Serial control register | SCR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 A043h | SCI2 | Transmit data register | TDR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 A044h | SCI2 | Serial status register | SSR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 A045h | SCI2 | Receive data register | RDR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 A046h | SCI2 | Smart card mode register | SCMR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 A047h | SCI2 | Serial extended mode register | SEM | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 A048h | SCI2 | Noise filter setting register | SNFR2 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 A049h | SCI2 | I ² C mode register 1 | SIMR1 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 A04Ah | SCI2 | I ² C mode register 2 | SIMR2 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 A04Bh | SCI2 | I ² C mode register 3 | SIMR3 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 A04Ch | SCI2 | I ² C status register | SISR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 A04Dh | SCI2 | SPI mode register | SPMR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 A060h | SCI3 | Serial mode register | SMR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 A061h | SCI3 | Bit rate register | BRR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 A062h | SCI3 | Serial control register | SCR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 A063h | SCI3 | Transmit data register | TDR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 A064h | SCI3 | Serial status register | SSR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 A065h | SCI3 | Receive data register | RDR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 A066h | SCI3 | Smart card mode register | SCMR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 A067h | SCI3 | Serial extended mode register | SEMR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 A068h | SCI3 | Noise filter setting register | SNFR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 A069h | SCI3 | I ² C mode register 1 | SIMR1 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 A06Ah | SCI3 | I ² C mode register 2 | SIMR2 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 A06Bh | SCI3 | I ² C mode register 3 | SIMR3 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 A06Ch | SCI3 | I ² C status register | SISR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 A06Dh | SCI3 | SPI mode register | SPMR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 A080h | SCI4 | Serial mode register | SMR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 A081h | SCI4 | Bit rate register | BRR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 A082h | SCI4 | Serial control register | SCR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 A083h | SCI4 | Transmit data register | TDR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 A084h | SCI4 | Serial status register | SSR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 A085h | SCI4 | Receive data register | RDR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 A086h | SCI4 | Smart card mode register | SCMR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 A087h | SCI4 | Serial extended mode register | SEMR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 A088h | SCI4 | Noise filter setting register | SNFR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 A089h | SCI4 | I ² C mode register 1 | SIMR1 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 A08Ah | SCI4 | I ² C mode register 2 | SIMR2 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 A08Bh | SCI4 | I ² C mode register 3 | SIMR3 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 A08Ch | SCI4 | I ² C status register | SISR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 A08Dh | SCI4 | SPI mode register | SPMR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 A0A0h | SCI5 | Serial mode register | SMR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 A0A1h | SCI5 | Bit rate register | BRR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 A0A2h | SCI5 | Serial control register | SCR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 A0A3h | SCI5 | Transmit data register | TDR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 A0A4h | SCI5 | Serial status register | SSR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 A0A5h | SCI5 | Receive data register | RDR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |

Table 4.1 List of I/O Registers (Address Order) (26/50)

| Address | Module Symbol | Register Name | Register Symbol | Number of Bits | Access Size | Number of Access States | | Related Function |
|------------|---------------|----------------------------------|-----------------|----------------|-------------|-------------------------|-----------|------------------|
| | | | | | | ICLK>PCLK | ICLK<PCLK | |
| 0008 A0A6h | SCI5 | Smart card mode register | SCMR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | SCIC, SCId |
| 0008 A0A7h | SCI5 | Serial extended mode register | SEMR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 A0A8h | SCI5 | Noise filter setting register | SNFR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 A0A9h | SCI5 | I ² C mode register 1 | SIMR1 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 A0AAh | SCI5 | I ² C mode register 2 | SIMR2 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 A0ABh | SCI5 | I ² C mode register 3 | SIMR3 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 A0ACh | SCI5 | I ² C status register | SISR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 A0ADh | SCI5 | SPI mode register | SPMR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 A0C0h | SCI6 | Serial mode register | SMR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 A0C1h | SCI6 | Bit rate register | BRR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 A0C2h | SCI6 | Serial control register | SCR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 A0C3h | SCI6 | Transmit data register | TDR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 A0C4h | SCI6 | Serial status register | SSR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 A0C5h | SCI6 | Receive data register | RDR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 A0C6h | SCI6 | Smart card mode register | SCMR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 A0C7h | SCI6 | Serial extended mode register | SEMR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 A0C8h | SCI6 | Noise filter setting register | SNFR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 A0C9h | SCI6 | I ² C mode register 1 | SIMR1 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 A0CAh | SCI6 | I ² C mode register 2 | SIMR2 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 A0CBh | SCI6 | I ² C mode register 3 | SIMR3 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 A0CCh | SCI6 | I ² C status register | SISR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 A0CDh | SCI6 | SPI mode register | SPMR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 A0E0h | SCI7 | Serial mode register | SMR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 A0E1h | SCI7 | Bit rate register | BRR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 A0E2h | SCI7 | Serial control register | SCR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 A0E3h | SCI7 | Transmit data register | TDR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 A0E4h | SCI7 | Serial status register | SSR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 A0E5h | SCI7 | Receive data register | RDR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 A0E6h | SCI7 | Smart card mode register | SCMR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 A0E7h | SCI7 | Serial extended mode register | SEMR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 A0E8h | SCI7 | Noise filter setting register | SNFR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 A0E9h | SCI7 | I ² C mode register 1 | SIMR1 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 A0EAh | SCI7 | I ² C mode register 2 | SIMR2 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 A0EBh | SCI7 | I ² C mode register 3 | SIMR3 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 A0ECh | SCI7 | I ² C status register | SISR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 A0EDh | SCI7 | SPI mode register | SPMR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 A100h | SCI8 | Serial mode register | SMR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 A101h | SCI8 | Bit rate register | BRR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 A102h | SCI8 | Serial control register | SCR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 A103h | SCI8 | Transmit data register | TDR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 A104h | SCI8 | Serial status register | SSR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 A105h | SCI8 | Receive data register | RDR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 A106h | SCI8 | Smart card mode register | SCMR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 A107h | SCI8 | Serial extended mode register | SEMR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 A108h | SCI8 | Noise filter setting register | SNFR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 A109h | SCI8 | I ² C mode register 1 | SIMR1 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 A10Ah | SCI8 | I ² C mode register 2 | SIMR2 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 A10Bh | SCI8 | I ² C mode register 3 | SIMR3 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 A10Ch | SCI8 | I ² C status register | SISR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 A10Dh | SCI8 | SPI mode register | SPMR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 A120h | SCI9 | Serial mode register | SMR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |

Table 4.1 List of I/O Registers (Address Order) (27/50)

| Address | Module Symbol | Register Name | Register Symbol | Number of Bits | Access Size | Number of Access States | | Related Function |
|------------|---------------|--|-----------------|----------------|-------------|-------------------------|-----------|------------------|
| | | | | | | ICLK \geq PCLK | ICLK<PCLK | |
| 0008 A121h | SCI9 | Bit rate register | BRR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | SClC, SClD |
| 0008 A122h | SCI9 | Serial control register | SCR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 A123h | SCI9 | Transmit data register | TDR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 A124h | SCI9 | Serial status register | SSR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 A125h | SCI9 | Receive data register | RDR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 A126h | SCI9 | Smart card mode register | SCMR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 A127h | SCI9 | Serial extended mode register | SEMR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 A128h | SCI9 | Noise filter setting register | SNFR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 A129h | SCI9 | I ² C mode register 1 | SIMR1 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 A12Ah | SCI9 | I ² C mode register 2 | SIMR2 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 A12Bh | SCI9 | I ² C mode register 3 | SIMR3 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 A12Ch | SCI9 | I ² C status register | SISR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 A12Dh | SCI9 | SPI mode register | SPMR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 A140h | SCI10 | Serial mode register | SMR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 A141h | SCI10 | Bit rate register | BRR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 A142h | SCI10 | Serial control register | SCR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 A143h | SCI10 | Transmit data register | TDR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 A144h | SCI10 | Serial status register | SSR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 A145h | SCI10 | Receive data register | RDR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 A146h | SCI10 | Smart card mode register | SCMR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 A147h | SCI10 | Serial extended mode register | SEMR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 A148h | SCI10 | Noise filter setting register | SNFR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 A149h | SCI10 | I ² C mode register 1 | SIMR1 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 A14Ah | SCI10 | I ² C mode register 2 | SIMR2 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 A14Bh | SCI10 | I ² C mode register 3 | SIMR3 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 A14Ch | SCI10 | I ² C status register | SISR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 A14Dh | SCI10 | SPI mode register | SPMR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 A160h | SCI11 | Serial mode register | SMR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 A161h | SCI11 | Bit rate register | BRR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 A162h | SCI11 | Serial control register | SCR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 A163h | SCI11 | Transmit data register | TDR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 A164h | SCI11 | Serial status register | SSR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 A165h | SCI11 | Receive data register | RDR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 A166h | SCI11 | Smart card mode register | SCMR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 A167h | SCI11 | Serial extended mode register | SEMR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 A168h | SCI11 | Noise filter setting register | SNFR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 A169h | SCI11 | I ² C mode register 1 | SIMR1 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 A16Ah | SCI11 | I ² C mode register 2 | SIMR2 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 A16Bh | SCI11 | I ² C mode register 3 | SIMR3 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 A16Ch | SCI11 | I ² C status register | SISR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 A16Dh | SCI11 | SPI mode register | SPMR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 A800h | IEB | IEBus control register | IECTR | 8 | 8 | 3 to 4 PCLKB | 2, 3 ICLK | IEB |
| 0008 A801h | IEB | IEBus command register | IECMR | 8 | 8 | 3 to 4 PCLKB | 2, 3 ICLK | |
| 0008 A802h | IEB | IEBus master control register | IEMCR | 8 | 8 | 3 to 4 PCLKB | 2, 3 ICLK | |
| 0008 A803h | IEB | IEBus master unit address register 1 | IEAR1 | 8 | 8 | 3 to 4 PCLKB | 2, 3 ICLK | |
| 0008 A804h | IEB | IEBus master unit address register 2 | IEAR2 | 8 | 8 | 3 to 4 PCLKB | 2, 3 ICLK | |
| 0008 A805h | IEB | IEBus slave address setting register 1 | IESA1 | 8 | 8 | 3 to 4 PCLKB | 2, 3 ICLK | |

Table 4.1 List of I/O Registers (Address Order) (28/50)

| Address | Module Symbol | Register Name | Register Symbol | Number of Bits | Access Size | Number of Access States | | Related Function | |
|--------------------------|---------------|--|-----------------|----------------|-------------|-------------------------|-----------|------------------|------------|
| | | | | | | ICLK≥PCLK | ICLK<PCLK | | |
| 0008 A806h | IEB | IEBus slave address setting register 2 | IESA2 | 8 | 8 | 3 to 4 PCLKB | 2, 3 ICLK | IEB | |
| 0008 A807h | IEB | IEBus transmit message length register | IETBFL | 8 | 8 | 3 to 4 PCLKB | 2, 3 ICLK | | |
| 0008 A809h | IEB | IEBus reception master address register 1 | IEMA1 | 8 | 8 | 3 to 4 PCLKB | 2, 3 ICLK | | |
| 0008 A80Ah | IEB | IEBus reception master address register 2 | IEMA2 | 8 | 8 | 3 to 4 PCLKB | 2, 3 ICLK | | |
| 0008 A80Bh | IEB | IEBus receive control field register | IERCTL | 8 | 8 | 3 to 4 PCLKB | 2, 3 ICLK | | |
| 0008 A80Ch | IEB | IEBus receive message length register | IERBFL | 8 | 8 | 3 to 4 PCLKB | 2, 3 ICLK | | |
| 0008 A80Eh | IEB | IEBus lock address register 1 | IELA1 | 8 | 8 | 3 to 4 PCLKB | 2, 3 ICLK | | |
| 0008 A80Fh | IEB | IEBus lock address register 2 | IELA2 | 8 | 8 | 3 to 4 PCLKB | 2, 3 ICLK | | |
| 0008 A810h | IEB | IEBus general flag register | IEFLG | 8 | 8 | 3 to 4 PCLKB | 2, 3 ICLK | | |
| 0008 A811h | IEB | IEBus transmit status register | IETSR | 8 | 8 | 3 to 4 PCLKB | 2, 3 ICLK | | |
| 0008 A812h | IEB | IEBus transmit interrupt enable register | IEIET | 8 | 8 | 3 to 4 PCLKB | 2, 3 ICLK | | |
| 0008 A814h | IEB | IEBus receive status register | IERSR | 8 | 8 | 3 to 4 PCLKB | 2, 3 ICLK | | |
| 0008 A815h | IEB | IEBus receive interrupt enable register | IEIER | 8 | 8 | 3 to 4 PCLKB | 2, 3 ICLK | | |
| 0008 A818h | IEB | IEBus clock select register | IECKSR | 8 | 8 | 3 to 4 PCLKB | 2, 3 ICLK | | |
| 0008 A900h to 0008 A91Fh | IEB | IEBus transmit data buffer register 001 to 032 | IETB001 to 032 | 8 | 8 | 3 to 4 PCLKB | 2, 3 ICLK | | |
| 0008 AA00h to 0008 AA1Fh | IEB | IEBus receive data buffer register 001 to 032 | IERB001 to 032 | 8 | 8 | 3 to 4 PCLKB | 2, 3 ICLK | | |
| 0008 B300h | SCI12 | Serial mode register | SMR12 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | | SClC, SCId |
| 0008 B301h | SCI12 | Bit rate register | BRR12 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | | |
| 0008 B302h | SCI12 | Serial control register | SCR12 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | | |
| 0008 B303h | SCI12 | Transmit data register | TDR12 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | | |
| 0008 B304h | SCI12 | Serial status register | SSR12 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | | |
| 0008 B305h | SCI12 | Receive data register | RDR12 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | | |
| 0008 B306h | SCI12 | Smart card mode register | SCMR12 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | | |
| 0008 B307h | SCI12 | Serial extended mode register | SEMR12 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | | |
| 0008 B308h | SCI12 | Noise filter setting register | SNFR12 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | | |
| 0008 B309h | SCI12 | I ² C mode register 1 | SIMR112 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | | |
| 0008 B30Ah | SCI12 | I ² C mode register 2 | SIMR212 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | | |
| 0008 B30Bh | SCI12 | I ² C mode register 3 | SIMR312 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | | |
| 0008 B30Ch | SCI12 | I ² C status register | SISR12 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | | |
| 0008 B30Dh | SCI12 | SPI mode register | SPMR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | | |
| 0008 B320h | SCI12 | Extended serial module enable register | ESMER | 8 | 8 | 2, 3 PCLKB | 2 ICLK | | |
| 0008 B321h | SCI12 | Control register 0 | CR0 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | | |
| 0008 B322h | SCI12 | Control register 1 | CR1 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | | |
| 0008 B323h | SCI12 | Control register 2 | CR2 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | | |
| 0008 B324h | SCI12 | Control register 3 | CR3 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | | |
| 0008 B325h | SCI12 | Port control register | PCR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | | |
| 0008 B326h | SCI12 | Interrupt control register | ICR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | | |
| 0008 B327h | SCI12 | Status register | STR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | | |
| 0008 B328h | SCI12 | Status clear register | STCR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | | |
| 0008 B329h | SCI12 | Control field 0 data register | CF0DR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | | |
| 0008 B32Ah | SCI12 | Control field 0 compare enable register | CF0CR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | | |
| 0008 B32Bh | SCI12 | Control field 0 receive data register | CF0RR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | SClC, SCId | |
| 0008 B32Ch | SCI12 | Primary control field 1 data register | PCF1DR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | | |
| 0008 B32Dh | SCI12 | Secondary control field 1 data register | SCF1DR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | | |
| 0008 B32Eh | SCI12 | Control field 1 compare enable register | CF1CR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | | |
| 0008 B32Fh | SCI12 | Control field 1 receive data register | CF1RR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | | |
| 0008 B330h | SCI12 | Timer control register | TCR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | | |
| 0008 B331h | SCI12 | Timer mode register | TMR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | | |
| 0008 B332h | SCI12 | Timer prescaler register | TPRE | 8 | 8 | 2, 3 PCLKB | 2 ICLK | | |
| 0008 B333h | SCI12 | Timer count register | TCNT | 8 | 8 | 2, 3 PCLKB | 2 ICLK | | |

Table 4.1 List of I/O Registers (Address Order) (29/50)

| Address | Module Symbol | Register Name | Register Symbol | Number of Bits | Access Size | Number of Access States | | Related Function |
|------------|---------------|---------------------------|-----------------|----------------|-------------|-------------------------|---------------|------------------|
| | | | | | | ICLK \geq PCLK | ICLK $<$ PCLK | |
| 0008 C000h | PORT0 | Port direction register | PDR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | I/O Ports |
| 0008 C001h | PORT1 | Port direction register | PDR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 C002h | PORT2 | Port direction register | PDR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 C003h | PORT3 | Port direction register | PDR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 C004h | PORT4 | Port direction register | PDR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 C005h | PORT5 | Port direction register | PDR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 C006h | PORT6 | Port direction register | PDR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 C007h | PORT7 | Port direction register | PDR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 C008h | PORT8 | Port direction register | PDR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 C009h | PORT9 | Port direction register | PDR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 C00Ah | PORTA | Port direction register | PDR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 C00Bh | PORTB | Port direction register | PDR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 C00Ch | PORTC | Port direction register | PDR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 C00Dh | PORTD | Port direction register | PDR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 C00Eh | PORTE | Port direction register | PDR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 C00Fh | PORTF | Port direction register | PDR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 C010h | PORTG | Port direction register | PDR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 C012h | PORTJ | Port direction register | PDR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 C020h | PORT0 | Port output data register | PODR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 C021h | PORT1 | Port output data register | PODR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 C022h | PORT2 | Port output data register | PODR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 C023h | PORT3 | Port output data register | PODR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 C024h | PORT4 | Port output data register | PODR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 C025h | PORT5 | Port output data register | PODR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 C026h | PORT6 | Port output data register | PODR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 C027h | PORT7 | Port output data register | PODR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 C028h | PORT8 | Port output data register | PODR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 C029h | PORT9 | Port output data register | PODR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 C02Ah | PORTA | Port output data register | PODR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 C02Bh | PORTB | Port output data register | PODR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 C02Ch | PORTC | Port output data register | PODR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 C02Dh | PORTD | Port output data register | PODR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 C02Eh | PORTE | Port output data register | PODR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 C02Fh | PORTF | Port output data register | PODR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 C030h | PORTG | Port output data register | PODR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 C032h | PORTJ | Port output data register | PODR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 C040h | PORT0 | Port input data register | PIDR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 C041h | PORT1 | Port input data register | PIDR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 C042h | PORT2 | Port input data register | PIDR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 C043h | PORT3 | Port input data register | PIDR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 C044h | PORT4 | Port input data register | PIDR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 C045h | PORT5 | Port input data register | PIDR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |

Table 4.1 List of I/O Registers (Address Order) (30/50)

| Address | Module Symbol | Register Name | Register Symbol | Number of Bits | Access Size | Number of Access States | | Related Function |
|------------|---------------|-------------------------------|-----------------|----------------|-------------|-------------------------|-----------|------------------|
| | | | | | | ICLK≥PCLK | ICLK<PCLK | |
| 0008 C046h | PORT6 | Port input data register | PIDR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | I/O Ports |
| 0008 C047h | PORT7 | Port input data register | PIDR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 C048h | PORT8 | Port input data register | PIDR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 C049h | PORT9 | Port input data register | PIDR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 C04Ah | PORTA | Port input data register | PIDR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 C04Bh | PORTB | Port input data register | PIDR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 C04Ch | PORTC | Port input data register | PIDR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 C04Dh | PORTD | Port input data register | PIDR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 C04Eh | PORTE | Port input data register | PIDR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 C04Fh | PORTF | Port input data register | PIDR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 C050h | PORTG | Port input data register | PIDR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 C052h | PORTJ | Port input data register | PIDR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 C060h | PORT0 | Port input data register | PMR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 C061h | PORT1 | Port input data register | PMR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 C062h | PORT2 | Port mode register | PMR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 C063h | PORT3 | Port mode register | PMR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 C064h | PORT4 | Port mode register | PMR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 C065h | PORT5 | Port mode register | PMR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 C066h | PORT6 | Port mode register | PMR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 C067h | PORT7 | Port mode register | PMR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 C068h | PORT8 | Port mode register | PMR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 C069h | PORT9 | Port mode register | PMR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 C06Ah | PORTA | Port mode register | PMR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 C06Bh | PORTB | Port mode register | PMR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 C06Ch | PORTC | Port mode register | PMR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 C06Dh | PORTD | Port mode register | PMR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 C06Eh | PORTE | Port mode register | PMR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 C06Fh | PORTF | Port mode register | PMR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 C070h | PORTG | Port mode register | PMR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 C072h | PORTJ | Port mode register | PMR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 C080h | PORT0 | Open drain control register 0 | ODR0 | 8 | 8, 16 | 2, 3 PCLKB | 2 ICLK | |
| 0008 C081h | PORT0 | Open drain control register 1 | ODR1 | 8 | 8, 16 | 2, 3 PCLKB | 2 ICLK | |
| 0008 C082h | PORT1 | Open drain control register 0 | ODR0 | 8 | 8, 16 | 2, 3 PCLKB | 2 ICLK | |
| 0008 C083h | PORT1 | Open drain control register 1 | ODR1 | 8 | 8, 16 | 2, 3 PCLKB | 2 ICLK | |
| 0008 C084h | PORT2 | Open drain control register 0 | ODR0 | 8 | 8, 16 | 2, 3 PCLKB | 2 ICLK | |
| 0008 C085h | PORT2 | Open drain control register 1 | ODR1 | 8 | 8, 16 | 2, 3 PCLKB | 2 ICLK | |
| 0008 C086h | PORT3 | Open drain control register 0 | ODR0 | 8 | 8, 16 | 2, 3 PCLKB | 2 ICLK | |
| 0008 C087h | PORT3 | Open drain control register 1 | ODR1 | 8 | 8, 16 | 2, 3 PCLKB | 2 ICLK | |
| 0008 C088h | PORT4 | Open drain control register 0 | ODR0 | 8 | 8, 16 | 2, 3 PCLKB | 2 ICLK | |
| 0008 C089h | PORT4 | Open drain control register 1 | ODR1 | 8 | 8, 16 | 2, 3 PCLKB | 2 ICLK | |
| 0008 C08Ah | PORT5 | Open drain control register 0 | ODR0 | 8 | 8, 16 | 2, 3 PCLKB | 2 ICLK | |
| 0008 C08Bh | PORT5 | Open drain control register 1 | ODR1 | 8 | 8, 16 | 2, 3 PCLKB | 2 ICLK | |
| 0008 C08Ch | PORT6 | Open drain control register 0 | ODR0 | 8 | 8, 16 | 2, 3 PCLKB | 2 ICLK | |
| 0008 C08Dh | PORT6 | Open drain control register 1 | ODR1 | 8 | 8, 16 | 2, 3 PCLKB | 2 ICLK | |
| 0008 C08Eh | PORT7 | Open drain control register 0 | ODR0 | 8 | 8, 16 | 2, 3 PCLKB | 2 ICLK | |
| 0008 C08Fh | PORT7 | Open drain control register 1 | ODR1 | 8 | 8, 16 | 2, 3 PCLKB | 2 ICLK | |
| 0008 C090h | PORT8 | Open drain control register 0 | ODR0 | 8 | 8, 16 | 2, 3 PCLKB | 2 ICLK | |
| 0008 C091h | PORT8 | Open drain control register 1 | ODR1 | 8 | 8, 16 | 2, 3 PCLKB | 2 ICLK | |
| 0008 C092h | PORT9 | Open drain control register 0 | ODR0 | 8 | 8, 16 | 2, 3 PCLKB | 2 ICLK | |
| 0008 C093h | PORT9 | Open drain control register 1 | ODR1 | 8 | 8, 16 | 2, 3 PCLKB | 2 ICLK | |
| 0008 C094h | PORTA | Open drain control register 0 | ODR0 | 8 | 8, 16 | 2, 3 PCLKB | 2 ICLK | |

Table 4.1 List of I/O Registers (Address Order) (31/50)

| Address | Module Symbol | Register Name | Register Symbol | Number of Bits | Access Size | Number of Access States | | Related Function |
|------------|---------------|----------------------------------|-----------------|----------------|-------------|-------------------------|-----------|------------------|
| | | | | | | ICLK>PCLK | ICLK<PCLK | |
| 0008 C095h | PORTA | Open drain control register 1 | ODR1 | 8 | 8, 16 | 2, 3 PCLKB | 2 ICLK | I/O Ports |
| 0008 C096h | PORTB | Open drain control register 0 | ODR0 | 8 | 8, 16 | 2, 3 PCLKB | 2 ICLK | |
| 0008 C097h | PORTB | Open drain control register 1 | ODR1 | 8 | 8, 16 | 2, 3 PCLKB | 2 ICLK | |
| 0008 C098h | PORTC | Open drain control register 0 | ODR0 | 8 | 8, 16 | 2, 3 PCLKB | 2 ICLK | |
| 0008 C099h | PORTC | Open drain control register 1 | ODR1 | 8 | 8, 16 | 2, 3 PCLKB | 2 ICLK | |
| 0008 C09Ah | PORTD | Open drain control register 0 | ODR0 | 8 | 8, 16 | 2, 3 PCLKB | 2 ICLK | |
| 0008 C09Bh | PORTD | Open drain control register 1 | ODR1 | 8 | 8, 16 | 2, 3 PCLKB | 2 ICLK | |
| 0008 C09Ch | PORTE | Open drain control register 0 | ODR0 | 8 | 8, 16 | 2, 3 PCLKB | 2 ICLK | |
| 0008 C09Dh | PORTE | Open drain control register 1 | ODR1 | 8 | 8, 16 | 2, 3 PCLKB | 2 ICLK | |
| 0008 C09Eh | PORTF | Open drain control register 0 | ODR0 | 8 | 8, 16 | 2, 3 PCLKB | 2 ICLK | |
| 0008 C09Fh | PORTF | Open drain control register 1 | ODR1 | 8 | 8, 16 | 2, 3 PCLKB | 2 ICLK | |
| 0008 C0A0h | PORTG | Open drain control register 0 | ODR0 | 8 | 8, 16 | 2, 3 PCLKB | 2 ICLK | |
| 0008 C0A1h | PORTG | Open drain control register 1 | ODR1 | 8 | 8, 16 | 2, 3 PCLKB | 2 ICLK | |
| 0008 C0A4h | PORTJ | Open drain control register 0 | ODR0 | 8 | 8, 16 | 2, 3 PCLKB | 2 ICLK | |
| 0008 C0A5h | PORTJ | Open drain control register 1 | ODR1 | 8 | 8, 16 | 2, 3 PCLKB | 2 ICLK | |
| 0008 C0C0h | PORT0 | Pull-up control register | PCR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 C0C1h | PORT1 | Pull-up control register | PCR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 C0C2h | PORT2 | Pull-up control register | PCR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 C0C3h | PORT3 | Pull-up control register | PCR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 C0C4h | PORT4 | Pull-up control register | PCR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 C0C5h | PORT5 | Pull-up control register | PCR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 C0C6h | PORT6 | Pull-up control register | PCR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 C0C7h | PORT7 | Pull-up control register | PCR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 C0C8h | PORT8 | Pull-up control register | PCR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 C0C9h | PORT9 | Pull-up control register | PCR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 C0CAh | PORTA | Pull-up control register | PCR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 C0CBh | PORTB | Pull-up control register | PCR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 C0CCh | PORTC | Pull-up control register | PCR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 C0CDh | PORTD | Pull-up control register | PCR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 C0CEh | PORTE | Pull-up control register | PCR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 C0CFh | PORTF | Pull-up control register | PCR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 C0D0h | PORTG | Pull-up control register | PCR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 C0D2h | PORTJ | Pull-up control register | PCR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 C0E0h | PORT0 | Drive ability control register | DSCR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 C0E2h | PORT2 | Drive ability control register | DSCR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 C0E5h | PORT5 | Drive ability control register | DSCR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 C0E9h | PORT9 | Drive ability control register | DSCR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 C0EAh | PORTA | Drive ability control register | DSCR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 C0EBh | PORTB | Drive ability control register | DSCR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 C0ECh | PORTC | Drive ability control register | DSCR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 C0EDh | PORTD | Drive ability control register | DSCR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 C0EEh | PORTE | Drive ability control register | DSCR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 C0F0h | PORTG | Drive ability control register | DSCR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 C100h | MPC | CS output enable register | PFCSE | 8 | 8 | 2, 3 PCLKB | 2 ICLK | MPC |
| 0008 C102h | MPC | CS output pin select register 0 | PFCSS0 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 C103h | MPC | CS output pin select register 1 | PFCSS1 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 C104h | MPC | Address output enable register 0 | PFAOE0 | 8 | 8, 16 | 2, 3 PCLKB | 2 ICLK | |
| 0008 C105h | MPC | Address output enable register 1 | PFAOE1 | 8 | 8, 16 | 2, 3 PCLKB | 2 ICLK | |
| 0008 C106h | MPC | External bus control register 0 | PFBCR0 | 8 | 8, 16 | 2, 3 PCLKB | 2 ICLK | |
| 0008 C107h | MPC | External bus control register 1 | PFBCR1 | 8 | 8, 16 | 2, 3 PCLKB | 2 ICLK | |
| 0008 C10Eh | MPC | Ethernet control register 1 | PFENET | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |

Table 4.1 List of I/O Registers (Address Order) (32/50)

| Address | Module Symbol | Register Name | Register Symbol | Number of Bits | Access Size | Number of Access States | | Related Function |
|------------|---------------|-----------------------------------|-----------------|----------------|-------------|-------------------------|-----------|------------------|
| | | | | | | ICLK≥PCLK | ICLK<PCLK | |
| 0008 C114h | MPC | USB0 control register | PFUSB0 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | MPC |
| 0008 C115h | MPC | USB1 control register | PFUSB1 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 C11Fh | MPC | Write-protect register | PWPR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 C120h | PORT | Port switching register B | PSRB | 8 | 8 | 2, 3 PCLKB | 2 ICLK | I/O Ports |
| 0008 C121h | PORT | Port switching register A | PSRA | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 C140h | MPC | P00 pin function control register | P00PFS | 8 | 8 | 2, 3 PCLKB | 2 ICLK | MPC |
| 0008 C141h | MPC | P01 pin function control register | P01PFS | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 C142h | MPC | P02 pin function control register | P02PFS | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 C143h | MPC | P03 pin function control register | P03PFS | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 C145h | MPC | P05 pin function control register | P05PFS | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 C147h | MPC | P07 pin function control register | P07PFS | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 C148h | MPC | P10 pin function control register | P10PFS | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 C149h | MPC | P11 pin function control register | P11PFS | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 C14Ah | MPC | P12 pin function control register | P12PFS | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 C14Bh | MPC | P13 pin function control register | P13PFS | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 C14Ch | MPC | P14 pin function control register | P14PFS | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 C14Dh | MPC | P15 pin function control register | P15PFS | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 C14Eh | MPC | P16 pin function control register | P16PFS | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 C14Fh | MPC | P17 pin function control register | P17PFS | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 C150h | MPC | P20 pin function control register | P20PFS | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 C151h | MPC | P21 pin function control register | P21PFS | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 C152h | MPC | P22 pin function control register | P22PFS | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 C153h | MPC | P23 pin function control register | P23PFS | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 C154h | MPC | P24 pin function control register | P24PFS | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 C155h | MPC | P25 pin function control register | P25PFS | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 C156h | MPC | P26 pin function control register | P26PFS | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 C157h | MPC | P27 pin function control register | P27PFS | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 C158h | MPC | P30 pin function control register | P30PFS | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 C159h | MPC | P31 pin function control register | P31PFS | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 C15Ah | MPC | P32 pin function control register | P32PFS | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 C15Bh | MPC | P33 pin function control register | P33PFS | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 C15Ch | MPC | P34 pin function control register | P34PFS | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 C160h | MPC | P40 pin function control register | P40PFS | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 C161h | MPC | P41 pin function control register | P41PFS | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 C162h | MPC | P42 pin function control register | P42PFS | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 C163h | MPC | P43 pin function control register | P43PFS | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 C164h | MPC | P44 pin function control register | P44PFS | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 C165h | MPC | P45 pin function control register | P45PFS | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 C166h | MPC | P46 pin function control register | P46PFS | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 C167h | MPC | P47 pin function control register | P47PFS | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 C168h | MPC | P50 pin function control register | P50PFS | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 C169h | MPC | P51 pin function control register | P51PFS | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 C16Ah | MPC | P52 pin function control register | P52PFS | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 C16Ch | MPC | P54 pin function control register | P54PFS | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 C16Dh | MPC | P55 pin function control register | P55PFS | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 C16Eh | MPC | P56 pin function control register | P56PFS | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 C16Fh | MPC | P57 pin function control register | P57PFS | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 C170h | MPC | P60 pin function control register | P60PFS | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 C171h | MPC | P61 pin function control register | P61PFS | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 C176h | MPC | P66 pin function control register | P66PFS | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 C177h | MPC | P67 pin function control register | P67PFS | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |

Table 4.1 List of I/O Registers (Address Order) (33/50)

| Address | Module Symbol | Register Name | Register Symbol | Number of Bits | Access Size | Number of Access States | | Related Function |
|------------|---------------|-----------------------------------|-----------------|----------------|-------------|-------------------------|-----------|------------------|
| | | | | | | ICLK _≥ PCLK | ICLK<PCLK | |
| 0008 C178h | MPC | P70 pin function control register | P70PFS | 8 | 8 | 2, 3 PCLKB | 2 ICLK | MPC |
| 0008 C179h | MPC | P71 pin function control register | P71PFS | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 C17Ah | MPC | P72 pin function control register | P72PFS | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 C17Bh | MPC | P73 pin function control register | P73PFS | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 C17Ch | MPC | P74 pin function control register | P74PFS | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 C17Dh | MPC | P75 pin function control register | P75PFS | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 C17Eh | MPC | P76 pin function control register | P76PFS | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 C17Fh | MPC | P77 pin function control register | P77PFS | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 C180h | MPC | P80 pin function control register | P80PFS | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 C181h | MPC | P81 pin function control register | P81PFS | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 C182h | MPC | P82 pin function control register | P82PFS | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 C183h | MPC | P83 pin function control register | P83PFS | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 C186h | MPC | P86 pin function control register | P86PFS | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 C187h | MPC | P87 pin function control register | P87PFS | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 C188h | MPC | P90 pin function control register | P90PFS | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 C189h | MPC | P91 pin function control register | P91PFS | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 C18Ah | MPC | P92 pin function control register | P92PFS | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 C18Bh | MPC | P93 pin function control register | P93PFS | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 C190h | MPC | PA0 pin function control register | PA0PFS | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 C191h | MPC | PA1 pin function control register | PA1PFS | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 C192h | MPC | PA2 pin function control register | PA2PFS | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 C193h | MPC | PA3 pin function control register | PA3PFS | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 C194h | MPC | PA4 pin function control register | PA4PFS | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 C195h | MPC | PA5 pin function control register | PA5PFS | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 C196h | MPC | PA6 pin function control register | PA6PFS | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 C197h | MPC | PA7 pin function control register | PA7PFS | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 C198h | MPC | PB0 pin function control register | PB0PFS | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 C199h | MPC | PB1 pin function control register | PB1PFS | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 C19Ah | MPC | PB2 pin function control register | PB2PFS | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 C19Bh | MPC | PB3 pin function control register | PB3PFS | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 C19Ch | MPC | PB4 pin function control register | PB4PFS | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 C19Dh | MPC | PB5 pin function control register | PB5PFS | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 C19Eh | MPC | PB6 pin function control register | PB6PFS | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 C19Fh | MPC | PB7 pin function control register | PB7PFS | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 C1A0h | MPC | PC0 pin function control register | PC0PFS | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 C1A1h | MPC | PC1 pin function control register | PC1PFS | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 C1A2h | MPC | PC2 pin function control register | PC2PFS | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 C1A3h | MPC | PC3 pin function control register | PC3PFS | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 C1A4h | MPC | PC4 pin function control register | PC4PFS | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 C1A5h | MPC | PC5 pin function control register | PC5PFS | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 C1A6h | MPC | PC6 pin function control register | PC6PFS | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 C1A7h | MPC | PC7 pin function control register | PC7PFS | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 C1A8h | MPC | PD0 pin function control register | PD0PFS | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 C1A9h | MPC | PD1 pin function control register | PD1PFS | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 C1AAh | MPC | PD2 pin function control register | PD2PFS | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 C1ABh | MPC | PD3 pin function control register | PD3PFS | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 C1ACh | MPC | PD4 pin function control register | PD4PFS | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 C1ADh | MPC | PD5 pin function control register | PD5PFS | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 C1AEh | MPC | PD6 pin function control register | PD6PFS | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 C1AFh | MPC | PD7 pin function control register | PD7PFS | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 C1B0h | MPC | PE0 pin function control register | PE0PFS | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |

Table 4.1 List of I/O Registers (Address Order) (34/50)

| Address | Module Symbol | Register Name | Register Symbol | Number of Bits | Access Size | Number of Access States | | Related Function |
|--------------------------|---------------|---|-----------------|----------------|-------------|-------------------------|-----------|--------------------------|
| | | | | | | ICLK≥PCLK | ICLK<PCLK | |
| 0008 C1B1h | MPC | PE1 pin function control register | PE1PFS | 8 | 8 | 2, 3 PCLKB | 2 ICLK | MPC |
| 0008 C1B2h | MPC | PE2 pin function control register | PE2PFS | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 C1B3h | MPC | PE3 pin function control register | PE3PFS | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 C1B4h | MPC | PE4 pin function control register | PE4PFS | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 C1B5h | MPC | PE5 pin function control register | PE5PFS | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 C1B6h | MPC | PE6 pin function control register | PE6PFS | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 C1B7h | MPC | PE7 pin function control register | PE7PFS | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 C1B8h | MPC | PF0 pin function control register | PF0PFS | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 C1B9h | MPC | PF1 pin function control register | PF1PFS | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 C1BAh | MPC | PF2 pin function control register | PF2PFS | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 C1BDh | MPC | PF5 pin function control register | PF5PFS | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 C1D3h | MPC | PJ3 pin function control register | PJ3PFS | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 C280h | SYSTEM | Deep standby control register | DPSBYCR | 8 | 8 | 4, 5 PCLKB | 2, 3 ICLK | |
| 0008 C282h | SYSTEM | Deep standby interrupt enable register 0 | DPSIER0 | 8 | 8 | 4, 5 PCLKB | 2, 3 ICLK | |
| 0008 C283h | SYSTEM | Deep standby interrupt enable register 1 | DPSIER1 | 8 | 8 | 4, 5 PCLKB | 2, 3 ICLK | |
| 0008 C284h | SYSTEM | Deep standby interrupt enable register 2 | DPSIER2 | 8 | 8 | 4, 5 PCLKB | 2, 3 ICLK | |
| 0008 C285h | SYSTEM | Deep standby interrupt enable register 3 | DPSIER3 | 8 | 8 | 4, 5 PCLKB | 2, 3 ICLK | |
| 0008 C286h | SYSTEM | Deep standby interrupt flag register 0 | DPSIFR0 | 8 | 8 | 4, 5 PCLKB | 2, 3 ICLK | |
| 0008 C287h | SYSTEM | Deep standby interrupt flag register 1 | DPSIFR1 | 8 | 8 | 4, 5 PCLKB | 2, 3 ICLK | |
| 0008 C288h | SYSTEM | Deep standby interrupt flag register 2 | DPSIFR2 | 8 | 8 | 4, 5 PCLKB | 2, 3 ICLK | |
| 0008 C289h | SYSTEM | Deep standby interrupt flag register 3 | DPSIFR3 | 8 | 8 | 4, 5 PCLKB | 2, 3 ICLK | |
| 0008 C28Ah | SYSTEM | Deep standby interrupt edge register 0 | DPSIEGR0 | 8 | 8 | 4, 5 PCLKB | 2, 3 ICLK | |
| 0008 C28Bh | SYSTEM | Deep standby interrupt edge register 1 | DPSIEGR1 | 8 | 8 | 4, 5 PCLKB | 2, 3 ICLK | |
| 0008 C28Ch | SYSTEM | Deep standby interrupt edge register 2 | DPSIEGR2 | 8 | 8 | 4, 5 PCLKB | 2, 3 ICLK | |
| 0008 C28Dh | SYSTEM | Deep standby interrupt edge register 3 | DPSIEGR3 | 8 | 8 | 4, 5 PCLKB | 2, 3 ICLK | |
| 0008 C290h | SYSTEM | Reset status register 0 | RSTSR0 | 8 | 8 | 4, 5 PCLKB | 2, 3 ICLK | Resets |
| 0008 C291h | SYSTEM | Reset status register 1 | RSTSR1 | 8 | 8 | 4, 5 PCLKB | 2, 3 ICLK | |
| 0008 C293h | SYSTEM | Main clock oscillator forced oscillation control register | MOFCR | 8 | 8 | 4, 5 PCLKB | 2, 3 ICLK | Clock Generation Circuit |
| 0008 C294h | SYSTEM | High-speed on-chip oscillator power supply control register | HOCOPCR | 8 | 8 | 4, 5 PCLKB | 2, 3 ICLK | |
| 0008 C296h | FLASH | Flash write erase protection register | FWEPOR | 8 | 8 | 4, 5 PCLKB | 2, 3 ICLK | ROM |
| 0008 C297h | SYSTEM | Voltage monitoring circuit control register | LVCMPCR | 8 | 8 | 4, 5 PCLKB | 2, 3 ICLK | LVDA |
| 0008 C298h | SYSTEM | Voltage detection level select register | LVDLVL | 8 | 8 | 4, 5 PCLKB | 2, 3 ICLK | |
| 0008 C29Ah | SYSTEM | Voltage monitoring 1 circuit control register 0 | LVD1CR0 | 8 | 8 | 4, 5 PCLKB | 2, 3 ICLK | |
| 0008 C29Bh | SYSTEM | Voltage monitoring 2 circuit control register 0 | LVD2CR0 | 8 | 8 | 4, 5 PCLKB | 2, 3 ICLK | |
| 0008 C2A0h to 0008 C2BFh | SYSTEM | Deep standby backup register 0 to 31 | DPSBKR0 to 31 | 8 | 8 | 4, 5 PCLKB | 2, 3 ICLK | Low Power Consumption |
| 0008 C300h | ICU | Group 0 interrupt source register | GRP00 | 32 | 32 | 1 to 2PCLKB | 2 ICLK | ICUb |
| 0008 C304h | ICU | Group 1 interrupt source register | GRP01 | 32 | 32 | 1 to 2PCLKB | 2 ICLK | |
| 0008 C308h | ICU | Group 2 interrupt source register | GRP02 | 32 | 32 | 1 to 2PCLKB | 2 ICLK | |
| 0008 C30Ch | ICU | Group 3 interrupt source register | GRP03 | 32 | 32 | 1 to 2PCLKB | 2 ICLK | |
| 0008 C310h | ICU | Group 4 interrupt source register | GRP04 | 32 | 32 | 1 to 2PCLKB | 2 ICLK | |
| 0008 C314h | ICU | Group 5 interrupt source register | GRP05 | 32 | 32 | 1 to 2PCLKB | 2 ICLK | |
| 0008 C318h | ICU | Group 6 interrupt source register | GRP06 | 32 | 32 | 1 to 2PCLKB | 2 ICLK | |
| 0008 C330h | ICU | Group 12 interrupt source register | GRP12 | 32 | 32 | 1 to 2PCLKB | 2 ICLK | |
| 0008 C340h | ICU | Group 0 interrupt enable register | GEN00 | 32 | 32 | 1 to 2PCLKB | 2 ICLK | |

Table 4.1 List of I/O Registers (Address Order) (35/50)

| Address | Module Symbol | Register Name | Register Symbol | Number of Bits | Access Size | Number of Access States | | Related Function |
|------------|---------------|------------------------------------|-----------------|----------------|-------------|-------------------------|-----------|------------------|
| | | | | | | ICLK \geq PCLK | ICLK<PCLK | |
| 0008 C344h | ICU | Group 1 interrupt enable register | GEN01 | 32 | 32 | 1 to 2PCLKB | 2 ICLK | ICUb |
| 0008 C348h | ICU | Group 2 interrupt enable register | GEN02 | 32 | 32 | 1 to 2PCLKB | 2 ICLK | |
| 0008 C34Ch | ICU | Group 3 interrupt enable register | GEN03 | 32 | 32 | 1 to 2PCLKB | 2 ICLK | |
| 0008 C350h | ICU | Group 4 interrupt enable register | GEN04 | 32 | 32 | 1 to 2PCLKB | 2 ICLK | |
| 0008 C354h | ICU | Group 5 interrupt enable register | GEN05 | 32 | 32 | 1 to 2PCLKB | 2 ICLK | |
| 0008 C358h | ICU | Group 6 interrupt enable register | GEN06 | 32 | 32 | 1 to 2PCLKB | 2 ICLK | |
| 0008 C370h | ICU | Group 12 interrupt enable register | GEN12 | 32 | 32 | 1 to 2PCLKB | 2 ICLK | |
| 0008 C380h | ICU | Group 0 interrupt clear register | GCR00 | 32 | 32 | 1 to 2PCLKB | 2 ICLK | |
| 0008 C384h | ICU | Group 1 interrupt clear register | GCR01 | 32 | 32 | 1 to 2PCLKB | 2 ICLK | |
| 0008 C388h | ICU | Group 2 interrupt clear register | GCR02 | 32 | 32 | 1 to 2PCLKB | 2 ICLK | |
| 0008 C38Ch | ICU | Group 3 interrupt clear register | GCR03 | 32 | 32 | 1 to 2PCLKB | 2 ICLK | |
| 0008 C390h | ICU | Group 4 interrupt clear register | GCR04 | 32 | 32 | 1 to 2PCLKB | 2 ICLK | |
| 0008 C394h | ICU | Group 5 interrupt clear register | GCR05 | 32 | 32 | 1 to 2PCLKB | 2 ICLK | |
| 0008 C398h | ICU | Group 6 interrupt clear register | GCR06 | 32 | 32 | 1 to 2PCLKB | 2 ICLK | |
| 0008 C3C0h | ICU | Unit select register | SEL | 32 | 32 | 1 to 2PCLKB | 2 ICLK | |
| 0008 C400h | RTC | 64-Hz counter | R64CNT | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 C402h | RTC | Second counter | RSECCNT | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 C404h | RTC | Minute counter | RMINCNT | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 C406h | RTC | Hour counter | RHRCNT | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 C408h | RTC | Day-of-week counter | RWKCNT | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 C40Ah | RTC | Date counter | RDAYCNT | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 C40Ch | RTC | Month counter | RMONCNT | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 C40Eh | RTC | Year counter | RYRCNT | 16 | 16 | 2, 3 PCLKB | 2 ICLK | |
| 0008 C410h | RTC | Second alarm register | RSECCAR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 C412h | RTC | Minute alarm register | RMINAR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 C414h | RTC | Hour alarm register | RHRAR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 C416h | RTC | Day-of-week alarm register | RWKAR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 C418h | RTC | Date alarm register | RDAYAR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 C41Ah | RTC | Month alarm register | RMONAR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 C41Ch | RTC | Year alarm register | RYRAR | 16 | 16 | 2, 3 PCLKB | 2 ICLK | |
| 0008 C41Eh | RTC | Year alarm enable register | RYRAREN | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 C422h | RTC | RTC control register 1 | RCR1 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 C424h | RTC | RTC control register 2 | RCR2 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 C426h | RTC | RTC control register 3 | RCR3 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 C428h | RTC | RTC control register 4 | RCR4 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 C42Ah | RTC | Frequency register H | RFRH | 16 | 16 | 2, 3 PCLKB | 2 ICLK | |
| 0008 C42Ch | RTC | Frequency register L | RFRL | 16 | 16 | 2, 3 PCLKB | 2 ICLK | |
| 0008 C42Eh | RTC | Time error adjustment register | RADJ | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 C440h | RTC | Time capture control register 0 | RTCCR0 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 C442h | RTC | Time capture control register 1 | RTCCR1 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 C444h | RTC | Time capture control register 2 | RTCCR2 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 C452h | RTC | Second capture register 0 | RSECCP0 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 C454h | RTC | Minute capture register 0 | RMINCP0 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |

Table 4.1 List of I/O Registers (Address Order) (36/50)

| Address | Module Symbol | Register Name | Register Symbol | Number of Bits | Access Size | Number of Access States | | Related Function |
|--------------------------|---------------|--|-----------------|----------------|-------------|-------------------------|-----------|------------------|
| | | | | | | ICLK≥PCLK | ICLK<PCLK | |
| 0008 C456h | RTC | Hour capture register 0 | RHRCP0 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | RTCa |
| 0008 C45Ah | RTC | Date capture register 0 | RDAYCP0 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 C45Ch | RTC | Month capture register 0 | RMONCP0 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 C462h | RTC | Second capture register 1 | RSECCP1 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 C464h | RTC | Minute capture register 1 | RMINCP1 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 C466h | RTC | Hour capture register 1 | RHRCP1 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 C46Ah | RTC | Date capture register 1 | RDAYCP1 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 C46Ch | RTC | Month capture register 1 | RMONCP1 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 C472h | RTC | Second capture register 2 | RSECCP2 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 C474h | RTC | Minute capture register 2 | RMINCP2 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 C476h | RTC | Hour capture register 2 | RHRCP2 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 C47Ah | RTC | Date capture register 2 | RDAYCP2 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 C47Ch | RTC | Month capture register 2 | RMONCP2 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 C500h | TEMPS | Temperature sensor control register | TSCR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 C880h | SYSTEM | Counter-clock extension register 1 | SCK1 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | MCK |
| 0008 C890h | SYSTEM | Counter-clock extension register 2 | SCK2 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0009 0200h to 0009 03FFh | CAN0 | Mailbox registers 0 to 31 | MB0 to 31 | 128 | 8, 16, 32 | 2, 3 PCLKB | 2 ICLK | CAN |
| 0009 0400h to 0009 041Fh | CAN0 | Mask register 0 to 7 | MKR0 to 7 | 32 | 8, 16, 32 | 2, 3 PCLKB | 2 ICLK | |
| 0009 0420h | CAN0 | FIFO received ID compare register 0 | FIDCR0 | 32 | 8, 16, 32 | 2, 3 PCLKB | 2 ICLK | |
| 0009 0424h | CAN0 | FIFO received ID compare register 1 | FIDCR1 | 32 | 8, 16, 32 | 2, 3 PCLKB | 2 ICLK | |
| 0009 0428h | CAN0 | Mask invalid register | MKIVLR | 32 | 8, 16, 32 | 2, 3 PCLKB | 2 ICLK | |
| 0009 042Ch | CAN0 | Mailbox interrupt enable register | MIER | 32 | 8, 16, 32 | 2, 3 PCLKB | 2 ICLK | |
| 0009 0820h to 0009 083Fh | CAN0 | Message control registers 0 to 31 | MCTL0 to 31 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0009 0840h | CAN0 | Control register | CTLR | 16 | 8, 16 | 2, 3 PCLKB | 2 ICLK | |
| 0009 0842h | CAN0 | Status register | STR | 16 | 8, 16 | 2, 3 PCLKB | 2 ICLK | |
| 0009 0844h | CAN0 | Bit configuration register | BCR | 32 | 8, 16, 32 | 2, 3 PCLKB | 2 ICLK | |
| 0009 0848h | CAN0 | Receive FIFO control register | RFCR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0009 0849h | CAN0 | Receive FIFO pointer control register | RFPCR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0009 084Ah | CAN0 | Transmit FIFO control register | TFCR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0009 084Bh | CAN0 | Transmit FIFO pointer control register | TFPCR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0009 084Ch | CAN0 | Error interrupt enable register | EIER | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0009 084Dh | CAN0 | Error interrupt factor judge register | EIFR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0009 084Eh | CAN0 | Receive error count register | RECR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0009 084Fh | CAN0 | Transmit error count register | TECR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0009 0850h | CAN0 | Error code store register | ECSR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0009 0851h | CAN0 | Channel search support register | CSSR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0009 0852h | CAN0 | Mailbox search status register | MSSR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0009 0853h | CAN0 | Mailbox search mode register | MSMR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0009 0854h | CAN0 | Time stamp register | TSR | 16 | 16 | 2, 3 PCLKB | 2 ICLK | |
| 0009 0856h | CAN0 | Acceptance filter support register | AFSR | 16 | 16 | 2, 3 PCLKB | 2 ICLK | |
| 0009 0858h | CAN0 | Test control register | TCR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0009 1200h to 0009 13FFh | CAN1 | Mailbox registers 0 to 31 | MB0 to 31 | 128 | 8, 16, 32 | 2, 3 PCLKB | 2 ICLK | |
| 0009 1400h to 0009 141Fh | CAN1 | Mask register 0 to 7 | MKR0 to 7 | 32 | 8, 16, 32 | 2, 3 PCLKB | 2 ICLK | |
| 0009 1420h | CAN1 | FIFO received ID compare register 0 | FIDCR0 | 32 | 8, 16, 32 | 2, 3 PCLKB | 2 ICLK | |
| 0009 1424h | CAN1 | FIFO received ID compare register 1 | FIDCR1 | 32 | 8, 16, 32 | 2, 3 PCLKB | 2 ICLK | |

Table 4.1 List of I/O Registers (Address Order) (37/50)

| Address | Module Symbol | Register Name | Register Symbol | Number of Bits | Access Size | Number of Access States | | Related Function |
|--------------------------|---------------|--|-----------------|----------------|-------------|-------------------------|---------------|------------------|
| | | | | | | ICLK \geq PCLK | ICLK $<$ PCLK | |
| 0009 1428h | CAN1 | Mask invalid register | MKIVLR | 32 | 8, 16, 32 | 2, 3 PCLKB | 2 ICLK | CAN |
| 0009 142Ch | CAN1 | Mailbox interrupt enable register | MIER | 32 | 8, 16, 32 | 2, 3 PCLKB | 2 ICLK | |
| 0009 1820h to 0009 183Fh | CAN1 | Message control registers 0 to 31 | MCTL0 to 31 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0009 1840h | CAN1 | Control register | CTLR | 16 | 8, 16 | 2, 3 PCLKB | 2 ICLK | |
| 0009 1842h | CAN1 | Status register | STR | 16 | 8, 16 | 2, 3 PCLKB | 2 ICLK | |
| 0009 1844h | CAN1 | Bit configuration register | BCR | 32 | 8, 16, 32 | 2, 3 PCLKB | 2 ICLK | |
| 0009 1848h | CAN1 | Receive FIFO control register | RFCR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0009 1849h | CAN1 | Receive FIFO pointer control register | RFPCR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0009 184Ah | CAN1 | Transmit FIFO control register | TFCR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0009 184Bh | CAN1 | Transmit FIFO pointer control register | TFPCR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0009 184Ch | CAN1 | Error interrupt enable register | EIER | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0009 184Dh | CAN1 | Error interrupt factor judge register | EIFR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0009 184Eh | CAN1 | Receive error count register | RECR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0009 184Fh | CAN1 | Transmit error count register | TECR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0009 1850h | CAN1 | Error code store register | ECSR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0009 1851h | CAN1 | Channel search support register | CSSR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0009 1852h | CAN1 | Mailbox search status register | MSSR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0009 1853h | CAN1 | Mailbox search mode register | MSMR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0009 1854h | CAN1 | Time stamp register | TSR | 16 | 8, 16 | 2, 3 PCLKB | 2 ICLK | |
| 0009 1856h | CAN1 | Acceptance filter support register | AFSR | 16 | 8, 16 | 2, 3 PCLKB | 2 ICLK | |
| 0009 1858h | CAN1 | Test control register | TCR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0009 2200h to 0009 23FFh | CAN2 | Mailbox registers 0 to 31 | MB0 to 31 | 128 | 8, 16, 32 | 2, 3 PCLKB | 2 ICLK | |
| 0009 2400h to 0009 241Fh | CAN2 | Mask register 0 to 7 | MKR0 to 7 | 32 | 8, 16, 32 | 2, 3 PCLKB | 2 ICLK | |
| 0009 2420h | CAN2 | FIFO received ID compare register 0 | FIDCR0 | 32 | 8, 16, 32 | 2, 3 PCLKB | 2 ICLK | |
| 0009 2424h | CAN2 | FIFO received ID compare register 1 | FIDCR1 | 32 | 8, 16, 32 | 2, 3 PCLKB | 2 ICLK | |
| 0009 2428h | CAN2 | Mask invalid register | MKIVLR | 32 | 8, 16, 32 | 2, 3 PCLKB | 2 ICLK | |
| 0009 242Ch | CAN2 | Mailbox interrupt enable register | MIER | 32 | 8, 16, 32 | 2, 3 PCLKB | 2 ICLK | |
| 0009 2820h to 0009 283Fh | CAN2 | Message control registers 0 to 31 | MCTL0 to 31 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0009 2840h | CAN2 | Control register | CTLR | 16 | 8, 16 | 2, 3 PCLKB | 2 ICLK | |
| 0009 2842h | CAN2 | Status register | STR | 16 | 8, 16 | 2, 3 PCLKB | 2 ICLK | |
| 0009 2844h | CAN2 | Bit configuration register | BCR | 32 | 8, 16, 32 | 2, 3 PCLKB | 2 ICLK | |
| 0009 2848h | CAN2 | Receive FIFO control register | RFCR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0009 2849h | CAN2 | Receive FIFO pointer control register | RFPCR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0009 284Ah | CAN2 | Transmit FIFO control register | TFCR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0009 284Bh | CAN2 | Transmit FIFO pointer control register | TFPCR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0009 284Ch | CAN2 | Error interrupt enable register | EIER | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0009 284Dh | CAN2 | Error interrupt factor judge register | EIFR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0009 284Eh | CAN2 | Receive error count register | RECR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0009 284Fh | CAN2 | Transmit error count register | TECR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0009 2850h | CAN2 | Error code store register | ECSR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0009 2851h | CAN2 | Channel search support register | CSSR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0009 2852h | CAN2 | Mailbox search status register | MSSR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0009 2853h | CAN2 | Mailbox search mode register | MSMR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0009 2854h | CAN2 | Time stamp register | TSR | 16 | 16 | 2, 3 PCLKB | 2 ICLK | |
| 0009 2856h | CAN2 | Acceptance filter support register | AFSR | 16 | 16 | 2, 3 PCLKB | 2 ICLK | |
| 0009 2858h | CAN2 | Test control register | TCR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |

Table 4.1 List of I/O Registers (Address Order) (38/50)

| Address | Module Symbol | Register Name | Register Symbol | Number of Bits | Access Size | Number of Access States | | Related Function |
|------------|---------------|--|-----------------|----------------|-------------|-------------------------|--|------------------|
| | | | | | | ICLK \geq PCLK | ICLK<PCLK | |
| 000A 0000h | USB0 | System configuration control register | SYSCFG | 16 | 16 | 3 to 4 PCLKB | 2, 3 ICLK | USBa |
| 000A 0004h | USB0 | System configuration status register 0 | SYSSTS0 | 16 | 16 | 9 PCLKB or more | Rounded up to the nearest integer greater than $1 + 9 / (\text{frequency ratio of ICLK} / \text{PCLKB})^6$ | |
| 000A 0008h | USB0 | Device state control register 0 | DVSTCTR0 | 16 | 16 | 9 PCLKB or more | Rounded up to the nearest integer greater than $1 + 9 / (\text{frequency ratio of ICLK} / \text{PCLKB})^6$ | |
| 000A 0014h | USB0 | CFIFO port register | CFIFO | 16 | 8, 16 | 3 to 4 PCLKB | 2, 3 ICLK | |
| 000A 0018h | USB0 | D0FIFO port register | D0FIFO | 16 | 8, 16 | 3 to 4 PCLKB | 2, 3 ICLK | |
| 000A 001Ch | USB0 | D1FIFO port register | D1FIFO | 16 | 8, 16 | 3 to 4 PCLKB | 2, 3 ICLK | |
| 000A 0020h | USB0 | CFIFO port select register | CFIFOSEL | 16 | 16 | 3 to 4 PCLKB | 2, 3 ICLK | |
| 000A 0022h | USB0 | CFIFO port control register | CFIFOCTR | 16 | 16 | 3 to 4 PCLKB | 2, 3 ICLK | |
| 000A 0028h | USB0 | D0FIFO port select register | D0FIFOSEL | 16 | 16 | 3 to 4 PCLKB | 2, 3 ICLK | |
| 000A 002Ah | USB0 | D0FIFO port control register | D0FIFOCTR | 16 | 16 | 3 to 4 PCLKB | 2, 3 ICLK | |
| 000A 002Ch | USB0 | D1FIFO port select register | D1FIFOSEL | 16 | 16 | 3 to 4 PCLKB | 2, 3 ICLK | |
| 000A 002Eh | USB0 | D1FIFO port control register | D1FIFOCTR | 16 | 16 | 3 to 4 PCLKB | 2, 3 ICLK | |
| 000A 0030h | USB0 | Interrupt enable register 0 | INTENB0 | 16 | 16 | 9 PCLKB or more | Rounded up to the nearest integer greater than $1 + 9 / (\text{frequency ratio of ICLK} / \text{PCLKB})^6$ | |
| 000A 0032h | USB0 | Interrupt enable register 1 | INTENB1 | 16 | 16 | 9 PCLKB or more | Rounded up to the nearest integer greater than $1 + 9 / (\text{frequency ratio of ICLK} / \text{PCLKB})^6$ | |
| 000A 0036h | USB0 | BRDY interrupt enable register | BRDYENB | 16 | 16 | 9 PCLKB or more | Rounded up to the nearest integer greater than $1 + 9 / (\text{frequency ratio of ICLK} / \text{PCLKB})^6$ | |
| 000A 0038h | USB0 | NRDY interrupt enable register | NRDYENB | 16 | 16 | 9 PCLKB or more | Rounded up to the nearest integer greater than $1 + 9 / (\text{frequency ratio of ICLK} / \text{PCLKB})^6$ | |

Table 4.1 List of I/O Registers (Address Order) (39/50)

| Address | Module Symbol | Register Name | Register Symbol | Number of Bits | Access Size | Number of Access States | | Related Function |
|------------|---------------|-----------------------------------|-----------------|----------------|-------------|-------------------------|---|------------------|
| | | | | | | ICLK \geq PCLK | ICLK<PCLK | |
| 000A 003Ah | USB0 | BEMP interrupt enable register | BEMPENB | 16 | 16 | 9 PCLKB or more | Rounded up to the nearest integer greater than 1 + 9/ (frequency ratio of ICLK/ PCLKB) ⁶ | USBa |
| 000A 003Ch | USB0 | SOF output configuration register | SOFCFG | 16 | 16 | 9 PCLKB or more | Rounded up to the nearest integer greater than 1 + 9/ (frequency ratio of ICLK/ PCLKB) ⁶ | |
| 000A 0040h | USB0 | Interrupt status register 0 | INTSTS0 | 16 | 16 | 9 PCLKB or more | Rounded up to the nearest integer greater than 1 + 9/ (frequency ratio of ICLK/ PCLKB) ⁶ | |
| 000A 0042h | USB0 | Interrupt status register 1 | INTSTS1 | 16 | 16 | 9 PCLKB or more | Rounded up to the nearest integer greater than 1 + 9/ (frequency ratio of ICLK/ PCLKB) ⁶ | |
| 000A 0046h | USB0 | BRDY interrupt status register | BRDYSTS | 16 | 16 | 9 PCLKB or more | Rounded up to the nearest integer greater than 1 + 9/ (frequency ratio of ICLK/ PCLKB) ⁶ | |
| 000A 0048h | USB0 | NRDY interrupt status register | NRDYSTS | 16 | 16 | 9 PCLKB or more | Rounded up to the nearest integer greater than 1 + 9/ (frequency ratio of ICLK/ PCLKB) ⁶ | |
| 000A 004Ah | USB0 | BEMP interrupt status register | BEMPSTS | 16 | 16 | 9 PCLKB or more | Rounded up to the nearest integer greater than 1 + 9/ (frequency ratio of ICLK/ PCLKB) ⁶ | |
| 000A 004Ch | USB0 | Frame number register | FRMNUM | 16 | 16 | 9 PCLKB or more | Rounded up to the nearest integer greater than 1 + 9/ (frequency ratio of ICLK/ PCLKB) ⁶ | |
| 000A 004Eh | USB0 | Device state changing register | DVCHGR | 16 | 16 | 9 PCLKB or more | Rounded up to the nearest integer greater than 1 + 9/ (frequency ratio of ICLK/ PCLKB) ⁶ | USBa |
| 000A 0050h | USB0 | USB address register | USBADDR | 16 | 16 | 9 PCLKB or more | Rounded up to the nearest integer greater than 1 + 9/ (frequency ratio of ICLK/ PCLKB) ⁶ | |

Table 4.1 List of I/O Registers (Address Order) (40/50)

| Address | Module Symbol | Register Name | Register Symbol | Number of Bits | Access Size | Number of Access States | | Related Function |
|------------|---------------|-----------------------------------|-----------------|----------------|-------------|-------------------------|---|------------------|
| | | | | | | ICLK \geq PCLK | ICLK<PCLK | |
| 000A 0054h | USB0 | USB request type register | USBREQ | 16 | 16 | 9 PCLKB or more | Rounded up to the nearest integer greater than 1 + 9/ (frequency ratio of ICLK/ PCLKB) ⁶ | |
| 000A 0056h | USB0 | USB request value register | USBVAL | 16 | 16 | 9 PCLKB or more | Rounded up to the nearest integer greater than 1 + 9/ (frequency ratio of ICLK/ PCLKB) ⁶ | |
| 000A 0058h | USB0 | USB request index register | USBINDX | 16 | 16 | 9 PCLKB or more | Rounded up to the nearest integer greater than 1 + 9/ (frequency ratio of ICLK/ PCLKB) ⁶ | |
| 000A 005Ah | USB0 | USB request length register | USBLENG | 16 | 16 | 9 PCLKB or more | Rounded up to the nearest integer greater than 1 + 9/ (frequency ratio of ICLK/ PCLKB) ⁶ | |
| 000A 005Ch | USB0 | DCP configuration register | DCPCFG | 16 | 16 | 9 PCLKB or more | Rounded up to the nearest integer greater than 1 + 9/ (frequency ratio of ICLK/ PCLKB) ⁶ | |
| 000A 005Eh | USB0 | DCP maximum packet size register | DCPMAXP | 16 | 16 | 9 PCLKB or more | Rounded up to the nearest integer greater than 1 + 9/ (frequency ratio of ICLK/ PCLKB) ⁶ | |
| 000A 0060h | USB0 | DCP control register | DCPCTR | 16 | 16 | 9 PCLKB or more | Rounded up to the nearest integer greater than 1 + 9/ (frequency ratio of ICLK/ PCLKB) ⁶ | |
| 000A 0064h | USB0 | Pipe window select register | PIPESEL | 16 | 16 | 9 PCLKB or more | Rounded up to the nearest integer greater than 1 + 9/ (frequency ratio of ICLK/ PCLKB) ⁶ | USBa |
| 000A 0068h | USB0 | Pipe configuration register | PIPECFG | 16 | 16 | 9 PCLKB or more | Rounded up to the nearest integer greater than 1 + 9/ (frequency ratio of ICLK/ PCLKB) ⁶ | |
| 000A 006Ch | USB0 | Pipe maximum packet size register | PIPEMAXP | 16 | 16 | 9 PCLKB or more | Rounded up to the nearest integer greater than 1 + 9/ (frequency ratio of ICLK/ PCLKB) ⁶ | |

Table 4.1 List of I/O Registers (Address Order) (41/50)

| Address | Module Symbol | Register Name | Register Symbol | Number of Bits | Access Size | Number of Access States | | Related Function |
|------------|---------------|-----------------------------|-----------------|----------------|-------------|-------------------------|---|------------------|
| | | | | | | ICLK \geq PCLK | ICLK<PCLK | |
| 000A 006Eh | USB0 | Pipe cycle control register | PIPEPERI | 16 | 16 | 9 PCLKB or more | Rounded up to the nearest integer greater than 1 + 9/ (frequency ratio of ICLK/ PCLKB) ⁶ | |
| 000A 0070h | USB0 | Pipe 1 control register | PIPE1CTR | 16 | 16 | 9 PCLKB or more | Rounded up to the nearest integer greater than 1 + 9/ (frequency ratio of ICLK/ PCLKB) ⁶ | |
| 000A 0072h | USB0 | Pipe 2 control register | PIPE2CTR | 16 | 16 | 9 PCLKB or more | Rounded up to the nearest integer greater than 1 + 9/ (frequency ratio of ICLK/ PCLKB) ⁶ | |
| 000A 0074h | USB0 | Pipe 3 control register | PIPE3CTR | 16 | 16 | 9 PCLKB or more | Rounded up to the nearest integer greater than 1 + 9/ (frequency ratio of ICLK/ PCLKB) ⁶ | |
| 000A 0076h | USB0 | Pipe 4 control register | PIPE4CTR | 16 | 16 | 9 PCLKB or more | Rounded up to the nearest integer greater than 1 + 9/ (frequency ratio of ICLK/ PCLKB) ⁶ | |
| 000A 0078h | USB0 | Pipe 5 control register | PIPE5CTR | 16 | 16 | 9 PCLKB or more | Rounded up to the nearest integer greater than 1 + 9/ (frequency ratio of ICLK/ PCLKB) ⁶ | USBa |
| 000A 007Ah | USB0 | Pipe 6 control register | PIPE6CTR | 16 | 16 | 9 PCLKB or more | Rounded up to the nearest integer greater than 1 + 9/ (frequency ratio of ICLK/ PCLKB) ⁶ | |
| 000A 007Ch | USB0 | Pipe 7 control register | PIPE7CTR | 16 | 16 | 9 PCLKB or more | Rounded up to the nearest integer greater than 1 + 9/ (frequency ratio of ICLK/ PCLKB) ⁶ | |
| 000A 007Eh | USB0 | Pipe 8 control register | PIPE8CTR | 16 | 16 | 9 PCLKB or more | Rounded up to the nearest integer greater than 1 + 9/ (frequency ratio of ICLK/ PCLKB) ⁶ | |
| 000A 0080h | USB0 | Pipe 9 control register | PIPE9CTR | 16 | 16 | 9 PCLKB or more | Rounded up to the nearest integer greater than 1 + 9/ (frequency ratio of ICLK/ PCLKB) ⁶ | |

Table 4.1 List of I/O Registers (Address Order) (42/50)

| Address | Module Symbol | Register Name | Register Symbol | Number of Bits | Access Size | Number of Access States | | Related Function |
|------------|---------------|--|-----------------|----------------|-------------|-------------------------|---|------------------|
| | | | | | | ICLK \geq PCLK | ICLK<PCLK | |
| 000A 0090h | USB0 | Pipe 1 transaction counter enable register | PIPE1TRE | 16 | 16 | 9 PCLKB or more | Rounded up to the nearest integer greater than 1 + 9/ (frequency ratio of ICLK/ PCLKB) ⁶ | |
| 000A 0092h | USB0 | Pipe 1 transaction counter register | PIPE1TRN | 16 | 16 | 9 PCLKB or more | Rounded up to the nearest integer greater than 1 + 9/ (frequency ratio of ICLK/ PCLKB) ⁶ | |
| 000A 0094h | USB0 | Pipe 2 transaction counter enable register | PIPE2TRE | 16 | 16 | 9 PCLKB or more | Rounded up to the nearest integer greater than 1 + 9/ (frequency ratio of ICLK/ PCLKB) ⁶ | |
| 000A 0096h | USB0 | Pipe 2 transaction counter register | PIPE2TRN | 16 | 16 | 9 PCLKB or more | Rounded up to the nearest integer greater than 1 + 9/ (frequency ratio of ICLK/ PCLKB) ⁶ | USBa |
| 000A 0098h | USB0 | Pipe 3 transaction counter enable register | PIPE3TRE | 16 | 16 | 9 PCLKB or more | Rounded up to the nearest integer greater than 1 + 9/ (frequency ratio of ICLK/ PCLKB) ⁶ | |
| 000A 009Ah | USB0 | Pipe 3 transaction counter register | PIPE3TRN | 16 | 16 | 9 PCLKB or more | Rounded up to the nearest integer greater than 1 + 9/ (frequency ratio of ICLK/ PCLKB) ⁶ | |
| 000A 009Ch | USB0 | Pipe 4 transaction counter enable register | PIPE4TRE | 16 | 16 | 9 PCLKB or more | Rounded up to the nearest integer greater than 1 + 9/ (frequency ratio of ICLK/ PCLKB) ⁶ | |
| 000A 009Eh | USB0 | Pipe 4 transaction counter register | PIPE4TRN | 16 | 16 | 9 PCLKB or more | Rounded up to the nearest integer greater than 1 + 9/ (frequency ratio of ICLK/ PCLKB) ⁶ | |
| 000A 00A0h | USB0 | Pipe 5 transaction counter enable register | PIPE5TRE | 16 | 16 | 9 PCLKB or more | Rounded up to the nearest integer greater than 1 + 9/ (frequency ratio of ICLK/ PCLKB) ⁶ | |
| 000A 00A2h | USB0 | Pipe 5 transaction counter register | PIPE5TRN | 16 | 16 | 9 PCLKB or more | Rounded up to the nearest integer greater than 1 + 9/ (frequency ratio of ICLK/ PCLKB) ⁶ | |

Table 4.1 List of I/O Registers (Address Order) (43/50)

| Address | Module Symbol | Register Name | Register Symbol | Number of Bits | Access Size | Number of Access States | | Related Function |
|------------|---------------|---|-----------------|----------------|-------------|-------------------------|---|------------------|
| | | | | | | ICLK \geq PCLK | ICLK<PCLK | |
| 000A 00D0h | USB0 | Device address 0 configuration register | DEVADD0 | 16 | 16 | 9 PCLKB or more | Rounded up to the nearest integer greater than 1 + 9/ (frequency ratio of ICLK/ PCLKB) ⁶ | |
| 000A 00D2h | USB0 | Device address 1 configuration register | DEVADD1 | 16 | 16 | 9 PCLKB or more | Rounded up to the nearest integer greater than 1 + 9/ (frequency ratio of ICLK/ PCLKB) ⁶ | USBa |
| 000A 00D4h | USB0 | Device address 2 configuration register | DEVADD2 | 16 | 16 | 9 PCLKB or more | Rounded up to the nearest integer greater than 1 + 9/ (frequency ratio of ICLK/ PCLKB) ⁶ | |
| 000A 00D6h | USB0 | Device address 3 configuration register | DEVADD3 | 16 | 16 | 9 PCLKB or more | Rounded up to the nearest integer greater than 1 + 9/ (frequency ratio of ICLK/ PCLKB) ⁶ | |
| 000A 00D8h | USB0 | Device address 4 configuration register | DEVADD4 | 16 | 16 | 9 PCLKB or more | Rounded up to the nearest integer greater than 1 + 9/ (frequency ratio of ICLK/ PCLKB) ⁶ | |
| 000A 00DAh | USB0 | Device address 5 configuration register | DEVADD5 | 16 | 16 | 9 PCLKB or more | Rounded up to the nearest integer greater than 1 + 9/ (frequency ratio of ICLK/ PCLKB) ⁶ | |
| 000A 0200h | USB1 | System configuration control register | SYSCFG | 16 | 16 | 3 to 4 PCLKB | 2, 3 ICLK | |
| 000A 0204h | USB1 | System configuration status register 0 | SYSSTS0 | 16 | 16 | 9 PCLKB or more | Rounded up to the nearest integer greater than 1 + 9/ (frequency ratio of ICLK/ PCLKB) ⁶ | |
| 000A 0208h | USB1 | Device state control register 0 | DVSTCTR0 | 16 | 16 | 9 PCLKB or more | Rounded up to the nearest integer greater than 1 + 9/ (frequency ratio of ICLK/ PCLKB) ⁶ | |
| 000A 0214h | USB1 | CFIFO port register | CFIFO | 16 | 8, 16 | 3 to 4 PCLKB | 2, 3 ICLK | |
| 000A 0218h | USB1 | D0FIFO port register | D0FIFO | 16 | 8, 16 | 3 to 4 PCLKB | 2, 3 ICLK | |
| 000A 021Ch | USB1 | D1FIFO port register | D1FIFO | 16 | 8, 16 | 3 to 4 PCLKB | 2, 3 ICLK | |
| 000A 0220h | USB1 | CFIFO port select register | CFIFOSEL | 16 | 16 | 3 to 4 PCLKB | 2, 3 ICLK | |
| 000A 0222h | USB1 | CFIFO port control register | CFIFOCTR | 16 | 16 | 3 to 4 PCLKB | 2, 3 ICLK | |
| 000A 0228h | USB1 | D0FIFO port select register | D0FIFOSEL | 16 | 16 | 3 to 4 PCLKB | 2, 3 ICLK | USBa |
| 000A 022Ah | USB1 | D0FIFO port control register | D0FIFOCTR | 16 | 16 | 3 to 4 PCLKB | 2, 3 ICLK | |
| 000A 022Ch | USB1 | D1FIFO port select register | D1FIFOSEL | 16 | 16 | 3 to 4 PCLKB | 2, 3 ICLK | |
| 000A 022Eh | USB1 | D1FIFO port control register | D1FIFOCTR | 16 | 16 | 3 to 4 PCLKB | 2, 3 ICLK | |

Table 4.1 List of I/O Registers (Address Order) (44/50)

| Address | Module Symbol | Register Name | Register Symbol | Number of Bits | Access Size | Number of Access States | | Related Function |
|------------|---------------|-----------------------------------|-----------------|----------------|-------------|-------------------------|---|------------------|
| | | | | | | ICLK \geq PCLK | ICLK<PCLK | |
| 000A 0230h | USB1 | Interrupt enable register 0 | INTENB0 | 16 | 16 | 9 PCLKB or more | Rounded up to the nearest integer greater than 1 + 9/ (frequency ratio of ICLK/ PCLKB) ⁶ | |
| 000A 0236h | USB1 | BRDY interrupt enable register | BRDYENB | 16 | 16 | 9 PCLKB or more | Rounded up to the nearest integer greater than 1 + 9/ (frequency ratio of ICLK/ PCLKB) ⁶ | |
| 000A 0238h | USB1 | NRDY interrupt enable register | NRDYENB | 16 | 16 | 9 PCLKB or more | Rounded up to the nearest integer greater than 1 + 9/ (frequency ratio of ICLK/ PCLKB) ⁶ | |
| 000A 023Ah | USB1 | BEMP interrupt enable register | BEMPENB | 16 | 16 | 9 PCLKB or more | Rounded up to the nearest integer greater than 1 + 9/ (frequency ratio of ICLK/ PCLKB) ⁶ | |
| 000A 023Ch | USB1 | SOF output configuration register | SOFCFG | 16 | 16 | 9 PCLKB or more | Rounded up to the nearest integer greater than 1 + 9/ (frequency ratio of ICLK/ PCLKB) ⁶ | |
| 000A 0240h | USB1 | Interrupt status register 0 | INTSTS0 | 16 | 16 | 9 PCLKB or more | Rounded up to the nearest integer greater than 1 + 9/ (frequency ratio of ICLK/ PCLKB) ⁶ | |
| 000A 0246h | USB1 | BRDY interrupt status register | BRDYSTS | 16 | 16 | 9 PCLKB or more | Rounded up to the nearest integer greater than 1 + 9/ (frequency ratio of ICLK/ PCLKB) ⁶ | |
| 000A 0248h | USB1 | NRDY interrupt status register | NRDYSTS | 16 | 16 | 9 PCLKB or more | Rounded up to the nearest integer greater than 1 + 9/ (frequency ratio of ICLK/ PCLKB) ⁶ | USBa |
| 000A 024Ah | USB1 | BEMP interrupt status register | BEMPSTS | 16 | 16 | 9 PCLKB or more | Rounded up to the nearest integer greater than 1 + 9/ (frequency ratio of ICLK/ PCLKB) ⁶ | |
| 000A 024Ch | USB1 | Frame number register | FRMNUM | 16 | 16 | 9 PCLKB or more | Rounded up to the nearest integer greater than 1 + 9/ (frequency ratio of ICLK/ PCLKB) ⁶ | |

Table 4.1 List of I/O Registers (Address Order) (45/50)

| Address | Module Symbol | Register Name | Register Symbol | Number of Bits | Access Size | Number of Access States | | Related Function |
|------------|---------------|----------------------------------|-----------------|----------------|-------------|-------------------------|---|------------------|
| | | | | | | ICLK \geq PCLK | ICLK<PCLK | |
| 000A 024Eh | USB1 | Device state changing register | DVCHGR | 16 | 16 | 9 PCLKB or more | Rounded up to the nearest integer greater than 1 + 9/ (frequency ratio of ICLK/ PCLKB) ⁶ | |
| 000A 0250h | USB1 | USB address register | USBADDR | 16 | 16 | 9 PCLKB or more | Rounded up to the nearest integer greater than 1 + 9/ (frequency ratio of ICLK/ PCLKB) ⁶ | |
| 000A 0254h | USB1 | USB request type register | USBREQ | 16 | 16 | 9 PCLKB or more | Rounded up to the nearest integer greater than 1 + 9/ (frequency ratio of ICLK/ PCLKB) ⁶ | |
| 000A 0256h | USB1 | USB request value register | USBVAL | 16 | 16 | 9 PCLKB or more | Rounded up to the nearest integer greater than 1 + 9/ (frequency ratio of ICLK/ PCLKB) ⁶ | |
| 000A 0258h | USB1 | USB request index register | USBINDX | 16 | 16 | 9 PCLKB or more | Rounded up to the nearest integer greater than 1 + 9/ (frequency ratio of ICLK/ PCLKB) ⁶ | |
| 000A 025Ah | USB1 | USB request length register | USBLENG | 16 | 16 | 9 PCLKB or more | Rounded up to the nearest integer greater than 1 + 9/ (frequency ratio of ICLK/ PCLKB) ⁶ | USBa |
| 000A 025Ch | USB1 | DCP configuration register | DCPCFG | 16 | 16 | 9 PCLKB or more | Rounded up to the nearest integer greater than 1 + 9/ (frequency ratio of ICLK/ PCLKB) ⁶ | |
| 000A 025Eh | USB1 | DCP maximum packet size register | DCPMAXP | 16 | 16 | 9 PCLKB or more | Rounded up to the nearest integer greater than 1 + 9/ (frequency ratio of ICLK/ PCLKB) ⁶ | |
| 000A 0260h | USB1 | DCP control register | DCPCTR | 16 | 16 | 9 PCLKB or more | Rounded up to the nearest integer greater than 1 + 9/ (frequency ratio of ICLK/ PCLKB) ⁶ | |
| 000A 0264h | USB1 | Pipe window select register | PIPESEL | 16 | 16 | 9 PCLKB or more | Rounded up to the nearest integer greater than 1 + 9/ (frequency ratio of ICLK/ PCLKB) ⁶ | |

Table 4.1 List of I/O Registers (Address Order) (46/50)

| Address | Module Symbol | Register Name | Register Symbol | Number of Bits | Access Size | Number of Access States | | Related Function |
|------------|---------------|-----------------------------------|-----------------|----------------|-------------|-------------------------|---|------------------|
| | | | | | | ICLK \geq PCLK | ICLK<PCLK | |
| 000A 0268h | USB1 | Pipe configuration register | PIPECFG | 16 | 16 | 9 PCLKB or more | Rounded up to the nearest integer greater than 1 + 9/ (frequency ratio of ICLK/ PCLKB) ⁶ | |
| 000A 026Ch | USB1 | Pipe maximum packet size register | PIPEMAXP | 16 | 16 | 9 PCLKB or more | Rounded up to the nearest integer greater than 1 + 9/ (frequency ratio of ICLK/ PCLKB) ⁶ | |
| 000A 026Eh | USB1 | Pipe cycle control register | PIPEPERI | 16 | 16 | 9 PCLKB or more | Rounded up to the nearest integer greater than 1 + 9/ (frequency ratio of ICLK/ PCLKB) ⁶ | |
| 000A 0270h | USB1 | Pipe 1 control register | PIPE1CTR | 16 | 16 | 9 PCLKB or more | Rounded up to the nearest integer greater than 1 + 9/ (frequency ratio of ICLK/ PCLKB) ⁶ | USBa |
| 000A 0272h | USB1 | Pipe 2 control register | PIPE2CTR | 16 | 16 | 9 PCLKB or more | Rounded up to the nearest integer greater than 1 + 9/ (frequency ratio of ICLK/ PCLKB) ⁶ | |
| 000A 0274h | USB1 | Pipe 3 control register | PIPE3CTR | 16 | 16 | 9 PCLKB or more | Rounded up to the nearest integer greater than 1 + 9/ (frequency ratio of ICLK/ PCLKB) ⁶ | |
| 000A 0276h | USB1 | Pipe 4 control register | PIPE4CTR | 16 | 16 | 9 PCLKB or more | Rounded up to the nearest integer greater than 1 + 9/ (frequency ratio of ICLK/ PCLKB) ⁶ | |
| 000A 0278h | USB1 | Pipe 5 control register | PIPE5CTR | 16 | 16 | 9 PCLKB or more | Rounded up to the nearest integer greater than 1 + 9/ (frequency ratio of ICLK/ PCLKB) ⁶ | |
| 000A 027Ah | USB1 | Pipe 6 control register | PIPE6CTR | 16 | 16 | 9 PCLKB or more | Rounded up to the nearest integer greater than 1 + 9/ (frequency ratio of ICLK/ PCLKB) ⁶ | |
| 000A 027Ch | USB1 | Pipe 7 control register | PIPE7CTR | 16 | 16 | 9 PCLKB or more | Rounded up to the nearest integer greater than 1 + 9/ (frequency ratio of ICLK/ PCLKB) ⁶ | |

Table 4.1 List of I/O Registers (Address Order) (47/50)

| Address | Module Symbol | Register Name | Register Symbol | Number of Bits | Access Size | Number of Access States | | Related Function |
|------------|---------------|--|-----------------|----------------|-------------|-------------------------|---|------------------|
| | | | | | | ICLK \geq PCLK | ICLK<PCLK | |
| 000A 027Eh | USB1 | Pipe 8 control register | PIPE8CTR | 16 | 16 | 9 PCLKB or more | Rounded up to the nearest integer greater than 1 + 9/ (frequency ratio of ICLK/ PCLKB) ⁶ | |
| 000A 0280h | USB1 | Pipe 9 control register | PIPE9CTR | 16 | 16 | 9 PCLKB or more | Rounded up to the nearest integer greater than 1 + 9/ (frequency ratio of ICLK/ PCLKB) ⁶ | USBa |
| 000A 0290h | USB1 | Pipe 1 transaction counter enable register | PIPE1TRE | 16 | 16 | 9 PCLKB or more | Rounded up to the nearest integer greater than 1 + 9/ (frequency ratio of ICLK/ PCLKB) ⁶ | |
| 000A 0292h | USB1 | Pipe 1 transaction counter register | PIPE1TRN | 16 | 16 | 9 PCLKB or more | Rounded up to the nearest integer greater than 1 + 9/ (frequency ratio of ICLK/ PCLKB) ⁶ | |
| 000A 0294h | USB1 | Pipe 2 transaction counter enable register | PIPE2TRE | 16 | 16 | 9 PCLKB or more | Rounded up to the nearest integer greater than 1 + 9/ (frequency ratio of ICLK/ PCLKB) ⁶ | |
| 000A 0296h | USB1 | Pipe 2 transaction counter register | PIPE2TRN | 16 | 16 | 9 PCLKB or more | Rounded up to the nearest integer greater than 1 + 9/ (frequency ratio of ICLK/ PCLKB) ⁶ | |
| 000A 0298h | USB1 | Pipe 3 transaction counter enable register | PIPE3TRE | 16 | 16 | 9 PCLKB or more | Rounded up to the nearest integer greater than 1 + 9/ (frequency ratio of ICLK/ PCLKB) ⁶ | |
| 000A 029Ah | USB1 | Pipe 3 transaction counter register | PIPE3TRN | 16 | 16 | 9 PCLKB or more | Rounded up to the nearest integer greater than 1 + 9/ (frequency ratio of ICLK/ PCLKB) ⁶ | |
| 000A 029Ch | USB1 | Pipe 4 transaction counter enable register | PIPE4TRE | 16 | 16 | 9 PCLKB or more | Rounded up to the nearest integer greater than 1 + 9/ (frequency ratio of ICLK/ PCLKB) ⁶ | |
| 000A 029Eh | USB1 | Pipe 4 transaction counter register | PIPE4TRN | 16 | 16 | 9 PCLKB or more | Rounded up to the nearest integer greater than 1 + 9/ (frequency ratio of ICLK/ PCLKB) ⁶ | USBa |

Table 4.1 List of I/O Registers (Address Order) (48/50)

| Address | Module Symbol | Register Name | Register Symbol | Number of Bits | Access Size | Number of Access States | | Related Function |
|------------|---------------|---|-----------------|----------------|-------------|-------------------------|---|------------------|
| | | | | | | ICLK \geq PCLK | ICLK<PCLK | |
| 000A 02A0h | USB1 | Pipe 5 transaction counter enable register | PIPE5TRE | 16 | 16 | 9 PCLKB or more | Rounded up to the nearest integer greater than 1 + 9/ (frequency ratio of ICLK/ PCLKB) ⁶ | |
| 000A 02A2h | USB1 | Pipe 5 transaction counter register | PIPE5TRN | 16 | 16 | 9 PCLKB or more | Rounded up to the nearest integer greater than 1 + 9/ (frequency ratio of ICLK/ PCLKB) ⁶ | |
| 000A 0400h | USB | Deep standby USB transceiver control/pin monitor register | DPUSR0R | 32 | 32 | 9 PCLKB or more | Rounded up to the nearest integer greater than 1 + 9/ (frequency ratio of ICLK/ PCLKB) ⁶ | |
| 000A 0404h | USB | Deep standby USB suspend/resume interrupt register | DPUSR1R | 32 | 32 | 9 PCLKB or more | Rounded up to the nearest integer greater than 1 + 9/ (frequency ratio of ICLK/ PCLKB) ⁶ | |
| 000A 0500h | PDC | PDC Control Register 0 | PCCR0 | 32 | 32 | 2, 3PCLKA | 2 ICLK | PDC |
| 000A 0504h | PDC | PDC Control Register 1 | PCCR1 | 32 | 32 | 2, 3PCLKA | 2 ICLK | |
| 000A 0508h | PDC | PDC Status Register | PCSR | 32 | 32 | 2, 3PCLKA | 2 ICLK | |
| 000A 050Ch | PDC | PDC Pin Monitor Register | PCMONR | 32 | 32 | 2, 3PCLKA | 2 ICLK | |
| 000A 0510h | PDC | PDC Receive Data Register | PCDR | 32 | 32 | 2, 3PCLKA | 2 ICLK | |
| 000A 0514h | PDC | Vertical Capture Register | VCR | 32 | 32 | 2, 3PCLKA | 2 ICLK | |
| 000A 0518h | PDC | Horizontal Capture Register | HCR | 32 | 32 | 2, 3PCLKA | 2 ICLK | |
| 000C 0000h | EDMAC | EDMAC mode register | EDMR | 32 | 32 | 5, 6 PCLKA | — | EDMAC |
| 000C 0008h | EDMAC | EDMAC transmit request register | EDTRR | 32 | 32 | 5, 6 PCLKA | — | |
| 000C 0010h | EDMAC | EDMAC receive request register | EDRRR | 32 | 32 | 5, 6 PCLKA | — | |
| 000C 0018h | EDMAC | Transmit descriptor list start address register | TDLAR | 32 | 32 | 5, 6 PCLKA | — | |
| 000C 0020h | EDMAC | Receive descriptor list start address register | RDLAR | 32 | 32 | 5, 6 PCLKA | — | |
| 000C 0028h | EDMAC | ETHERC/EDMAC status register | EESR | 32 | 32 | 5, 6 PCLKA | — | |
| 000C 0030h | EDMAC | ETHERC/EDMAC status interrupt permission register | EESIPR | 32 | 32 | 5, 6 PCLKA | — | |
| 000C 0038h | EDMAC | Transmit/receive status copy enable register | TRSCER | 32 | 32 | 5, 6 PCLKA | — | |
| 000C 0040h | EDMAC | Receive missed-frame counter register | RMFCR | 32 | 32 | 5, 6 PCLKA | — | |
| 000C 0048h | EDMAC | Transmit FIFO threshold register | TFTR | 32 | 32 | 5, 6 PCLKA | — | |
| 000C 0050h | EDMAC | FIFO depth register | FDR | 32 | 32 | 5, 6 PCLKA | — | |
| 000C 0058h | EDMAC | Receiving method control register | RMCR | 32 | 32 | 5, 6 PCLKA | — | |
| 000C 0064h | EDMAC | Transmit FIFO underrun counter | TFUCR | 32 | 32 | 5, 6 PCLKA | — | |
| 000C 0068h | EDMAC | Receive FIFO overflow counter | RFOCR | 32 | 32 | 5, 6 PCLKA | — | |
| 000C 006Ch | EDMAC | Independent output signal setting register | IOSR | 32 | 32 | 5, 6 PCLKA | — | EDMAC |
| 000C 0070h | EDMAC | Flow control start FIFO threshold setting register | FCFTR | 32 | 32 | 5, 6 PCLKA | — | |
| 000C 0078h | EDMAC | Receive data padding insert register | RPADIR | 32 | 32 | 5, 6 PCLKA | — | |
| 000C 007Ch | EDMAC | Transmit interrupt setting register | TRIMD | 32 | 32 | 5, 6 PCLKA | — | |
| 000C 00C8h | EDMAC | Receive buffer write address register | RBWAR | 32 | 32 | 5, 6 PCLKA | — | |
| 000C 00CCh | EDMAC | Receive descriptor fetch address register | RDFAR | 32 | 32 | 5, 6 PCLKA | — | |
| 000C 00D4h | EDMAC | Transmit buffer read address register | TBRAR | 32 | 32 | 5, 6 PCLKA | — | |
| 000C 00D8h | EDMAC | Transmit descriptor fetch address register | TDFAR | 32 | 32 | 5, 6 PCLKA | — | |

Table 4.1 List of I/O Registers (Address Order) (49/50)

| Address | Module Symbol | Register Name | Register Symbol | Number of Bits | Access Size | Number of Access States | | Related Function |
|------------|---------------|---|-----------------|----------------|-------------|-------------------------|-----------|------------------|
| | | | | | | ICLK \geq PCLK | ICLK<PCLK | |
| 000C 0100h | ETHERC | ETHERC mode register | ECMR | 32 | 32 | 5, 6 PCLKA | — | ETHERC |
| 000C 0108h | ETHERC | Receive frame length register | RFLR | 32 | 32 | 5, 6 PCLKA | — | |
| 000C 0110h | ETHERC | ETHERC status register | ECSR | 32 | 32 | 5, 6 PCLKA | — | |
| 000C 0118h | ETHERC | ETHERC interrupt permission register | ECSIPR | 32 | 32 | 5, 6 PCLKA | — | |
| 000C 0120h | ETHERC | PHY interface register | PIR | 32 | 32 | 5, 6 PCLKA | — | |
| 000C 0128h | ETHERC | PHY status register | PSR | 32 | 32 | 5, 6 PCLKA | — | |
| 000C 0140h | ETHERC | Random number generation counter upper limit setting register | RDMLR | 32 | 32 | 5, 6 PCLKA | — | |
| 000C 0150h | ETHERC | IPG register | IPGR | 32 | 32 | 5, 6 PCLKA | — | |
| 000C 0154h | ETHERC | Automatic PAUSE frame register | APR | 32 | 32 | 5, 6 PCLKA | — | |
| 000C 0158h | ETHERC | Manual PAUSE frame register | MPR | 32 | 32 | 5, 6 PCLKA | — | |
| 000C 0160h | ETHERC | PAUSE Frame receive counter register | RFCF | 32 | 32 | 5, 6 PCLKA | — | |
| 000C 0164h | ETHERC | Automatic PAUSE frame retransmit count register | TPAUSER | 32 | 32 | 5, 6 PCLKA | — | |
| 000C 0168h | ETHERC | PAUSE frame retransmit counter register | TPAUSECR | 32 | 32 | 5, 6 PCLKA | — | |
| 000C 016Ch | ETHERC | Broadcast frame receive count setting register | BCFRR | 32 | 32 | 5, 6 PCLKA | — | |
| 000C 01C0h | ETHERC | MAC address high register | MAHR | 32 | 32 | 5, 6 PCLKA | — | |
| 000C 01C8h | ETHERC | MAC address low register | MALR | 32 | 32 | 5, 6 PCLKA | — | |
| 000C 01D0h | ETHERC | Transmit retry over counter register | TROCR | 32 | 32 | 5, 6 PCLKA | — | |
| 000C 01D4h | ETHERC | Delayed collision detect counter register | CDCR | 32 | 32 | 5, 6 PCLKA | — | |
| 000C 01D8h | ETHERC | Lost carrier counter register | LCCR | 32 | 32 | 5, 6 PCLKA | — | |
| 000C 01DCh | ETHERC | Carrier not detect counter register | CNDCR | 32 | 32 | 5, 6 PCLKA | — | |
| 000C 01E4h | ETHERC | CRC error frame receive counter register | CEFCR | 32 | 32 | 5, 6 PCLKA | — | |
| 000C 01E8h | ETHERC | Frame receive error counter register | FRECR | 32 | 32 | 5, 6 PCLKA | — | |
| 000C 01ECh | ETHERC | Too-short frame receive counter register | TSFRCR | 32 | 32 | 5, 6 PCLKA | — | |
| 000C 01F0h | ETHERC | Too-long frame receive counter register | TLFRCR | 32 | 32 | 5, 6 PCLKA | — | |
| 000C 01F4h | ETHERC | Residual-bit frame receive counter register | RFCR | 32 | 32 | 5, 6 PCLKA | — | |
| 000C 01F8h | ETHERC | Multicast address frame receive counter register | MAFCR | 32 | 32 | 5, 6 PCLKA | — | |

Table 4.1 List of I/O Registers (Address Order) (50/50)

| Address | Module Symbol | Register Name | Register Symbol | Number of Bits | Access Size | Number of Access States | | Related Function |
|------------|---------------|--|-----------------|----------------|-------------|-------------------------|-----------|--------------------|
| | | | | | | ICLK≥PCLK | ICLK<PCLK | |
| 007F C402h | FLASH | Flash mode register | FMODR | 8 | 8 | 2 to 4 FCLK | 2, 3 ICLK | Flash Memory |
| 007F C410h | FLASH | Flash access status register | FASTAT | 8 | 8 | 2 to 4 FCLK | 2, 3 ICLK | |
| 007F C411h | FLASH | Flash access error interrupt enable register | FAEINT | 8 | 8 | 2 to 4 FCLK | 2, 3 ICLK | |
| 007F C412h | FLASH | Flash ready interrupt enable register | FRDYIE | 8 | 8 | 2 to 4 FCLK | 2, 3 ICLK | |
| 007F C440h | FLASH | E2 DataFlash read enable register 0 | DFLRE0 | 16 | 16 | 2 to 4 FCLK | 2, 3 ICLK | |
| 007F C442h | FLASH | E2 DataFlash read enable register 1 | DFLRE1 | 16 | 16 | 2 to 4 FCLK | 2, 3 ICLK | |
| 007F C450h | FLASH | E2 DataFlash P/E enable register 0 | DFLWE0 | 16 | 16 | 2 to 4 FCLK | 2, 3 ICLK | |
| 007F C452h | FLASH | E2 DataFlash P/E enable register 1 | DFLWE1 | 16 | 16 | 2 to 4 FCLK | 2, 3 ICLK | |
| 007F C454h | FLASH | FCU RAM enable register | FCURAME | 16 | 16 | 2 to 4 FCLK | 2, 3 ICLK | |
| 007F FFB0h | FLASH | Flash status register 0 | FSTATR0 | 8 | 8 | 2 to 4 FCLK | 2, 3 ICLK | |
| 007F FFB1h | FLASH | Flash status register 1 | FSTATR1 | 8 | 8 | 2 to 4 FCLK | 2, 3 ICLK | |
| 007F FFB2h | FLASH | Flash P/E mode entry register | FENTRYR | 16 | 16 | 2 to 4 FCLK | 2, 3 ICLK | |
| 007F FFB4h | FLASH | Flash protection register | FPROTR | 16 | 16 | 2 to 4 FCLK | 2, 3 ICLK | |
| 007F FFB6h | FLASH | Flash reset register | FRESETR | 16 | 16 | 2 to 4 FCLK | 2, 3 ICLK | |
| 007F FFBAh | FLASH | FCU command register | FCMDR | 16 | 16 | 2 to 4 FCLK | 2, 3 ICLK | |
| 007F FFC8h | FLASH | FCU processing switching register | FCPSR | 16 | 16 | 2 to 4 FCLK | 2, 3 ICLK | |
| 007F FFCAh | FLASH | E2 data flash blank check control register | DFLBCCNT | 16 | 16 | 2 to 4 FCLK | 2, 3 ICLK | |
| 007F FFCCh | FLASH | Flash P/E status register | FPESTAT | 16 | 16 | 2 to 4 FCLK | 2, 3 ICLK | |
| 007F FFCEh | FLASH | E2 DataFlash blank check status register | DFLBCSTAT | 16 | 16 | 2 to 4 FCLK | 2, 3 ICLK | |
| 007F FFE8h | FLASH | Peripheral clock notification register | PCKAR | 16 | 16 | 2 to 4 FCLK | 2, 3 ICLK | |
| FEFF FAC0h | FLASH | Unique ID register 0*8 | UIDR0 | 8 | 8 | 1 ICLK | 1 ICLK | |
| FEFF FAC1h | FLASH | Unique ID register 1*8 | UIDR1 | 8 | 8 | 1 ICLK | 1 ICLK | |
| FEFF FAC2h | FLASH | Unique ID register 2*8 | UIDR2 | 8 | 8 | 1 ICLK | 1 ICLK | |
| FEFF FAC3h | FLASH | Unique ID register 3*8 | UIDR3 | 8 | 8 | 1 ICLK | 1 ICLK | |
| FEFF FAC4h | FLASH | Unique ID register 4*8 | UIDR4 | 8 | 8 | 1 ICLK | 1 ICLK | |
| FEFF FAC5h | FLASH | Unique ID register 5*8 | UIDR5 | 8 | 8 | 1 ICLK | 1 ICLK | |
| FEFF FAC6h | FLASH | Unique ID register 6*8 | UIDR6 | 8 | 8 | 1 ICLK | 1 ICLK | |
| FEFF FAC7h | FLASH | Unique ID register 7*8 | UIDR7 | 8 | 8 | 1 ICLK | 1 ICLK | |
| FEFF FAC8h | FLASH | Unique ID register 8*8 | UIDR8 | 8 | 8 | 1 ICLK | 1 ICLK | |
| FEFF FAC9h | FLASH | Unique ID register 9*8 | UIDR9 | 8 | 8 | 1 ICLK | 1 ICLK | |
| FEFF FACAh | FLASH | Unique ID register 10*8 | UIDR10 | 8 | 8 | 1 ICLK | 1 ICLK | |
| FEFF FACBh | FLASH | Unique ID register 11*8 | UIDR11 | 8 | 8 | 1 ICLK | 1 ICLK | |
| FEFF FACCh | FLASH | Unique ID register 12*8 | UIDR12 | 8 | 8 | 1 ICLK | 1 ICLK | |
| FEFF FACDh | FLASH | Unique ID register 13*8 | UIDR13 | 8 | 8 | 1 ICLK | 1 ICLK | |
| FEFF FACEh | FLASH | Unique ID register 14*8 | UIDR14 | 8 | 8 | 1 ICLK | 1 ICLK | |
| FEFF FACFh | FLASH | Unique ID register 15*8 | UIDR15 | 8 | 8 | 1 ICLK | 1 ICLK | |
| FEFF FAD2h | TEMPS | Temperature sensor calibration data register*8 | TSCDRL | 8 | 8 | 1 ICLK | 1 ICLK | Temperature sensor |
| FEFF FAD3h | TEMPS | Temperature sensor calibration data register*8 | TSCDRH | 8 | 8 | 1 ICLK | 1 ICLK | |

- Note 1. When the same output trigger is specified for pulse output groups 2 and 3 by the PPG0.PCR setting, the PPG0.NDRH address is 000881ECh. When different output triggers are specified, the PPG0.NDRH addresses for pulse output groups 2 and 3 are 000881EEh and 000881ECh, respectively.
- Note 2. When the same output trigger is specified for pulse output groups 0 and 1 by the PPG0.PCR setting, the PPG0.NDRL address is 000881EDh. When different output triggers are specified, the PPG0.NDRL addresses for pulse output groups 0 and 1 are 000881EFh and 000881EDh, respectively.
- Note 3. When the same output trigger is specified for pulse output groups 6 and 7 by the PPG1.PCR setting, the PPG1.NDRH address is 000881FCh. When different output triggers are specified, the PPG1.NDRH addresses for pulse output groups 6 and 7 are 000881FEh and 000881FCh, respectively.
- Note 4. When the same output trigger is specified for pulse output groups 4 and 5 by the PPG1.PCR setting, the PPG1.NDRL address is 000881FDh. When different output triggers are specified, the PPG1.NDRL addresses for pulse output groups 4 and 5 are 000881FFh and 000881FDh, respectively.
- Note 5. Odd addresses should not be accessed in 16-bit units. When accessing a register in 16-bit units, access the address of the TMR0 or TMR2 register. Table 27.4 lists register allocation for 16-bit access in the User's manual: Hardware.
- Note 6. When the register is accessed while the USB is operating, a delay may be generated in accessing.
- Note 7. The addresses with odd number cannot be accessed in 16-bit units. 16-bit access to a register should be made to the addresses of the TMOCNL register. Allocation of registers to be accessed in 16-bit units is described in the Table 36.6, Allocation of Registers to be Accessed in 16-bit Units in the User's manual: Hardware.
- Note 8. These registers are only present in the G version.

5. Electrical Characteristics

5.1 Absolute Maximum Ratings

Table 5.1 Absolute Maximum Ratings

Conditions: $V_{SS} = AV_{SS0} = V_{REFL}/V_{REFL0} = V_{SS_USB} = 0\text{ V}$

| Item | Symbol | Value | Unit | |
|---|-------------------|-------------------|-------------|----|
| Power supply voltage | VCC, VCC_USB | -0.3 to +4.6 | V | |
| V _{BATT} power supply voltage | V _{BATT} | -0.3 to +4.6 | V | |
| Input voltage (except for ports for 5 V tolerant*1) | V _{in} | -0.3 to VCC + 0.3 | V | |
| Input voltage (ports for 5 V tolerant*1) | V _{in} | -0.3 to +5.8 | V | |
| Reference power supply voltage | VREFH | -0.3 to VCC + 0.3 | V | |
| Analog power supply voltage | AVCC*2 | -0.3 to +4.6 | V | |
| Analog input voltage | V _{AN} | -0.3 to VCC + 0.3 | V | |
| Operating temperature | D version | T _{opr} | -40 to +85 | °C |
| | G version | | -40 to +105 | °C |
| Storage temperature | T _{stg} | -55 to +125 | °C | |

Caution: Permanent damage to the LSI may result if absolute maximum ratings are exceeded.

Note 1. Ports 07, 12 to 17, 20, 21, 30 to 33, 67, and C0 to C3 are 5 V tolerant.

Note 2. Connect AVCC0 to VCC. When neither the A/D converter nor the D/A converter is in use, do not leave the AVCC0, VREFH/VREFH0, AVSS0, and VREFL/VREFL0 pins open. Connect the AVCC0 and VREFH/VREFH0 pins to VCC, and the AVSS0 and VREFL/VREFL0 pins to VSS, respectively.

5.2 DC Characteristics

Table 5.2 DC Characteristics (1)

Conditions: $V_{CC} = AV_{CC0} = V_{REFH} = V_{CC_USB} = 2.7$ to 3.6 V, $V_{REFH0} = 2.7$ V to AV_{CC0} ,
 $V_{SS} = AV_{SS0} = V_{REFL}/V_{REFL0} = V_{SS_USB} = 0$ V, $T_a = T_{opr}$

| Item | Symbol | Min. | Typ. | Max. | Unit | Test Conditions |
|---|---|---------------------|----------------------|---------------------|---------------------|-----------------|
| Schmitt trigger input voltage | IRQ input pin*1 | V_{IH} | $V_{CC} \times 0.8$ | — | $V_{CC} + 0.3$ | V |
| | MTU input pin*1 | V_{IL} | -0.3 | — | $V_{CC} \times 0.2$ | |
| | TMR input pin*1 | ΔV_T | $V_{CC} \times 0.06$ | — | — | |
| | SCI input pin*1 | | | | | |
| | ADTRG# input pin*1 | | | | | |
| | RES#, NMI | | | | | |
| | RIIC input pin (except for SMBus) | V_{IH} | $V_{CC} \times 0.7$ | — | 5.8 | |
| | | V_{IL} | -0.3 | — | $V_{CC} \times 0.3$ | |
| | | ΔV_T | $V_{CC} \times 0.05$ | — | — | |
| | Ports for 5 V tolerant*2 | V_{IH} | $V_{CC} \times 0.8$ | — | 5.8 | |
| V_{IL} | | -0.3 | — | $V_{CC} \times 0.2$ | | |
| Other input pins excluding ports for 5 V tolerant*3 | V_{IH} | $V_{CC} \times 0.8$ | — | $V_{CC} + 0.3$ | | |
| | V_{IL} | -0.3 | — | $V_{CC} \times 0.2$ | | |
| Input high voltage (except for Schmitt trigger input pin) | MD pin, EMLE | V_{IH} | $V_{CC} \times 0.9$ | — | $V_{CC} + 0.3$ | V |
| | EXTAL, RSPI, EXDMAC, WAIT#, TCK | | $V_{CC} \times 0.8$ | — | $V_{CC} + 0.3$ | |
| | ETHERC | | 2.3 | — | $V_{CC} + 0.3$ | |
| | XCIN | | — | — | $V_{CC} + 0.3$ | |
| | D0 to D31 | | $V_{CC} \times 0.7$ | — | $V_{CC} + 0.3$ | |
| | RIIC (SMBus) | | 2.1 | — | $V_{CC} + 0.3$ | |
| Input low voltage (except for Schmitt trigger input pin) | MD pin, EMLE | V_{IL} | -0.3 | — | $V_{CC} \times 0.1$ | V |
| | EXTAL, RSPI, ETHERC, EXDMAC, WAIT#, TCK | | -0.3 | — | $V_{CC} \times 0.2$ | |
| | XCIN | | -0.3 | — | — | |
| | D0 to D31 | | -0.3 | — | $V_{CC} \times 0.3$ | |
| | RIIC (SMBus) | | -0.3 | — | 0.8 | |

Note 1. V_{IH} characteristics of the pins which are multiplexed with pin functions having 5-V tolerance are those of the pin functions for 5-V tolerance.

Note 2. Ports 07, 12 to 17, 20, 21, 30 to 33, 67, and C0 to C3 are 5 V tolerant.

Note 3. For P32, P31, P30, input as follows when the V_{BATT} power supply is selected.

V_{IH} Min. = $V_{BATT} \times 0.8$, V_{IH} Max. = $V_{BATT} + 0.3$, V_{IL} Min. = -0.3, V_{IL} Max. = $V_{BATT} \times 0.2$

Table 5.3 DC Characteristics (2)

Conditions: $V_{CC} = AV_{CC0} = V_{REFH} = V_{CC_USB} = 2.7$ to 3.6 V, $V_{REFH0} = 2.7$ V to AV_{CC0} ,
 $V_{SS} = AV_{SS0} = V_{REFL}/V_{REFL0} = V_{SS_USB} = 0$ V, $T_a = T_{opr}$

| Item | Symbol | Min. | Typ. | Max. | Unit | Test Conditions |
|---|---|-------------|----------------|------|------------------------|--|
| Output high voltage | All output pins | V_{OH} | $V_{CC} - 0.5$ | — | — | V $I_{OH} = -1$ mA |
| Output low voltage | All output pins (except for RIIC pins, and ETHERC) | V_{OL} | — | — | 0.5 | V $I_{OL} = 1.0$ mA |
| | RIIC pins | | — | — | 0.4 | V $I_{OL} = 3.0$ mA |
| | | | — | — | 0.6 | V $I_{OL} = 6.0$ mA |
| | RIIC pins (only P12 and P13 in channel 0) | V_{OL} | — | — | 0.4 | V $I_{OL} = 15.0$ mA (ICFER.FMPE = 1) |
| | | | — | 0.4 | — | V $I_{OL} = 20.0$ mA (ICFER.FMPE = 1) |
| ETHERC | V_{OL} | — | — | 0.4 | V $I_{OL} = 1.0$ mA | |
| Input leakage current | RES#, MD pin, EMLE*1, NMI | $ I_{in} $ | — | — | 1.0 | μ A $V_{in} = 0$ V $V_{in} = V_{CC}$ |
| Three-state leakage current (off state) | Other than ports for 5 V tolerant | $ I_{TSI} $ | — | — | 1.0 | μ A $V_{in} = 0$ V $V_{in} = V_{CC}$ |
| | Ports for 5 V tolerant | | — | — | 5.0 | μ A $V_{in} = 0$ V $V_{in} = 5.5$ V |
| Input pull-up MOS current | Ports 0 to 2, 30 to 34, 36, 37, 4 to G, J3, J5 | I_p | -10 | — | -300 | μ A $V_{CC} = 2.7$ to 3.6 V $V_{in} = 0$ V |
| Input capacitance | All input pins (except for ports 12, 13, 16, 17, 20, 21, 4, C0, C1, and EMLE) | C_{in} | — | — | 15 | μ F $V_{in} = 0$ V $f = 1$ MHz $T_a = 25^\circ$ C |
| | Ports 12, 13, 16, 17, 20, 21, 4, C0, C1, EMLE | | — | — | 30 | |
| Input pull-down MOS current | EMLE, BSCANP | I_p | 10 | — | 300 | μ A $V_{in} = V_{CC}$ |

Note 1. The input leakage current value at the EMLE pin is only when $V_{in} = 0$ V.

Table 5.4 DC Characteristics (3) (for D and G Versions (-40 ≤ Ta ≤ +85°C))

Conditions: VCC = AVCC0 = VREFH = VCC_USB = VBATT = 2.7 to 3.6 V, VREFH0 = 2.7 V to AVCC0, VSS = AVSS0 = VREFL/VREFL0 = VSS_USB = 0 V, Ta = Topr

| Item | | Symbol | Min. | Typ. | Max. | Unit | Test Conditions | |
|--|---|--|--|------|--|-------------------|--|----|
| Supply current*1 | High-speed operating mode | Max.*2 | — | — | 100 | mA | ICLK = 100 MHz PCLKA = 100MHz PCLKB = 50 MHz FCLK = 50 MHz BCLK = 100MHz | |
| | | Normal*4 | Peripheral function: clock signal supplied*4 | — | 52 | | | — |
| | | | Peripheral function: clock signal stopped*4 | — | 40 | | | — |
| | | Sleep mode | | — | 25 | | | 65 |
| | | All-module-clock-stop mode (reference value) | | — | 20 | | | 38 |
| | | Increased by BGO operation*5 | | — | 15 | | | — |
| | Low-speed operating mode 1*6 | | — | 4 | — | ICLK = 1 MHz | | |
| | Low-speed operating mode 2 | | — | 1 | — | ICLK = 32.768 kHz | | |
| | Software standby mode | | — | 0.2 | 6 | | | |
| | Deep software standby mode | Power supplied to RAM and USB resume detecting unit | — | 22 | 200 | μA | | |
| | | | Power not supplied to RAM and USB resume detecting unit | — | 21 | | | 60 |
| | | Power-on reset circuit and low-power | | — | 6.2 | | | 28 |
| | | Increase when the RTC is operating | When a crystal oscillator for low clock loads is in use | — | 1.0 | | | — |
| | | | When a crystal oscillator for standard clock loads is in use | — | 3.0 | | | — |
| | | RTC operating while VCC is off (with the battery backup function, only the RTC and sub-clock oscillator operate) | When a crystal oscillator for low clock loads is in use | — | 0.9 | | | — |
| When a crystal oscillator for standard clock loads is in use | — | | 1.6 | — | V _{BATT} = 3.3 V, VCC = 0V | | | |
| | — | | 1.7 | — | V _{BATT} = 2.0 V (for products with 100 pins or more), V _{BATT} = 2.3 V (for the 64-pin product), VCC = 0V | | | |
| | | — | 3.3 | — | V _{BATT} = 3.3 V, VCC = 0V | | | |
| Analog power supply current*7 | During 12-bit A/D conversion (including temperature sensor) | | I _{AVCC0} | — | 2.3 | 3.2 | mA | |
| | During 10-bit A/D conversion | | I _{VREFH} *9 | — | 1.0 | 1.65 | mA | |
| | During D/A conversion (per unit) | | | — | 0.7 | 1.0 | mA | |
| | Waiting for A/D, D/A conversion (all units)*10 | | — | — | 25 | 35 | μA | |
| | A/D, D/A converter in standby mode (all units)*10 | | — | — | 0.1 | 4.0 | μA | |
| Reference power supply current | During 12-bit A/D conversion | | I _{VREFH0} | — | 0.6 | 0.7 | mA | |
| | Waiting for 12-bit A/D conversion (per unit) | | | — | 0.5 | 0.6 | mA | |
| | 12-bit A/D converter in standby mode (per unit) | | | — | 0.1 | 2.0 | μA | |

Table 5.4 DC Characteristics (3) (for D and G Versions (-40 ≤ Ta ≤ +85°C))

Conditions: VCC = AVCC0 = VREFH = VCC_USB = V_{BATT} = 2.7 to 3.6 V, VREFH0 = 2.7 V to AVCC0,
VSS = AVSS0 = VREFL/VREFL0 = VSS_USB = 0 V, T_a = T_{opr}

| Item | Symbol | Min. | Typ. | Max. | Unit | Test Conditions |
|------------------------|------------------|------|------|-------|------|-----------------|
| RAM standby voltage | V _{RAM} | 2.7 | — | — | V | |
| VCC rising gradient | SrVCC | 8.4 | — | 20000 | μs/V | |
| VCC falling gradient*8 | SfVCC | 8.4 | — | — | μs/V | |

Note 1. Supply current values are with all output pins unloaded and all input pull-up MOSs in the off state.

Note 2. Measured with clocks supplied to the peripheral functions. This does not include the BGO operation.

Note 3. I_{CC} depends on f (ICLK) as follows. (ICLK:PCLK:BCLK:BCLK pin = 8:4:4:2)

I_{CC} Max. = 0.87 × f + 13 (max. operation in high-speed operating mode)

I_{CC} Typ. = 0.35 × f + 5 (normal operation in high-speed operating mode)

I_{CC} Typ. = 1.0 × f + 3 (low-speed operating mode 1)

I_{CC} Max. = 0.53 × f + 12 (sleep mode)

Note 4. This does not include the BGO operation.

Note 5. This is the increase for programming or erasure of the ROM or flash memory for data storage during program execution.

Note 6. Supply of the clock signal to peripherals is stopped in this state. This does not include the BGO operation.

Note 7. The reference power supply current is included in the power supply current value for 10-bit A/D conversion and D/A conversion.

Note 8. When V_{BATT} is used

Note 9. The current values for 10-bit A/D converter and 10-bit D/A converter are included in the current from the VREFH pin.

Note 10. The values are the sum of I_{AVCC0} and I_{VREFH}.

Table 5.5 DC Characteristics (4) (for G Version (+85 < Ta ≤ +105°C))

Conditions: VCC = AVCC0 = VREFH = VCC_USB = V_{BATT} = 2.7 to 3.6 V, VREFH0 = 2.7 V to AVCC0,
VSS = AVSS0 = VREFL/VREFLO = VSS_USB = 0 V, T_a = T_{opr}

| Item | | Symbol | Min. | Typ. | Max. | Unit | Test Conditions | |
|--|--|---|--|------|--|-------------------------------------|--|----|
| Supply current*1 | High-speed operating mode | Max.*2 | — | — | 115 | mA | ICLK = 100 MHz PCLKA = 100MHz PCLKB = 50 MHz FCLK = 50 MHz BCLK = 100MHz | |
| | | Normal*4 | Peripheral function: clock signal supplied*4 | — | 52 | | | — |
| | | | Peripheral function: clock signal stopped*4 | — | 40 | | | — |
| | | Sleep mode | | — | 25 | | | 80 |
| | | All-module-clock-stop mode (reference value) | | — | 20 | | | 53 |
| | | Increased by BGO operation*5 | | — | 15 | | | — |
| | Low-speed operating mode 1*6 | | — | 4 | — | ICLK = 1 MHz | | |
| | Low-speed operating mode 2 | | — | 1 | — | ICLK = 32.768 kHz | | |
| | Software standby mode | | — | 0.2 | 9 | | | |
| | Deep software standby mode | Power supplied to RAM and USB resume detecting unit | | — | 22 | 200 | μA | |
| | | Power not supplied to RAM and USB resume detecting unit | Power-on reset circuit and low-power consumption function disabled | — | 21 | 60 | | |
| | | | Power-on reset circuit and low-power consumption function enabled | — | 6.2 | 28 | | |
| | | Increase when the RTC is operating | When a crystal oscillator for low clock loads is in use | — | 1.0 | — | | |
| When a crystal oscillator for standard clock loads is in use | | | — | 3.0 | — | | | |
| RTC operating while VCC is off (with the battery backup function, only the RTC and sub-clock oscillator operate) | | When a crystal oscillator for low clock loads is in use | — | 0.9 | — | V _{BATT} = 2.0 V, VCC = 0V | | |
| | When a crystal oscillator for standard clock loads is in use | — | 1.6 | — | V _{BATT} = 3.3 V, VCC = 0V | | | |
| | | — | 1.7 | — | V _{BATT} = 2.0 V (for products with 100 pins or more), V _{BATT} = 2.3 V (for the 64-pin product), VCC = 0V | | | |
| | | — | 3.3 | — | V _{BATT} = 3.3 V, VCC = 0V | | | |
| Analog power supply current*7 | During 12-bit A/D conversion (including temperature sensor) | | I _{AVCC0} | — | 2.3 | 3.2 | mA | |
| | During 10-bit A/D conversion | | I _{VREFH} *9 | — | 1.0 | 1.65 | | |
| | During D/A conversion (per unit) | | | — | 0.7 | 1.0 | | |
| | Waiting for A/D, D/A conversion (all units)*10 | | — | — | 25 | 35 | | μA |
| | A/D, D/A converter in standby mode (all units)*10 | | | — | 0.1 | 5 | | μA |
| Reference power supply current | During 12-bit A/D conversion | | I _{VREFH0} | — | 0.6 | 0.7 | mA | |
| | Waiting for 12-bit A/D conversion (per unit) | | | — | 0.5 | 0.6 | | |
| | 12-bit A/D converter in standby mode (per unit) | | | — | 0.1 | 2.0 | | μA |
| RAM standby voltage | | V _{RAM} | 2.7 | — | — | V | | |
| VCC rising gradient | | SrVCC | 8.4 | — | 20000 | μs/V | | |
| VCC falling gradient*8 | | SfVCC | 8.4 | — | — | μs/V | | |

- Note 1. Supply current values are with all output pins unloaded and all input pull-up MOSs in the off state.
- Note 2. Measured with clocks supplied to the peripheral functions. This does not include the BGO operation.
- Note 3. I_{CC} depends on f (ICLK) as follows. (ICLK:PCLK:BCLK:BCLK pin = 8:4:4:2)
 I_{CC} Max. = $0.87 \times f + 13$ (max. operation in high-speed operating mode)
 I_{CC} Typ. = $0.35 \times f + 5$ (normal operation in high-speed operating mode)
 I_{CC} Typ. = $1.0 \times f + 3$ (low-speed operating mode 1)
 I_{CC} Max. = $0.53 \times f + 12$ (sleep mode)
- Note 4. This does not include the BGO operation.
- Note 5. This is the increase for programming or erasure of the ROM or flash memory for data storage during program execution.
- Note 6. Supply of the clock signal to peripherals is stopped in this state. This does not include the BGO operation.
- Note 7. The reference power supply current is included in the power supply current value for 10-bit A/D conversion and D/A conversion.
- Note 8. When V_{BATT} is used
- Note 9. The current values for 10-bit A/D converter and 10-bit D/A converter are included in the current from the VREFH pin.
- Note 10. The values are the sum of I_{AVCC0} and I_{VREFH} .

Table 5.6 DC Characteristics (4)

Conditions: $V_{CC} = AVCC0 = VREFH = VCC_USB = 2.7$ to 3.6 V, $VREFH0 = 2.7$ V to $AVCC0$,
 $VSS = AVSS0 = VREFL/VREFLO = VSS_USB = 0$ V, $T_a = T_{opr}$

| Item | Symbol | Min. | Typ. | Max. | Unit | Test Conditions |
|---------------------------------------|--------|------|------|------|------|-----------------|
| Permissible total power consumption*1 | P_d | — | — | 380 | mW | *2 |

Note 1. This is the total power consumption of the chip as a whole (including the power consumed by the output buffers).

Note 2. Contact a Renesas sales office or agent regarding further details of the conditions of measurement.

Table 5.7 Permissible Output Currents

Conditions: $V_{CC} = AVCC0 = VREFH = VCC_USB = 2.7$ to 3.6 V, $VREFH0 = 2.7$ V to $AVCC0$,
 $VSS = AVSS0 = VREFL/VREFLO = VSS_USB = 0$ V, $T_a = T_{opr}$

| Item | | Symbol | Min. | Typ. | Max. | Unit | |
|--|--------------------------|--------------|-----------------|------|------|------|----|
| Permissible output low current (average value per pin) | All output pins*1 | Normal drive | I_{OL} | — | — | 2.0 | mA |
| | All output pins*2 | High drive | I_{OL} | | | 3.8 | mA |
| Permissible output low current (max. value per pin) | All output pins*1 | Normal drive | I_{OL} | — | — | 4.0 | mA |
| | All output pins*2 | High drive | I_{OL} | | | 7.6 | mA |
| Permissible output low current (total) | Total of all output pins | | ΣI_{OL} | — | — | 80 | mA |
| Permissible output high current (average value per pin) | All output pins*1 | Normal drive | I_{OH} | — | — | -2.0 | mA |
| | USB_DPUPE pin*2 | High drive | I_{OH} | — | — | -3.8 | mA |
| Permissible output high current (max. value per pin) | All output pins*1 | Normal drive | I_{OH} | — | — | -4.0 | mA |
| | All output pins*2 | High drive | I_{OH} | — | — | -7.6 | mA |
| Permissible output high current (total) | Total of all output pins | | ΣI_{OH} | — | — | -80 | mA |

Caution: To protect the LSI's reliability, the output current values should not exceed the values in this table.

Note 1. This is the value when normal driving ability is set with a pin for which normal driving ability is selectable.

Note 2. This is the value when high driving ability is set with a pin for which normal driving ability is selectable or the value of the pin to which high driving ability is fixed.

5.3 AC Characteristics

Table 5.8 Operation Frequency Value (High-Speed Operating Mode)

Conditions: $V_{CC} = AVCC0 = VREFH = VCC_USB = V_{BATT} = 2.7$ to 3.6 V, $VREFH0 = 2.7$ V to $AVCC0$,
 $VSS = AVSS0 = VREFL/VREFL0 = VSS_USB = 0$ V, $T_a = T_{opr}$

| Item | | Symbol | Min. | Typ. | Max. | Unit | |
|---------------------|---------------------------------|--------|------------------------------------|------|------|------|-----|
| Operation frequency | System clock (ICLK) | f | —*1 | — | 100 | MHz | |
| | Peripheral module clock (PCLKA) | | —*1 | — | 100 | | |
| | Peripheral module clock (PCLKB) | | —*2 | — | 50 | | |
| | FlashIF clock (FCLK) | | —*3 | — | 50 | | |
| | External bus clock (BCLK) | | Packages with 177 to 144 pins | — | — | | 100 |
| | | | Packages with 100 pins or less | — | — | | 50 |
| | BCLK pin output | | Packages with 177 to 144 pins | — | — | | 50 |
| | | | Packages with 100 pins or less | — | — | | 25 |
| | SDRAM clock (SDCLK) | | Packages with 177 to 144 pins only | — | — | | 50 |
| | SDCLK pin output | | Packages with 177 to 144 pins only | — | — | | 50 |
| | USB clock (UCLK) | | — | — | 48 | | |
| IEBUS clock (IECLK) | — | — | 44.03 | | | | |

Note 1. The ICLK and PCLKA frequencies must be the same and at least 12.5 MHz if the Ethernet controller is in use

Note 2. The PCLKB must run at a frequency of at least 24 MHz if the USB is in use.

Note 3. The FCLK must run at a frequency of at least 4 MHz when changing the ROM or E2 DataFlash memory contents.

Table 5.9 Operation Frequency Value (Low-Speed Operating Mode 1)

Conditions: $V_{CC} = AVCC0 = VREFH = VCC_USB = V_{BATT} = 2.7$ to 3.6 V, $VREFH0 = 2.7$ V to $AVCC0$,
 $VSS = AVSS0 = VREFL/VREFL0 = VSS_USB = 0$ V, $T_a = T_{opr}$

| Item | | Symbol | Min. | Typ. | Max. | Unit | |
|---------------------|---------------------------------|--------|------------------------------------|------|------|------|---|
| Operation frequency | System clock (ICLK) | f | — | — | 1 | MHz | |
| | Peripheral module clock (PCLKA) | | — | — | 1 | | |
| | Peripheral module clock (PCLKB) | | — | — | 1 | | |
| | FlashIF clock (FCLK) | | — | — | 1 | | |
| | External bus clock (BCLK) | | Packages with 177 to 144 pins | — | — | | 1 |
| | | | Packages with 100 pins or less | — | — | | 1 |
| | BCLK pin output | | Packages with 177 to 144 pins | — | — | | 1 |
| | | | Packages with 100 pins or less | — | — | | 1 |
| | SDRAM clock (SDCLK) | | Packages with 177 to 144 pins only | — | — | | 1 |
| | SDCLK pin output | | Packages with 177 to 144 pins only | — | — | | 1 |
| | USB clock (UCLK) | | — | — | 1 | | |
| IEBUS clock (IECLK) | — | — | 1 | | | | |

Table 5.10 Operation Frequency Value (Low-Speed Operating Mode 2)

Conditions: $V_{CC} = AVCC0 = VREFH = VCC_USB = V_{BATT} = 2.7$ to 3.6 V, $VREFH0 = 2.7$ V to $AVCC0$,
 $VSS = AVSS0 = VREFL/VREFL0 = VSS_USB = 0$ V, $T_a = T_{opr}$

| Item | | Symbol | Min. | Typ. | Max. | Unit | |
|---------------------|---------------------------------|------------------------------------|------|------|--------|------|--------|
| Operation frequency | System clock (ICLK) | f | 32 | — | 143.75 | kHz | |
| | Peripheral module clock (PCLKA) | | — | — | 143.75 | | |
| | Peripheral module clock (PCLKB) | | — | — | 143.75 | | |
| | FlashIF clock (FCLK) | | 32 | — | 143.75 | | |
| | External bus clock (BCLK) | Packages with 177 to 144 pins | | — | — | | 143.75 |
| | | Packages with 100 pins or less | | — | — | | 143.75 |
| | BCLK pin output | Packages with 177 to 144 pins | | — | — | | 143.75 |
| | | Packages with 100 pins or less | | — | — | | 143.75 |
| | SDRAM clock (SDCLK) | Packages with 177 to 144 pins only | | — | — | | 143.75 |
| | SDCLK pin output | Packages with 177 to 144 pins only | | — | — | | 143.75 |
| USB clock (UCLK) | | | — | — | 143.75 | | |
| IEBUS clock (IECLK) | | | — | — | 143.75 | | |

5.3.1 Reset Timing

Table 5.11 Reset Timing

Conditions: $V_{CC} = AVCC0 = VREFH = VCC_USB = V_{BATT} = 2.7$ to 3.6 V, $VREFH0 = 2.7$ V to $AVCC0$,
 $VSS = AVSS0 = VREFL/VREFL0 = VSS_USB = 0$ V, $T_a = T_{opr}$

| Item | | Symbol | Min. | Typ. | Max. | Unit | Test Conditions |
|--|--|-------------|------|------|-----------|------------|-----------------|
| RES# pulse width | Power-on | t_{RESWP} | 2 | — | — | ms | Figure 5.1 |
| | Deep software standby mode | t_{RESWD} | 1 | — | — | ms | Figure 5.2 |
| | Software standby mode, low-speed operating mode 2 | t_{RESWS} | 1 | — | — | ms | |
| | Programming or erasure of the ROM or E2 data-flash memory or blank checking of the E2 DataFlash memory | t_{RESW} | 200 | — | — | μ s | |
| | Other than above | t_{RESW} | 200 | — | — | μ s | |
| Wait time after RES# cancellation | t_{RESWT} | 59 | — | 60 | t_{cyc} | Figure 5.1 | |
| Internal reset time (independent watchdog timer reset, watchdog timer reset, software reset) | t_{RESW2} | 112 | — | 120 | t_{cyc} | | |

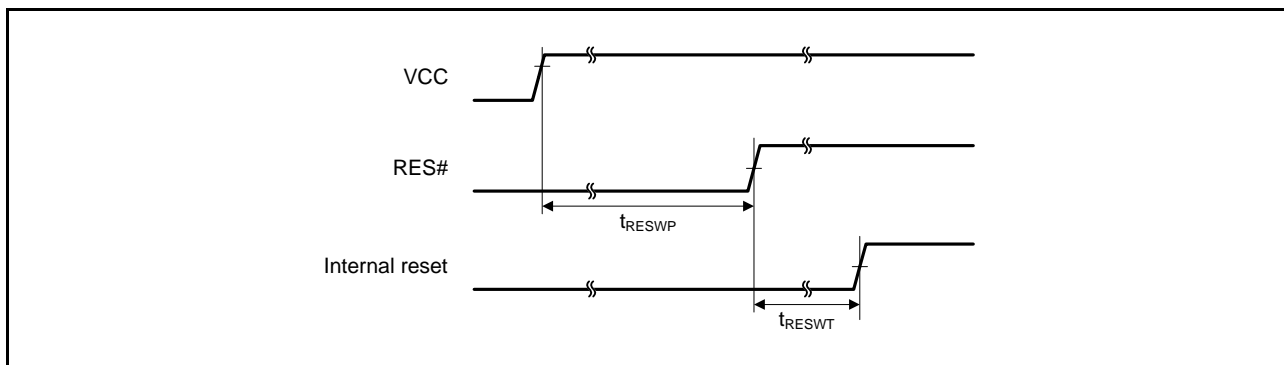


Figure 5.1 Reset Input Timing at Power-On

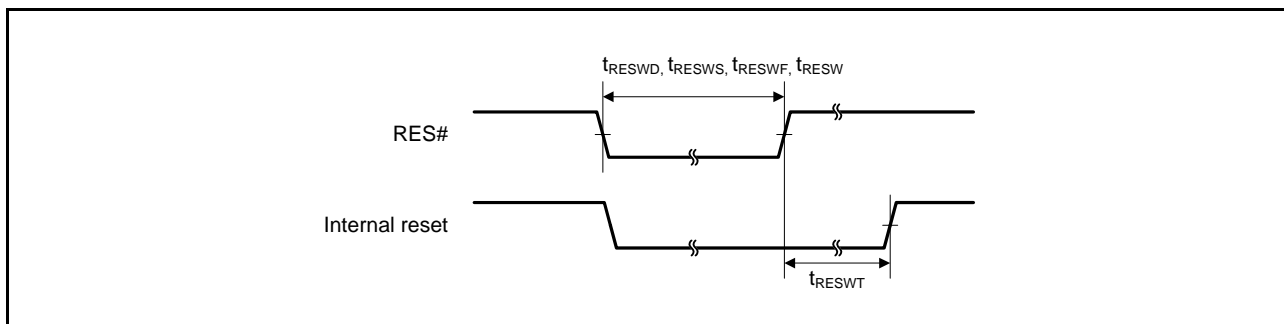


Figure 5.2 Reset Input Timing

5.3.2 Clock Timing

Table 5.12 Clock Timing (Except for Sub-Clock Related)

Conditions: $V_{CC} = AV_{CC0} = V_{REFH} = V_{CC_USB} = V_{BATT} = 2.7$ to 3.6 V, $V_{REFH0} = 2.7$ V to AV_{CC0} ,
 $V_{SS} = AV_{SS0} = V_{REFL}/V_{REFL0} = V_{SS_USB} = 0$ V, $T_a = T_{opr}$

| Item | | Symbol | Min. | Typ. | Max. | Unit | Test Conditions |
|---|---|-----------------|--------|------|--------------------------|---------|-----------------|
| BCLK pin output cycle time | Packages with 177 to 144 pins | t_{Bcyc} | 20 | — | — | ns | Figure 5.3 |
| | Packages with 100 pins or less | | 40 | — | — | ns | |
| BCLK pin output high pulse width | | t_{CH} | 5 | — | — | ns | |
| BCLK pin output low pulse width | | t_{CL} | 5 | — | — | ns | |
| BCLK pin output rising time | | t_{Cr} | — | — | 5 | ns | |
| BCLK pin output falling time | | t_{Cf} | — | — | 5 | ns | |
| SDCLK pin output cycle time | only 177 to 144 pin | t_{Bcyc} | 20 | — | — | ns | |
| SDCLK pin output high pulse width | | t_{CH} | 5 | — | — | ns | |
| SDCLK pin output low pulse width | | t_{CH} | 5 | — | — | ns | |
| SDCLK pin output rising time | | t_{CH} | — | — | 5 | ns | |
| SDCLK pin output falling time | | t_{CH} | — | — | 5 | ns | |
| EXTAL external clock input cycle time | | t_{EXcyc} | 50 | — | — | ns | Figure 5.4 |
| EXTAL external clock input high pulse width | | t_{EXH} | 20 | — | — | ns | |
| EXTAL external clock input low pulse width | | t_{EXL} | 20 | — | — | ns | |
| EXTAL external clock rising time | | t_{EXr} | — | — | 5 | ns | |
| EXTAL external clock falling time | | t_{EXf} | — | — | 5 | ns | |
| EXTAL external clock input wait time*1 | | t_{EXWT} | 1 | — | — | ms | |
| Main clock frequency | | f_{MAIN} | 4 | — | 16 | MHz | |
| Main clock oscillator start-up time | | $t_{MAINOSC}$ | — | — | —*3 | ms | Figure 5.5 |
| Main clock oscillation stabilization wait time | | $t_{MAINOSCWT}$ | — | — | —*4 | ms | |
| LOCO and IWDTCCLK clock cycle time | | t_{cyc} | 6.96 | 8 | 9.4 | μ s | |
| LOCO and IWDTCCLK clock oscillation frequency | | f_{LOCO} | 106.25 | 125 | 143.75 | kHz | |
| LOCO and IWDTCCLK clock oscillation stabilization wait time | | t_{LOCOWT} | — | — | 20 | μ s | Figure 5.6 |
| HOCO clock oscillator oscillation frequency | | f_{HOCO} | 45 | 50 | 55 | MHz | |
| HOCO clock oscillation stabilization wait time 1*2 | | $t_{HOCOWT1}$ | — | — | 1.8 | ms | Figure 5.7 |
| HOCO clock oscillation stabilization wait time 2 | | $t_{HOCOWT2}$ | — | — | 2.0 | ms | Figure 5.8 |
| HOCO clock power supply settling time | | t_{HOCOP} | — | — | 1 | ms | Figure 5.9 |
| PLL clock frequency | | f_{PLL} | 104 | — | 200 | MHz | |
| PLL lock time | PLL operation started after main clock oscillation has settled | t_{PLL1} | — | — | 500 | μ s | Figure 5.10 |
| PLL clock oscillation stabilization wait time | | t_{PLLWT1} | — | — | —*5 | ms | |
| PLL lock time | PLL operation started before main clock oscillation has settled | t_{PLL2} | — | — | $t_{MAINOSC} + t_{PLL1}$ | ms | Figure 5.11 |
| PLL clock oscillation stabilization wait time | | t_{PLLWT2} | — | — | —*5 | ms | |

- Note 1. This is the time until the clock is used after setting P36 and P37 as inputs, and then clearing the main clock oscillator stop bit (MOSCCR.MOSTP) to 0 (selecting operation).
- Note 2. This is the time until the frequency of oscillation by the HOCO (fHOCO) reaches the range for guaranteed operation after release from the reset state.
- Note 3. When using a main clock, ask the manufacturer of the oscillator to evaluate its oscillation. Refer to the results of evaluation provided by the manufacturer for the oscillation stabilization time.
- Note 4. The number of cycles n selected by the value of the MOSCWTCR.MSTS[4:0] bits determines the main-clock oscillation stabilization waiting time in accord with the formula below.

$$t_{\text{MAINOSCWT}} = t_{\text{MAINOSC}} + \frac{n + 16384}{f_{\text{MAIN}}}$$

- Note 5. The number of cycles n selected by the value of the PLLWTCR.PSTS[4:0] bits determines the PLL-clock oscillation stabilization waiting time in accord with the formula below.

$$t_{\text{PLLWT1}} = t_{\text{PLL1}} + \frac{n + 131072}{f_{\text{PLL}}}$$

$$t_{\text{PLLWT2}} = t_{\text{PLL2}} + \frac{n + 131072}{f_{\text{PLL}}} = t_{\text{MAINOSC}} + t_{\text{PLL1}} + \frac{n + 131072}{f_{\text{PLL}}}$$

Table 5.13 Clock Timing (Sub-Clock Related)

Conditions: $V_{CC} = AV_{CC0} = V_{REFH} = V_{CC_USB} = 2.7$ to 3.6 V, $V_{REFH0} = 2.7$ V to AV_{CC0} , $V_{BATT} = 2.0$ to 3.6 V (for products with 100 pins or more), $V_{BATT} = 2.3$ to 3.6 V (for the 64-pin product), $V_{SS} = AV_{SS0} = V_{REFL}/V_{REFL0} = V_{SS_USB} = 0$ V, $T_a = T_{opr}$

| Item | Symbol | Min. | Typ. | Max. | Unit | Test Conditions |
|--|-----------------|------|--------|------|------|-----------------|
| Sub-clock frequency | f_{SUB} | — | 32.768 | — | kHz | |
| Sub-clock oscillator start-up time | t_{SUBOSC} | — | — | *1 | | Figure 5.12 |
| Sub-clock oscillation stabilization wait offset time*3 | $t_{SUBOSCWT0}$ | 1.8 | — | 2.6 | s | |
| Sub-clock oscillation stabilization wait time | $t_{SUBOSCWT}$ | — | — | *2 | s | |

Note 1. When using a sub-clock, ask the manufacturer of the oscillator to evaluate its oscillation. Refer to the results of evaluation provided by the manufacturer for the oscillation stabilization time.

Note 2. The number of cycles n selected by the value of the $SOSCWT[4:0]$ bits determines the sub-clock oscillation stabilization waiting time in accord with the formula below.

$$t_{SUBOSCWT} = \max(t_{SUBOSC}, t_{SUBOSCWT0}) + \frac{n}{f_{SUB}}$$

The notation “ $\max(t_{SUBOSC}, t_{SUBOSCWT0})$ ” indicates whichever is higher of t_{SUBOSC} and $t_{SUBOSCWT0}$.

Note 3. The minimum value and maximum value of the sub-clock oscillation stabilization wait offset time ($t_{SUBOSCWT0}$) is the references only for 100-pin or more products. For 64-pin products, consider the value of $t_{SUBOSCWT0}$ to be 0.

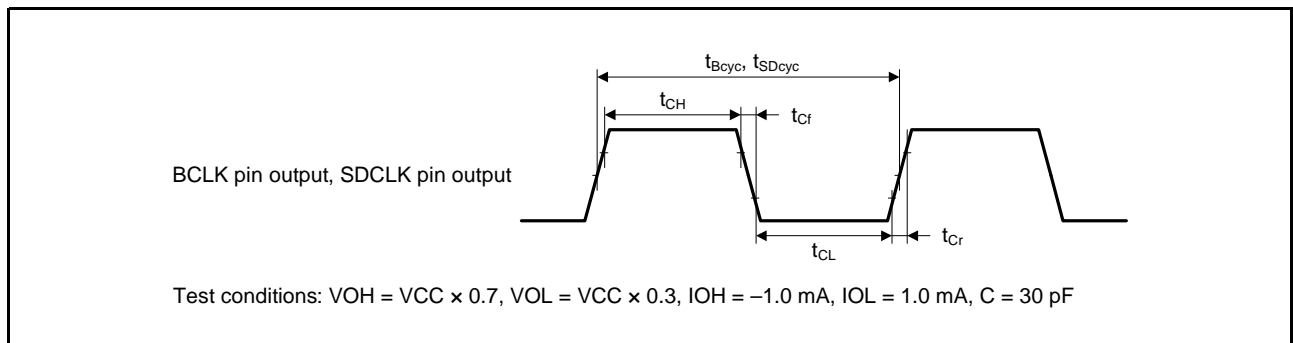


Figure 5.3 BCLK Pin Output, SDCLK Pin Output Timing

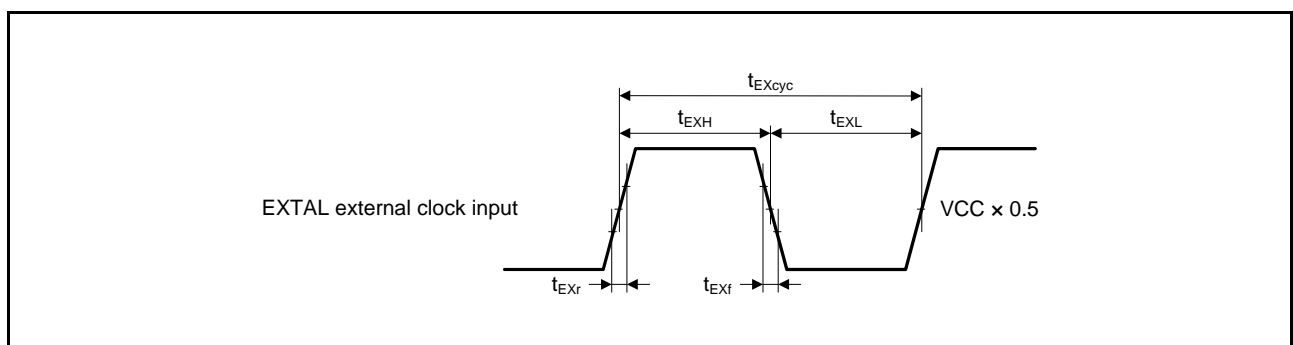


Figure 5.4 EXTAL External Clock Input Timing

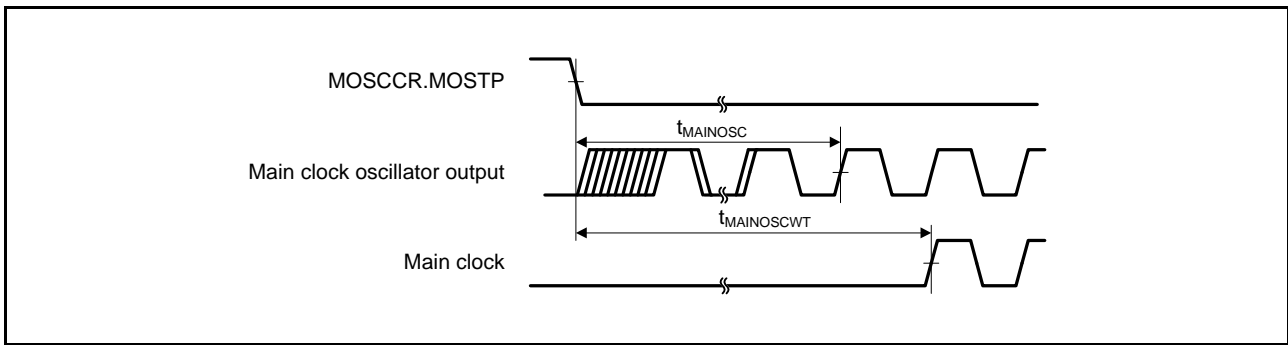


Figure 5.5 Main Clock Oscillation Start Timing

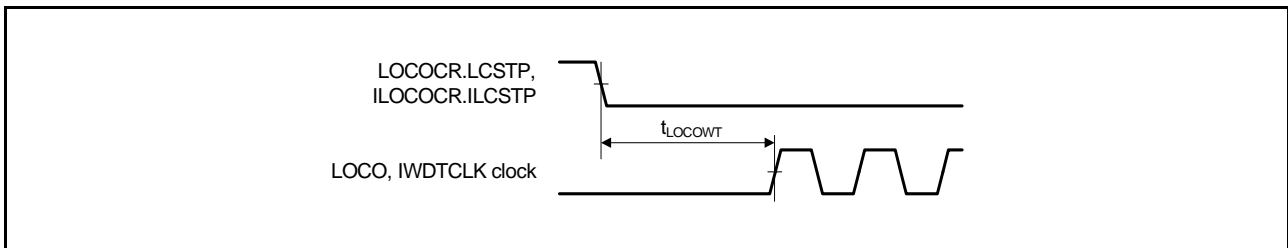


Figure 5.6 LOCO, IWDTCLK Oscillation Start Timing

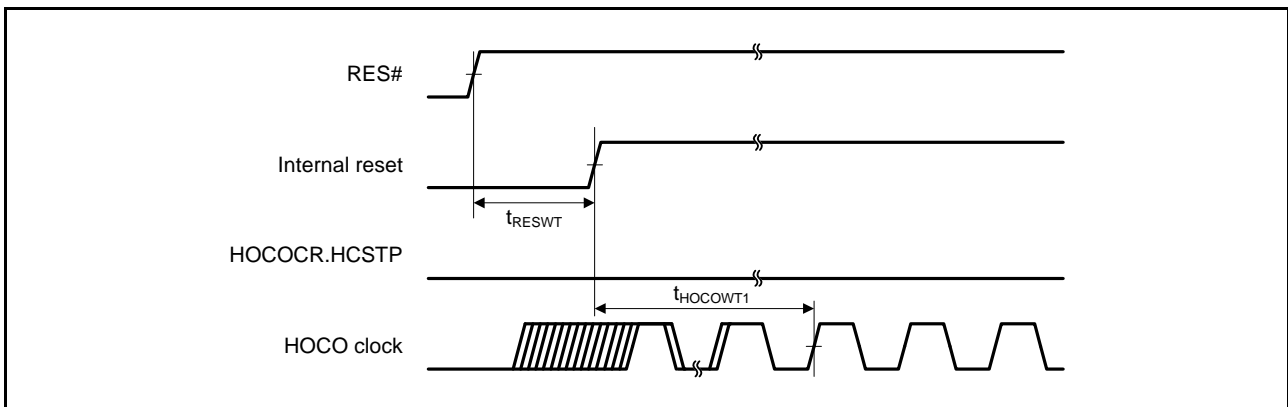


Figure 5.7 HOCO Oscillation Start Timing (After Reset is Canceled by Setting the OFS1.HOCOEN Bit to 0)

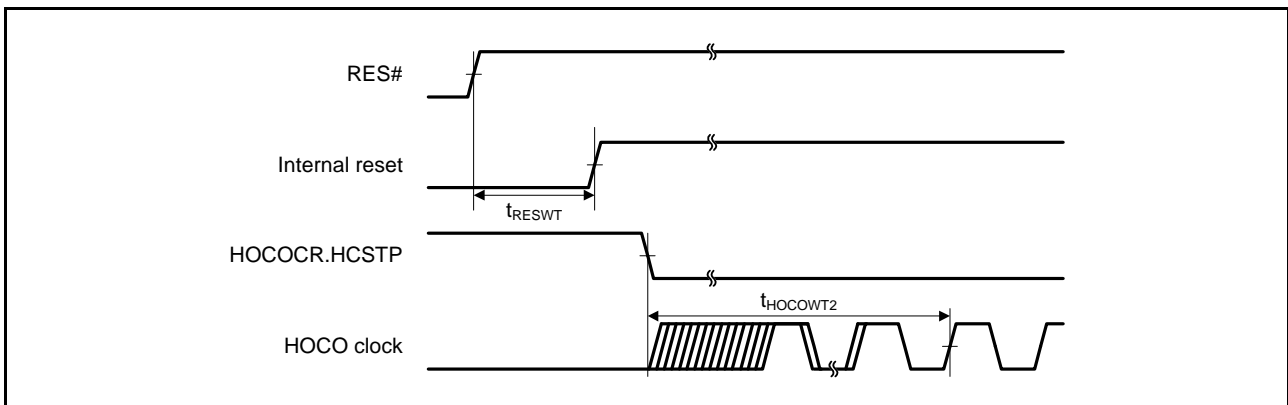


Figure 5.8 HOCO Clock Oscillation Start Timing (Oscillation is Started by Setting the HOCOEN Bit)

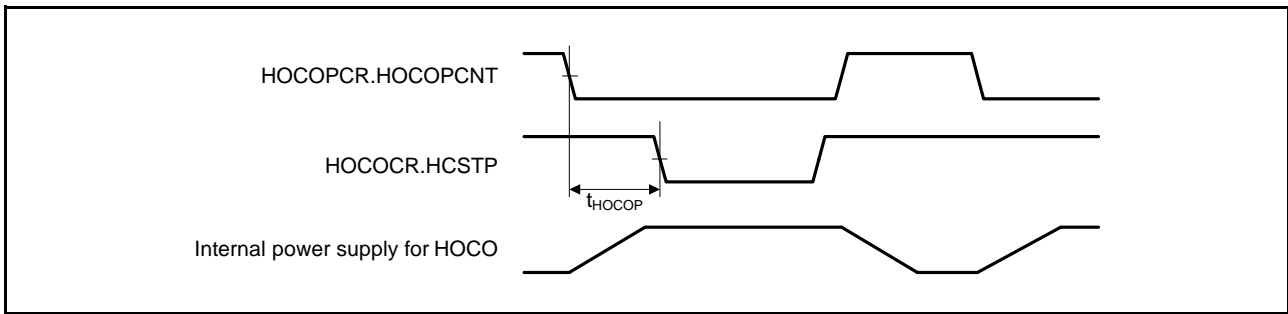


Figure 5.9 HOCO Power Supply Control Timing

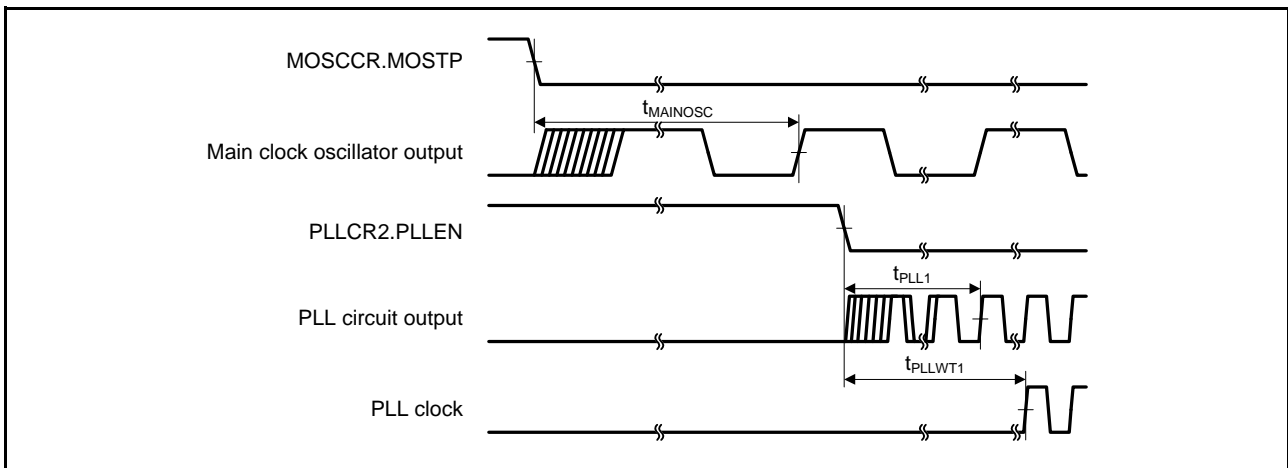


Figure 5.10 PLL Clock Oscillation Start Timing (PLL is Operated after Main Clock Oscillation Has Settled)

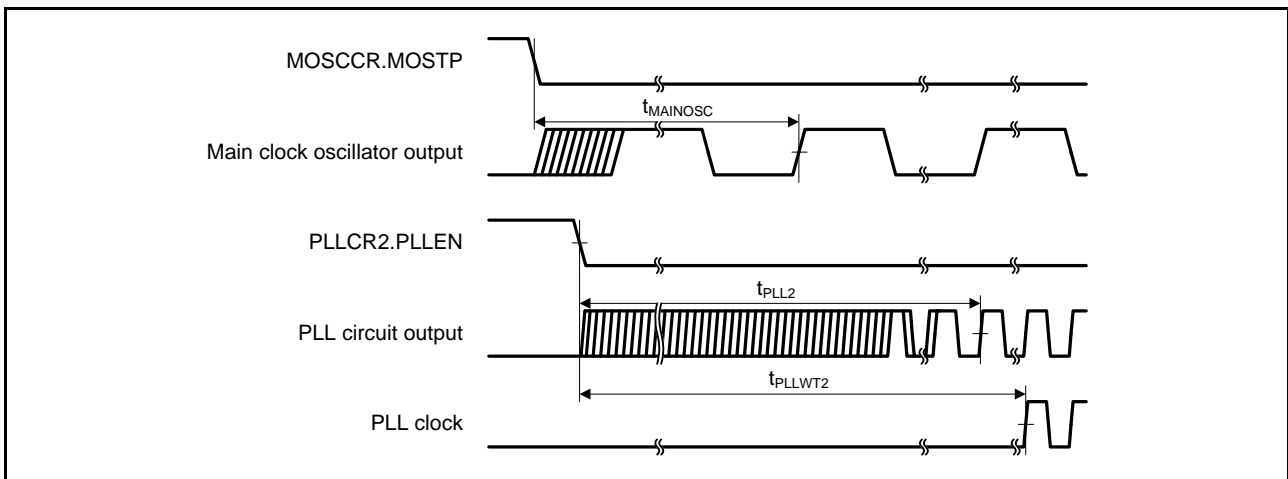


Figure 5.11 PLL Clock Oscillation Start Timing (PLL is Operated before Main Clock Oscillation Has Settled)

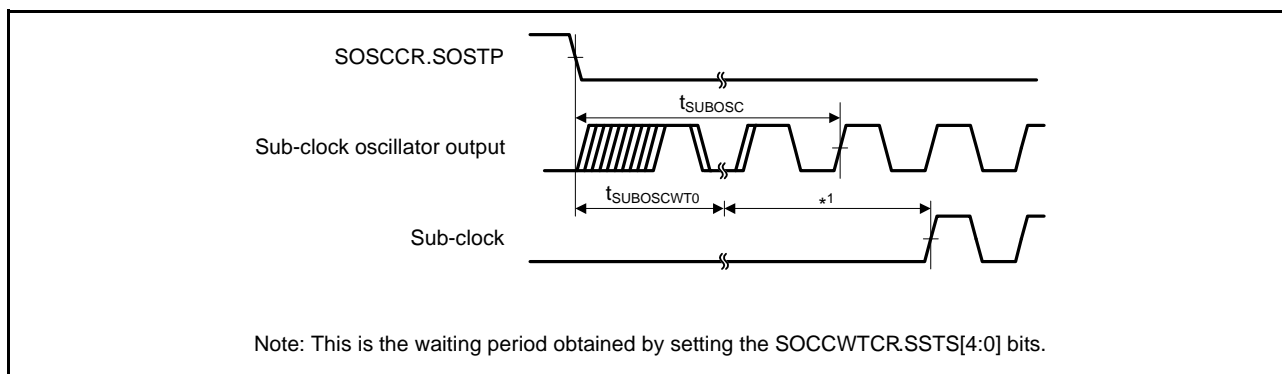


Figure 5.12 Sub-Clock Oscillation Start Timing

5.3.3 Timing of Recovery from Low Power Consumption Modes

Table 5.14 Timing of Recovery from Low Power Consumption Modes

Conditions: VCC = AVCC0 = VREFH = VCC_USB = V_{BATT} = 2.7 to 3.6 V, VREFH0 = 2.7 V to AVCC0, VSS = AVSS0 = VREFL/VREFLO = VSS_USB = 0 V, T_a = T_{opr}

| Item | | | Symbol | Min. | Typ. | Max. | Unit | Test Conditions |
|--|---|---|---------------------|------|------|------|------------------|-----------------|
| Recovery time after cancellation of software standby mode | Crystal resonator connected to main clock oscillator | Main clock oscillator operating | t _{SBYMC} | 10 | — | — | ms | Figure 5.13 |
| | | Main clock oscillator and PLL circuit operating | t _{SBYPC} | 10 | — | — | ms | |
| | External clock input to main clock oscillator | Main clock oscillator operating | t _{SBYEX} | 1 | — | — | ms | |
| | | Main clock oscillator and PLL circuit operating | t _{SBYPE} | 1 | — | — | ms | |
| | Sub-clock oscillator operating | | t _{SBYSC} | 2 | — | — | s | |
| | High-speed on-chip oscillator operating | | t _{SBYHO} | — | — | 2 | ms | |
| | Low-speed on-chip oscillator or IWDG-dedicated on-chip oscillator operating | | t _{SBYLO} | — | — | 800 | μs | |
| Recovery time after cancellation of deep software standby mode | | | t _{DSBY} | — | — | 1.0 | ms | Figure 5.14 |
| Wait time after cancellation of deep software standby mode | | | t _{DSBYWT} | 45 | — | 46 | t _{cyc} | |

Note: The wait time varies depending on the state in which each oscillator was when the WAIT instruction was executed. The recovery time when multiple oscillators are operating is the same period as that when the oscillator which requires the longest time of all operating oscillators to recover is operating alone.

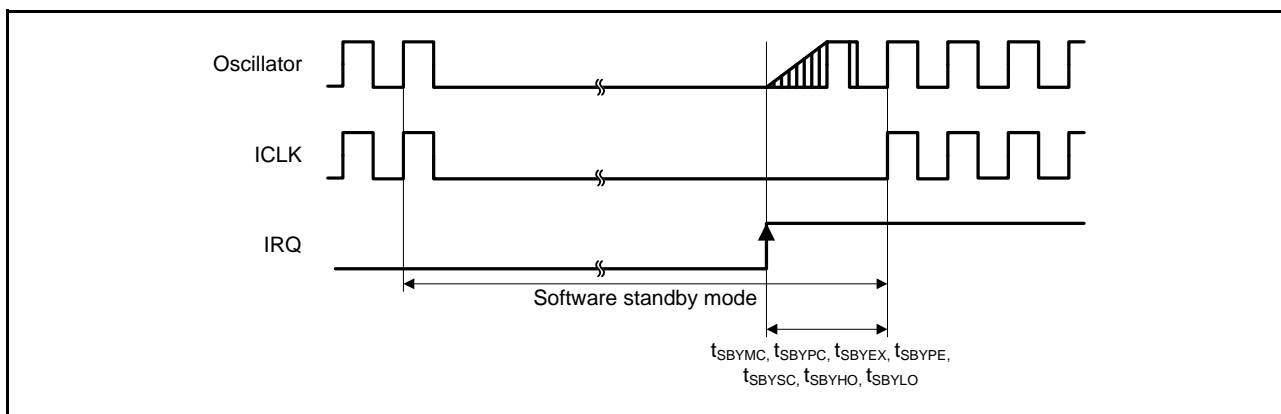


Figure 5.13 Software Standby Mode Cancellation Timing

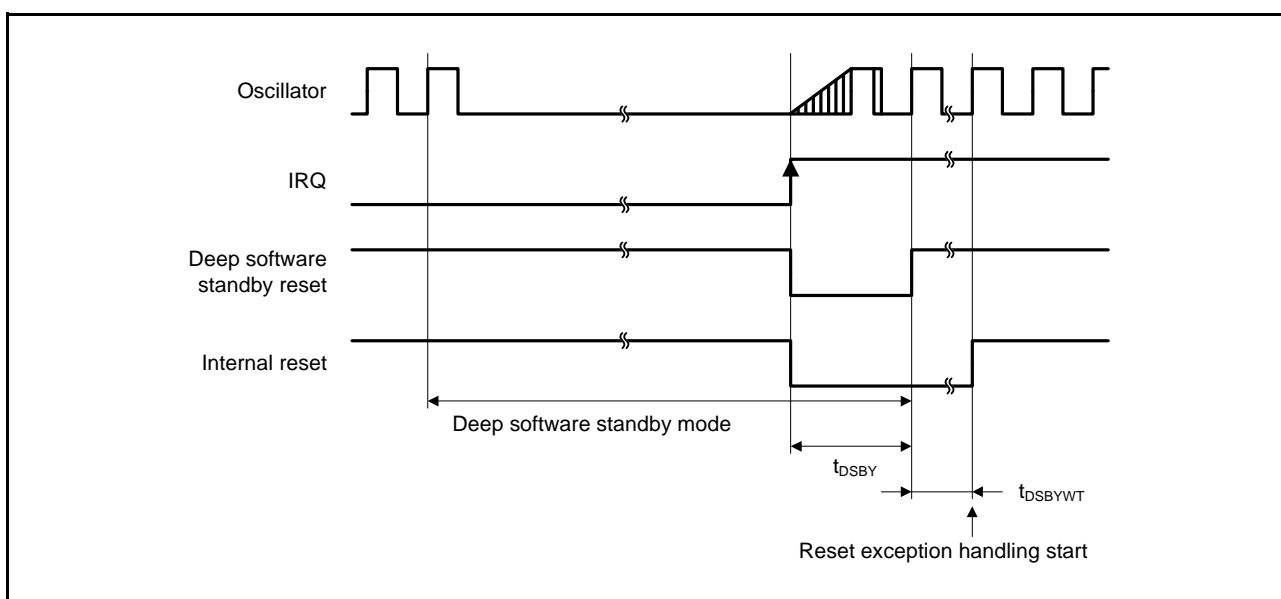


Figure 5.14 Deep Software Standby Mode Cancellation Timing

5.3.4 Control Signal Timing

Table 5.15 Control Signal Timing

Conditions: $V_{CC} = AV_{CC0} = V_{REFH} = V_{CC_USB} = V_{BATT} = 2.7$ to 3.6 V, $V_{REFH0} = 2.7$ V to AV_{CC0} ,
 $V_{SS} = AV_{SS0} = V_{REFL}/V_{REFL0} = V_{SS_USB} = 0$ V, $T_a = T_{opr}$

| Item | Symbol | Min. | Typ. | Max. | Unit | Test Conditions |
|-----------------|------------|-----------------------|------|------|------|---|
| NMI pulse width | t_{NMIW} | 200 | — | — | ns | $t_c (PCLK) \times 2 \leq 200$ ns Figure 5.15 |
| | | $t_c (PCLK) \times 2$ | — | — | | $t_c (PCLK) \times 2 > 200$ ns Figure 5.15 |
| IRQ pulse width | t_{IRQW} | 200 | — | — | ns | $t_c (PCLK) \times 2 \leq 200$ ns Figure 5.16 |
| | | $t_c (PCLK) \times 2$ | — | — | | $t_c (PCLK) \times 2 > 200$ ns Figure 5.16 |

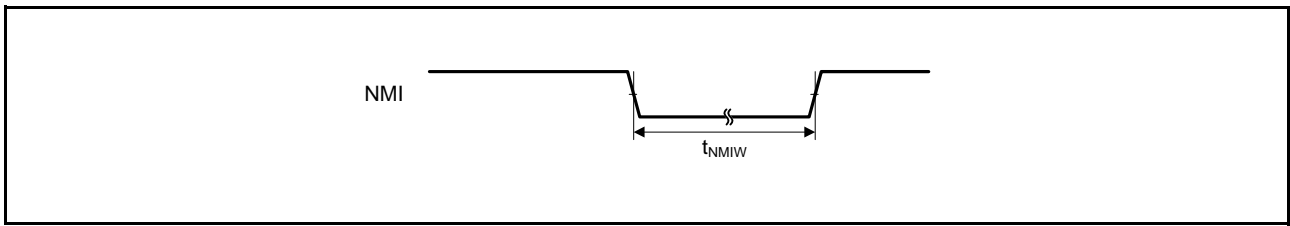


Figure 5.15 NMI Interrupt Input Timing

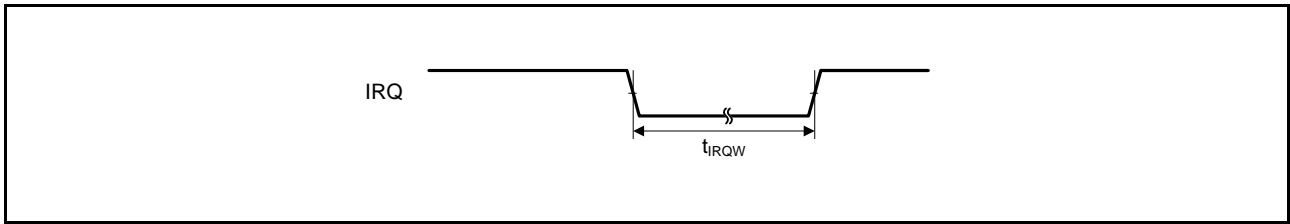


Figure 5.16 IRQ Interrupt Input Timing

5.3.5 Bus Timing

Table 5.16 Bus Timing (packages with 177 to 144 pins)

Conditions: $V_{CC} = AVCC0 = VREFH = VCC_USB = 2.7$ to 3.6 V, $VREFH0 = 2.7$ V to $AVCC0$,
 $VSS = AVSS0 = VREFL/VREFLO = VSS_USB = 0$ V,
 $ICLK = 8$ to 100 MHz, $BCLK$ pin = 8 to 50 MHz, $SDCLK$ pin = 8 to 50 MHz, $T_a = T_{opr}$
 Output load conditions: $V_{OH} = VCC \times 0.5$, $V_{OL} = VCC \times 0.5$, $I_{OH} = -1.0$ mA, $I_{OL} = 1.0$ mA, $C = 30$ pF
 High drive output is selected by the drive capacity control register.

| Item | Symbol | Min. | Max. | Unit | Test Conditions |
|---------------------------------|------------|------|------|------|-------------------------------|
| Address delay time | t_{AD} | — | 15 | ns | Figure 5.17 to Figure 5.22 |
| Byte control delay time | t_{BCD} | — | 15 | ns | |
| CS# delay time | t_{CSD} | — | 15 | ns | |
| ALE delay time | t_{ALED} | — | 20 | ns | |
| RD# delay time | t_{RSD} | — | 15 | ns | |
| Read data setup time | t_{RDS} | 15 | — | ns | |
| Read data hold time | t_{RDH} | 0 | — | ns | |
| WR# delay time | t_{WRD} | — | 15 | ns | |
| Write data delay time | t_{WDD} | — | 15 | ns | |
| Write data hold time | t_{WDH} | 0 | — | ns | |
| WAIT# setup time | t_{WTS} | 15 | — | ns | |
| WAIT# hold time | t_{WTH} | 0 | — | ns | |
| Address delay time 2 (SDRAM) | t_{AD2} | 1 | 15 | ns | Figure 5.24 to Figure 5.30 |
| CS# delay time 2 (SDRAM) | t_{CSD2} | 1 | 15 | ns | |
| DQM delay time (SDRAM) | t_{DQMD} | 1 | 15 | ns | |
| CKE delay time (SDRAM) | t_{CKED} | 1 | 15 | ns | |
| Read data setup time 2 (SDRAM) | t_{RDS2} | 12 | — | ns | |
| Read data hold time 2 (SDRAM) | t_{RDH2} | 0 | — | ns | |
| Write data delay time 2 (SDRAM) | t_{WDD2} | — | 15 | ns | |
| Write data hold time 2 (SDRAM) | t_{WDH2} | 1 | — | ns | |
| WE# delay time (SDRAM) | t_{WED} | 1 | 15 | ns | |
| RAS# delay time (SDRAM) | t_{RASD} | 1 | 15 | ns | |
| CAS# delay time (SDRAM) | t_{CASD} | 1 | 15 | ns | |

Table 5.17 Bus Timing (packages with 100 pins or less)

Conditions: $V_{CC} = AVCC0 = VREFH = VCC_USB = 2.7$ to 3.6 V, $VREFH0 = 2.7$ V to $AVCC0$,

$VSS = AVSS0 = VREFL/VREFL0 = VSS_USB = 0$ V,

$ICLK = 8$ to 100 MHz, $BCLK$ pin = 8 to 50 MHz, $T_a = T_{opr}$

Output load conditions: $V_{OH} = VCC \times 0.5$, $V_{OL} = VCC \times 0.5$, $I_{OH} = -1.0$ mA, $I_{OL} = 1.0$ mA, $C = 30$ pF

High drive output is selected by the drive capacity control register.

| Item | Symbol | Min. | Max. | Unit | Test Conditions |
|-------------------------|------------|------|------|------|-------------------------------|
| Address delay time | t_{AD} | — | 20 | ns | Figure 5.17 to Figure 5.22 |
| Byte control delay time | t_{BCD} | — | 20 | ns | |
| CS# delay time | t_{CSD} | — | 20 | ns | |
| ALE delay time | t_{ALED} | — | 20 | ns | |
| RD# delay time | t_{RSD} | — | 20 | ns | |
| Read data setup time | t_{RDS} | 15 | — | ns | |
| Read data hold time | t_{RDH} | 0 | — | ns | |
| WR# delay time | t_{WRD} | — | 20 | ns | |
| Write data delay time | t_{WDD} | — | 20 | ns | |
| Write data hold time | t_{WDH} | 0 | — | ns | |
| WAIT# setup time | t_{WTS} | 15 | — | ns | Figure 5.23 |
| WAIT# hold time | t_{WTH} | 0 | — | ns | |

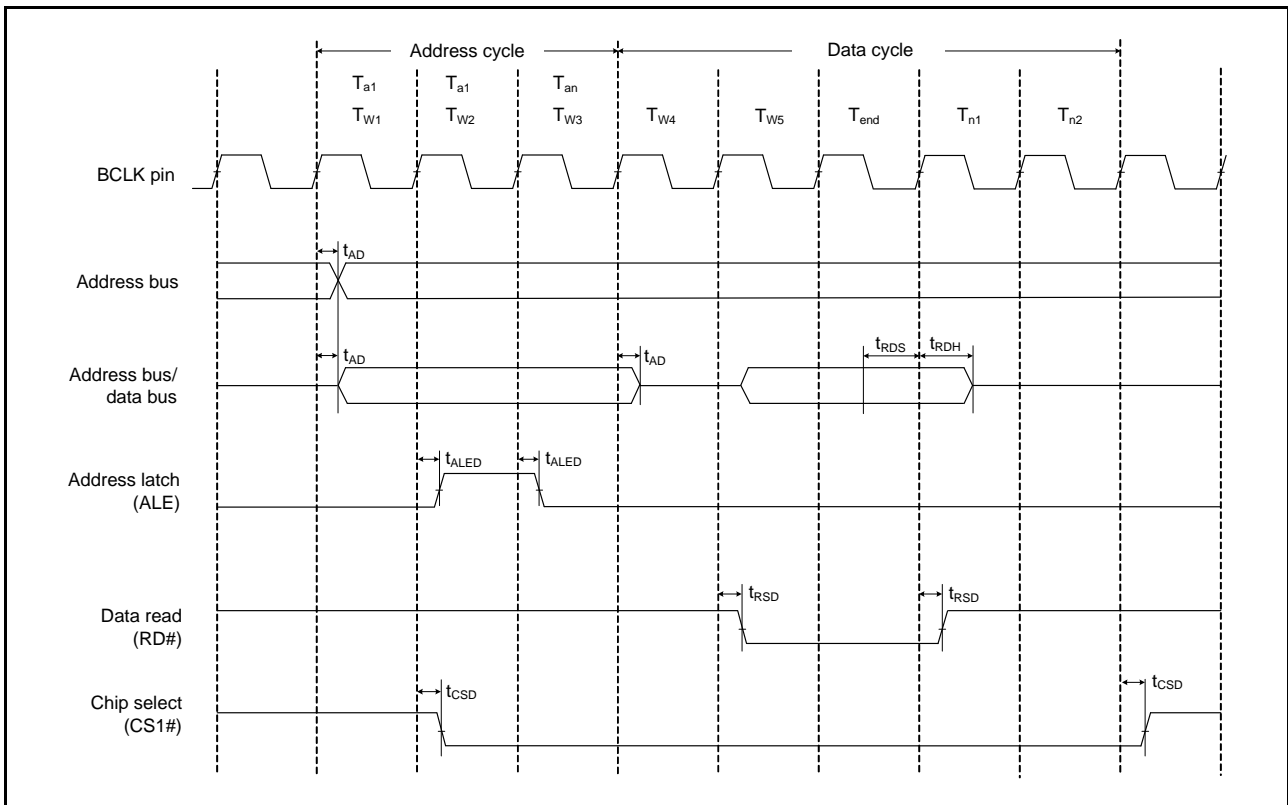


Figure 5.17 Address/Data Multiplexed Bus Read Access Timing

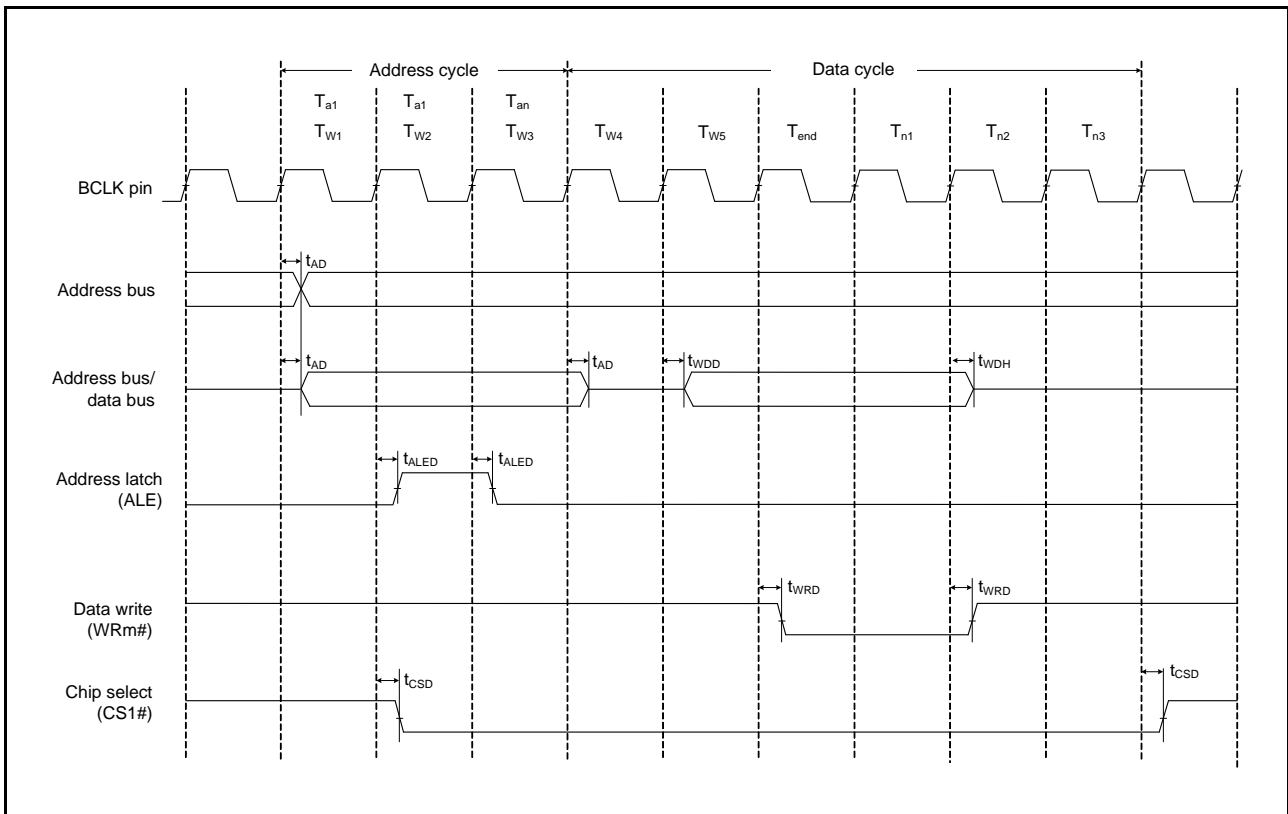


Figure 5.18 Address/Data Multiplexed Bus Write Access Timing

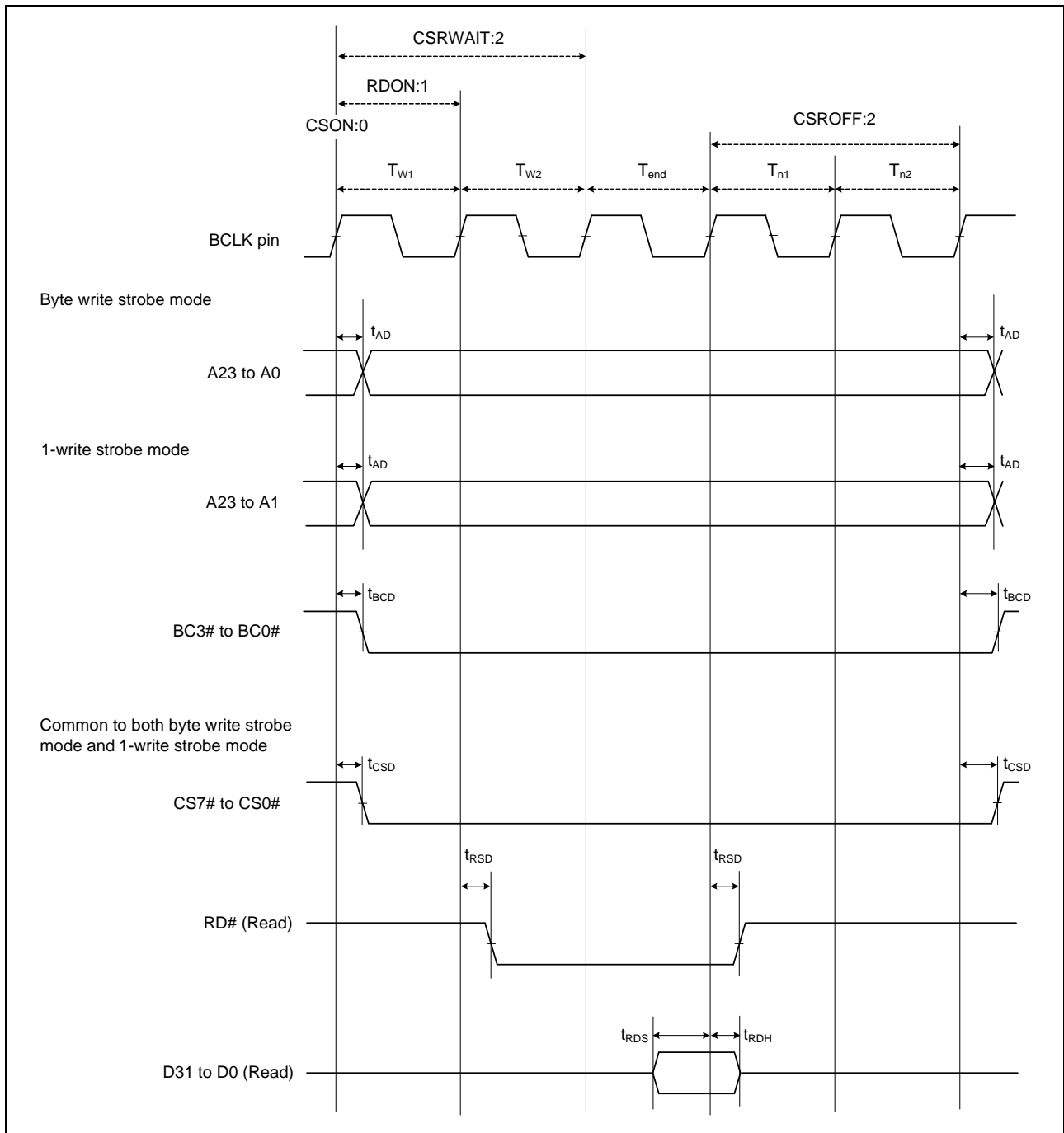


Figure 5.19 External Bus Timing/Normal Read Cycle (Bus Clock Synchronized)

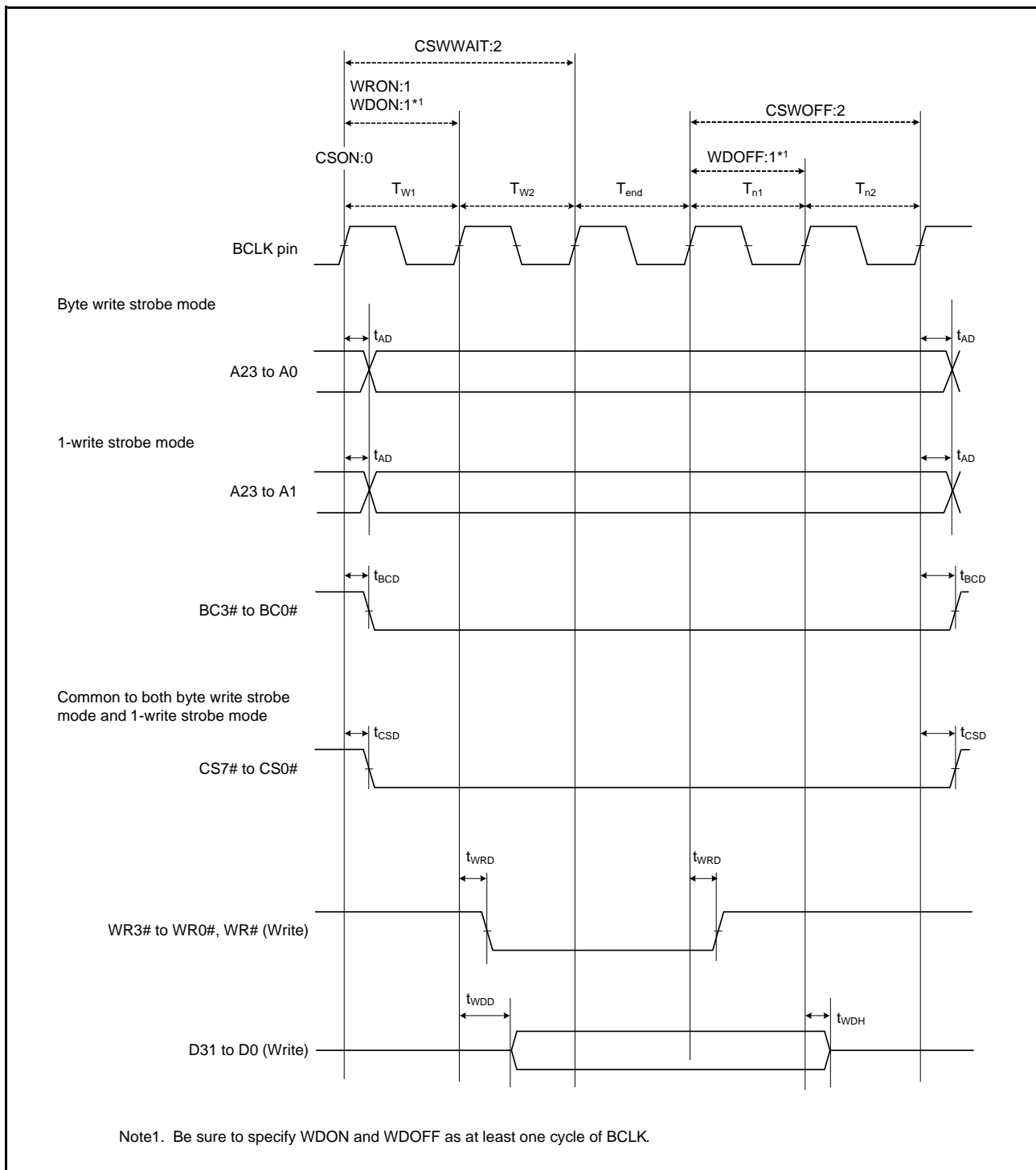


Figure 5.20 External Bus Timing/Normal Write Cycle (Bus Clock Synchronized)

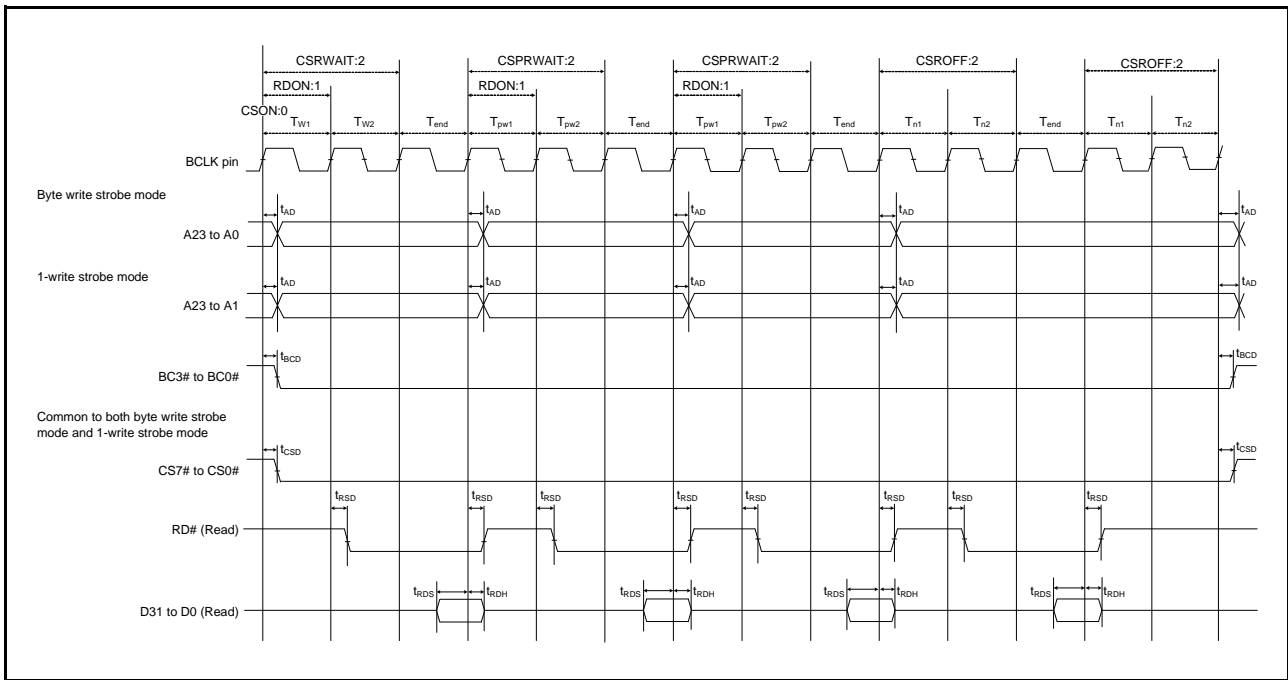


Figure 5.21 External Bus Timing/Page Read Cycle (Bus Clock Synchronized)

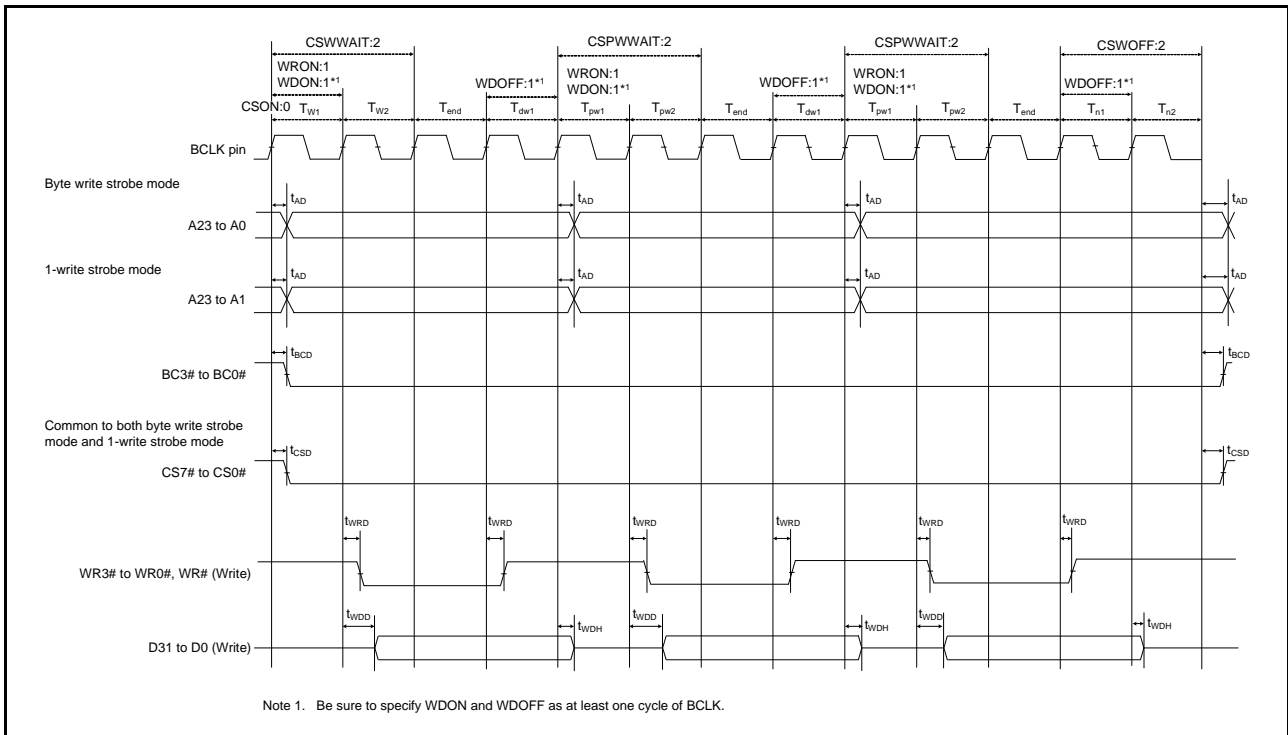


Figure 5.22 External Bus Timing/Page Write Cycle (Bus Clock Synchronized)

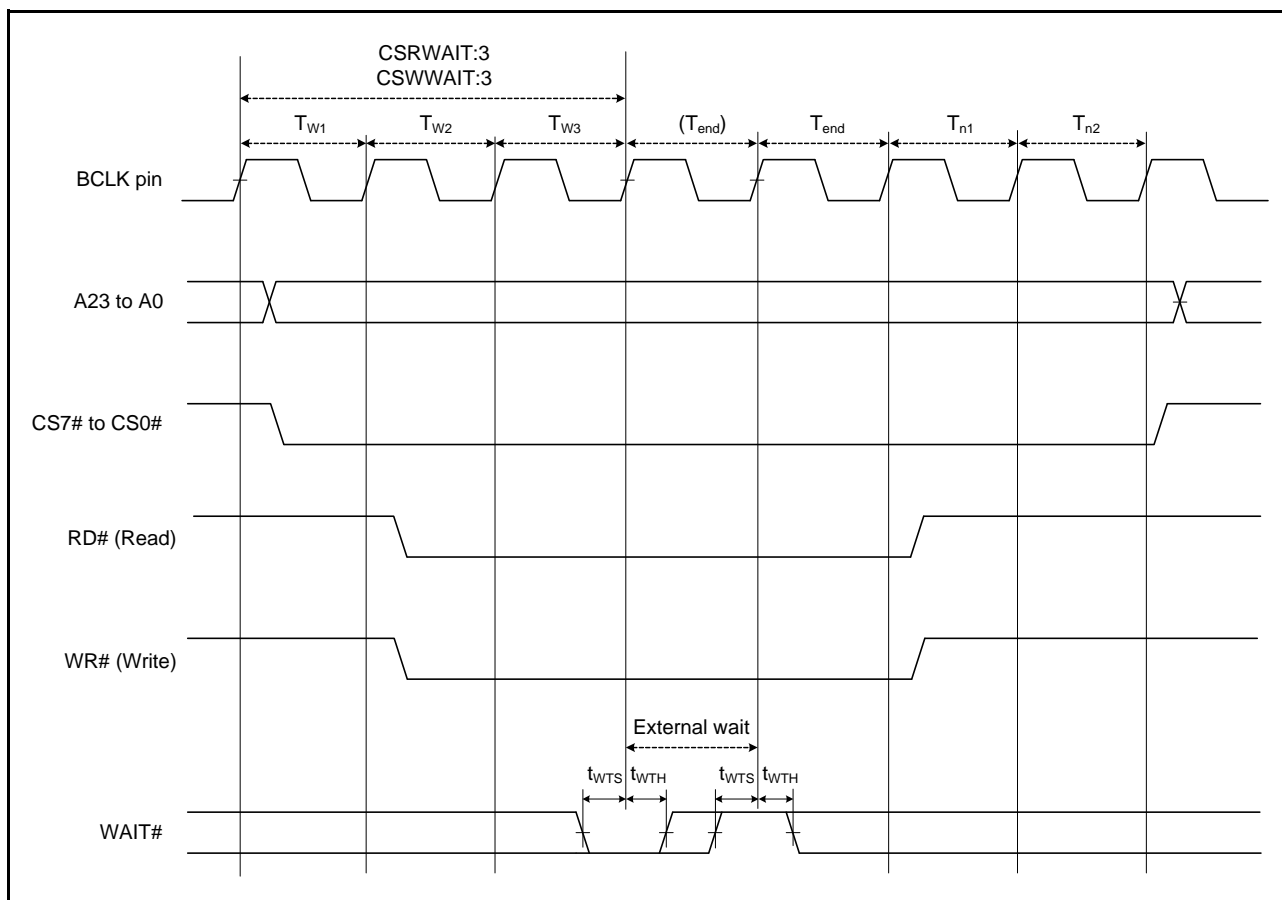


Figure 5.23 External Bus Timing/External Wait Control

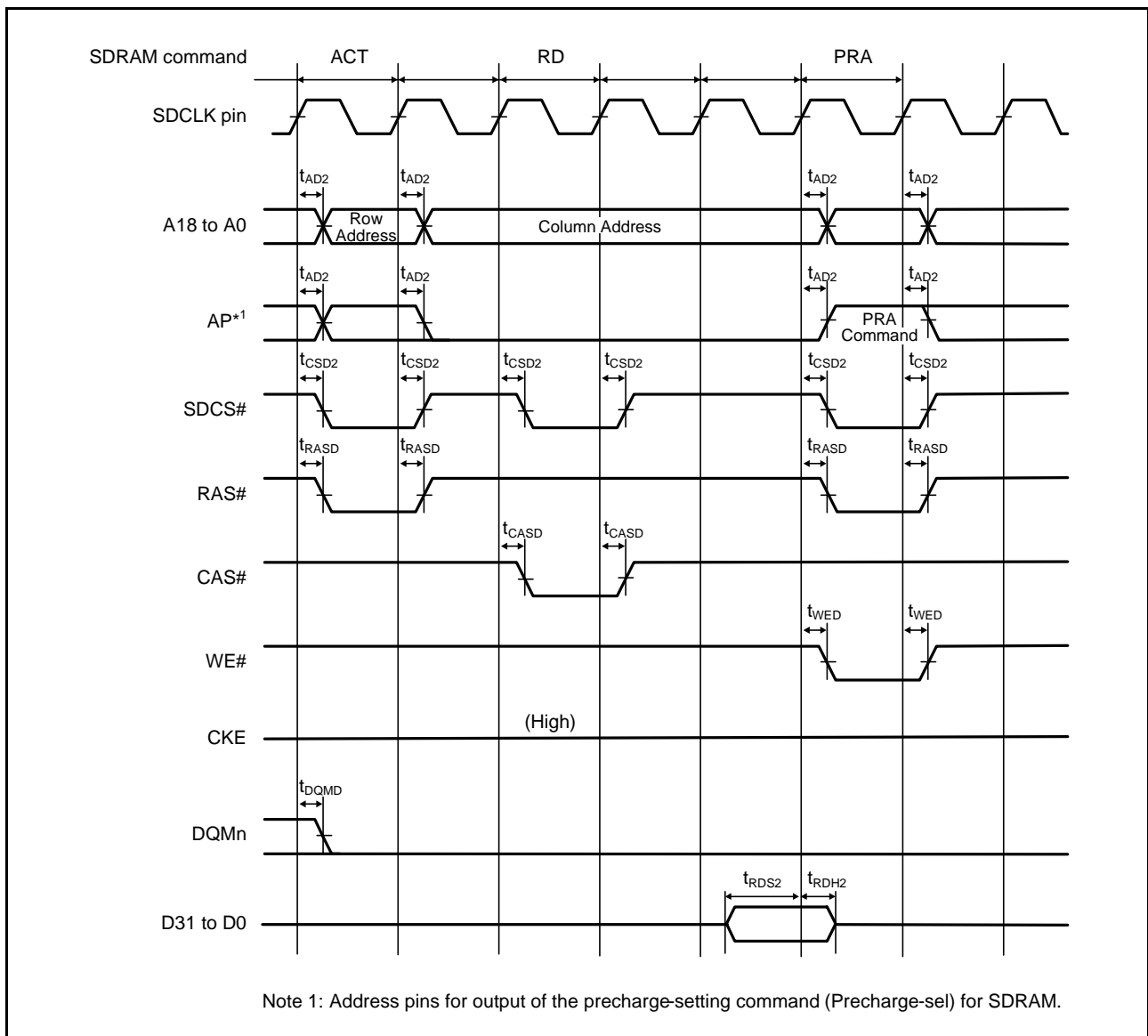


Figure 5.24 SDRAM Space Single Read Bus Timing

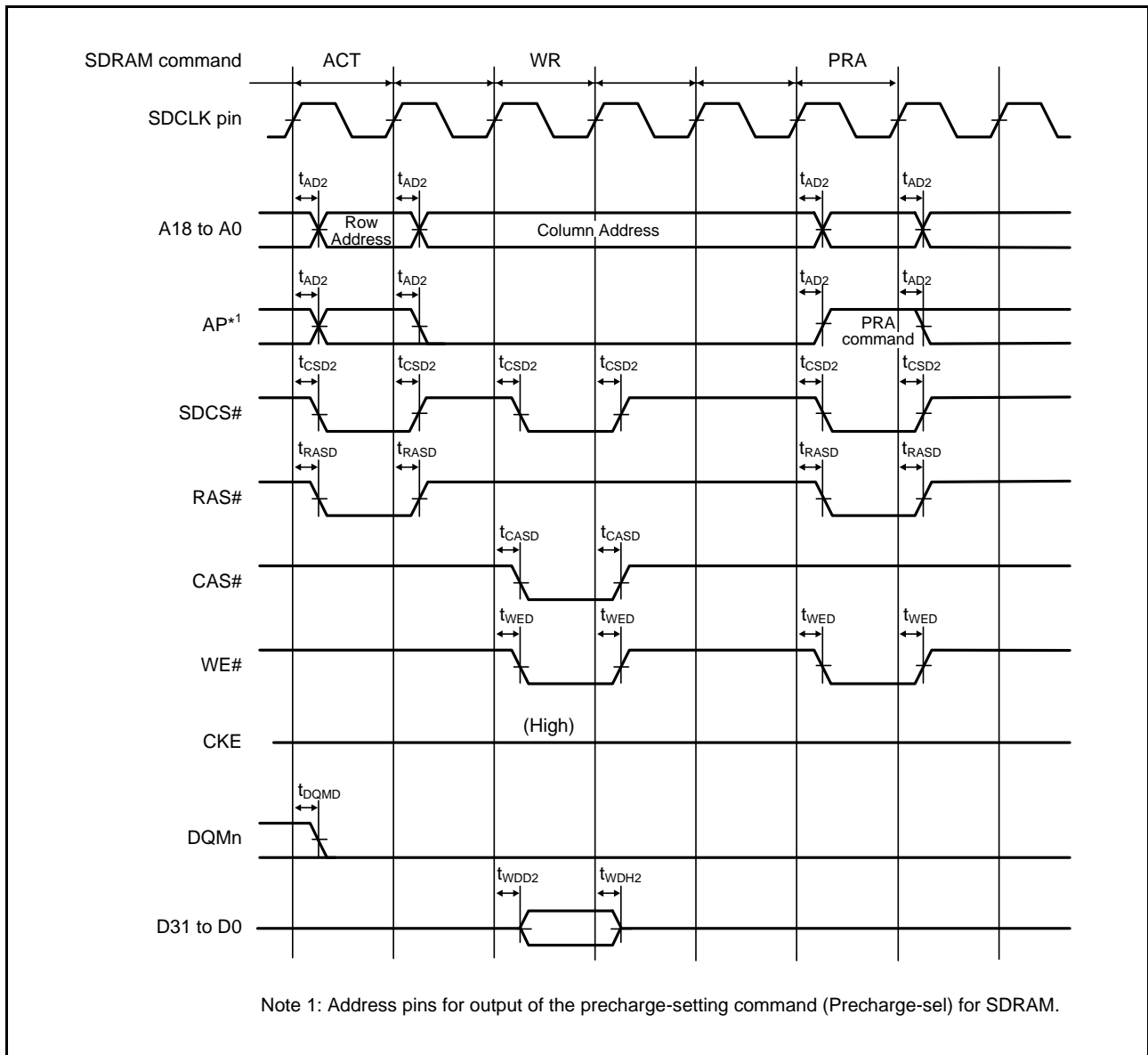


Figure 5.25 SDRAM Space Single Write Bus Timing

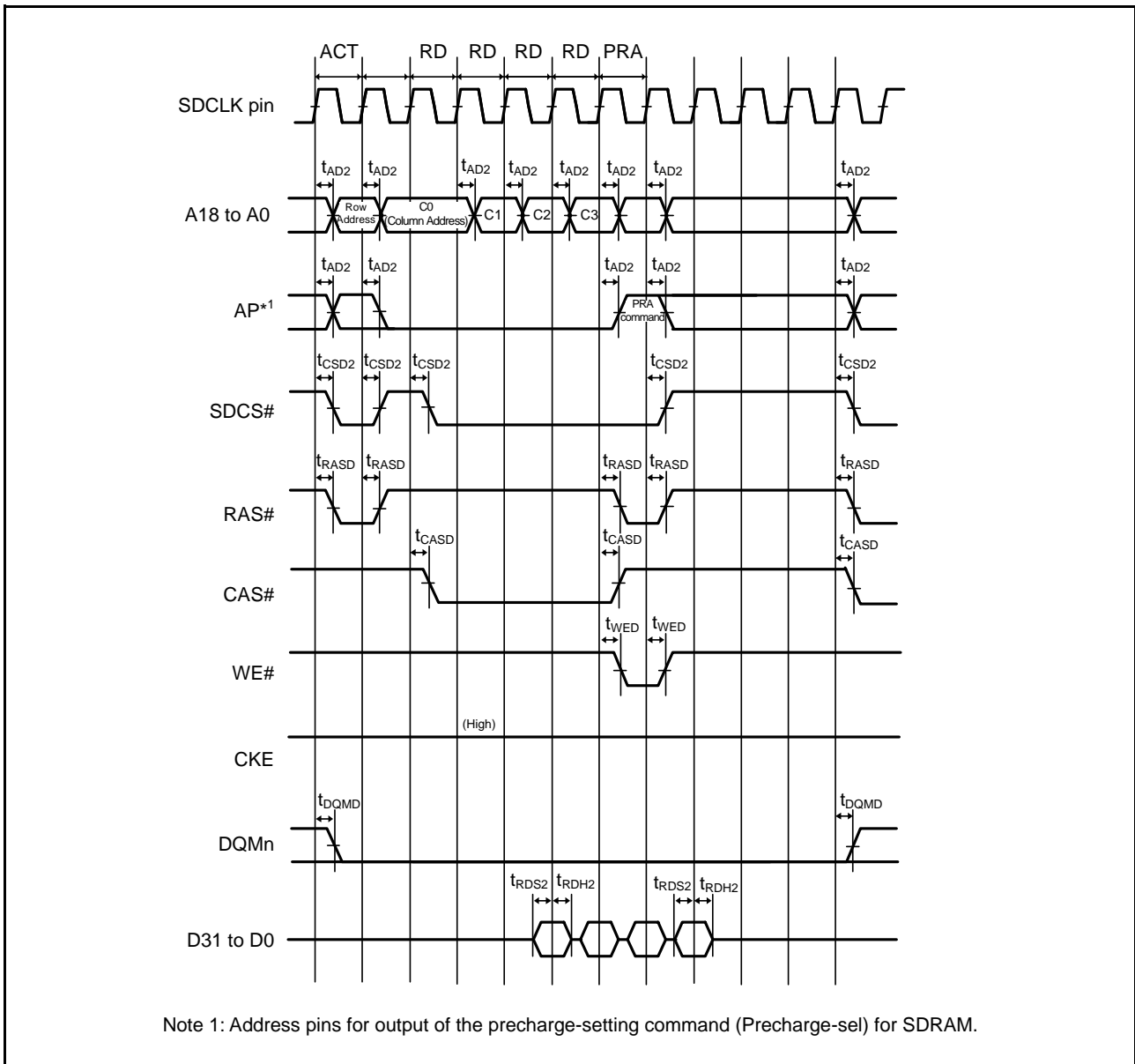


Figure 5.26 SDRAM Space Multiple Read Bus Timing

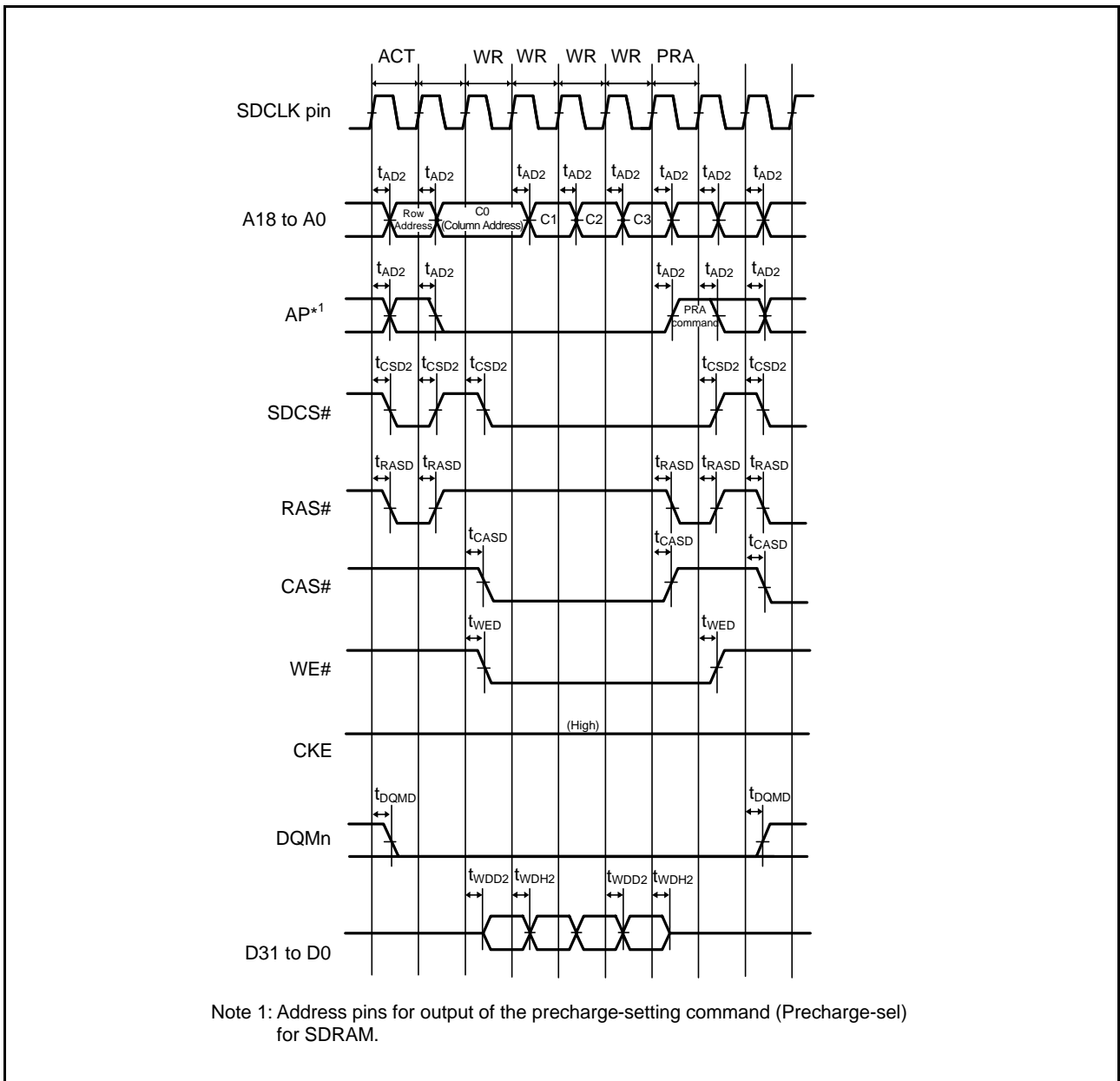


Figure 5.27 SDRAM Space Multiple Write Bus Timing

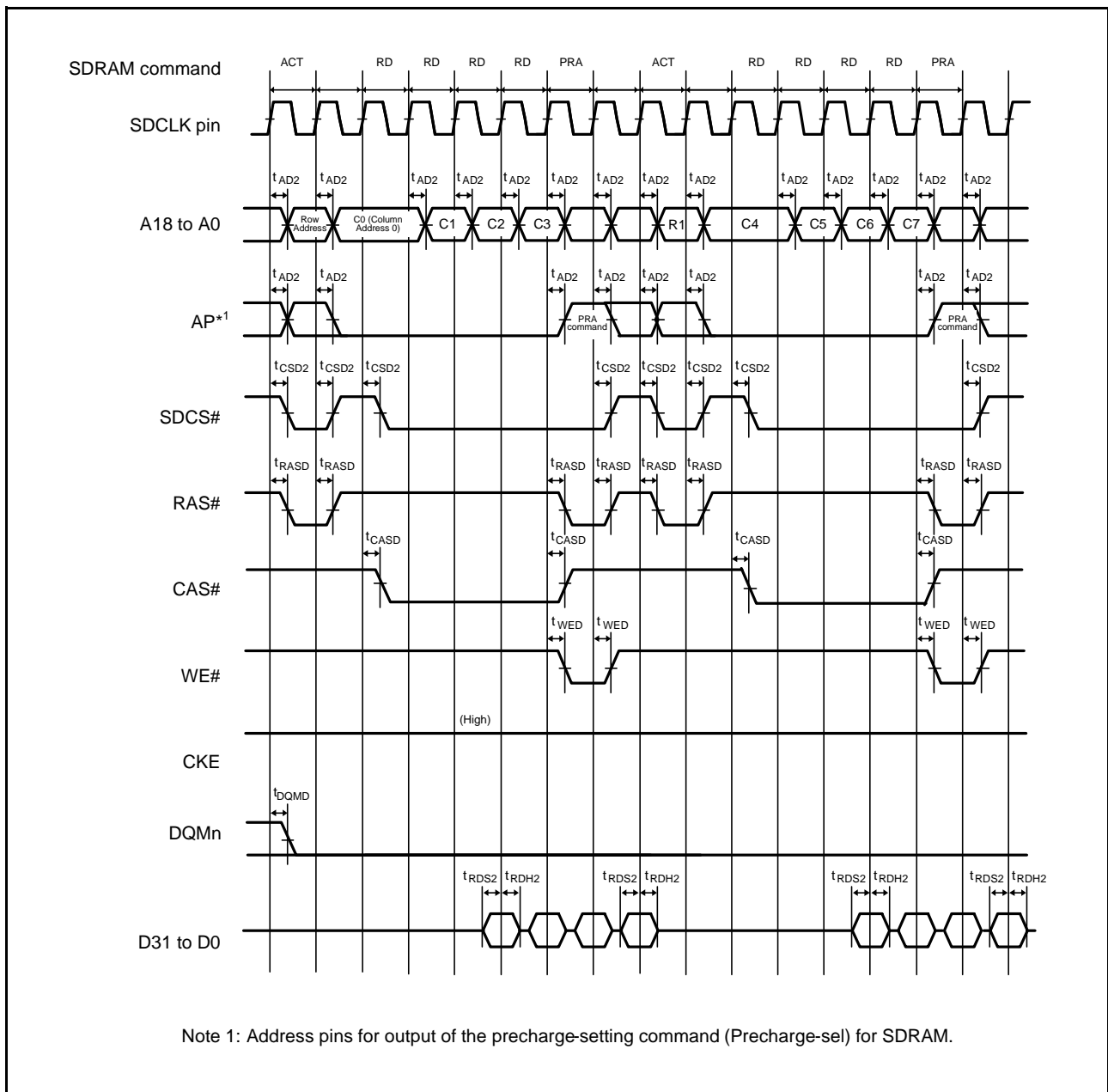


Figure 5.28 SDRAM Space Multiple Read Line Stride Bus Timing

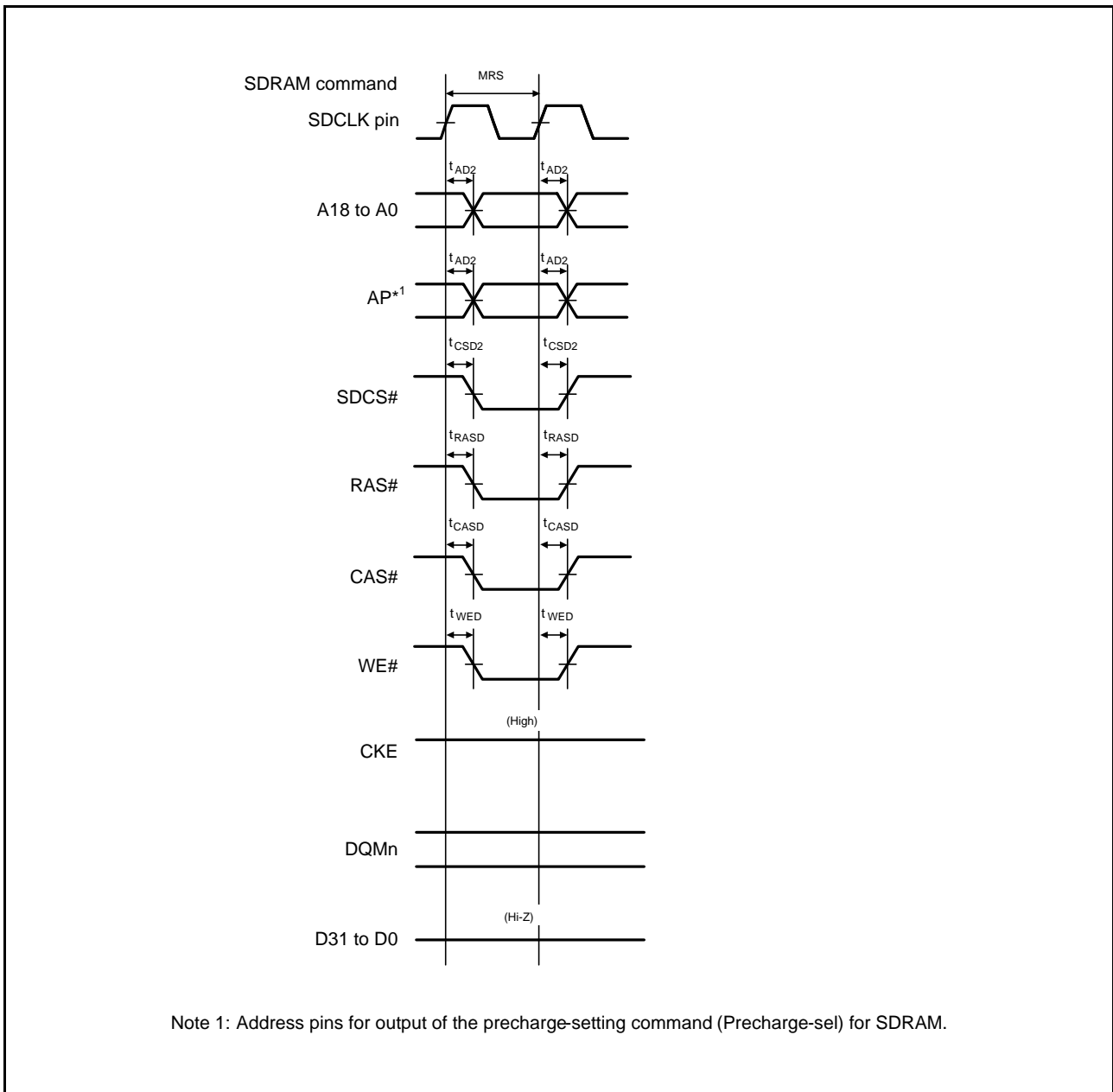


Figure 5.29 SDRAM Space Mode Register Set Bus Timing

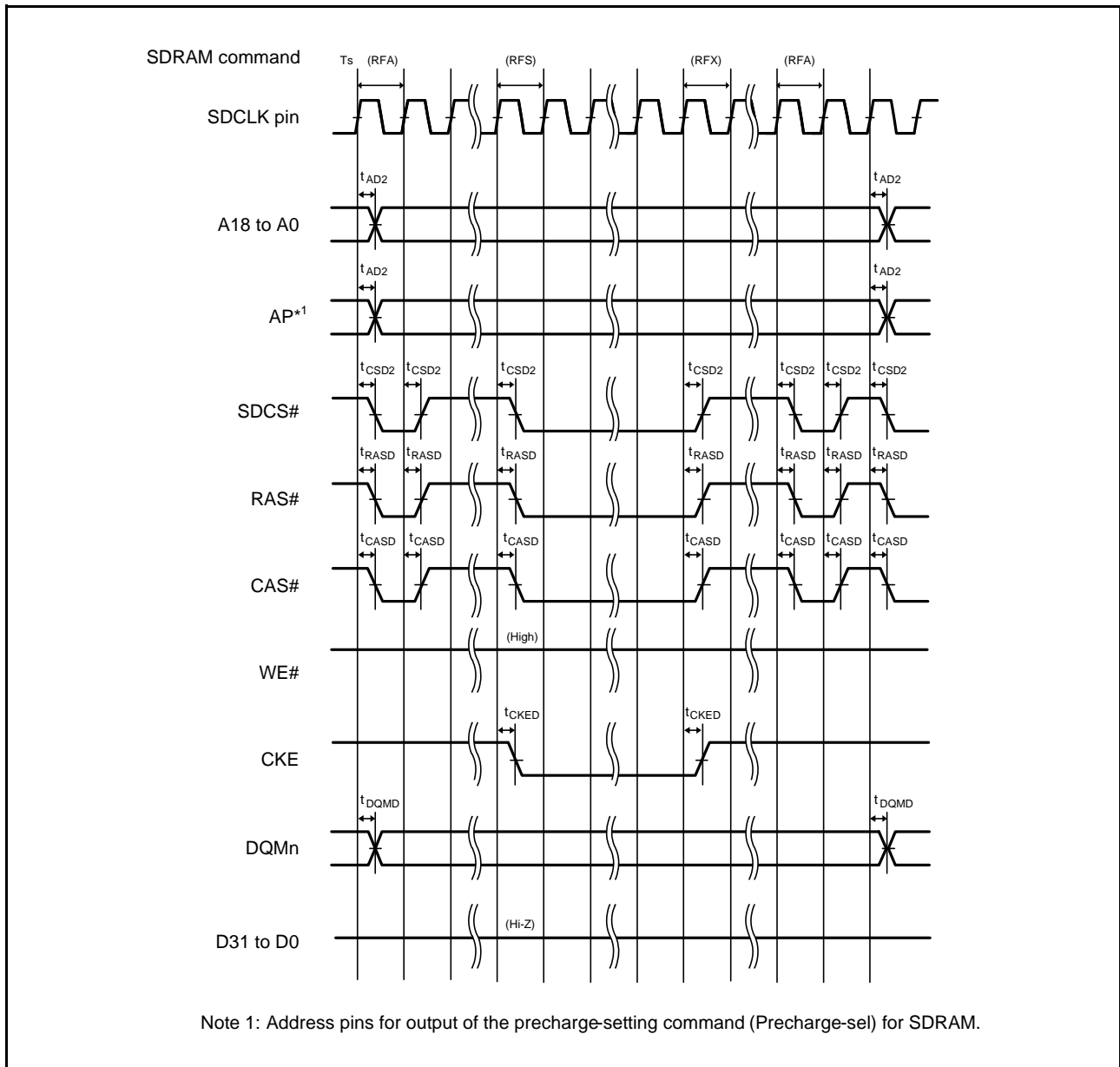


Figure 5.30 SDRAM Space Self-Refresh Bus Timing

5.3.6 EXDMAC Timing

Table 5.18 EXDMAC Timing

Conditions: VCC = AVCC0 = VREFH = VCC_USB = 2.7 to 3.6 V, VREFH0 = 2.7 V to AVCC0,
 VSS = AVSS0 = VREFL/VREFL0 = VSS_USB = 0 V
 ICLK = 8 to 100 MHz, PCLK = 8 to 50 MHz, BCLK pin = 8 to 100 MHz, SDCLK pin = 8 to 50 MHz, T_a = T_{opr}
 High drive output is selected by the drive capacity control register

| Item | Symbol | Min. | Max. | Unit | Test Conditions | |
|--------|------------------|--------------------|------|------|-----------------|-----------------------------|
| EXDMAC | EDREQ setup time | t _{EDRQS} | 20 | — | ns | Figure 5.31 |
| | EDREQ hold time | t _{EDRQH} | 5 | — | ns | Figure 5.32 and Figure 5.33 |
| | EDACK delay time | t _{EDACD} | — | 15 | ns | |

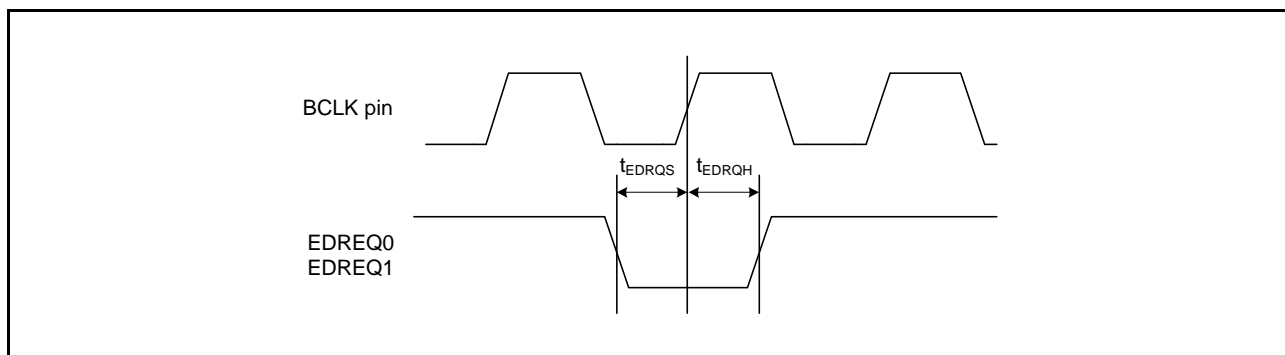


Figure 5.31 EDREQ0 and EDREQ1 Input Timing

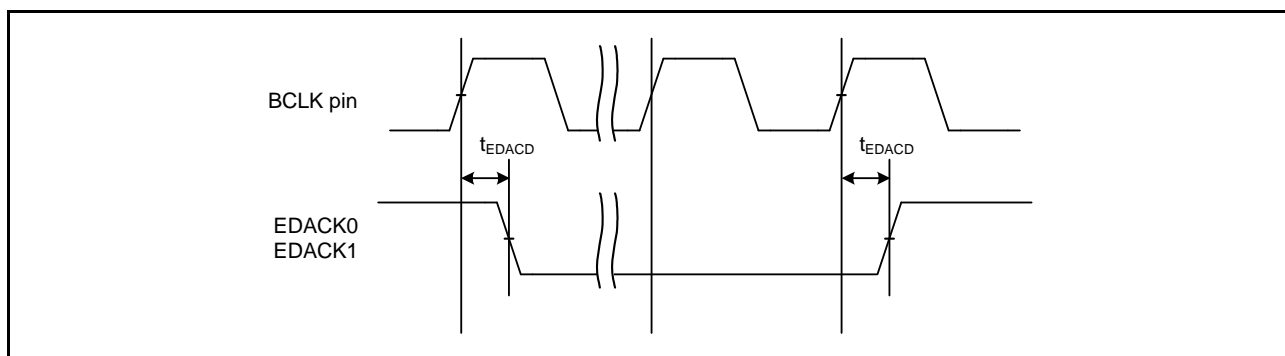


Figure 5.32 EDACK0 and EDACK1 Single-Address Transfer Timing (for a CS Area)

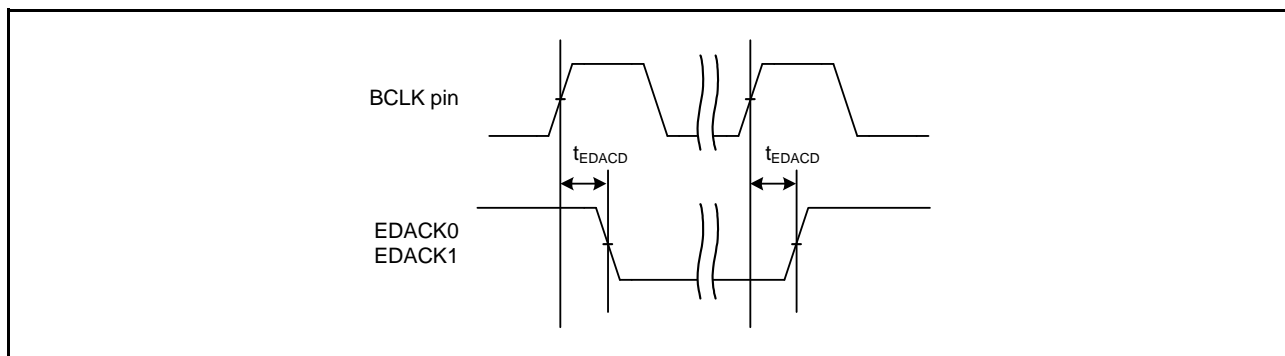


Figure 5.33 EDACK0 and EDACK1 Single-Address Transfer Timing (for SDRAM)

5.3.7 Timing of On-Chip Peripheral Modules

Table 5.19 Timing of On-Chip Peripheral Modules (1)

Conditions: VCC = AVCC0 = VREFH = VCC_USB = 2.7 to 3.6 V, VREFH0 = 2.7 V to AVCC0,
VSS = AVSS0 = VREFL/VREFL0 = VSS_USB = 0 V
PCLK = 8 to 50 MHz
T_a = T_{opr}
High drive output is selected by the drive capacity control register.

| Item | | Symbol | Min. | Max. | Unit*1 | Test Conditions | |
|-------------------------|--|---------------------|--|------|-------------------|-------------------|-------------|
| I/O ports | Input data pulse width | t _{PRW} | 1.5 | — | t _{Pcyc} | Figure 5.34 | |
| MTU/TPU | Input capture input pulse width | Single-edge setting | t _{TICW} | 1.5 | — | t _{Pcyc} | Figure 5.35 |
| | | Both-edge setting | | 2.5 | — | | |
| | Timer clock pulse width | Single-edge setting | t _{TCKWH} , t _{TCKWL} | 1.5 | — | t _{Pcyc} | Figure 5.36 |
| Both-edge setting | | 2.5 | | — | | | |
| Phase counting mode | | 2.5 | | — | | | |
| POE | POE# input pulse width | t _{POEW} | 1.5 | — | t _{Pcyc} | Figure 5.37 | |
| 8-bit timer | Timer clock pulse width | Single-edge setting | t _{TMCWH} , t _{TMCWL} | 1.5 | — | t _{Pcyc} | Figure 5.38 |
| | | Both-edge setting | | 2.5 | — | | |
| SCI | Input clock cycle | Asynchronous | t _{Scyc} | 4 | — | t _{Pcyc} | Figure 5.39 |
| | | Clock synchronous | | 6 | — | | |
| | Input clock pulse width | | t _{SCKW} | 0.4 | 0.6 | t _{Scyc} | |
| | Input clock rise time | | t _{SCKr} | — | 20 | ns | |
| | Input clock fall time | | t _{SCKf} | — | 20 | ns | |
| | Output clock cycle | Asynchronous | t _{Scyc} | 16 | — | t _{Pcyc} | |
| | | Clock synchronous | | 4 | — | | |
| | Output clock pulse width | | t _{SCKW} | 0.4 | 0.6 | t _{Scyc} | |
| | Output clock rise time | | t _{SCKr} | — | 20 | ns | |
| | Output clock fall time | | t _{SCKf} | — | 20 | ns | |
| | Transmit data delay time | Clock synchronous | t _{TXD} | — | 40 | ns | Figure 5.40 |
| Receive data setup time | Clock synchronous | t _{RXS} | 40 | — | ns | | |
| Receive data hold time | Clock synchronous | t _{RXH} | 40 | — | ns | | |
| A/D converter | 10-bit A/D converter trigger input pulse width | t _{TRGW} | 1.5 | — | t _{Pcyc} | Figure 5.41 | |
| | 12-bit A/D converter trigger input pulse width | | 1.5 | — | | | |

Note 1. t_{Pcyc}: PCLK cycle

Table 5.20 Timing of On-Chip Peripheral Modules (2)

Conditions: $V_{CC} = AV_{CC0} = V_{REFH} = V_{CC_USB} = 2.7$ to 3.6 V*1, $V_{REFH0} = 2.7$ V to AV_{CC0} *1,
 $V_{SS} = AV_{SS0} = V_{REFL}/V_{REFL0} = V_{SS_USB} = 0$ V,
 $PCLK = 8$ to 50 MHz,
 $T_a = T_{opr}$
 High drive output is selected by the drive capacity control register.

| Item | | | Symbol | Min. | Max. | Unit*2 | Test Conditions | | |
|----------------------|------------------------------|---|---------------------|---|------|-------------|-------------------------|----|---|
| RSPI | RSPCK clock cycle | Master | t_{SPCyc} | 2 | 4096 | t_{PCyc} | Figure 5.42 C = 30pF | | |
| | | Slave | | 8 | 4096 | | | | |
| | RSPCK clock high pulse width | Master | t_{SPCKWH} | $(t_{SPCyc} - t_{SPCKR} - t_{SPCKF}) / 2 - 3$ | | — | | ns | |
| | | Slave | | $(t_{SPCyc} - t_{SPCKR} - t_{SPCKF}) / 2$ | | — | | | |
| | RSPCK clock low pulse width | Master | t_{SPCKWL} | $(t_{SPCyc} - t_{SPCKR} - t_{SPCKF}) / 2 - 3$ | | — | | ns | |
| | | Slave | | $(t_{SPCyc} - t_{SPCKR} - t_{SPCKF}) / 2$ | | — | | | |
| | RSPCK clock rise/fall time | Output [packages with 177 to 144 pins] | | t_{SPCKr} , t_{SPCKf} | — | 5 | | ns | |
| | | Output [packages with 100 pins or less] | | | — | 10 | | | |
| | | Input | | | — | 1 | | | μ s |
| | Data input setup time | Master [packages with 177 to 144 pins] | $V_{CC} \geq 3.0$ V | t_{SU} | 15 | — | | ns | Figure 5.43 to Figure 5.46 C = 30pF |
| | | | $V_{CC} < 3.0$ V | | 20 | — | | | |
| | | Master [packages with 100 pins or less] | | | 30 | — | | | |
| Slave | | $20 - t_{PCyc}$ | — | | | | | | |
| Data input hold time | Master | | t_H | 0 | — | ns | | | |
| | Slave | | | $20 + 2 \times t_{PCyc}$ | — | | | | |
| SSL setup time | Master | | t_{LEAD} | 1 | 8 | t_{SPCyc} | | | |
| | Slave | | | 4 | — | t_{PCyc} | | | |
| SSL hold time | Master | | t_{LAG} | 1 | 8 | t_{SPCyc} | | | |
| | Slave | | | 4 | — | t_{PCyc} | | | |

Note 1. When operation at 3.0 V or a lower voltage is needed, please contact a Renesas sales office.

Note 2. t_{PCyc} : PCLK cycle

Table 5.21 Timing of On-Chip Peripheral Modules (3)

Conditions: $V_{CC} = AV_{CC0} = V_{REFH} = V_{CC_USB} = 2.7$ to 3.6 V*1, $V_{REFH0} = 2.7$ V to AV_{CC0} *1,
 $V_{SS} = AV_{SS0} = V_{REFL}/V_{REFL0} = V_{SS_USB} = 0$ V,
 $PCLK = 8$ to 50 MHz,
 $T_a = T_{opr}$
 High drive output is selected by the drive capacity control register.

| Item | | | Symbol | Min. | Max. | Unit*2 | Test Conditions | |
|---------------------------|------------------------------------|--------------------------------|--------------------------------|---------------------------------|--|--------------------------|--|---|
| RSPI | Data output delay time | Master | Packages with 177 to 144 pins | t_{OD} | — | 18 | ns | Figure 5.43 to Figure 5.46 $C = 30$ pF |
| | | | Packages with 100 pins or less | | — | 30 | | |
| | | Slave | Packages with 177 to 144 pins | | — | $3 \times t_{Pcyc} + 40$ | | |
| | | | Packages with 100 pins or less | | — | $3 \times t_{Pcyc} + 50$ | | |
| | Data output hold time | Master | t_{OH} | 0 | — | ns | | |
| | | Slave | | 0 | — | | | |
| | Successive transmission delay time | Master | t_{TD} | $t_{SPcyc} + 2 \times t_{Pcyc}$ | $8 \times t_{SPcyc} + 2 \times t_{Pcyc}$ | ns | | |
| | | Slave | | $4 \times t_{Pcyc}$ | — | | | |
| | MOSI and MISO rise/fall time | Output | Packages with 177 to 144 pins | t_{Dr}, t_{Df} | — | 5 | ns | |
| | | | Packages with 100 pins or less | | — | 10 | | |
| Input | | — | 1 | | μ s | | | |
| SSL rise/fall time | Output | Packages with 177 to 144 pins | t_{SSLr}, t_{SSLf} | — | 5 | ns | | |
| | | Packages with 100 pins or less | | — | 10 | | | |
| | Input | — | | 1 | μ s | | | |
| Slave access time | | | t_{SA} | — | 4 | t_{Pcyc} | Figure 5.45 and Figure 5.46 $C = 30$ pF | |
| Slave output release time | | | t_{REL} | — | 3 | t_{Pcyc} | | |

Note 1. When operation at 3.0 V or a lower voltage is needed, please contact a Renesas sales office.

Note 2. t_{Pcyc} : PCLK cycle

Table 5.22 Timing of On-Chip Peripheral Modules (4)

Conditions: $VCC = AVCC0 = VREFH = VCC_USB = 2.7$ to 3.6 V, $VREFH0 = 2.7$ V to $AVCC0$
 $VSS = AVSS0 = VREFL/VREFL0 = VSS_USB = 0$ V
 $PCLK = 8$ to 50 MHz
 $T_a = T_{opr}$
 High drive output is selected by the drive capacity control register.

| Item | | Symbol | Min. | Max. | Unit*1 | Test Conditions | |
|------------|---------------------------------|------------------------|------|-------|-------------|-------------------------------|-------------|
| Simple SPI | SCK clock cycle output (master) | t_{SPCyc} | 4 | 65536 | t_{PCyc} | Figure 5.42 | |
| | SCK clock cycle input (slave) | | 8 | 65536 | | | |
| | SCK clock high pulse width | t_{SPCKWH} | 0.4 | 0.6 | t_{SPCyc} | | |
| | SCK clock low pulse width | t_{SPCKWL} | 0.4 | 0.6 | t_{SPCyc} | | |
| | SCK clock rise/fall time | t_{SPCKr}, t_{SPCKf} | — | 20 | ns | | |
| | Data input setup time | t_{SU} | 40 | — | ns | Figure 5.43 to Figure 5.46 | |
| | Data input hold time | t_{H} | 40 | — | ns | | |
| | SS input setup time | t_{LEAD} | 1 | — | t_{SPCyc} | | |
| | SS input hold time | t_{LAG} | 1 | — | t_{SPCyc} | | |
| | Data output delay time | t_{OD} | — | 40 | ns | | |
| | Data output hold time | t_{OH} | -10 | — | ns | | |
| | Data rise/fall time | t_{Dr}, t_{Df} | — | 20 | ns | | |
| | SS input rise/fall time | t_{SSLr}, t_{SSLf} | — | 20 | ns | | |
| | Slave access time | t_{SA} | — | 5 | t_{PCyc} | | Figure 5.46 |
| | Slave output release time | t_{REL} | — | 5 | t_{PCyc} | | |

Note 1. t_{PCyc} : PCLK cycle

Table 5.23 Timing of On-Chip Peripheral Modules (5)

Conditions: $V_{CC} = AV_{CC0} = V_{REFH} = V_{CC_USB} = 2.7$ to 3.6 V, $V_{REFH0} = 2.7$ V to AV_{CC0}
 $V_{SS} = AV_{SS0} = V_{REFL}/V_{REFL0} = V_{SS_USB} = 0$ V
 $PCLK = 8$ to 50 MHz
 $T_a = T_{opr}$
 High drive output is selected by the drive capacity control register.

| Item | | Symbol | Min.*1,*2 | Max.* | Unit | Test Conditions |
|---|---|------------|----------------------------------|--------------------------|------|-----------------|
| RIIC (Standard-mode, SMBus) ICFER.FMPE = 0 | SCL input cycle time | t_{SCL} | $6(12) \times t_{IICcyc} + 1300$ | — | ns | Figure 5.47 |
| | SCL input high pulse width | t_{SCLH} | $3(6) \times t_{IICcyc} + 300$ | — | ns | |
| | SCL input low pulse width | t_{SCLL} | $3(6) \times t_{IICcyc} + 300$ | — | ns | |
| | SCL, SDA input rise time | t_{Sr} | — | 1000 | ns | |
| | SCL, SDA input fall time | t_{Sf} | — | 300 | ns | |
| | SCL, SDA input spike pulse removal time | t_{SP} | 0 | $1(4) \times t_{IICcyc}$ | ns | |
| | SDA input bus free time | t_{BUF} | $3(6) \times t_{IICcyc} + 300$ | — | ns | |
| | Start condition input hold time | t_{STAH} | $t_{IICcyc} + 300$ | — | ns | |
| | Restart condition input setup time | t_{STAS} | 1000 | — | ns | |
| | Stop condition input setup time | t_{STOS} | 1000 | — | ns | |
| | Data input setup time | t_{SDAS} | $t_{IICcyc} + 50$ | — | ns | |
| | Data input hold time | t_{SDAH} | 0 | — | ns | |
| | SCL, SDA capacitive load | C_b | — | 400 | pF | |
| RIIC (Fast-mode) | SCL input cycle time | t_{SCL} | $6(12) \times t_{IICcyc} + 600$ | — | ns | |
| | SCL input high pulse width | t_{SCLH} | $3(6) \times t_{IICcyc} + 300$ | — | ns | |
| | SCL input low pulse width | t_{SCLL} | $3(6) \times t_{IICcyc} + 300$ | — | ns | |
| | SCL, SDA input rise time | t_{Sr} | $20 + 0.1C_b$ | 300 | ns | |
| | SCL, SDA input fall time | t_{Sf} | $20 + 0.1C_b$ | 300 | ns | |
| | SCL, SDA input spike pulse removal time | t_{SP} | 0 | $1(4) \times t_{IICcyc}$ | ns | |
| | SDA input bus free time | t_{BUF} | $3(6) \times t_{IICcyc} + 300$ | — | ns | |
| | Start condition input hold time | t_{STAH} | $t_{IICcyc} + 300$ | — | ns | |
| | Restart condition input setup time | t_{STAS} | 300 | — | ns | |
| | Stop condition input setup time | t_{STOS} | 300 | — | ns | |
| | Data input setup time | t_{SDAS} | $t_{IICcyc} + 50$ | — | ns | |
| | Data input hold time | t_{SDAH} | 0 | — | ns | |
| | SCL, SDA capacitive load | C_b | — | 400 | pF | |

Note: t_{IICcyc} : RIIC internal reference clock (IIC ϕ) Cycle

Note 1. The value within parentheses is applicable when the value of the ICMR3.NF[1:0] bits is 11b while the digital filter is enabled by the setting ICFER.NFE = 1.

Note 2. C_b is the total capacitance of the bus lines.

Table 5.24 Timing of On-Chip Peripheral Modules (6)

Conditions: VCC = AVCC0 = VREFH = VCC_USB = 2.7 to 3.6 V, VREFH0 = 2.7 V to AVCC0
VSS = AVSS0 = VREFL/VREFLO = VSS_USB = 0 V
PCLK = 8 to 50 MHz
T_a = T_{opr}
High drive output is selected by the drive capacity control register.

| Item | | Symbol | Min.* *2 | Max.* | Unit | Test Conditions |
|--|---|-------------------|-----------------------------------|----------------------------|------|-----------------|
| RIIC (Fast-mode+) ICFER.FMPE = 1 | SCL input cycle time | t _{SCL} | 6(12) × t _{IICcyc} + 240 | — | ns | Figure 5.47 |
| | SCL input high pulse width | t _{SCLH} | 3(6) × t _{IICcyc} + 120 | — | ns | |
| | SCL input low pulse width | t _{SCLL} | 3(6) × t _{IICcyc} + 120 | — | ns | |
| | SCL, SDA input rise time | t _{Sr} | — | 120 | ns | |
| | SCL, SDA input fall time | t _{Sf} | — | 120 | ns | |
| | SCL, SDA input spike pulse removal time | t _{SP} | 0 | 1(4) × t _{IICcyc} | ns | |
| | SDA input bus free time | t _{BUF} | 3(6) × t _{IICcyc} + 120 | — | ns | |
| | Start condition input hold time | t _{STAH} | t _{IICcyc} + 120 | — | ns | |
| | Restart condition input setup time | t _{STAS} | 120 | — | ns | |
| | Stop condition input setup time | t _{STOS} | 120 | — | ns | |
| | Data input setup time | t _{SDAS} | t _{IICcyc} + 120 | — | ns | |
| | Data input hold time | t _{SDAH} | 0 | — | ns | |
| | SCL, SDA capacitive load | C _b | — | 550 | pF | |
| Simple IIC (Standard-mode) | SDA input rise time | t _{Sr} | — | 1000 | ns | |
| | SDA input fall time | t _{Sf} | — | 300 | ns | |
| | SDA input spike pulse removal time | t _{SP} | 0 | 4 × t _{IICcyc} | ns | |
| | Data input setup time | t _{SDAS} | 250 | — | ns | |
| | Data input hold time | t _{SDAH} | 0 | — | ns | |
| | SCL, SDA capacitive load | C _b | — | 400 | pF | |
| Simple IIC (Fast-mode) | SCL, SDA input rise time | t _{Sr} | 20 + 0.1C _b | 300 | ns | |
| | SCL, SDA input fall time | t _{Sf} | 20 + 0.1C _b | 300 | ns | |
| | SCL, SDA input spike pulse removal time | t _{SP} | 0 | 4 × t _{IICcyc} | ns | |
| | Data input setup time | t _{SDAS} | 100 | — | ns | |
| | Data input hold time | t _{SDAH} | 0 | — | ns | |
| | SCL, SDA capacitive load | C _b | — | 400 | pF | |

Note: t_{IICcyc}: RIIC internal reference clock (IICφ) Cycle, t_{Pcyc}: PCLK cycle

Note 1. The value in parentheses is used when ICMR3.NF[1:0] are set to 11b while a digital filter is enabled with ICFER.NFE = 1.

Note 2. C_b indicates the total capacity of the bus line.

Table 5.25 Timing of On-Chip Peripheral Modules (7)

Conditions: VCC = AVCC0 = VREFH = VCC_USB = 2.7 to 3.6 V, VREFH0 = 2.7 V to AVCC0

VSS = AVSS0 = VREFL/VREFL0 = VSS_USB = 0 V

ICLK = 12.5 to 100 MHz, T_a = T_{opr}

High drive output is selected by the drive capacity control register.

| Item | | Symbol | Min. | Max. | Unit | Test Conditions |
|--------------|--|----------------------|------|-------------|------|-------------------------------|
| ETHERC(RMII) | REF50CK cycle time | T _{ck} | 20 | — | ns | Figure 5.48 to Figure 5.51 |
| | REF50CK frequency Typ. 50 MHz | — | — | 50 + 100ppm | MHz | |
| | REF50CK duty | — | 35 | 65 | % | |
| | REF50CK rise/fall time | T _{ckr/ckf} | 0.5 | 3.5 | ns | |
| | RMII_xxxx*1 output delay time | T _{co} | 2.5 | 15.0 | ns | |
| | RMII_xxxx*2 setup time | T _{su} | 3 | — | ns | |
| | RMII_xxxx*2 hold time | T _{hd} | 1 | — | ns | |
| | RMII_xxxx*1, *2 rise/fall time | Tr/Tf | 0.5 | 6 | ns | |
| | ET_WOL output delay time | t _{WOLd} | 1 | 23.5 | ns | |
| ETHERC(MII) | ET_TX_CLK cycle time | t _{Tcyc} | 40 | — | ns | — |
| | ET_TX_EN output delay time | t _{TENd} | 1 | 20 | ns | Figure 5.53 |
| | ET_ETXD0 to ET_ETXD3 output delay time | t _{MTDd} | 1 | 20 | ns | |
| | ET_CRs setup time | t _{CRSs} | 10 | — | ns | |
| | ET_CRs hold time | t _{CRSh} | 10 | — | ns | |
| | ET_COL setup time | t _{COLs} | 10 | — | ns | Figure 5.54 |
| | ET_COL hold time | t _{COLh} | 10 | — | ns | |
| | ET_RX_CLK cycle time | t _{TRcyc} | 40 | — | ns | — |
| | ET_RX_DV setup time | t _{RDVs} | 10 | — | ns | Figure 5.55 |
| | ET_RX_DV hold time | t _{RDVh} | 10 | — | ns | |
| | ET_ERXD0 to ET_ERXD3 setup time | t _{MRDs} | 10 | — | ns | |
| | ET_ERXD0 to ET_ERXD3 hold time | t _{MRDh} | 10 | — | ns | |
| | ET_RX_ER setup time | t _{RERs} | 10 | — | ns | Figure 5.56 |
| | ET_RX_ER hold time | t _{RESh} | 10 | — | ns | |
| | ET_WOL output delay time | t _{WOLd} | 1 | 23.5 | ns | Figure 5.57 |

Note 1. RMII_TXD_EN, RMII_TXD1, RMII_TXD0.

Note 2. RMII_CRs_DV, RMII_RXD1, RMII_RXD0, RMII_RX_ER

Table 5.26 Timing of On-Chip Peripheral Modules (8)

Conditions: VCC = AVCC0 = VREFH = VCC_USB = 2.7 to 3.6V, VREFH0 = 2.7V to AVCC0,
VSS = AVSS0 = VREFL/VREFL0 = VSS_USB = 0V, PIXCLK = 27MHz, T_a = T_{opr}

| Item | Symbol | min | typ | max | Unit | Test Conditions | |
|--------|--|-------------------------|-----|-----|------|-----------------|-------------|
| PDC | VSYNC/HSYNC input setup time | t _{SYNCSSETUP} | 10 | — | — | ns | Figure 5.58 |
| | VSYNC/HSYNC input hold time | t _{SYNCHOLD} | 5 | — | — | ns | |
| | PIXD input setup time | t _{DATASETUP} | 10 | — | — | ns | |
| | PIXD input hold time | t _{DATAHOLD} | 5 | — | — | ns | |
| PIXCLK | PIXCLK input cycle time | t _{PIXcyc} | 37 | — | 1000 | ns | Figure 5.59 |
| | PIXCLK input pulse width high level | t _{PIXH} | 10 | — | — | ns | |
| | PIXCLK input pulse width low level | t _{PIXL} | 10 | — | — | ns | |
| PCKO | PCKO pin output cycle time | t _{PCKcyc} | 40 | — | 1000 | ns | Figure 5.60 |
| | PCKO pin output high level pulse width | t _{PCKH} | 13 | — | — | ns | |
| | PCKO pin output low level pulse width | t _{PCKL} | 13 | — | — | ns | |
| | PCKO pin output rising time | t _{PCKr} | — | — | 5 | ns | |
| | PCKO pin output falling time | t _{PCKf} | — | — | 5 | ns | |
| | | | | | | | |

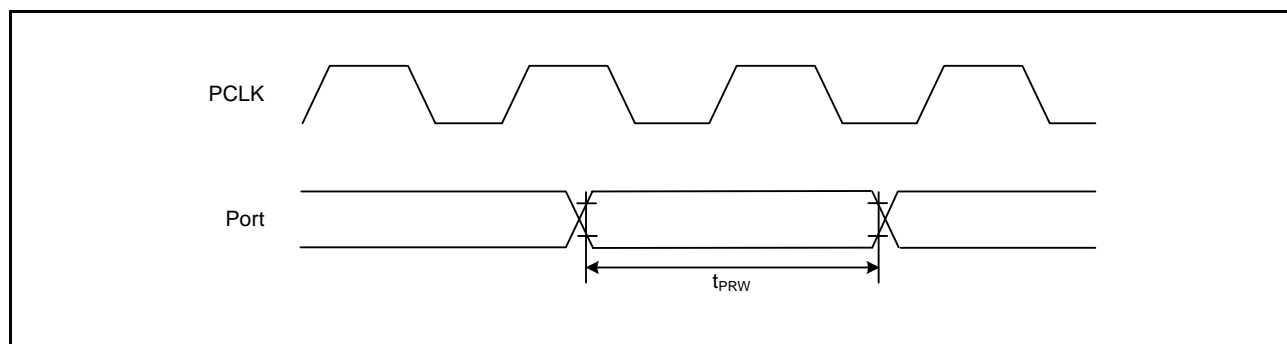


Figure 5.34 I/O Port Input Timing

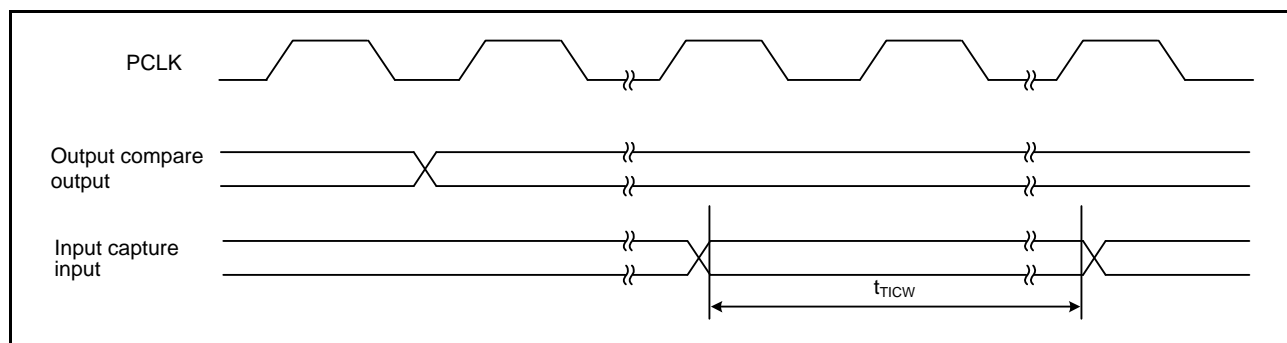


Figure 5.35 MTU Input/Output Timing

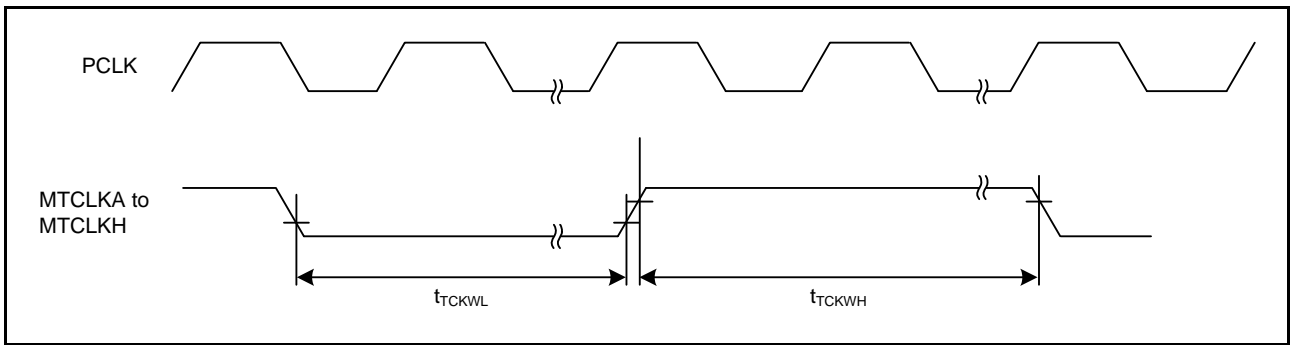


Figure 5.36 MTU Clock Input Timing

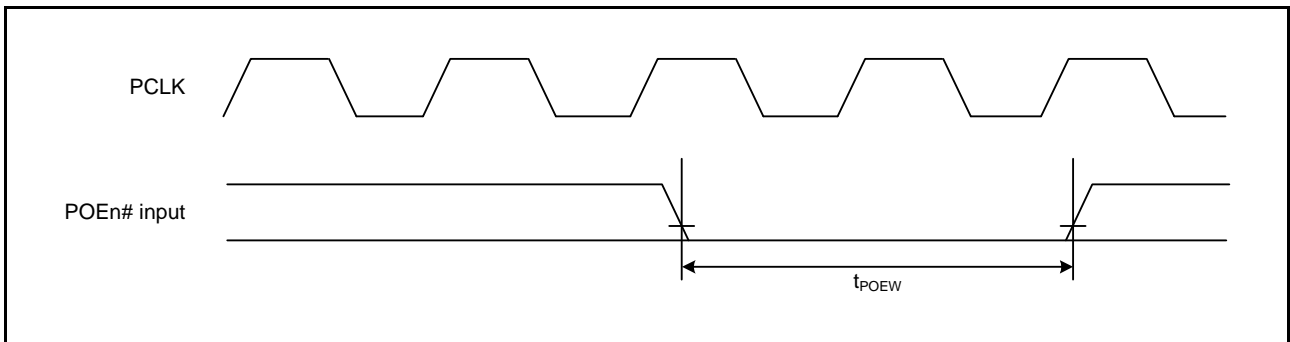


Figure 5.37 POE# Input Timing

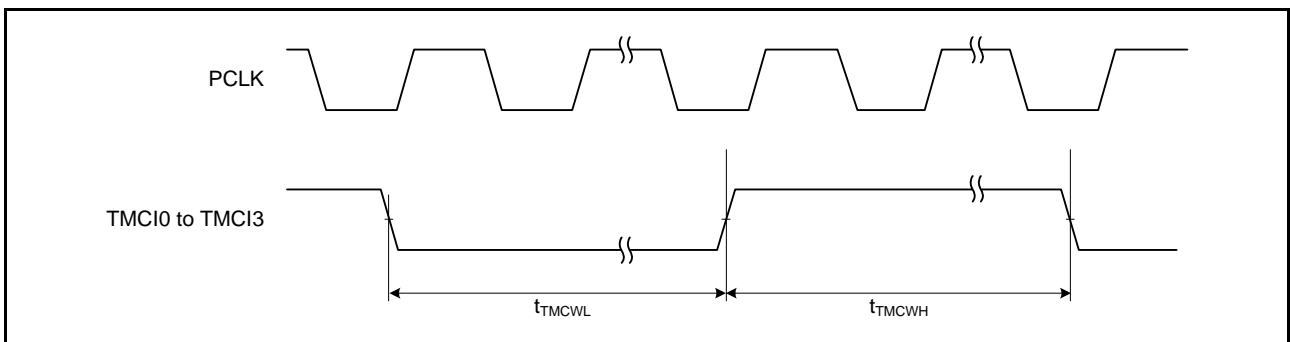


Figure 5.38 8-Bit Timer Clock Input Timing

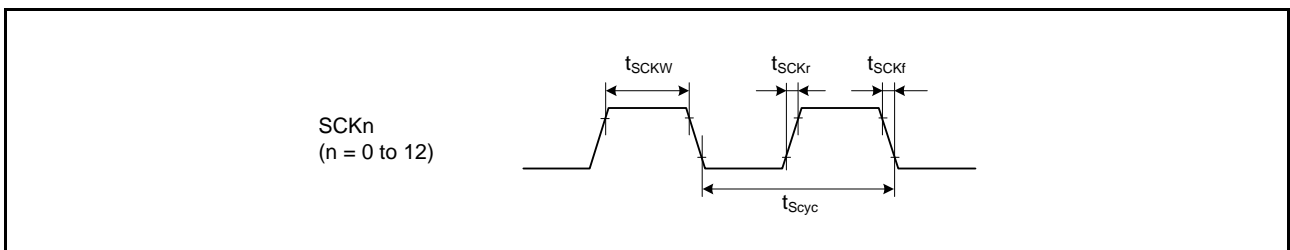


Figure 5.39 SCK Clock Input Timing

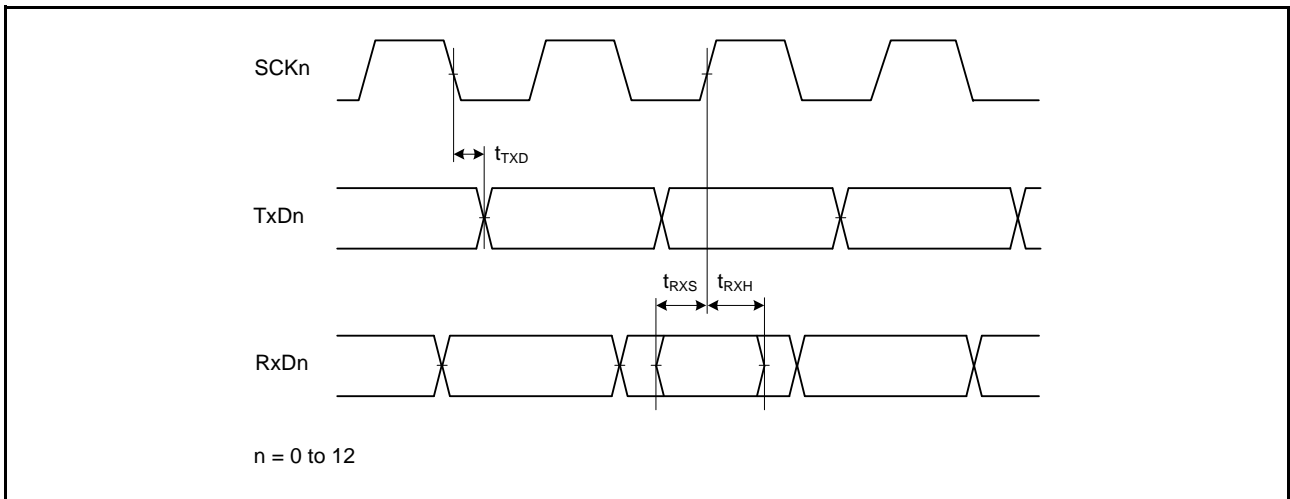


Figure 5.40 SCI Input/Output Timing: Clock Synchronous Mode

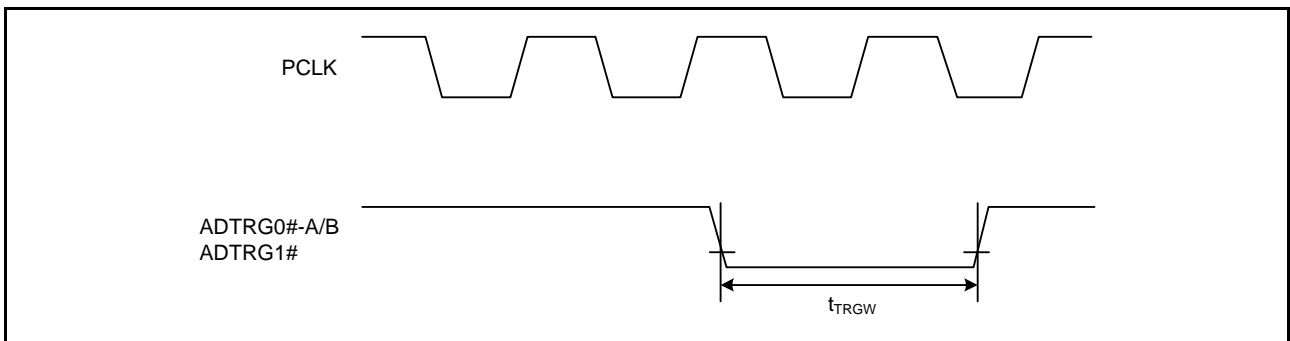


Figure 5.41 A/D Converter External Trigger Input Timing

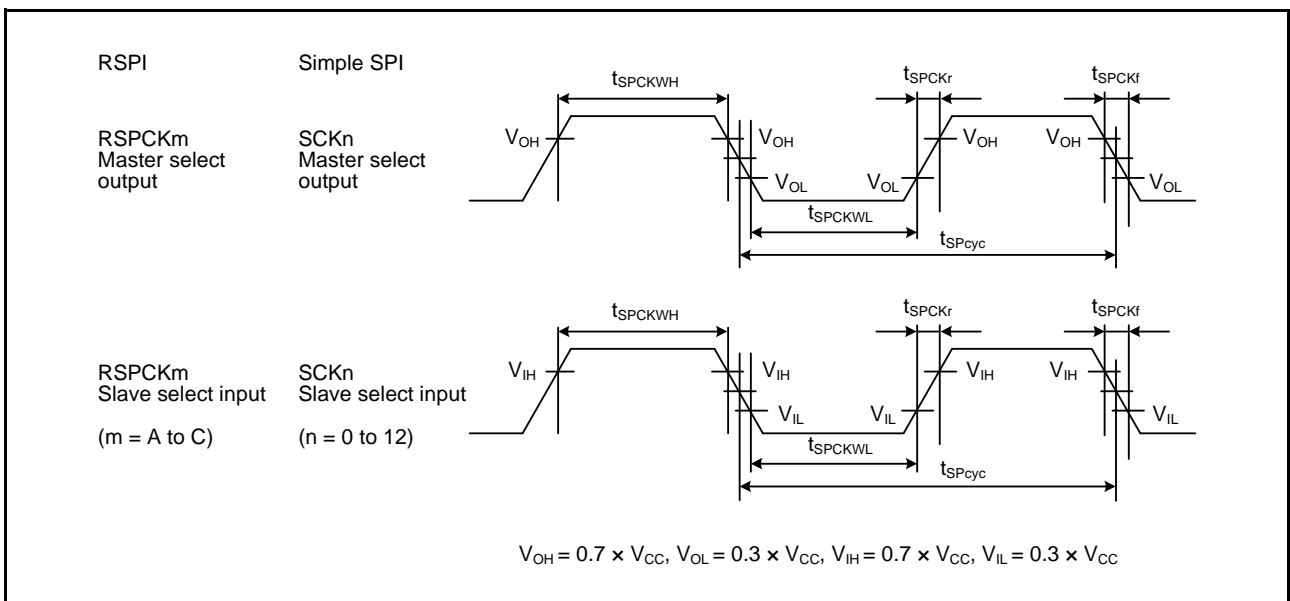


Figure 5.42 RSPi Clock Timing and Simple SPI Clock Timing

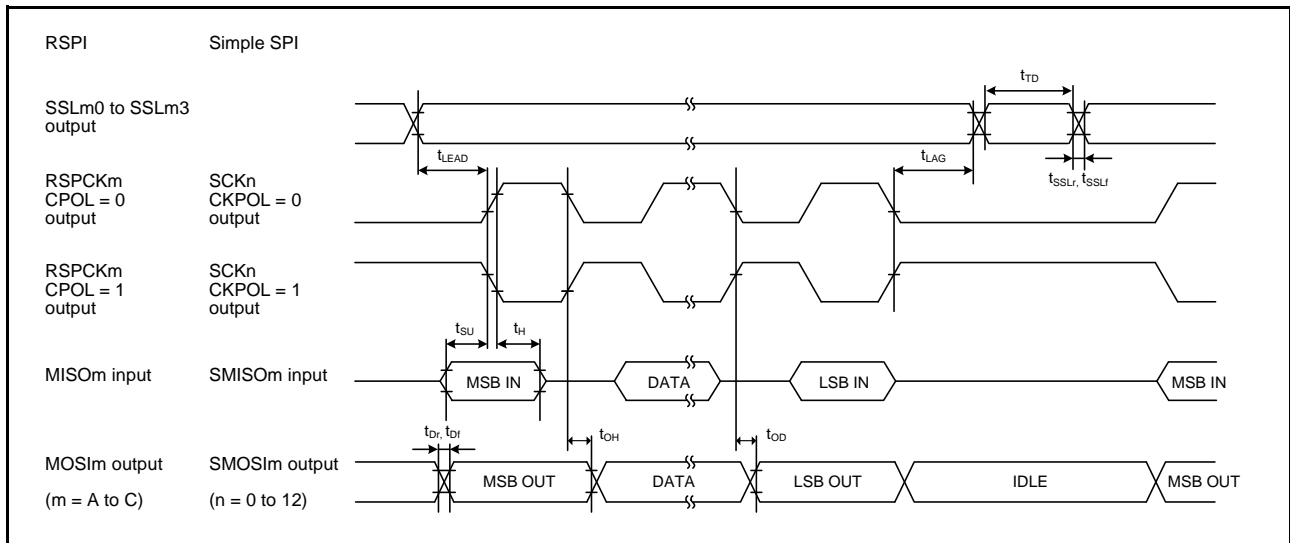


Figure 5.43 RSPI Timing (Master, CPHA = 0) and Simple SPI Timing (Master, CKPH = 1)

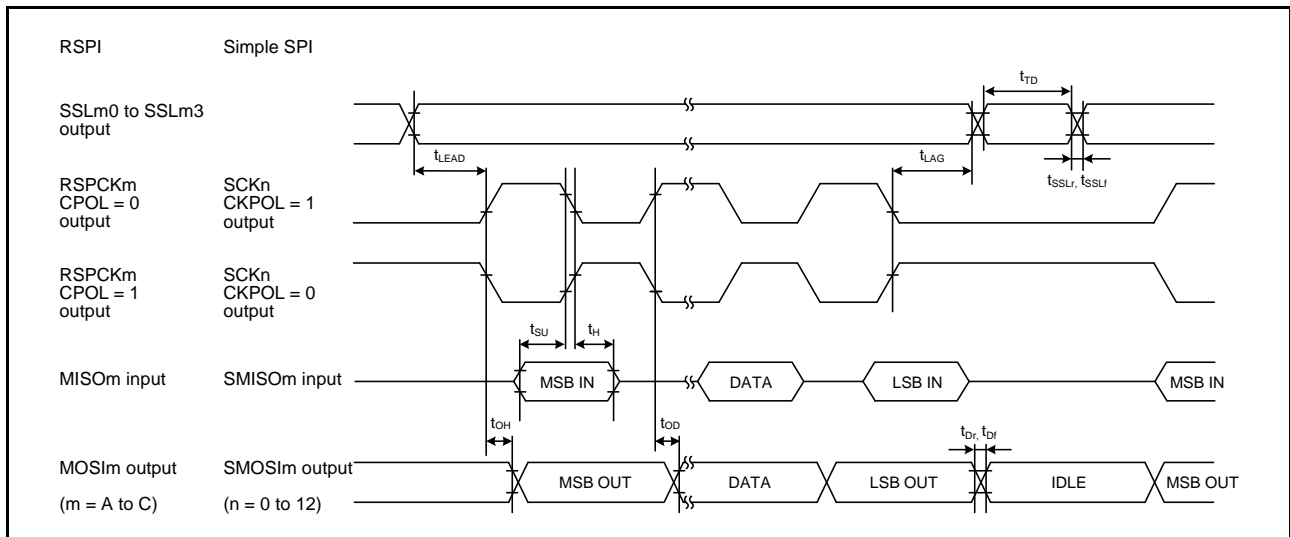


Figure 5.44 RSPI Timing (Master, CPHA = 1) and Simple SPI Timing (Master, CKPH = 0)

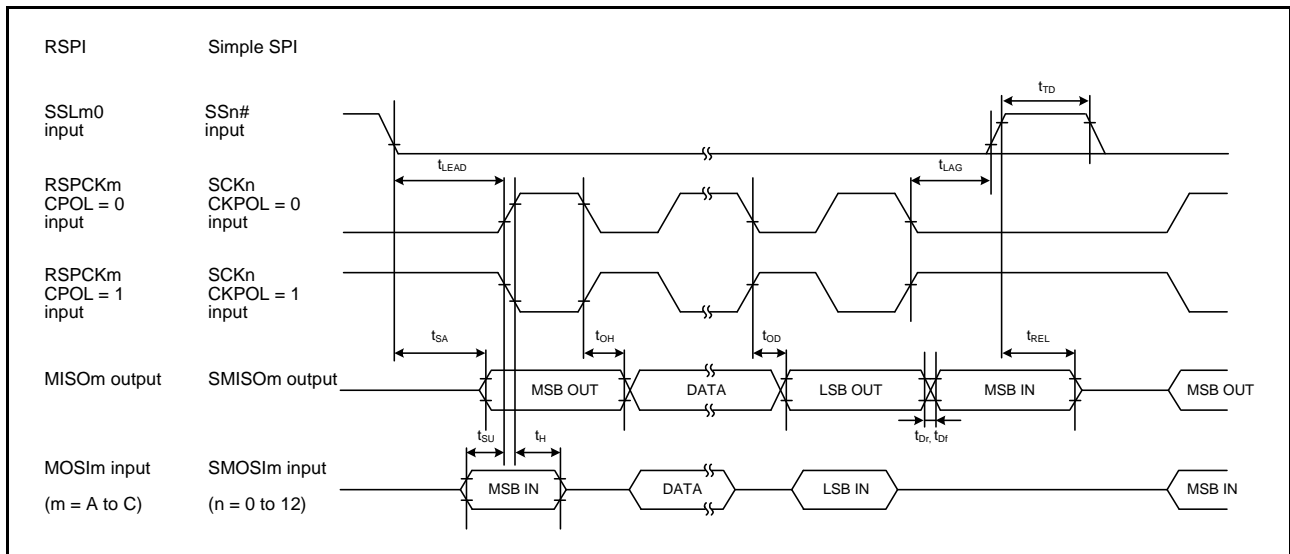


Figure 5.45 RSPI Timing (Slave, CPHA = 0) and Simple SPI Timing (Slave, CKPH = 1)

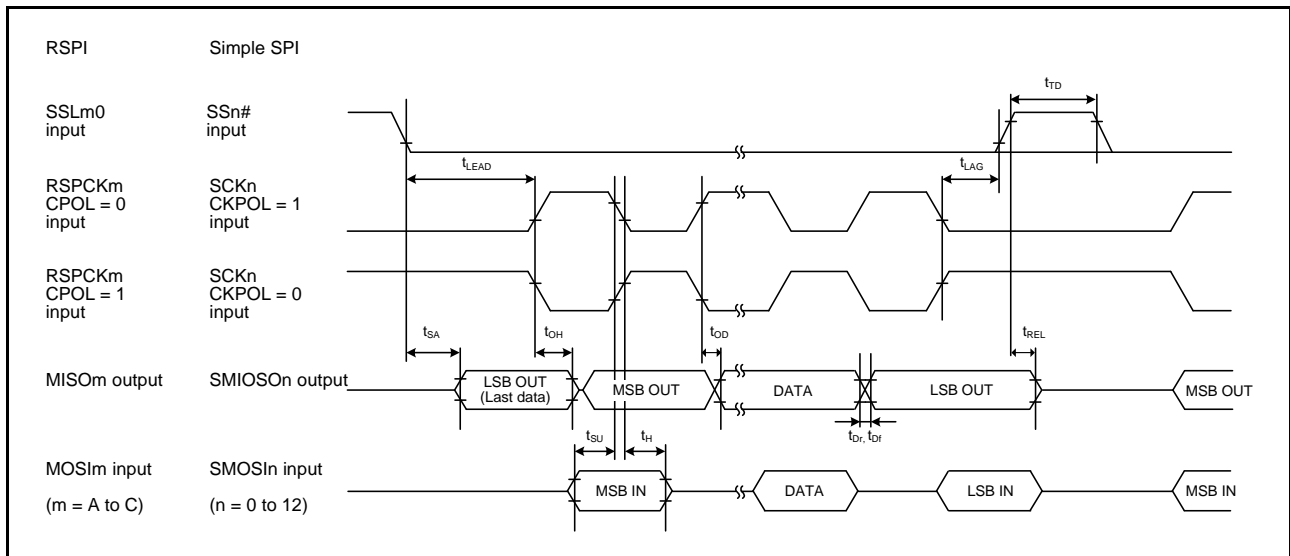


Figure 5.46 RSPI Timing (Slave, CPHA = 1) and Simple SPI Timing (Slave, CKPH = 0)

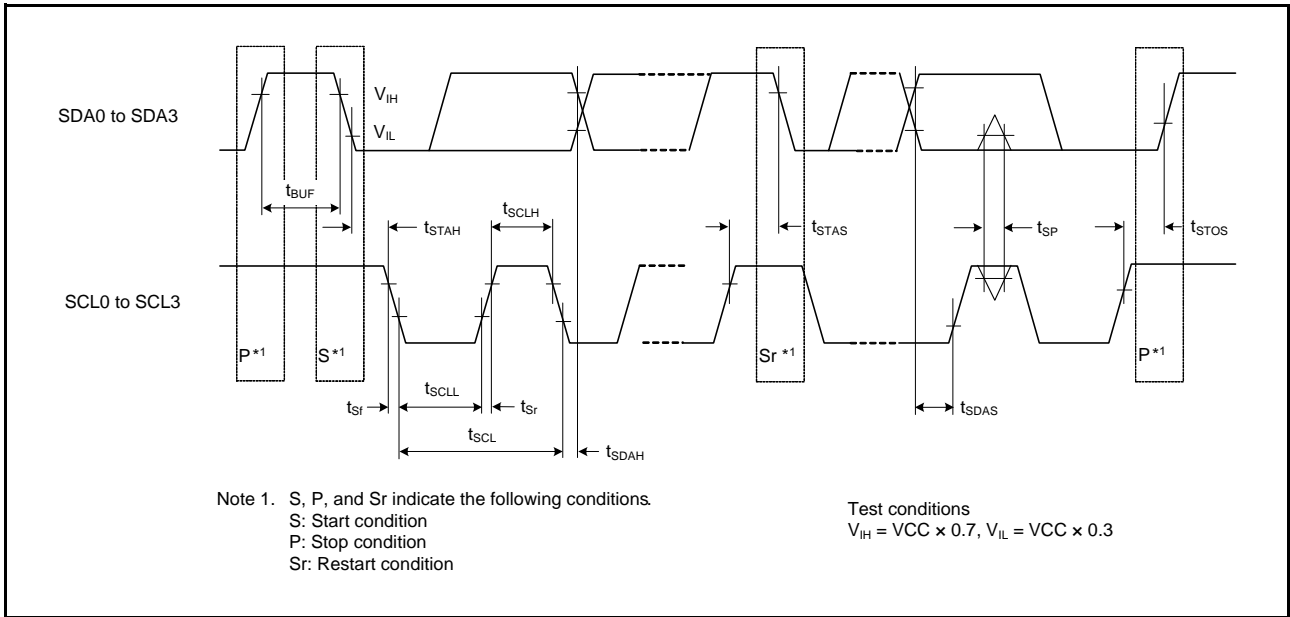


Figure 5.47 IIC Bus Interface Input/Output Timing and Simple IIC Bus Interface Input/Output Timing

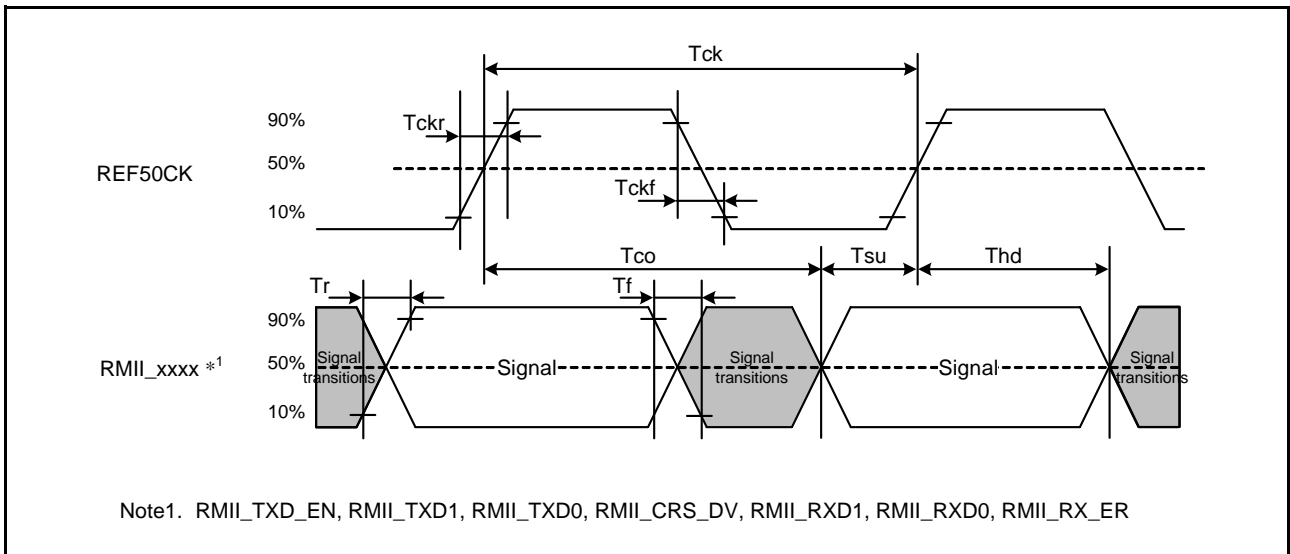


Figure 5.48 REF50CK and RMII Signal Timing

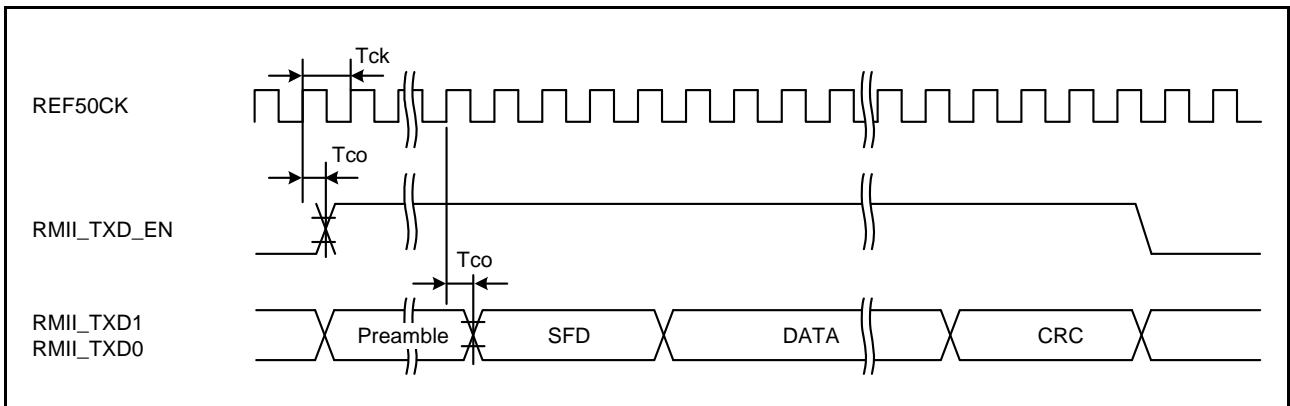


Figure 5.49 RMII Transmission Timing

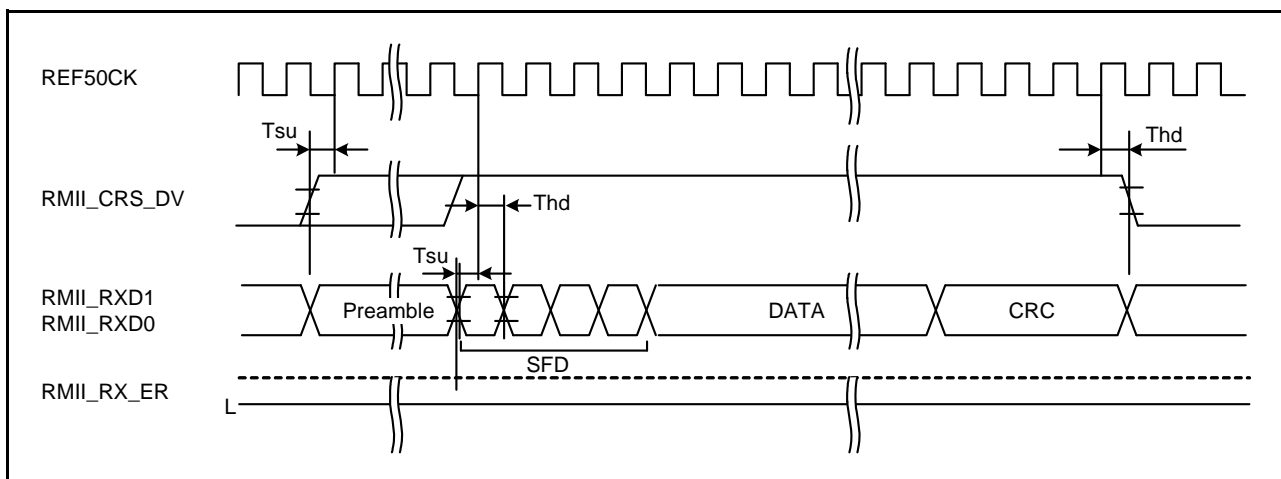


Figure 5.50 RMI Reception Timing (Normal Operation)

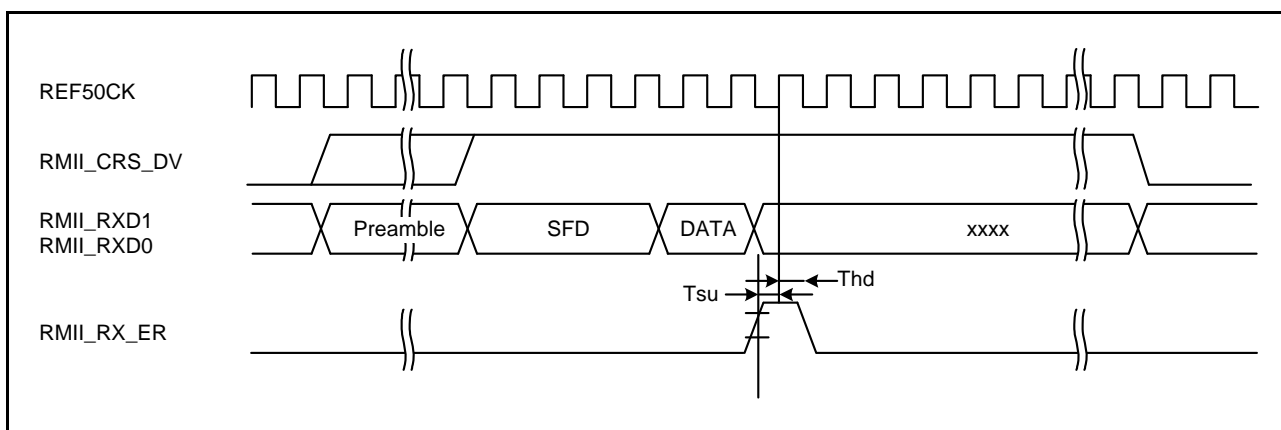


Figure 5.51 RMI Reception Timing (Error Occurrence)

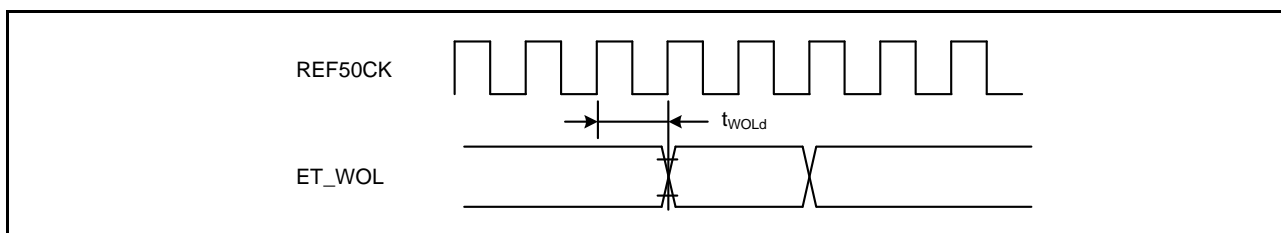


Figure 5.52 WOL Output Timing (RMI)

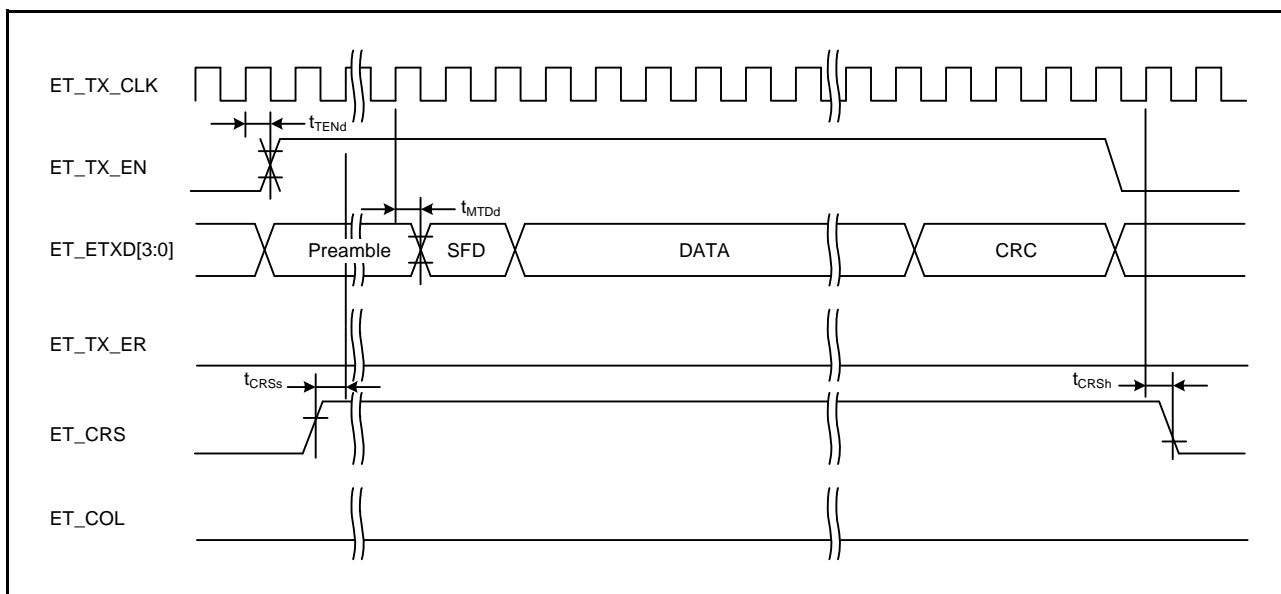


Figure 5.53 MII Transmission Timing (Normal Operation)

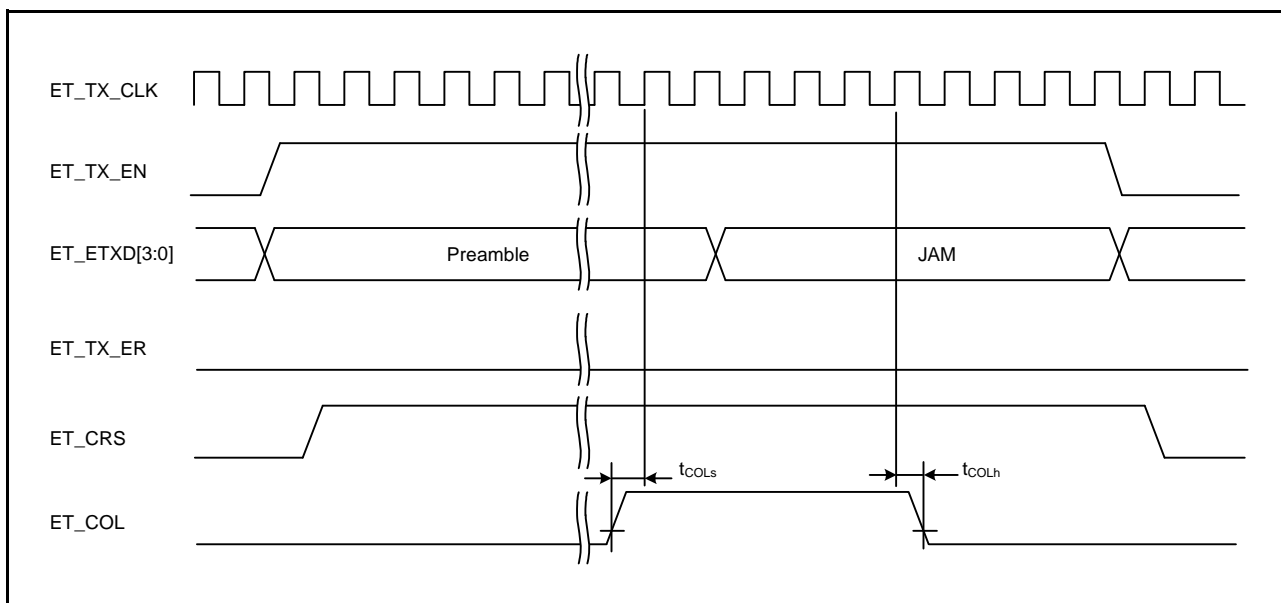


Figure 5.54 MII Transmission Timing (Conflict Occurrence)

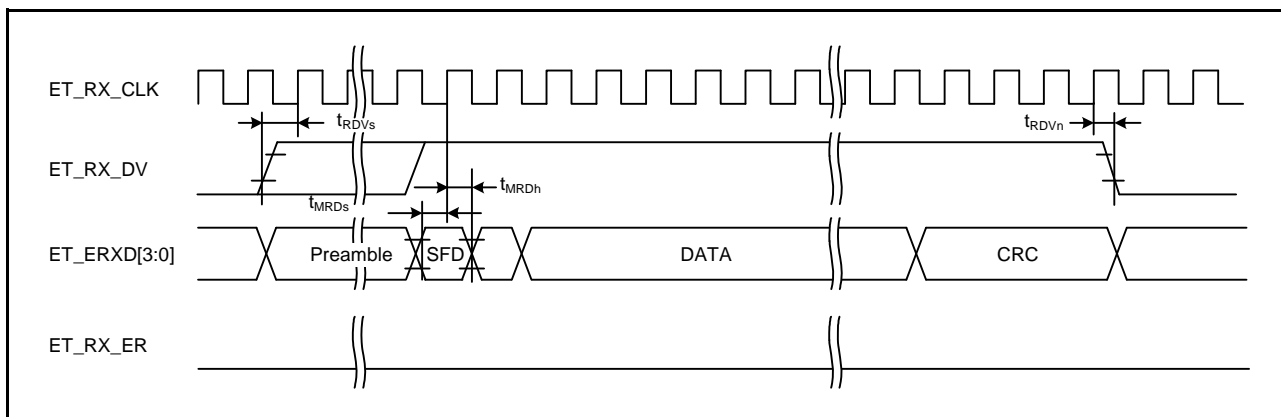


Figure 5.55 MII Reception Timing (Normal Operation)

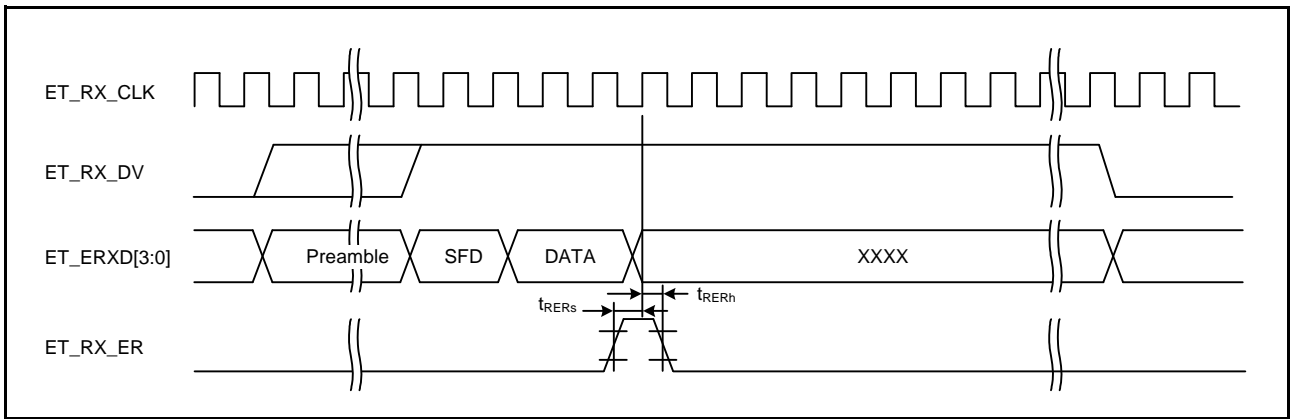


Figure 5.56 MII Reception Timing (Error Occurrence)

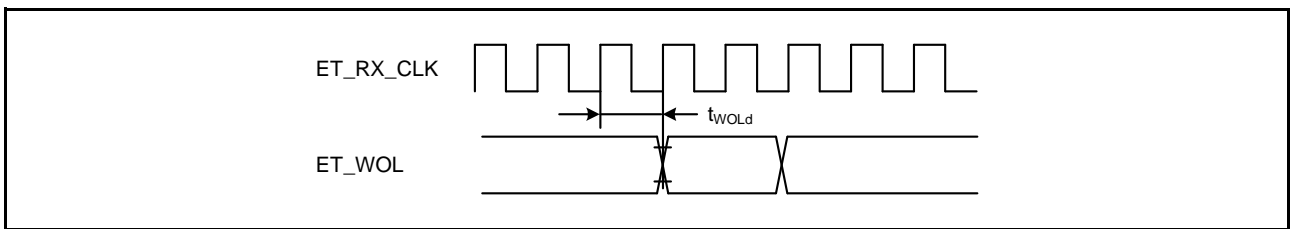


Figure 5.57 WOL Output Timing (MII)

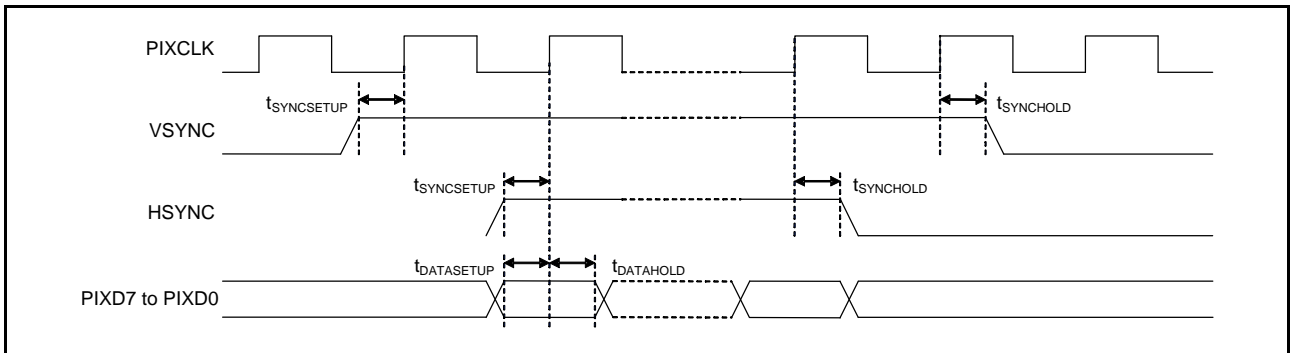


Figure 5.58 PDC Timing

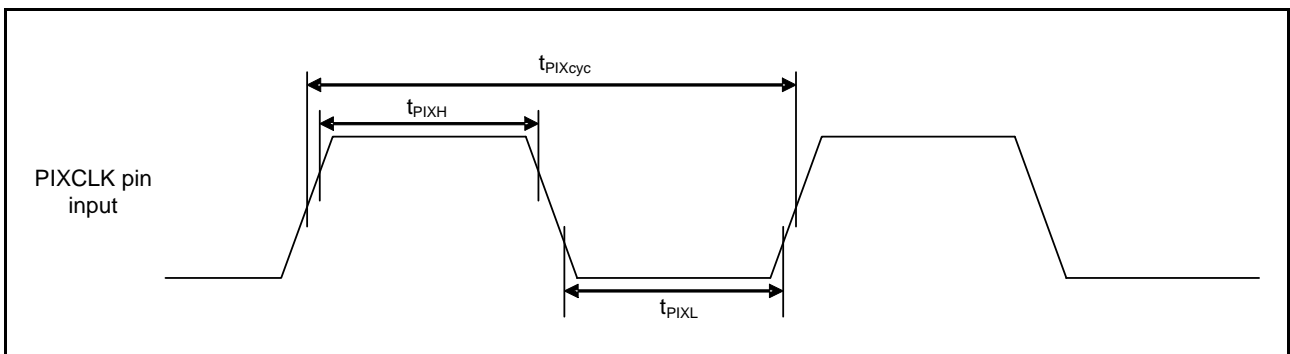


Figure 5.59 PDC Input Clock Characteristic

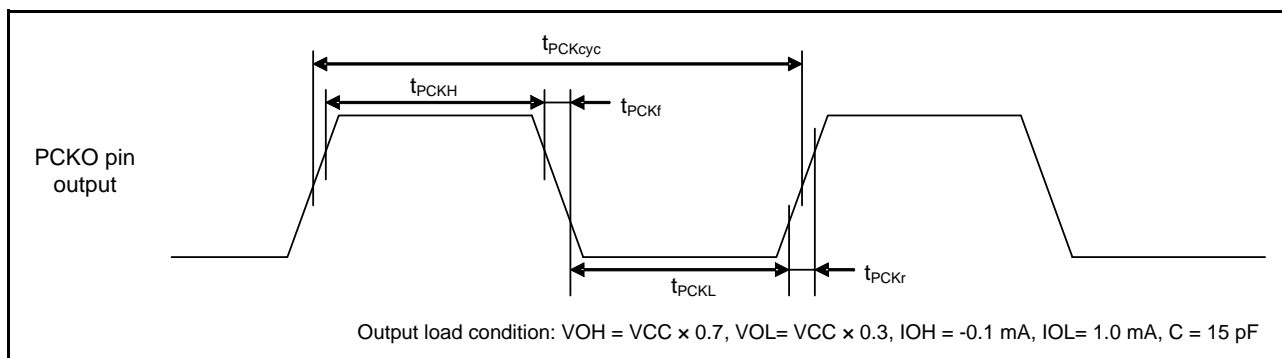


Figure 5.60 PDC Output Clock Characteristic

5.4 USB Characteristics

Table 5.27 On-Chip USB Full-Speed Characteristics (DP and DM Pin Characteristics)

Conditions: $V_{CC} = AV_{CC0} = V_{REFH} = V_{CC_USB} = 3.0$ to 3.6 V, $V_{REFH0} = 3.0$ V to AV_{CC0}
 $V_{SS} = AV_{SS0} = V_{REFL}/V_{REFL0} = V_{SS_USB} = 0$ V
 $PCLK = 24$ to 50 MHz
 $T_a = T_{opr}$
 High drive output is selected by the drive capacity control register.

| Item | | Symbol | Min. | Max. | Unit | Test Conditions | |
|------------------------|--------------------------------|-------------------|------|--------|----------|----------------------------|-------------|
| Input characteristics | Input high level voltage | V_{IH} | 2.0 | — | V | | |
| | Input low level voltage | V_{IL} | — | 0.8 | V | | |
| | Differential input sensitivity | V_{DI} | 0.2 | — | V | DP – DM | |
| | Differential common mode range | V_{CM} | 0.8 | 2.5 | V | | |
| Output characteristics | Output high level voltage | V_{OH} | 2.8 | 3.6 | V | $I_{OH} = -200 \mu A$ | |
| | Output low level voltage | V_{OL} | 0.0 | 0.3 | V | $I_{OL} = 2$ mA | |
| | Cross-over voltage | V_{CRS} | 1.3 | 2.0 | V | | Figure 5.61 |
| | Rise time | t_{Lr} | 4 | 20 | ns | | |
| | Fall time | t_{Lf} | 4 | 20 | ns | | |
| | Rise/fall time ratio | t_{Lr} / t_{Lf} | 90 | 111.11 | % | t_{Lr} / t_{Lf} | |
| | Output resistance | Z_{DRV} | 28 | 44 | Ω | $R_s = 22 \Omega$ included | |

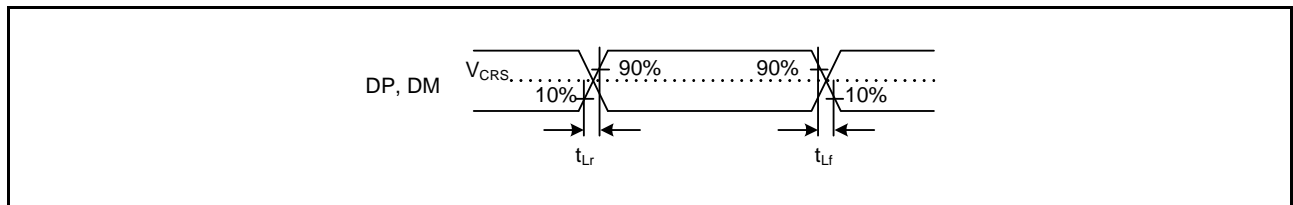


Figure 5.61 DP and DM Output Timing (Full-Speed)

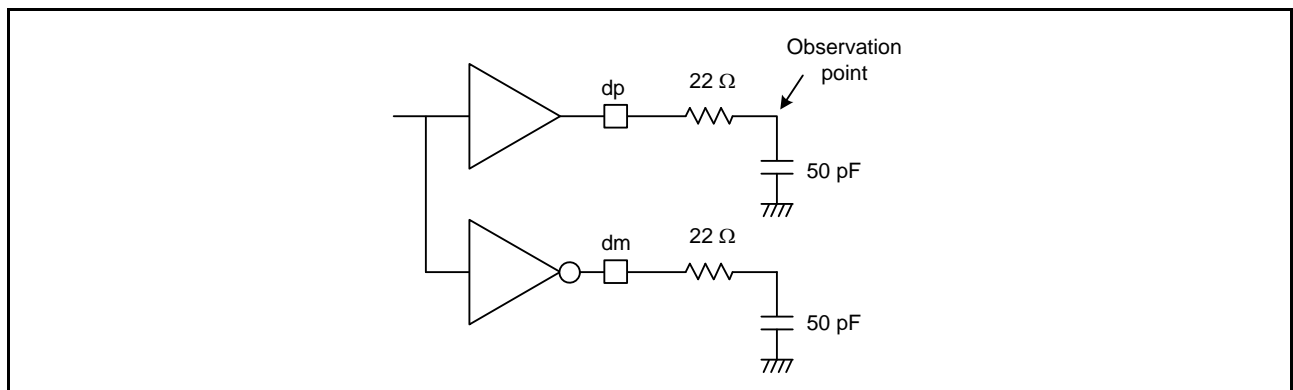


Figure 5.62 Test Circuit (Full-Speed)

5.5 A/D Conversion Characteristics

Table 5.28 10-Bit A/D Conversion Characteristics

Conditions: $V_{CC} = AV_{CC0} = V_{REFH} = V_{CC_USB} = 2.7$ to 3.6 V, $V_{REFH0} = 2.7$ V to AV_{CC0}
 $V_{SS} = AV_{SS0} = V_{REFL}/V_{REFL0} = V_{SS_USB} = 0$ V
 $PCLK = 8$ to 50 MHz
 $T_a = T_{opr}$

| Item | | Min. | Typ. | Max. | Unit | Test Conditions | |
|---|---|---|-------------|-----------|------|-----------------|------------------------|
| Resolution | | — | — | 10 | Bit | | |
| Conversion time*1 (Operation at $PCLK = 50$ MHz) | With 0.1- μ F external capacitor | When the capacitor is charged enough*2 | 3.0 (2.5)*3 | — | — | μ s | Sampling in 125 states |
| | Without 0.1- μ F external capacitor | Permissible signal source impedance (max.) = 1.0 k Ω , $V_{CC} \geq 3.0$ V | 1.5 (1.0)*3 | — | — | | Sampling in 50 states |
| | | Permissible signal source impedance (max.) = 1.0 k Ω , $V_{CC} \geq 2.7$ V | 3.5 (3.0)*3 | — | — | | Sampling in 150 states |
| | | Permissible signal source impedance (max.) = 5.0 k Ω , $V_{CC} \geq 3.0$ V | 2.0 (1.5)*3 | — | — | | Sampling in 75 states |
| | | Permissible signal source impedance (max.) = 5.0 k Ω , $V_{CC} \geq 2.7$ V | 4.0 (3.5)*3 | — | — | | Sampling in 175 states |
| Analog input capacitance | | — | — | 6.0 | pF | | |
| Offset error | | — | ± 1.5 | ± 3.0 | LSB | | |
| Full-scale error | | — | ± 1.5 | ± 3.0 | LSB | | |
| Quantization error | | — | ± 0.5 | — | LSB | | |
| Absolute accuracy | | — | ± 1.5 | ± 3.0 | LSB | | |
| DNL differential nonlinearity error | | — | ± 0.5 | ± 1.0 | LSB | | |
| INL integral nonlinearity error | | — | ± 1.5 | ± 3.0 | LSB | | |

Note: The above specification values apply when there is no access to the external bus during A/D conversion. If access proceeds during A/D conversion, values may not fall within the above ranges.

Note 1. The conversion time includes the sampling time and the comparison time. As the test conditions, the number of sampling states is indicated.

Note 2. The scanning is not supported.

Note 3. The value in parentheses indicates the sampling time.

Table 5.29 12-Bit A/D Conversion Characteristics

Conditions: $V_{CC} = AVCC0 = VREFH = VCC_USB = 2.7$ to 3.6 V, $VREFH0 = 2.7$ V to $AVCC0$
 $VSS = AVSS0 = VREFL/VREFLO = VSS_USB = 0$ V
 $PCLK = 8$ to 50 MHz
 $T_a = T_{opr}$

| Item | | | Min. | Typ. | Max. | Unit | Test Conditions |
|---|----------------|---|------------------|-----------|-----------|---------|------------------------|
| Resolution | | | — | — | 12 | Bit | |
| Conversion time*1 (Operation at $PCLK = 50$ MHz) | AN0 to AN7 | Permissible signal source impedance (max.) = 1.0 k Ω | $1.0 (0.4)^{*2}$ | — | — | μ s | Sampling in 20 states |
| | Other channels | Permissible signal source impedance (max.) = 1.0 k Ω , $AVCC \geq 3.0$ V | $2.0 (1.4)^{*2}$ | — | — | μ s | Sampling in 70 states |
| | | Permissible signal source impedance (max.) = 1.0 k Ω , $AVCC \geq 2.7$ V | $5.6 (5.0)^{*2}$ | — | — | μ s | Sampling in 250 states |
| Analog input capacitance | | | — | — | 30 | pF | |
| Offset error | | | — | ± 2.0 | ± 7.5 | LSB | |
| Full-scale error | | | — | ± 2.0 | ± 7.5 | LSB | |
| Quantization error | | | — | ± 0.5 | — | LSB | |
| Absolute accuracy | | | — | ± 2.5 | ± 8.0 | LSB | |
| DNL differential nonlinearity error | | | — | ± 2.0 | ± 4.0 | LSB | |
| INL integral nonlinearity error | | | — | ± 2.0 | ± 4.0 | LSB | |

Note: The above specification values apply when there is no access to the external bus during A/D conversion. If access proceeds during A/D conversion, values may not fall within the above ranges.

Note 1. The conversion time includes the sampling time and the comparison time. As the test conditions, the number of sampling states is indicated.

Note 2. The value in parentheses indicates the sampling time.

Table 5.30 A/D Internal Reference Voltage Characteristics

Conditions: $V_{CC} = AVCC0 = VREFH = VCC_USB = 2.7$ to 3.6 V, $VREFH0 = 2.7$ V to $AVCC0$
 $VSS = AVSS0 = VREFL/VREFLO = VSS_USB = 0$ V
 $PCLK = 8$ to 50 MHz
 $T_a = T_{opr}$

| Item | Min. | Typ. | Max. | Unit | Test Conditions |
|--------------------------------|------|------|------|------|-----------------|
| A/D Internal reference voltage | 1.45 | 1.50 | 1.55 | V | |

5.6 D/A Conversion Characteristics

Table 5.31 D/A Conversion Characteristics

Conditions: $VCC = AVCC0 = VREFH = VCC_USB = 2.7$ to 3.6 V, $VREFH0 = 2.7$ V to VCC
 $VSS = AVSS0 = VREFL/VREFL0 = VSS_USB = 0$ V
 $T_a = T_{opr}$

| Item | Min. | Typ. | Max. | Unit | Test Conditions |
|----------------------|------|-----------|-----------|------------|------------------------------|
| Resolution | 10 | 10 | 10 | Bit | |
| Conversion time | — | — | 3.0 | μ s | 20-pF capacitive load |
| Absolute accuracy | — | ± 2.0 | ± 4.0 | LSB | 2-M Ω resistive load |
| | — | — | ± 3.0 | LSB | 4-M Ω resistive load |
| | — | — | ± 2.0 | LSB | 10-M Ω resistive load |
| RO output resistance | — | 3.6 | — | k Ω | |

5.7 Temperature Sensor Characteristics

Table 5.32 Temperature Sensor Characteristics

Conditions: $VCC = AVCC0 = VREFH = VCC_USB = 2.7$ to 3.6 V, $VREFH0 = 2.7$ V to VCC
 $VSS = AVSS0 = VREFL/VREFL0 = VSS_USB = 0$ V
 $T_a = T_{opr}$

| Item | Min. | Typ. | Max. | Unit | Test Conditions |
|-----------------------------------|------|---------|------|------------------|-----------------|
| Relative accuracy | — | ± 1 | — | $^{\circ}$ C | |
| Temperature slope | — | 4.1 | — | mV/ $^{\circ}$ C | |
| Output voltage (@25 $^{\circ}$ C) | — | 1.26 | — | V | |
| Temperature sensor start time | — | — | 30 | μ s | |
| Sampling time | — | — | 5 | μ s | |

5.8 Power-on Reset Circuit and Voltage Detection Circuit Characteristics

Table 5.33 Power-on Reset Circuit and Voltage Detection Circuit Characteristics

Conditions: $V_{CC} = AV_{CC0} = V_{REFH} = V_{CC_USB} = V_{BATT} = 2.7$ to 3.6 V, $V_{REFH0} = 2.7$ V to AV_{CC0}
 $V_{SS} = AV_{SS0} = V_{REFL}/V_{REFL0} = V_{SS_USB} = 0$ V
 $T_a = T_{opr}$

| Item | | Symbol | Min. | Typ. | Max. | Unit | Test Conditions | |
|---|----------------------------------|---|---------------|------|------|------|-----------------|-----------------------------|
| Voltage detection level | Power-on reset (POR) | Low power consumption function disabled | V_{POR} | 2.5 | 2.6 | 2.7 | V | Figure 5.63 |
| | | Low power consumption function enabled | | 2.0 | 2.35 | 2.7 | | |
| | Voltage detection circuit (LVD0) | | V_{det0} | 2.7 | 2.80 | 2.9 | | Figure 5.64 |
| | Voltage detection circuit (LVD1) | | V_{det1_A} | 2.75 | 2.95 | 3.15 | | Figure 5.65 |
| | Voltage detection circuit (LVD2) | | V_{det2_A} | 2.75 | 2.95 | 3.15 | | Figure 5.66 |
| Internal reset time | Power-on reset time | | t_{POR} | — | 4.6 | — | ms | Figure 5.63 |
| | LVD0 reset time | | t_{LVD0} | — | 4.6 | — | | Figure 5.64 |
| | LVD1 reset time | | t_{LVD1} | — | 0.9 | — | | Figure 5.65 |
| | LVD2 reset time | | t_{LVD2} | — | 0.9 | — | | Figure 5.66 |
| Minimum VCC down time | | | t_{VOFF} | 200 | — | — | μ s | Figure 5.63 and Figure 5.64 |
| Response delay time | | | t_{det} | — | — | 200 | μ s | Figure 5.63 to Figure 5.66 |
| LVD operation stabilization time (after LVD is enabled) | | | $T_{d(E-A)}$ | — | — | 3 | μ s | Figure 5.65 and Figure 5.66 |
| Hysteresis width (LVD1 and LVD2) | | | V_{LVH} | — | 80 | — | mV | |

Note: The minimum VCC down time indicates the time when VCC is below the minimum value of voltage detection levels V_{POR} , V_{det1} , and V_{det2} for the POR/ LVD.

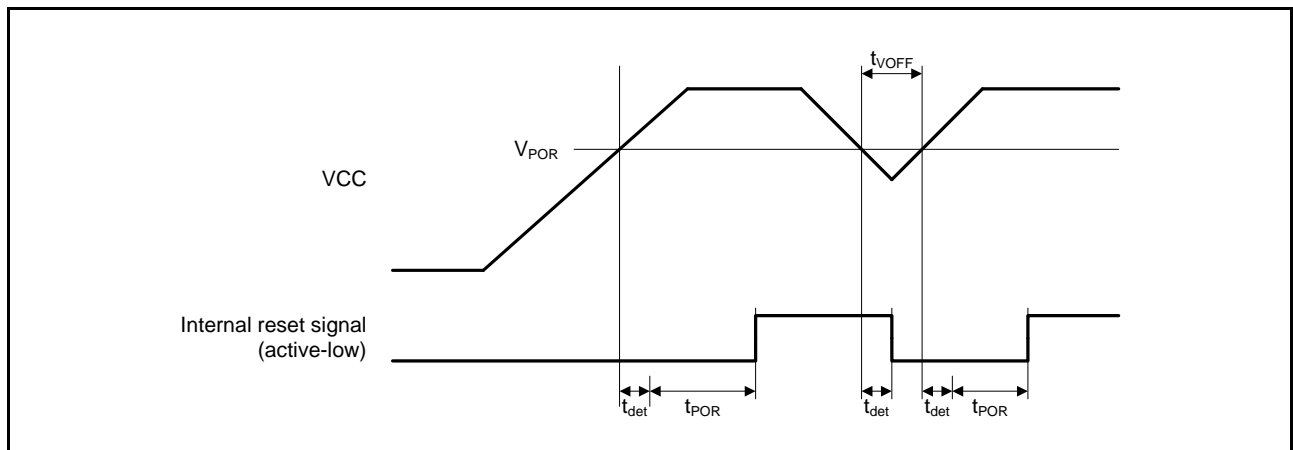


Figure 5.63 Power-on Reset Timing

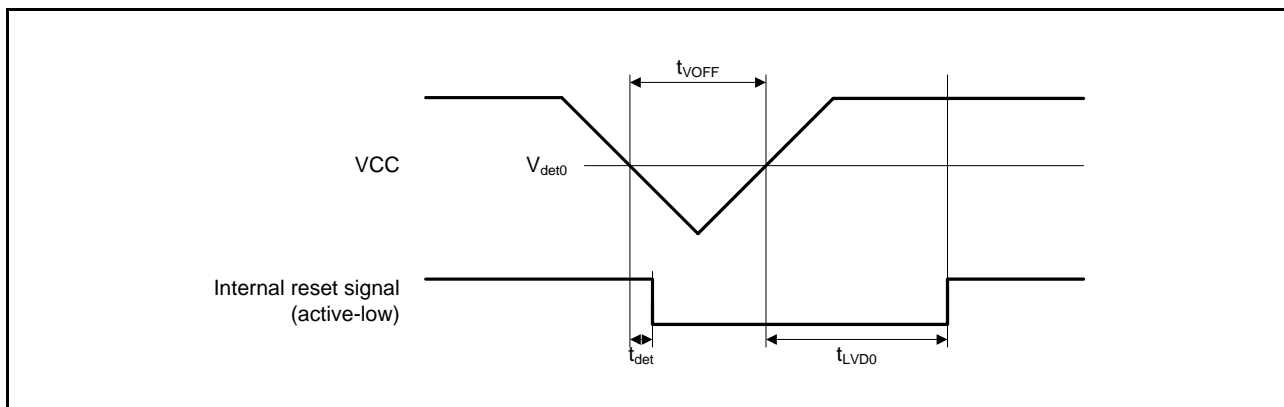


Figure 5.64 Voltage Detection Circuit Timing (V_{det0})

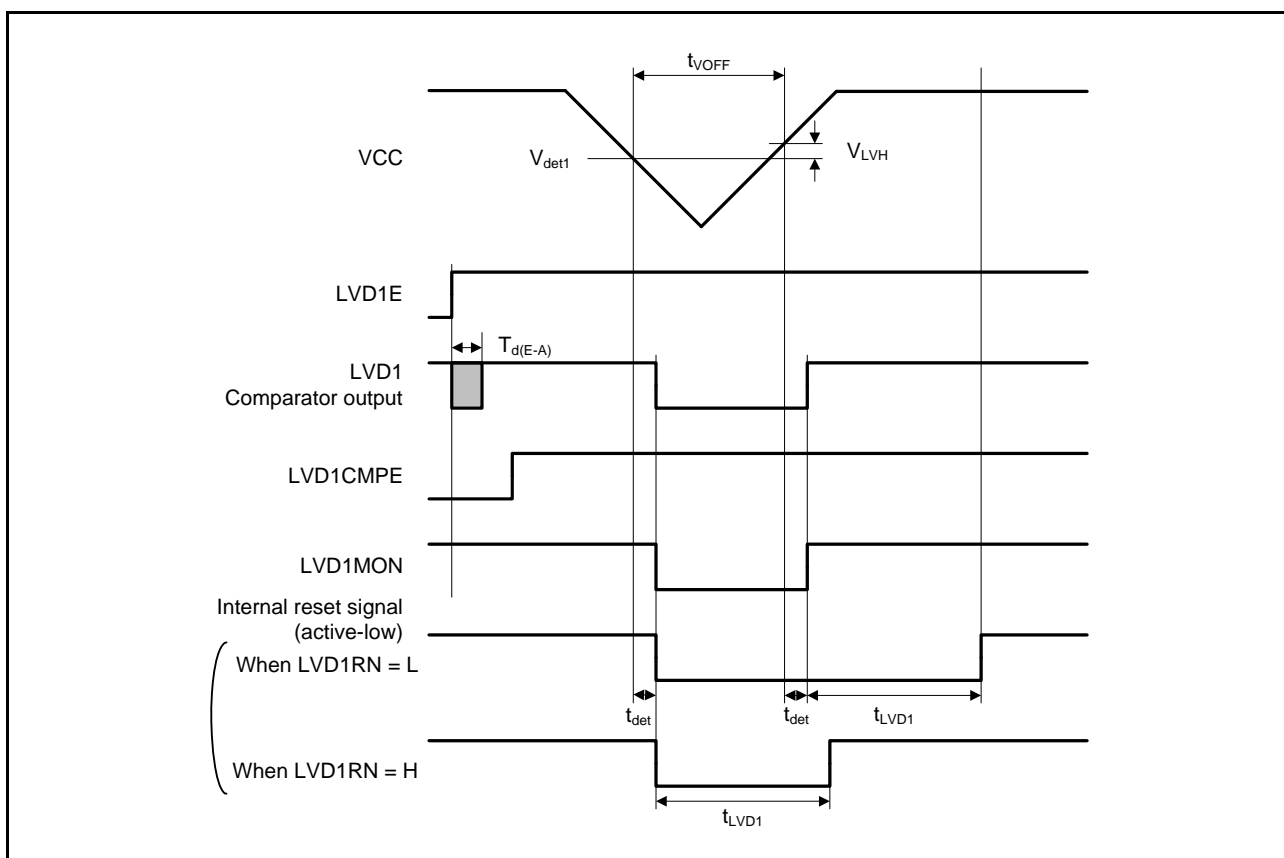


Figure 5.65 Voltage Detection Circuit Timing (V_{det1})

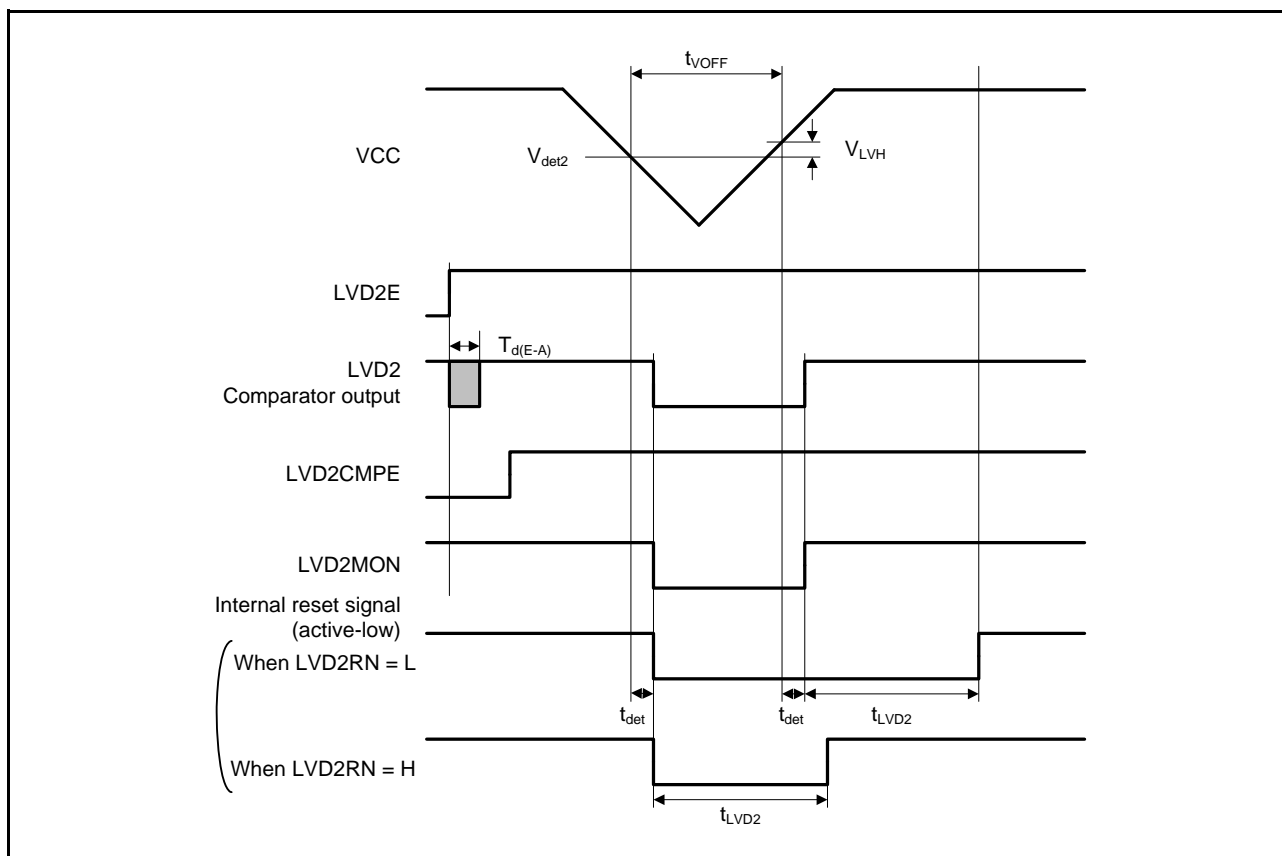


Figure 5.66 Voltage Detection Circuit Timing (V_{det2})

5.9 Oscillation Stop Detection Timing

Table 5.34 Oscillation Stop Detection Circuit Characteristics

Conditions: VCC = AVCC0 = VREFH = VCC_USB = V_{BATT} = 2.7 to 3.6 V, VREFH0 = 2.7 V to AVCC0
 VSS = AVSS0 = VREFL/VREFL0 = VSS_USB = 0 V
 T_a = T_{opr}

| Item | Symbol | Min. | Typ. | Max. | Unit | Test Conditions |
|----------------|-----------------|------|------|------|------|-----------------|
| Detection time | t _{dr} | — | — | 1 | ms | Figure 5.67 |

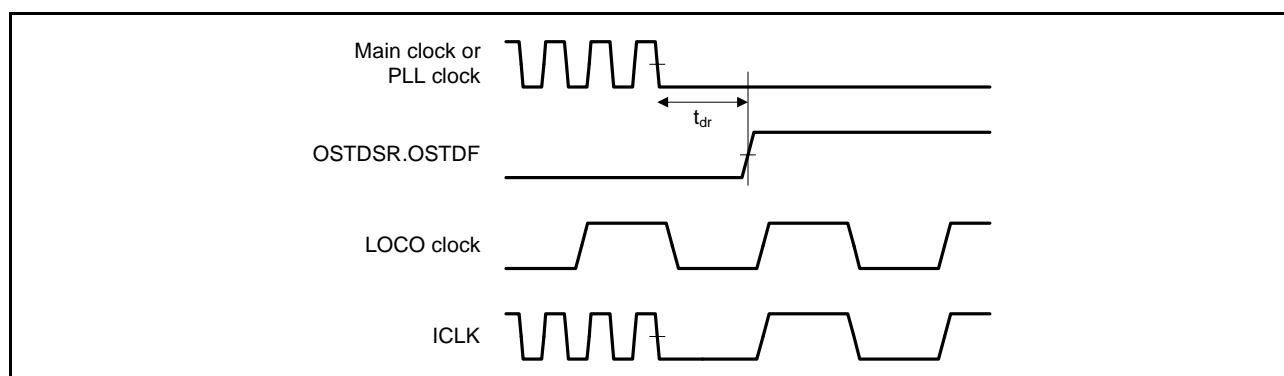


Figure 5.67 Oscillation Stop Detection Timing

5.10 Battery Backup Function Characteristics

Table 5.35 Battery Backup Function Characteristics

Conditions: $V_{CC} = AVCC0 = VREFH = VCC_USB = 2.7$ to 3.6 V, $VREFH0 = 2.7$ V to $AVCC0$, $V_{BATT} = 2.0$ to 3.6 V (for products with 100 pins or more), $V_{BATT} = 2.3$ to 3.6 V (for the 64-pin product)
 $VSS = AVSS0 = VREFL/VREFLO = VSS_USB = 0$ V
 $T_a = T_{opr}$

| Item | Symbol | Min. | Typ. | Max. | Unit | Test Conditions |
|---|----------------|------|------|------|---------|-----------------|
| Voltage level for switching to battery backup | $V_{DETBATT}$ | 2.50 | 2.60 | 2.70 | V | Figure 5.68 |
| Lower-limit V_{BATT} voltage for power supply switching due to VCC voltage drop | V_{BATTSW} | 2.70 | — | — | | |
| VCC-off period for starting power supply switching | $t_{VOFFBATT}$ | 200 | — | — | μs | |

Note: The VCC-off period for starting power supply switching indicates the period in which VCC is below the minimum value of the voltage level for switching to battery backup ($V_{DETBATT}$).

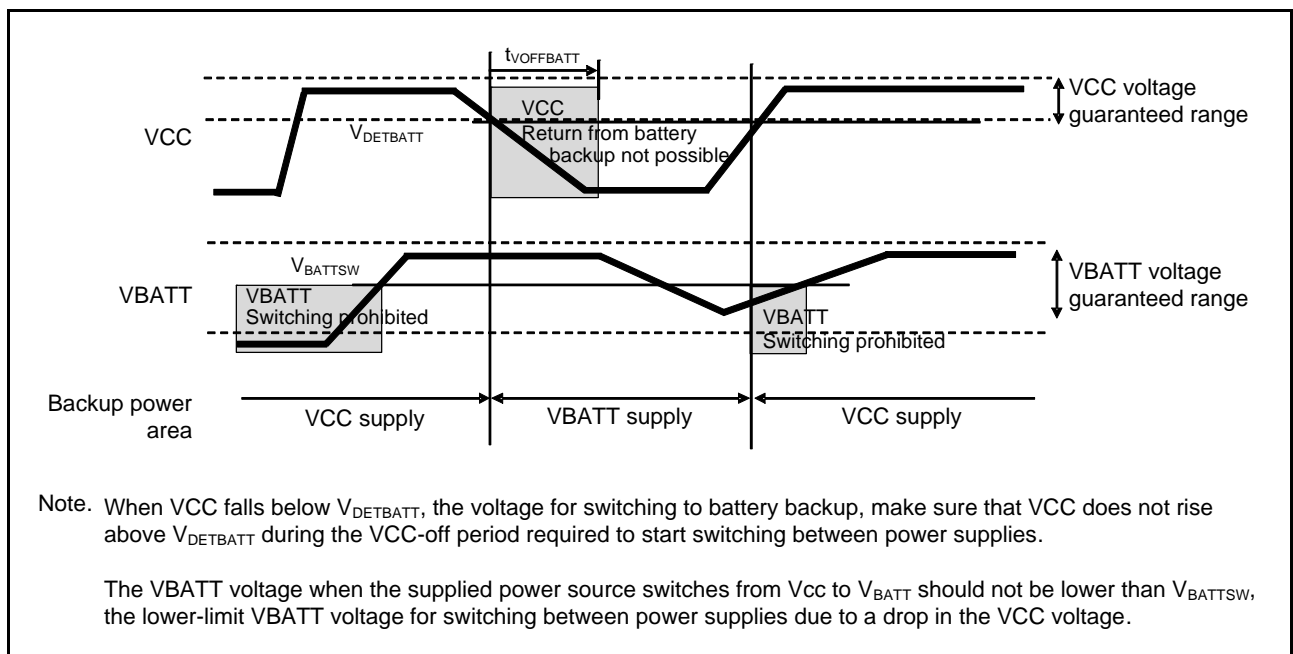


Figure 5.68 Battery Backup Function Characteristics

5.11 ROM (Flash Memory for Code Storage) Characteristics

Table 5.36 ROM (Flash Memory for Code Storage) Characteristics (1)

Conditions: VCC = AVCC0 = VREFH = VCC_USB = 2.7 to 3.6V, VREFH0 = 2.7V to AVCC0
 VSS = AVSS0 = VREFL/VREFL0 = VSS_USB = 0V
 Temperature range for the programming/erasure operation: T_a = T_{opr}

| Item | Symbol | min | typ | max | Unit | Condition |
|---------------------------|------------------|------|-----|-----|-------|------------------------|
| Reprogram/erasure cycle*1 | N _{PEC} | 1000 | — | — | Times | |
| Data hold time | t _{DRP} | 30*2 | — | — | Year | T _a = +85°C |

Note 1. Definition of reprogram/erase cycle:

The reprogram/erase cycle is the number of erasing for each block. When the reprogram/erase cycle is n times (n = 1000), erasing can be performed n times for each block. For instance, when 256-byte programming is performed 16 times for different addresses in 4-Kbyte block and then the entire block is erased, the reprogram/erase cycle is counted as one. However, programming the same address for several times as one erasing is not enabled (overwriting is prohibited).

Note 2. The result obtained from the reliability test.

Table 5.37 ROM (Flash Memory for Code Storage) Characteristics (2)

Conditions: VCC = AVCC0 = VREFH = VCC_USB = 2.7 to 3.6 V, VREFH0 = 2.7 V to AVCC0
 VSS = AVSS0 = VREFL/VREFL0 = VSS_USB = 0 V
 Temperature range for the programming/erasure operation: T_a = T_{opr}

| Item | Symbol | FCLK = 4 MHz | | | 20 MHz ≤ FCLK ≤ 50 MHz | | | Unit | |
|--|--------------------|-------------------|------|-------|------------------------|------|------|------|----|
| | | Min. | Typ. | Max. | Min. | Typ. | Max. | | |
| Programming time N _{PEC} ≤ 100 times | 128 bytes | t _{P128} | — | 2.8 | 28 | — | 1 | 10 | ms |
| | 4 Kbytes | t _{P4K} | — | 63 | 140 | — | 23 | 50 | ms |
| | 16 Kbytes | t _{P16K} | — | 252 | 560 | — | 90 | 200 | ms |
| Programming time N _{PEC} > 100 times | 128 bytes | t _{P128} | — | 3.4 | 33.6 | — | 1.2 | 12 | ms |
| | 4 Kbytes | t _{P4K} | — | 75.6 | 168 | — | 27.6 | 60 | ms |
| | 16 Kbytes | t _{P16K} | — | 302.4 | 672 | — | 108 | 240 | ms |
| Erasure time N _{PEC} ≤ 100 times | 4 Kbytes | t _{E4K} | — | 50 | 120 | — | 25 | 60 | ms |
| | 16 Kbytes | t _{E16K} | — | 200 | 480 | — | 100 | 240 | ms |
| Erasure time N _{PEC} > 100 times | 4 Kbytes | t _{E4K} | — | 60 | 144 | — | 30 | 72 | ms |
| | 16 Kbytes | t _{E16K} | — | 240 | 576 | — | 120 | 288 | ms |
| Suspend delay time during programming | t _{SPD} | — | — | 400 | — | — | 120 | μs | |
| First suspend delay time during erasure (in suspend priority mode) | t _{SESD1} | — | — | 300 | — | — | 120 | μs | |
| Second suspend delay time during erasure (in suspend priority mode) | t _{SESD2} | — | — | 1.7 | — | — | 1.7 | ms | |
| Suspend delay time during erasure (in erasure priority mode) | t _{SEED} | — | — | 1.7 | — | — | 1.7 | ms | |
| FCU reset time | t _{FCUR} | 35 | — | — | 35 | — | — | μs | |

5.12 E² Flash Characteristics**Table 5.38 E² Flash Characteristics (1)**

Conditions: VCC = AVCC0 = VREFH = VCC_USB = 2.7 to 3.6V, VREFH0 = 2.7V to AVCC0
 VSS = AVSS0 = VREFL/VREFL0 = VSS_USB = 0V
 Temperature range for the programming/erasure operation: T_a = T_{opr}

| Item | Symbol | min | typ | max | Unit | Condition |
|---------------------------|-------------------|--------|-----|-----|-------|------------------------|
| Reprogram/erasure cycle*1 | N _{DPEC} | 100000 | — | — | Times | |
| Data hold time | t _{DDRP} | 30*2 | — | — | Year | T _a = +85°C |

Note 1. Definition of reprogram/erase cycle:

The reprogram/erase cycle is the number of erasing for each block. When the reprogram/erase cycle is n times (n = 100000), erasing can be performed n times for each block. For instance, when 128-byte programming is performed 16 times for different addresses in 2-Kbyte block and then the entire block is erased, the reprogram/erase cycle is counted as one. However, programming the same address for several times as one erasing is not enabled (overwriting is prohibited).

Note 2. The result obtained from the reliability test.

Table 5.39 E² Flash Characteristics (2)

Conditions: VCC = AVCC0 = VREFH = VCC_USB = 2.7 to 3.6 V, VREFH0 = 2.7 V to AVCC0
 VSS = AVSS0 = VREFL/VREFL0 = VSS_USB = 0 V
 Temperature range for the programming/erasure operation: T_a = T_{opr}

| Item | Symbol | FCLK = 4 MHz | | | 20 MHz ≤ FCLK ≤ 50 MHz | | | Unit | |
|--|----------|---------------------|------|------|------------------------|------|------|------|----|
| | | Min. | Typ. | Max. | Min. | Typ. | Max. | | |
| Programming time N _{P_{EC}} ≤ 100 times | 2 bytes | t _{DP2} | — | 0.7 | 6 | — | 0.25 | 2 | ms |
| Programming time N _{P_{EC}} > 100 times | 2 bytes | t _{DP2} | — | 0.7 | 6 | — | 0.25 | 2 | ms |
| Erasure time N _{P_{EC}} ≤ 100 times | 32 bytes | t _{DE32} | — | 4 | 40 | — | 2 | 20 | ms |
| Erasure time N _{P_{EC}} > 100 times | 32 bytes | t _{DE32} | — | 7 | 40 | — | 4 | 20 | ms |
| Blank check time | 2 bytes | t _{DBC2} | — | — | 100 | — | — | 30 | μs |
| Suspend delay time during programming | | t _{DSPD} | — | — | 250 | — | — | 120 | μs |
| First suspend delay time during erasure (in suspend priority mode) | | t _{DSESD1} | — | — | 250 | — | — | 120 | μs |
| Second suspend delay time during erasure (in suspend priority mode) | | t _{DSESD2} | — | — | 500 | — | — | 300 | μs |
| Suspend delay time during erasure (in erasure priority mode) | | t _{DSEED} | — | — | 500 | — | — | 300 | μs |

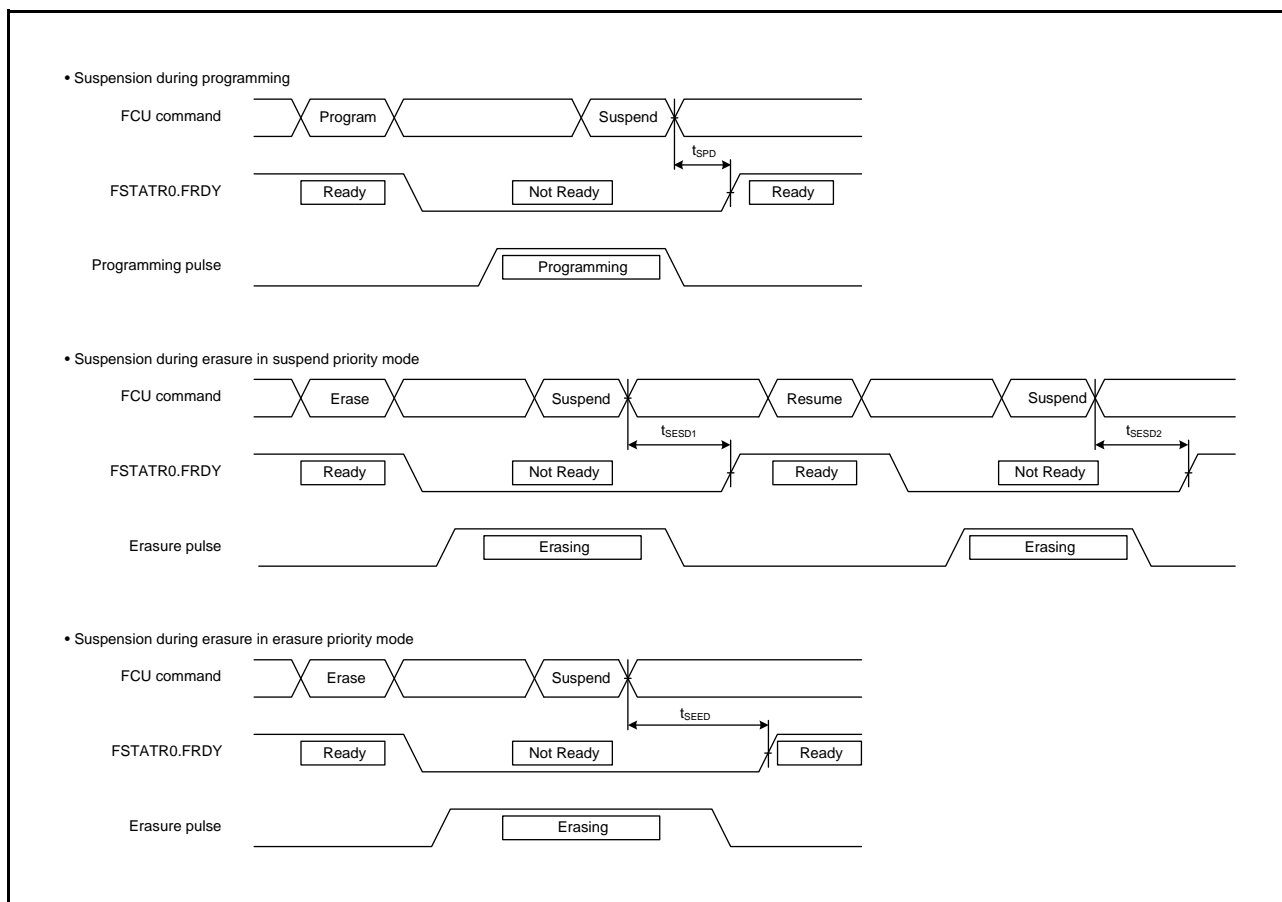


Figure 5.69 Flash Memory Program/Erase Suspend Timing

5.13 Boundary Scan

Table 5.40 Boundary Scan

Conditions: VCC = AVCC0 = VREFH = VCC_USB = 2.7 to 3.6V, VREFH0 = 2.7V to AVCC0
 VSS = AVSS0 = VREFL/VREFLO = VSS_USB = 0V
 T_a = T_{opr}

| Item | Symbol | Min. | Typ. | Max. | Unit | Test Conditions |
|----------------------------|---------------------|------|------|------|---------------------|-----------------|
| TCK clock cycle time | t _{TCKcyc} | 100 | — | — | ns | Figure 5.70 |
| TCK clock high pulse width | t _{TCKH} | 45 | — | — | ns | |
| TCK clock low pulse width | t _{TCKL} | 45 | — | — | ns | |
| TCK clock rise time | t _{TCKr} | — | — | 5 | ns | |
| TCK clock fall time | t _{TCKf} | — | — | 5 | ns | |
| TRST# pulse width | t _{TRSTW} | 20 | — | — | t _{TCKcyc} | Figure 5.71 |
| TMS setup time | t _{TMSS} | 20 | — | — | ns | Figure 5.72 |
| TMS hold time | t _{TMSH} | 20 | — | — | ns | |
| TDI setup time | t _{TDIS} | 20 | — | — | ns | |
| TDI hold time | t _{TDIH} | 20 | — | — | ns | |
| TDO data delay time | t _{TDOD} | — | — | 40 | ns | |

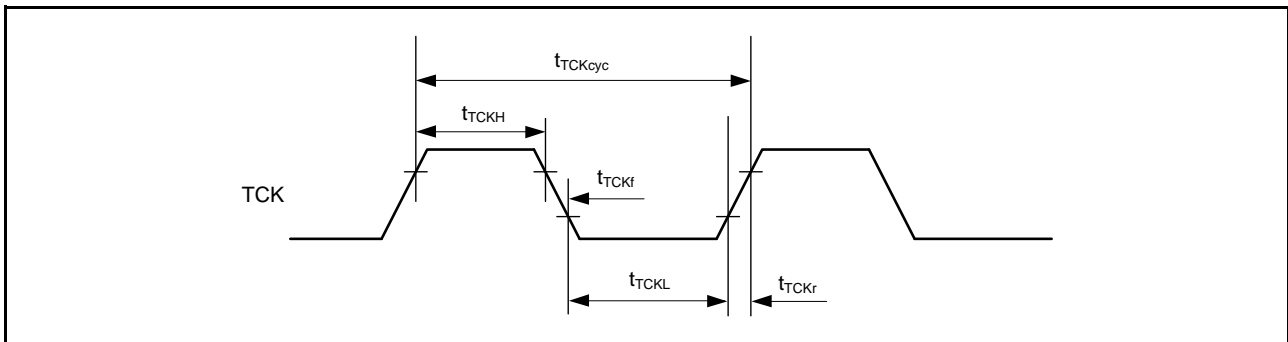


Figure 5.70 Boundary Scan TCK Timing

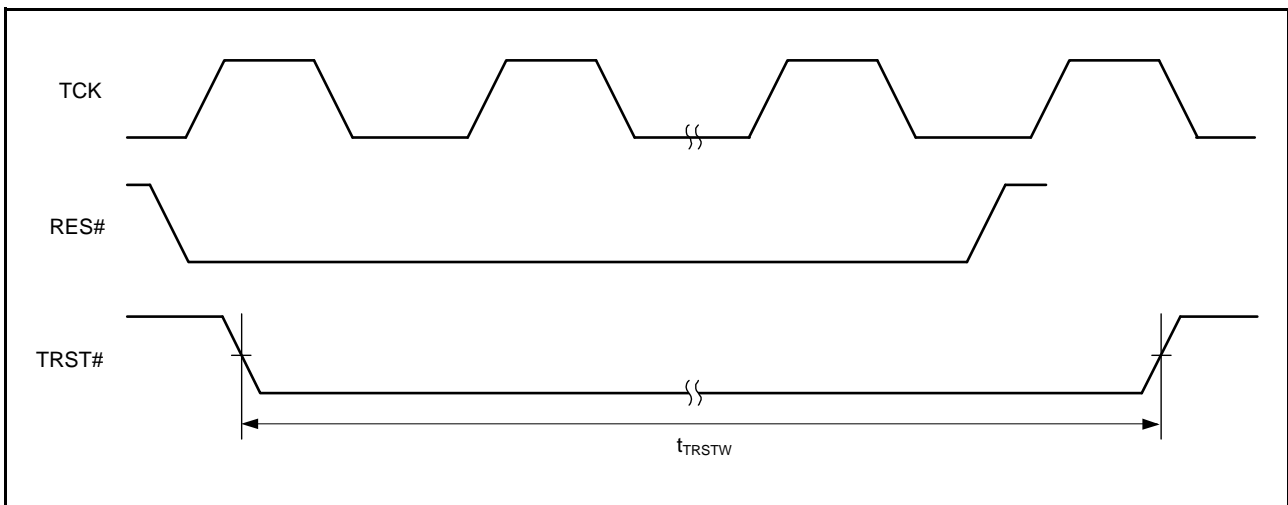


Figure 5.71 Boundary Scan TRST# Timing

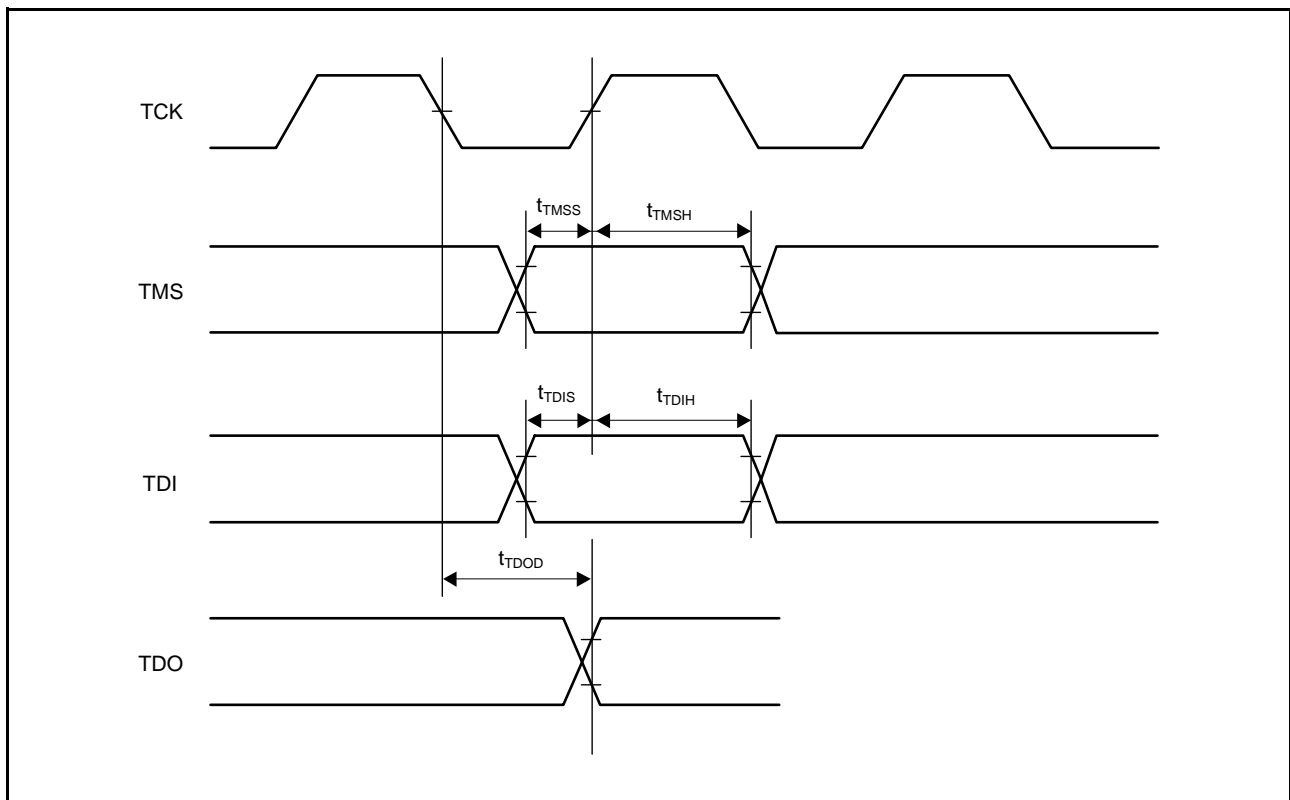


Figure 5.72 Boundary Scan Input/Output Timing

Appendix 1. Package Dimensions

Information on the latest version of the package dimensions or mountings has been displayed in “Packages” on Renesas Electronics Corporation website.

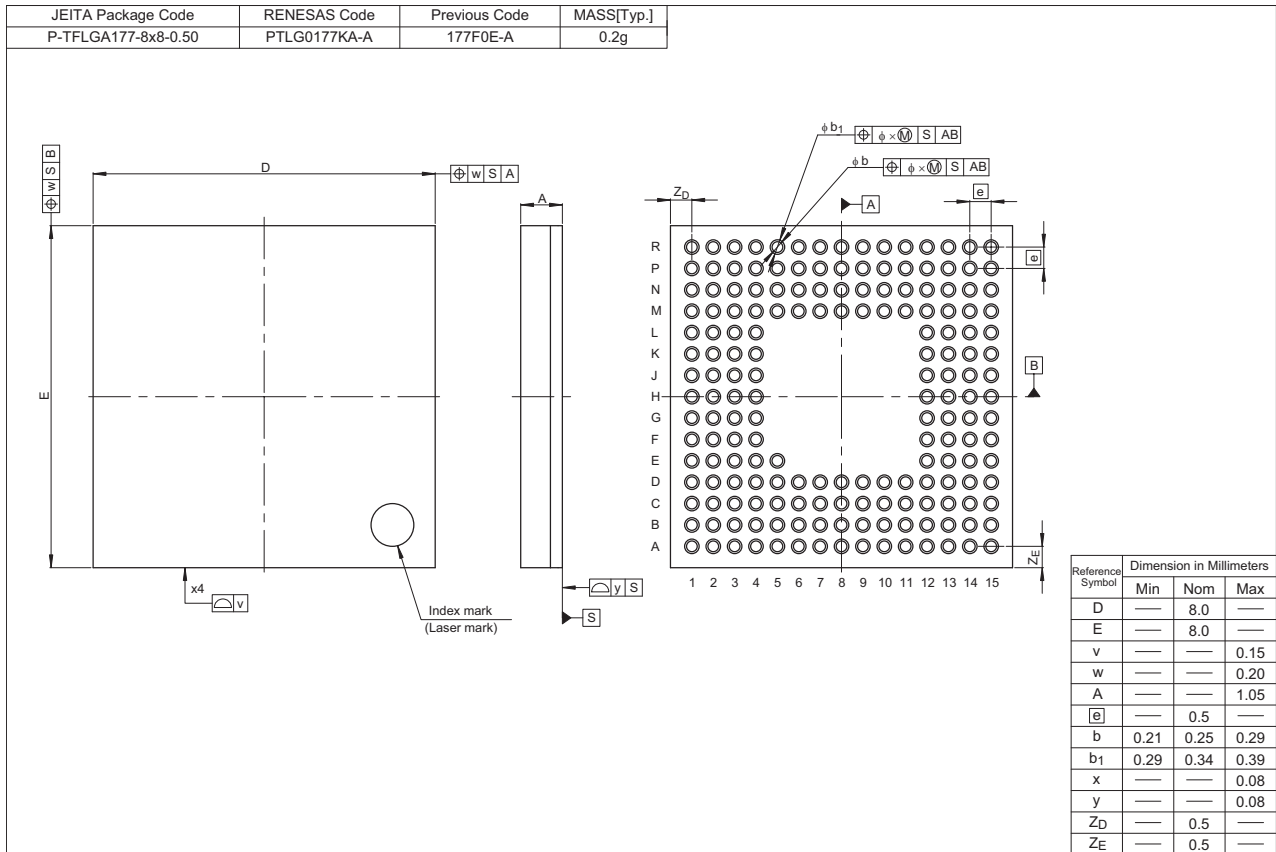


Figure A 177-pin TFLGA (PTLG0177KA-A)

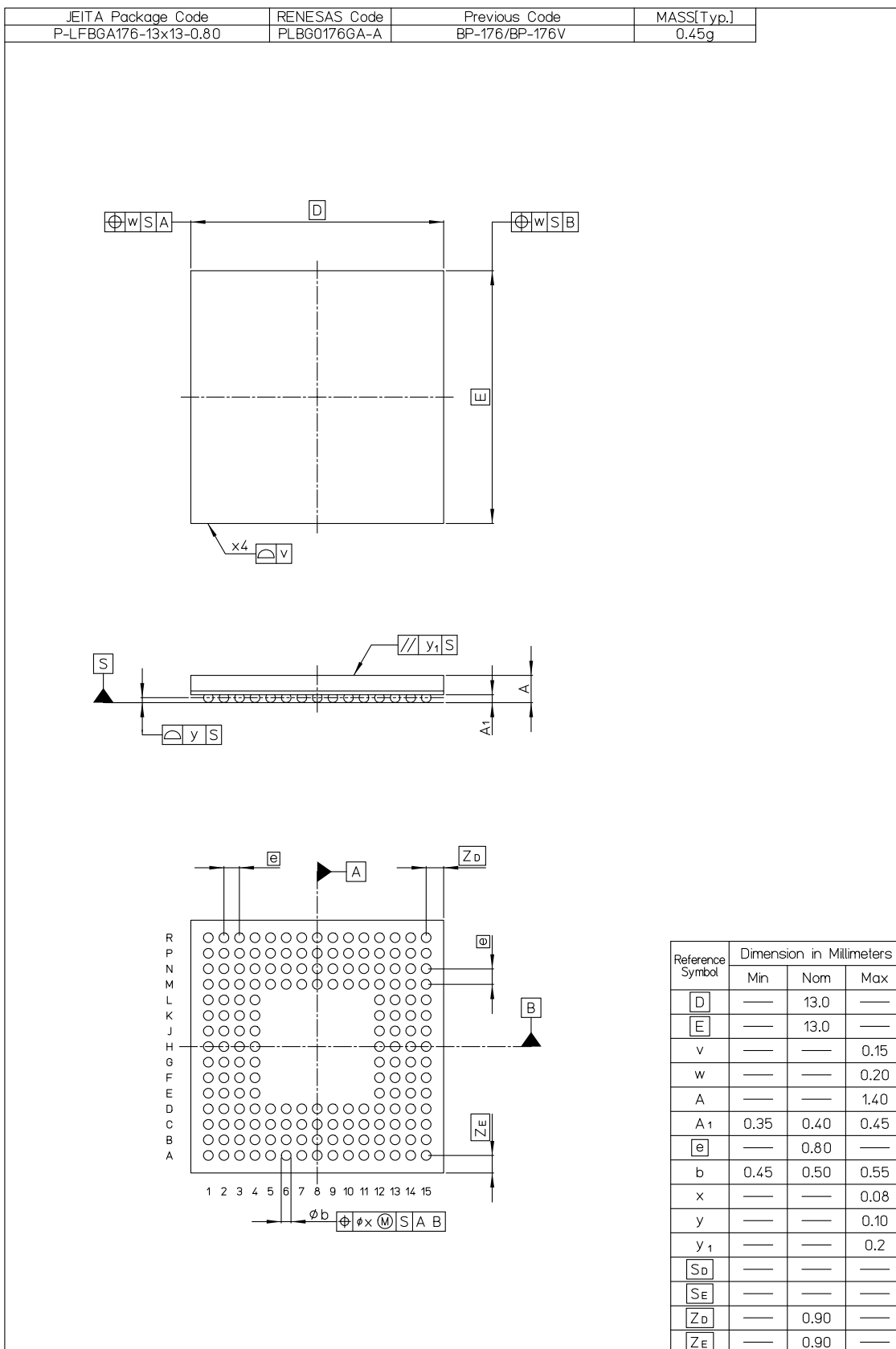


Figure B 176-pin LFBGA (PLBG0176GA-A)

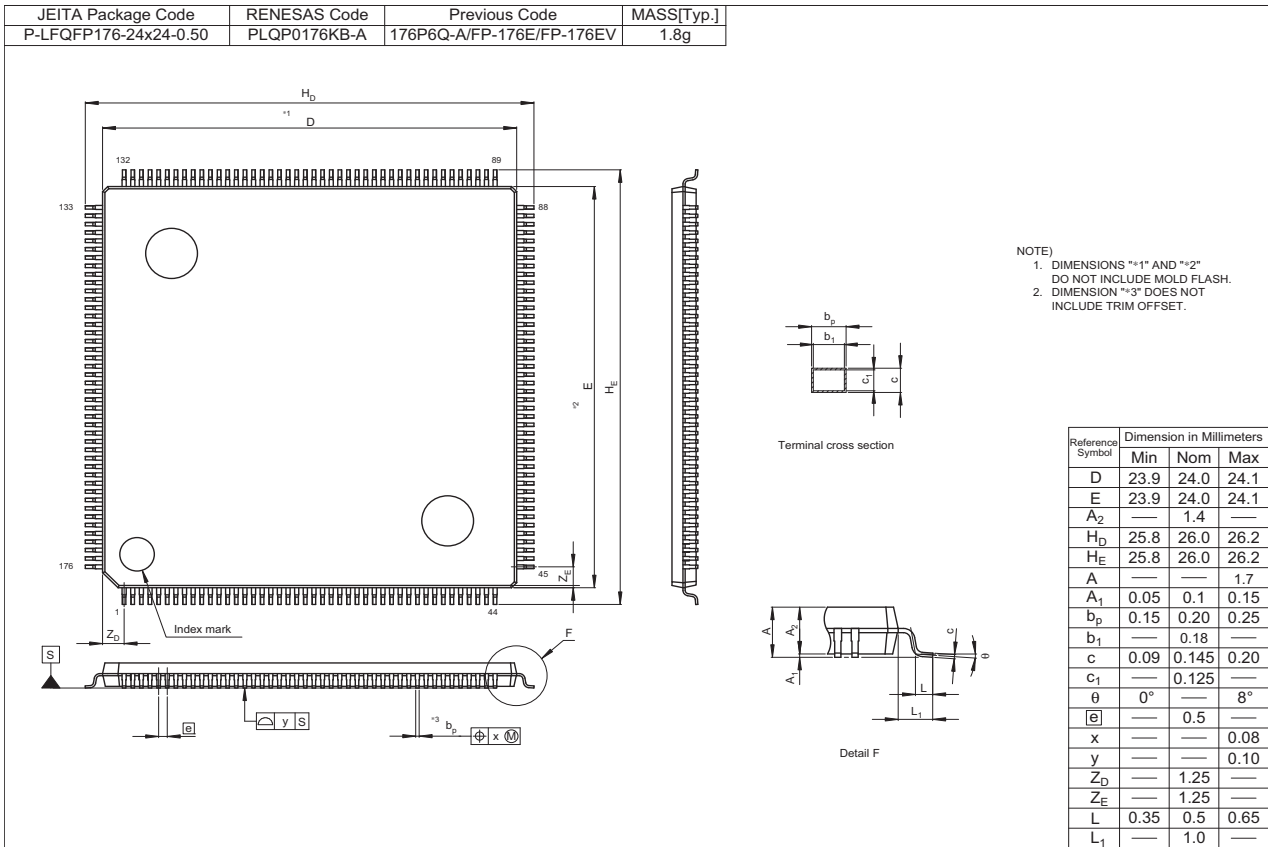


Figure C 176-pin LQFP (PLQP0176KB-A)

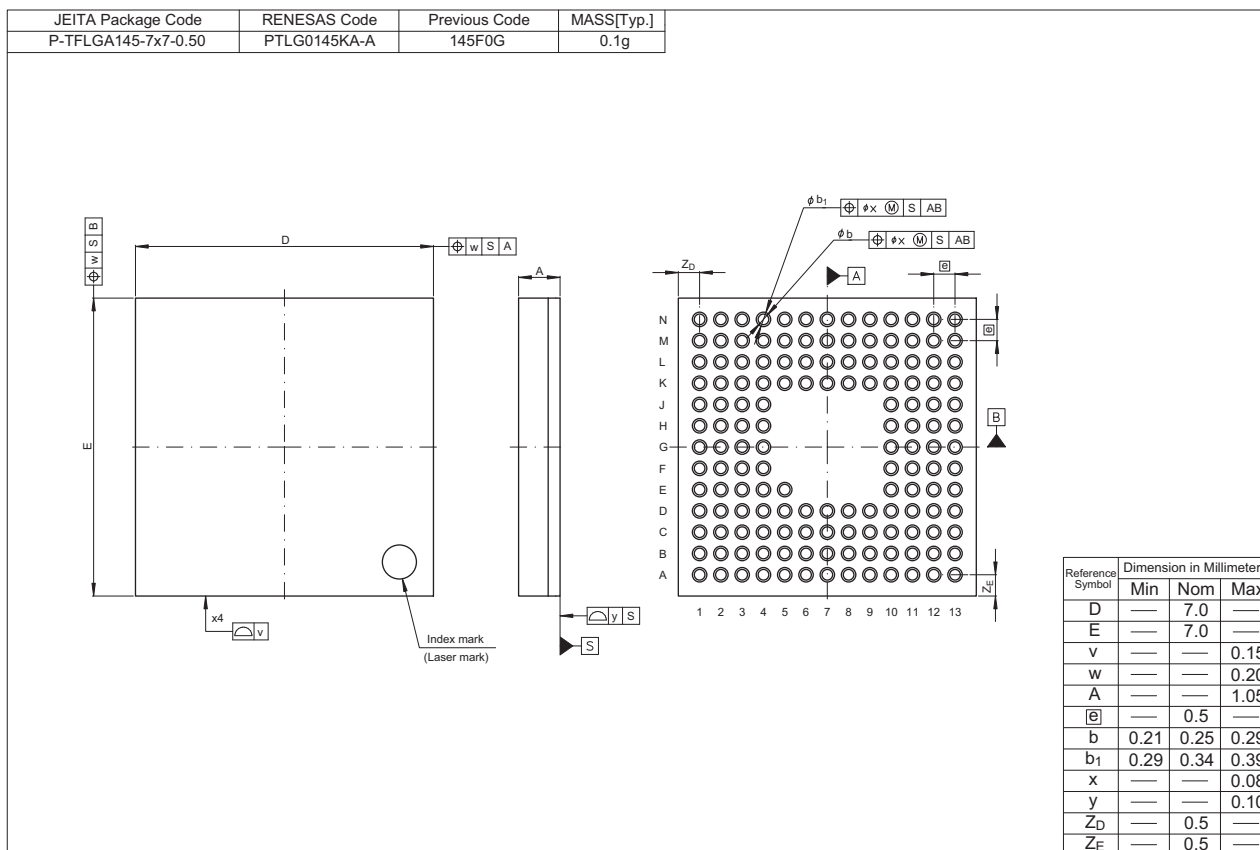


Figure D 145-pin TFLGA (PTLG0145KA-A)

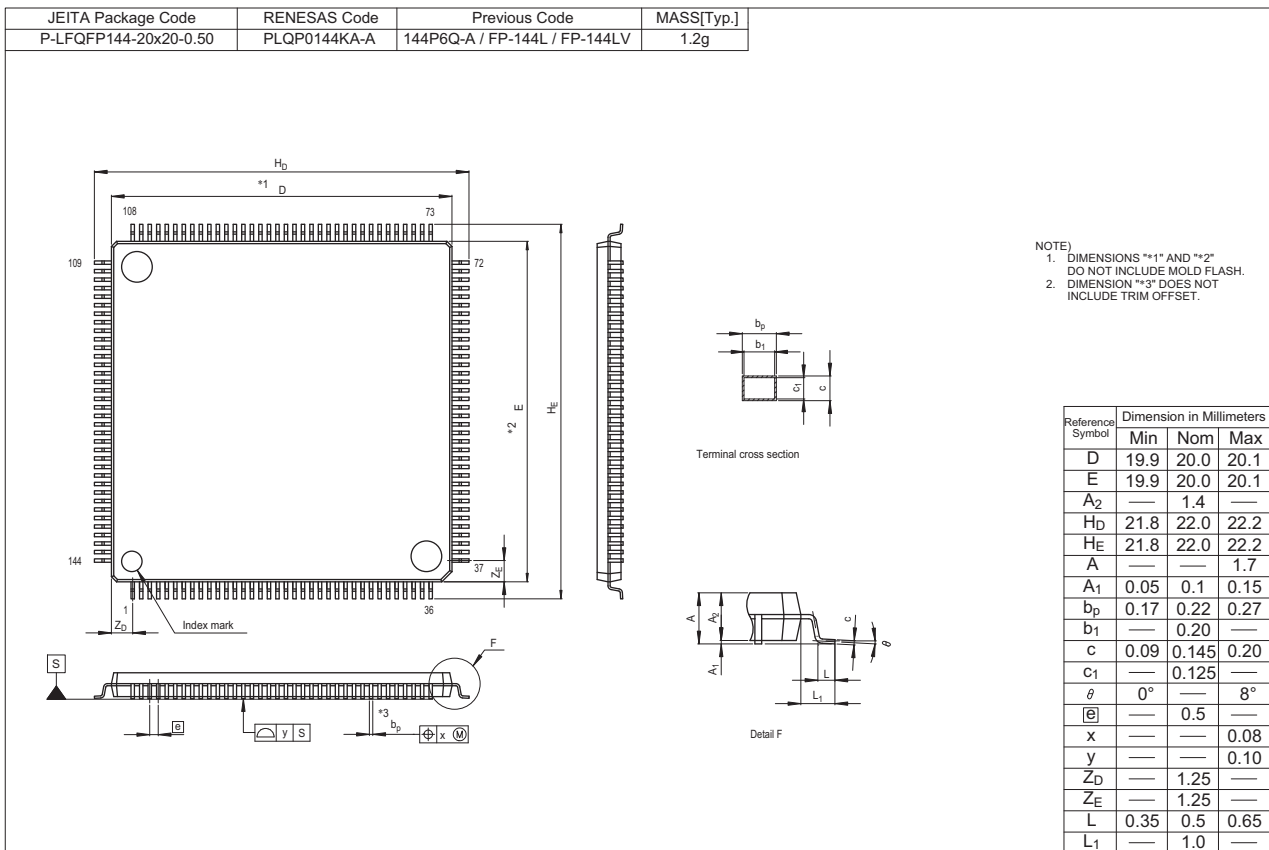


Figure E 144-pin LQFP (PLQP0144KA-A)

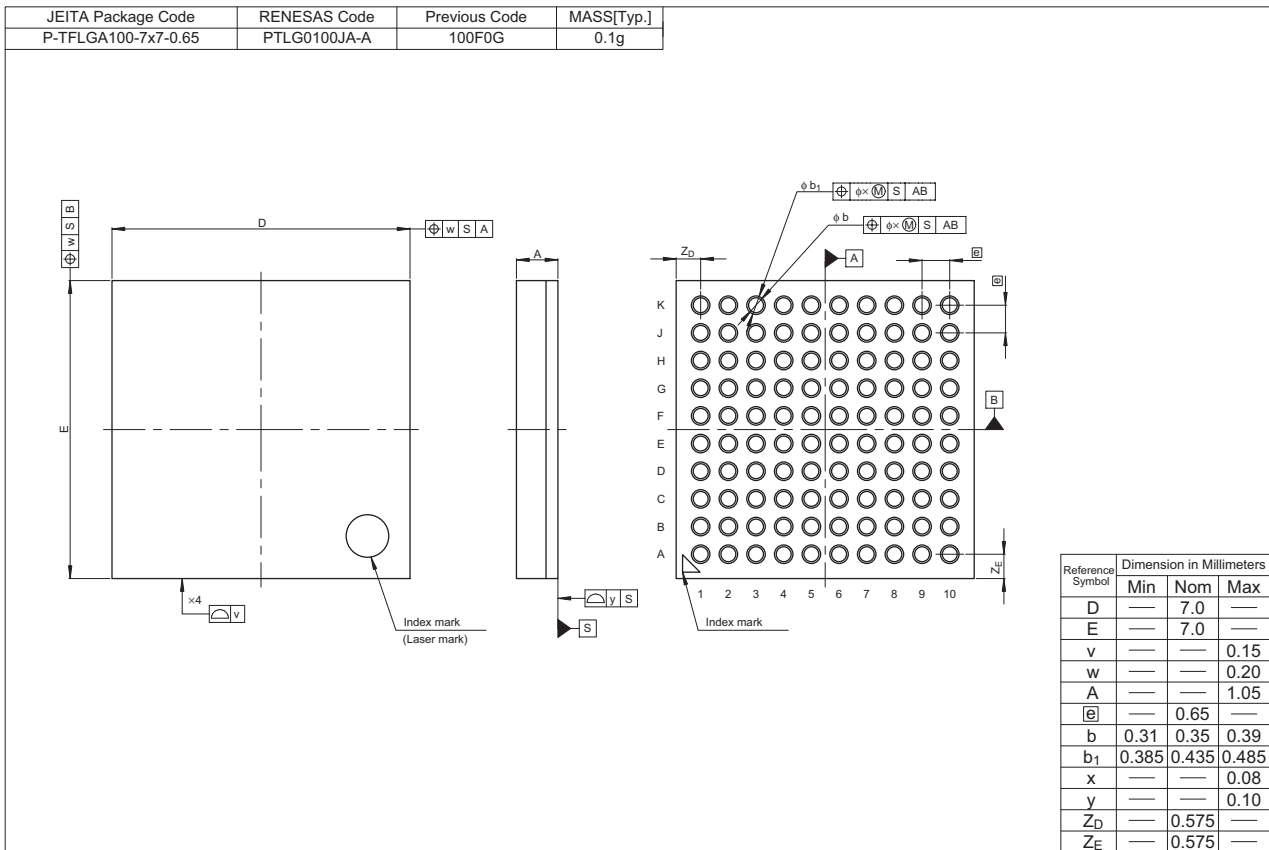


Figure F 100-pin TFLGA (PTLG0100JA-A)

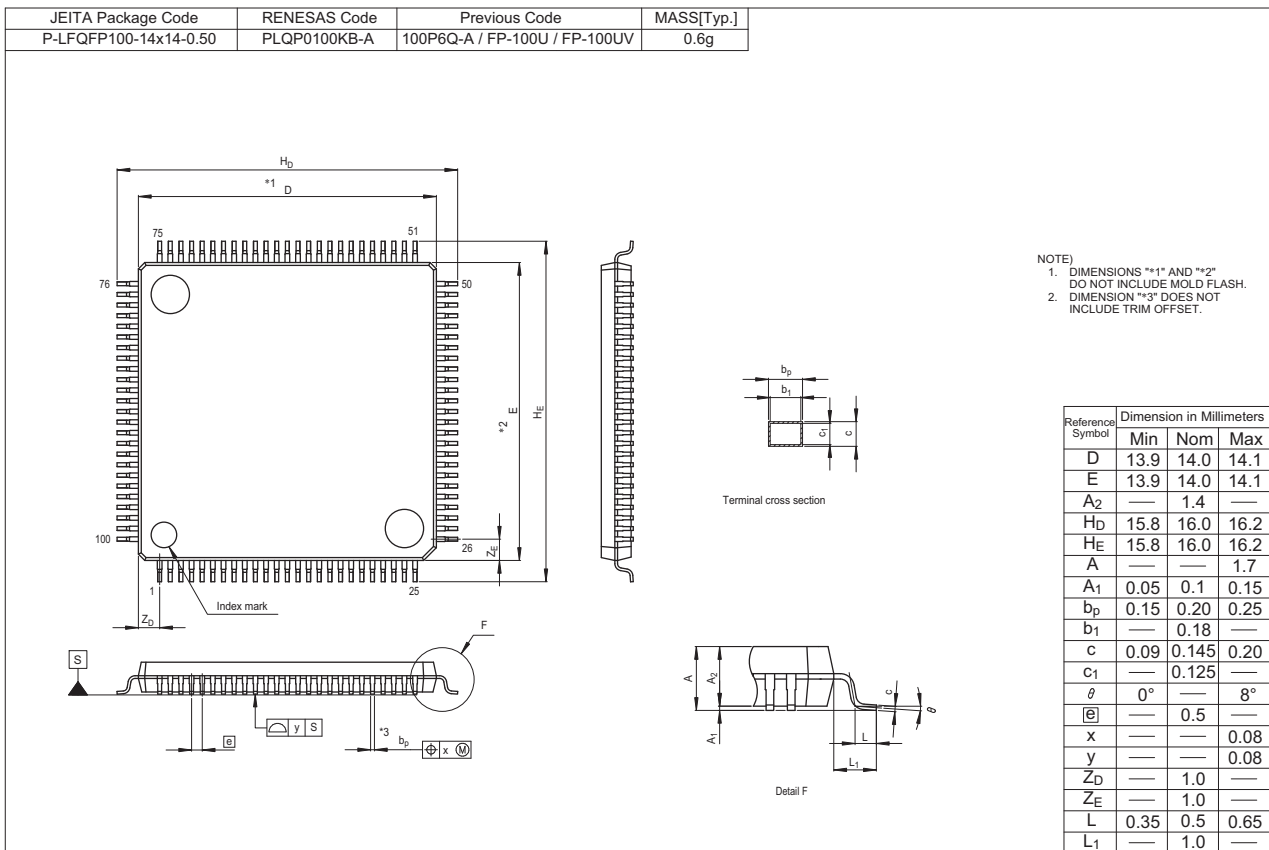


Figure G 100-pin LQFP (PLQP0100KB-A)

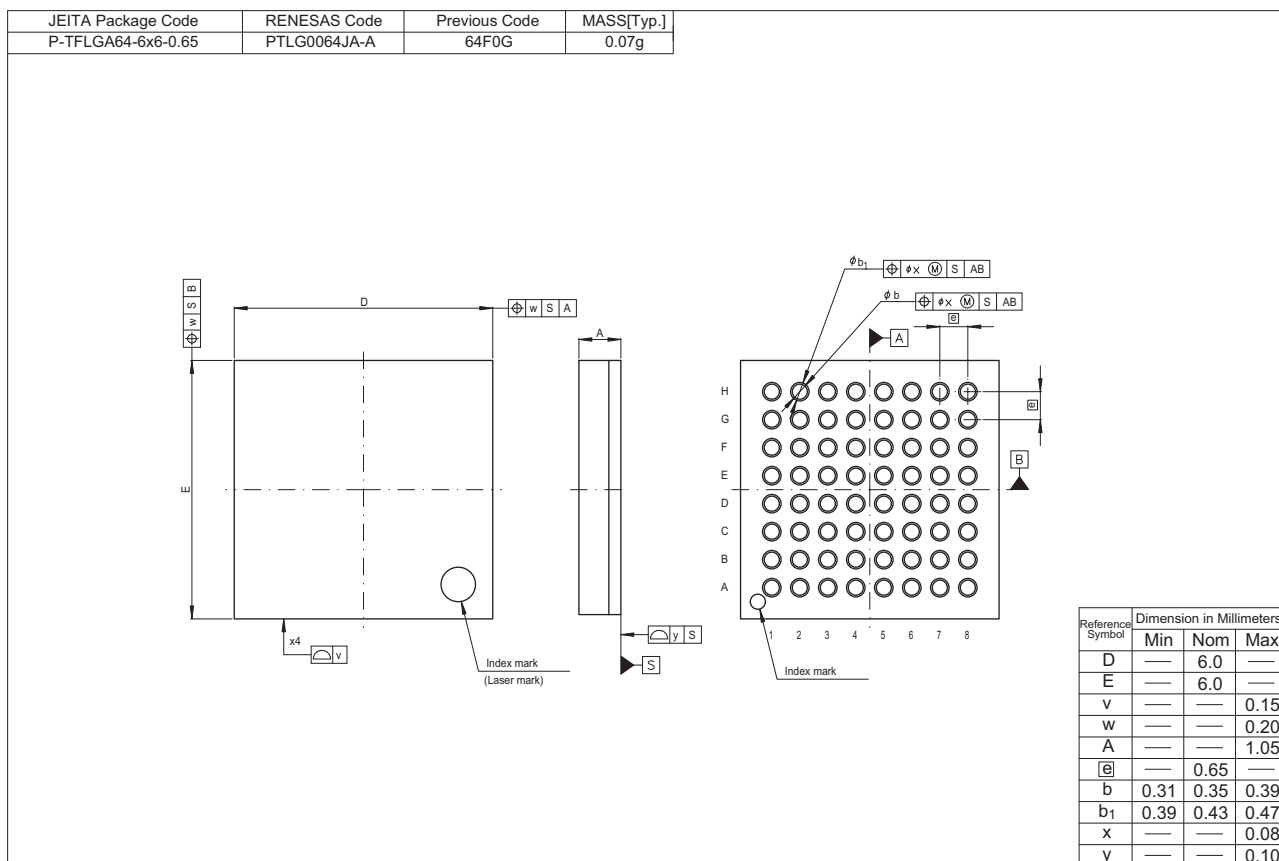


Figure H 64-pin TFLGA (PTLG0064JA-A)

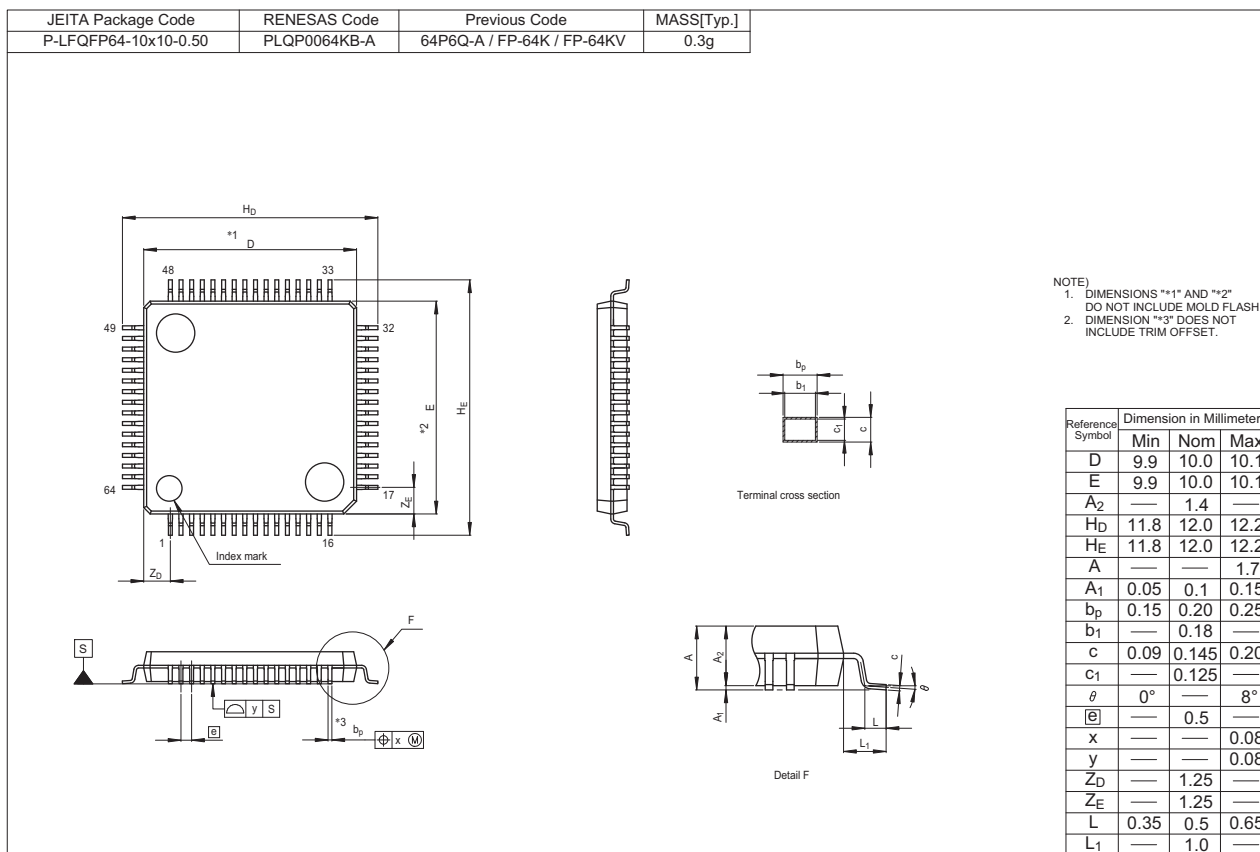


Figure I 64-pin LQFP (PLQP0064KB-A)

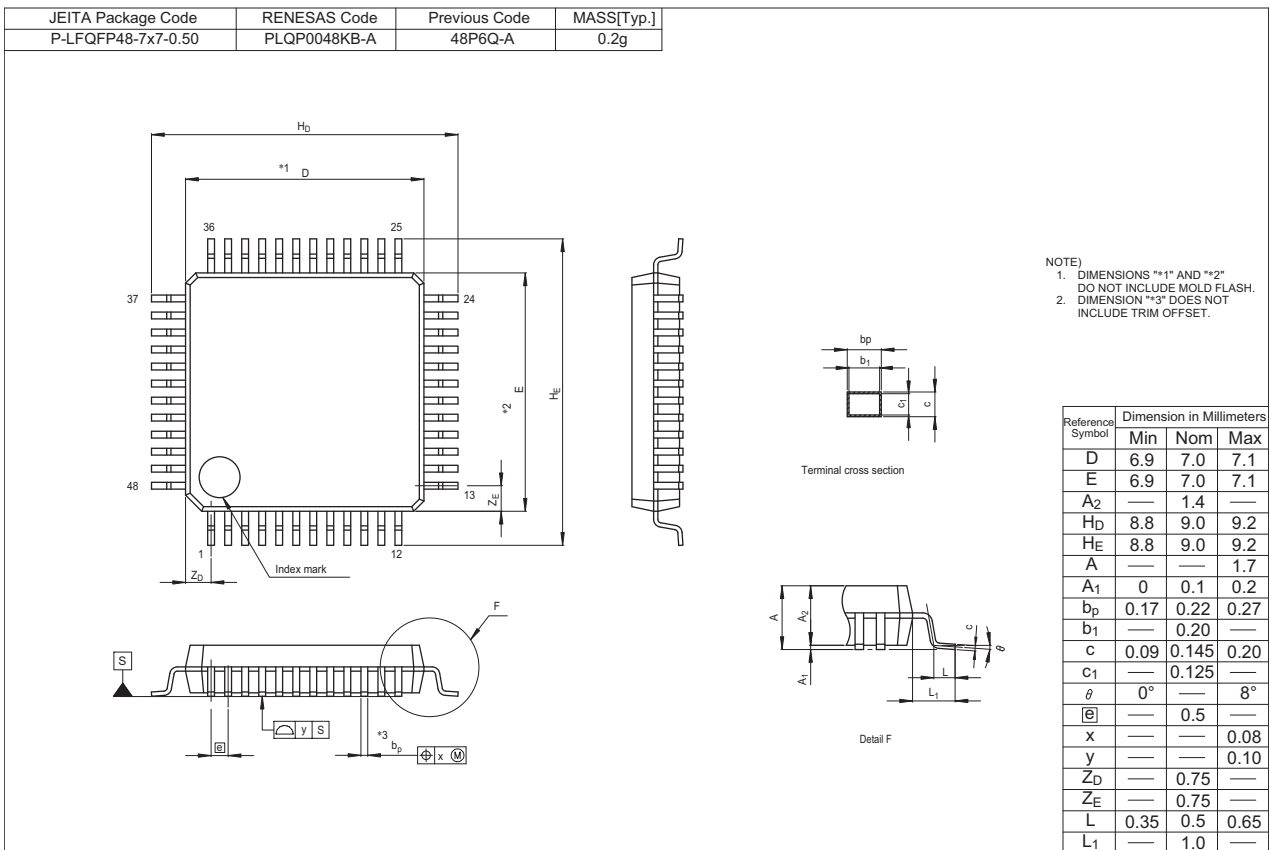


Figure J 48-pin LQFP (PLQP0048KB-A)

| | |
|------------------|------------------------------------|
| REVISION HISTORY | RX63N Group, RX631 Group Datasheet |
|------------------|------------------------------------|

| Rev. | Date | Description | |
|------|--------------|--------------------------------|---|
| | | Page | Summary |
| 0.50 | May 13. 2011 | — | First Edition issued |
| 0.90 | Dec 27. 2011 | All | |
| | | — | Package added (177-pin TFLGA, 176-pin LFBGA, 145-pin TFLGA), module name changed |
| | | — | Interrupt Controller (ICUb) module name changed |
| | | 1. Overview | |
| | | 2 to 6 | Table 1.1 Outline of Specifications, Reset, Realtime clock, Temperature sensor, Power supply voltage, changed |
| | | 8 to 10 | Table 1.3 List of Products, changed |
| | | 10 | Figure 1.1 How to Read the Product Part No., changed |
| | | 12 to 17 | Table 1.4 Pin Functions, BSCANP pin added |
| | | 18 | Figure 1.3 Pin Assignment (176-Pin TFLGA), added |
| | | 19 | Figure 1.4 Pin Assignment (176-Pin LFBGA), added |
| | | 20 | Figure 1.5 Pin Assignment (176-Pin LQFP), pin 18 changed |
| | | 21 | Figure 1.6 Pin Assignment (144-Pin TFLGA), added |
| | | 22 | Figure 1.7 Pin Assignment (144-Pin LQFP), pin 16 changed |
| | | 23 | Figure 1.8 Pin Assignment (100-Pin LQFP), pin 7 changed |
| | | 24 to 28 | Table 1.5 List of Pins and Pin Functions (177-pin TFLGA, 176-pin LFBGA), added |
| | | 34 to 38 | Table 1.7 List of Pins and Pin Functions (145-Pin TFLGA), added |
| | | 4. I/O Registers | |
| | | 56 to 99 | Table 5.1 List of I/O Registers, changed |
| | | Appendix 2. Package Dimensions | |
| | | 100 | Figure A. 177-pin TFLGA (PTLG0177KA-A), added |
| | | 101 | Figure B. 176-pin LFBGA (PLBG0176GA-A), added |
| | | 103 | Figure D. 145-pin TFLGA (PTLG0145KA-A), added |
| | | 105 | Figure F. 100-pin TFLGA (PTLG0100KA-A), added |
| 1.00 | Jun 06. 2012 | 1. Overview | |
| | | 2 to 6 | Table 1.1 Outline of Specifications: CPU, ROM, RAM, E2 DataFlash, clock generation circuit, temperature sensor, power supply voltage, changed. Low power consumption, deleted |
| | | 8 to 10 | Table 1.3 List of Products, changed |
| | | 11 | Figure 1.2 Block Diagram, changed |
| | | 12 | Table 1.4 Pin Functions, description of VCC, changed |
| | | 24 to 28 | Table 1.5 List of Pin and Pin Functions (177-Pin TFLGA, 176-Pin LFBGA): SDRAMC, added to table header; BCLK in pin number line M8, moved to Power Supply Clock System Control column |
| | | 29 to 33 | Table 1.6 List of Pin and Pin Functions (176-Pin LQFP): SDRAMC, added to table header; BCLK in pin number line 68, moved to Power Supply Clock System Control column |
| | | 34 to 38 | Table 1.7 List of Pin and Pin Functions (145-Pin TFLGA): SDRAMC, added to table header; MOSIB, added to pin number line D13; T_ERXD1 in pin number line H12, changed to ET_ERXD1; PO8, added to pin number line J4; BCLK in pin number line K6, moved to Power Supply Clock System Control column |
| | | 39 to 43 | Table 1.8 List of Pins and Pin Functions (144-Pin LQFP): SDRAMC, added to table header; PO8, added to pin number line 29; BCLK in pin number line 53, moved to Power Supply Clock System Control column; T_ERXD1 in pin number 87, changed to ET_ERXD1; MOSIB, added to pin number line 102 |
| | | 44 to 47 | Table 1.9 List of Pins and Pin Functions (100-Pin LQFP): BCLK in pin number line 41, moved to Power Supply Clock System Control column |
| | | 4. I/O Registers | |
| | | 57, 58 | Table 4.1, MPU registers, added |
| | | 5. Electrical Characteristics | |
| | | 105 to 163 | Added |

| Rev. | Date | Description | |
|------------------|---|-------------------------------|--|
| | | Page | Summary |
| 1.60 | Mar 13. 2013 | Feature | |
| | | 1 | Changed |
| | | 1. Overview | |
| | | 2 to 7 | Table 1.1 Outline of Specifications: changed, note added |
| | | 8 | Table 1.2 Comparison of Functions for Different Packages in the RX63N/RX631 Group, changed |
| | | 9 to 15 | Table 1.3 List of Products, changed |
| | | 16 | Figure 1.1 How to Read the Product Part No., changed |
| | | 17 | Figure 1.2 Block Diagram, changed |
| | | 24 to 32 | Figure 1.3 to Figure 1.11 Pin Assignment: note, added |
| | | 53 to 57 | Table 1.9 List of Pins and Pin Functions (100-Pin TFLGA), added |
| | | 62 to 64 | Table 1.11 List of Pins and Pin Functions (64-Pin LQFP), added |
| | | 65, 66 | Table 1.12 List of Pins and Pin Functions (48-Pin LQFP), added |
| | | 3. Address Space | |
| | | 71 | Figure 3.1 Memory Map in Each Operating Mode, changed |
| | | 4. I/O Registers | |
| | | 75 to 120 | Table 4.1 List of I/O Registers (Address Order), changed |
| | | 5. Electrical Characteristics | |
| | | All | Characteristics and timing conditions in the tables, changed |
| | | 124, 125 | Table 5.4 DC Characteristics (3), changed |
| | | 126 | Table 5.5 DC Characteristics (4), changed |
| | | 127 | 5.3 AC Characteristics, changed |
| | | 130, 131 | Table 5.11, Clock Timing (Except for Sub-Clock Related): Condition and the table, changed, note, added |
| | | 132 | Table 5.12 Clock Timing (Sub-Clock Related): Condition and the table, changed, note, added |
| | | 176 | Table 5.33 Battery Backup Function Characteristics: Condition, changed |
| | | Appendix 1.Package Dimensions | |
| | | 189 | Figure H 64-pin LQFP (PLQP0064KB-A), added |
| | | 190 | Figure I 48-pin LQFP (PLQP0048KB-A), added |
| | | 1.70 | Oct 08. 2013 |
| 1 | changed | | |
| 1. Overview | | | |
| 2 to 7 | Table 1.1 Outline of Specifications, General I/O ports, Packages, changed, Parallel data capture unit (PDC), added. | | |
| 8 | Table 1.2 Comparison of Functions for Different Packages in the RX63N/RX631 Group, 64-pin LQFP, changed, 64-pin TFLGA, Parallel data capture unit (PDC), added. | | |
| 9 to 16 | Table 1.3 List of Products, changed. | | |
| 17 | Figure 1.1 How to Read the Product Part No., changed | | |
| 18 | Figure 1.2 Block Diagram, changed | | |
| 19 to 24 | Table 1.4 Pin Functions,changed, Parallel data capture unit (PDC), added | | |
| 32 | Figure 1.10 Pin Assignment (64-Pin TFLGA), added | | |
| 35 to 40 | Table 1.5 List of Pin and Pin Functions (177-Pin TFLGA, 176-Pin LFBGA), changed | | |
| 41 to 45 | Table 1.6 List of Pin and Pin Functions (176-Pin LQFP), changed | | |
| 46 to 50 | Table 1.7 List of Pins and Pin Functions (145-Pin TFLGA), changed | | |
| 51 to 55 | Table 1.8 List of Pins and Pin Functions (144-Pin LQFP), changed | | |
| 65 to 66 | Table 1.11 List of Pins and Pin Functions (64-Pin TFLGA), added | | |
| 3. Address Space | | | |
| 76 | Figure 3.1 Memory Map in Each Operating Mode, changed | | |
| 4. I/O Registers | | | |
| 79 | (4) Restrictions in Relation to RMPA and String-Manipulation Instructions, added | | |

| Rev. | Date | Description | |
|------|--------------|--------------------------------|---|
| | | Page | Summary |
| 1.70 | Oct 08. 2013 | 80 to 127 | Table 4.1 List of I/O Registers (Address Order), changed |
| | | 5. Electrical Characteristics | |
| | | 131, 132 | Table 5.4 DC Characteristics (3), changed, Note. 9, Note. 10, added |
| | | 133 | Table 5.6 Permissible Output Currents, changed |
| | | 139 | Table 5.12 Clock Timing (Sub-Clock Related), Note 3, added |
| | | 167 | Table 5.25 Timing of On-Chip Peripheral Modules (8), added |
| | | 175 | Figure 5.58 PDC Timing, added |
| | | 175 | Figure 5.59 PDC Input Clock Characteristic, added |
| | | 176 | Figure 5.60 PDC Output Clock Characteristic, added |
| | | 178 | Table 5.27 10-Bit A/D Conversion Characteristics, changed |
| | | 179 | Table 5.28 12-Bit A/D Conversion Characteristics, changed |
| | | 185 | Table 5.35 ROM (Flash Memory for Code Storage) Characteristics (1), added |
| | | 185 | Table 5.36 ROM (Flash Memory for Code Storage) Characteristics (2), changed |
| | | 186 | Table 5.37 E2 Flash Characteristics (1), added |
| | | 186 | Table 5.38 E2 Flash Characteristics (2), changed |
| | | Appendix 1. Package Dimensions | |
| | | 197 | Figure H 64-pin TFLGA (PTLG0064JA-A), added |

Classifications

- Items with Technical Update document number: Changes according to the corresponding issued Technical Update

- Items without Technical Update document number: Minor changes that do not require Technical Update to be issued

| Rev. | Date | Description | | Classification |
|------|--|-------------------------------|---|----------------|
| | | Page | Summary | |
| 1.80 | May 13. 2014 | Features | | |
| | | 1 | Operating temp. range chaged, Unique ID added | |
| | | 1. Overview | | |
| | | 2 to 7 | Table 1.1 Outline of Specifications: Operating temperature changed, Unique ID and Note 2, added | |
| | | 8 | Table 1.2 Comparison of Functions for Different Packages: Unique ID, added | |
| | | 9 to 16 | Table 1.3 List of Products, changed and Note 2, added | TN-RX*-A092A/J |
| | | 17 | Figure 1.1 How to Read the Product Part Number: Operating temperature range, changed | |
| | | 19, 23 | Table 1.4 Pin Functions: VBATT and USB power pins, changed | |
| | | 3. Address Space | | |
| | | 76 | Figure 3.1 Memory Map in Each Operating Mode, changed | TN-RX*-A081A/E |
| | | 77 | Figure 3.2 Correspondence between External Address Spaces and CS Areas (In On-Chip ROM Disabled Extended Mode), changed | TN-RX*-A081A/E |
| | | 5. Electrical Characteristics | | |
| | | 130 | Table 5.1 Absolute Maximum Ratings: Operating temperature, changed | |
| | | 131 | Table 5.2 DC Characteristics (1): Note 1, chaged | |
| | | 133 to 134 | Table 5.4 DC Characteristics (3) (for D and G Versions (-40 ≤ Ta ≤ +85°C)): Title | |
| | | 135 to 136 | Table 5.5 DC Characteristics (4) (for G Version (-85 < Ta ≤ +105°C)), added | |
| | | 1921 | Table 5.12 Clock Timing (Except for Sub-Clock Related): LOCO changed to LOCO and IWDTCLKB | TN-RX*-A097A/J |
| 144 | Figure 5.6 LOCO, IWDTCLK Clock Oscillation Start Timing, added | TN-RX*-A097A/J | | |
| 189 | Figure 5.68 Battery Backup Function Characteristics changed | | | |

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General Precautions in the Handling of MPU/MCU Products

The following usage notes are applicable to all MPU/MCU products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Handling of Unused Pins

Handle unused pins in accordance with the directions given under Handling of Unused Pins in the manual.

- The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible. Unused pins should be handled as described under Handling of Unused Pins in the manual.

2. Processing at Power-on

The state of the product is undefined at the moment when power is supplied.

- The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the moment when power is supplied.
In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the moment when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the moment when power is supplied until the power reaches the level at which resetting has been specified.

3. Prohibition of Access to Reserved Addresses

Access to reserved addresses is prohibited.

- The reserved addresses are provided for the possible future expansion of functions. Do not access these addresses; the correct operation of LSI is not guaranteed if they are accessed.

4. Clock Signals

After applying a reset, only release the reset line after the operating clock signal has become stable. When switching the clock signal during program execution, wait until the target clock signal has stabilized.

- When the clock signal is generated with an external resonator (or from an external oscillator) during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Moreover, when switching to a clock signal produced with an external resonator (or by an external oscillator) while program execution is in progress, wait until the target clock signal is stable.

5. Differences between Products

Before changing from one product to another, i.e. to a product with a different part number, confirm that the change will not lead to problems.

- The characteristics of an MPU or MCU in the same group but having a different part number may differ in terms of the internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

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