80 MSPS, Dual-Channel WCDMA Receive Signal Processor (RSP)

AD6634

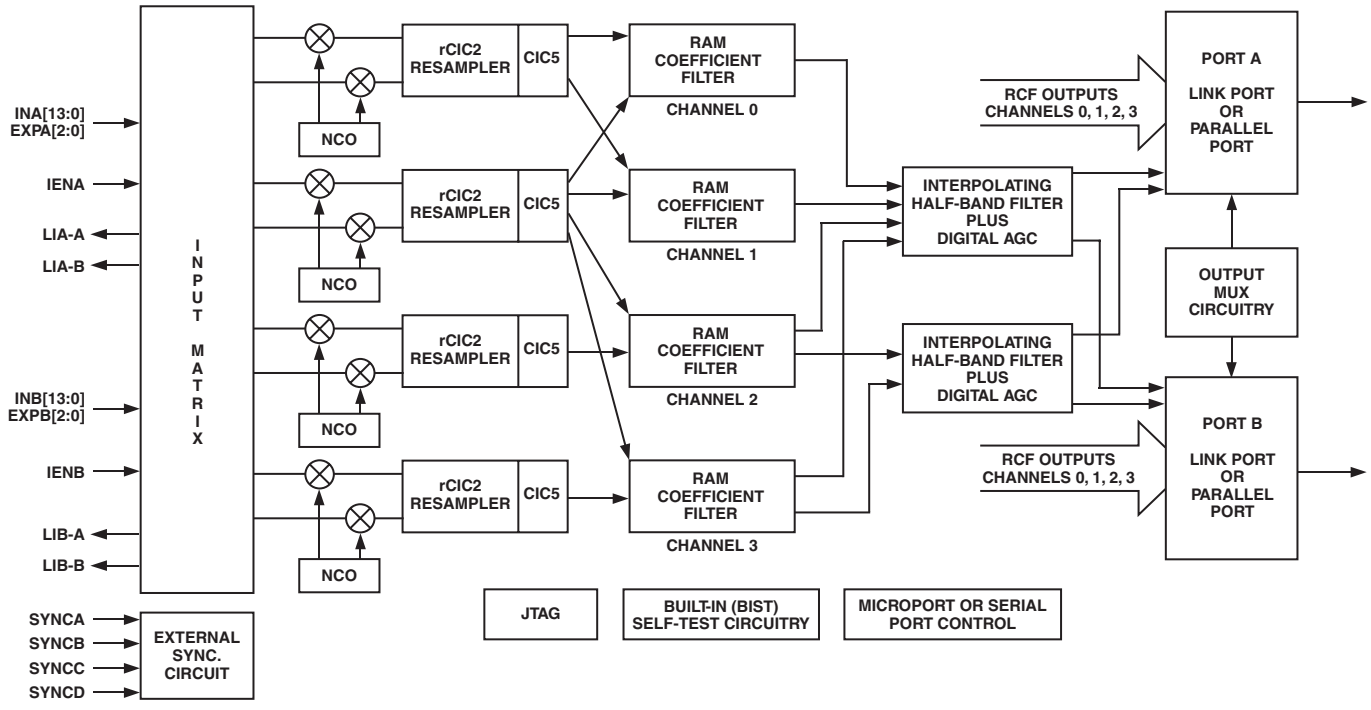
FEATURES

80 MSPS Wideband Inputs (14 Linear Bits Plus Three RSSI)
Processes Two WCDMA Channels (UMTS or CDMA2000 1×) or Four GSM/EDGE, IS136 Channels
Four Independent Digital Receivers in a Single Package
Dual 16-Bit Parallel Output Ports
Dual 8-Bit Link Ports
Programmable Digital AGC Loops with 96 dB Range
Digital Resampling for Noninteger Decimation Rates
Programmable Decimating FIR Filters
Interpolating Half-Band Filters
Programmable Attenuator Control for Clip Prevention and External Gain Ranging via Level Indicator
Flexible Control for Multicarrier and Phased Array
3.3 V I/O, 2.5 V CMOS Core
User Configurable Built-In Self-Test (BIST) Capability
JTAG Boundary Scan

APPLICATIONS

Multicarrier, Multimode Digital Receivers
GSM, IS136, EDGE, PHS, IS95, UMTS, CDMA2000
Micro and Pico Cell Systems, Software Radios
Wireless Local Loop
Smart Antenna Systems
In Building Wireless Telephony

FUNCTIONAL BLOCK DIAGRAM



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One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 781/329-4700 www.analog.com
Fax: 781/326-8703

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GENERAL DESCRIPTION

The AD6634 is a multimode 4-channel digital receive signal processor (RSP) capable of processing up to two WCDMA channels. Each channel consists of four cascaded signal processing elements: a frequency translator, two fixed coefficient decimating filters, and a programmable coefficient decimating filter. Each input port has input level threshold detection circuitry and an AGC controller for accommodating large dynamic ranges or situations where gain ranging converters are used. Dual 16-bit parallel output ports accommodate high data rate WBCDMA applications. On-chip interpolating half-band can also be used to further increase the output rate. In addition, each parallel output port has a digital AGC for output data scaling. Link port outputs are provided to enable glueless interfaces to ADI's TigerSHARC® DSP core.

The AD6634 is part of Analog Devices' SoftCell® Multicarrier transceiver chipset designed for compatibility with Analog Devices' family of high sample rate IF sampling ADCs (AD9238/AD6645 12- and 14-bit). The SoftCell receiver comprises a digital receiver capable of digitizing an entire spectrum of carriers and digitally selecting the carrier of interest for tuning and channel selection. This architecture eliminates redundant radios in wireless base station applications.

High dynamic range decimation filters offer a wide range of decimation rates. The RAM-based architecture allows easy reconfiguration for multimode applications.

The decimating filters remove unwanted signals and noise from the channel of interest. When the channel of interest occupies less bandwidth than the input signal, this rejection of out-of-band noise is called *processing gain*. By using large decimation factors, this processing gain can improve the SNR of the ADC by 30 dB or more. In addition, the programmable RAM coefficient filter allows antialiasing, matched filtering, and static equalization functions to be combined in a single, cost-effective filter. Half-band interpolating filters at the output are used in WCDMA applications to increase the output rate from 2× to 4× of the chip rate. The AD6634 is also equipped with two independent automatic gain control (AGC) loops for direct interface to a RAKE receiver.

The AD6634 is compatible with standard ADC converters such as the AD664x, AD923x, AD943x, and the AD922x families of data converters. The AD6634 is also compatible with the AD6600 diversity ADC, providing a cost and size reduction path.

ARCHITECTURE

The AD6634 has four signal processing stages: a frequency translator, second order resampling cascaded integrator comb FIR filters (rCIC2), a fifth order cascaded integrator comb FIR filter (CIC5), and a RAM coefficient FIR filter (RCF). Multiple modes are supported for clocking data into and out of the chip and provide flexibility for interfacing to a wide variety of digitizers. Programming and control are accomplished via serial and/or microprocessor interfaces.

Frequency translation is accomplished with a 32-bit, complex, numerically controlled oscillator (NCO). Real data entering this stage is separated into inphase (I) and quadrature (Q) components. This stage translates the input signal from a digital intermediate frequency (IF) to digital baseband. Phase and amplitude dither may be enabled on-chip to improve spurious performance of the NCO. A phase-offset word is available to create a known phase relationship among multiple AD6634s or between channels.

Following frequency translation is a resampling, fixed coefficient, high speed, second order, resampling cascade integrator comb (rCIC2) filter that reduces the sample rate based on the ratio between the decimation and interpolation registers.

The next stage is a fifth order cascaded integrator comb (CIC5) filter whose response is defined by the decimation rate. The purpose of this filter is to reduce the data rate to the final filter stage so that it can calculate more taps per output.

The final stage is a sum-of-products FIR filter with programmable 20-bit coefficients, and decimation rates programmable from 1 to 256 (1–32 in practice). The RAM coefficient FIR filter (RCF in the Functional Block Diagram) can handle a maximum of 160 taps.

The next stage is a fixed coefficient half-band interpolation filter where data from different channels is combined together and interpolated by a factor of 2. Next, an AGC section with a gain range of 96.3 dB is available. This AGC section is completely programmable in terms of its response. Two each of half-band filters and AGCs are present in the AD6634, as shown in the Functional Block Diagram. These half-band filters and AGC sections can be bypassed independent of each other.

The overall filter response for the AD6634 is the composite of all decimating and interpolating stages. Each successive filter stage is capable of narrower transition bandwidths but requires a greater number of CLK cycles to calculate the output. More decimation in the first filter stage will minimize overall power consumption. Data from the chip is interfaced to the DSP via either a high speed parallel port or a TigerSHARC compatible link port.

Figure 1a illustrates the basic function of the AD6634: to select and filter a single channel from a wide input spectrum. The frequency translator tunes the desired carrier to baseband. Figure 1b shows the combined filter response of the rCIC2, CIC5, and RCF.

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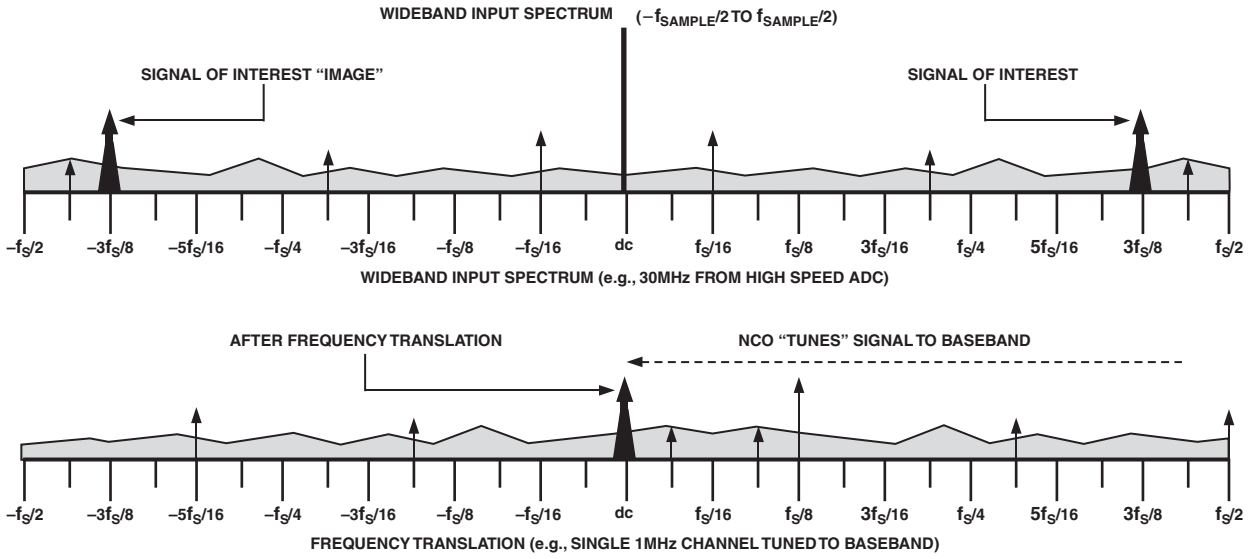


Figure 1a. Frequency Translation of Wideband Input Spectrum

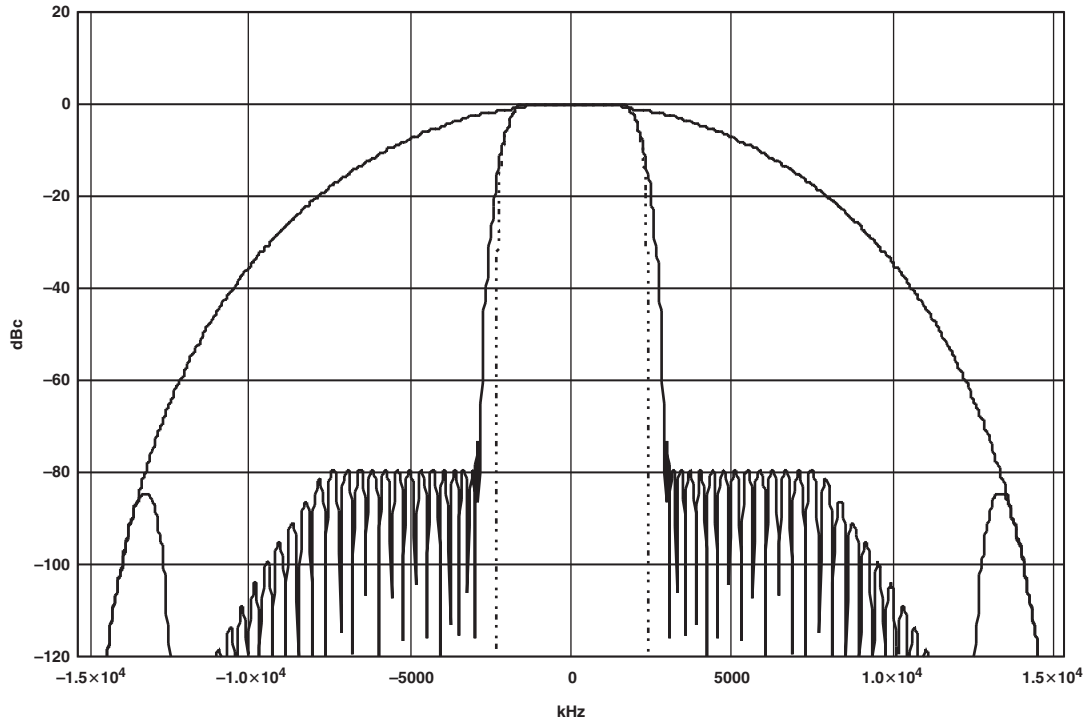


Figure 1b. Composite Filter Response of rCIC2, CIC5, and RCF

ABSOLUTE MAXIMUM RATINGS*

Supply Voltage . . . . . 3.6 V
Input Voltage . . . . . –0.3 V to +5.3 V (5 V Tolerant)
Output Voltage Swing . . . . . –0.3 V to VDDIO +0.3 V
Load Capacitance . . . . . 200 pF
Junction Temperature Under Bias . . . . . 125°C
Storage Temperature Range . . . . . –65°C to +150°C
Lead Temperature (5 sec) . . . . . 280°C

*Stresses greater than those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only; functional operation of the devices at these or any other conditions greater than those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

THERMAL CHARACTERISTICS

196-Lead BGA:
θ_{JA} = 41°C/W, No Airflow
θ_{JA} = 39°C/W, 200-lfpm Airflow
θ_{JA} = 37°C/W, 400-lfpm Airflow
Thermal measurements made in the horizontal position on a 4-layer board.

EXPLANATION OF TEST LEVELS

I. 100% Production Tested.
II. 100% Production Tested at 25°C, and Sampled Tested at Specified Temperatures.
III. Sample Tested Only
IV. Parameter Guaranteed by Design and Analysis
V. Parameter is Typical Value Only
VI. 100% Production Tested at 25°C, and Sampled Tested at Temperature Extremes

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
AD6634BBC	–40°C to +85°C (Ambient)	196-Lead CSPBGA (Ball Grid Array)	BC-196
AD6634BC/PCB		Evaluation Board with AD6634 and Software	

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD6634 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

SPECIFICATIONS

RECOMMENDED OPERATING CONDITIONS

Parameter	Temp	Test Level	AD6634BBC Min	Typ	Max	Unit
VDD		IV	2.25	2.5	2.75	V
VDDIO		IV	3.0	3.3	3.6	V
$T_{AMBIENT}$		IV	–40	+25	+85	°C

ELECTRICAL CHARACTERISTICS

Parameter (Conditions)	Temp	Test Level	AD6634BBC Min	Typ	Max	Unit
LOGIC INPUTS (5 V Tolerant)						
Logic Compatibility	Full	IV		3.3 CMOS		V
Logic "1" Voltage	Full	IV	2.0		5.0	V
Logic "0" Voltage	Full	IV	–0.3		+0.8	V
Logic "1" Current	Full	IV		1	10	µA
Logic "0" Current	Full	IV		1	10	µA
Logic "1" Current (Inputs with Pull-Down)	Full	IV				
Logic "0" Current (Inputs with Pull-Up)	Full	IV				
Input Capacitance	25°C	V		4		pF
LOGIC OUTPUTS						
Logic Compatibility	Full	IV		3.3 CMOS/TTL		V
Logic "1" Voltage (I_{OH} = 0.25 mA)	Full	IV	2.4	VDD–0.2		V
Logic "0" Voltage (I_{OL} = 0.25 mA)	Full	IV		0.2	0.4	V
IDD SUPPLY CURRENT						
CLK = 80 MHz, (VDD = 2.75 V, VDDIO = 3.6 V)	Full	IV				
I_{VDD}			397		443	mA
I_{VDDIO}			50		58	mA
CLK = GSM Example (65 MSPS, VDD = 2.5 V, VDDIO = 3.3 V, Dec = 2/10/6 120 Taps Four Channels)	25°C	V				
I_{VDD}				TBD		mA
I_{VDDIO}				TBD		mA
CLK = WBCDMA Example (76.8 MSPS, VDD = 2.5 V, VDDIO = 3.3 V, Dec = 2/10/6 120 Taps Four Channels)	25°C	V				
I_{VDD}				TBD		mA
I_{VDDIO}				TBD		mA
POWER DISSIPATION						
CLK = 80 MHz	Full	IV	1.05		1.45	W
CLK = 65 MHz GSM/EDGE Example		V		840		mW
CLK = 76.8 MHz WBCDMA Example		V		1.2		W
Sleep Mode	Full	IV		287		µW

Specifications subject to change without notice.

GENERAL TIMING CHARACTERISTICS[1, 2]

Parameter (Conditions)		Temp	Test Level	AD6634BBC Min	Typ	Max	Unit
CLK TIMING REQUIREMENTS							
t_{CLK}	CLK Period	Full	I	12.5			ns
t_{CLKL}	CLK Width Low	Full	IV	5.6	0.5 × t_{CLK}		ns
t_{CLKH}	CLK Width High	Full	IV	5.6	0.5 × t_{CLK}		ns
$\overline{\text{RESET}}$ TIMING REQUIREMENTS							
t_{RESL}	$\overline{\text{RESET}}$ Width Low	Full	I	30.0			ns
INPUT WIDEBAND DATA TIMING REQUIREMENTS							
t_{SI}	Input to ↑CLK Setup Time	Full	IV	2.0			ns
t_{HI}	Input to ↑CLK Hold Time	Full	IV	1.0			ns
LEVEL INDICATOR OUTPUT SWITCHING CHARACTERISTICS							
t_{DLI}	↑CLK to LI (A–A, B; B–A, B) Output Delay Time	Full	IV	3.3		10.0	ns
SYNC TIMING REQUIREMENTS							
t_{SS}	SYNC (A, B, C, D) to ↑CLK Setup Time	Full	IV	2.0			ns
t_{HS}	SYNC (A, B, C, D) to ↑CLK Hold Time	Full	IV	1.0			ns
SERIAL PORT CONTROL TIMING REQUIREMENTS SWITCHING CHARACTERISTICS[2]							
t_{SCLK}	SCLK Period	Full	IV	16			ns
t_{SCLKL}	SCLK Low Time	Full	IV	3.0			ns
t_{SCLKH}	SCLK High Time	Full	IV	3.0			ns
INPUT CHARACTERISTICS							
t_{SSI}	SDI to ↓SCLK Setup Time	Full	IV	1.0			ns
t_{HSI}	SDI to ↓SCLK Hold Time	Full	IV	1.0			ns
PARALLEL PORT TIMING REQUIREMENTS (MASTER MODE) SWITCHING CHARACTERISTICS[3]							
$t_{DPOCLKL}$	↓CLK to ↑PCLK Delay (Divide by 1)	Full	IV	6.5		10.5	ns
$t_{DPOCLKLL}$	↓CLK to ↑PCLK Delay (Divide by 2, 4, or 8)	Full	IV	8.3		14.6	ns
t_{DPREQ}	↑CLK to ↑PxREQ Delay					1.0	ns
t_{DPP}	↑CLK to Px[15:0] Delay					0.0	ns
INPUT CHARACTERISTICS							
t_{SPA}	PxACK to ↓PCLK Setup Time			+7.0			ns
t_{HPA}	PxACK to ↓PCLK Hold Time			–3.0			ns
PARALLEL PORT TIMING REQUIREMENTS (SLAVE MODE) SWITCHING CHARACTERISTICS[3]							
t_{POCLK}	PCLK Period	Full	I	12.5			ns
t_{POCLKL}	PCLK Low Period (when PCLK Divisor = 1)	Full	IV	2.0	0.5 × t_{POCLK}		ns
t_{POCLKH}	PCLK High Period (when PCLK Divisor = 1)	Full	IV	2.0	0.5 × t_{POCLK}		ns
t_{DPREQ}	↑CLK to ↑PxREQ Delay					10.0	ns
t_{DPP}	↑CLK to Px[15:0] Delay					11.0	ns
INPUT CHARACTERISTICS							
t_{SPA}	PxACK to ↓PCLK Setup Time			1.0			ns
t_{HPA}	PxACK to ↓PCLK Hold Time			1.0			ns
LINK PORT TIMING REQUIREMENTS SWITCHING CHARACTERISTICS[3]							
t_{RDLCLK}	↑PCLK to ↑LxCLKOUT Delay	Full	IV			2.5	ns
t_{FDLCLK}	↓PCLK to ↓LxCLKOUT Delay	Full	IV			0	ns
$t_{RLCLKDAT}$	↑LCLKOUT to Lx[7:0] Delay	Full	IV	0		2.9	ns
$t_{FLCLKDAT}$	↓LCLKOUT to Lx[7:0] Delay	Full	IV	0		2.2	ns

NOTES
[1]All Timing Specifications valid over VDD range of 2.25 V to 2.75 V and VDDIO range of 3.0 V to 3.6 V.
[2]C_{LOAD} = 40 pF on all outputs unless otherwise specified
[3]The timing parameters for Px[15:0], PxREQ, PxACK, LxCLKOUT, Lx[7:0] apply for port A and B (x stands for A or B).

Specifications subject to change without notice.

MICROPROCESSOR PORT TIMING CHARACTERISTICS[1, 2]

Parameter (Conditions)		Temp	Test Level	AD6634BBC Min	Typ	Max	Unit
MICROPROCESSOR PORT, MODE INM (MODE = 0)							
MODE INM WRITE TIMING							
t_{SC}	Control[3] to ↑CLK Setup Time	Full	IV	2.0			ns
t_{HC}	Control[3] to ↑CLK Hold Time	Full	IV	2.5			ns
t_{HWR}	$\overline{WR}$(RW) to RDY($\overline{DTACK}$) Hold Time	Full	IV	7.0			ns
t_{SAM}	Address/Data to $\overline{WR}$(RW) Setup Time	Full	IV	3.0			ns
t_{HAM}	Address/Data to RDY($\overline{DTACK}$) Hold Time	Full	IV	5.0			ns
t_{DRDY}	$\overline{WR}$(RW) to RDY($\overline{DTACK}$) Delay	Full	IV	8.0			ns
t_{ACC}	$\overline{WR}$(RW) to RDY($\overline{DTACK}$) High Delay	Full	IV	$4 \times t_{CLK}$	$5 \times t_{CLK}$	$9 \times t_{CLK}$	ns
MODE INM READ TIMING							
t_{SC}	Control[3] to ↑CLK Setup Time	Full	IV	5.0			ns
t_{HC}	Control[3] to ↑CLK Hold Time	Full	IV	2.0			ns
t_{SAM}	Address to $\overline{RD}$($\overline{DS}$) Setup Time	Full	IV	0.0			ns
t_{HAM}	Address to Data Hold Time	Full	IV	5.0			ns
t_{DRDY}	$\overline{RD}$($\overline{DS}$) to RDY($\overline{DTACK}$) Delay	Full	IV	8.0			ns
t_{ACC}	$\overline{RD}$($\overline{DS}$) to RDY($\overline{DTACK}$) High Delay	Full	IV	$8 \times t_{CLK}$	$10 \times t_{CLK}$	$13 \times t_{CLK}$	ns
MICROPROCESSOR PORT, MODE MNM (MODE = 1)							
MODE MNM WRITE TIMING							
t_{SC}	Control[3] to ↑CLK Setup Time	Full	IV	2.0			ns
t_{HC}	Control[3] to ↑CLK Hold Time	Full	IV	2.5			ns
t_{HDS}	$\overline{DS}$($\overline{RD}$) to $\overline{DTACK}$(RDY) Hold Time	Full	IV	8.0			ns
t_{HRW}	RW($\overline{WR}$) to $\overline{DTACK}$(RDY) Hold Time	Full	IV	7.0			ns
t_{SAM}	Address/Data to RW($\overline{WR}$) Setup Time	Full	IV	3.0			ns
t_{HAM}	Address/Data to RW($\overline{WR}$) Hold Time	Full	IV	5.0			ns
t_{DDTACK}	$\overline{DS}$($\overline{RD}$) to $\overline{DTACK}$(RDY) Delay	Full	IV	8.0			ns
t_{ACC}	RW($\overline{WR}$) to $\overline{DTACK}$(RDY) Low Delay	Full	IV	$4 \times t_{CLK}$	$5 \times t_{CLK}$	$9 \times t_{CLK}$	ns
MODE MNM READ TIMING							
t_{SC}	Control[3] to ↑CLK Setup Time	Full	IV	5.0			ns
t_{HC}	Control[3] to ↑CLK Hold Time	Full	IV	2.0			ns
t_{HDS}	$\overline{DS}$($\overline{RD}$) to $\overline{DTACK}$(RDY) Hold Time	Full	IV	8.0			ns
t_{SAM}	Address to $\overline{DS}$($\overline{RD}$) Setup Time	Full	IV	0.0			ns
t_{HAM}	Address to Data Hold Time	Full	IV	5.0			ns
t_{DDTACK}	$\overline{DS}$($\overline{RD}$) to $\overline{DTACK}$(RDY) Delay	Full	IV	8.0			ns
t_{ACC}	$\overline{DS}$($\overline{RD}$) to $\overline{DTACK}$(RDY) Low Delay	Full	IV	$8 \times t_{CLK}$	$10 \times t_{CLK}$	$13 \times t_{CLK}$	ns

NOTES
[1]All Timing Specifications valid over VDD range of 2.25 V to 2.75 V and VDDIO range of 3.0 V to 3.6 V.
[2]C_{LOAD} = 40 pF on all outputs, unless otherwise specified.
[3]Specification pertains to control signals: R/W, ($\overline{WR}$), $\overline{DS}$ ($\overline{RD}$), $\overline{CS}$.

Specifications subject to change without notice.

TIMING DIAGRAMS

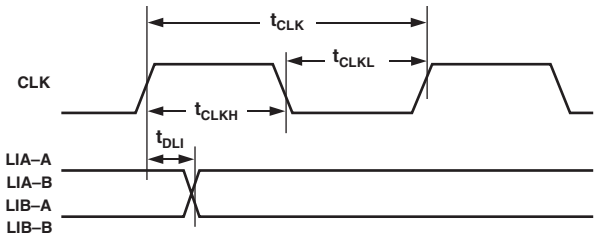


Figure 2. Level Indicator Output Switching Characteristics

Figure 3. $\overline{RESET}$ Timing Requirements

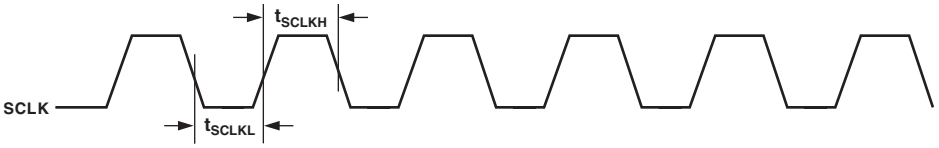


Figure 4. SCLK Switching Characteristics

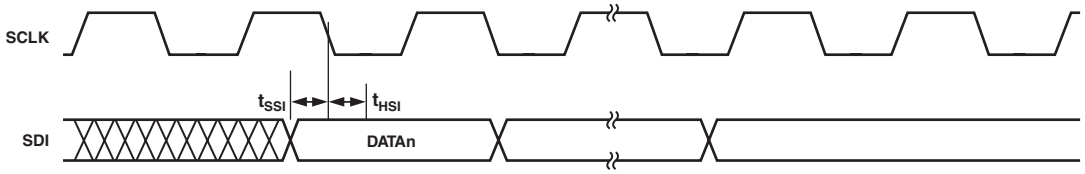


Figure 5. Serial Port Input Timing Characteristics

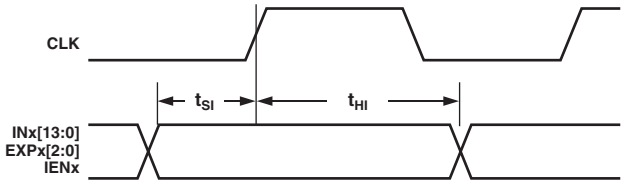


Figure 6. Input Timing for A and B Channels

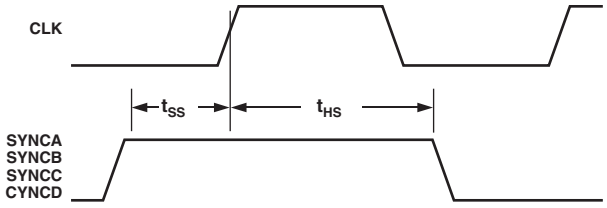


Figure 7. SYNC Timing Inputs

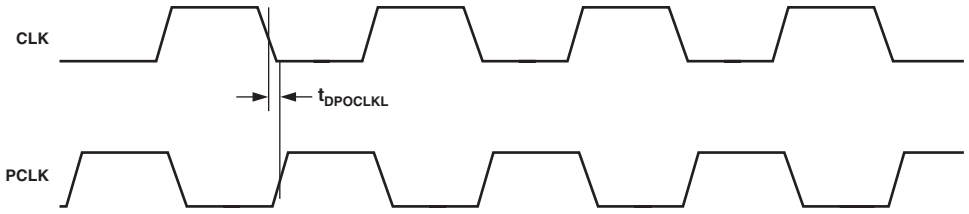


Figure 8. PCLK to CLK Switching Characteristics Divide by 1

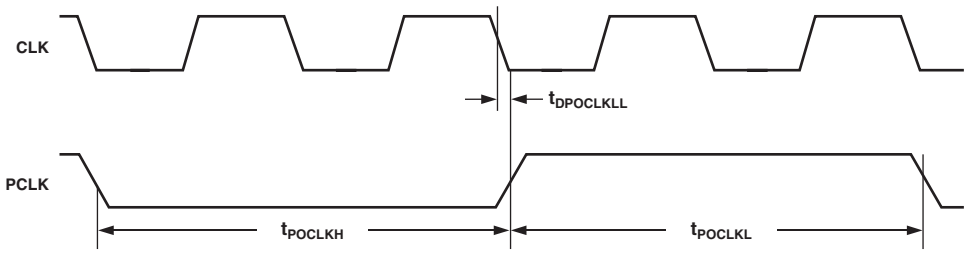


Figure 9. PCLK to CLK Switching Characteristics Divide by 2, 4, or 8

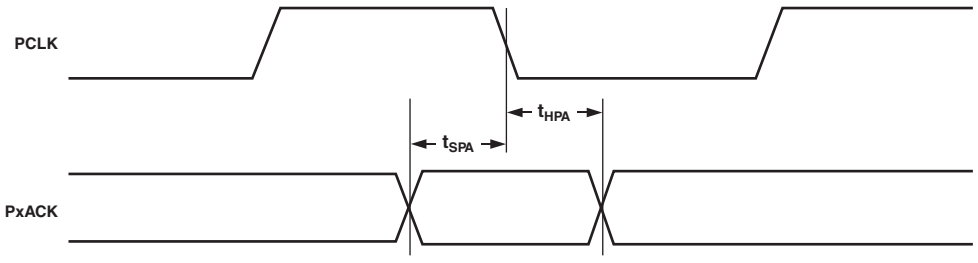


Figure 10. Master Mode PxACK to PCLK Setup and Hold Characteristics

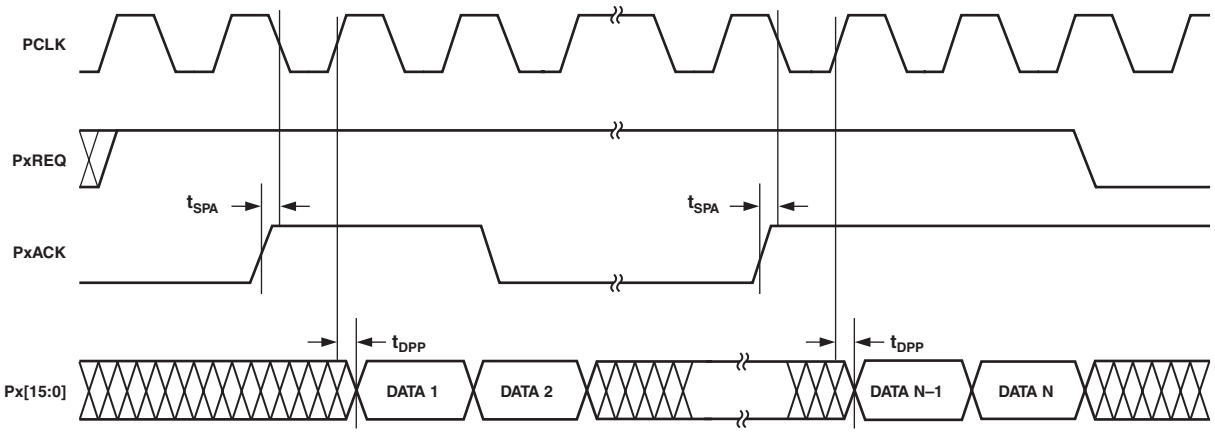


Figure 11. Master Mode PxACK to PCLK Switching Characteristics

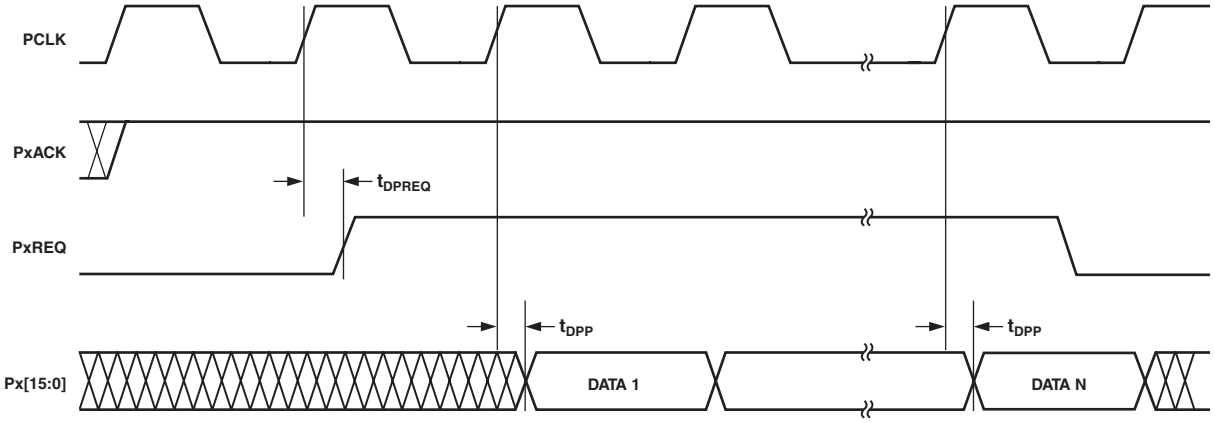


Figure 12. Master Mode PxREQ to PCLK Switching Characteristics

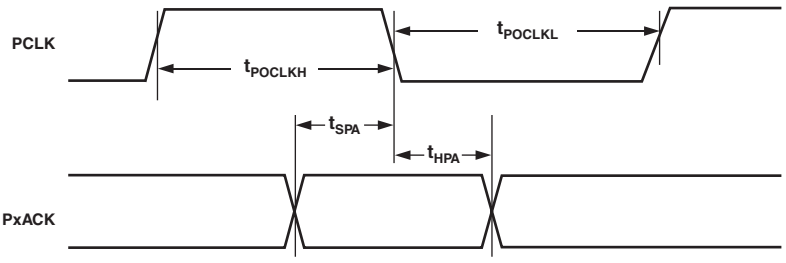


Figure 13. Slave Mode PxACK to PCLK Setup and Hold Characteristics

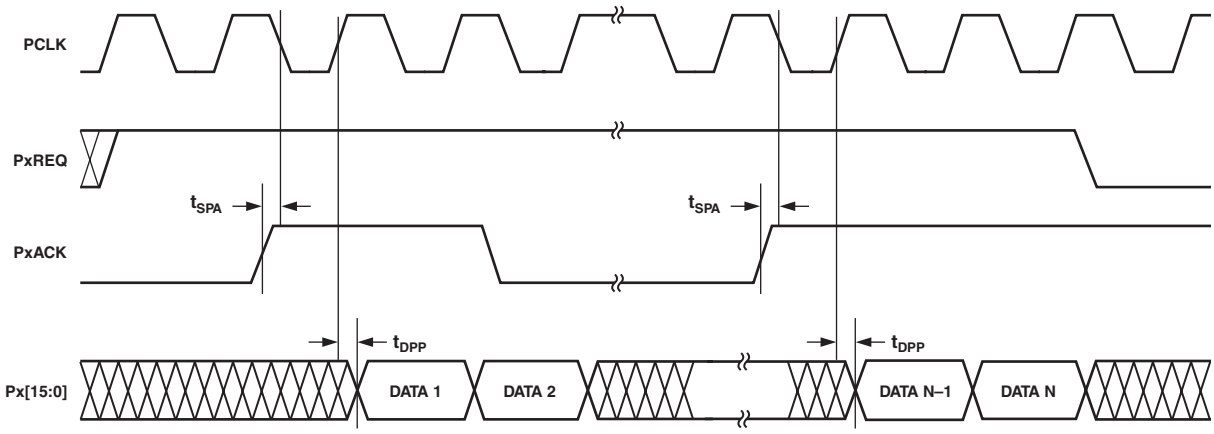


Figure 14. Slave Mode PxACK to PCLK Switching Characteristics

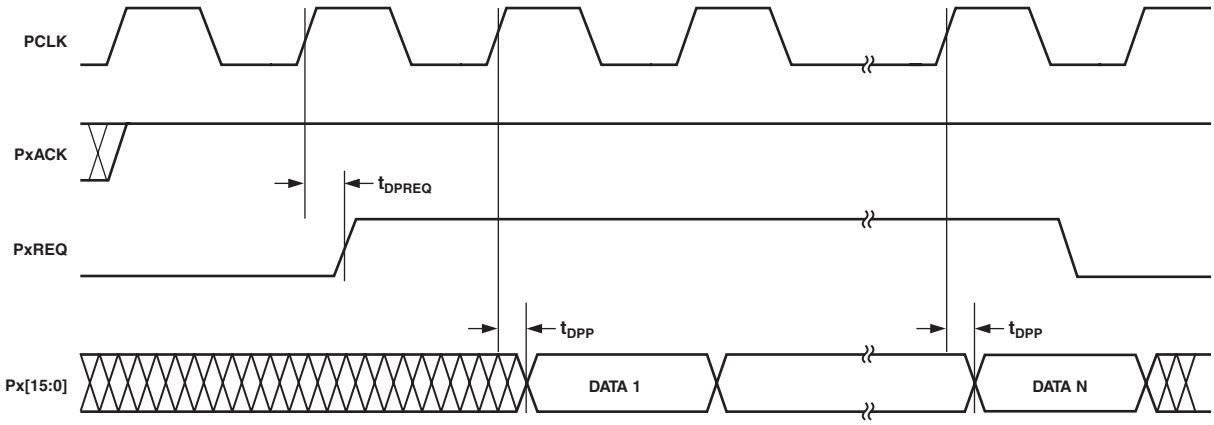


Figure 15. Slave Mode PxREQ to PCLK Switching Characteristics

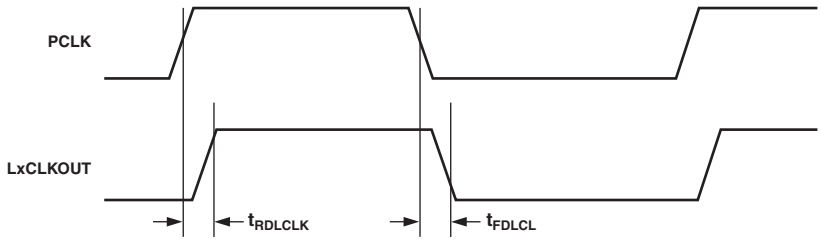


Figure 16. LxCLKOUT to PCLK Switching Characteristics

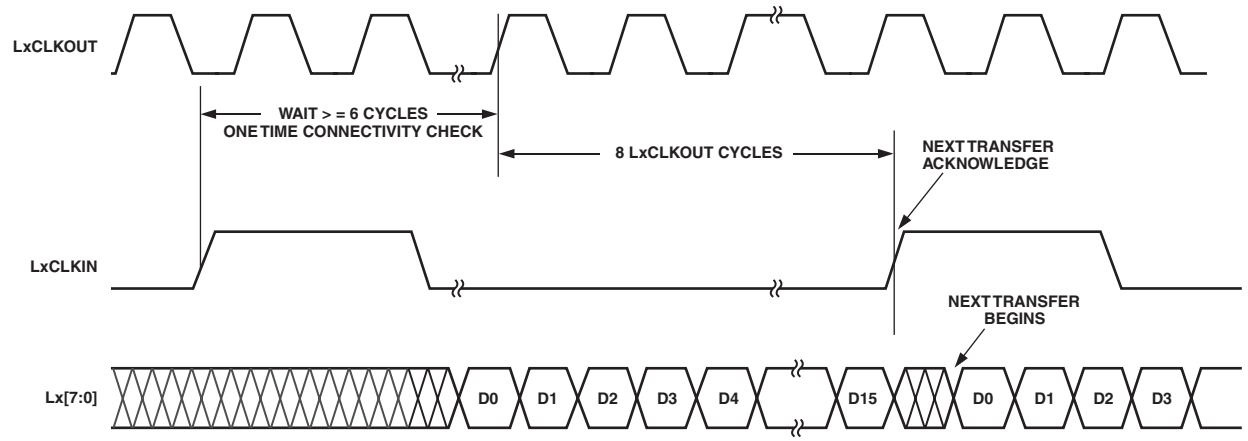


Figure 17. LxCLKIN to LxCLKOUT Data Switching Characteristics

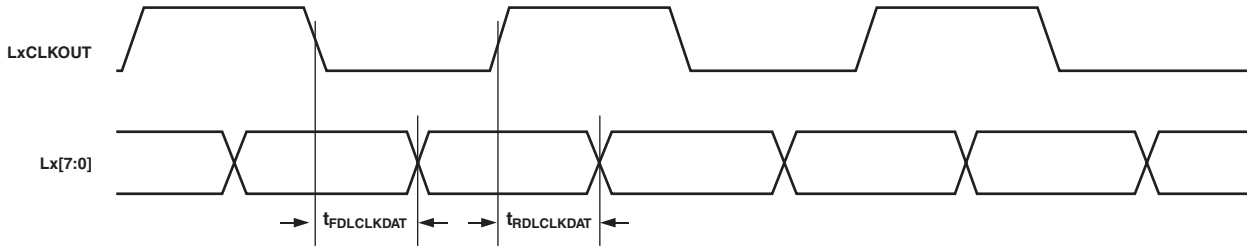
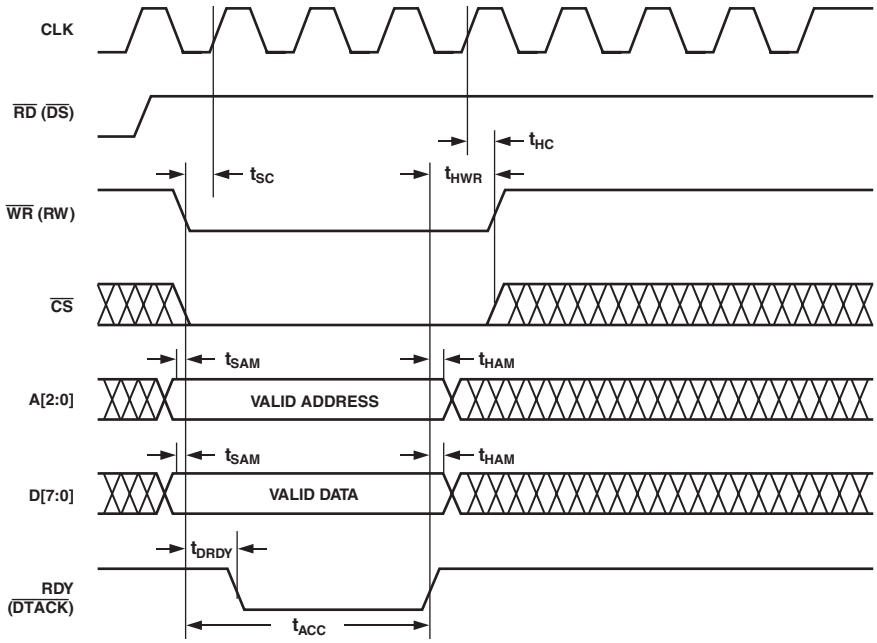


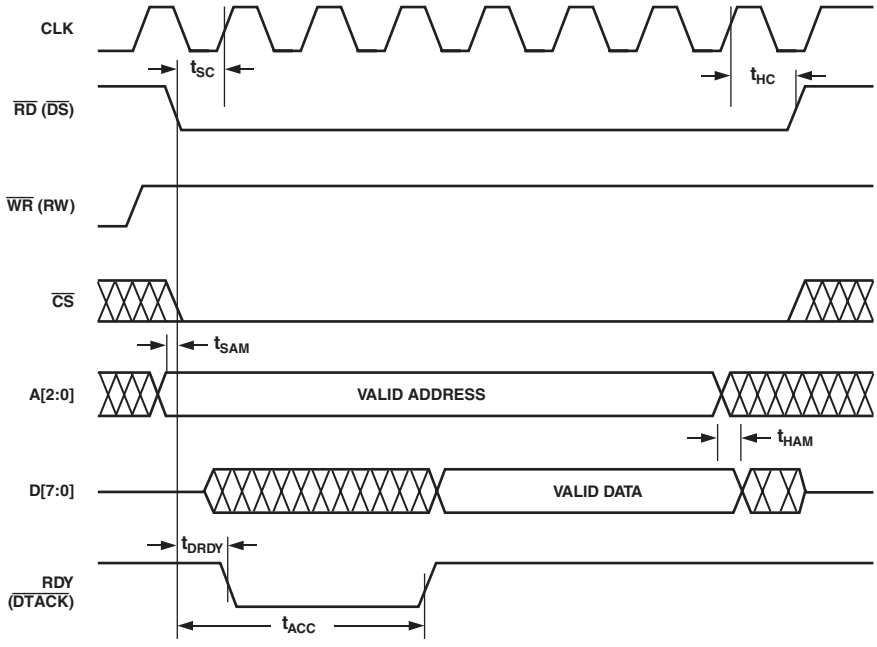
Figure 18. LxCLKOUT to Lx[7:0] Data Switching Characteristics

TIMING DIAGRAMS—INM MICROPORT MODE



NOTES
1. t_{ACC} ACCESS TIME DEPENDS ON THE ADDRESS ACCESSED. ACCESS TIME IS MEASURED FROM FE OF $\overline{WR}$ TO RE OF RDY.
2. t_{ACC} REQUIRES A MAXIMUM OF 9 CLK PERIODS.

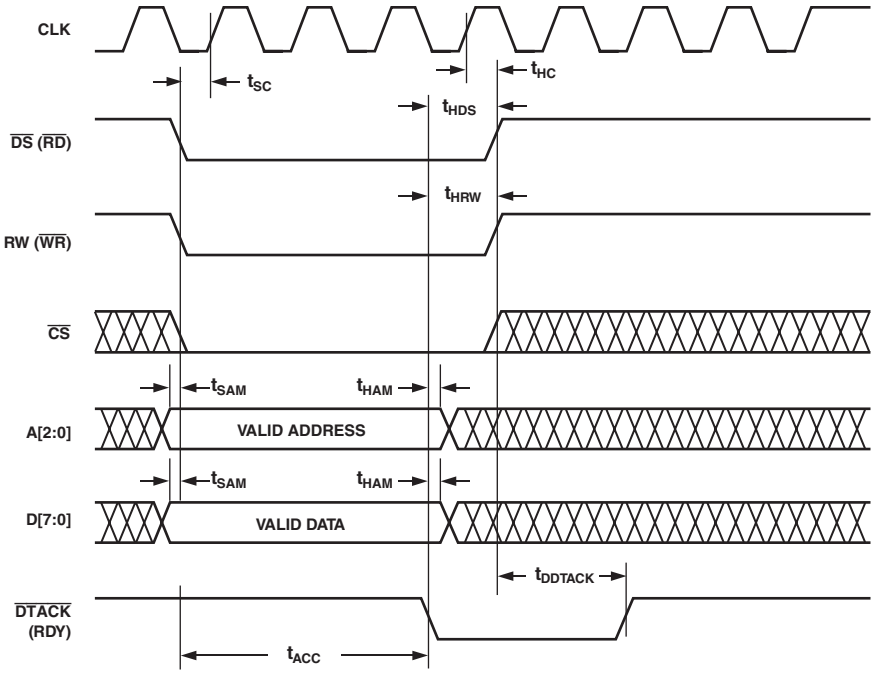
Figure 19. INM Microport Write Timing Requirements



NOTES
1. t_{ACC} ACCESS TIME DEPENDS ON THE ADDRESS ACCESSED. ACCESS TIME IS MEASURED FROM FE OF $\overline{WR}$ TO RE OF RDY.
2. t_{ACC} REQUIRES A MAXIMUM OF 13 CLK PERIODS.

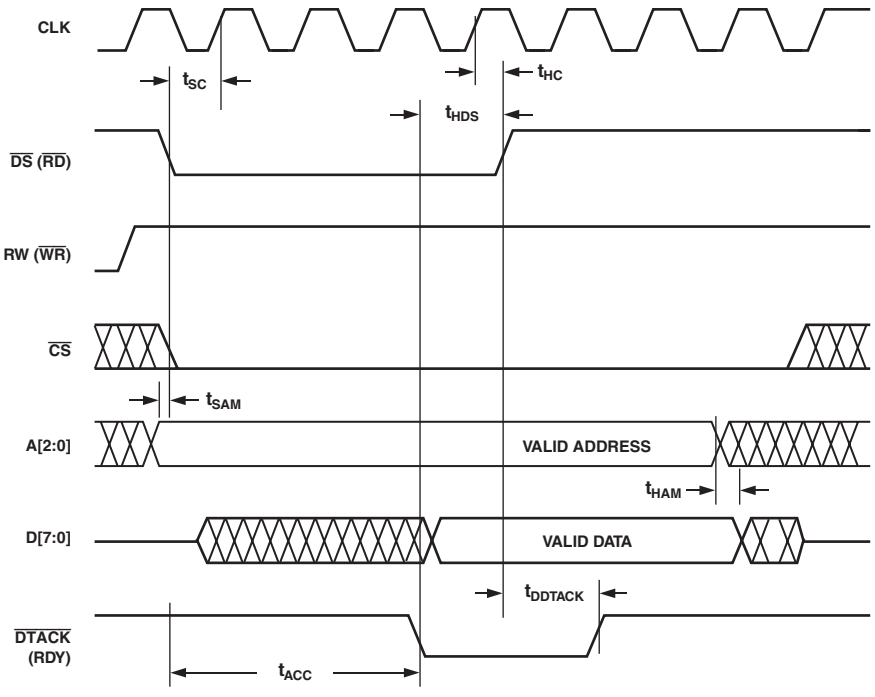
Figure 20. INM Microport Read Timing Requirements

TIMING DIAGRAMS—MNM MICROPORT MODE



NOTES
1. t_{ACC} ACCESS TIME DEPENDS ON THE ADDRESS ACCESSED. ACCESS TIME IS MEASURED FROM FE OF $\overline{DS}$ TO THE FE OF $\overline{DTACK}$.
2. t_{ACC} REQUIRES A MAXIMUM OF 9 CLK PERIODS.

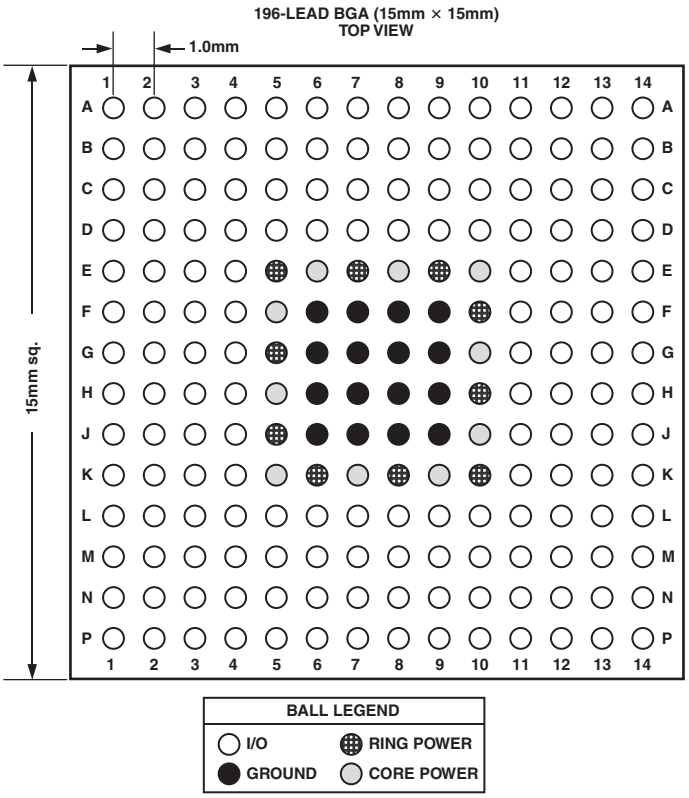
Figure 21. MNM Microport Write Timing Requirements



NOTES
1. t_{ACC} ACCESS TIME DEPENDS ON THE ADDRESS ACCESSED. ACCESS TIME IS MEASURED FROM THE FE OF $\overline{DS}$ TO THE FE OF $\overline{DTACK}$.
2. t_{ACC} REQUIRES A MAXIMUM OF 13 CLK PERIODS.

Figure 22. MNM Microport Read Timing Requirements

PIN CONFIGURATION



	1	2	3	4	5	6	7	8	9	10	11	12	13	14	
A	NO CONNECT	INB6	INB9	INB11	EXPB1	VDDIO (RESERVED)	PB14	PB12	PB10	PB1 | LB1	PB2 | LB2	PB5 | LB5	PBCH1 | LBCLKIN	NO CONNECT	A
B	INB2	INB4	INB5	INB8	INB12	EXPB0	PB15	PB13	PB11	PB4 | LB4	PB0 | LB0	PB3 | LB3	PBCH0 | LBCLKOUT	PB7 | LB7	B
C	INB0	INB3	INB7	INB13	INB10	EXPB2	PBACK	PBREQ	PB9	PB8		PBIQ	PCLK	PB6 | LB6	C
D	LIB-B	INB1										PAACK	SDI	PAIQ	D
E	CLK	IENB			VDDIO	VDD	VDDIO	VDD	VDDIO	VDD		SCLK	CHIP_ID2	CHIP_ID3	E
F	EXPA1	EXPA0	EXPA2		VDD	GND	GND	GND	GND	VDDIO			CHIP_ID0	CHIP_ID1	F
G	INA12	INA13	INA10		VDDIO	GND	GND	GND	GND	VDD			TDI	TMS	G
H	INA11	INA9	INA7		VDD	GND	GND	GND	GND	VDDIO			PA14	PA15	H
J	INA8	INA6			VDDIO	GND	GND	GND	GND	VDD		PAREQ	PA12	PA13	J
K	INA5	INA4			VDD	VDDIO	VDD	VDD	VDD	VDDIO		TDO	PA10	PA11	K
L	INA3	INA1										TCLK	PA8	PA9	L
M	INA2	IENA		$\overline{\text{DTACK}}$ (RDY)	MODE	$\overline{\text{CS}}$	RW ($\overline{\text{WR}}$)	$\overline{\text{TRST}}$	$\overline{\text{DS}}$($\overline{\text{RD}}$)	A1	A0	PA4 | LA4	PA2 | LA2	PA0 | LA0	M
N	INA0	LIB-A	LIA-B	SYNCB	SYNCD	D7	D5	D3	D1	A2	PCHA1 | LACLKIN	PA5 | LA5	PA3 | LA3	PA1 | LA1	N
P	NO CONNECT	LIA-A	SYNCA	SYNCC	$\overline{\text{RESET}}$	D6	D4	D2	D0	PA6 | LA6	PCHA0 | LACLKOUT	PA7 | LA7		NO CONNECT	P
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	

PIN FUNCTION DESCRIPTIONS

	Mnemonic	Type	Function
POWER SUPPLY			
	VDD	P	2.5 V Supply
	VDDIO	P	3.3 V IO Supply
	GND	G	Ground
INPUTS			
	INA[13:0][1]	I	A Input Data (Mantissa)
	EXPA[2:0][1]	I	A Input Data (Exponent)
	IENA[2]	I	Input Enable—Input A
	INB[13:0][1]	I	B Input Data (Mantissa)
	EXPB[2:0][1]	I	B Input Data (Exponent)
	$\overline{\text{IENB}}$[2]	I	Input Enable—Input B
	$\overline{\text{RESET}}$	I	Active Low Reset Pin
	CLK	I	Input Clock
	PCLK	I/O	Link/Parallel Port Clock
	LACLKIN	I	Link Port A Data Ready
	LBCLKIN	I	Link Port B Data Ready
	SYNCA[1]	I	All Sync pins go to all four output channels.
	SYNCB[1]	I	All Sync pins go to all four output channels.
	SYNCC[1]	I	All Sync pins go to all four output channels.
	SYNCD[1]	I	All Sync pins go to all four output channels.
	$\overline{\text{CS}}$[1]	I	Chip Select
	CHIP_ID[3:0][1]	I	Chip ID Selector
CONTROL			
	PAACK	I	Parallel Port A Acknowledge
	PAREQ	O	Parallel Port A Request
	PBACK	I	Parallel Port B Acknowledge
	PBREQ	O	Parallel Port B Request
MICROPORT CONTROL			
	D[7:0]	I/O/T	Bidirectional Microport Data
	A[2:0]	I	Microport Address Bus
	$\overline{\text{DS}}$($\overline{\text{RD}}$)	I	Active Low Data Strobe (Active Low Read)
	$\overline{\text{DTACK}}$(RDY)[2]	O/T	Active Low Data Acknowledge (Microport Status Bit)
	R/$\overline{\text{W}}$($\overline{\text{WR}}$)	I	Read Write (Active Low Write)
	MODE	I	Intel or Motorola Mode Select
SERIAL PORT CONTROL			
	SDI[1]	I	Serial Port Control Data Input
	SCLK[1]	I	Serial Port Control Clock
OUTPUTS			
	LIA–A	O	Level Indicator—Input A, Interleaved–Data A
	LIA–B	O	Level Indicator—Input A, Interleaved–Data B
	LIB–B	O	Level Indicator—Input B, Interleaved–Data B
	LIB–A	O	Level Indicator—Input B, Interleaved–Data A
	LACLKOUT	O	Link Port A Clock Output
	LBCLKOUT	O	Link Port B Clock Output
	LA[7:0]	O	Link Port A Output Data
	LB[7:0]	O	Link Port B Output Data
	PA[15:0]	O	Parallel Output Data Port A
	PB[15:0]	O	Parallel Output Data Port B
	PACH[1:0]	O	Parallel Output Port A Channel Indicator
	PBCH[1:0]	O	Parallel Output Port B Channel Indicator
	PAIQ	O	Parallel Port A I/Q Data Indicator
	PBIQ	O	Parallel Port B I/Q Data Indicator
JTAG AND BIST			
	$\overline{\text{TRST}}$[2]	I	Test Reset Pin
	TCLK[1]	I	Test Clock Input
	TMS[2]	I	Test Mode Select Input
	TDO	O/T	Test Data Output
	TDI[2]	I	Test Data Input

NOTES
[1]Pins with a pull-down resistor of nominal 70 kΩ.
[2]Pins with a pull-up resistor of nominal 70 kΩ.

EXAMPLE FILTER RESPONSE

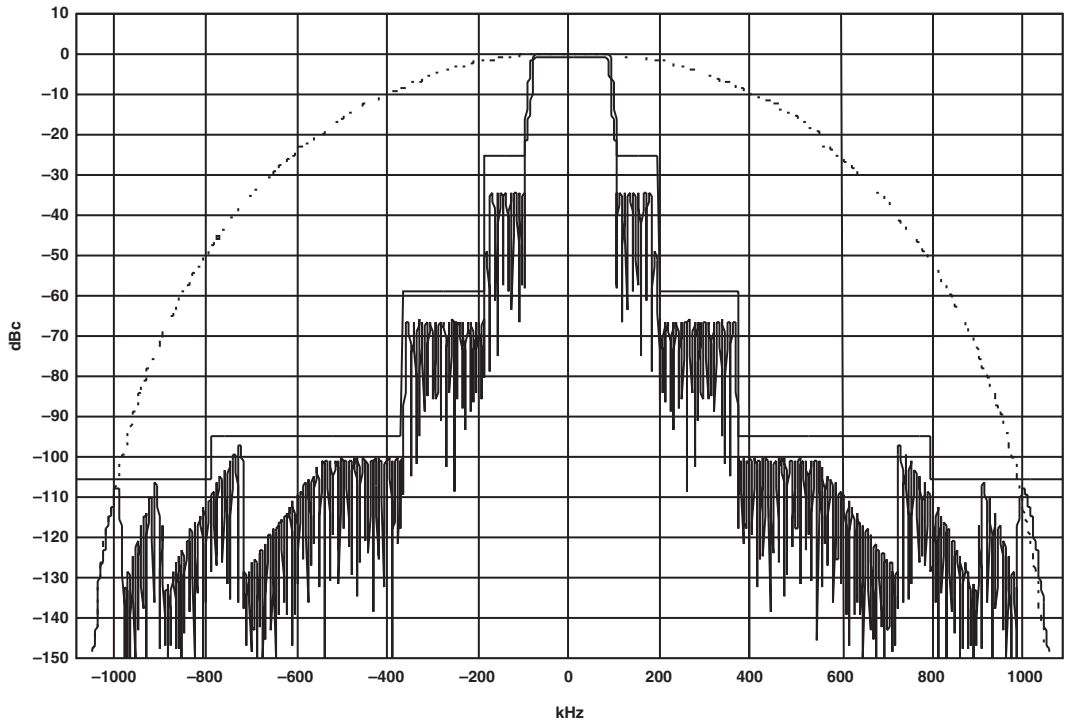


Figure 23. The Filter Above Is Based on a 65 MSPS Input Data Rate and an Output Rate of 541.6666 kSPS (Two Samples per Symbol for EDGE). Total decimation rate is 120, distributed between the rCIC2, CIC5, and RCF.

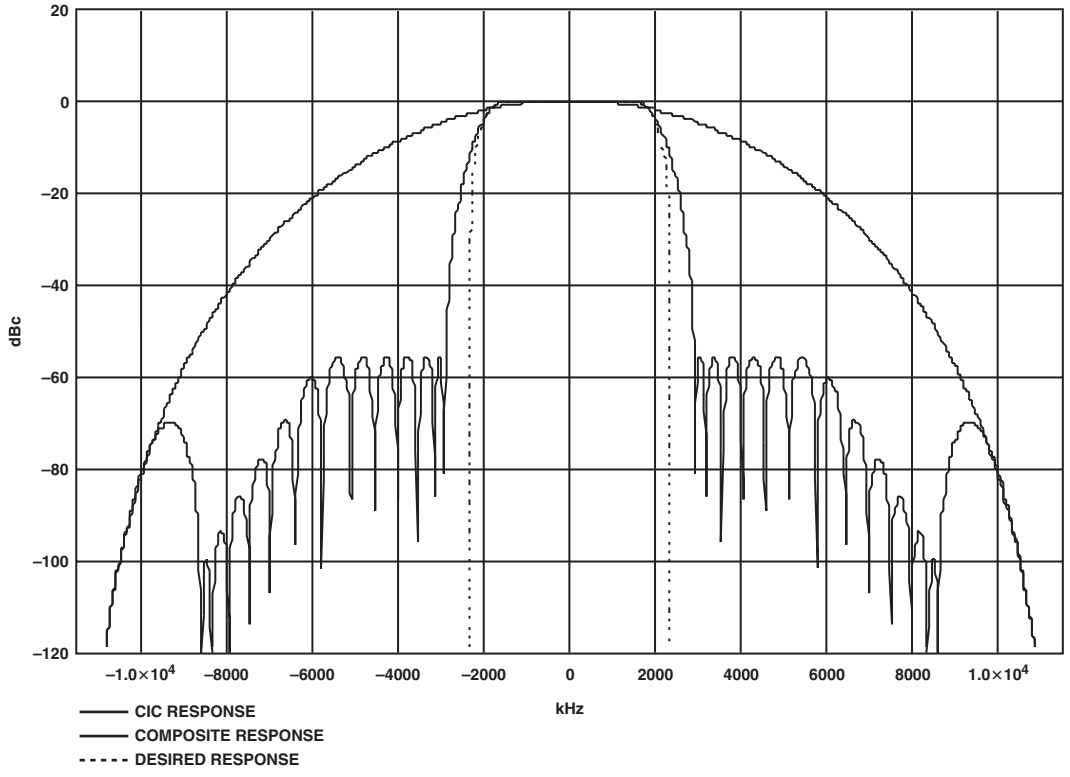


Figure 24. The Filter Above Is Designed to Meet UMTS Specifications. For this configuration, the clock is set to 76.8 MSPS with 20× chip rate (3.84 MCPS) and a 2× output data rate of 7.68 MCPS using two channels of the AD6634.

INPUT DATA PORTS

The AD6634 features dual high speed ADC input ports, input port A and input port B. The dual input ports allow for the most flexibility with a single tuner chip. These can be diversity inputs or truly independent inputs such as separate antenna segments. Either ADC port can be routed to one of four tuner channels. For added flexibility, each input port can be used to support multiplexed inputs such as those found on the AD6600 or other ADCs with multiplexed outputs. This added flexibility can allow for up to four different analog sources to be processed simultaneously by the four internal channels.

In addition, the front end of the AD6634 contains circuitry that enables high speed signal level detection and control. This is accomplished with a unique high speed level detection circuit that offers minimal latency and maximum flexibility to control up to four analog signal paths. The overall signal path latency from input to output on the AD6634 can be expressed in high speed clock cycles. The following equation can be used to calculate the latency.

$$T_{LATENCY} = M_{rCIC2}\left(M_{CIC5} + 7\right) + N_{TAPS} + 26$$

M_{rCIC2} and M_{CIC5} are decimation values for the rCIC2 and CIC5 filters, respectively. N_{TAPS} is the number RCF taps chosen.

Input Data Format

Each input port consists of a 14-bit mantissa and 3-bit exponent. If interfacing to a standard ADC is required, the exponent bits can be grounded. If connected to a floating point ADC such as the AD6600, the exponent bits from that product can be connected to the input exponent bits of the AD6634. The mantissa data format is two's complement and the exponent is unsigned binary.

Input Timing

The data from each high speed input port is latched on the rising edge of CLK. This clock signal is used to sample the input port and clock the synchronous signal processing stages that follow in the selected channels.

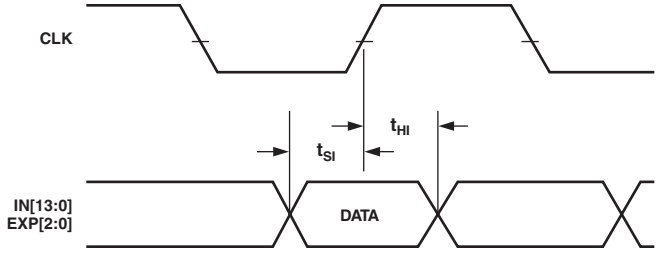


Figure 25. Input Data Timing Requirements

The clock signals can operate up to 80 MHz and have a 50% duty cycle. In applications using high speed ADCs, the ADC sample clock or data valid strobe is typically used to clock the AD6634.

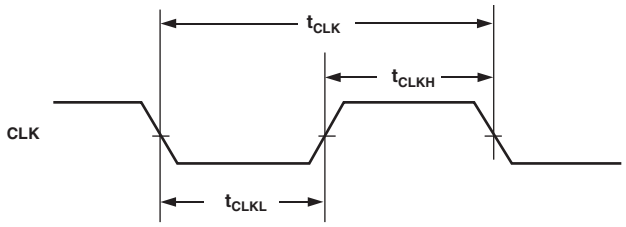


Figure 26. CLK Timing Requirements

Input Enable Control

There is an IENA and an IENB pin for Input Port A and Input Port B, respectively. There are four modes of operation possible while using each IEN pin. Using these modes, it is possible to emulate operation of the other RSPs, such as the AD6620, which offer dual channel modes normally associated with diversity operations. These modes are: IEN transition to Low, IEN transition to High, IEN High, and Blank on IEN low.

In the IEN High mode, the inputs and normal operations occur when the input enable is high. In the IEN transition to Low mode, normal operations occur on the first rising edge of the clock after the IEN transitions to low. Likewise in the IEN transition to High mode, operations occur on the rising edge of the clock after the IEN transitions to High. (See the Numerically Controlled Oscillator section for more details on configuring the Input Enable Modes.) In Blank on IEN low mode, the input data is interpreted as zero when IEN is low.

A typical application for this feature would be to take the data from an AD6600 Diversity ADC to one of the inputs of the AD6634. The A/B_OUT from that chip would be tied to the IEN. Then one channel within the AD6634 would be set so that IEN transition to Low is enabled. Another channel would be configured so that IEN transition to High is enabled. This would allow two of the AD6634 channels to be configured to emulate that AD6620 in diversity mode. Of course the NCO frequencies and other channel characteristics would need to be set similarly, but this feature allows the AD6634 to handle interleaved data streams such as those found on the AD6600.

The difference between the IEN transition to high and the IEN high is found when a system clock is provided that is higher than the data rate of the converter. It is often advantageous to supply a clock that runs faster than the data rate so that additional filter taps can be computed. This naturally provides better filtering. In order to ensure that other parts of the circuit properly recognize the faster clock in the simplest manner, the IEN transition to low or high should be used. In this mode, only the first clock edge that meets the setup and hold times will be used to latch and process the input data. All other clock pulses are ignored by front end processing. However, each clock cycle will still produce a new filter computation pair.

Gain Switching

The AD6634 includes circuitry that is useful in applications where either large dynamic ranges exist or where gain ranging converters are employed. This circuitry allows digital thresholds to be set such that an upper and a lower threshold can be programmed.

One such use of this may be to detect when an ADC is about to reach full scale with a particular input condition. The results would be to provide a flag that could be used to quickly insert an attenuator that would prevent ADC overdrive. If 18 dB (or any arbitrary value) of attenuation (or gain) is switched in, the signal dynamic range of the system will have been increased by 18 dB. The process begins when the input signal reaches the upper programmed threshold. In a typical application, this may be set 1 dB (user-definable) below full scale. When this input condition is met, the appropriate LI (LIA-A, LIA-B, LIB-A, or LIB-B) signal associated with either the A or B input port is made active. This can be used to switch the gain or attenuation of the external circuit. The LI line stays active until the input condition falls below the lower programmed threshold. In order to provide hysteresis, a dwell time register (see Memory Map for Input Control Registers) is available to hold off switching of the control line for a predetermined number of clocks. Once the input condition is below the lower threshold, the programmable counter begins counting high speed clocks. As long as the input signal stays below the lower threshold for the number of high speed clock cycles programmed, the attenuator will be removed on the terminal count. However, if the input condition goes above the lower threshold with the counter running, it will be reset and must fall below the lower threshold again to initiate the process. This will prevent unnecessary switching between states and is illustrated in Figure 27.

When the input signal goes above the upper threshold, the appropriate LI signal becomes active. Once the signal falls below the lower threshold, the counter begins counting. If the input condition goes above the lower threshold, the counter is reset and starts again as shown in Figure 27. Once the counter has terminated to 0, the LI line goes inactive.

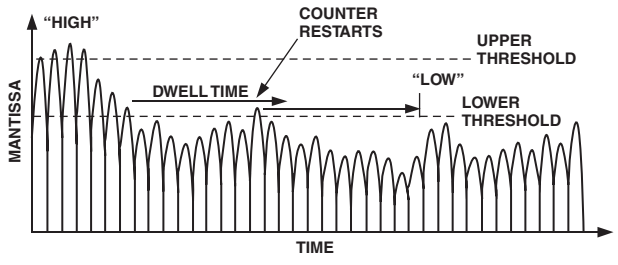


Figure 27. Threshold Settings for LI

The LI line can be used for a variety of functions. It can be used to set the controls of an attenuator, DVGA, or integrated and used with an analog VGA. To simplify the use of this feature, the AD6634 includes two separate gain settings, one when this line is inactive (rCIC2_QUIET[4:0] stored in bits 9:5 of 0x92 register) and the other when active (rCIC2_LOUD[4:0] stored in bits 4:0 of 0x92 register). This allows the digital gain to be adjusted to the external changes. In conjunction with the gain setting, a variable hold-off is included to compensate for the pipeline delay of the ADC and the switching time of the gain control element. Together, these two features provide seamless gain switching.

Another use of this pin is to facilitate a gain range hold-off within a gain ranging ADC. For converters that use gain ranging to increase total signal dynamic range, it may be desirable to prohibit internal gain ranging from occurring in some instances. For such converters, the LI (A or B) line can be used to hold this off. For this application, the upper threshold would be set based on similar criteria. However, the lower threshold would be set to a level consistent with the gain ranges of the specific converter. The hold-off delay can then be set appropriately for any of a number of factors such as fading profile, signal peak to average ratio, or any other time-based characteristics that might cause unnecessary gain changes.

Since the AD6634 has a total of four gain control circuits that can be used if both A and B input ports have interleaved data. Each respective LI pin is independent and can be set to different set points. It should be noted that the gain control circuits are wideband and are implemented prior to any filtering elements to minimize loop delay. Any of the four channels can be set to monitor any of the possible four input channels (two in normal mode and four when the inputs are time multiplexed).

The chip also provides appropriate scaling of the internal data based on the attenuation associated with the LI signal. In this manner, data to the DSP maintains a correct scale value throughout the process, making it totally independent. Since there are often finite delays associated with external gain switching components, the AD6634 includes a variable pipeline delay that can be used to compensate for external pipeline delays or gross settling times associated with gain/attenuator devices. This delay may be set up to seven high speed clocks. These features ensure smooth switching between gain settings.

Input Data Scaling

The AD6634 has two data input ports, an A input port and a B input port. Each accepts 14-bit mantissa (two's complement integer) IN[13:0], a 3-bit exponent (unsigned integer) EXP[2:0] and the Input Enable(IEN). Both inputs are clocked by CLK. These pins allow direct interfacing to both standard fixed-point ADCs such as the AD9238 and AD6645, as well as to gain-ranging ADCs such as the AD6600. For normal operation with ADCs having fewer than 14 bits, the active bits should be MSB justified and the unused LSBs should be tied low.

The 3-bit exponent, EXP[2:0] is interpreted as an unsigned integer. The exponent will subsequently be modified by either of rCIC2_LOUD[4:0] or rCIC2_QUIET[4:0] depending on whether LI line is active or not. These 5-bit scale values are stored in the rCIC2 scale register (0x92) and the scaling is applied before the data enters the rCIC2 resampling filter. These 5-bit registers contain scale values to compensate for the rCIC2 gain, external attenuator (if used) and the exponent offset (Expoff). If no external attenuator is used, both the rCIC2_QUIET and rCIC2_LOUD registers would contain the same value. A detailed explanation and equation for setting the attenuating scale register is given in the Scaling with Floating-Point or Gain-Ranging ADCs section.

Scaling with Fixed-Point ADCs

For fixed-point ADCs, the AD6634 exponent inputs EXP[2:0] are typically not used and should be tied low. The ADC outputs are tied directly to the AD6634 Inputs, MSB-justified. The ExpOff bits in 0x92 should be programmed to 0. Likewise, the Exponent Invert bit should be 0. Thus for fixed-point ADCs, the exponents are typically static and no input scaling is used in the AD6634.

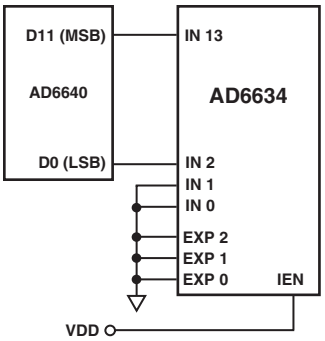


Figure 28. Typical Interconnection of the AD6640 Fixed Point ADC and the AD6634

Scaling with Floating-Point or Gain-Ranging ADCs

An example of the exponent control feature combines the AD6600 and the AD6634. The AD6600 is an 11-bit ADC with three bits of gain ranging. In effect, the 11-bit ADC provides the mantissa, and the three bits of relative signal strength indicator (RSSI) for the exponent. Only five of the eight available steps are used by the AD6600. See the AD6600 data sheet for additional details.

For gain-ranging ADCs such as the AD6600,

$$SCALED\_INPUT = IN \times 2^{-MOD(7-EXP+rCIC2,\ 32)},$$
$$EXPINV = 1, EXPWEIGHT = 0$$

where, *IN* is the value of IN[13:0], *EXP* is the value of EXP[2:0], and rCIC2 is the rCIC scale register value (0x92 Bits 9–5 and 4–0).

The RSSI output of the AD6600 numerically grows with increasing signal strength of the analog input (RSSI = 5 for a large signal, RSSI = 0 for a small signal). When the Exponent Invert Bit (ExpInv) is set to zero, the AD6634 will consider the smallest signal at the IN[13:0] to be the largest and as the EXP word increases, it shifts the data down internally (EXP = 5 will shift a 14-bit word right by five internal bits before passing the data to the rCIC2). In this example where ExpInv = 0, the AD6634 regards the largest signal possible on the AD6600 as the smallest signal. Thus, we can use the Exponent Invert Bit to make the AD6634 exponent agree with the AD6600 RSSI. By setting ExpInv = 1, this forces the AD6634 to shift the data up (left) for growing EXP instead of down. The exponent invert bit should always be set high for use with the AD6600.

The exponent offset is used to shift the data up. For example, Table I shows that with no rCIC2 scaling, 12 dB of range is lost when the ADC input is at the largest level. This is undesirable because it lowers the dynamic range and SNR of the system by reducing the signal of interest relative to the quantization noise floor.

To avoid this automatic attenuation of the full-scale ADC signal the ExpOff is used to move the largest signal (RSSI = 5) up to the point where there is no down shift. In other words, once the Exponent Invert bit has been set, the exponent offset should be adjusted so that mod(7–5 + ExpOff, 32) = 0. This is the case when exponent offset is set to 30 since mod(32, 32) = 0. Table II illustrates the use of ExpInv and ExpOff when used with the AD6600 ADC.

Table I. AD6600 Transfer Function with AD6634 ExpInv = 1, and No ExpOff

ADC Input Level	AD6600 RSSI[2:0]	AD6634 Data	Signal Reduction (dB)
Largest	101 (5)	/4 (>> 2)	–12
	100 (4)	/8 (>>3)	–18
	011 (3)	/16 (>> 4)	–24
	010 (2)	/32 (>> 5)	–30
	001 (1)	/64 (>> 6)	–36
Smallest	000 (0)	/128 (>> 7)	–42

(ExpInv = 1, rCIC2 Scale = 0)

Table II. AD6600 Transfer Function with AD6620 ExpInv = 1, and ExpOff = 6

ADC Input Level	AD6600 RSSI[2:0]	AD6634 Data	Signal Reduction (dB)
Largest	101 (5)	/1 (>> 0)	0
	100 (4)	/2 (>> 1)	–6
	011 (3)	/4 (>> 2)	–12
	010 (2)	/8 (>> 3)	–18
	001 (1)	/16 (>> 4)	–24
Smallest	000 (0)	/32 (>> 5)	–30

(ExpInv = 1, ExpOff = 30, ExpWeight = 0)

This flexibility in handling the exponent allows the AD6634 to interface with gain-ranging ADCs other than the AD6600. The Exponent Offset can be adjusted to allow up to seven RSSI(EXP) ranges to be used as opposed to the AD6600's five. It also allows the AD6634 to be tailored in a system that employs the AD6600 but does not utilize all of its signal range. For example, if only the first four RSSI ranges are expected to occur, the ExpOff could be adjusted to 29, which would then make RSSI = 4 correspond to the 0 dB point of the AD6634.

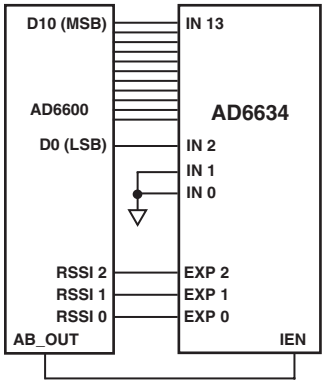


Figure 29. Typical Interconnection of the AD6600 Gain-Ranging ADC and the AD6634

NUMERICALLY CONTROLLED OSCILLATOR

Frequency Translation

This processing stage comprises a digital tuner consisting of two multipliers and a 32-bit complex NCO. Each channel of the AD6634 has an independent NCO. The NCO serves as a quadrature local oscillator capable of producing an NCO frequency between –CLK/2 and +CLK/2 with a resolution of CLK/2^{32} in the complex mode. The worst-case spurious signal from the NCO is better than –100 dBc for all output frequencies.

The NCO frequency value in registers 0x85 and 0x86 is interpreted as a 32-bit unsigned integer. The NCO frequency is calculated using the equation below.

$$NCO\_FREQ = 2^{32} \times MOD\left(\frac{f_{CHANNEL}}{CLK}\right)$$

where, *NCO_FREQ* is the 32-bit integer (registers 0x85 and 0x86), $f_{CHANNEL}$ is the desired channel frequency, and *CLK* is the AD6634 master clock rate or input data rate depending on the Input Enable mode used. See Input Enable Control section.

NCO Frequency Hold-Off Register
When the NCO Frequency registers are written, data is actually passed to a shadow register. Data may be moved to the main registers by one of two methods: when the channel comes out of sleep mode or when a SYNC Hop occurs. In either event a counter can be loaded with NCO Frequency Hold-Off register value. The 16-bit unsigned integer counter (0x84) starts counting down clocked by the master clock and when it reaches zero, the new frequency value in the shadow register is written to the NCO Frequency register. The NCO could also be set up to SYNC immediately, in which case the Frequency Hold-off counter is bypassed and new frequency values are updated immediately.

Phase Offset
The phase offset register (0x87) adds an offset to the phase accumulator of the NCO. This is a 16-bit register and is interpreted as a 16-bit unsigned integer. A 0x0000 in this register corresponds to a 0 Radian offset and a 0xFFFF corresponds to an offset of 2π $(1\text{-}1/(2^{16}))$ Radians. This register allows multiple NCOs to be synchronized to produce sine waves with a known and steady phase difference.

NCO Control Register
The NCO control register located at 0x88 is used to configure the features of the NCO. These are controlled on a per-channel basis, and are described below.

Bypass
The NCO in the front end of the AD6634 can be bypassed. Bypass mode is enabled by setting Bit 0 of 0x88 high. When it is bypassed, down conversion is not performed and the AD6634 channel functions simply as a real filter on complex data. This is useful for baseband sampling applications where the A input is connected to the I signal path within the filter and the B input is connected to the Q signal path. This may be desired if the digitized signal has already been converted to baseband in prior analog stages or by other digital preprocessing.

Phase Dither
The AD6634 provides a phase dither option for improving the spurious performance of the NCO. Phase dither is enabled by setting Bit 1. When phase dither is enabled by setting this bit high, spurs due to phase truncation in the NCO are randomized. The energy from these spurs is spread into the noise floor and spurious-free dynamic range is increased at the expense of very slight decreases in the SNR. The choice of whether phase dither is used in a system will ultimately be decided by the system goals. It should be employed if lower spurs are desired at the expense of a slightly raised noise floor. If a low noise floor is desired, and the higher spurs can be tolerated or filtered by subsequent stages, phase dither is not needed.

Amplitude Dither
Amplitude dither can also be used to improve spurious performance of the NCO. Amplitude dither is enabled by setting Bit 2. Amplitude dither improves performance by randomizing the amplitude quantization errors within the angular to Cartesian conversion of the NCO. This option may reduce spurs at the expense of a slightly raised noise floor. Amplitude dither and phase dither can be used together, separately, or not at all.

Clear Phase Accumulator on HOP
When Bit 3 is set, the NCO phase accumulator is cleared prior to a frequency hop. This ensures a consistent phase of the NCO on each hop. The NCO phase offset is unaffected by this setting and is still in effect. If phase continuous hopping is desired, this bit should be cleared and the last phase in the NCO phase register will be the initiating point for the new frequency.

Input Enable Control
There are four different modes of operation for the input enable. Each of the high speed input ports includes an IEN line. Any of the four filter channels can be programmed to take data from either of the two A or B input ports. (See WB Input Select section.) Along with data is the IEN(A,B) signal. Each filter channel can be configured to process the IEN signal in one of four modes. Three of the modes are associated with when data is processed based on a time division multiplexed data stream. The fourth mode is used in applications that employ time division duplex such as radar, sonar, ultrasound, and communications that involve TDD.

Mode 00: Blank on IEN Low
In this mode, data is blanked while the IEN line is low. During the period of time when the IEN line is high, new data is strobed on each rising edge of the input clock. When the IEN line is lowered, input data is replaced with zero values. During this period, the NCO continues to run such that when the IEN line is raised again, the NCO value will be at the value it would have been otherwise had the IEN line never been lowered. This mode has the effect of blanking the digital inputs when the IEN line is lowered. Back end processing (rCIC2, CIC5, and RCF) continues while the IEN line is high. This mode is useful for time division multiplexed applications.

Mode 01: Clock on IEN High
In this mode, data is clocked into the chip while the IEN line is high. During the period of time when the IEN line is high, new data is strobed on each rising edge of the input clock. When the IEN line is lowered, input data is no longer latched into the channel. Additionally, NCO advances are halted. However, back end processing (rCIC2, CIC5, and RCF) continues during this period. The primary use for this mode is to allow for a clock that is faster than the input sample data rate to allow more filter taps to be computed than would otherwise be possible. In Figure 30, input data is strobed only during the period of time that IEN is high despite the fact that the CLK continues to run at a rate four times faster than the data.

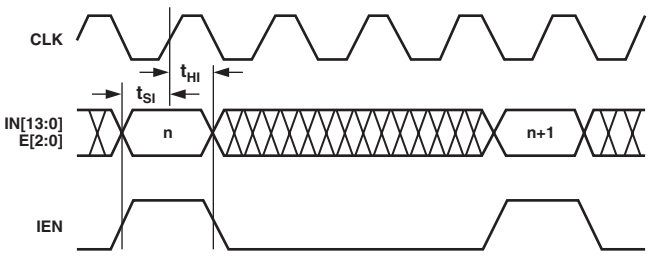


Figure 30. Fractional Rate Input Timing (4x CLK) in Mode 01

Mode 10: Clock on IEN Transition to High
In this mode, data is clocked into the chip only on the first clock edge after the rising transition of the IEN line. Although data is latched only on the first valid clock edge, the back end processing (rCIC2, CIC5, and RCF) continues on each available clock that may be present, similar to Mode 01. The NCO phase accumulator is incremented only once for each new input data sample and not once for each input clock.

Mode 11: Clock on IEN Transition to Low
In this mode, data is clocked into the chip only on the first clock edge after the falling transition of the IEN line. Although data is latched only on the first valid clock edge, the back end processing (rCIC2, CIC5, and RCF) continues one each available clock that may be present, similar to Mode 01. The NCO phase accumulator is incremented only once for each new input data sample and not once for each input clock.

WB Input Select
Bit 6 in this register controls which input port is selected for signal processing. If this bit is set high, input port B (INB, EXPB, and IENB) is connected to the selected filter channel. If this bit is cleared, input port A (INA, EXPA, and IENA) is connected to the selected filter channel.

Sync Select
Bits 7 and 8 of this register determine which external sync pin is associated with the selected channel. The AD6634 has four sync pins named SYNCA, SYNCB, SYNCC, and SYNCD. Any of these sync pins can be associated with any of the four receiver channels within the AD6634. Additionally, if only one sync signal is required for the system, all four receiver channels can reference the same sync pulse. Bit value 00 is channel A, 01 is channel B, 10 is channel C, and 11 is channel D.

SECOND ORDER rCIC FILTER

The rCIC2 filter is a second order cascaded resampling integrator comb filter. The resampler is implemented using a unique technique that does not require the use of a high speed clock, thus simplifying the design and saving power. The resampler allows for noninteger relationships between the master clock and the output data rate, which allows easier implementation of systems that are either multimode or require a master clock that is not a multiple of the data rate to be used.

Interpolation up to 512 and decimation up to 4096 is allowed in the rCIC2. The resampling factor for the rCIC2 (L) is a 9-bit integer. When combined with the decimation factor M, a 12-bit number, the total rate change can be any fraction in the form of:

$$R_{rCIC2} = \frac{L}{M}$$
$$R_{rCIC2} \le 1$$

The only constraint is that the ratio *L*/*M* must be less than or equal to one. This implies that the rCIC2 decimates by 1 or more.

Resampling is implemented by apparently increasing the input sample rate by the factor L, using zero stuffing for the new data samples. Following the resampler is a second order cascaded integrator comb filter. Filter characteristics are determined only by the fractional rate change (L/M).

The filter can process signals at the full rate of the input port, 80 MHz. The output rate of this stage is given by the equation:

$$f_{SAMP2} = \frac{L_{rCIC2}\ f_{SAMP}}{M_{rCIC2}}$$

Both L_{rCIC2} and M_{rCIC2} are unsigned integers. The interpolation rate (L_{rCIC2}) may be from 1 to 512 and the decimation (M_{rCIC2}) may be between 1 and 4096. The stage can be bypassed by setting the decimation to 1/1. The frequency response of the rCIC2 filter is given by the following equations.

$$H(z) = \frac{1}{2^{S_{rCIC2}} \times L_{rCIC2}} \times \left(\frac{1 - z\frac{M_{rCIC2}}{L_{rCIC2}}}{1 - z^1} \right)^2$$

$$H(f) = \frac{1}{2^{S_{rCIC2}} \times L_{rCIC2}} \times \left(\frac{\sin\left(\pi \frac{M_{rCIC2} \times f}{L_{rCIC2} \times f_{SAMP}}\right)}{\sin\left(\pi \frac{f}{f_{SAMP}}\right)} \right)^2$$

The gain and pass-band droop of the rCIC2 should be calculated by the equations above, as well as the filter transfer equations that follow. Excessive pass-band droop can be compensated for in the RCF stage by peaking the pass band by the inverse of the roll-off.

The scale factor, S_{rCIC2} is a programmable unsigned 5-bit between 0 and 31. This serves as an attenuator that can reduce the gain of the rCIC2 in 6 dB increments. For the best dynamic range, S_{rCIC2} should be set to the smallest value possible (i.e., lowest attenuation) without creating an overflow condition. This can be safely accomplished using the equation below, where *input_level* is the largest fraction of full scale possible at the input to the AD6634 (normally 1). The rCIC2 scale factor is always used whether or not the rCIC2 is bypassed.

Moreover, there are two scale registers (rCIC2_LOUD[4:0] Bits 4–0 in x92) and (rCIC2_QUIET[4:0] Bits 9–5 in x92) that are used in conjunction with the computed $S_{rCIC2,}$ which determines the overall rCIC2 scaling. The S_{rCIC2} value must be summed with the values in each respective scale registers and ExpOff to determine the scale value that must be placed in the rCIC2 scale register. This number must be less than 32 or the interpolation and decimation rates must be adjusted to validate this equation. The ceil function denotes the next whole integer and the floor function denotes the previous whole integer. For example, the ceil(4.5) is 5 while the floor(4.5) is 4.

$$scaled\_input = IN \times 2^{-MOD(Exp + rCIC2, 32)},\ ExpInv = 0$$
$$scaled\_input = IN \times 2^{-MOD(7 - Exp + rCIC2, 32)},\ ExpInv = 1$$

$$S_{rCIC2} = ceil\left[\log_2\left(M_{rCIC2} + floor\left(\frac{M_{rCIC2}}{L_{rCIC2}}\right) \times \left(2 \times M_{rCIC2} - L_{rCIC2} \times floor\left(\frac{M_{rCIC2}}{L_{rCIC2}} + 1\right)\right)\right)\right]$$

$$OL_{rCIC2} = \frac{\left(M_{rCIC2}{}^2\right)}{L_{rCIC2} \times 2^{S^{rCIC2}}} \times input\_level$$

Table III. SSB rCIC2 Alias Rejection Table (f_{SAMP} = 1) Bandwidth Shown in Percentage of f_{SAMP}

M_{rCIC2}/L_{rCIC2}	–50 dB	–60 dB	–70 dB	–80 dB	–90 dB	–100 dB
2	1.79	1.007	0.566	0.318	0.179	0.101
3	1.508	0.858	0.486	0.274	0.155	0.087
4	1.217	0.696	0.395	0.223	0.126	0.071
5	1.006	0.577	0.328	0.186	0.105	0.059
6	0.853	0.49	0.279	0.158	0.089	0.05
7	0.739	0.425	0.242	0.137	0.077	0.044
8	0.651	0.374	0.213	0.121	0.068	0.038
9	0.581	0.334	0.19	0.108	0.061	0.034
10	0.525	0.302	0.172	0.097	0.055	0.031
11	0.478	0.275	0.157	0.089	0.05	0.028
12	0.439	0.253	0.144	0.082	0.046	0.026
13	0.406	0.234	0.133	0.075	0.043	0.024
14	0.378	0.217	0.124	0.07	0.04	0.022
15	0.353	0.203	0.116	0.066	0.037	0.021
16	0.331	0.19	0.109	0.061	0.035	0.02

where, *IN* is the value of IN[13:0], *EXP* is the value of EXP[2:0], and *rCIC2* is the value of the 0x92 (rCIC2_QUIET[4:0], and rCIC2_LOUD[4:0]) scale register.

rCIC2 Rejection

Table III illustrates the amount of bandwidth in percent of the data rate into the rCIC2 stage. The data in this table may be scaled to any other allowable sample rate up to 80 MHz in Single Channel Mode or 40 MHz in Diversity Channel Mode. Table III can be used as a tool to decide how to distribute the decimation between rCIC2, CIC5, and the RCF.

Example Calculations

Goal: Implement a filter with an Input Sample Rate of 10 MHz requiring 100 dB of Alias Rejection for a ±7 kHz pass band.

Solution: First determine the percentage of the sample rate that is represented by the pass band.

$$BW_{FRACTION} = 100 \times \frac{7\ kHz}{10\ MHz} = 0.07$$

Find the –100 dB column on the right of Table III and look down this column for a value greater than or equal to the pass-band percentage of the clock rate. Then look across to the extreme left column and find the corresponding rate change factor (M_{rCIC2}/L_{rCIC2}). Referring to the table, notice that for a M_{rCIC2}/L_{rCIC2} of 4, the frequency having –100 dB of alias rejection is 0.071 percent, which is slightly greater than the 0.07 percent calculated. Therefore, for this example, the maximum bound on rCIC2 rate change is 4. A higher chosen M_{rCIC2}/L_{rCIC2} means less alias rejection than the 100 dB required.

An M_{rCIC2}/L_{rCIC2} of less than 4 would still yield the required rejection; however, the power consumption can be minimized by decimating as much as possible in this rCIC2 stage. Decimation in rCIC2 lowers the data rate, and thus reduces power consumed in subsequent stages. It should also be noted that there is more than one way to get the decimation by 4. A decimation of 4 is the same as an L/M ratio of 0.25. Thus any integer combination of L/M that yields 0.25 will work (1/4, 2/8, or 4/16). However, for the best dynamic range, the simplest ratio should be used. For example, 1/4 gives better performance than 4/16.

Decimation and Interpolation Registers

rCIC2 decimation values are stored in register 0x90. This is a 12-bit register and contains the decimation portion less 1. The interpolation portion is stored in register 0x91. This 9-bit value holds the interpolation less one.

rCIC2 Scale

Register 0x92 contains the scaling information for this section of the circuit. The primary function is to store the scale value computed in the sections above.

Bits 4–0 (rCIC2_LOUD[4:0]) of this register are used to contain the scaling factor for the rCIC2 during conditions of strong signals. These five bits represent the rCIC2 scalar calculated above plus any external signal scaling with an attenuator.

Bits 9–5 (rCIC2_QUIET[4:0]) of this register are used to contain the scaling factor for the rCIC2 during conditions of weak signals. In this register, an external attenuator would not be used and is not included. Only the value computed above is stored in these bits.

Bit 10 of this register is used to indicate the value of the external exponent. If this bit is set LOW, then each external exponent represents 6 dB per step as in the AD6600. If this bit is set to HIGH, each exponent represents a 12 dB step.

Bit 11 of this register is used to invert the external exponent before internal calculation. This bit should be set HIGH for gain ranging ADCs that use an increasing exponent to represent an increasing signal level. This bit should be set LOW for gain ranging ADCs that use a decreasing exponent for representing an increasing signal level.

In applications that do not require the features of the rCIC2, it may be by setting the L/M ratio to 1/1. This effectively bypasses all circuitry of the rCIC2 except the scaling that is still effectual.

FIFTH ORDER CIC FILTER

The third signal processing stage, CIC5, implements a sharper fixed-coefficient, decimating filter than rCIC2. The input rate to this filter is f_{SAMP2}. The maximum input rate is given by the equation below. N_{CH} equals 2 for diversity channel real input mode; otherwise N_{CH} equals 1. In order to satisfy this equation, M_{rCIC2} can be increased, N_{CH} can be reduced, or f_{CLK} can be increased (reference fractional rate input timing described in the Input Timing section).

$$f_{SAMP2} \le \frac{f_{CLK}}{N_{CH}}$$

The decimation ratio, M_{CIC5}, may be programmed from 2 to 32 (all integer values). The frequency response of the filter is given by the following equations. The gain and pass-band droop of CIC5 should be calculated by these equations. Both parameters may be compensated for in the RCF stage.

$$H(z) = \frac{1}{2^{S_{CIC5}+5}}\left(\frac{1-z^{-M_{CIC5}}}{1-z^{-1}}\right)^5$$

$$H(f) = \frac{1}{2^{S_{CIC5}+5}}\left(\frac{\sin\left(\pi\frac{M_{CIC5}\times f}{f_{SAMP2}}\right)}{\sin\left(\pi\frac{f}{f_{SAMP2}}\right)}\right)^5$$

The scale factor, S_{CIC5} is a programmable unsigned integer between 0 and 20. It serves to control the attenuation of the data into the CIC5 stage in 6 dB increments. For the best dynamic range, S_{CIC5} should be set to the smallest value possible (lowest attenuation) without creating an overflow condition. This can be safely accomplished using the following equation, where OL_{rCIC2} is the largest fraction of full scale possible at the input to this filter stage. This value is output from the rCIC2 stage then pipelined into the CIC5.

$$S_{CIC5} = ceil\left(\log_2\left({M_{CIC5}}^5 \times OL_{rCIC2}\right)\right) - 5$$

$$OL_{rCIC2} = \frac{\left({M_{CIC5}}^5\right)}{2^{S_{CIC5}+5}} \times OL_{rCIC2}$$

The output rate of this stage is given by the equation below.

$$f_{SAMP5} = \frac{f_{SAMP2}}{M_{CIC5}}$$

CIC5 Rejection

Table IV illustrates the amount of bandwidth in percentage of the clock rate that can be protected with various decimation rates and alias rejection specifications. The maximum input rate into the CIC5 is 80 MHz when the rCIC2 decimates by 1. As in the Table III, these are the one-half bandwidth characteristics of the CIC5. Notice that the CIC5 stage can protect a much wider band to any given rejection.

This table helps to calculate an upper bound on decimation, M_{CIC5}, given the desired filter characteristics.

Table IV. SSB CIC5 Alias Rejection Table (f_{SAMP2} = 1)

MCIC5	–50 dB	–60 dB	–70 dB	–80 dB	–90 dB	–100 dB
2	10.227	8.078	6.393	5.066	4.008	3.183
3	7.924	6.367	5.11	4.107	3.297	2.642
4	6.213	5.022	4.057	3.271	2.636	2.121
5	5.068	4.107	3.326	2.687	2.17	1.748
6	4.267	3.463	2.808	2.27	1.836	1.48
7	3.68	2.989	2.425	1.962	1.588	1.281
8	3.233	2.627	2.133	1.726	1.397	1.128
9	2.881	2.342	1.902	1.54	1.247	1.007
10	2.598	2.113	1.716	1.39	1.125	0.909
11	2.365	1.924	1.563	1.266	1.025	0.828
12	2.17	1.765	1.435	1.162	0.941	0.76
13	2.005	1.631	1.326	1.074	0.87	0.703
14	1.863	1.516	1.232	0.998	0.809	0.653
15	1.74	1.416	1.151	0.932	0.755	0.61
16	1.632	1.328	1.079	0.874	0.708	0.572
17	1.536	1.25	1.016	0.823	0.667	0.539
18	1.451	1.181	0.96	0.778	0.63	0.509
19	1.375	1.119	0.91	0.737	0.597	0.483
20	1.307	1.064	0.865	0.701	0.568	0.459
21	1.245	1.013	0.824	0.667	0.541	0.437
22	1.188	0.967	0.786	0.637	0.516	0.417
23	1.137	0.925	0.752	0.61	0.494	0.399
24	1.09	0.887	0.721	0.584	0.474	0.383
25	1.046	0.852	0.692	0.561	0.455	0.367
26	1.006	0.819	0.666	0.54	0.437	0.353
27	0.969	0.789	0.641	0.52	0.421	0.34
28	0.934	0.761	0.618	0.501	0.406	0.328
29	0.902	0.734	0.597	0.484	0.392	0.317
30	0.872	0.71	0.577	0.468	0.379	0.306
31	0.844	0.687	0.559	0.453	0.367	0.297
32	0.818	0.666	0.541	0.439	0.355	0.287

RAM COEFFICIENT FILTER

The final signal processing stage is a sum-of-products decimating filter with programmable coefficients. A simplified block diagram is shown in Figure 31. The data memories I-RAM and Q-RAM store the 160 most recent complex samples from the previous filter stage with 20-bit resolution. The coefficient memory, CMEM, stores up to 256 coefficients with 20-bit resolution. On every CLK cycle, one tap for I and one tap for Q are calculated using the same coefficients. The RCF output consists of 24-bit data bits.

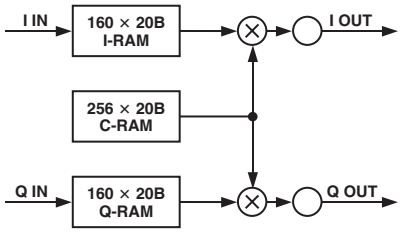


Figure 31. RAM Coefficient Filter Block Diagram

RCF Decimation Register

Each RCF channel can be used to decimate the data rate. The decimation register is an 8-bit register and can decimate from 1 to 256. The RCF decimation is stored in 0xA0 in the form of M_{RCF}–1. The input rate to the RCF is f_{SAMP5}.

RCF Decimation Phase

The RCF decimation phase can be used to synchronize multiple filters within a chip. This is useful when using multiple channels within the AD6634 to implement the polyphase filter, allowing the resources of several filters to be paralleled. In such an application, two RCF filters would be processing the same data from the CIC5. However, each filter will be delayed by one-half the decimation rate, thus creating a 180 degree phase difference between the two halves. The AD6634 filter channel uses the value stored in this register to preload the RCF counter. Therefore, instead of starting from 0, the counter is loaded with this value, thus creating an offset in the processing that should be equivalent to the required processing delay. This data is stored in 0xA1 as an 8-bit number.

RCF Filter Length

The maximum number of taps this filter can calculate, N_{taps}, is given by the equation below. The value N_{taps}–1 is written to the channel register within the AD6634 at address 0xA2.

$$N_{taps} \le min\left(\frac{f_{CLK} \times M_{RCF}}{f_{SAMP\ 5}}, 160\right)$$

The RCF coefficients are located in addresses 0x00 to 0x7F and are interpreted as 20-bit two's complement numbers. When writing the coefficient RAM, the lower addresses will be multiplied by relatively older data from the CIC5 and the higher coefficient addresses will be multiplied by relatively newer data from the CIC5. The coefficients need not be symmetric and the coefficient length, N_{taps}, may be even or odd. If the coefficients are symmetric, then both sides of the impulse response must be written into the coefficient RAM.

Although the base memory for coefficients is only 128 words long, the actual length is 256 words long. There are two pages, each of 128 words long. The page is selected by Bit 8 of 0xA4. Although this data must be written in pages, the internal core handles filters that exceed the length of 128 taps. Therefore, the full length of the data RAM may be used as the filter length (160 taps).

The RCF stores the data from the CIC5 into a 160 × 40 RAM. 160 × 20 is assigned to I data and 160 × 20 is assigned to Q data. The RCF uses the RAM as a circular buffer, so it is difficult to know in which address a particular data element is stored.

When the RCF is triggered to calculate a filter output, it starts by multiplying the oldest value in the data RAM by the first coefficient, which is pointed to by the RCF Coefficient Offset Register (0xA3). This value is accumulated with the products of newer data-words multiplied by the subsequent locations in the coefficient RAM until the coefficient address $RCF_{OFF} + N_{taps}$–1 is reached.

Table V. Three-Tap Filter

Coefficient Address	Impulse Response	Data
0	h(0)	N(0) oldest
1	h(1)	N(1)
2 = (N_{taps}–1)	h(2)	N(2) newest

The RCF Coefficient Offset register can be used for two purposes. The main purpose of this register is to allow for multiple filters to be loaded into memory and selected simply by changing the offset as a pointer for rapid filter changes. The other use of this register is to form part of the symbol timing adjustment. If the desired filter length is padded with zeros on the ends, the starting point can be adjusted to form slight delays in when the filter is computed with reference to the high speed clock. This allows for vernier adjustment of the symbol timing. Course adjustments can be made with the RCF Decimation Phase.

The output rate of this filter is determined by the output rate of the CIC5 stage and M_{RCF}.

$$f_{SAMPR} = \frac{f_{SAMP5}}{M_{RCF}}$$

RCF Output Scale Factor and Control Register

Register 0xA4 is a compound register and is used to configure several aspects of the RCF register. Bits 3–0 are used to set the scale of the fixed-point output mode. This scale value may also be used to set the floating-point outputs in conjunction with Bit 6 of this register.

Bits 4 and 5 determine the output mode. Mode 00 sets up the chip in fixed-point mode. The number of bits is determined by the parallel or link port configuration.

Mode 01 selects floating-point mode 8 + 4. In this mode, an 8-bit mantissa is followed by a 4-bit exponent. In mode 1x (x is don't care), the mode is 12 + 4, or 12-bit mantissa and 4-bit exponent.

Table VI. Output Mode Formats

Floating Point 12 + 4	1x
Floating Point 8 + 4	01
Fixed Point	00

Normally, the AD6634 will determine the exponent value that optimizes numerical accuracy. However, if Bit 6 is set, the value stored in Bits 3–0 is used to scale the output. This ensures consistent scaling and accuracy during conditions that may warrant predictable output ranges. If Bits 3–0 are represented by RCF Scale, the scaling factor in dB is given by:

$$Scaling\ Factor = \left(RCF\ Scale - 3\right) \times 20 \log_{10}\left(2\right) dB$$

For *RCF Scale* of 0, *Scaling Factor* is equal to –18.06 dB, and for maximum *RCF Scale* of 15, *Scaling Factor* is equal to 72.25 dB.

If Bit 7 is set, the same exponent will be used for both the real and imaginary (I and Q) outputs. The exponent used will be the one that prevents numeric overflow at the expense of small signal accuracy. However, this is seldom a problem as small numbers would represent 0 regardless of the exponent used.

Bit 8 is the RCF bank select bit used to program the register. When this bit is 0, the lowest block of 128 is selected (taps 0 through 127). When high, the highest block is selected (taps 128 through 255). It should be noted that while the chip is computing filters, tap 127 is adjacent to 128 and there are no paging issues.

Bit 9 selects where the input to each RCF originates. If Bit 9 is clear, the RCF input comes from the CIC5 normally associated with the RCF. If, however, the bit is set, the input comes from CIC5 channel 1. The only exception is channel 1, which uses the output of CIC5 channel 0 as its alternate. Using this feature, each RCF can operate on its own channel data or be paired with the RCF of channel 1. The RCF of channel 1 can also be paired with channel 0. This control bit is used with polyphase distributed filtering.

If Bit 10 is clear, the AD6634 channel operates in normal mode. However, if Bit 10 is set, the RCF is bypassed to Channel BIST. See the BIST (Built-In Self-Test) section for more details.

INTERPOLATING HALF-BAND FILTERS

The AD6634 has two interpolating half-band finite impulse response filters that immediately precede the two digital AGCs and follow the four RCF channel outputs. Each interpolating half-band takes 16-bit I and 16-bit Q data from the preceding RCF and outputs 16-bit I and 16-bit Q to the AGC. The half-band and AGC operate independently of each other, so the AGC can be bypassed, in which case the output of the half-band is sent directly to the output data port. The half-bands also operate independently of each other—either one can be enabled or disabled. The control register for half-band A is at address 0x08 and for half-band B, address 0x09.

Half-band filters also perform the function of interleaving data from various RCF channel outputs prior to the actual function of interpolation. This interleaving of data is allowed even when the actual function of Half-band filter is bypassed. This feature allows for the usage of multiple channels (implementing a polyphase filter) on the AD6634 to process a single carrier. Either RCF phase decimation or start hold-off counter for the channels is used to appropriately phase the channels. For example, if two channels of AD6634 are used to process one CDMA2000 carrier, RCF filters for both the channels should be 180° out of phase. This can be done using RCF phase decimation or an appropriate start hold-off counter followed by appropriate NCO phase offsets.

Half-band A can listen to all four channels: 0, 1, 2, and 3; channel 0 and 1; or only channel 0. Half-band B can listen to channels 2 and 3, or only channel 2. Each half-band interleaves the channels specified in its control register and interpolates by 2 on the combined data from those channels. For one channel running at twice the chip rate, the half-band can be used to output channel data at 43 the chip rate.

With respect to the chip rate, the frequency response of the interpolating half-band FIR is shown in Figure 32.

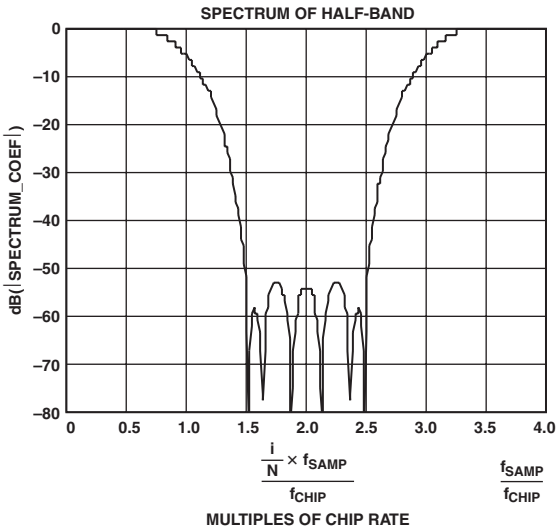


Figure 32. Interpolating Half-Band Frequency Response

The SNR of the interpolating half-band is around –149.6 dB. The highest error spurs due to fixed-point arithmetic are around –172.9 dB. The coefficients of the 13-tap interpolating half-band FIR are given in the Table VII.

Table VII. Half-Band Coefficients

0
14
0
–66
0
309
512
309
0
–66
0
14
0

AUTOMATIC GAIN CONTROL

The AD6634 is equipped with two independent automatic gain control (AGC) loops for direct interface with a RAKE receiver. Each AGC circuit has 96 dB of range. It is important that the decimating filters of the AD6634 preceding the AGC reject undesired signals, so that each AGC loop is only operating on the carrier of interest and carriers at other frequencies do not affect the ranging of the loop.

The AGC compresses the 23-bit complex output from the interpolating half-band filter into a programmable word size of 4–8, 10, 12, or 16 bits. Since the small signals from the lower bits are pushed into higher bits by adding gain, the clipping of the lower bits does not compromise the SNR of the signal of interest. The AGC maintains a constant mean power on the output despite the level of the signal of interest, allowing operation in environments where the dynamic range of the signal exceeds the dynamic range of the output resolution.

The AGC and the interpolation filters are not tied together and any one, or both of them, can be selected without the other. The AGC section can be bypassed, if desired, by setting Bit 0 of the AGC control word. When bypassed, the I/Q data is still clipped to a desired number of bits and a constant gain can be provided through the AGC Gain multiplier.

There are three sources of error introduced by the AGC function: underflow, overflow, and modulation. Underflow is caused by truncation of bits below the output range. Overflow is caused by clipping errors when the output signal exceeds the output range. Modulation error occurs when the output gain varies during the reception of data.

The desired signal level should be set based on the probability density function of the signal so that the errors due to underflow and overflow are balanced. The gain and damping values of the loop filter should be set so that the AGC is fast enough to track long-term amplitude variations of the signal that might cause excessive underflow or overflow, but slow enough to avoid excessive loss of amplitude information due to the modulation of the signal.

The AGC Loop

The AGC loop is implemented using a log-linear architecture. It contains four basic operations: power calculation, error calculation, loop filtering, and gain multiplication.

The AGC can be configured to operate in one of two modes: Desired Signal level mode or Desired Clipping level mode as set by Bit 4 of AGC control word (0x0A, 0x12). The AGC adjusts the gain of the incoming data according to how far it is from a given desired signal level or desired clipping level, depending on the mode of operation selected. Two data paths to the AGC loop are provided: one before the clipping circuitry and one after the clipping circuitry, as shown in Figure 33. For Desired Signal level mode, only the I/Q path from before the clipping is used. For Desired Clipping level mode, the difference of the I/Q signals from before and after the clipping circuitry is used.

Desired Signal Level Mode

In this mode of operation, the AGC strives to maintain the output signal at a programmable set level. This mode of operation is selected by putting a value of zero in Bit 4 of AGC control word (0x0A, 0x12). First, the loop finds the square (or power) of the incoming complex data signal by squaring I and Q and adding them. This operation is implemented in exponential domain using 2^x (power of 2).

The AGC loop has an average and decimate block. This average and decimate operation takes place on power samples and before the square root operation. This block can be programmed to average 1–16384 power samples and the decimate section can be programmed to update the AGC once every 1–4096 samples. The limitation on the averaging operation is that the number of averaged power samples should be a multiple of the decimation value (1×, 2×, 3×, or 4× times).

The averaging and decimation effectively means the AGC can operate over averaged power of 1–16384 output samples. The choice of updating the AGC once every 1–4096 samples and operating on average power facilitates the implementation of loop filter with slow time constants, where the AGC error converges slowly and makes infrequent gain adjustments. It would also be useful in scenarios where the user wants to keep the gain scaling constant over a frame of data (or a stream of symbols).

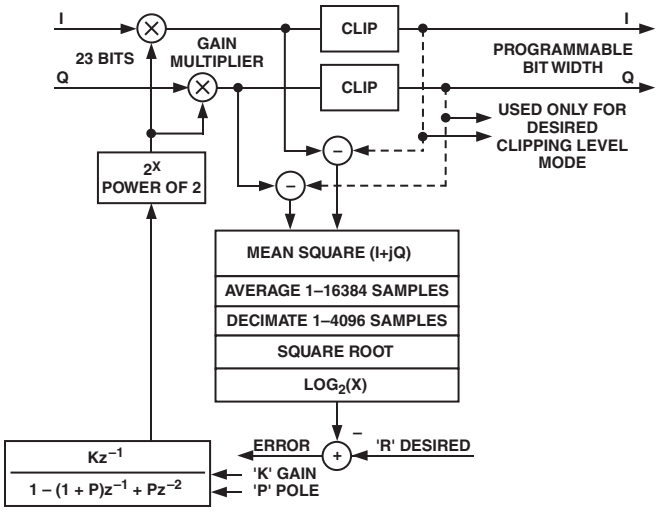


Figure 33. Block Diagram of the AGC

Due to the limitation on the number of average samples to be a multiple of decimation value, only the multiple number 1, 2, 3, or 4 is programmed. This number is programmed in Bits 1,0 of 0x10 and 0x18 registers. These averaged samples are then decimated with decimation ratios programmable from 1 to 4096. This decimation ratio is defined in 12-bit registers 0x11 and 0x19.

The average and decimate operations are tied together and implemented using a first-order CIC filter and some FIFO registers. There is a gain and bit growth associated with CIC filters and these depend on the decimation ratio. To compensate for the gain associated with these operations, attenuation scaling is provided before the CIC filter.

This scaling operation accounts for the division associated with averaging operation as well as the traditional bit growth in CIC filters. Since this scaling is implemented as a bit shift operation, only coarse scaling is possible. Fine scale is implemented as an offset in the request level explained later. The attenuation scaling S_{CIC} is programmable from 0 to 14 using four bits of 0x10 and 0x18 registers and is given by:

$$S_{CIC} = ceil\left[\log_2\left(M_{CIC} \times N_{AVG}\right)\right]$$

where, M_{CIC} is the decimation ratio (1–4096) and N_{AVG} is the number of averaged samples programmed as a multiple of decimation ratio (1, 2, 3, or 4).

For example, if a decimation ratio M_{CIC} is 1000 and N_{AVG} is selected to be 3 (decimation of 1000 and averaging of 3000 samples), the actual gain due to averaging and decimation is 3000 or 69.54 dB (= $\log_2(3000)$). Since attenuation is implemented as a bit shift operation, only multiples of 6.02 dB attenuations are possible. S_{CIC} in this case is 12, corresponding to 72.24 dB. This way, S_{CIC} scaling always attenuates more than sufficient to compensate for the gain changes in average and decimate sections and thus prevents overflows in the AGC loop. It is also evident that the CIC scaling is inducing a gain error (difference between gain due to CIC and attenuation provided) of up to 6.02 dB. This error should be compensated for in the request signal level as explained below.

Logarithm to the base 2 is applied to the output from the average and decimate section. These decimated power samples (in logarithmic domain) are converted to rms signal samples by applying a square root. This square root is implemented using a simple shift

operation. The rms samples so obtained are subtracted from the request signal level, R, specified in registers (0x0B, 0x14), leaving an error term to be processed by the loop filter, G(z).

The user sets this programmable request signal level, R, according to the output signal level desired. The request signal level, R, is programmable from –0 dB to –23.99 dB in steps of 0.094 dB. The request signal level should also compensate for error, if any, due to the CIC scaling as explained previously. Therefore, the request signal level is offset by the amount of error induced in CIC, given by,

$$Offset = 20 \times \log_{10}\left(M_{CIC} \times N_{AVG}\right) - S_{CIC} \times 6.02$$

where the offset is in dB. Continuing with the previous example this offset is given by, *Offset* = 72.24 – 69.54 = 2.7 dB. The request signal level is given by,

$$R = ceil\left[\frac{\left(DSL - offset\right)}{0.094}\right] \times 0.094$$

where *R* is the request signal level and *DSL* (Desired Signal Level) is the output signal level that the user desires. In the previous example if the desired signal level is –13.8 dB, the request level, *R*, is programmed to be –16.54 dB.

The AGC provides a programmable second order loop filter. The programmable parameters gain, K, and pole, P, completely define the loop filter characteristics. The error term after subtracting the request signal level is processed by the loop filter, G(z). The open loop poles of the second order loop filter are '1' and, P, respectively. The loop filter parameters, pole, P, and gain, K, allow adjustment of the filter time constant that determines the window for calculating the peak-to-average ratio.

The open loop transfer function for the filter including the gain parameter is given below.

$$G(z) = \frac{Kz^{-1}}{1 - (1+P)z^{-1} + Pz^{-2}}$$

If the AGC is properly configured (in terms of offset in request level), there are no gains except the filter gain *K*. Under these circumstances, a closed loop expression for the AGC loop is possible and is given by,

$$G_{CLOSED}(z) = \frac{G(z)}{1+G(z)} = \frac{Kz^{-1}}{1 + (K-1-P)z^{-1} + Pz^{-2}}$$

The gain parameter *K* and pole *P* are programmable through registers (0x0E and 0x0F, respectively, for AGC channel A and B) from 0 to 0.996 in steps of 0.0039 using 8-bit representation. Though the user defines the open loop pole *P* and gain *K*, they will directly impact the placement of the closed loop poles and filter characteristics. These closed loop poles P_1, P_2, are the roots of the denominator of the above closed loop transfer function and are given by,

$$P_1, P_2 = \frac{(1+P-K) + \sqrt{(1+P-K)^2 - 4P}}{2}$$

Typically, the AGC loop performance is defined in terms of its time constant or settling time. In such a case the closed loop poles should be set to meet the time constants required by the AGC loop. The following relation between time constant and closed loop poles can be used for this purpose.

$$P_{1,2} = exp\left[\frac{M_{CIC}}{SAMPLE\ RATE \times \tau_{1,2}}\right]$$

where $\tau_{1,2}$ are the time constants corresponding to the poles $P_{1,2}$. The time constants can also be derived from settling times as given below,

$$\frac{2\%\ Setting\ Time}{4}\ or\ \frac{5\%\ Setting\ Time}{3}$$

M_{CIC} (CIC decimation is from 1 to 4096), and either the settling time or time constant should be chosen by the user. The sample rate is the combined sample rate of all the interleaved channels coming into the AGC/half-band interpolated filters. If two channels are being used to process one carrier of UMTS at 2× chip rate, each channel works at 3.84 MHz and the combined sample rate coming into the half-band interpolated filters is 7.68 MSPS. This rate should be used in the calculation of poles in the above equation, if half-band interpolating filters are bypassed.

The loop filter output corresponds to the signal gain that is updated by the AGC. Since all computation in the loop filter is done in logarithmic domain (to the base 2) of the samples, the signal gain is generated using the exponent (power of 2) of the loop filter output.

The gain multiplier gives the product of the signal gain with both the I and Q data entering the AGC section. This signal gain is applied as a coarse 4-bit scaling and then a fine scale 8-bit multiplier. Thus the applied signal gain is between 0 dB and 96.296 dB in steps of 0.024 dB. Initial value for signal gain is programmable using the registers 0x0D and 0x15 for AGC A and AGC B, respectively.

The products of the gain multiplier, the AGC scaled outputs, have 19-bit representation. These are in turn used as I and Q for calculating the power and AGC error and loop filtered to produce signal gain for next set of samples. These AGC scaled outputs can be programmed to have 4, 5, 6, 7, 8, 10, 12, or 16-bit widths using the AGC control word (0x0A, 0x12). The AGC scaled outputs are truncated to required bit widths using the clipping circuitry as shown in the block diagram.

Open Loop Gain Setting

If filter gain K occupies only one LSB, or 0.0039, during the multiplication with error term, errors of up to 6.02 dB could be truncated. This truncation is due to the lower bit widths available in the AGC loop. If filter gain K were the maximum value, truncated errors would be a less than 0.094 dB (equivalent to 1 LSB of error term representation). Generally, a small filter gain is used to achieve a large time constant loop (or slow loops), but in this case it would cause large errors to go undetected. Due to this peculiarity, the designers recommend that if a user wants slow AGC loops that they use fairly high values for filter gain K and then use CIC decimation to achieve a slow loop. In this way, the AGC loop will make large infrequent gain changes compared to small and frequent gain changes as in the case of normal small gain loop filter. However, though the AGC loop makes large infrequent gain changes, a slow time constant is still achieved and there is lesser truncation of errors.

Average Samples Setting

Though it is complicated to express the exact effect of the number of averaging samples, thinking intuitively it has a smoothing effect on the way the AGC loop attacks a sudden increase or a

spike in the signal level. If averaging of four samples is used, the AGC will attack a sudden increase in signal level more slowly compared to no averaging. The same would apply to the manner in which the AGC would attack a sudden decrease in the signal level.

Desired Clipping Level Mode
As noted previously, each AGC can be configured so that the loop locks on to a desired clipping level or a desired signal level. The Desired Clipping Level mode can be selected by setting Bit 4 of individual AGC control words (0x0A, 0x12). For signals that tend to exceed the bounds of the peak-to-average ratio, the desired clipping level option allows a way to keep from truncating those signals and still provide an AGC that attacks quickly and settles to the desired output level. The signal path for this mode of operation is shown with broken arrows in the Functional Block Diagram and the operation is similar to the desired signal level mode.

First, the data from the gain multiplier is truncated to a lower resolution (4, 5, 6, 7, 8, 10, 12, or 16 bits) as set by the AGC control word. An error term (both I and Q) is generated that is the difference between the signals before and after truncation. This term is passed to the complex squared magnitude block, for averaging and decimating the update samples and taking their square root to find rms samples as in desired signal level mode. In place of the request desired signal level, a desired clipping level is subtracted, leaving an error term to be processed by the second order loop filter. The rest of the loop operates the same way as the desired signal level mode. This way the truncation error is calculated and the AGC loop operates to maintain a constant truncation error level.

Apart from Bit 4 of the AGC control words, the only register setting changes compared to the Desired Signal level mode is that the Desired Clipping level is stored in the AGC Desired Level registers (0x0C, 0x15) instead of the Request Signal level (as in Desired Signal Level mode).

Synchronization
In scenarios where AGC output is connected to a RAKE receiver, the RAKE receiver can synchronize the average and update section to update the average power for AGC error calculation and loop filtering. This external sync signal synchronizes the AGC changes to RAKE receiver and makes sure that the AGC gain word does not change over a symbol period and thus more accurate estimation. Such synchronization can be accomplished by setting the appropriate bits of the AGC control register.

When the channel comes out of sleep, it loads the AGC hold-off counter value and starts counting down, clocked by the Master clock. When this counter reaches zero, the CIC filter of the AGC starts decimation and updates the AGC loop filter based on the CIC decimation value set.

Further, whenever the user wants to synchronize the start of decimation for a new update sample, an appropriate hold-off value can be set in AGC hold-off counter (0x0B, 0x13) and the Sync now bit (Bit 3) in the AGC control word is set. Upon setting this bit, the hold-off counter value is counted down and a CIC decimated value is updated on the count of zero.

Along with updating a new value, the CIC filter accumulator can be reset if Init on Sync bit (Bit 2) of the AGC control word is set. Each sync will initiate a new sync signal unless first sync only bit (Bit 1) of the AGC control word is set. If this bit is not set, again the hold-off counter is loaded with the value in the hold-off register to count down and repeat the same process. These additional features make the AGC synchronization more flexible and applicable to varied circumstances.

Addresses 0x0A–0x11 have been reserved for configuring AGC A and addresses 0x12–0x19 have been reserved for configuring AGC B. The register specifications are detailed in the Memory Map for Output Port Control Registers section.

USER CONFIGURABLE BUILT-IN SELF-TEST (BIST)

The AD6634 includes two built-in test features to test the integrity of each channel. The first is a RAM BIST (Built-In Self-Test) and is intended to test the integrity of the high speed random access memory within the AD6634. The second is Channel BIST, which is designed to test the integrity of the main signal paths of the AD6634. Each BIST function is independent of the other, meaning that each channel can be tested independently at the same time.

RAM BIST
The RAM BIST can be used to validate functionality of the on-chip RAM. This feature provides a simple pass/fail test, which will give confidence that the channel RAM is operational. The following steps should be followed to perform this test.

1. The channels to be tested should be put into Sleep mode via the external address register 0x011.
2. The RAM BIST Enable bit in the RCF register 0xA8 should be set high.
3. Wait 1600 clock cycles.
4. Register 0xA8 should be read back. If Bit 0 is high, the test is not yet complete. If Bit 0 is low, the test is complete and Bits 1 and 2 indicate the condition of the internal RAM. If Bit 1 is high, CMEM is bad. If Bit 2 is high, DMEM is bad.

Table VIII. BIST Register 0xA8

XA8	Coefficient MEM	Data MEM
XX1	Test Incomplete	Test Incomplete
000	Pass	Pass
010	Fail	Pass
100	Pass	Fail
110	Fail	Fail

Channel BIST
The Channel BIST is a thorough test of the selected AD6634 signal path. With this test mode, it is possible to use externally supplied vectors or an internal pseudo-random generator. An error signature register in the RCF monitors the output data of the channel and is used to determine if the proper data exits the RCF. If errors are detected, each internal block may be bypassed and another test can be run to debug the fault. The I and Q paths are tested independently. The following steps should be taken to perform this test.

1. The channels to be tested should be configured as required for the application setting the decimation rates, scalars, and RCF coefficients.
2. The channels should remain in the Sleep mode.
3. The Start Hold-Off counter of the channels to be tested should be set to 1.
4. Memory location 0xA5 and 0xA6 should be set to 0.

5. The Channel BIST located at 0xA7 should be enabled by setting Bits 19–0 to the number of RCF outputs to observe.
6. Bit 4 of external address register 5 should be set high to start the soft sync.
7. Set the SYNC bits high for the channels to be tested.
8. Bit 6 must be set to 0 to allow the user to provide test vectors. The internal pseudo-random number generator may also be used to generate an input sequence by setting Bit 7 high.
9. An internal full scale sine wave can be inserted when Bit 6 is set to 1 and Bit 7 is cleared.
10. When the SOFT_SYNC is addressed, the selected channels will come out of the sleep mode and processing will occur.
11. If the user is providing external vectors, the chip may be brought out of Sleep mode by one of the other methods provided that either of the IEN inputs is inactive until the Channel is ready to accept data.
12. After a sufficient amount of time, the Channel BIST Signature registers 0xA5 and 0xA6 will contain a numeric value that can be compared to the expected value for a known good AD6634 with the exact same configuration. If the values are the same, then there is a very low probability that there is an error in the channel.

CHIP SYNCHRONIZATION

Two types of synchronization can be achieved with the AD6634. These are Start and Hop. Each is described in detail below. The synchronization is accomplished with the use of a shadow register and a hold-off counter. See Figure 34 for a simplistic schematic of the NCO Shadow Register and NCO Freq Hold-Off Counter to understand basic operation. Enabling the clock (AD6634 CLK) for the hold-off counter can occur with either a Soft_Sync (via the microport), or a Pin Sync (via any of the four AD6634 SYNC pins A, B, C, and D). The functions that include shadow registers to allow synchronization include:

1. Start
2. Hop (NCO Frequency)

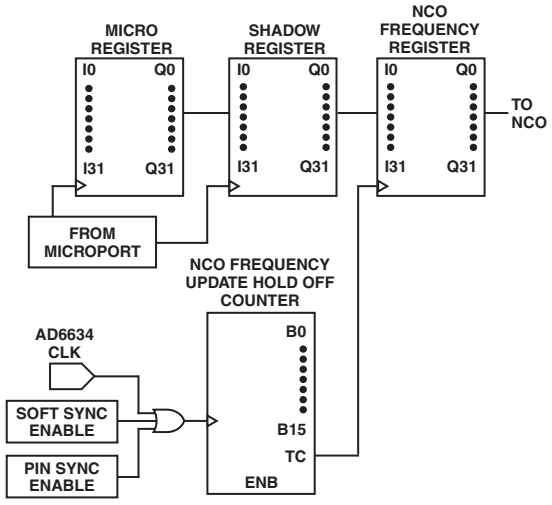


Figure 34. NCO Shadow Register and Hold-Off Counter

Start

Start refers to the start-up of an individual channel, chip, or multiple chips. If a channel is not used, it should be put in the Sleep Mode to reduce power dissipation. Following a hard reset (low pulse on the AD6634 $\overline{\text{RESET}}$ pin), all channels are placed in the Sleep Mode. Channels may also be manually put to sleep by writing to the mode register controlling the sleep function.

Start with No Sync

If no synchronization is needed to start multiple channels or multiple AD6634s, the following method should be used to initialize the device.

1. To program a channel, it must first be set to Sleep Mode (bit high) (Ext Address 3). All appropriate control and memory registers (filter) are then loaded. The Start Update Hold-Off Counter (0x83) should be set to 1.
2. Set the Sleep bits low (Ext Address 3). This enables the channel. The channel must the Sleep Mode low to activate a channel.

Start with Soft Sync

The AD6634 includes the ability to synchronize channels or chips under microprocessor control. One action to synchronize is the start of channels or chips. The Start Update Hold-Off Counter (0x83) in conjunction with the Start bit and Sync bit (Ext Address 5) allow this synchronization. Basically, the Start Update Hold-Off Counter delays the Start of a channel(s) by its value (number of AD6634 CLKs). The following method is used to synchronize the start of multiple channels via microprocessor control.

1. Set the appropriate channels to sleep mode (a hard reset to the AD6634 RESET pin brings all four channels up in sleep mode).
2. Note that the time from when DTACK (Pin 57) goes high to when the NCO begins processing data is the content of the Start Update Hold-Off Counter(s) (0x83) + 6 master clock cycles.
3. Write the Start Update Hold-Off Counter(s) (0x83) to the appropriate value (greater than 1 and less than 2^16–1). If the chip(s) is not initialized, all other registers should be loaded at this step.
4. Write the Start bit and the SYNC bit high (Ext Address 5).
5. This starts the Start Update Hold-Off Counter counting down. The counter is clocked with the AD6634 CLK signal. When it reaches a count of 1, the Sleep bit of the appropriate channel(s) is set low to activate the channel(s).

Start With Pin Sync

The AD6634 has four Sync pins, A, B, C, and D, that can be used to provide for very accurate synchronization channels. Each channel can be programmed to look at any of the four sync pins. Additionally, any or all channels can monitor a single Sync pin or each can monitor a separate pin, providing complete flexibility of synchronization. Synchronization of Start with one of the external signals is accomplished with the following method.

1. Set the appropriate channels to Sleep mode (a hard reset to the AD6634 $\overline{\text{RESET}}$ pin brings all four channels up in Sleep mode).
2. Note that the time from when the SYNC pin goes high to when the NCO begins processing data is the content of the Start Update Hold-Off Counter(s) (0x83) + 3 master clock cycles.
3. Write the Start Update Hold-Off Counter(s) (0x83) to the appropriate value (greater than 1 and less than 2^{16}–1). If the chip(s) is not initialized, all other registers should be loaded at this step.

4. Set the Start on Pin Sync bit and the appropriate Sync Pin Enable high (Ext Address 4) (A, B, C, or D).
5. When the Sync pin is sampled high by the AD6634 CLK, this enables the count down of the Start Update Hold-Off Counter. The counter is clocked with the AD6634 CLK signal. When it reaches a count of 1, the Sleep bit of the appropriate channel(s) is set low to activate the channel(s).

Hop

Hop is a jump from one NCO frequency to a new NCO frequency. This change in frequency can be synchronized via microprocessor control (Soft Sync) or an external Sync signal (PIN Sync) as described below.

To set the NCO frequency without synchronization the following method should be used.

Set Freq No Hop

1. Set the NCO Freq Hold-Off counter to 0.
2. Load the appropriate NCO frequency. The new frequency will be immediately loaded to the NCO.

Hop with Soft Sync

The AD6634 includes the ability to synchronize a change in NCO frequency of multiple channels or chips under microprocessor control. The NCO Freq Hold-Off counter (0x84) in conjunction with the Hop bit and the Sync bit (Ext Address 4) allow this synchronization. Basically the NCO Freq Hold-Off counter delays the new frequency from being loaded into the NCO by its value (number of AD6634 CLKs). The following method is used to synchronize a hop in frequency of multiple channels via microprocessor control.

1. Note that the time from when DTACK (Pin 57) goes high to when the NCO begins processing data is the contents of the NCO Freq Hold-Off counter (0x84) + 7 master clock cycles.
2. Write the NCO Freq Hold-Off (0x84) counter to the appropriate value (greater than 1 and less then 2^{16}–1).
3. Write the NCO Frequency register(s) to the new desired frequency.
4. Write the Hop bit and the Sync(s) bit high (Ext Address 4).
5. This starts the NCO Freq Hold-Off counter counting down. The counter is clocked with the AD6634 CLK signal. When it reaches a count of 1, the new frequency is loaded into the NCO.

Hop with Pin Sync

The AD6634 include four Sync pins to provide the most accurate synchronization, especially between multiple AD6634s. Synchronization of hopping to a new NCO frequency with an external signal is accomplished with the following method.

1. Note that the time from when the SYNC pin goes high to when the NCO begins processing data is the contents of the NCO Freq Hold-Off counter (0x84) + 5 master clock cycles.
2. Write the NCO Freq Hold-Off counter(s) (0x84) to the appropriate value (greater than 1 and less than 2^{16}–1).
3. Write the NCO Frequency register(s) to the new desired frequency.
4. Set the Hop on Pin Sync bit and the appropriate Sync Pin Enable high.
5. When the selected Sync pin is sampled high by the AD6634 CLK, this enables the countdown of the NCO Freq Hold-Off counter. The counter is clocked with the AD6634 CLK signal. When it reaches a count of 1, the new frequency is loaded into the NCO.

PARALLEL OUTPUT PORTS

The AD6634 incorporates two independent 16-bit parallel ports for output data transfer. Both parallel ports share pins and internal mux circuitry. A single parallel port and a single Link Port can be used simultaneously, but only if they do not share the same data path; the two possible choices are Parallel Port A with Link Port B, or Parallel Port B with Link Port A. Figure 35 presents a simplified block diagram showing the AD6634's output data routing configuration.

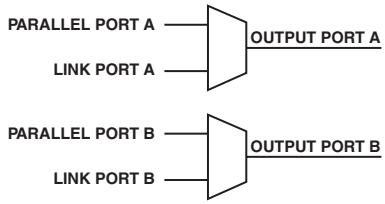


Figure 35. Output Port Data Routing

Parallel port configuration is specified by accessing Port Control Register addresses 0x1A and 0x1C for parallel ports A and B, respectively. Port clock Master/Slave mode (described later) is configured using the Port Clock Control register at address 0x1E. Note that to access these registers, Bit 5 (Access Port Control Registers) of external address 3 (SLEEP register) must be set. The address is then selected by programming the CAR register at external address 6.

The parallel ports are enabled by setting Bit 7 of the Link Control registers at addresses 0x1B and 0x1D for ports A and B, respectively.

Each parallel port is capable of operating in either Channel mode or AGC mode. Each mode is described in detail below.

Channel Mode

Parallel port Channel mode is selected by setting Bit 0 of addresses 0x1B and 0x1D for parallel ports A and B, respectively. In Channel mode, I and Q words from each channel is directed to the parallel port, bypassing the AGC. The specific channels output by the port are selected by setting Bits 1 through 4 of Parallel Port Control Register 0x1A (port A) and 0x1C (port B).

Channel mode provides two data formats. Each format requires a different number of parallel port clock (PCLK) cycles to complete the transfer of data. In each case, each data element is transferred during one PCLK cycle. See Figures 36 and 37, which present Channel mode parallel port timing.

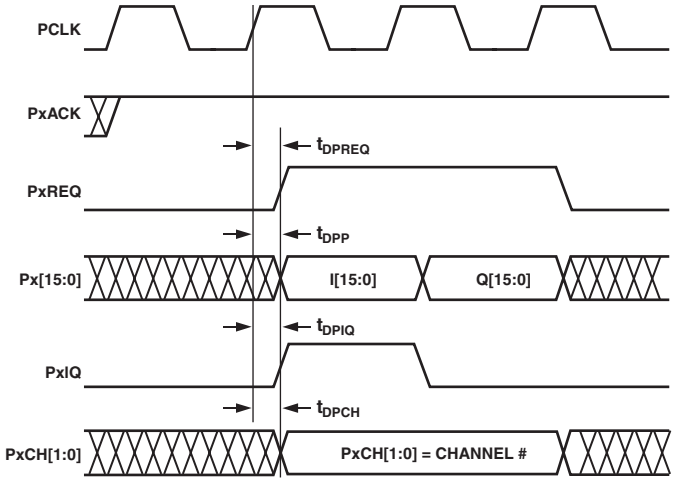


Figure 36. Channel Mode Interleaved Format

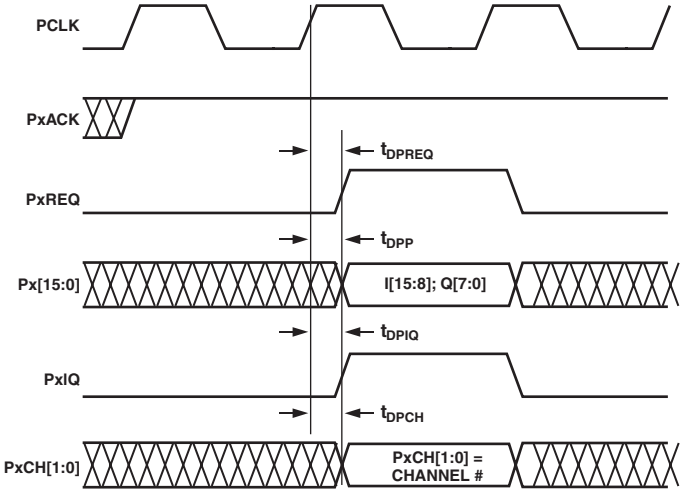


Figure 37. Channel Mode 8I/8Q Parallel Format

The 16-bit interleaved format provides I and Q data for each output sample on back-to-back PCLK cycles. Both I and Q words consist of the full port width of 16 bits. Data output is triggered on the rising edge of PCLK when both REQ and ACK are asserted. I data is output during the first PCLK cycle; and the PAIQ and PBIQ output indicator pins are set high to indicate that I data is on the bus. Q data is output during the subsequent PCLK cycle; and the PAIQ and PBIQ output indicator pins are low during this cycle.

The 8-bit concurrent format provides eight bits of I data and eight bits of Q data simultaneously during one PCLK cycle, also triggered on the rising edge of PCLK. The I byte occupies the most significant byte of the port, while the Q byte occupies the least significant byte. The PAIQ and PBIQ output indicator pins are set high during the PCLK cycle. Note that if data from multiple channels are output consecutively, the PAIQ and PBIQ output indicator pins will remain high until data from all channels has been output.

The PACH[1:0] and PBCH[1:0] pins provide a 2-bit binary value indicating the source channel of the data currently being output.

Care should be taken to read data from the port as soon as possible. If not, the sample will be overwritten when the next new data sample arrives. This occurs on a per-channel basis; i.e., a channel 0 sample will only be overwritten by a new channel 0 sample, and so on.

The order of data output is dependent on when data arrived at the port, which is a function of total decimation rate, Start-Hold-Off values, and so on. Priority order is, from highest to lowest, channels 0, 1, 2, 3.

AGC Mode

Parallel port channel mode is selected by clearing Bit 0 of addresses 0x1A and 0x1C for parallel ports A and B, respectively. I and Q data output in AGC mode are output from the AGC, not the individual channels. Each AGC receives data from only two AD6634 channels; AGC A accepts data from channels 0 and 1, while AGC B accepts data from channels 2 and 3. Each pair of channels is required to be configured such that the generation of output samples from the channels is out of phase (by typically 180 degrees). Each parallel port can provide data from either one or both AGCs. Bits 1 and 2 of register addresses 0x1A (port A) and 0x1C (port B) control the inclusion of data from AGCs A and B, respectively.

AGC mode provides only one I and Q format, which is similar to the 16-bit interleaved format of Channel mode. When both REQ and ACK are asserted, the next rising edge of PCLK triggers the output of a 16-bit AGC I word for one PCLK cycle. The PAIQ and PBIQ output indicator pins are high during this cycle, and low otherwise. A 16-bit AGC Q word is provided during the subsequent PCLK cycle. If the AGC gain word has been updated since the last sample, a 12-bit RSSI (Receive Signal Strength Indicator) word is provided during the PCLK cycle following the Q word on 12 MSBs of the parallel port data pins. The RSSI word is the bit-inverse of the Signal Gain word used in the Gain multiplier of the AGC.

The data provided by the PACH[1:0] and PBCH[1:0] pins in AGC mode is different than that provided in Channel mode. In AGC mode, PACH[0] and PBCH[0] indicate the AGC source of the data currently being output (0 = AGC A, 1 = AGC B). PACH[1] and PBCH[1] indicate whether the current data is an I/Q word or an AGC RSSI word (0 = I/Q word, 1 = AGC RSSI word). The two different AGC outputs are shown in Figures 38 and 39.

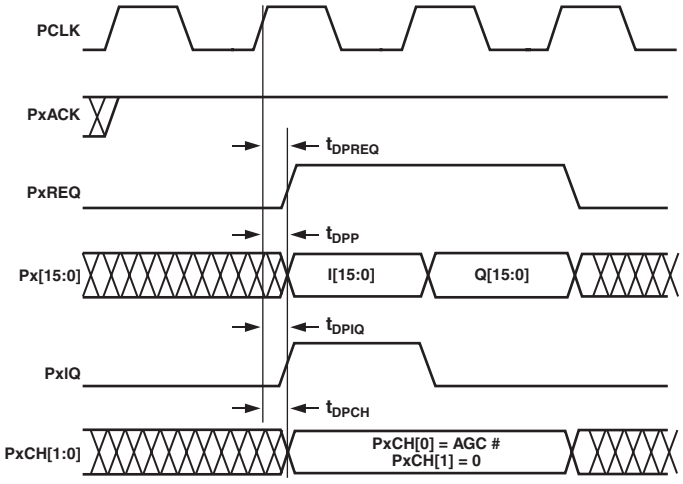


Figure 38. AGC Output with No RSSI Word

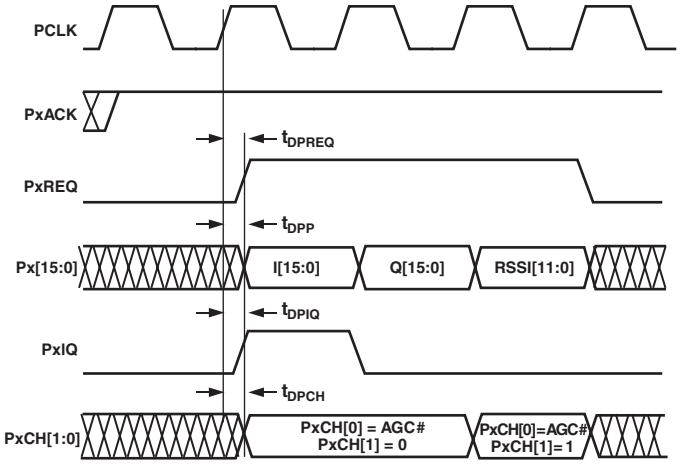


Figure 39. AGC Output with RSSI Word

Master/Slave PCLK Modes

The parallel ports may operate in either Master or Slave mode. The mode is set via the Port Clock Control register (address 0x1E). The parallel ports power up in Slave mode to avoid possible contentions on the PCLK pin.

In Master mode, PCLK is an output whose frequency is the AD6634 clock frequency divided by the PCLK divisor. Since values for PCLK_divisor[2:1] can range from 0 to 3, integer divisors of 1, 2, 4, or 8, respectively, can be obtained. Since the maximum clock rate of the AD6634 is 80 MHz, the highest PLCK rate in Master mode is also 80 MHz. Master mode is selected by setting Bit 0 of address 0x1E.

In Slave mode, external circuitry provides the PCLK signal. Slave mode PCLK signals may be either synchronous or asynchronous. The maximum Slave mode PCLK frequency is 100 MHz.

Parallel Port Pin Functionality

The following describes the functionality of the pins used by the parallel ports.

PCLK—Input/Output. As an output (Master mode), the maximum frequency is CLK/N, where CLK is AD6634 clock and N is an integer divisor from 1, 2, 4, or 8. As an input (Slave mode), it may be asynchronous relative to the AD6634 CLK. This pin powers up as an input to avoid possible contentions. Other port outputs change on the rising edge of PCLK.

REQ—Active HIGH output, synchronous to PCLK. A logic HIGH on this pin indicates that data is available to be shifted out of the port. A logic HIGH value remains high until all pending data has been shifted out.

ACK—Active HIGH asynchronous input. Applying a logic LOW on this pin inhibits parallel port data shifting. Applying a logic HIGH to this pin when REQ is high causes the parallel port to shift out data according the programmed data mode. ACK is sampled on the rising edge of PCLK. Assuming REQ is asserted, the latency from the assertion of ACK to data appearing at the parallel port output is no more than 1.5 PCLK cycles (see Figure 12). ACK may be held high continuously; in this case, when data becomes available, shifting begins 1 PCLK cycle after the assertion of REQ (see Figure 36).

PAIQ, PBIQ—High whenever I data is present on the port output, low otherwise.

PACH[1:0], PBCH[1:0]—These pins serve to identify data in both of the data modes. In Channel mode, these pins form a 2-bit binary number identifying the source channel of the current data-word. In AGC mode, [0] indicates the AGC source (0 = AGC A, 1 = AGC B), and [1] indicates whether the current data-word is I/Q data (0) or an RSSI word (1).

PA[15:0], PB[15:0]—Parallel Output Data Ports. Contents and format are mode-dependent.

LINK PORT

The AD6634 has two configurable link ports that provide a seamless data interface with the TigerSHARC DSP. Each link port allows the AD6634 to write output data to the receive DMA channel in the TigerSHARC for transfer to memory. Since they operate independently of each other, each link port can be connected to a different TigerSHARC or different link ports on the same TigerSHARC. Figure 40 shows how to connect one of the two AD6634 link ports to one of the four TigerSHARC link ports. Link Port A is configured through register 0x1B and Link Port B is configured through register 0x1D.

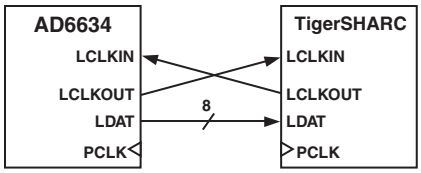


Figure 40. Link Port Connection between AD6634 and TigerSHARC

Link Port Data Format

Each link port can output data to the TigerSHARC in five different formats: 2-channel, 4-channel, dedicated AGC, redundant AGC with RSSI word, and redundant AGC without RSSI word. Each format outputs two bytes of I data and two bytes of Q data to form a 4-byte IQ pair. Since the TigerSHARC link port transfers data in quad-word (16-byte) blocks, four IQ pairs can make up one quad-word. If the channel data is selected (Bit 0 = 0 of 0x1B/0x1D), 4-byte IQ words of the four channels can be output in succession or alternating channel pair IQ words can be output. Figures 41 and 42 show the quad-word transmitted for each scenario with corresponding register values for configuring each link port.

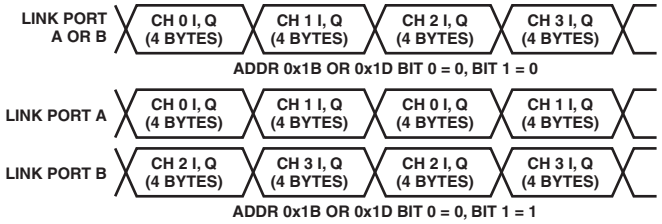


Figure 41. Link Port Data from RCF

If AGC output is selected (Bit 0 = 1), RSSI information can be sent with the IQ pair from each AGC. Each link port can be configured to output data from one AGC or both link ports can output data from the same AGC. If both link ports are transmitting the same data, RSSI information must be sent with the IQ words (Bit 2 = 0). Note that the actual RSSI word is only two bytes (12 bits appended with four zeros), so the link port sends two bytes of 0s immediately after each RSSI word to make a full 16-byte quad-word.

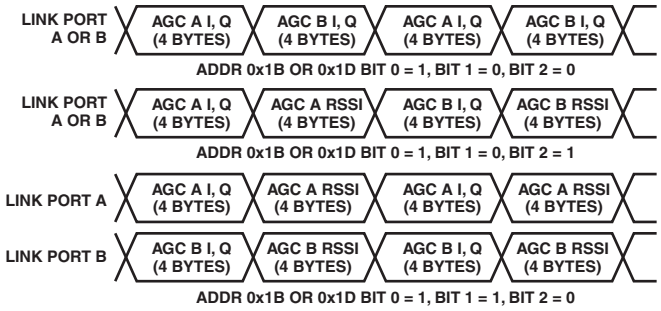


Figure 42. Link Port Data from AGC

Note that Bit 0 = 1 Bit 1 = 0, and Bit 2 = 1 is not a valid configuration. Bit 2 must be set to 0 to output AGC A IQ and RSSI words on link port A, and AGC B IQ and RSSI words on link port B.

Link Port Timing

Both link ports run off of PCLK, which can be externally provided to the chip (Addr 0x1E Bit 0 = 0) or generated from the master clock of the AD6634 (Addr 0x1E Bit 0 = 1). This register boots to 0 (Slave mode) and allows the user to control the data rate coming from the AD6634. PCLK can be run as fast as 100 MHz.

The link port provides a 1-byte data-word (LA[7:0], LB[7:0] pins) and output clocks (LACLKOUT, LBCLKOUT pins) in response to a ready signals (LACLKIN, LBCLKIN pins) from the receiver. Each link port transmits eight bits on each edge of LCLKOUT, requiring eight LCLKOUT cycles to complete transmission of the full 16 bytes of a TigerSHARC quad-word.

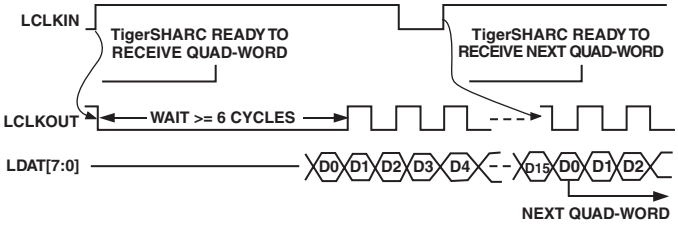


Figure 43. Link Port Data Transfer

Due to the TigerSHARC link port protocol, the AD6634 must wait at least six PCLK cycles after the TigerSHARC is ready to receive data, as indicated by the TigerSHARC setting the respective AD6634 LCLKIN pin high. Once the AD6634 link port has waited the appropriate number of PCLK cycles and has begun transmitting data, the TigerSHARC does a connectivity check by sending the AD6634 LCLKIN low and then high while the data is being transmitted. This tells the AD6634 link port that the TigerSHARC's DMA is ready to receive the next quad-word after completion of the current quad-word. Because the connectivity check is done in parallel to the data transmission, the AD6634 is able to stream uninterrupted data to the TigerSHARC.

The length of the wait before data transmission is a 4-bit programmable value in the link port control registers (0x1B and 0x1D Bits 6–3). This value allows the AD6634 PCLK and the TigerSHARC PCLK to be run at different rates and out of phase.

$$WAIT \geq ceil\left(6 \times \frac{f_{LCLK\_34}}{f_{LCLK\_TSHARC}}\right)$$

WAIT ensures that the amount of time the AD6634 needs to wait to begin data transmission is at least equal to the minimum amount of time the TigerSHARC is expecting it to wait. If the PCLK of the AD6634 is out of phase with the PCLK of the TigerSHARC and the argument to the ceil() function is an integer, *WAIT* must be strictly greater than the value given in the above formula.
If the LCLKs are in phase, the maximum output data rate is:

$$f_{LCLK\_34} \leq \frac{15}{6} \times f_{LCLK\_TSHARC}$$

otherwise it is:

$$f_{LCLK\_34} \leq \frac{14}{6} \times f_{LCLK\_TSHARC}$$

TigerSHARC Configuration

Since the AD6634 is always the transmitter in this link and the TigerSHARC is always the receiver, the values in Table IX can be programmed into the LCTL register for the link port used to receive AD6634 output data. User means that the actual register value depends on the user's application.

Table IX. TigerSHARC LCTLx Register Configuration

VERE	0
SPD	User
LTEN	0
PSIZE	1
TTOE	0
CERE	0
LREN	1
RTOE	1

MEMORY MAPS

0x00–0x7F: Coefficient Memory(CMEM)

This is the Coefficient Memory(C-MEM) used by the RCF (See Table X). It is memory mapped as 128 words by 20 bits. A second 128 words of RAM may be accessed via this same location by writing Bit 8 of the RCF control register high at channel address 0xA4. The filter calculated will always use the same coefficients for I and Q. By using memory from both of these 128 blocks, a filter up to 160 taps can be calculated. Multiple filters can be loaded and selected with a single internal access to the Coefficient Offset register at channel address 0xA3.

Table X. Channel Address Memory Map

Channel Address	Register	Bit Width	Comments
00–7F	Coefficient Memory (CMEM)	20	128 × 20-Bit Memory
80	CHANNEL SLEEP	1	0: SLEEP Bit from EXT_ADDRESS 3
81	Soft_Sync Control Register	2	1: Hop 0: Start
82	Pin_SYNC Control Register	3	2: First SYNC Only 1: Hop_En 0: Start_En
83	Start Hold-Off Counter	16	Start Hold-Off Value
84	NCO Frequency Hold-Off Counter	16	NCO_FREQ Hold-Off Value
85	NCO Frequency Register 0	16	NCO_FREQ[15:0]
86	NCO Frequency Register 1	16	NCO_FREQ[31:16]
87	NCO Phase Offset Register	16	NCO_PHASE[15:0]
88	NCO Control Register	9	8–7: SYNC Input Select[1:0] 6: WB Input Select B/A 5–4: Input Enable Control 11: Clock on IEN Transition to Low 10: Clock on IENTransition to High 01: Clock on IEN High 00: Mask on IEN Low 3: Clear Phase Accumulator on HOP 2: Amplitude Dither 1: Phase Dither 0: Bypass (A-Input → I-Path, B → Q)
89–8F	Unused		

0x80: Channel Sleep Register
This register contains the SLEEP bit for the channel. When this bit is high, the channel is placed in a low power state. When this bit is low, the channel processes data. This bit can also be set by accessing the SLEEP register at external address 3. When the External SLEEP register is accessed, all four channels are accessed simultaneously and the SLEEP bits of the channels are set appropriately.

0x81: Soft_SYNC Register
This register is used to initiate SYNC events through the microport. If the Hop bit is written high, the Hop Hold-Off Counter at address 0x84 is loaded and begins to count down. When this value reaches 1, the NCO Frequency register used by the NCO accumulator is loaded with the data from channel addresses 0x85 and 0x86. When the Start bit is set high, the Start Hold-Off Counter is loaded with the value at address 0x83 and begins to count down. When this value hits 1, the Sleep bit in address 0x80 is dropped low and the channel is started.

0x82: Pin_SYNC Register
This register is used to control the functionality of the SYNC pins. Any of the four SYNC pins can be chosen and monitored by the channel. The channel can be configured to initiate either a Start or Hop SYNC event by setting the Hop or Start bit high. These bits function as enables so that when a SYNC pulse occurs, either the Start or Hop Hold-Off Counters are activated in the same manner as with a Soft_SYNC.

0x83: Start Hold-Off Counter
The Start Hold-Off Counter is loaded with the value written to this address when a Start_Sync is initiated. It can be initiated by either a Soft_SYNC or Pin_SYNC. The counter begins decrementing and when it reaches a value of 1, the channel is brought out of SLEEP and begins processing data. If the channel is already running, the phase of the filters is adjusted such that multiple AD6634s can be synchronized. A periodic pulse on the SYNC pin can be used in this way to adjust the timing of the filters with the resolution of the ADC sample clock. If this register is written to a 1, the Start will occur immediately when the SYNC comes into the channel. If it is written to a 0, no SYNC will occur.

0x84: NCO Frequency Hold-Off Counter
The NCO Frequency Hold-Off Counter is loaded with the value written to this address when either a Soft_SYNC or Pin_SYNC comes into the channel. The counter begins counting down so that when it reaches 1, the NCO frequency word is updated with the values of addresses 0x85 and 0x86. This is known as a Hop or Hop_SYNC. If this register is written to a 1, the NCO Frequency will be updated immediately when the SYNC comes into the channel. If it is written to a 0, no HOP will occur. NCO HOPs can be either phase continuous or nonphase continuous, depending upon the state of Bit 3 of the NCO control register at channel address 0x88. When this bit is low, the phase accumulator of the NCO is not cleared but starts to add the new NCO frequency word to the accumulator as soon as the SYNC occurs. If this bit is high, the phase accumulator of the NCO is cleared to 0 and the new word is then accumulated.

0x85: NCO Frequency Register 0
This register represents the 16 LSBs of the NCO Frequency word. These bits are shadowed and are not updated to the register used for the processing until the channel is either brought out of SLEEP or a Soft_SYNC or Pin_SYNC has been issued. In the latter two cases, the register is updated when the Frequency

Hold-Off Counter hits a value of 1. If the Frequency Hold-Off Counter is set to 1, the register will be updated as soon as the shadow is written.

0x86: NCO Frequency Register 1
This register represents the 16 MSBs of the NCO Frequency word. These bits are shadowed and are not updated to the register used for the processing until the channel is either brought out of SLEEP or a Soft_SYNC or Pin_SYNC has been issued. In the latter two cases the register is updated only when the Frequency Hold-Off Counter hits a value of 1. If the Frequency Hold-Off Counter is set to 1, the register will be updated as soon as the shadow is written.

0x87: NCO Phase Offset Register
This register represents a 16-bit phase offset to the NCO. It can be interpreted as values ranging from 0 to just under 2π.

0x88: NCO Control Register
This 9-bit register controls features of the NCO and the channel. The bits are defined below. For more details, the NCO section should be consulted.

Bits 8–7 of this register choose which of the four SYNC pins are used by the channel. The SYNC pin selected can be used to initiate a START, HOP, or timing adjustment to the channel. The Synchronization section provides more details on this.

Bit 6 of this register defines whether the A or B input port is used by the channel. If this bit is low, the A Input Port is selected; and if this bit is high, the B Input Port is selected. Each input port consists of a 14-bit input mantissa(INx[13:0]), a 3-bit exponent(EXPx[2:0]), and an input enable pin IENx. The x represents either A or B.

Bits 5–4 determine how the sample clock for the channel is derived from the high speed CLK signal. There are four possible choices. Each is defined below but for further details, the NCO section of the data sheet should be consulted.

When these bits are 00, the input sample rate (f_{SAMP}) of the channel is equal to the rate of the high speed CLK signal. When IEN is low, the data going into the channel is masked to 0. This is an appropriate mode for TDD systems where the receiver may wish to mask off the transmitted data yet still remain in the proper phase for the next receive burst.

When these bits are 01, the input sample rate is determined by the fraction of the rising edges of CLK on which the IEN input is high. For example, if IEN toggles on every rising edge of CLK, the IEN signal will only be sampled high on one out of every two rising edges of CLK, which means that the input sample rate f_{SAMP} will be one-half the CLK rate.

When these bits are 10, the input sample rate is determined by the rate at which the IEN pin toggles. The data that is captured on the rising edge of CLK after IEN transitions from low to high is processed. When these bits are 11, the accumulator and sample CLK are determined by the rate at which the IEN pin toggles. The data that is captured on the rising edge of CLK after IEN transitions from high to low is processed. For example, control modes 10 and 11 can be used to allow interleaved data from either the A or B input ports and then assigned to the respective channel. The IEN pin selects the data such that a channel could be configured in mode 10 and another could be configured in mode 11.

Bit 3 determines whether or not the phase accumulator of the NCO is cleared when a Hop occurs. The Hop can originate from either the Pin_SYNC or Soft_SYNC. When this bit is set to 0, the Hop is phase continuous and the accumulator is not cleared. When this bit is set to 1, the accumulator is cleared to 0 before it begins accumulating the new frequency word. This is appropriate when multiple channels are hopping from different frequencies to a common frequency.

Bits 2–1 control whether or not the dithers of the NCO are activated. The use of these features is heavily determined by the system constraints. Consult the NCO section of the data sheet for more detailed information on the use of dither.

Bit 0 of this register allows the NCO Frequency translation stage to be bypassed. When this occurs the data from the A Input Port is passed down the I path of the channel and the data from the B Input Port is passed down the Q path of the channel. This allows a real filter to be performed on baseband I and Q data.

Table XI. Channel Address Memory Map

Channel Address	Register	Bit Width	Comments
90	rCIC2 Decimation – 1	12	M_{rCIC2}–1
91	rCIC2 Decimation – 1	9	L_{rCIC2}–1
92	rCIC2 Scale	12	11: Exponent Invert 10: Exponent Weight 9–5: rCIC2_QUIET[4:0] 4–0: rCIC2_LOUD[4:0]
93	Reserved	8	Reserved (Must Be Written Low)
94	CIC5 Decimation – 1	8	M_{CIC5}–1
95	CIC5 Scale	5	4–0: CIC5_SCALE[4:0]
96	Reserved	8	Reserved (Must Be Written Low)
97–9F	Unused		
A0	RCF Decimation – 1	8	M_{RCF}–1
A1	RCF Decimation Phase	8	P_{RCF}
A2	RCF Number of Taps – 1	8	N_{TAPS}–1
A3	RCF Coefficient Offset	8	CO_{RCF}
A4	RCF Control Register	11	10: RCF Bypass BIST 9: RCF Input Select (Own 0, Other 1) 8: Program RAM Bank 1/0 7: Use Common Exponent 6: Force Output Scale 5–4: Output Format 1x: Floating Point 12 + 4 01: Floating Point 8 + 4 00: Fixed Point 3–0:1Output Scale
A5	BIST Signature for I Path	16	BIST-I
A6	BIST Signature for Q Path	16	BIST-Q
A7	No. of BIST Outputs to Accumulate	20	19–0: No. of Outputs(Counter Value Read)
A8	RAM BIST Control Register	3	2: D-RAM Fail/Pass 1: NC-RAM Fail/Pass 0: RAM BIST Enable
A9	Output Control Register		9: Map RCF Data to BIST Registers 5: Output Format 1:16-Bit I and 16-Bit Q 0:12-Bit I and 12-Bit Q

0x90: rCIC2 Decimation – 1 (M_{rCIC2} – 1)
This register is used to set the decimation in the rCIC2 filter. The value written to this register is the decimation minus one. The rCIC2 decimation can range from 1 to 4096, depending upon the interpolation of the channel. The decimation must always be greater than the interpolation. M_{rCIC2} must be chosen larger than L_{rCIC2} and both must be chosen such that a suitable rCIC2 scalar can be chosen. For more details, the rCIC2 section should be consulted.

0x91: rCIC2 Interpolation – 1 (L_{rCIC2} – 1)
This register is used to set the interpolation in the rCIC2 filter. The value written to this register is the interpolation minus one. The rCIC2 interpolation can range from 1 to 512, depending upon the decimation of the rCIC2. There is no timing error associated with this interpolation. See the rCIC2 section for further details.

0x92: rCIC2 Scale
The rCIC2 scale register is used to provide attenuation to compensate for the gain of the rCIC2 and to adjust the linearization of the data from the floating-point input. The use of this scale register is influenced both by the rCIC2 growth and floating-point input port considerations. The rCIC2 section should be consulted for details. The rCIC2 scalar has been combined with the exponent offset and will need to be handled appropriately in both the input port and rCIC2 sections.

Bit 11 determines the polarity of the exponent. Normally, this bit will be cleared unless an ADC such as the AD6600 is used, in which case this bit will be set.

Bit 10 determines the weight of the exponent word associated with the input port. When this bit is Low, each exponent step is considered to be worth 6.02 dB. When this bit is High, each exponent step is considered to be worth 12.02 dB.

Bits 9–5 are the actual scale value used when the Level Indicator, LI pin associated with this channel is active.

Bits 4–0 are the actual scale value used when the Level Indicator, LI pin associated with this channel is active.

0x93:
Reserved (must be written Low).

0x94: CIC5 Decimation – 1 (M_{CIC5} – 1)
This register is used to set the decimation in the CIC5 filter. The value written to this register is the decimation minus one. Although this is an 8-bit register, the decimation is usually limited to between 1 and 32. Decimations higher than 32 would require more scaling than the CIC5 is capable of.

0x95: CIC5 Scale
The CIC5 scale factor is used to compensate for the growth of the CIC5 filter. Consult the CIC5 section for details.

0x96:
Reserved (must be written low).

0xA0: RCF Decimation – 1 (M_{RCF} – 1)
This register is used to set the decimation of the RCF stage. The value written is the decimation minus one. Although this is an 8-bit register that allows decimation up to 256, for most filtering scenarios the decimation should be limited between 1 and 32. Higher decimations are allowed but the alias protection of the RCF may not be acceptable for some applications.

0xA1: RCF Decimation Phase (P_{RCF})
This register allows any one of the M_{RCF} phases of the filter to be used and can be adjusted dynamically. This phase is updated each time a filter is started. When a channel is synchronized, it will retain the phase setting chosen here. This can be used as part of a timing recovery loop with an external processor or can allow multiple RCFs to work together while using a single RCF pair. The RCF section should be consulted for further details.

0xA2: RCF Number of Taps – 1 (N_{TAPS} – 1)
The number of taps for the RCF filter minus one is written here.

0xA3: RCF Coefficient Offset (CO_{RCF})
This register is used to specify which section of the 256-word coefficient memory is used for a filter. It can be used to select between multiple filters that are loaded into memory and referenced by this pointer. This register is shadowed and the filter pointer is updated every time a new filter is started. This allows the coefficient offset to be written even while a filter is being computed with disturbing operation. The next sample that comes out of the RCF will be with the new filter.

0xA4: RCF Control Register
The RCF control register is an 11-bit register that controls the general features of the RCF as well as the output formatting. The bits of this register and their functions are described below.

Bit 10 bypasses the RCF filter and sends the CIC5 output data to the BIST-I and BIST-Q registers. The 16 MSBs of the CIC5 data can be accessed from this register if Bit 9 of the RCF Control Register 2 at Channel Address 0xA9 is set.

Bit 9 of this register controls the source of the input data to the RCF. If this bit is 0, the RCF processes the output data of its own channel. If this bit is 1, it processes the data from the CIC5 of another channel. The CIC5 that the RCF is connected to when this bit is 1 is shown in the Table XII. These can be used to allow multiple RCFs to be used together to process wider bandwidth channels. See the Multiprocessing section for further details.

Table XII. RCF Input Configurations

Channel	RCF Input Source When Bit 9 is 1
0	1
1	0
2	1
3	1

Bit 8 is used as an extra address to allow a second block of 128 words of CMEM to be addressed by the channel addresses at 0x00–0x7F. If this bit is 0, the first 128 words are written; and if this bit is 1, a second 128 words is written. This bit is only used to program the coefficient memory. It is not used in any way by the processing and filters longer than 128 taps can be performed.

Bit 7 is used to help control the output formatting of the AD6634s RCF data. This bit is only used when the 8 + 4 or 12 + 4 floating-point modes are chosen. These modes are enabled by Bits 5 and 4 of this register below. When this bit is 0, the I and Q output exponents are determined separately based on their individual magnitudes. When this bit is 1, the I and Q data is a complex floating-point number where I and Q use a single exponent that is determined based on the maximum magnitude of I or Q.

Bit 6 is used to force the Output Scale Factor in Bits 3–0 of this register to be used to scale the data even when one of the floating-point output modes is used. If the number was too large to represent with the output scale chosen, the mantissas of the I and Q data clip and do not overflow.

Bits 5 and 4 choose the output formatting option used by the RCF data. The options are defined in the Table XIII and are discussed further in the Output Format section.

Table XIII. Output Formats

Bit Values	Output Option
1x	12-Bit Mantissa and 4-Bit Exponent (12 + 4)
01	8-Bit Mantissa and 4-Bit Exponent (8 + 4)
00	Fixed-Point Mode

Bits 3–0 of this register represent the Output Scale Factor of the RCF. It is used to scale the data when the output format is in fixed-point mode or when the Force Exponent bit is high.

0xA5: BIST Register for I
This register serves two purposes. The first is to allow the complete functionality of the I data path in the channel to be tested in the system. The BIST section of the data sheet should be consulted for further details. The second function is to provide access to the I output data through the microport. To accomplish this, the Map RCF data to BIST bit in the RCF Control register 2, 0xA9, should be set high. Sixteen bits of I data can then be read through the microport in either the 8 + 4, 12 + 4, 12-bit linear, or 16-bit linear output modes. This data may come from either the formatted RCF output or the CIC5 output.

0xA6: BIST Register for Q
This register serves two purposes. The first is to allow the complete functionality of Q data path in the channel to be tested in the system. The BIST section of the data sheet should be consulted for further details. The second function is to provide access to

the Q output data through the microport. To accomplish this, the Map RCF data to BIST bit in the RCF Control register 2, 0xA9, should be set high. Sixteen bits of Q data can then be read through the microport in either the 8 + 4, 12 + 4, 12-bit linear, or 16-bit linear output modes. This data may come from either the formatted RCF output or the CIC5 output.

0xA7: BIST Control Register
This register controls the number of outputs of the RCF or CIC filter that are observed when a BIST test is performed. The BIST signature registers at addresses 0xA5 and 0xA6 will observe this number of outputs and then terminate. The loading of this register also starts the BIST engine running. Details of how to utilize the BIST circuitry are defined in the BIST section.

0xA8: RAM BIST Control Register
This register is used to test the memories of the AD6634 should they ever be suspected of a failure. Bit 0 of this register is written with a 1 when the channel is in SLEEP and the user waits for 1600 CLKs and then polls the bits. If Bit 1 is high, the CMEM failed the test; and if Bit 2 is high, the data memory used by the RCF failed the test.

0xA9: Output Control Register
Bit 9 of this register allows the RCF or CIC5 data to be mapped to the BIST registers at addresses 0xA5 and 0xA6. When this bit is 0, the BIST register is in signature mode and ready for a self-test to be run. When this bit is 1, the output data from the RCF after formatting or the CIC5 data is mapped to these registers and can be read through the microport.

Bits 5 determines the word length used by the parallel port. If this bit is 0, the parallel port uses 12-bit words for I and Q. If this bit is 1, the parallel port uses 16-bit words for I and Q. When the fixed-point output option is chosen from the RCF control register, these bits also set the rounding correctly in the output formatter of the RCF.

Remaining bits in this register are reserved and should be written low when programming.

In order to access the Input/Output Port Registers, Bit 5 of $\overline{\text{SLEEP}}$ register (on external memory map) should be written high. The CAR is then written with the address to the correct Input Port Register.

Input Port Control Registers
The Input Port control register enables various input related features used primarily for input detection and level control. Depending on the mode of operation, up to four different signal paths can be monitored with these registers. These features are accessed by setting Bit 5 of external address 3 (Sleep Register) and then using the CAR (external address 6) to address the eight locations available.

Response to these settings is directed to the LIA-A, LIA-B, LIB-A, and LIB-B Pins.

0x00 Lower Threshold A
This word is 10 bits wide and maps to the 10 most significant bits of the mantissa. If the upper 10 bits of input port A are less than or equal to this value, the lower threshold has been met. In normal chip operation, this starts the dwell time counter. If the input signal increases above this value, the counter is reloaded and awaits the input to drop back to this level.

0x01 Upper Threshold A
This word is 10 bits wide and maps to the 10 most significant bits of the mantissa. If the upper 10 bits of input port A are greater than or equal to this value, the upper threshold has been met. In normal chip operation, this will cause the appropriate LI pin (LIA-A or LIA-B) to become active.

0x02 Dwell Time A
This sets the time that the input signal must be at or below the lower threshold before the LI pin is deactivated. For the input level detector to work, the dwell time must be set to at least 1. If set to 0, the LI functions are disabled.

This is a 20-bit register. When the lower threshold is met following an excursion into the upper threshold, the dwell time counter is loaded and begins to count high speed clock cycles as long as the input is at or below the lower threshold. If the signal increases above the lower threshold, the counter is reloaded and waits for the signal to fall below the lower threshold again.

0x03 Gain Range A Control Register
Bit 4 determines the polarity of LIA-A and LIA-B. If this bit is clear, the LI signal is high when the upper threshold has been exceeded. However, if this bit is set, the LI pin is low when active. This allows maximum flexibility when using this function.

Bit 3 determines if the input consists of a single channel or TDM channels such as when using the AD6600. If this bit is cleared, a single ADC is assumed. In this mode, LIA-A functions as the active output indicator. LIA-B provides the complement of LIA-A. However, if this bit is set, the input is determined to

Table XIV. Memory Map for Input Port Control Registers

Channel Address	Register	Bit Width	Comments
00	Lower Threshold A	10	9–0: Lower Threshold for Input A
01	Upper Threshold A	10	9–0: Upper Threshold for Input A
02	Dwell Time A	20	19–0: Minimum Time Below Lower Threshold A
03	Gain Range A Control Register	5	4: Output Polarity LIA-A and LIA-B 3: Interleaved Channels 2–0: Linearization Hold-Off Register
04	Lower Threshold B	10	9–0: Lower Threshold for Input B
05	Upper Threshold B	10	9–0: Upper Threshold for Input B
06	Dwell Time B	20	19–0: Minimum Time Below Lower Threshold B
07	Gain Range B Control Register	5	4: Output Polarity LIB-A and LIB-B 3: Interleaved Channels 2–0: Linearization Hold-Off Register

be dual-channel and determined by the state of the IENA pin. If the IENA pin is low, the input detection is directed to LIA-A. If the IENA pin is high, the input is directed to LIA-B. In either case, Bit 4 determines the actual polarity of these signals.

Bits 2–0 determine the internal latency of the gain detect function. When the LIA-A,B pins are made active, they are typically used to change an attenuator or gain stage. Since this is prior to the ADC, there is a latency associated with the ADC and with the settling of the gain change. This register allows the internal delay of the LIA-A,B signal to be programmed.

0x04 Lower Threshold B
This word is 10 bits wide and maps to the 10 most significant bits of the mantissa. If the upper 10 bits of input port B are less than or equal to this value, the lower threshold has been met. In normal chip operation, this starts the dwell time counter. If the input signal increases above this value, the counter is reloaded and awaits the input to drop back to this level.

0x05 Upper Threshold B
This word is 10 bits wide and maps to the 10 most significant bits of the mantissa. If the upper 10 bits of input port B are greater than or equal to this value, the upper threshold has been met. In normal chip operation, this will cause the appropriate LI pin (LIB-A or LIB-B) to become active.

0x06 Dwell Time B
This sets the time that the input signal must be at or below the lower threshold before the LI pin is deactivated. For the input level detector to work, the dwell time must be set to at least 1. If set to 0, the LI functions are disabled.

This is a 20-bit register. When the lower threshold is met following an excursion into the upper threshold, the dwell time counter is loaded and begins to count high speed clock cycles as long as the input is at or below the lower threshold. If the signal increases above the lower threshold, the counter is reloaded and waits for the signal to fall below the lower threshold again.

0x07 Gain Range B Control Register
Bit 4 determines the polarity of LIB-A and LIB-B. If this bit is clear then the LI signal is high when the upper threshold has been exceeded. However, if this bit is set, the LI pin is low when active. This allows maximum flexibility when using this function.

Bit 3 determines if the input consists of a single channel or TDM channels such as when using the AD6600. If this bit is cleared, a single ADC is assumed. In this mode, LIB-A functions as the active output indicator. LIB-B provides the complement of LIB-A. However if this bit is set, the input is determined to be dual channel and determined by the state of the IENB pin. If the IENB pin is low, the input detection is directed to LIB-A. If the IENB pin is high, the input is directed to LIB-B. In either case, Bit 4 determines the actual polarity of these signals.

Bits 2–0 determine the internal latency of the gain detect function. When the LIB-A,B pins are made active, they are typically used to change an attenuator or gain stage. Since this is prior to the ADC, there is a latency associated with the ADC and with the settling of the gain change. This register allows the internal delay of the LIB-A,B signal to be programmed.

Table XV. Memory Map for Output Port Control Registers

Channel Address	Register	Bit Width	Comments
08	Port A Control Register	4	3: Port A Enable 2–1: HB A Signal Interleaving 11 All 4 Channels 10 Chs 0, 1, 2 01 Chs 0,1 00 Ch 0 0: Bypass
09	Port B Control Register	3	2: Port B Enable 1: HB A Signal Interleaving 1 Chs 2, 3 0 Ch 2 0: Bypass
0A	AGC A Control Register	8	7–5: Output Word Length 111 4 Bits 110 5 Bits 101 6 Bits 100 7 Bits 011 8 Bits 010 10 Bits 001 12 Bits 000 16 Bits 4: Clipping Error 1: Maintain Level of Clipping Error 0: Maintain Output Signal Level 3: Sync Now 2: Init on Sync 1: First Sync Only 0: Bypass
0B	AGC A Hold-Off Counter	16	15–0: Hold Off Value
0C	AGC A Desired Level	8	7–0: Desired Output Power Level or Clipping Energy (R Parameter)
0D	AGC A Signal Gain	12	11–0: G_S Parameter
0E	AGC A Loop Gain	8	7–0: K Parameter
0F	AGC A Pole Location	8	7–0: P Parameter
10	AGC A Average Samples	6	5–2: Scale for CIC Decimator 1-0: Number of Averaging Samples
11	AGC A Update Decimation	12	11–0: CIC Decimation Ratio
12	AGC B Control Register	8	7–5: Output Word Length 112 4 Bits 110 5 Bits 102 6 Bits 101 7 Bits 011 8 Bits 010 10 Bits 001 12 Bits 000 16 Bits 4: Clipping Error 1: Maintain Level of Clipping Error 0: Maintain Output Signal Level 3: Sync Now 2: Init on Sync 1: First Sync Only 0: Bypass
13	AGC B Hold-Off Counter	16	15–0: Hold Off Value
14	AGC B Desired Level	8	7–0: Desired Output Power Level or Clipping Energy (R Parameter)
15	AGC B Signal Gain	12	11–0: G_S Parameter

Table XV. Memory Map for Output Port Control Registers (continued)

Channel Address	Register	Bit Width	Comments
16	AGC B Loop Gain	8	7–0: K Parameter
17	AGC B Pole Location	8	7–0: P Parameter
18	AGC B Average Samples	6	5–2: Scale for CIC Decimator 1–0: Number of Averaging Samples
19	AGC B Update Decimation	12	11–0: CIC Decimation
1A	Parallel A Control	8	7–6: Reserved 5: Parallel Port Data Format 1: 8-Bit Parallel I, Q 0: 16-Bit Interleaved I, Q 4: Channel 3 3: Channel 2 2: Channel 1/AGC B Enable 1: Channel 0/AGC A Enable 0: AGC_CH Select 1: Data Comes from AGCs 0: Data Comes from Channels
1B	Link A Control	8	7: Link Port A Enable 6–3: Wait 2: No RSSI Word 1: Don't Output RSSI Word 0: Output RSSI Word 1: Channel Data Interleaved 1: 2-Channel Mode/Separate AB 0: 4-Channel Mode/AB Same Port 0: AGC_CH Select 1: Data Comes from AGCs 0: Data Comes from Channels
1C	Parallel B Control	8	7–6: Reserved 5: Parallel Port Data Format 1: 8-Bit Parallel I, Q 0: 16-Bit Interleaved I, Q 4: Channel 3 3: Channel 2 2: Channel 1/AGC B Enable 1: Channel 0/AGC A Enable 0: AGC_CH Select 1: Data Comes from AGCs 0: Data Comes from Channels
1D	Link B Control	8	7: Link Port B Enable 6–3: Wait 2: No RSSI Word 1: Don't Output RSSI Word 0: Output RSSI Word 1: Channel Data Interleaved 1: 2-Channel Mode/Separate AB 0: 4-Channel Mode/AB Same Port 0: AGC_CH Select 1: Data Comes from AGCs 0: Data Comes from Channels
1E	Port Clock Control	3	2–1: PCLK Divisor 0: PCLK Master/Slave* 0: Slave 1: Master

*PCLK boots as slave.

In order to access the Input/Output Port Registers, Bit 5 of SLEEP register (on external memory map) should be written high. The CAR is then written with the address to the correct Output Port Register.

0x08 Port A Control Register
Bit 0 enables the use of interpolating half-band filter corresponding to Port A. Half-band A can be used to interleave the data streams of multiple channels and interpolate by two providing a maximum output data rate of 4× the chip rate. It can be configured to listen to all four channels; channels 0, 1, 2, 3; channels 0, 1, 2; channels 0, 1; or only channel 0. Half-band A is bypassed when bit 0 = 1, in which case the outputs of the RCFs are directly sent to the AGC. The channel data streams are still interleaved with the half-band bypassed, but they are not filtered and interpolated. The maximum data rate from this configuration would be 2× the chip rate.

0x09 Port B Control Register
Bit 0 enables the use of interpolating half-band filter corresponding to Port B. Half-band B can be used to interleave the data streams of multiple channels and interpolate by 2 providing a maximum output data rate of 4× the chip rate. It can be configured to listen to channels 2 and 3; or only channel two. Half-band B is bypassed when bit 0 = 1, in which case the outputs of the RCFs are directly sent to the AGC. The channel data streams are still interleaved with the half-band bypassed, but they are not filtered and interpolated. The maximum data rate from this configuration would be 2× the chip rate.

0x0A AGC A Control Register
This 8-bit register controls features of the AGC A. The bits are defined below:

Bits 7–5 define the output word length of the AGC. The output word can be 4–8, 10, 12, or 16 bits wide. The control register bit representation to obtain different output word lengths is given in the Memory Map Table.

Bit 4 of this register sets the mode of operation for the AGC. When this bit is 0, the AGC tracks to maintain the output signal level and when this bit is 1, the AGC tracks to maintain a constant clipping error. Consult the AGC section for more details about these modes.

Bits 3–1 are used to configure the synchronization of the AGC. The CIC decimator filter in the AGC can be synchronized to an external sync signal to output an update sample for the AGC error calculation and filtering. This way the AGC gain changes can be synchronized to an external block like a Rake receiver. Whenever an external sync signal is received, the hold-off counter at 0x0B is loaded and begins to count down. When the counter reaches one, the CIC filter dumps an update sample and starts working towards a new update sample. The AGC can be initialized on each SYNC or only on the first SYNC.

Bit 3 is used to issue a command to the AGC to SYNC immediately. If this bit is set, the CIC filter will update the AGC with a new sample immediately and start operating towards the next update sample. The AGC can be synchronized by the microport control interface using this method.

Bit 2 is used to determine whether the AGC should initialize on a SYNC or not. When this bit is set, the CIC filter is cleared and new values for CIC decimation, number of averaging samples, CIC scale, Signal gain G_S, gain K, and pole parameter P are loaded. When Bit 2 = 0, the above-mentioned parameters are not updated and the CIC filter is not cleared. In both cases, an AGC update sample is output from the CIC filter and the decimator starts operating towards the next output sample whenever a SYNC occurs.

Bit 1 is used to ignore repetitive synchronization signals. In some applications, the synchronization signal may occur periodically. If this bit is clear, each synchronization request will resynchronize the AGC. If this bit is set, only the first occurrence will cause the AGC to synchronize and will update AGC gain values periodically depending on the decimation factor of the AGC CIC filter.

Bit 0 is used to bypass the AGC section, when it is set. The 23-bit representation from interpolating half-band filters is still reduced to a lower bit width representation as set by Bits 7–5 of the AGC A Control Register. A truncation at the output of the AGC accomplishes this task.

0x0B AGC A Hold-Off Counter
The AGC A Hold-Off counter is loaded with the value written to this address when either a Soft_SYNC or Pin_SYNC comes into the channel. The counter begins counting down so when it reaches one, a SYNC is given to AGC A. This SYNC may or may not initialize the AGC, as defined by the control word. The AGC loop is updated with a new sample from the CIC filter whenever a SYNC occurs. If this register is written to 1, the AGC will be updated immediately when the SYNC occurs. If this register is written to a 0, the AGC cannot be synchronized.

0x0C AGC A Desired Level
This 8-bit register contains the desired output power level or desired clipping level depending on the mode of operation. This desired Request R level can be set in dB from 0 to –23.99 in steps of 0.094 dB. 8-bit binary floating-point representation is used with 2-bit exponent followed by 6-bit mantissa. Mantissa is in steps of 0.094 dB and exponent in 6.02 dB steps. For example, 10'100101 represents $2 \times 6.02 + 37 \times 0.094 = 15.518$ dB.

0x0D AGC A Signal Gain
This register is used to set the initial value for a signal gain used in the gain multiplier. This 12-bit value sets the initial signal gain between 0 and 96.296 dB in steps of 0.024 dB. 12-bit binary floating-point representation is used with 4-bit exponent followed by 8-bit mantissa. For example, 0111'10001001 is equivalent to $7 \times 6.02 + 137 \times 0.024 = 45.428$ dB.

0x0E AGC A Loop Gain
This 8-bit register is used to define the open loop gain, K. Its value can be set from 0 to 0.996 in steps of 0.0039. This value of K is updated in the AGC loop each time the AGC is initialized.

0x0F AGC A Pole Location
This 8-bit register is used to define the open loop filter pole location P. Its value can be set from 0 to 0.996 in steps of 0.0039. This value of P is updated in the AGC loop each time the AGC is initialized. This open loop pole location will directly impact the closed loop pole locations as explained in the AGC section.

0x10 AGC A Average Samples
This 6-bit register contains the scale used for the CIC filter and the number of power samples to be averaged before being fed to the CIC filter.

Bits 5–2 define the scale used for the CIC filter.

Bits 1–0 define the number of samples to be averaged before they are sent to the CIC decimating filter. This number can be

set between 1 and 4 with bit representation 00 meaning one sample and bit representation 11 meaning four samples.

0x11 AGC A Update Decimation
This 12-bit register sets the AGC decimation ratio from 1 to 4096. An appropriate scaling factor should be set to avoid loss of bits.

0x12 AGC B Control Register
This 8-bit register controls features of the AGC A. The bits are defined below:

Bits 7–5 define the output word length of the AGC. The output word can be 4–8, 10, 12, or 16 bits wide. The control register bit representation to obtain different output word lengths is given in the Memory Map table.

Bit 4 of this register sets the mode of operation for the AGC. When this bit is 0, the AGC tracks to maintain the output signal level and when this bit is 1, the AGC tracks to maintain a constant clipping error. Consult the AGC section for more details about these modes.

Bits 3–1 are used to configure the synchronization of the AGC. The CIC decimator filter in the AGC can be synchronized to an external sync signal to output an update sample for the AGC error calculation and filtering. This way the AGC gain changes can be synchronized to an external block like a Rake receiver. Whenever an external sync signal is received, the hold-off counter at 0x0B is loaded and begins to count down. When the counter reaches one, the CIC filter dumps an update sample and starts working towards a new update sample. The AGC can be initialized on each SYNC or only on the first SYNC.

Bit 3 is used to issue a command to the AGC to SYNC immediately. If this bit is set, the CIC filter will update the AGC with a new sample immediately and start operating towards the next update sample. The AGC can be synchronized by the microport control interface using this method.

Bit 2 is used to determine whether the AGC should initialize on a SYNC or not. When this bit is set, the CIC filter is cleared and new values for CIC decimation, number of averaging samples, CIC scale, Signal gain G_S, gain K and pole parameter P are loaded. When Bit 2 = 0, the above-mentioned parameters are not updated and the CIC filter is not cleared. In both cases, an AGC update sample is output from the CIC filter and the decimator starts operating towards the next output sample whenever a SYNC occurs.

Bit 1 is used to ignore repetitive synchronization signals. In some applications, the synchronization signal may occur periodically. If this bit is clear, each synchronization request will resynchronize the AGC. If this bit is set, only the first occurrence will cause the AGC to synchronize and will update AGC gain values periodically depending on the decimation factor of the AGC CIC filter.

Bit 0 is used to bypass the AGC section, when it is set. The 23-bit representation from interpolating half-band filters is still reduced to a lower bit width representation as set by Bits 7–5 of the AGC A Control Register. A truncation at the output of the AGC accomplishes this task.

0x13 AGC B Hold-Off Counter
The AGC A Hold-Off counter is loaded with the value written to this address when either a Soft_SYNC or Pin_SYNC comes into the channel. The counter begins counting down so when it reaches one, a SYNC is given to AGC A. This SYNC may or may not initialize the AGC, as defined by the control word. The AGC loop is updated with a new sample from the CIC filter whenever a SYNC occurs. If this register is written to one, the AGC will be updated immediately when the SYNC occurs. If this register is written to a zero the AGC cannot be synchronized.

0x14 AGC B Desired Level
This 8-bit register contains the desired output power level or desired clipping level, depending on the mode of operation. This desired Request R level can be set in dB from 0 to –23.99 in steps of 0.094 dB. 8-bit binary floating-point representation is used with 2-bit exponent followed by 6-bit mantissa. Mantissa is in steps of 0.094 dB and exponent in 6.02 dB steps. For example, 10'100101 represents $2 \times 6.02 + 37 \times 0.094 = 15.518$ dB.

0x15 AGC B Signal Gain
This register is used to set the initial value for a Signal Gain used in the gain multiplier. This 12-bit value sets the initial signal gain between 0 and 96.296 dB in steps of 0.024 dB. 12-bit binary floating-point representation is used with 4-bit exponent followed by 8-bit mantissa. For example, 0111'10001001 is equivalent to $7 \times 6.02 + 137 \times 0.024 = 45.428$ dB.

0x16 AGC B Loop Gain
This 8-bit register is used to define the open loop gain, K. Its value can be set from 0 to 0.996 in steps of 0.0039. This value of K is updated in the AGC loop each time the AGC is initialized.

0x17 AGC B Pole Location
This 8-bit register is used to define the open loop filter pole location P. Its value can be set from 0 to 0.996 in steps of 0.0039. This value of P is updated in the AGC loop each time the AGC is initialized. This open loop pole location will directly impact the closed loop pole locations as explained in the AGC section.

0x18 AGC B Average Samples
This 6-bit register contains the scale used for the CIC filter and the number of power samples to be averaged before being fed to the CIC filter.

Bits 5–2 define the scale used for the CIC filter.

Bits 1–0 define the number of samples to be averaged before they are sent to the CIC decimating filter. This number can be set between 1 and 4 with bit representation 00 meaning one sample and bit representation 11 meaning four samples.

0x19 AGC B Update Decimation
This 12-bit register sets the AGC decimation ratio from 1 to 4096. An appropriate scaling factor should be set to avoid loss of bits.

0x1A Parallel Port Control A
Data is output through either a parallel port interface or a link port interface. When 0x1B Bit 7 = 0, the use of link port A is disabled and the use of parallel port A is enabled. The parallel port provides different data modes for interfacing with DSPs or FPGAs.

Bit 0 selects which data is output on parallel port A. When Bit 0 = 0, parallel port A outputs data from the RCF according to the format specified by Bits 1 through 4. When Bit 0 = 1, parallel port A outputs the data from the AGCs according to the format specified by Bits 1 and 2.

In AGC mode, Bit 0 = 1, Bit 1 determines if parallel port A is able to output data from AGC A, and Bit 2 determines if parallel port A is able to output data from AGC B. The order of output depends on the rate of triggers from each AGC, which in turn is determined by the decimation rate of the channels feeding it. In channel mode, Bit 0 = 0 and Bits 1 through 4 determine which combination of the four processing channels is output. The output order depends on the rate of triggers received from each

channel, which is determined by the decimation rate of each channel. The channel output indicator pins can be used to determine which data came from which channel.

Bit 5 determines the format of the output data-words. When Bit 5 = 0, parallel port A outputs 16-bit words on its 16-bit bus. This means that I and Q data are interleaved and the IQ indicator pin determines whether data on the port is I data or Q data. When Bit 5 = 1, parallel port A is outputting an 8-bit I word and an 8-bit Q word at the same time, and the IQ indicator pins will be HIGH.

0x1B Link Port Control A

Data is output through either a parallel port interface or a link port interface. The link port provides an efficient data link between the AD6634 and a TigerSHARC DSP and can be enabled by setting Bit 7 = 1.

Bit 0 selects which data is output on link port A. When Bit 0 = 0, link port A outputs data from the RCF according to the format specified by Bit 1. When Bit 0 = 1, link port A outputs the data from the AGCs according to the format specified by Bits 1 and 2.

Bit 1 has two different meanings that depend on whether data is coming from the AGCs or from the RCFs. When data is coming from the RCFs (Bit 0 = 0), Bit 1 selects between 2- and 4-channel data mode. Bit 1 = 1 indicates link port A transmits RCF IQ words alternately from channels 0 and 1. When Bit 1 = 1, link port A outputs RCF IQ words from each of the four channels in succession: 0, 1, 2, then 3. However, when AGC data is selected (Bit 0 = 1), Bit 1 selects the AGC data output mode. In this mode, when Bit 1 = 1, link port A outputs AGC A IQ and gain words. With this mode, gain words must be included by setting Bit 2 = 0. However, if Bit 0 = Bit 1 = 0, then AGC A and B are alternately output on link port A and the inclusion or exclusion of the gain words is determined by Bit 2.

Bit 2 selects if RSSI words are included or not in the data output. If Bit 1 = 1, Bit 2 = 0. Since the RSSI words are only two bytes long and the IQ words are four bytes long, the RSSI words are padded with zeros to give a full 16-byte TigerSHARC quad-word. If AGC output is not selected (Bit 0 = 0), this bit can be any value.

Bits 6 through 3 specify the programmable delay value for link port A between the time the link port receives a data ready from the receiver and the time it transmits the first data-word. The link port must wait at least six cycles of the receiver's clock, so this value allows the user to use clocks of differing frequency and phase for the AD6634 link port and the TigerSHARC link port. There is more information on the limitations and relationship of these clocks in the section on Link Ports.

0x1C Parallel Port Control B

Data is output through either a parallel port interface or a link port interface. When 0x1D Bit 7 = 0, the use of link port B is disabled and the use of parallel port B is enabled. The parallel port provides different data modes for interfacing with DSPs or FPGAs.

Bit 0 selects which data is output on parallel port B. When Bit 0 = 0, parallel port B outputs data from the RCF according to the format specified by Bits 1 through 4. When Bit 0 = 1, parallel port B outputs the data from the AGCs according to the format specified by Bits 1 and 2.

In AGC mode, Bit 0 = 1 and Bit 1 determines if parallel port B is able to output data from AGC A and Bit 2 determines if parallel port B is able to output data from AGC B. The order of output depends on the rate of triggers from each AGC, which in turn is determined by the decimation rate of the channels feeding it. In channel mode, Bit 0 = 0 and Bits 1 through 4 determine which combination of the four processing channels is output. The output order depends on the rate of triggers received from each channel, which is determined by the decimation rate of each channel. The channel output indicator pins can be used to determine which data came from which channel.

Bit 5 determines the format of the output data words. When Bit 5 = 0, parallel port B outputs 16-bit words on its 16-bit bus. This means that I and Q data are interleaved and the IQ indicator pin determines whether data on the port is I data or Q data. When Bit 5 = 1, parallel port B is outputting an 8-bit I word and an 8-bit Q word at the same time, and the IQ indicator pins will be HIGH.

0x1D Link Port Control B

Data is output through either a parallel port interface or a link port interface. The link port provides an efficient data link between the AD6634 and a TigerSHARC DSP and can be enabled by setting Bit 7 = 1.

Bit 0 selects which data is output on link port B. When Bit 0 = 0, link port B outputs data from the RCF according to the format specified by bit 1. When Bit 0 = 1, link port B outputs the data from the AGCs according to the format specified by Bits 1 and 2.

Bit 1 has two different meanings that depend on whether data is coming from the AGCs or from the RCFs. When data is coming from the RCFs (Bit 0 = 0), Bit 1 selects between 2- and 4- channel data mode. Bit 1 = 1 indicates link port A transmits RCF IQ words alternately from channels 0 and 1. When Bit 1 = 1, link port B outputs RCF IQ words from each of the four channels in succession: 0, 1, 2, then 3. However, when AGC data is selected (Bit 0 = 1), Bit 1 selects the AGC data output mode. In this mode, when Bit 1 = 1, link port B outputs AGC B IQ and gain words. With this mode, gain words must be included by setting Bit 2 = 0. However, if Bit 0 = Bit 1 = 0, then AGC A and B are alternately output on link port B and the inclusion or exclusion of the gain words is determined by Bit 2.

Bit 2 selects if RSSI words are included or not in the data output. If Bit 1 = 1, Bit 2 = 0. Since the RSSI words are only two bytes long and the IQ words are four bytes long, the RSSI words are padded with zeros to give a full 16-byte TigerSHARC quad-word. If AGC output is not selected (Bit 0 = 0) then this bit can be any value.

Bits 6 through 3 specify the programmable delay value for link port B between the time the link port receives a data ready from the receiver and the time it transmits the first data-word. The link port must wait at least six cycles of the receiver's clock, so this value allows the user to use clocks of differing frequency and phase for the AD6634 link port and the TigerSHARC link port. There is more information on the limitations and relationship of these clocks in the section on Link Ports.

0x1E Port Clock Control

Bit 0 determines whether PCLK is supplied externally by the user or derived internally in the AD6634. If PCLK is derived internally from CLK (Bit 0 = 1), it is output through the PCLK pin as a master clock. For most applications, PCLK will be provided by the user as an input to the AD6634 via the PCLK pin.

Bits 2 and 1 allow the user to divide CLK by an integer value to generate PCLK (00 = 1, 01 = 2, 10 = 4, 11 = 8).

MICROPORT CONTROL

The AD6634 has an 8-bit microprocessor port and a serial control port. The use of each of these ports is described separately below. The interaction of the ports is then described. The microport interface is a multimode interface that is designed to give flexibility when dealing with the host processor. There are two modes of bus operation: Intel Nonmultiplexed mode (INM), and Motorola Nonmultiplexed mode (MNM). The mode is selected based on host processor and which mode is best suited to that processor. The microport has an 8-bit databus(D[7:0]), 3-bit address bus(A[2:0]), three control pins lines ($\overline{CS}$, $\overline{DS}$, or $\overline{RD}$, RW or $\overline{WR}$), and one status pin (DTACK or RDY). The functionality of the control signals and status line changes slightly depending upon the mode that is chosen. Refer to the timing diagrams and the following descriptions for details on the operation of both modes.

External Memory Map

The External Memory Map is used to gain access to the channel address space described previously. The 8-bit data and address buses are used to this set of eight registers that can be seen in Table XVI. These registers are collectively referred to as the External Interface registers since they control all accesses to the Channel Address space as well as input/output control registers. The use of each of these individual registers is described in detail. It should be noted that the Serial Control interface has the same memory map as the microport interface and can carry out the exact same functions, although at a slower rate.

Access Control Register (ACR)

The Access Control register serves to define the channel or channels that receive an access from the microport or serial port control.

Bit 7 of this register is the Auto-Increment bit. If this bit is a 1, the CAR register described below will increment its value after every access to the channel. This allows blocks of address space such as coefficient memory to be initialized more efficiently.

Bit 6 of the register is the Broadcast bit and determines how Bits 5–2 are interpreted. If Broadcast is 0, then Bits 5–2, which are referred to as Instruction bits (Instruction[3:0]), are compared with the CHIP_ID[3:0] pins. The instruction that matches the CHIP_ID[3:0] pins will determine the access. This allows up to 16 chips to be connected to the same port and memory mapped without external logic. This also allows the same serial port of a host processor to configure up to 16 chips. If the Broadcast bit is high, the Instruction[3:0] word allows multiple AD6634 channels and/or chips to be simultaneously configured independent of the CHIP_ID[3:0] pins. There are 10 possible instructions defined in Table XVI. This is useful for smart antenna systems, where multiple channels listing to a single antenna or carrier can be configured simultaneously. The x(s) in the table represent don't cares in the digital decoding.

Table XVI. External Memory Map

A[2:0]	Name	Comment
111	Access Control Register (ACR)	7: Auto Increment 6: Broadcast 5–2: Instruction[3:0] 1–0: A[9:8]
110	Channel Address Register (CAR)	7–0: A[7:0]
101	SOFT_SYNC Control Register (Write Only)	7: PN_EN 6: Test_MUX_Select 5: Hop 4: Start 3: SYNC D 2: SYNC C 1: SYNC B 0: SYNC A
100	PIN_SYNC Control Register (Write Only)	7: Toggle IEN for BIST 6: First SYNC Only 5: Hop_En 4: Start_En 3: SYNC_EN D 2: SYNC_EN C 1: SYNC_EN B 0: SYNC_EN A
011	SLEEP (Write Only)	7–6: Reserved 5: Access Input/Output Control Registers 4: Reserved low 3: SLEEP 3 2: SLEEP 2 1: SLEEP 1 0: SLEEP 0
010	Data Register 2 (DR2)	7–4: Reserved 3–0: D[19:16]
001	Data Register 1 (DR1)	15–8: D[15:8]
000	Data Register 0 (DR0)	7–0: D[7:0]

Table XVII. Microport Instructions

Instruction	Comment
0000	All chips and all channels will get the access.
0001	Channel 0, 1, 2 of all chips will get the access.
0010	Channel 1, 2, 3 of all chips will get the access.
0100	All chips will get the access.*
1000	All chips with Chip_ID[3:0] = xxx0 will get the access.*
1001	All chips with Chip_ID[3:0] = xxx1 will get the access.*
1100	All chips with Chip_ID[3:0] = xx00 will get the access.*
1101	All chips with Chip_ID[3:0] = xx01 will get the access.*
1110	All chips with Chip_ID[3:0] = xx10 will get the access.*
1111	All chips with Chip_ID[3:0] = xx11 will get the access.*

*A[9:8] bits control which channel is decoded for the access.

When broadcast is enabled (Bit 6 set high), readback is not valid because of the potential for internal bus contention. Therefore, if readback is subsequently desired, the broadcast bit should be set low.

Bits 1–0 of this register are address bits that decode which of the four channels are being accessed. If the Instruction bits decode an access to multiple channels then these bits are ignored. If the instruction decodes an access to a subset of chips, then the A[9:8] bits will otherwise determine the channel being accessed.

Channel Address Register (CAR)
This register represents the 8-bit internal address of each channel. If the Auto-Increment bit of the ACR is 1, this value will be incremented after every access to the DR0 register, which will in turn access the location pointed to by this address. The Channel Address register cannot be read back while the Broadcast bit is set high.

SOFT_SYNC Control Register
External Address [5] is the SOFT_SYNC control register and is write only.

Bits 0–3 of this register are the SOFT_SYNC control bits. These pins may be written to by the controller to initiate the synchronization of a selected channel. Although there are four inputs, these do not necessarily go to the channel of the same number. This is fully configurable at the channel level as to which bit to look at. All four channels may be configured to synchronize from a single position, or they may be paired or all independent.

Bit 4 determines if the synchronization is to apply to a chip start. If this bit is set, a chip start will be initiated.

Bit 5 determines if the synchronization is to apply to a chip hop. If this bit is set, the NCO frequency will be updated when the SOFT_SYNC occurs.

Bit 6 configures how the internal databus is configured. If this bit is set low, the internal ADC databuses are configured normally. If this bit is set, the internal test signals are selected. The internal test signals are configured in Bit 7 of this register.

Bit 7 if set clear, a negative full scale signal is generated and made available to the internal databus. If this bit is high, internal pseudo-random sequence generator is enabled and this data is available to the internal databus. The combined functions of Bits 6 and 7 facilitate verification of a given filter design. Also, in conjunction with the MISR registers allows for detailed in-system chip testing. In conjunction with the JTAG test board, very high levels of chip verification can be done during system test, both in the factory and field.

PIN_SYNC Control Register
External Address [4] is the PIN_SYNC control register and is write only.

Bits 0–3 of this register are the SYNC_EN control bits. These pins may be written to by the controller to allow pin synchronization of a selected sync channel. Although there are four inputs, these do not necessarily go to the channel of the same number. This is fully configurable at the channel level as to which bit to look at. All four channels may be configured to synchronize from a single position, or they may be paired or all independent.

Bit 4 determines if the synchronization is to apply to a chip start. If this bit is set, a chip start will be initiated when the PIN_SYNC occurs.

Bit 5 determines if the synchronization is to apply to a chip hop. If this bit is set, the NCO frequency will be updated when the when the PIN_SYNC occurs.

Bit 6 is used to ignore repetitive synchronization signals. In some applications, this signal may occur periodically. If this bit is clear, each PIN_SYNC will restart/hop the channel. If this bit is set, only the first occurrence will cause the chip to take action.

Bit 7 is used with Bits 6 and 7 of external address 5. When this bit is cleared, the data supplied to the internal databus simulates a normal ADC. When this bit is set, the data supplied is in the form of a time multiplexed ADC such as the AD6600 (this allows the equivalent of testing in the 4-channel input mode). Internally, when set, this bit forces the IEN pin to toggle as if it were driven by the A/B signal of the AD6600.

SLEEP Control Register
External Address [3] is the Sleep register.

Bits 3–0 control the state of each of the channels. Each bit corresponds to one of the possible RSP channels within the device. If this bit is cleared, the channel operates normally. However, when this bit is set, the indicated channel enters a low power Sleep mode.

Bit 4 is reserved and should always be set to 0.

Bit 5 allows access to the Input/Output Control Port Registers. When this bit is set low, the channel memory map is accessed. However, when this bit is set high, it allows access to the Input/Output Port Control Registers. When this bit is set high, the value in external address 6 (CAR) points to the memory map for the Input/Output Port Control Registers instead of the normal channel memory map. See Input and Output Port Control Registers in the respective Input and Output memory map sections.

Bits 6–7 are reserved and should be set low.

Data Address Registers
External Address [2–0] forms the data registers DR2, DR1, and DR0, respectively. All internal data-words have widths that are less than or equal to 20 bits. Accesses to External Address [0] DR0 trigger an internal access to the AD6634 based on the address indicated in the ACR and CAR. Thus during writes to the internal registers, External Address [0] DR0 must be written last. At this point data is transferred to the internal memory indicated in A[9:0]. Reads are performed in the opposite direction. Once the

address is set, External Address [0] DR0 must be the first data register read to initiate an internal access. DR2 is only four bits wide. Data written to the upper four bits of this register will be ignored. Likewise reading from this register will produce only 4 LSBs.

Write Sequencing
Writing to an internal location is achieved by first writing the upper two bits of the address to Bits 1 through 0 of the ACR. Bits 7:2 may be set to select the channel as indicated above. The CAR is then written with the lower eight bits of the internal address (it doesn't matter if the CAR is written before the ACR as long as both are written before the internal access). Data Register 2 (DR2) and Register 1 (DR1) must be written first because the write to data register DR0 triggers the internal access. Data register DR0 must always be the last register written to initiate the internal write.

Read Sequencing
Reading from the microport is accomplished in the same manner. The internal address is set up the same way as the write. A read from data register DR0 activates the internal read, thus register DR0 must always be read first to initiate an internal read followed by DR1 and DR2. This provides the 8 LSBs of the internal read through the microport (D[7:0]). Additional data registers can be read to read the balance of the internal memory.

Read/Write Chaining
The microport of the AD6634 allows for multiple accesses while $\overline{CS}$ is held low ($\overline{CS}$ can be tied permanently low if the microport is not shared with additional devices). The user can access multiple locations by pulsing the $\overline{WR}$ or $\overline{RD}$ line and changing the contents of the external 3-bit address bus. External access to the external registers of Table XIII is accomplished in one of two modes using the $\overline{CS}$, $\overline{RD}$, $\overline{WR}$, and MODE inputs. The access modes are Intel nonmultiplexed mode and Motorola nonmultiplexed mode. These modes are controlled by the MODE input (MODE = 0 for INM, MODE = 1 for MNM). $\overline{CS}$, $\overline{RD}$, and $\overline{WR}$ control the access type for each mode.

Intel Nonmultiplexed Mode (INM)
MODE must be tied Low to operate the AD6634 microprocessor in INM mode. The access type is controlled by the user with the $\overline{CS}$, $\overline{RD}$ ($\overline{DS}$), and $\overline{WR}$ (RW) inputs. The RDY ($\overline{DTACK}$) signal is produced by the microport to communicate to the user that an access has been completed. RDY ($\overline{DTACK}$) goes Low at the start of the access and is released when the internal cycle is complete. See the timing diagrams for both the read and write modes in the Specifications.

Motorola Nonmultiplexed Mode (MNM)
MODE must be tied High to operate the AD6634 microprocessor in MNM mode. The access type is controlled by the user with the $\overline{CS}$, $\overline{DS}$ ($\overline{RD}$), and RW ($\overline{WR}$) inputs. The $\overline{DTACK}$ (RDY) signal is produced by the microport to communicate to the user that an access has been completed. $\overline{DTACK}$ (RDY) goes Low when an internal access is complete and then will return High after $\overline{DS}$ ($\overline{RD}$) is deasserted. See the timing diagrams for both the read and write modes in the Specifications.

SERIAL PORT CONTROL

The AD6634 has a serial port serving as a control interface apart from the microport control interface. Serial port input pin (SDI) can access all of the internal registers for all of the channels and has pre-emptive access over the microport. In this manner, a single DSP could be used to control the AD6634 over the serial port control interface.

The serial control port uses the serial clock (SCLK). The serial input port is self-framing as described below and allows more efficient use of the serial input bandwidth for programming. The beginning of a serial input frame is signaled by a Frame bit that appears on the SDI pin. This is the MSB of the Serial Input frame. After the frame bit has been sampled high on the falling edge of SCLK, a state counter will start and enable an 11-bit serial shifter four serial clock cycles later. These four SCLK cycles represent the Don't Care bits of the serial frame that are ignored. After all of the bits are shifted, the serial input port will pass along the 8-bit data and 3-bit address to the arbitration block.

The serial word structure for the SDI input is illustrated in Figure 47. Only 15 bits are listed so that the second bit in a standard 16-bit serial word is considered the frame bit. This is done for compatibility with the AD6620 serial input port. The shifting order begins with frame and shifts the address MSB first and then the data MSB first.

Serial Port Timing Specifications
The AD6634 serial control channel can operate only in the slave mode. Figures 44–46 indicate the required timing for each specification.

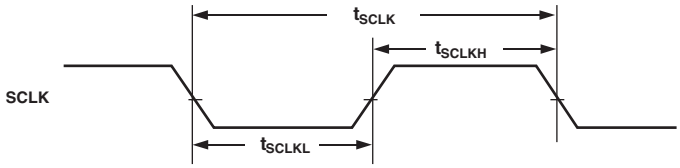


Figure 44. SCLK Timing Requirements

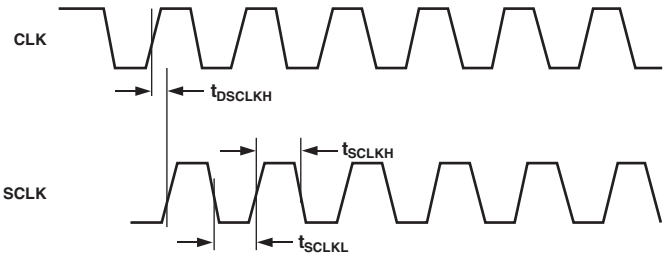


Figure 45. SCLK Switching Characteristics (Divide by 1)

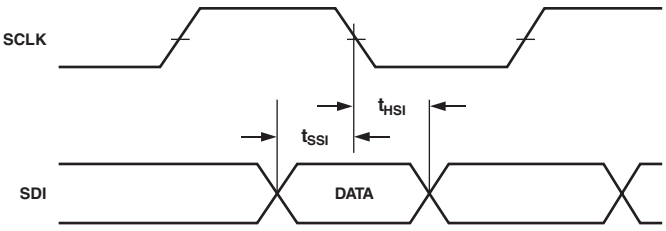


Figure 46. Serial Input Data Timing Requirements

SDI
SDI is the Serial Data Input. Serial Data is sampled on the falling edge of SCLK. This pin is used in the serial control mode to write the internal control registers of the AD6634.

SCLK
SCLK is a clock input and the SDI input is sampled on the falling edge of SCLK and all outputs are switched on the rising edge of SCLK. The maximum speed of this port is 80 MHz.

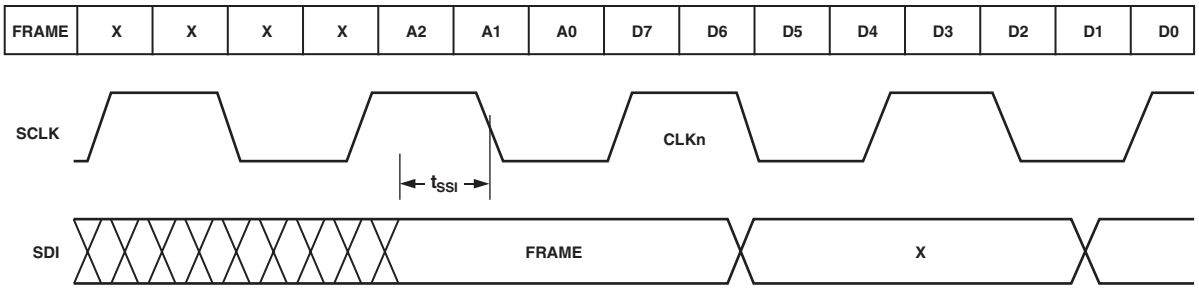


Figure 47. Serial Word Structure and Serial Port Control Timing

JTAG BOUNDARY SCAN

The AD6634 supports a subset of IEEE Standard 1149.1 specification. For additional details of the standard, please see "IEEE Standard Test Access Port and Boundary-Scan Architecture," IEEE-1149 publication from IEEE.

The AD6634 has five pins associated with the JTAG interface. These pins are used to access the on-chip Test Access Port and are listed in Table XVIII. All input JTAG pins are pull-up except for TCLK, which is a pull-down.

Table XVIII. Boundary Scan Test Pins

Name	Pin Number	Description
$\overline{\text{TRST}}$	67	Test Access Port Reset
TCLK	68	Test Clock
TMS	69	Test Access Port Mode Select
TDI	72	Test Data Input
TDO	70	Test Data Output

The AD6634 supports six op codes as shown in Table XIX. These instructions set the mode of the JTAG interface.

Table XIX. Boundary Scan Op Codes

Instruction	Op Code
IDCODE	001
BYPASS	111
SAMPLE/PRELOAD	010
EXTEST	000
HIGHZ	011
CLAMP	100

The Vendor Identification Code can be accessed through the IDCODE instruction and has the format shown in Table XX.

Table XX. Vendor ID Code

MSB Version	Part Number	Manufacturing ID #	LSB Mandatory
0000	0010 0111 1000 1100	000 1110 0101	1

A BSDL file for this device is available. Please contact Analog Devices for more information.

EXTEST (3'b000)—Places the IC into an external boundary-test mode and selects the boundary-scan register to be connected between TDI and TDO. During this, the boundary-scan register is accessed to drive test data off-chip via boundary outputs and receive test data off-chip from boundary inputs.

IDCODE (3'b001)—Allows the IC to remain in its functional mode and selects device ID register to be connected between TDI and TDO. Accessing the ID register does not interfere with the operation of the IC.

SAMPLE/PRELOAD (3'b010)—Allows the IC to remain in normal functional mode and selects the boundary-scan register to be connected between TDI and TDO. The boundary-scan register can be accessed by a scan operation to take a sample of the functional data entering and leaving the IC. Also, test data can be preloaded into the boundary scan register before an EXTEST instruction.

HIGHZ (3'b011)—Sets all outputs to high impedance state. Selects 1-bit bypass register to be connected between TDI and TDO.

CLAMP (3'b100)—Sets the outputs of the IC to logic levels determined by the boundary-scan register and selects 1-bit bypass register to be connected between TDI and TDO. Before this instruction, boundary-scan data can be preloaded with the SAMPLE/PRELOAD instruction.

BYPASS (3'b111)—Allows the IC to remain in normal functional mode and selects 1-bit bypass register between TDI and TDO. During this instruction, serial data is transferred from TDI to TDO without affecting operation of the IC.

INTERNAL WRITE ACCESS

Up to 20 bits of data (as needed) can be written by the process described below. Any high order bytes that are needed are written to the corresponding data registers defined in the external 3-bit address space. The least significant byte is then written to DR0 at address (000). When a write to DR0 is detected, the internal microprocessor port state machine then moves the data in DR2–DR0 to the internal address pointed to by the address in the LAR and AMR.

Write Pseudocode

```
void write_micro(ext_address, int data);

main();

{

/* This code shows the programming of the NCO phase offset
register using the write_micro function as defined above. The
variable address is the External Address A[2:0] and data is the
value to be placed in the external interface register.
```

```
Internal Address = 0x087
 */

// holding registers for NCO phase byte wide access data
int d1, d0;

// NCO frequency word (16-bits wide)
NCO_PHASE = 0xCBEF;

// write ACR
write_micro(7, 0x03 );

// write CAR
write_micro(6, 0x87);

// write DR1 with D[15:8]
d1 = (NCO_PHASE & 0xFF00) >> 8;
write_micro(1, d1);

// write DR0 with D[7:0]
// On this write all data is transferred to the internal address
d0 = NCO_FREQ & 0xFF;
write_micro(0, d0);
} // end of main
```

INTERNAL READ ACCESS

A read is performed by first writing the CAR and AMR as with a write. The data registers (DR2–DR0) are then read in the reverse order that they were written. First, the Least Significant Byte of the data (D[7:0]) is read from DR0. On this transaction the high bytes of the data are moved from the internal address pointed to by the CAR and AMR into the remaining data registers (DR2–DR1). This data can then be read from the data registers using the appropriate 3-bit addresses. The number of data registers used depends solely on the amount of data to be read or written. Any unused bit in a data register should be masked out for a read.

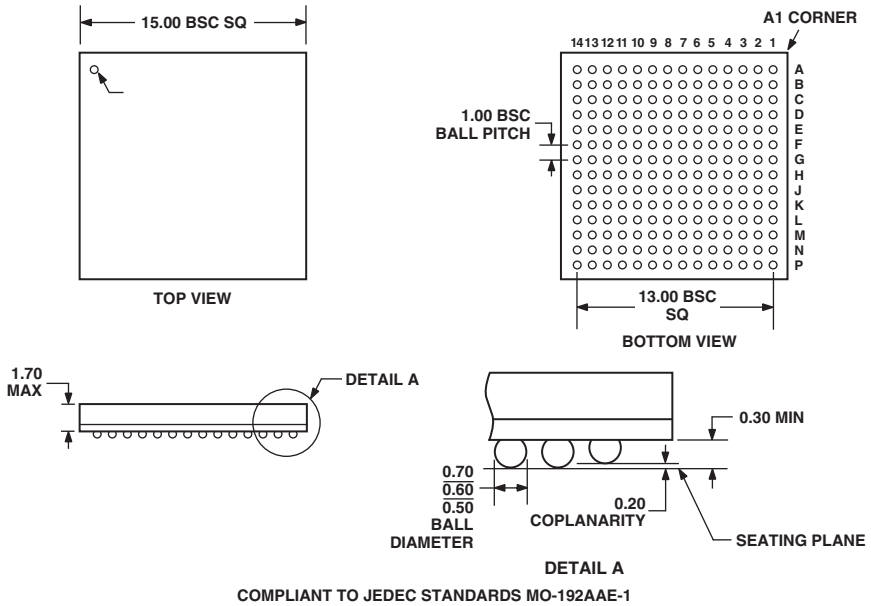
Read Pseudocode

```
int read_micro(ext_address);

main();

{

/* This code shows the reading of the first RCF coefficient
using the read_micro function as defined above. The variable
address is the External Address A[2..0].

Internal Address = 0x000
 */

// holding registers for the coefficient
int d2, d1, d0;

// coefficient (20-bits wide)
long coefficient;

// write AMR
write_micro(7, 0x00 );

// write LAR
write_micro(6, 0x00);

/* read D[7:0] from DR0. All data is moved from the Internal
Registers to the interface registers on this access.
*/

d0 = read_micro(0) & 0xFF;

// read D[15:8] from DR1
d1 = read_micro(1) & 0xFF;

// read D[23:16] from DR2
d2 = read_micro(2) & 0x0F;

coefficient = d0 + (d1 << 8) + (d2 << 16);

} // end of main
```

OUTLINE DIMENSIONS

196-Lead Chip Scale Ball Grid Array [CSPBGA]
(BC-196)

Dimensions shown in millimeters



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