AN11037

LDO voltage regulators: fundamentals, topologies and parameters

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Document information

Info	Content
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Abstract	This application note illustrates the fundamentals of NXP LDO voltage regulators and explains their main parameters

Revision history

Rev	Date	Description
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Contact information

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1. Introduction

A Low DropOut voltage regulator (LDO) reduces a DC input voltage to a specific DC output voltage. This application note illustrates the fundamentals and topologies of voltage regulators and explains their main parameters.

2. Fundamentals of low dropout voltage regulators

A typical LDO, as illustrated in Figure 1, includes pass element, resistors, overcurrent protection, voltage reference generator, thermal protection, feedback divider and error amplifier.

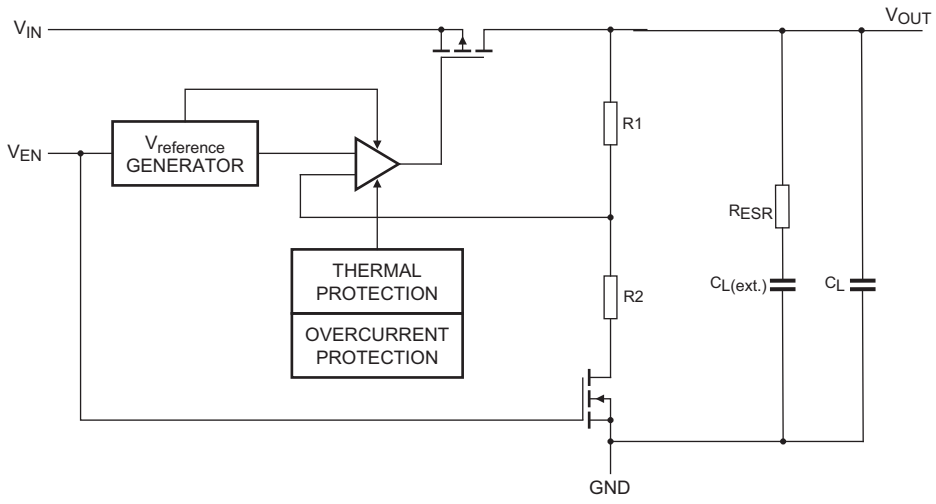


Fig 1. Schematic LDO

To simplify: An LDO (R_{LDO}) and a load (R_L) describe a setup of a resistor divider (see Figure 2, left side). The LDO behaves like an adjustable resistor (R_{LDO}) which compensates the load change as well as source variations. The load (R_L) is also described as adjustable because it can be a system with a dynamic power consumption. The target of an LDO is to keep the output voltage (V_{OUT}) constant.

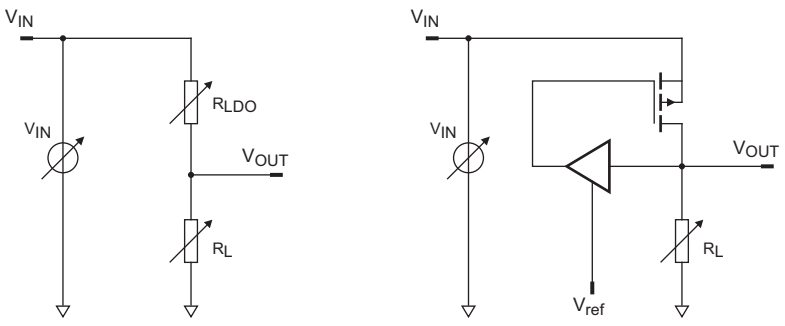


Fig 2. Simplified low dropout voltage regulator

The left schematic of Figure 2 describes the voltage divider which allows to calculate the output voltage of an LDO.

$$V_{OUT} = V_{IN} \times R_L / (R_L + R_{LDO}) \quad (1)$$

In order to keep the output voltage stable, R_{LDO} has to change in function of R_L. For an accurate output voltage, the output node must be control by itself. Therefore a pass element plus an error amplifier replace the R_{LDO}.

A feedback path tracks the output voltage via a resistor divider. The signal is compared with a reference voltage, which is part of an LDO. The error amplifier adjusts the pass element (see Figure 2 right).

2.1 Difference between bipolar and MOS pass element

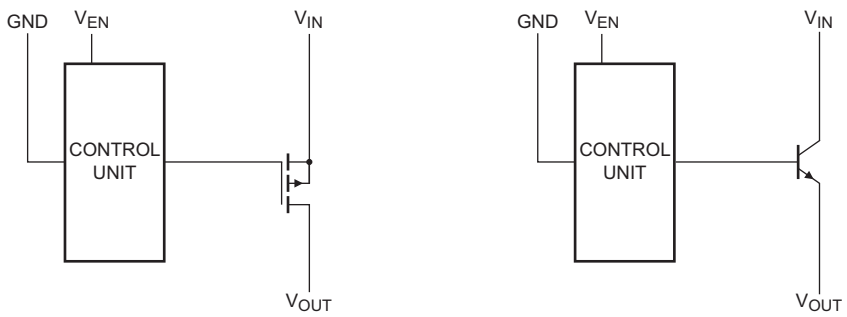


Fig 3. Simplified low dropout voltage regulator

There are two kinds of pass elements for an LDO (Figure 3): a bipolar and a MOS transistor. Each architecture has an impact on dropout voltage, quiescent current, and the overall performance.

The bipolar transistor is current-driven by the base current which is proportional to the collector current. The MOS element is gate voltage driven. It means that most bipolar regulators have a higher ground current. Modern bipolar systems are often used for applications greater 5 V and for higher current ratings if ground current is negligible.

Voltage regulators with MOS pass elements allow a low voltage drop and can be optimized for ground current. For example, for mobile phones with a battery. Here the input voltage decreases after discharging the battery, nevertheless the output voltage has to be stable. MOS devices realize an on-resistance less than 0.1 Ω and a dropout voltage less than 80 mV.

3. Dropout Voltage

3.1 Description

The dropout voltage is the smallest input to output voltage difference at a specific current when the pass transistor works as a simple resistor.

For instance, an LDO has a PMOS pass element. The dropout voltage is equivalent to the drain-source voltage of the PMOS. The minimum dropout voltage of the LDO at a certain current is always limited by the PMOS / pass element output characteristic (see Figure 4).

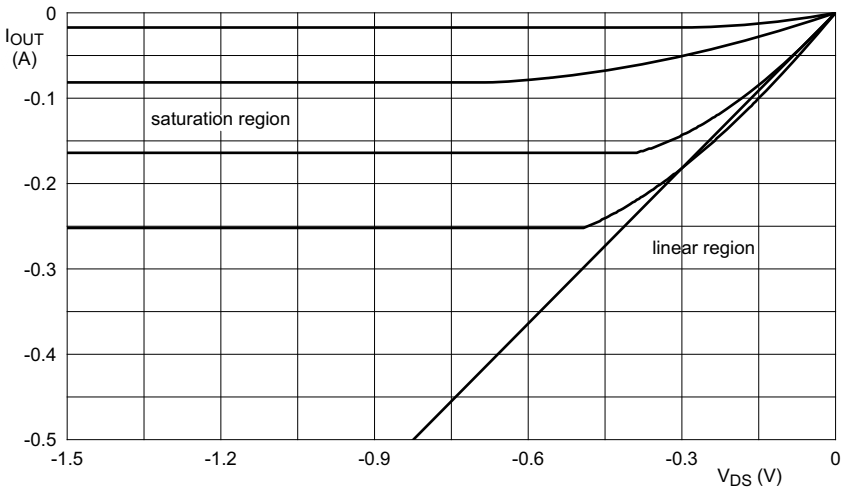


Fig 4. Typical output characteristic of a PMOS

If the input voltage of an LDO is higher than the output voltage, the error amplifier and gate driver force the gate of a pass transistor. As shown in Figure 4, the device operates in the saturation region. If the input voltage is near the nominal output voltage, the pass element works in the linear region. The pass element is limited by its on-resistance.

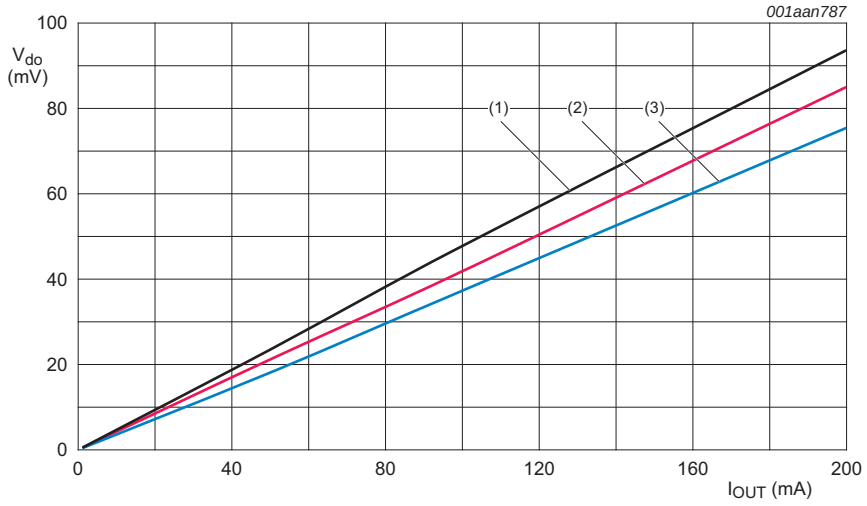
A small dropout voltage value guaranties possible lower power consumption and maximizes the efficiency.

3.2 Data sheet values

In a data sheet, the dropout voltage is often described in two ways. The first one is only a value at a certain current (Table 1 operation point). The second one (Figure 5) is a characteristic of the dropout voltage in dependency of the output current for different temperatures.

Table 1. Dropout voltage LD6806CX4/25H

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{do}	dropout voltage	I_{OUT} = 200 mA; $V_{IN} > V_{O(nom)}$	-	60	100	mV



(1) T_{amb} = +85 °C
(2) T_{amb} = +25 °C
(3) T_{amb} = −40 °C

Fig 5. Dropout voltage over temperature LD6806CX4/25H

Figure 6 can be used for both test setups. The dropout voltage over temperature describes the NXP LD6806 under the test conditions from Table 2.

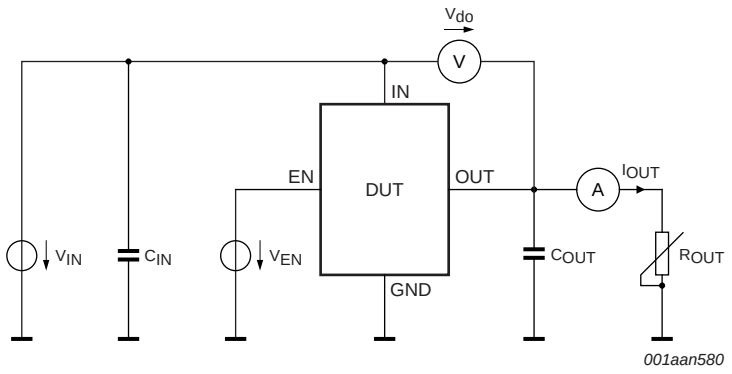


Fig 6. Dropout voltage measurement circuit

Table 2. LD6806: Dropout voltage test conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IN}	voltage on pin IN		0	-	5.5	V
V_{EN}	voltage on pin EN		-	1.4	-	V
C_{IN}	input capacitance	case 0603 X5R	-	1	-	µF
C_{OUT}	output capacitance	case 0603 X5R	-	1	-	µF
I_{OUT}	current on pin OUT		-	200	-	mA

To use an LDO in a non-constant current mode, estimate the voltage dropout from Figure 5 or estimate the voltage drop as rude estimation:

$$Dropout\ voltage = V_{do(typ)} \div I_{OUT} \times load\ current \quad (2)$$

4. Efficiency, quiescent current and standby current

4.1 Description

Quiescent or ground current, is the difference between input and output current. It describes the current which the LDO consumes by itself. A low quiescent current I_q improves the current efficiency of an LDO.

$$I_q = I_{IN} - I_{OUT} \quad (3)$$

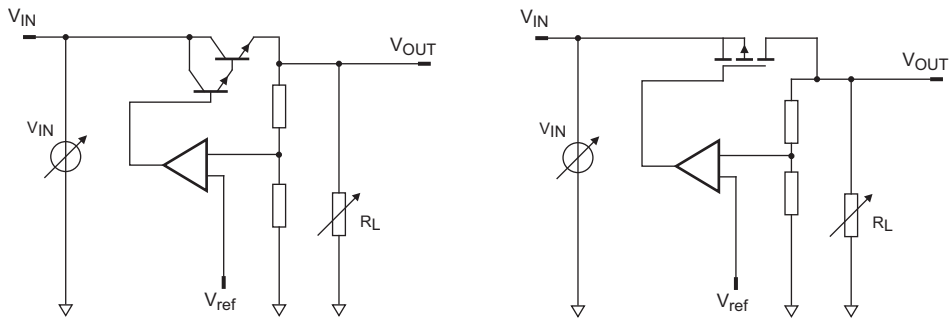


Fig 7. Difference ground current caused by bipolar or MOS pass elements

The quiescent current depends on the topology of an LDO. It is the sum of internal current sinks like, for example, band gap, error amplifier, resistor divider, pass element and drivers.

The LDO topologies from Figure 7 can theoretical have the same ground current when the load is 0 mA. When the load current increases, the MOS topology has a nearly linear increasing current consumption but the bipolar setup is not linear. The LDO with MOS device has only to drive the gate of MOS pass element. The main current depends on the resistor divider and the internal control logic.

As shown on the left side of Figure 7, an LDO with a bipolar pass element raises the quiescent current when the collector (load) current increases. This behavior is given by the base-current-driven pass element. Replacing the driver transistor against a

complementary driver transistor and implementing a current source would reduce the quiescent current. But in this case, the current consumption would be higher than for an equivalent MOS construction. The current consumption of both topologies is always a compromise of effort, cost and price.

The LDO efficiency is given by the equation:

$$LDO\ efficiency = \frac{V_{OUT} \times I_{OUT}}{V_{IN} \times (I_{OUT} + I_q)} \times 100\ \% \quad (4)$$

Both topologies have a standby current which is the current consumption of the device under no-load, when the LDO is disabled.

4.1.1 Data sheet values

A comparison of LDOs quiescent current from different manufacturers is difficult. In order to compare LDOs with different topologies, NXP data sheets offer static values of quiescent current (see Table 3) and a chart of quiescent current versus load.

Table 3. Example for regulator quiescent current from LD6806CX4/25H data sheet

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Load regulation error						
I_q	quiescent current [1]	V_{EN} = 1.4 V; I_{OUT} = 0 mA	-	70	100	µA
		V_{EN} = 1.4 V; 0 mA < I_{OUT} < 200 mA	-	155	250	µA
		V_{EN} < 0.4 V	-	-	1	µA

[1] Quiescent current is also called standby current or shut-down current.

Note: For devices with a battery, the quiescent current in Standby mode and under load is important. A lower quiescent current can increase charging cycles.

5. Output noise RMS (μV)

5.1 Description

The output noise voltage of an LDO circuit is the intrinsic noise of an LDO. The internal noise sources are amplifiers, transistors, resistors, and so on. Supplied circuits like analog to digital converters, voltage references or digital circuits can influence the noise.

Nowadays there are only few LDO concepts using some special features to reduce the noise. The simplest concept is to filter the reference voltage (band gap) with an additional external capacitor. This construction creates a low pass and smooths the reference voltage of the LDO. Another concept is to reduce the bandwidth of the error amplifier, but it also reduces the transient response. It is a trade-off between noise performance and the step response of an LDO.

Linear regulator data sheets typically give two noise values:

- noise spectral density curve: μV/√Hz as a function of frequency
- absolute result: μV-RMS over a defined frequency range (typically 10 Hz to 100 kHz)

The absolute value is the integration of the noise spectral density curve over the bandwidth.

5.2 Data sheet values

The noise signal can be analyzed in the time or frequency domain. The time domain setups use an oscilloscope and the frequency domain utilizes a spectrum analyzer. Both setups are equivalent. Modern digital oscilloscopes allow noise calculation via a fast Fourier transformation. Using a spectrum or audio analyzer is the easiest way for measuring noise.

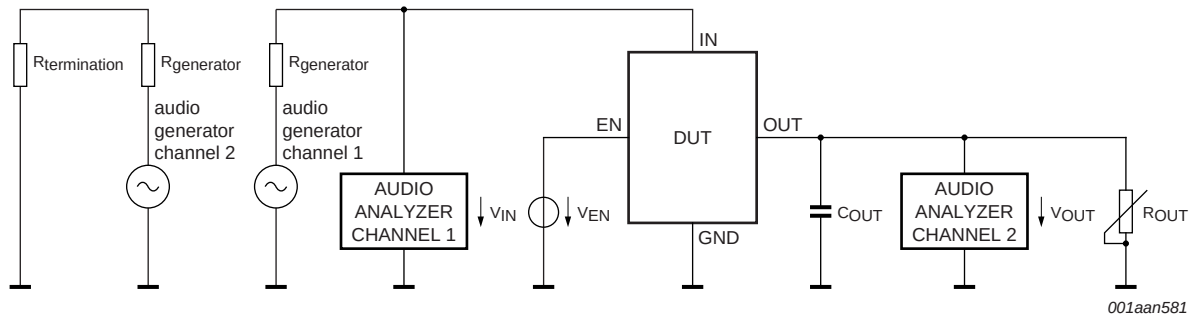


Fig 8. Noise measurement setup

The measurement setup typically consists of an audio analyzer (Figure 8) or a simple voltage supply for the regulator input and a spectrum analyzer for the output. A constant output current and a ripple-free input voltage constitute the measurement conditions. The noise generated by the LDO regulator becomes the output noise voltage.

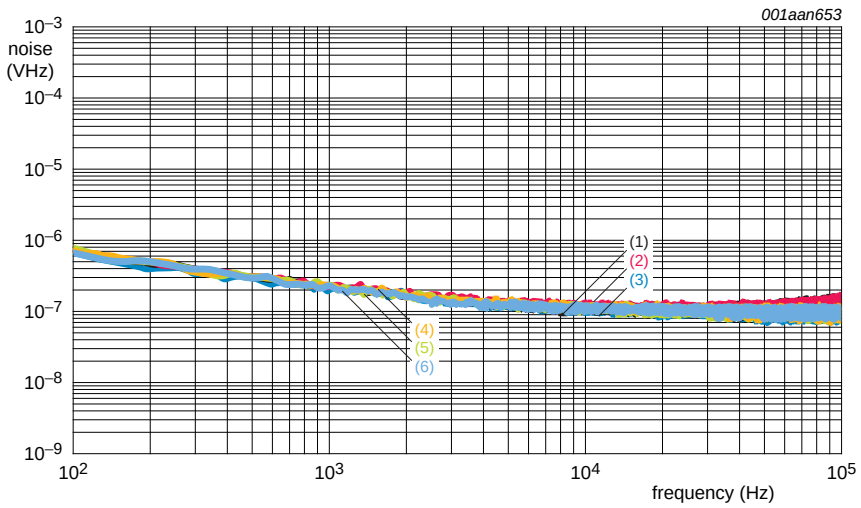
The NXP LD68xy family has a low output noise. The noise spectral density curve (Figure 9) is measured with the setup illustrated on Figure 8 and the conditions from Table 4. Out of it, it is possible to calculate the root mean square value of Table 5.

Table 4. Test conditions for output noise test

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IN}	voltage on pin IN		0	-	5.5	V
V_{EN}	voltage on pin EN		-	1.4	-	V
C_{IN}	input capacitance	case 0603 X5R	-	1	-	µF
C_{OUT}	output capacitance	case 0603 X5R	-	1	-	µF
I_{OUT}	current on pin OUT		-	200	-	mA

Table 5. Example of output noise test conditions for output noise test

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{n(o)RMS}$	RMS output noise voltage	bandwidth 10 Hz to 100 kHz; C_{OUT} = 1 µF	-	30	-	µV



(1) I_{OUT} = 0 mA
(2) I_{OUT} = 1 mA
(3) I_{OUT} = 50 mA
(4) I_{OUT} = 100 mA
(5) I_{OUT} = 150 mA
(6) I_{OUT} = 200 mA

Fig 9. Noise density test result for LD6806CX4/25H

6. Power Supply Rejection Ratio (PSRR)

6.1 Description for PSRR

Power supply rejection ratio (PSRR) stands for the ratio of output noise to input noise at various frequencies. In other words, it is the capability of the regulator to suppress unwanted signals from the input to the output.

$$PSRR\ (\text{dB}) = 20log\frac{V_{(o)ripple}}{V_{(in)ripple}} \quad (5)$$

The PSRR is important for radio-frequency-sensitive applications. Noise or ripples of a supply, an improper PCB layout or a DC-to-DC converter which produces unwanted input voltage variations have to be filtered by an LDO.

There are two ways to measure PSRR. The first one is to use a digital oscilloscope and the second one is to use a network analyzer with two high impedance probes. The PSRR test setup (Figure 10) consists of a network analyzer which includes a pattern generator and high-ohmic probes, a preamplifier, a DC source and load. The pattern generator forces a sinus signal into a preamplifier and the output signal is mixed with a DC signal and forced into the LDO. The input and output voltage are measured with high impedance probes. The analyzer allows the deviation of the input and output voltage and describes the PSRR Figure 11.

As an advantage the network analyzer allow accurate measurements and can measure PSRR values greater than 100 dB. A state-of-the-art digital oscilloscope has a regulation down to millivolts allowing only a maximum PSRR measurement of about 65 dB. This measurement is not enough for high-performance LDOs in mobile application.

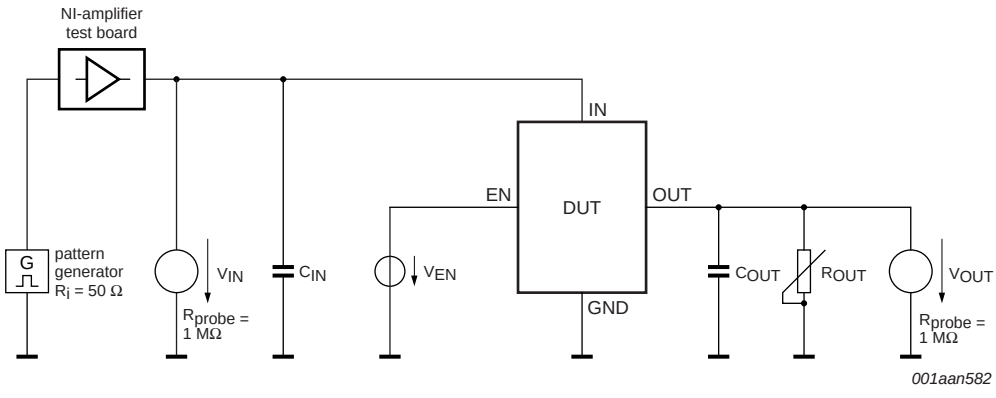


Fig 10. PSRR measurement circuit

6.2 Data sheet values

Considering the PSRR values in data sheets of different manufacturers, it is difficult to establish an exact comparison. The output capacitor has a huge influence on the PSRR performance. For low voltage applications, an output capacitor of 1 μF is often recommended. A bigger capacitance suppresses the output ripple and increases the PSRR value. Also an input voltage ripple has impact on the PSRR value. If the amplitude is reduced at the input, the PSRR value increases.

Today most LDOs have a proper PSRR performance in the lower frequency range but at high frequencies of about 1 MHz the PSRR decreases rapidly. PSRR is given by the topology of the LDO. More and more DC-to-DC converters increase the switching frequency from kHz to MHz. Digital circuits like microcontrollers create noise due to fast switching in the MHz range. For these reasons, there is more demand of LDOs with a better PSRR performance in the range above 1 MHz to protect sensitive Radio Frequency (RF) applications.

See Table 6 for typical test conditions for low voltage LDOs:

Table 6. LD68xy family: Test conditions for PSRR

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IN}	voltage on pin IN		0	-	5.5	V
V_{EN}	voltage on pin EN		-	1.4	-	V
C_{IN}	input capacitance	case 0603 X5R	-	1	-	μF
C_{OUT}	output capacitance	case 0603 X5R	-	1	-	μF
R_{OUT}	load on pin OUT		-	13	-	Ω
I_{OUT}	current on pin OUT		-	200	-	mA

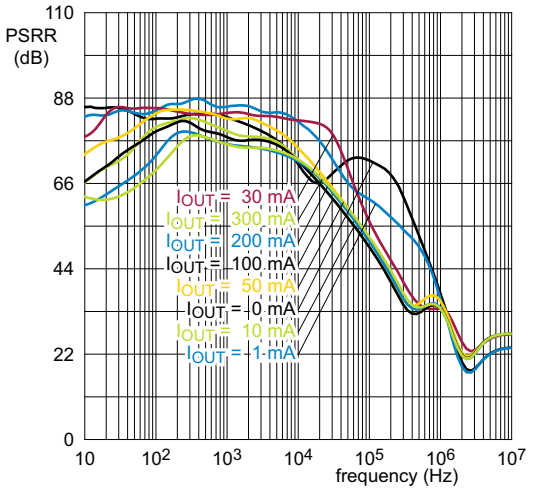


Fig 11. LD6835K/33H: Power supply rejection ratio

7. Start-up time, soft start, inrush current limiter and shut-down time

7.1 Description

Start-up time defines the time which the LDO needs for achieving 95 % of its typical output voltage level after activation via the enable pin.

For example, an LDO with a fast turn-on time and a heavy load can cause a voltage dip on the input. During the start-up time, the inrush current can exceed the maximum peak current of the LDO. This behavior depends on the capacitive and resistive load. In order to prevent peak current and massive voltage dips at the input for sensitive sources (for example, base bands in mobile phone), an inrush current limiter or soft-start circuit can be implemented into an LDO.

The soft start describes the dedicated start-up of integrated LDO elements (pass element, error amplifier and bang gap) step-by-step. This mode limits the inrush current to a certain level until the output voltage is raised. However the peak current depends on the load. An inherent inrush current limiter is used to limit inrush current and not to start softly. This limiter avoids excessive current when a power supply or the LDO is turned on independently from the load. It prevents damaging the connected circuits and eliminates voltage dips at the LDO input.

The shut-down time is the time which the LDO needs for reducing the output voltage to 10 % of the nominal output voltage after deactivating the enable pin. This parameter is massively influenced by the load capacitance as well as the load series resistance which is part of the discharge path. The test setup (Figure 12) can be used for all three parameters.

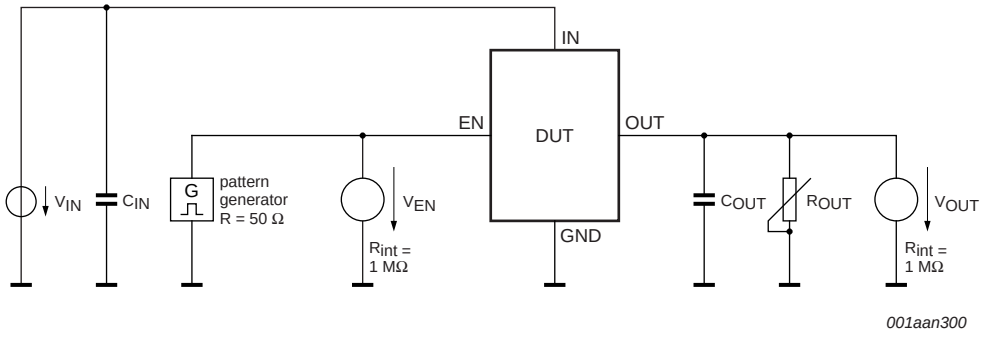


Fig 12. Enable response measurement circuit (start-up, soft start and shut-down)

7.2 Data sheet values

In most data sheets, the values are measured under maximum load condition. When comparing data sheets, take notice that some manufacturers do not use only a capacitor at the output (Figure 12) but also a resistive load. Only a resistive load leads to less inrush current peaks, influences the comparability and does not represent the reality of a circuit.

Table 7. Test conditions for enable response test

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IN}	voltage on pin IN		0	-	5.5	V
V_{EN}	voltage on pin EN		-	1.4	-	V
C_{IN}	input capacitance	case 0603 X5R	-	1	-	µF
C_{OUT}	output capacitance	case 0603 X5R	-	1	-	µF
I_{OUT}	current on pin OUT		-	200	-	mA

Table 7 shows the typical test conditions of start-up and shut-down time. Figure 13 and Figure 14 describe the test results measured with an oscilloscope.

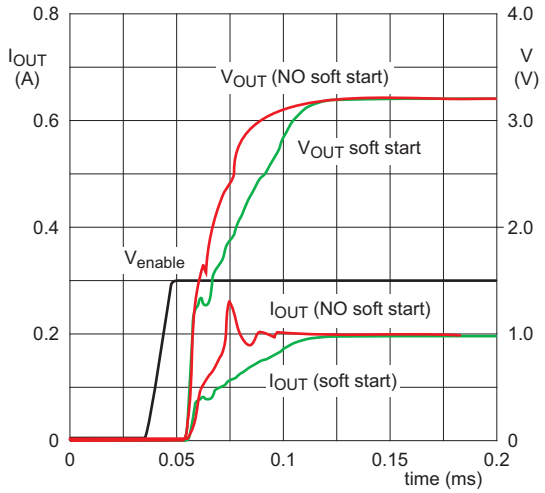
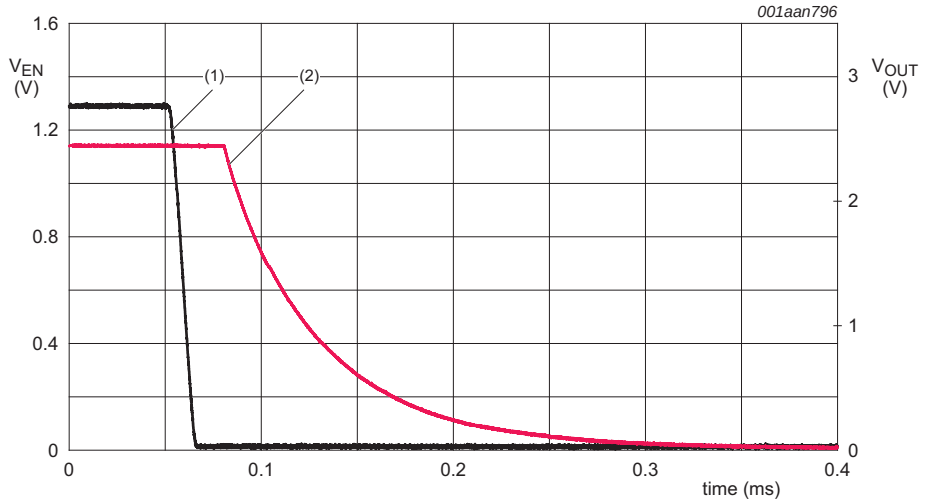


Fig 13. Comparison start-up behavior of an LDO with and without soft start



V_{IN} = 5 V; C_{IN} = 1 µF; C_{OUT} = 1 µF

(1) V_{EN}

(2) V_{OUT}

Fig 14. LD6806CX4/25H: Shut-down time

8. Delay circuit only for dual LDO

8.1 Description

The delay circuit prevents an unwanted input voltage dip of a dual LDO when both outputs are enabled at the same time. The circuit delays the second LDO when enabling both LDOs simultaneously until the first LDO is ready.

8.2 Data sheet values

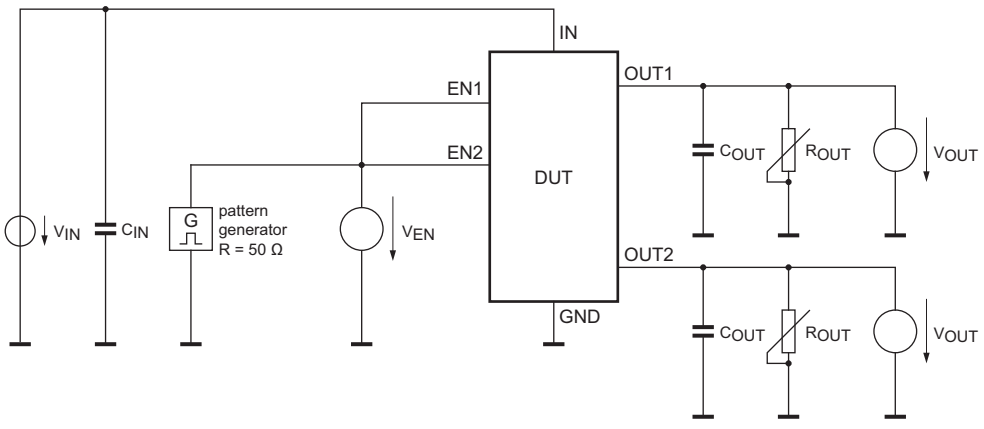


Fig 15. Delay circuit measurement setup

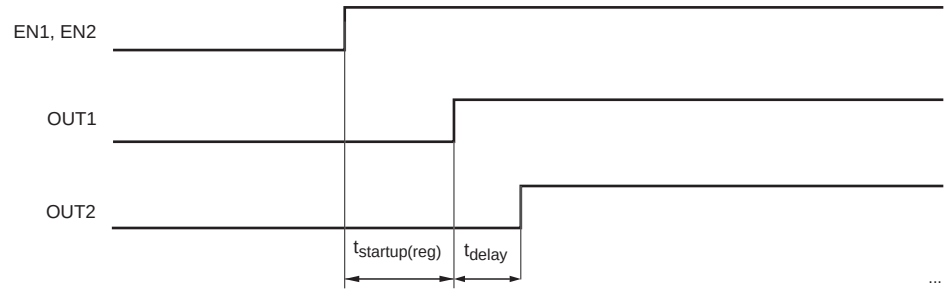


Fig 16. Delay timing of a dual LDO with delay circuit

9. Line transient and line regulation response

9.1 Description

The line transient response is the maximum output voltage variation for an input voltage step change.

$$Regulation[\%/V] = \frac{\Delta V_{OUT}}{\Delta V_{IN}} \times \frac{100}{V_{OUT}} \quad (6)$$

The line transient response can be caused by a disturbance, transient or a simple voltage change at the LDO input. The line response is often described in two ways. The first one is the static change, the second one the transient behavior. The static change is the delta between the output voltage at low input voltage and the output voltage at high input voltage. The transient behavior is the spike of the output voltage when the input voltage rises and falls from low to high and vice versa.

9.2 Data sheet values

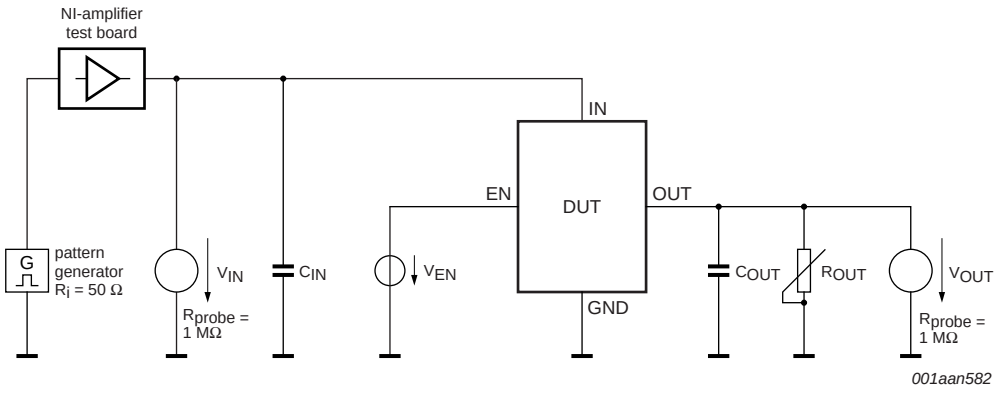


Fig 17. Line transient measurements setup

Table 8. Test conditions for line transient test

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IN}	voltage on pin IN		0	-	5.5	V
V_{EN}	voltage on pin EN		-	1.4	-	V
C_{IN}	input capacitance	case 0603 X5R	-	1	-	µF
C_{OUT}	output capacitance	case 0603 X5R	-	1	-	µF
I_{OUT}	current on pin OUT		-	200	-	mA

For example, the test setup (Figure 17) and the test conditions of Table 8 allow switching the input voltage for an LD6806CX4/12H LDO from 2.1 V to 5.5 V. The graphic Figure 18 shows the input voltage and the resulting output voltage. The output voltage curve illustrates two peaks and a delta. The transient response is the maximum positive or negative peak of 7 mV and the delta is the line regulation and increasing from 1.2 V to 1.23 V.

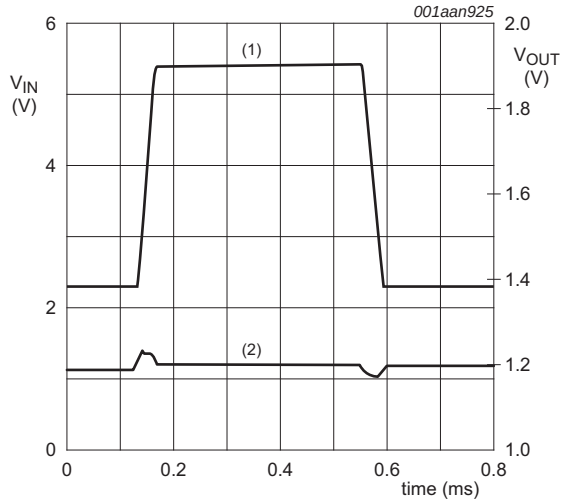


Fig 18. Line transient (rising and falling edge) test result for LD6806CX4/12H

10. Load transient response or load step response

10.1 Description

The load regulation and load transient response describe the maximum output voltage variation for an output load step change. The load transient response describes the maximum transient spikes at the output voltage when the load switches from low to high current and back. The load regulation response is more static and shown as delta between the output voltage before and after switching from low to high.

A load step response indicates conditional stability and allows testing an LDO with an output capacitor under different load conditions. Fast transient response is essential when a load switches between different operation modes quickly. The load change can dip temporarily the output voltage of the LDO. Some applications like digital circuits with low input voltage react sensitive to voltage dip. For this purpose NXP offers fast response LDOs like, for example, LD6835.

10.2 Data sheet values

The test setup (Figure 19) offers the maximum output voltage variation for an output load step change. The test is only an indication of stability because each LDO loop tends to start oscillation at the frequency where the loop gain is unity (0 dB). Unknown load condition can decrease the loop gain of an LDO or avoid reaching a stable operating point of the inherent LDO loop. So an application test is required.

Typical test conditions are given in Table 9.

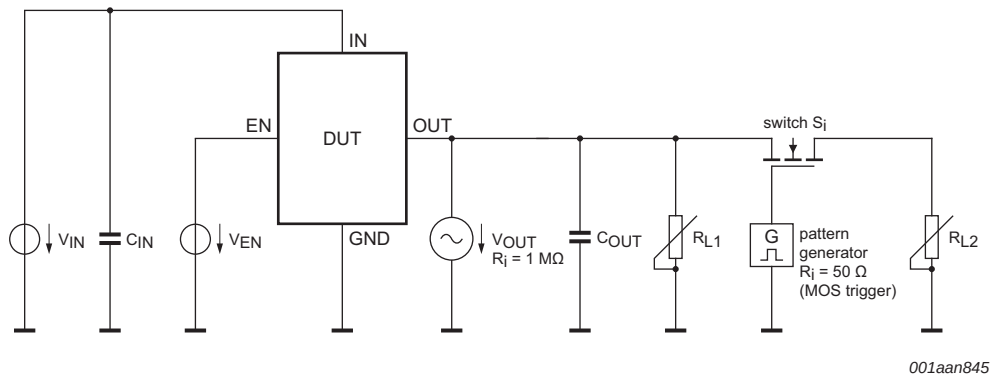
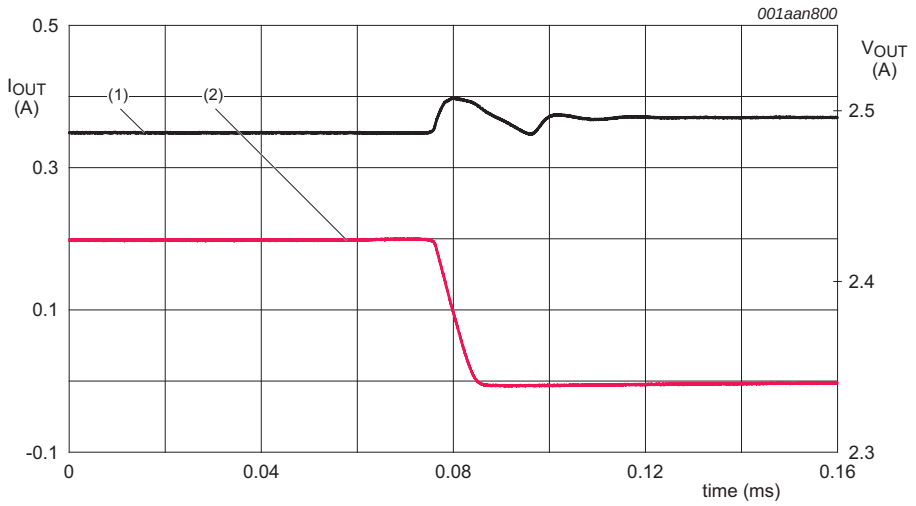


Fig 19. Load transient measurements setup

Table 9. Test conditions for load transient test

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IN}	voltage on pin IN		2.7	-	5.5	V
V_{EN}	voltage on pin EN		-	1.4	-	V
C_{IN}	input capacitance	case 0603 X5R	-	1	-	µF
C_{OUT}	output capacitance	case 0603 X5R	-	1	-	µF
R_{L1}	load resistor 1		0	-	∝	Ω
R_{L2}	load resistor 2		0	-	∝	Ω



(1) V_{OUT}

(2) I_{OUT}

Fig 20. Load transient (off) test result for LD6806CX4/25H

Figure 20 shows the load transient response when the load of the LD6806Cx4/25H changes from 200 mA to 1 mA. The test analyses the dynamic behavior of the LDO and aim to detect unwanted conditions in combination with downstream circuits. One of the key benefits of the response test is its capability to detect the impact of output capacitor value to the output voltage variation. This capability is important for sensitive circuits which do not allow an input voltage variation more than 2 % to 10 %.

For example Figure 21 shows the impact of an output voltage variation when changing the capacitor with different ESR and ESL values. Each capacitor has an equivalent circuit and it is described by an ESR and an ESL value. The ESR value can reach from few milliohms up to several hundred milliohms. The time until the output voltage reaches its original value increases when the ESR value increases. For higher ESL values or inductive PCB parts, the voltage drop rises. Both impacts can cause an oscillation of an LDO, too.

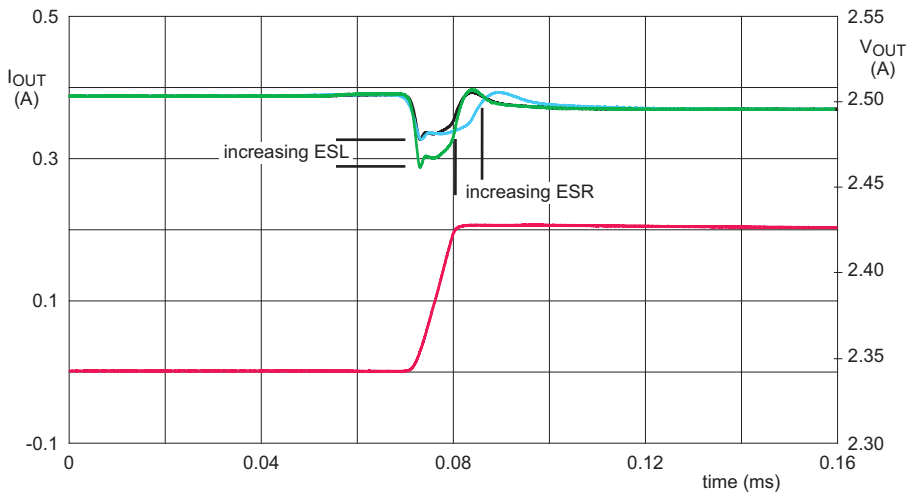


Fig 21. LD6806F/25H impact of output capacitor ESR and ESL to output voltage variation

The best practice is to check the device under real load conditions and to check if the step response tends to oscillate. For NXP low voltage LDOs like LD6806, LD6805 or LD6815 the use of capacitors with a low ESR is the best choice. The devices should be placed as close as possible to the LDO.

11. Accuracy or output voltage variation

11.1 Description

The accuracy is the output voltage divergence of an LDO and is described over temperature.

This parameter is influenced by each part of the LDO. A semiconductor circuit (error amplifier, reference voltage, resistor divider (internal or external) or pass element) has a certain behavior over a specific temperature range and is influenced by the manufacturing process. The accuracy is the sum of all variations.

11.2 Data sheet values

The accuracy test setup is illustrated in Figure 22. The LDO is driven under different load and different temperature levels. For tests, the temperature changes from ambient in steps from low to high values and is controlled with a thermal control apparatus (thermo stream).

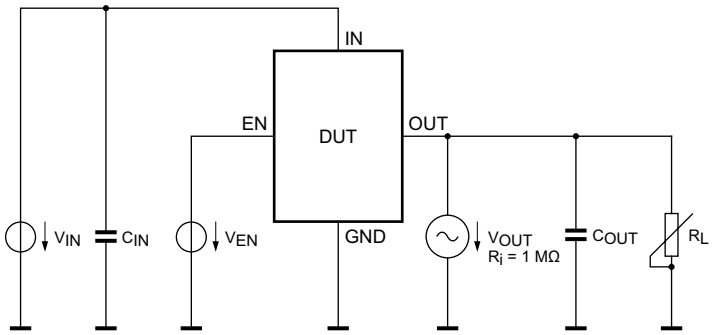


Fig 22. Accuracy test setup

Typical test conditions are: V_{IN} = 2.2 V; C_{OUT} = 1 µF and C_{IN} = 1 µF. As described in Figure 23, the accuracy, for example, for a LD6815TD is of about ±3 % over temperature. The device is produced for low voltage applications in mobile devices.

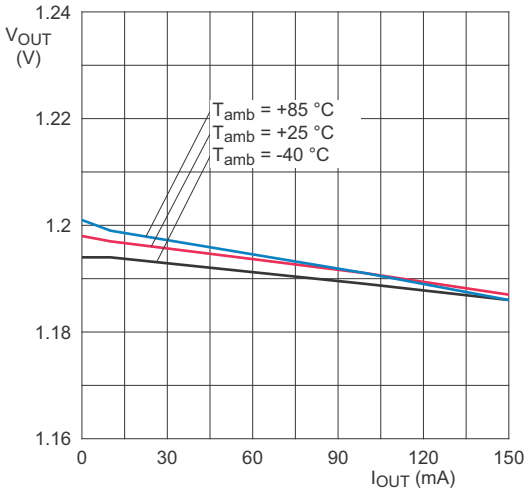


Fig 23. Accuracy LD6815TD/12x

Note: It is not possible to compare an accuracy of an LDO with and without inherent resistors. The accuracy of an adjustable LDO (without resistors) is always calculated without the tolerance of the inherent resistors divider for the feedback circuit.

12. Current limit, foldback circuit and thermal overload protection

12.1 Description

Current limiter and foldback circuits limit the current flow via an LDO when the device is used outside its specification. The current protection prevents device fail. This feature is required, for example, when the LDO output is accessible from the outside.

Example: An SD-card is tucked in an SD-card reader slot. A user breaks out the card from the slot with a screwdriver. During this procedure, it is possible to create a short between supply and ground. If it is not possible to disconnect the short, the device fails.

In this situation, an LDO with current protection shuts down and the device is not permanently damaged.

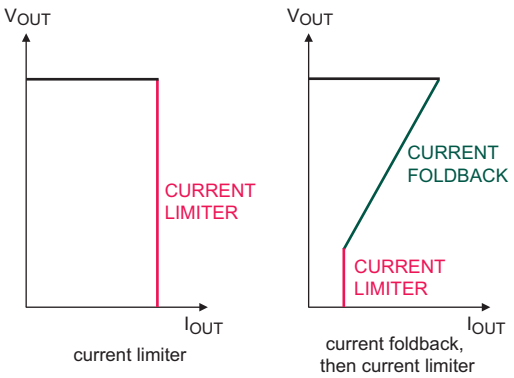


Fig 24. Current limiter and foldback

Therefore NXP includes three current protections in its low voltage LDOs.

The first one, a self-protection, is a thermal protection shutting down the device when a certain temperature on the LDO die is reached. The temperature watchdog helps avoiding overheating and short circuit. In order to prevent permanent damage, NXP LDOs with temperature watchdog can withstand short circuit until the watchdog is active.

The second protection is the current limiter (Figure 24 left). The feature is implemented in some LDOs for certain applications. The current limiter limits the current at a certain level until the current-demand declines.

The third protection is the foldback: a combination of a foldback circuit and a current limiter. A control unit observes the current flow. If the current overruns a certain level, the foldback circuit is activated and reduces the current to a defined level. A limiter clamps the current on a specific level. If the current decreases, the LDO switches off the limiter and starts up again. If the limit is reached again, the foldback is activated anew (Figure 24).

12.2 Data sheet values

Table 10 shows the static parameters from a data sheet. The thermal shutdown is typically at 160 °C. When the junction temperature exceeds this value, the LDO shuts down. It restarts at normal operation when the temperature sinks below 140 °C.

Table 10. Data sheet values

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
T_{sd}	shutdown temperature		-	160	-	°C
$T_{sd(hys)}$	shutdown temperature hysteresis		-	20	-	K
I_{sc}	short-circuit current	V_{OUT} = 0.0 V	-	30	-	mA
I_{fold}	foldback current		-	500	-	mA

The short-circuit current describes two parameter arrangements. Without foldback, the short-circuit current is the value when the limiter starts operation. When a foldback circuit is implemented, the foldback current is the value when the foldback circuit starts operation. Then the short-circuit value is the current limit after foldback is activated.

13. Conclusion

This application note summarizes the most common test conditions for an LDO data sheet. It shows that a comparison of parameters from different manufacturers is not so easy. Each parameter follows special rules. The application note underlines that NXP Semiconductors has a standardized process to evaluate its LDO products, ensuring high quality for its customers.

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