

CRYSTAL OSCILLATOR LOW-JITTER SPXO



SG-210S*H

•Frequency range : 80.000 MHz to 170.000 MHz

Fundamental mode oscillator

•Supply voltage : 1.8 V / 2.5 V / 3.3 V

•Output : CMOS •Function : Standby(s̄T) •External dimensions : 2.5 x 2.0 x 0.8 mm





Product Number (please contact us) SG-210SCH: X1G003931xxxx00 SG-210SDH: X1G003941xxxx00 SG-210SEH: X1G003951xxxx00





Actual size

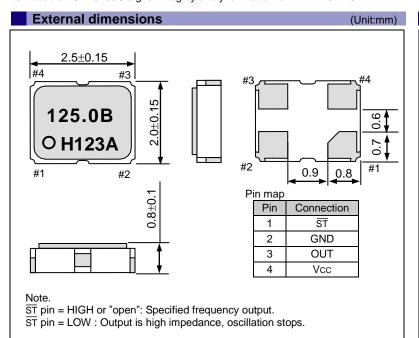
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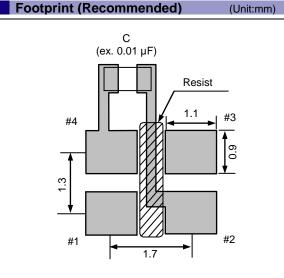
Specifications (characteristics)

Item	Cumbal	Specifications			Conditions / Demostro
	Symbol	SG-210SEH	SG-210SDH	SG-210SCH	Conditions / Remarks
		80.000 MHz to 170.000 MHz			
Output frequency range	fo	100MHz, 106.25MHz, 125MHz, 133.33MHz, 150MHz, 156.25MHz			Standard frequency. *1
Supply voltage	Vcc	1.8 V ± 10%	2.5 V ± 10%	3.3 V ± 10%	*2
Storage temperature	T_stg	-40 °C to +125 °C			Storage as single product.
Operating temperature	T_use	-40 °C to +85 °C			
Frequency tolerance	f_tol -	B: $\pm 50 \times 10^{-6}$, C: $\pm 100 \times 10^{-6}$			-20 °C to +70 °C
		L: $\pm 50 \times 10^{-6}$, M: $\pm 100 \times 10^{-6}$			-40 °C to +85 °C
Current consumption	Icc -	6.0 mA Max.	7.0 mA Max.	9.0 mA Max.	No load condition,80 MHz≤fo≤125 MHz
		8.0 mA Max.	9.0 mA Max.	11.0 mA Max.	No load condition,125 MHz <fo≤170 mhz<="" td=""></fo≤170>
Stand-by current	I_std	10.0 μA Max.			ST =GND
Symmetry	SYM	45 % to 55 %			50 % Vcc level, L_CMOS ≤ 15 pF
Output voltage	Voн	90 % Vcc Min.			Iон = -4mA
	Vol	10 % Vcc Max.		IoL = 4mA	
Output load condition (CMOS)	L_CMOS	15 pF Max.			
Input voltage	ViH	80 % Vcc Min.		ST terminal	
	VIL	20 % Vcc Max.			
Rise time / Fall time	tr/ tf	3 ns Max. 2 ns Max.		20 % Vcc to 80 % Vcc level, L_CMOS ≤15 pF	
Start-up time	t_str	5 ms Max.		T=0 at 90 % Vcc	
Jitter *3	tp-p	22 ps Typ.	20 ps Typ.		Peak to Peak
Phase Jitter	tpJ	0.7 ps Max. 0.6 ps Max.		Offset frequency: L_CMOS ≤ 15 pF 12kHz to 20MHz	
Frequency aging	f_aging	±5 × 10 ⁻⁶ / year Max.			+25 °C, First year

^{*1} Please contact us for requirements not listed in the specification.

^{*3} Based on SIA-3100C signal integrity analyzer made from WAVECREST.





To maintain stable operation, provide a 0.01uF to 0.1uF by-pass capacitor at a location as near as possible to the power source terminal of the crystal product (between Vcc - GND).

^{*2} fo \geq 157MHz: Vcc \pm 5%

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