



PSMN9R5-100PS

N-channel 100 V 9.6 m Ω standard level MOSFET in TO220

17 October 2013

Product data sheet

1. General description

Standard level N-channel MOSFET in a TO220 packages qualified to 175C. This product is designed and qualified for use in a wide range of industrial, communications and domestic equipment.

2. Features and benefits

- High efficiency due to low switching and conduction losses
- Suitable for standard level gate drive

3. Applications

- DC-to-DC converters
- Load switching
- Motor control
- Server power supplies

4. Quick reference data

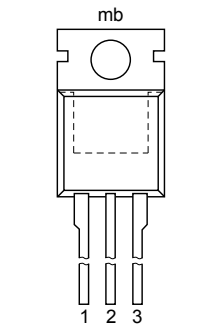
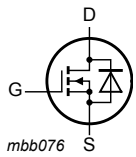
Table 1. Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V _{DS}	drain-source voltage	T _j ≥ 25 °C; T _j ≤ 175 °C	-	-	100	V
I _D	drain current	T _{mb} = 25 °C; V _{GS} = 10 V; Fig. 1	-	-	89	A
P _{tot}	total power dissipation	T _{mb} = 25 °C; Fig. 2	-	-	211	W
Static characteristics						
R _{DS(on)}	drain-source on-state resistance	V _{GS} = 10 V; I _D = 15 A; T _j = 25 °C; Fig. 13	-	8.16	9.6	m Ω
Dynamic characteristics						
Q _{GD}	gate-drain charge	V _{GS} = 10 V; I _D = 60 A; V _{DS} = 50 V; Fig. 14 ; Fig. 15	-	23	-	nC
Q _{G(tot)}	total gate charge		-	82	-	nC
Avalanche ruggedness						
E _{DS(AL)S}	non-repetitive drain-source avalanche energy	V _{GS} = 10 V; T _{j(init)} = 25 °C; I _D = 89 A; V _{sup} ≤ 100 V; unclamped; R _{GS} = 50 Ω	-	-	177	mJ



5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	G	gate	 <p>TO-220AB (SOT78)</p>	 <p>mbb076</p>
2	D	drain		
3	S	source		
mb	D	mounting base; connected to drain		

6. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
PSMN9R5-100PS	TO-220AB	plastic single-ended package; heatsink mounted; 1 mounting hole; 3-lead TO-220AB	SOT78

7. Marking

Table 4. Marking codes

Type number	Marking code
PSMN9R5-100PS	PSMN9R5-100PS

8. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DS}	drain-source voltage	$T_j \geq 25\text{ °C}$; $T_j \leq 175\text{ °C}$	-	100	V
V_{DGR}	drain-gate voltage	$T_j \leq 175\text{ °C}$; $T_j \geq 25\text{ °C}$; $R_{GS} = 20\text{ k}\Omega$	-	100	V
V_{GS}	gate-source voltage		-20	20	V
I_D	drain current	$V_{GS} = 10\text{ V}$; $T_{mb} = 100\text{ °C}$; Fig. 1	-	63	A
		$V_{GS} = 10\text{ V}$; $T_{mb} = 25\text{ °C}$; Fig. 1	-	89	A
I_{DM}	peak drain current	pulsed; $t_p \leq 10\text{ }\mu\text{s}$; $T_{mb} = 25\text{ °C}$; Fig. 3	-	355	A

Symbol	Parameter	Conditions	Min	Max	Unit
P _{tot}	total power dissipation	T _{mb} = 25 °C; Fig. 2	-	211	W
T _{stg}	storage temperature		-55	175	°C
T _j	junction temperature		-55	175	°C
T _{slid(M)}	peak soldering temperature		-	260	°C
Source-drain diode					
I _S	source current	T _{mb} = 25 °C	-	89	A
I _{SM}	peak source current	pulsed; t _p ≤ 10 μs; T _{mb} = 25 °C	-	355	A
Avalanche ruggedness					
E _{DS(AL)S}	non-repetitive drain-source avalanche energy	V _{GS} = 10 V; T _{j(init)} = 25 °C; I _D = 89 A; V _{sup} ≤ 100 V; unclamped; R _{GS} = 50 Ω	-	177	mJ

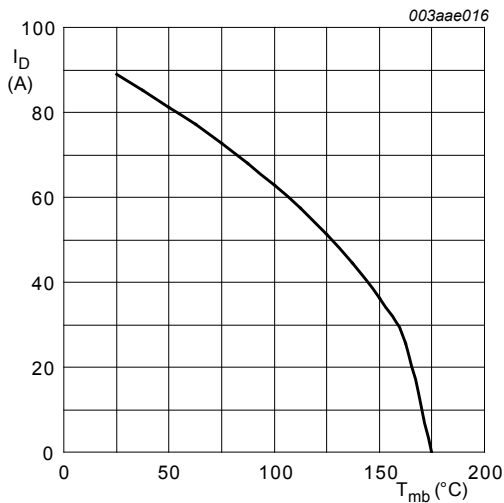


Fig. 1. Continuous drain current as a function of mounting base temperature

$$V_{GS} \geq 10 \text{ V}$$

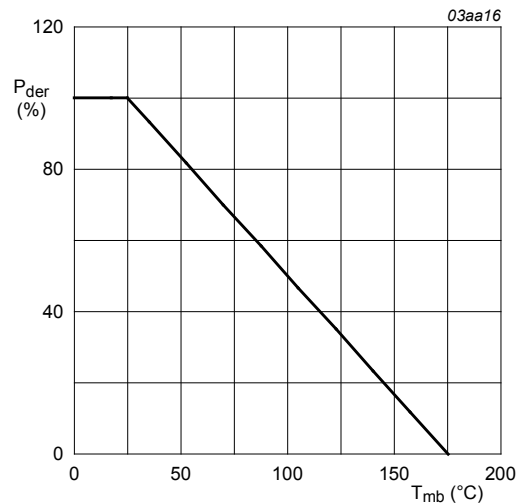
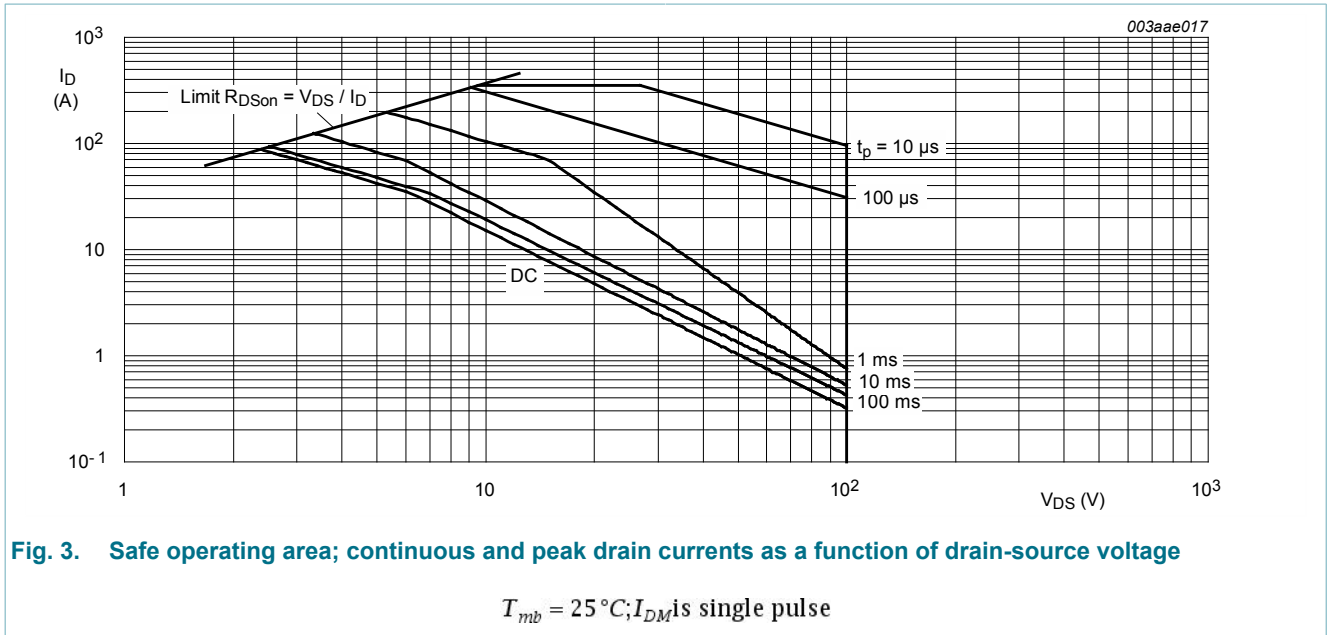


Fig. 2. Normalized total power dissipation as a function of mounting base temperature

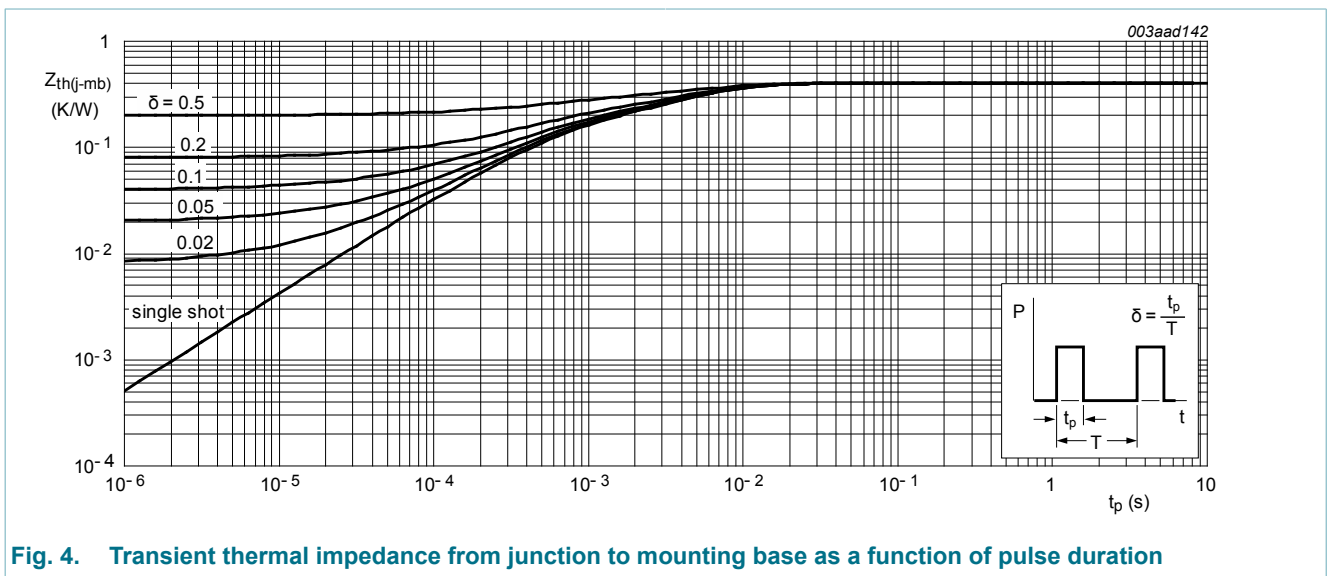
$$P_{der} = \frac{P_{tot}}{P_{tot(25^\circ\text{C})}} \times 100 \%$$



9. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	Fig. 4	-	0.38	0.71	K/W

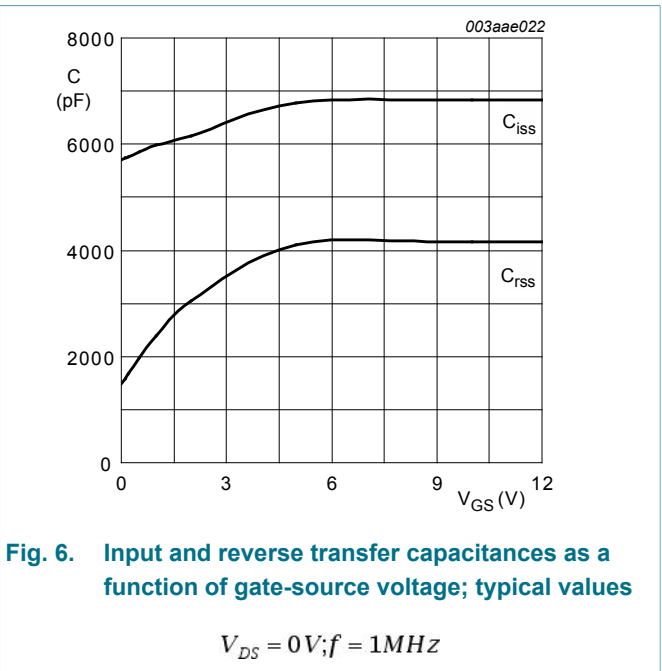
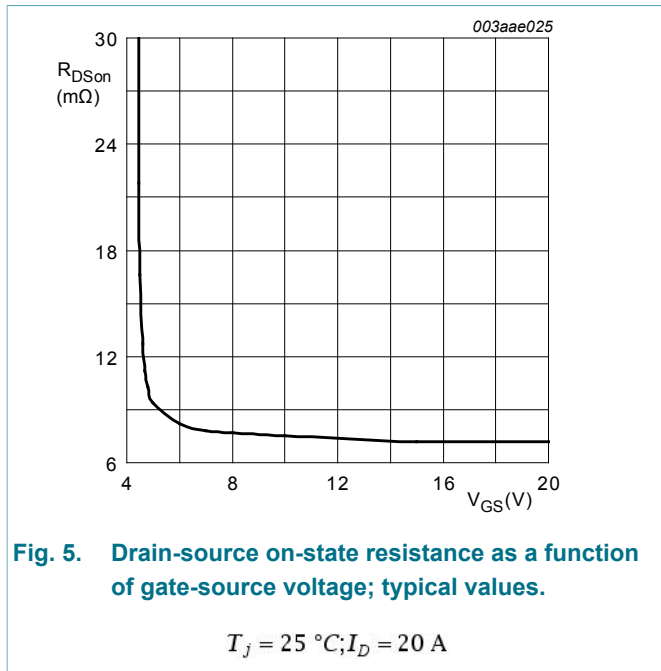


10. Characteristics

Table 7. Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static characteristics						
$V_{(BR)DSS}$	drain-source breakdown voltage	$I_D = 0.25 \text{ mA}; V_{GS} = 0 \text{ V}; T_j = -55 \text{ }^\circ\text{C}$	90	-	-	V
		$I_D = 0.25 \text{ mA}; V_{GS} = 0 \text{ V}; T_j = 25 \text{ }^\circ\text{C}$	100	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	$I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = 175 \text{ }^\circ\text{C};$ Fig. 10; Fig. 11	1	-	-	V
		$I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = 25 \text{ }^\circ\text{C};$ Fig. 10; Fig. 11	2	3	4	V
		$I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = -55 \text{ }^\circ\text{C};$ Fig. 10; Fig. 11	-	-	4.8	V
I_{DSS}	drain leakage current	$V_{DS} = 100 \text{ V}; V_{GS} = 0 \text{ V}; T_j = 125 \text{ }^\circ\text{C}$	-	-	100	μA
		$V_{DS} = 100 \text{ V}; V_{GS} = 0 \text{ V}; T_j = 25 \text{ }^\circ\text{C}$	-	0.02	4	μA
I_{GSS}	gate leakage current	$V_{GS} = 20 \text{ V}; V_{DS} = 0 \text{ V}; T_j = 25 \text{ }^\circ\text{C}$	-	10	100	nA
		$V_{GS} = -20 \text{ V}; V_{DS} = 0 \text{ V}; T_j = 25 \text{ }^\circ\text{C}$	-	10	100	nA
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = 10 \text{ V}; I_D = 15 \text{ A}; T_j = 100 \text{ }^\circ\text{C};$ Fig. 12	-	-	17.3	mΩ
		$V_{GS} = 10 \text{ V}; I_D = 15 \text{ A}; T_j = 175 \text{ }^\circ\text{C};$ Fig. 12	-	23.5	27.4	mΩ
		$V_{GS} = 10 \text{ V}; I_D = 15 \text{ A}; T_j = 25 \text{ }^\circ\text{C};$ Fig. 13	-	8.16	9.6	mΩ
R_G	internal gate resistance (AC)	$f = 1 \text{ MHz}$	-	0.7	-	Ω
Dynamic characteristics						
$Q_{G(tot)}$	total gate charge	$I_D = 0 \text{ A}; V_{DS} = 0 \text{ V}; V_{GS} = 10 \text{ V};$ Fig. 14	-	67	-	nC
		$I_D = 60 \text{ A}; V_{DS} = 50 \text{ V}; V_{GS} = 10 \text{ V};$ Fig. 14; Fig. 15	-	82	-	nC
Q_{GS}	gate-source charge		-	21	-	nC
$Q_{GS(th)}$	pre-threshold gate-source charge	$I_D = 60 \text{ A}; V_{DS} = 50 \text{ V}; V_{GS} = 3 \text{ V};$ Fig. 14	-	13.1	-	nC
$Q_{GS(th-pl)}$	post-threshold gate-source charge	$I_D = 60 \text{ A}; V_{DS} = 50 \text{ V}; V_{GS} = 10 \text{ V};$ Fig. 14	-	7.8	-	nC
Q_{GD}	gate-drain charge	$I_D = 60 \text{ A}; V_{DS} = 50 \text{ V}; V_{GS} = 10 \text{ V};$ Fig. 14; Fig. 15	-	23	-	nC
$V_{GS(pl)}$	gate-source plateau voltage	$V_{DS} = 50 \text{ V};$ Fig. 14; Fig. 15	-	4.5	-	V
C_{iss}	input capacitance	$V_{DS} = 50 \text{ V}; V_{GS} = 0 \text{ V}; f = 1 \text{ MHz};$	-	4454	-	pF
C_{oss}	output capacitance	$T_j = 25 \text{ }^\circ\text{C};$ Fig. 16	-	302	-	pF

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
C_{rss}	reverse transfer capacitance		-	185	-	pF
$t_{d(on)}$	turn-on delay time	$V_{DS} = 50\text{ V}; R_L = 0.8\ \Omega; V_{GS} = 10\text{ V};$ $R_{G(ext)} = 4.7\ \Omega; T_j = 25\text{ }^\circ\text{C}$	-	22	-	ns
t_r	rise time		-	25.2	-	ns
$t_{d(off)}$	turn-off delay time		-	52.2	-	ns
t_f	fall time		-	22.8	-	ns
Source-drain diode						
V_{SD}	source-drain voltage	$I_S = 15\text{ A}; V_{GS} = 0\text{ V}; T_j = 25\text{ }^\circ\text{C};$ Fig. 17	-	0.85	1.2	V
t_{rr}	reverse recovery time	$I_S = 20\text{ A}; dI_S/dt = 100\text{ A}/\mu\text{s}; V_{GS} = 0\text{ V};$	-	61.5	-	ns
Q_r	recovered charge	$V_{DS} = 50\text{ V}$	-	157	-	nC



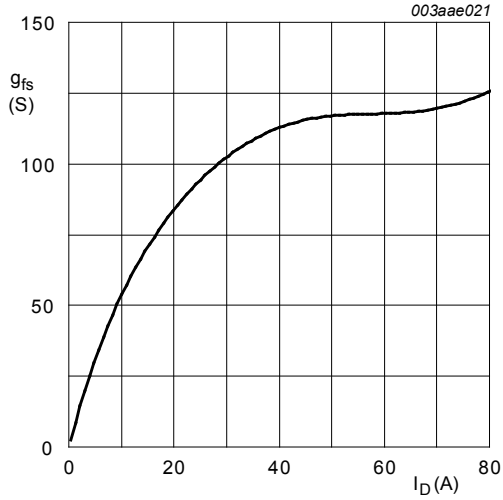


Fig. 7. Forward transconductance as a function of drain current; typical values

$$T_j = 25\text{ }^\circ\text{C}; V_{DS} = 25\text{ V}$$

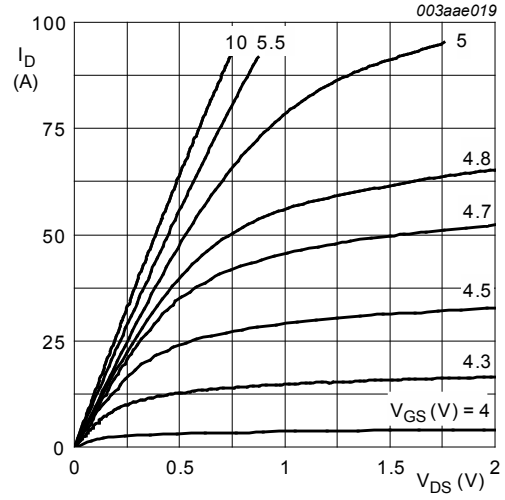


Fig. 8. Output characteristics: drain current as a function of drain-source voltage; typical values

$$T_j = 25\text{ }^\circ\text{C}$$

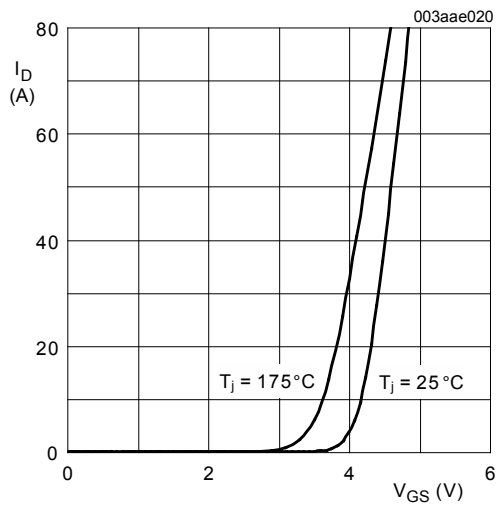


Fig. 9. Transfer characteristics: drain current as a function of gate-source voltage; typical values

$$V_{DS} > I_D \times R_{DS(on)}$$

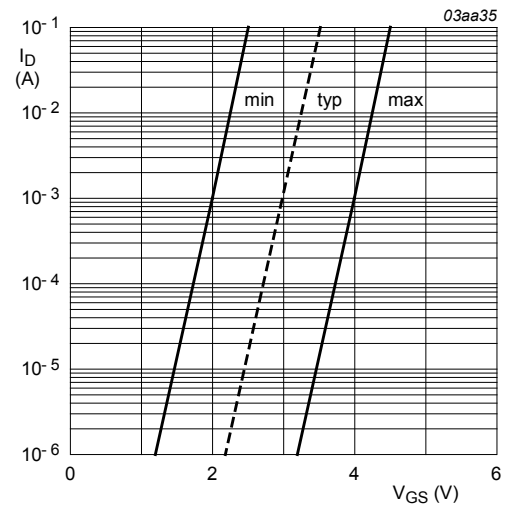


Fig. 10. Sub-threshold drain current as a function of gate-source voltage

$$T_j = 25\text{ }^\circ\text{C}; V_{DS} = 5\text{ V}$$

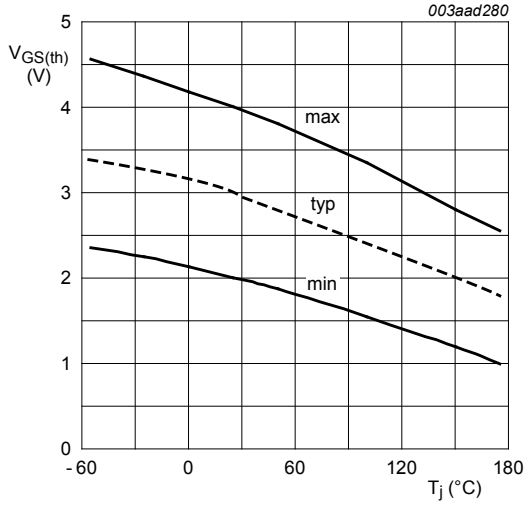


Fig. 11. Gate-source threshold voltage as a function of junction temperature

$$I_D = 1 \text{ mA}; V_{DS} = V_{GS}$$

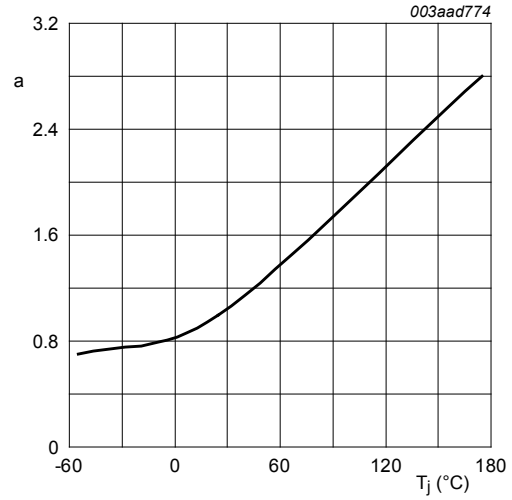


Fig. 12. Normalized drain-source on-state resistance factor as a function of junction temperature

$$a = \frac{R_{DSon}}{R_{DSon(25^\circ\text{C})}}$$

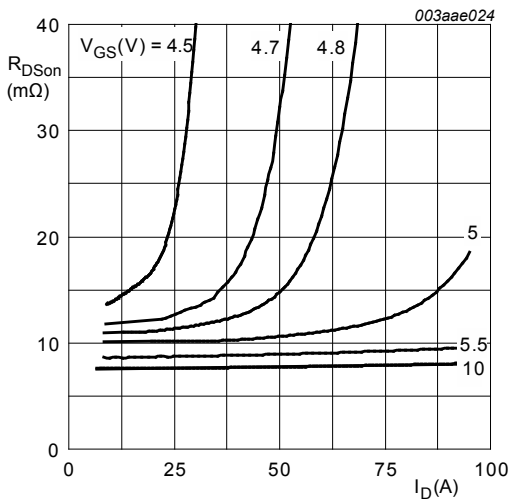


Fig. 13. Drain-source on-state resistance as a function of drain current; typical values

$$T_j = 25^\circ\text{C}$$

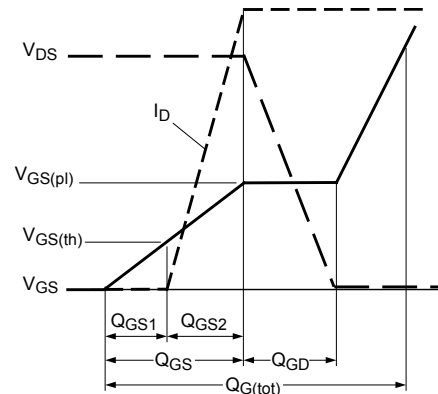


Fig. 14. Gate charge waveform definitions

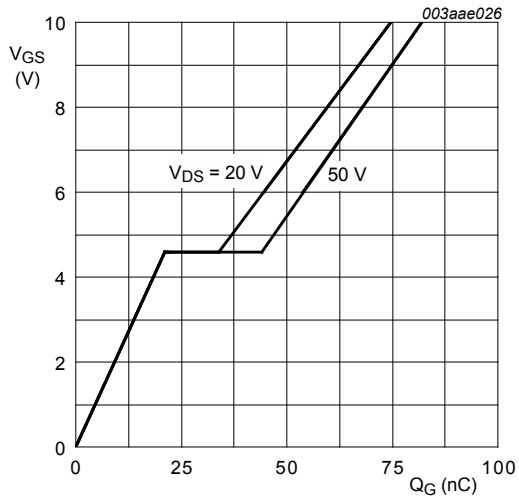


Fig. 15. Gate-source voltage as a function of gate charge; typical values

$T_j = 25\text{ }^\circ\text{C}$; $I_D = 60\text{ A}$

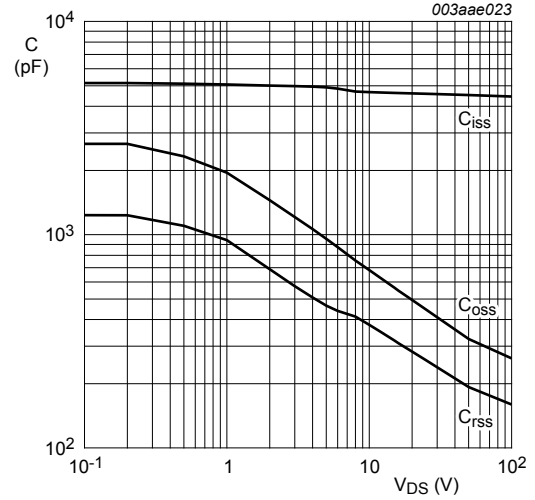


Fig. 16. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values

$V_{GS} = 0\text{ V}$; $f = 1\text{ MHz}$

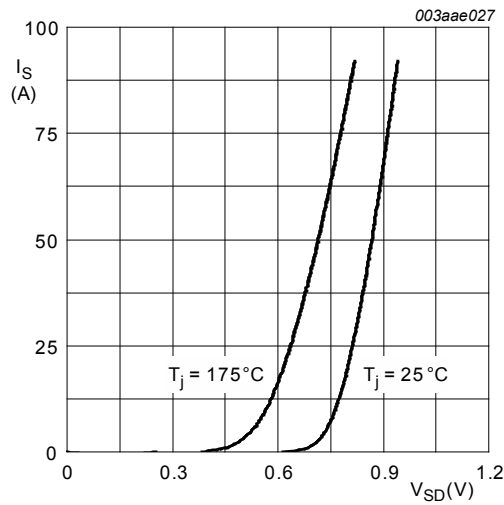


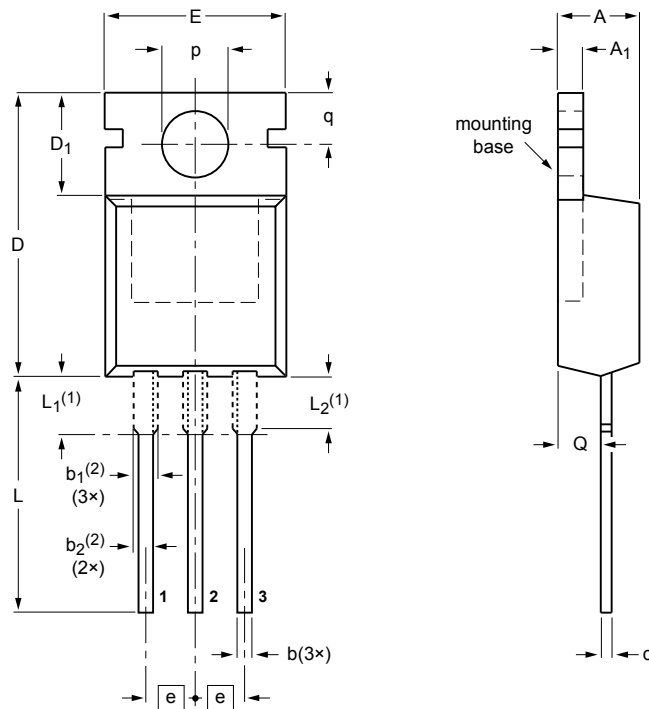
Fig. 17. Source current as a function of source-drain voltage; typical values

$V_{GS} = 0\text{ V}$

11. Package outline

Plastic single-ended package; heatsink mounted; 1 mounting hole; 3-lead TO-220AB

SOT78



DIMENSIONS (mm are the original dimensions)

UNIT	A	A ₁	b	b ₁ (2)	b ₂ (2)	c	D	D ₁	E	e	L	L ₁ (1)	L ₂ (1) max.	p	q	Q
mm	4.7 4.1	1.40 1.25	0.9 0.6	1.6 1.0	1.3 1.0	0.7 0.4	16.0 15.2	6.6 5.9	10.3 9.7	2.54	15.0 12.8	3.30 2.79	3.0	3.8 3.5	3.0 2.7	2.6 2.2

Notes

- 1. Lead shoulder designs may vary.
- 2. Dimension includes excess dambar.

OUTLINE VERSION	REFERENCES			EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA		
SOT78		3-lead TO-220AB	SC-46		08-04-23 08-06-13

Fig. 18. Package outline TO-220AB (SOT78)

12. Legal information

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Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

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[K66F](#) [FRDM-KW40Z](#) [FRDM-MC-LVBLDC](#) [PESD18VF1BSFYL](#) [PMF63UNEX](#) [PSMN4R0-60YS,115](#) [HEF4028BPN](#) [RAPPID-567XFSW](#)
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[BZT52H-B9V1.115](#) [BZV85-C3V9.113](#) [BZX79-C47.113](#) [P5020NSE7VNB](#) [S12ZVML12EVBLIN](#) [SCC2692AC1N40](#) [LPC1785FBD208K](#)
[LPC2124FBD64/01](#) [LS1020ASN7KQB](#) [LS1020AXN7HNB](#) [LS1020AXN7KQB](#) [LS1043ASE7PQA](#) [T1023RDB-PC](#)