

# PSMN5R8-40YS

N-channel LPAK 40 V 5.7 m $\Omega$  standard level MOSFET

Rev. 03 — 25 October 2010

Product data sheet

## 1. Product profile

### 1.1 General description

Standard level N-channel MOSFET in LPAK package qualified to 175 °C. This product is designed and qualified for use in a wide range of industrial, communications and domestic equipment.

### 1.2 Features and benefits

- Advanced TrenchMOS provides low R<sub>DSon</sub> and low gate charge
- High efficiency gains in switching power converters
- Improved mechanical and thermal characteristics
- LPAK provides maximum power density in a Power SO8 package

### 1.3 Applications

- DC-to-DC convertors
- Lithium-ion battery protection
- Load switching
- Motor control
- Server power supplies

### 1.4 Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V <sub>DS</sub>	drain-source voltage	T <sub>j</sub> ≥ 25 °C; T <sub>j</sub> ≤ 175 °C	-	-	40	V
I <sub>D</sub>	drain current	T <sub>mb</sub> = 25 °C; V <sub>GS</sub> = 10 V; see <a href="#">Figure 1</a>	-	-	90	A
P <sub>tot</sub>	total power dissipation	T <sub>mb</sub> = 25 °C; see <a href="#">Figure 2</a>	-	-	89	W
T <sub>j</sub>	junction temperature		-55	-	175	°C
<b>Static characteristics</b>						
R <sub>DSon</sub>	drain-source on-state resistance	V <sub>GS</sub> = 10 V; I <sub>D</sub> = 15 A; T <sub>j</sub> = 100 °C; see <a href="#">Figure 12</a>	-	-	7.7	m $\Omega$
		V <sub>GS</sub> = 10 V; I <sub>D</sub> = 15 A; T <sub>j</sub> = 25 °C; see <a href="#">Figure 13</a>	-	4.4	5.7	m $\Omega$

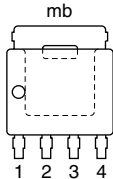
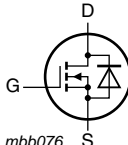


**Table 1. Quick reference data ...continued**

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>Dynamic characteristics</b>						
$Q_{GD}$	gate-drain charge	$V_{GS} = 10\text{ V}; I_D = 75\text{ A};$	-	7.8	-	nC
$Q_{G(\text{tot})}$	total gate charge	$V_{DS} = 20\text{ V};$ see <a href="#">Figure 14</a> ; see <a href="#">Figure 15</a>	-	28.8	-	nC
<b>Avalanche ruggedness</b>						
$E_{DS(\text{AL})S}$	non-repetitive drain-source avalanche energy	$V_{GS} = 10\text{ V}; T_{j(\text{init})} = 25\text{ °C};$ $I_D = 90\text{ A}; V_{\text{sup}} \leq 40\text{ V};$ unclamped; $R_{GS} = 50\text{ }\Omega$	-	-	65	mJ

## 2. Pinning information

**Table 2. Pinning information**

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	S	source	 <p>SOT669 (LPAK)</p>	 <p>mbb076</p>
2	S	source		
3	S	source		
4	G	gate		
mb	D	mounting base; connected to drain		

## 3. Ordering information

**Table 3. Ordering information**

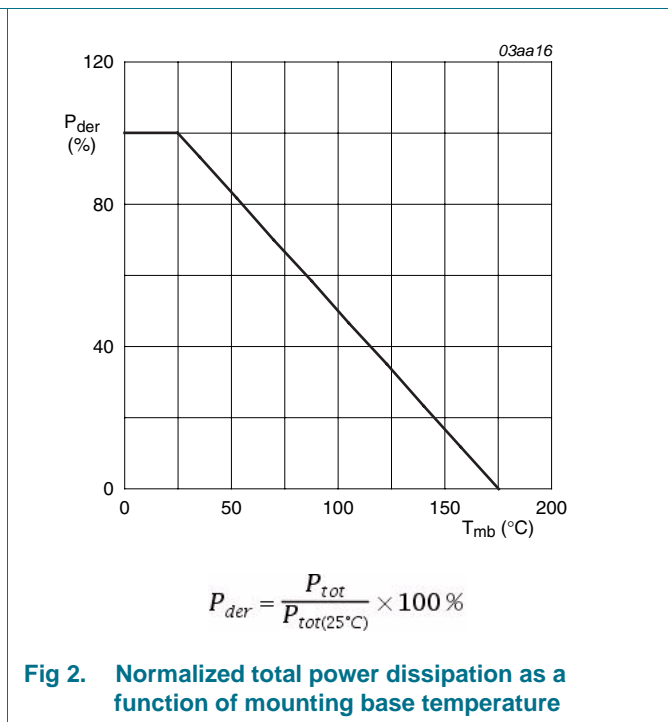
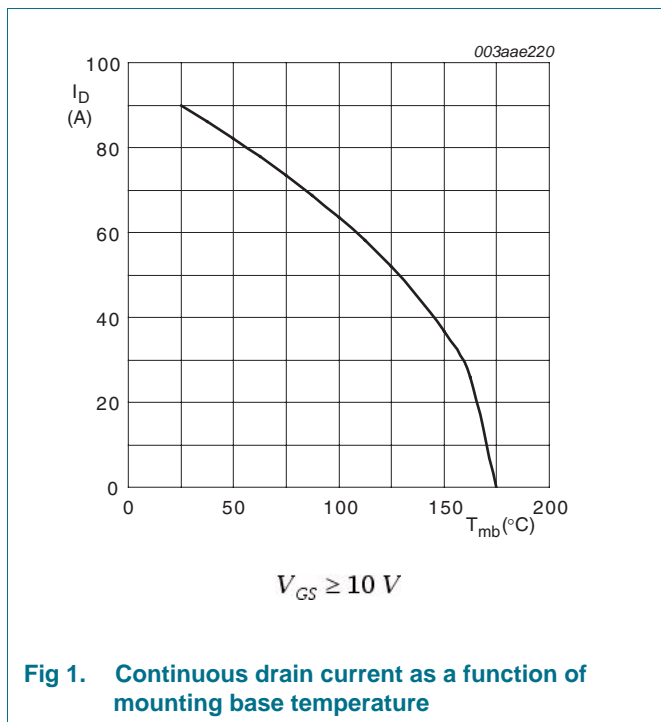
Type number	Package		Version
	Name	Description	
PSMN5R8-40YS	LPAK	plastic single-ended surface-mounted package (LPAK); 4 leads	SOT669

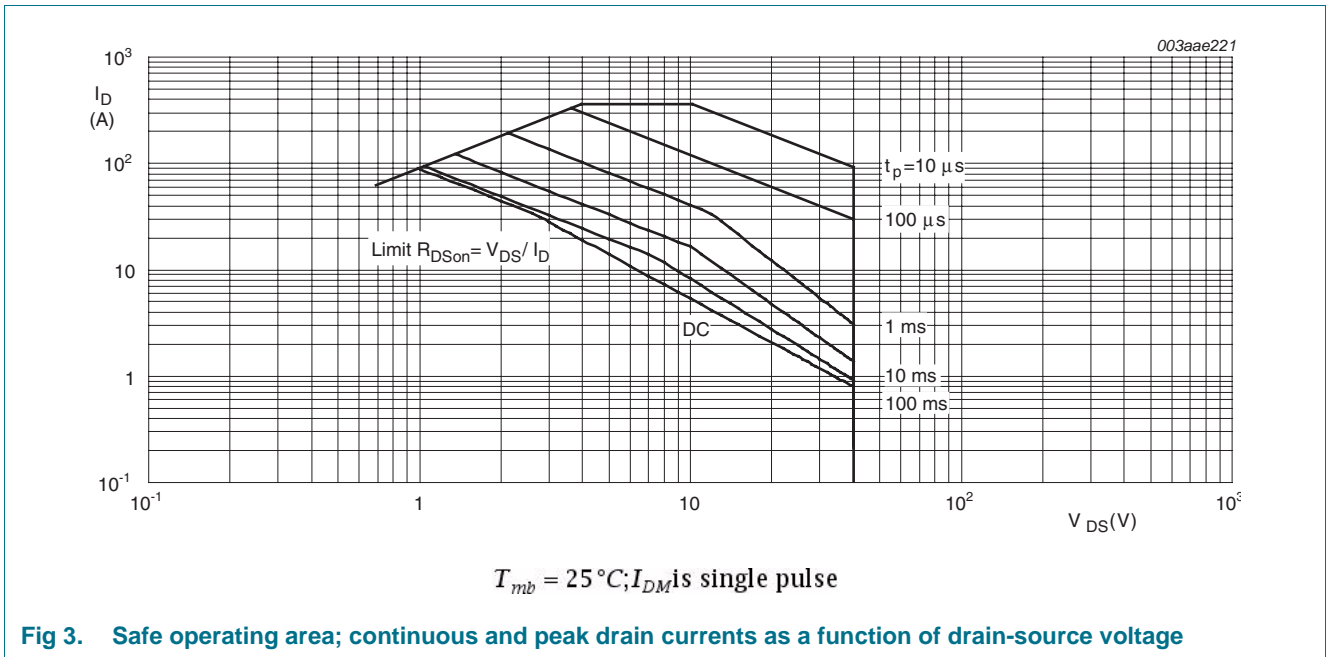
### 4. Limiting values

**Table 4. Limiting values**

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{DS}$	drain-source voltage	$T_j \geq 25\text{ °C}; T_j \leq 175\text{ °C}$	-	40	V
$V_{DGR}$	drain-gate voltage	$T_j \geq 25\text{ °C}; T_j \leq 175\text{ °C}; R_{GS} = 20\text{ k}\Omega$	-	40	V
$V_{GS}$	gate-source voltage		-20	20	V
$I_D$	drain current	$V_{GS} = 10\text{ V}; T_{mb} = 100\text{ °C};$ see <a href="#">Figure 1</a>	-	64	A
		$V_{GS} = 10\text{ V}; T_{mb} = 25\text{ °C};$ see <a href="#">Figure 1</a>	-	90	A
$I_{DM}$	peak drain current	pulsed; $t_p \leq 10\text{ }\mu\text{s}; T_{mb} = 25\text{ °C};$ see <a href="#">Figure 3</a>	-	360	A
$P_{tot}$	total power dissipation	$T_{mb} = 25\text{ °C};$ see <a href="#">Figure 2</a>	-	89	W
$T_{stg}$	storage temperature		-55	175	°C
$T_j$	junction temperature		-55	175	°C
$T_{sld(M)}$	peak soldering temperature		-	260	°C
<b>Source-drain diode</b>					
$I_S$	source current	$T_{mb} = 25\text{ °C}$	-	90	A
$I_{SM}$	peak source current	pulsed; $t_p \leq 10\text{ }\mu\text{s}; T_{mb} = 25\text{ °C}$	-	360	A
<b>Avalanche ruggedness</b>					
$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	$V_{GS} = 10\text{ V}; T_{j(\text{init})} = 25\text{ °C}; I_D = 90\text{ A}; V_{sup} \leq 40\text{ V};$ unclamped; $R_{GS} = 50\text{ }\Omega$	-	65	mJ





### 5. Thermal characteristics

Table 5. Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	see <a href="#">Figure 4</a>	-	0.81	1.68	K/W

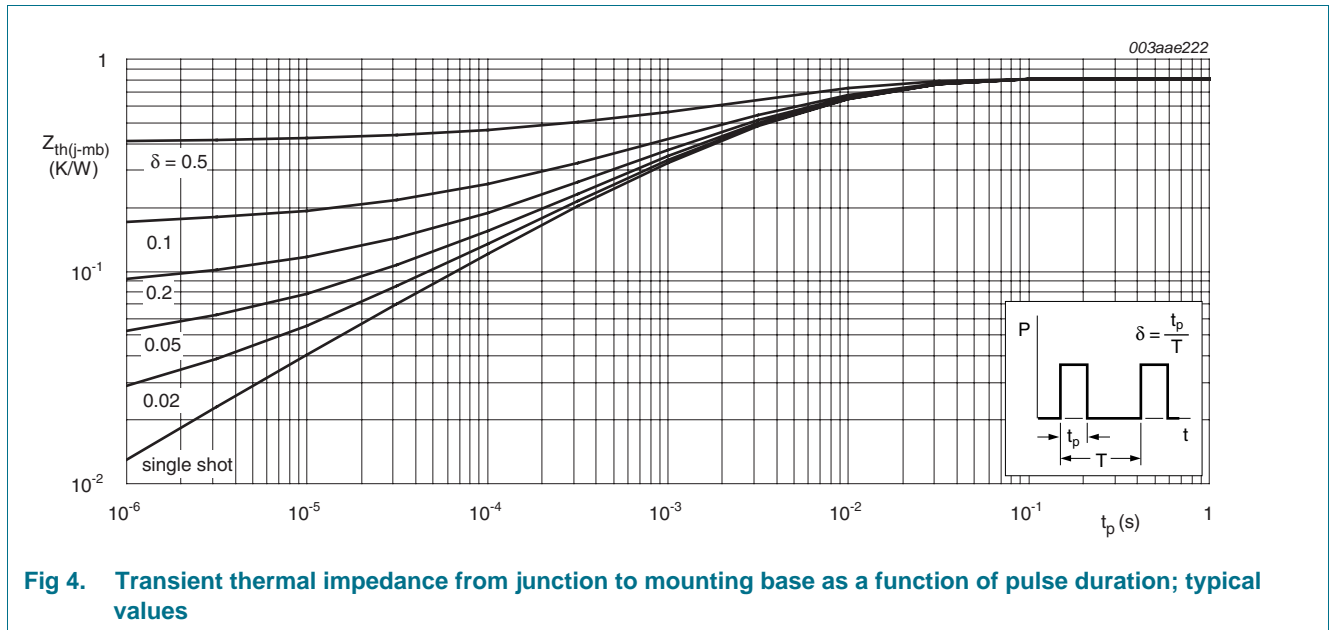


Fig 4. Transient thermal impedance from junction to mounting base as a function of pulse duration; typical values

## 6. Characteristics

**Table 6. Characteristics**

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>Static characteristics</b>						
$V_{(BR)DSS}$	drain-source breakdown voltage	$I_D = 250 \mu A; V_{GS} = 0 V; T_j = -55 \text{ }^\circ C$	36	-	-	V
		$I_D = 250 \mu A; V_{GS} = 0 V; T_j = 25 \text{ }^\circ C$	40	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	$I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = -55 \text{ }^\circ C$ ; see <a href="#">Figure 10</a>	-	-	4.6	V
		$I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = 175 \text{ }^\circ C$ ; see <a href="#">Figure 10</a>	1	-	-	V
		$I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = 25 \text{ }^\circ C$ ; see <a href="#">Figure 11</a> ; see <a href="#">Figure 10</a>	2	3	4	V
$I_{DSS}$	drain leakage current	$V_{DS} = 40 V; V_{GS} = 0 V; T_j = 25 \text{ }^\circ C$	-	0.02	1	$\mu A$
		$V_{DS} = 40 V; V_{GS} = 0 V; T_j = 125 \text{ }^\circ C$	-	10	100	$\mu A$
$I_{GSS}$	gate leakage current	$V_{GS} = 20 V; V_{DS} = 0 V; T_j = 25 \text{ }^\circ C$	-	10	100	nA
		$V_{GS} = -20 V; V_{DS} = 0 V; T_j = 25 \text{ }^\circ C$	-	10	100	nA
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = 10 V; I_D = 15 A; T_j = 100 \text{ }^\circ C$ ; see <a href="#">Figure 12</a>	-	-	7.7	mΩ
		$V_{GS} = 10 V; I_D = 15 A; T_j = 175 \text{ }^\circ C$ ; see <a href="#">Figure 12</a>	-	-	10.26	mΩ
		$V_{GS} = 10 V; I_D = 15 A; T_j = 25 \text{ }^\circ C$ ; see <a href="#">Figure 13</a>	-	4.4	5.7	mΩ
$R_G$	internal gate resistance (AC)	$f = 1 \text{ MHz}$	-	0.53	-	Ω
<b>Dynamic characteristics</b>						
$Q_{G(tot)}$	total gate charge	$I_D = 0 A; V_{DS} = 0 V; V_{GS} = 10 V$	-	23.8	-	nC
		$I_D = 75 A; V_{DS} = 20 V; V_{GS} = 10 V$ ; see <a href="#">Figure 14</a> ; see <a href="#">Figure 15</a>	-	28.8	-	nC
$Q_{GS}$	gate-source charge	$I_D = 75 A; V_{DS} = 20 V; V_{GS} = 10 V$ ; see <a href="#">Figure 14</a>	-	9.8	-	nC
$Q_{GS(th)}$	pre-threshold gate-source charge		-	5.1	-	nC
$Q_{GS(th-pl)}$	post-threshold gate-source charge		-	4.7	-	nC
$Q_{GD}$	gate-drain charge	$I_D = 75 A; V_{DS} = 20 V; V_{GS} = 10 V$ ; see <a href="#">Figure 14</a> ; see <a href="#">Figure 15</a>	-	7.8	-	nC
$V_{GS(pl)}$	gate-source plateau voltage	$I_D = 75 A; V_{DS} = 20 V$ ; see <a href="#">Figure 14</a> ; see <a href="#">Figure 15</a>	-	5.7	-	V
$C_{iss}$	input capacitance	$V_{DS} = 20 V; V_{GS} = 0 V; f = 1 \text{ MHz}$ ;	-	1703	-	pF
$C_{oss}$	output capacitance	$T_j = 25 \text{ }^\circ C$ ; see <a href="#">Figure 16</a>	-	384	-	pF
$C_{rss}$	reverse transfer capacitance		-	213	-	pF
$t_{d(on)}$	turn-on delay time	$V_{DS} = 20 V; R_L = 0.3 \text{ } \Omega; V_{GS} = 10 V$ ;	-	16	-	ns
$t_r$	rise time	$R_{G(ext)} = 4.7 \text{ } \Omega$	-	12	-	ns
$t_{d(off)}$	turn-off delay time		-	25	-	ns
$t_f$	fall time		-	8	-	ns

Table 6. Characteristics ...continued

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>Source-drain diode</b>						
$V_{SD}$	source-drain voltage	$I_S = 15\text{ A}$ ; $V_{GS} = 0\text{ V}$ ; $T_j = 25\text{ °C}$ ; see <a href="#">Figure 17</a>	-	0.82	1.2	V
$t_{rr}$	reverse recovery time	$I_S = 25\text{ A}$ ; $di_S/dt = -100\text{ A}/\mu\text{s}$ ;	-	33	-	ns
$Q_r$	recovered charge	$V_{GS} = 0\text{ V}$ ; $V_{DS} = 20\text{ V}$	-	30	-	nC

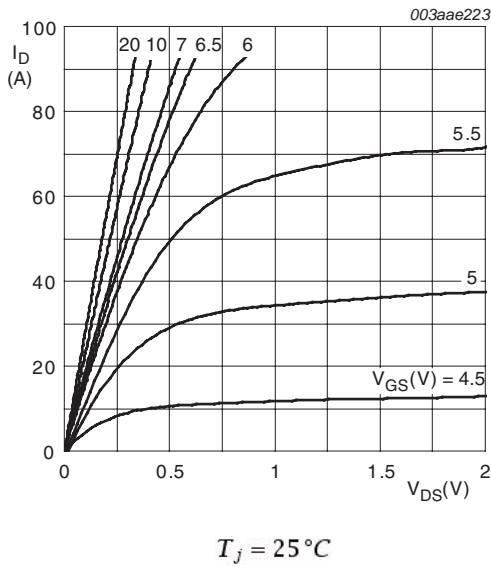


Fig 5. Output characteristics: drain current as a function of drain-source voltage; typical values

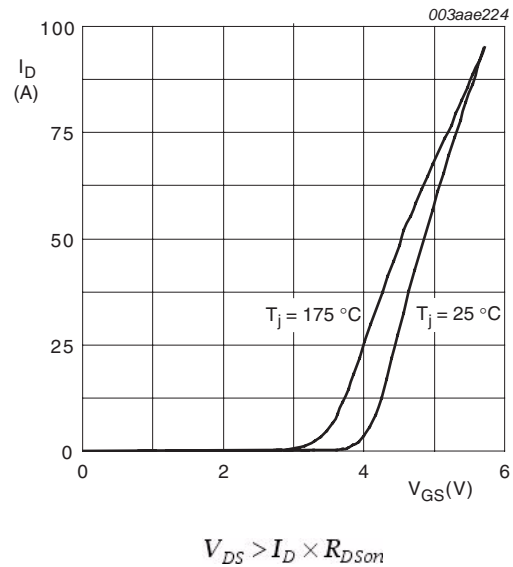


Fig 6. Transfer characteristics: drain current as a function of gate-source voltage; typical values

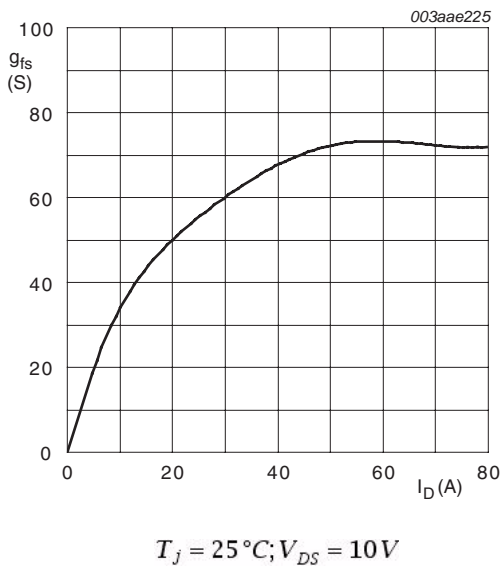


Fig 7. Forward transconductance as a function of drain current; typical values

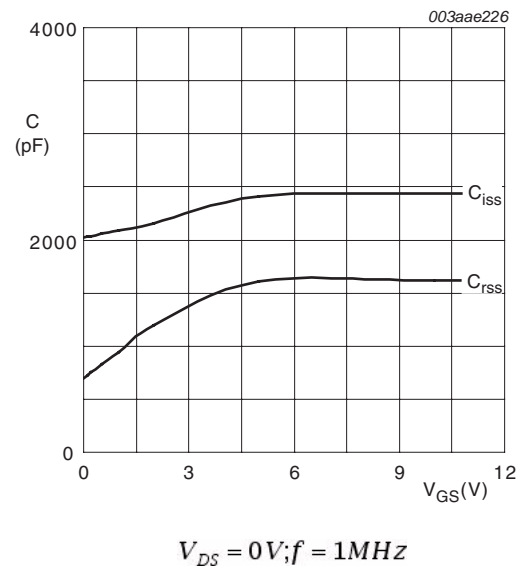
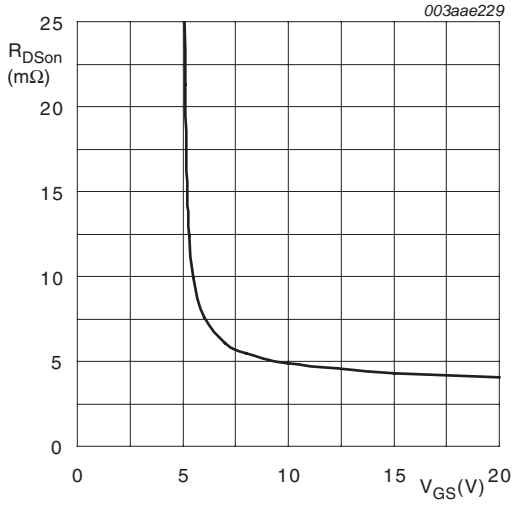
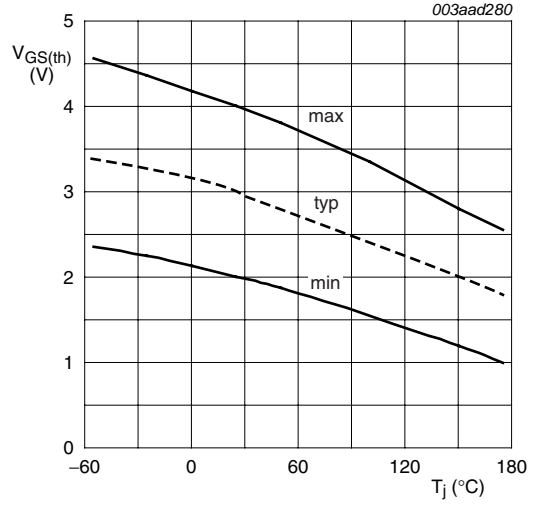


Fig 8. Input and reverse transfer capacitances as a function of gate-source voltage; typical values



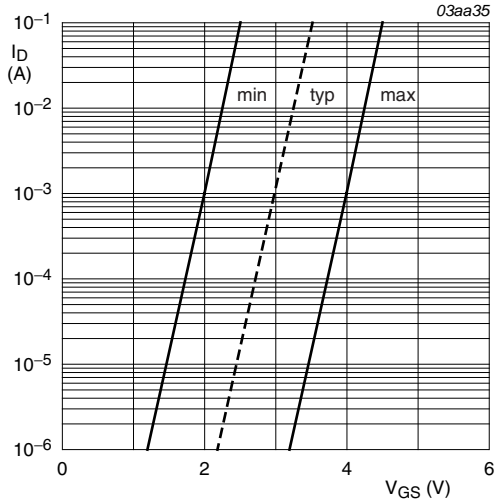
$T_j = 25^\circ\text{C}; I_D = 25\text{A}$

Fig 9. Drain-source on-state resistance as a function of gate-source voltage; typical values.



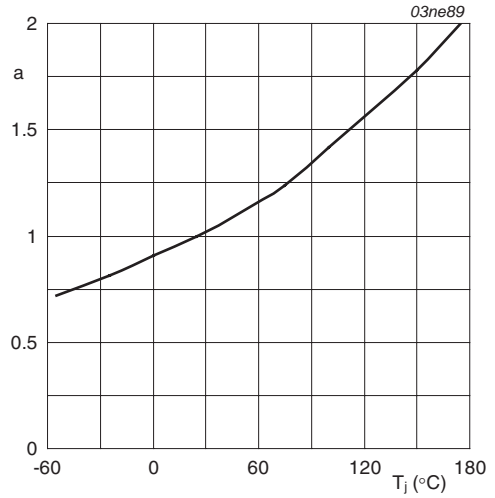
$I_D = 1\text{ mA}; V_{DS} = V_{GS}$

Fig 10. Gate-source threshold voltage as a function of junction temperature



$T_j = 25^\circ\text{C}; V_{DS} = 5\text{V}$

Fig 11. Sub-threshold drain current as a function of gate-source voltage



$$a = \frac{R_{DS(on)}}{R_{DS(on)@25^\circ\text{C}}}$$

Fig 12. Normalized drain-source on-state resistance factor as a function of junction temperature



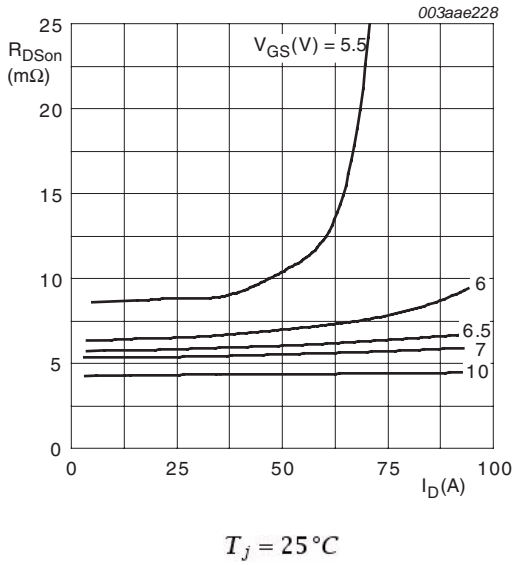


Fig 13. Drain-source on-state resistance as a function of drain current; typical values

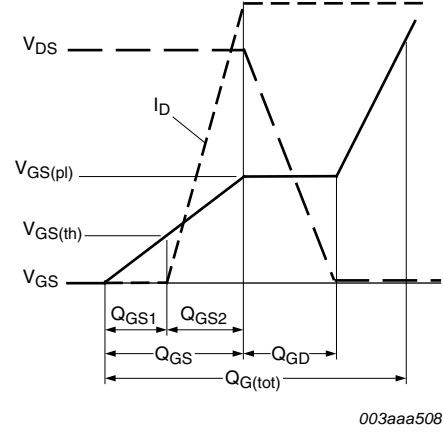


Fig 14. Gate charge waveform definitions

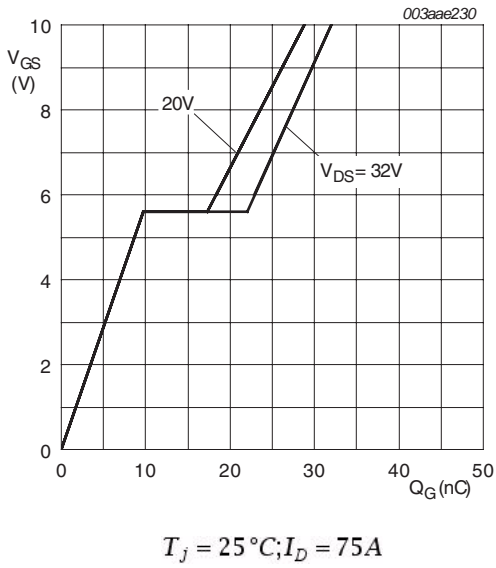


Fig 15. Gate-source voltage as a function of gate charge; typical values

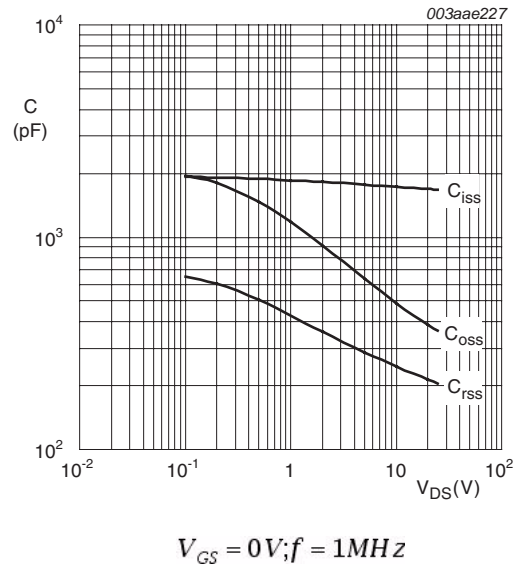


Fig 16. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values

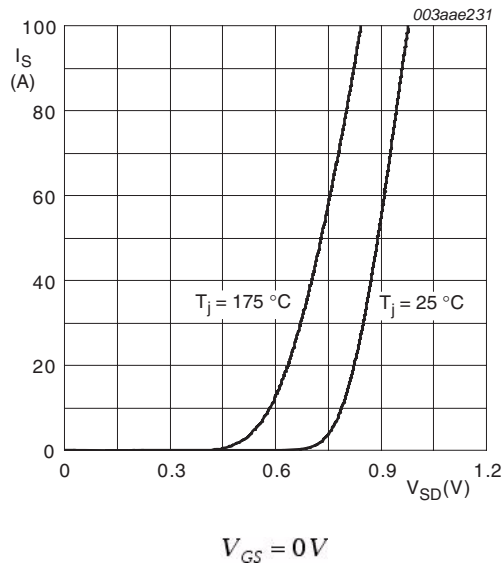


Fig 17. Source current as a function of source-drain voltage; typical values

7. Package outline

Plastic single-ended surface-mounted package (LPAK); 4 leads

SOT669

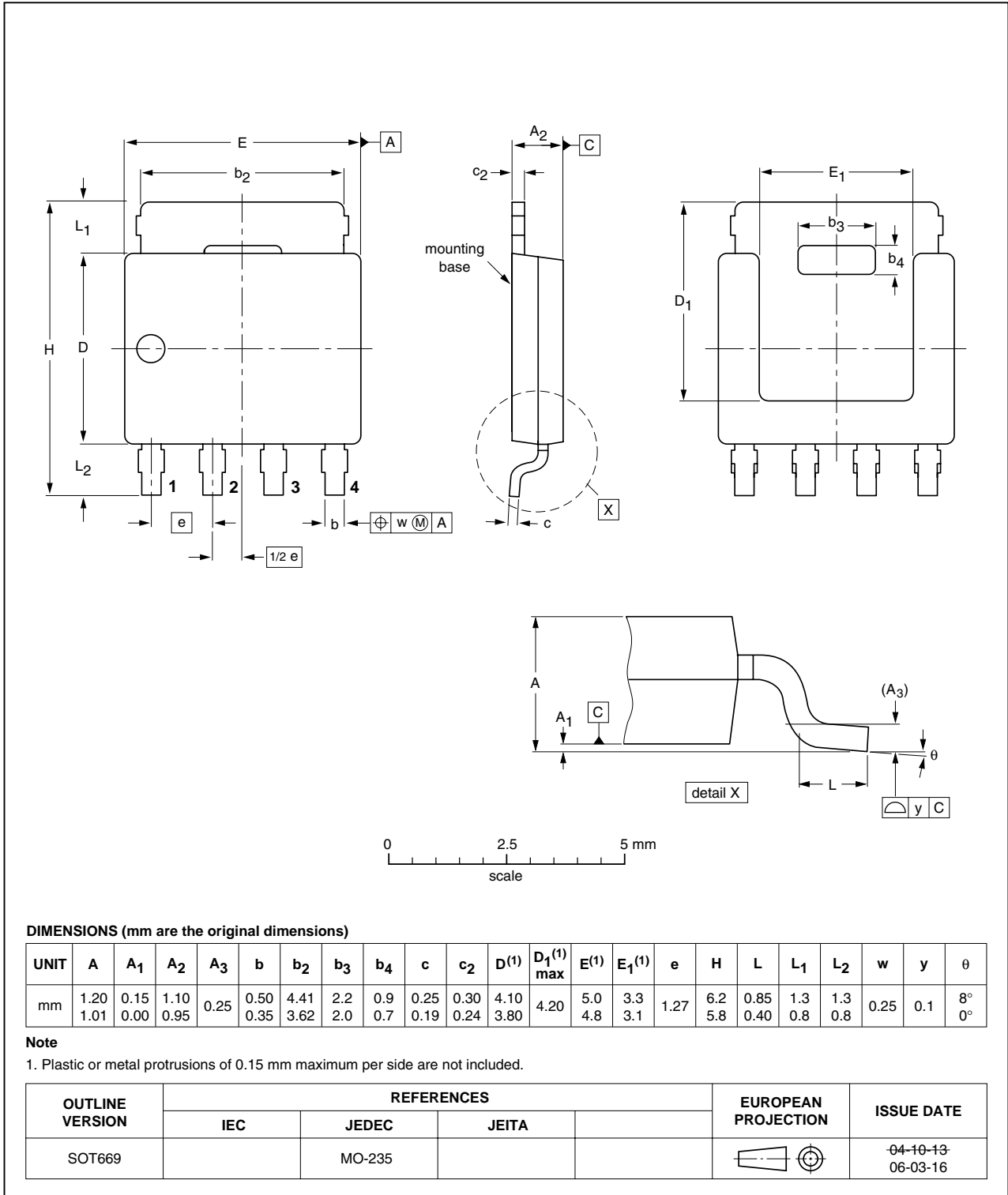


Fig 18. Package outline SOT669 (LPAK)

## 8. Revision history

Table 7. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
PSMN5R8-40YS v.3	20101025	Product data sheet	-	PSMN5R8-40YS v.2
Modifications:	<ul style="list-style-type: none"><li>• Status changed from objective to product.</li><li>• Various changes to content.</li></ul>			
PSMN5R8-40YS v.2	20100526	Objective data sheet	-	PSMN5R8-40YS v.1

## 9. Legal information

### 9.1 Data sheet status

Document status <sup>[1][2]</sup>	Product status <sup>[3]</sup>	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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