



# PSMN2R8-40BS

N-channel 40 V 2.9 mΩ standard level MOSFET in D2PAK

Rev. 1 — 20 March 2012

Product data sheet

## 1. Product profile

### 1.1 General description

Standard level N-channel MOSFET in SOT404 package qualified to 175 °C. This product is designed and qualified for use in a wide range of industrial, communications and domestic equipment.

### 1.2 Features and benefits

- High efficiency due to low switching and conduction losses
- Suitable for standard level gate drive sources

### 1.3 Applications

- DC-to-DC converters
- Motor control
- Load switching
- Server power supplies

### 1.4 Quick reference data

Table 1. Quick reference data

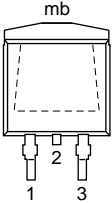
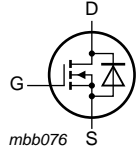
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{DS}$	drain-source voltage	$T_j \geq 25\text{ °C}; T_j \leq 175\text{ °C}$	-	-	40	V
$I_D$	drain current	$T_{mb} = 25\text{ °C}; V_{GS} = 10\text{ V};$ see <a href="#">Figure 1</a>	[1]	-	100	A
$P_{tot}$	total power dissipation	$T_{mb} = 25\text{ °C};$ see <a href="#">Figure 2</a>	-	-	211	W
$T_j$	junction temperature		-55	-	175	°C
<b>Static characteristics</b>						
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = 10\text{ V}; I_D = 10\text{ A}; T_j = 100\text{ °C};$ see <a href="#">Figure 13</a> ; see <a href="#">Figure 14</a>	-	3.58	4.2	mΩ
		$V_{GS} = 10\text{ V}; I_D = 10\text{ A}; T_j = 25\text{ °C};$ see <a href="#">Figure 14</a>	-	2.47	2.9	mΩ
<b>Dynamic characteristics</b>						
$Q_{GD}$	gate-drain charge	$V_{GS} = 10\text{ V}; I_D = 10\text{ A}; V_{DS} = 20\text{ V};$ see <a href="#">Figure 15</a> ; see <a href="#">Figure 16</a>	-	17	-	nC
$Q_{G(tot)}$	total gate charge		-	71	-	nC
<b>Avalanche ruggedness</b>						
$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	$V_{GS} = 10\text{ V}; T_{j(init)} = 25\text{ °C};$ $I_D = 100\text{ A}; V_{sup} \leq 40\text{ V};$ unclamped; $R_{GS} = 50\text{ }\Omega$	-	-	407	mJ

[1] Continuous current rating is limited by package.



## 2. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	G	gate	 <p>SOT404 (D2PAK)</p>	 <p>mbb076</p>
2	D	drain <sup>[1]</sup>		
3	S	source		
mb	D	mounting base; connected to drain		

[1] It is not possible to make connection to pin 2

## 3. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
PSMN2R8-40BS	D2PAK	plastic single-ended surface-mounted package (D2PAK); 3 leads (one lead cropped)	SOT404

## 4. Marking

Table 4. Marking codes

Type number	Marking code
PSMN2R8-40BS	PSMN2R8-40BS

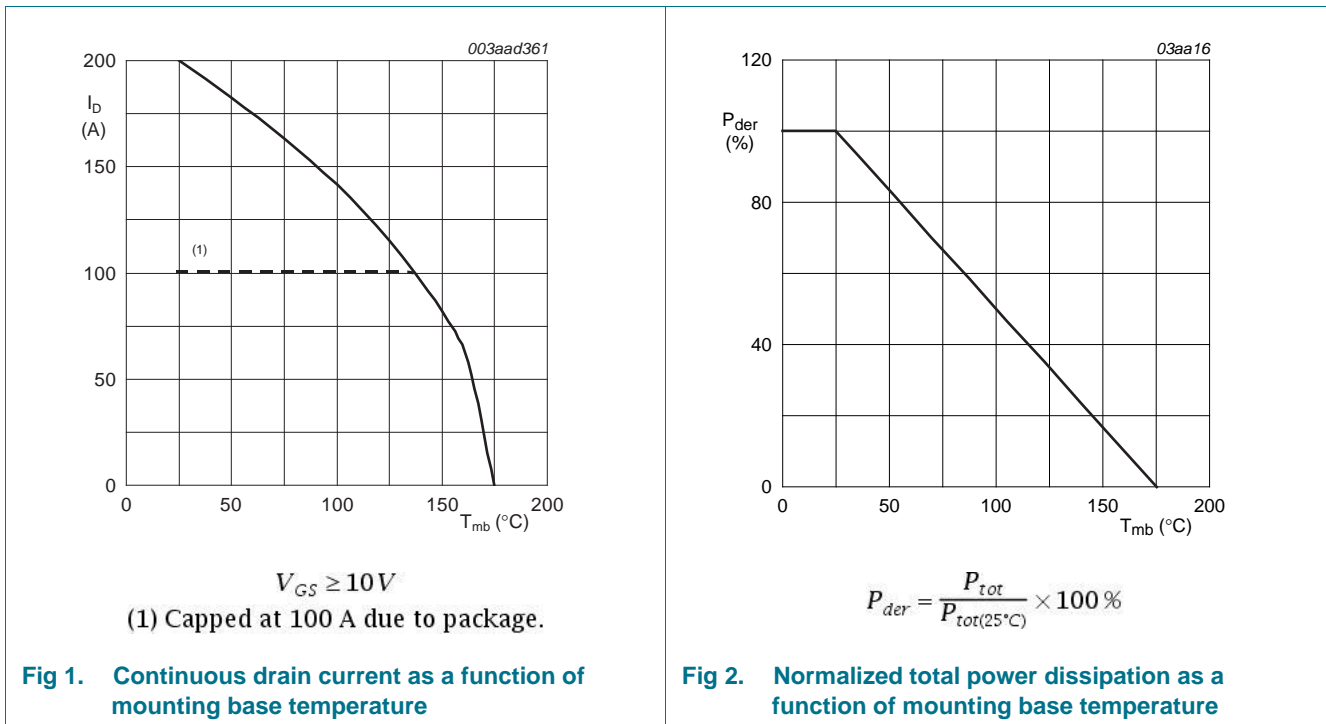
## 5. Limiting values

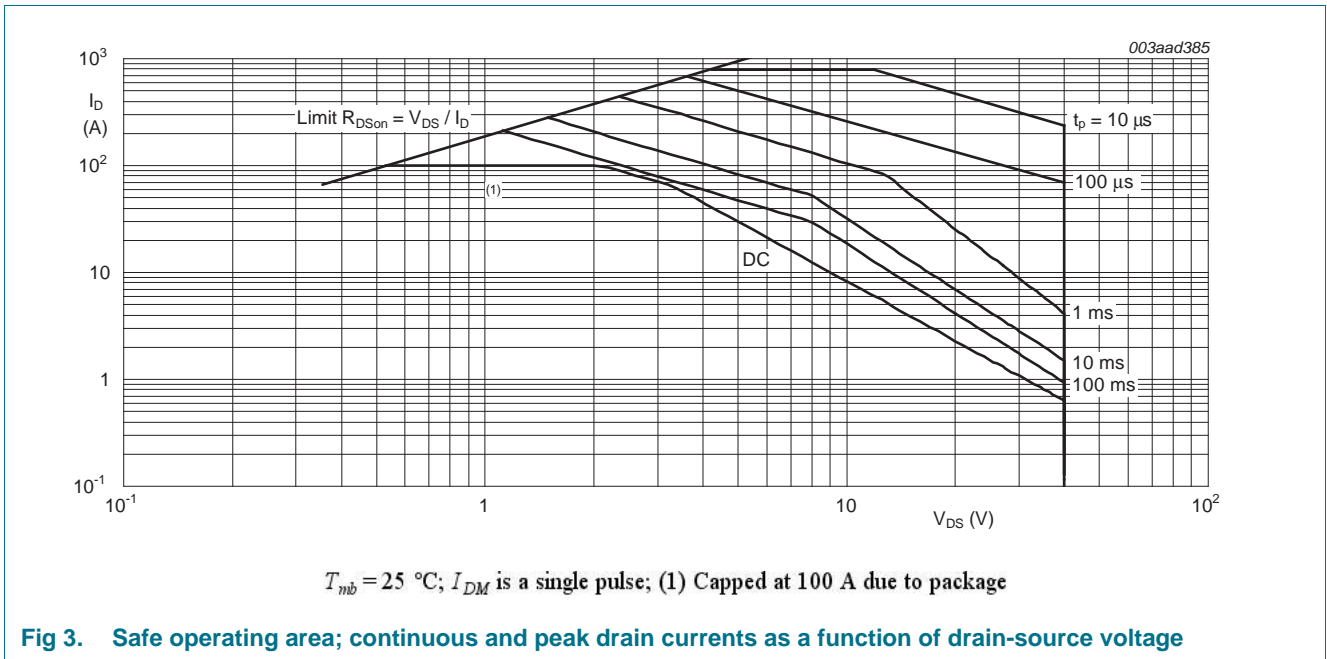
**Table 5. Limiting values**

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit	
$V_{DS}$	drain-source voltage	$T_j \geq 25\text{ °C}; T_j \leq 175\text{ °C}$	-	40	V	
$V_{DGR}$	drain-gate voltage	$T_j \geq 25\text{ °C}; T_j \leq 175\text{ °C}; R_{GS} = 20\text{ k}\Omega$	-	40	V	
$V_{GS}$	gate-source voltage		-20	20	V	
$I_D$	drain current	$V_{GS} = 10\text{ V}; T_{mb} = 100\text{ °C}$ ; see <a href="#">Figure 1</a>	[1]	-	100	A
		$V_{GS} = 10\text{ V}; T_{mb} = 25\text{ °C}$ ; see <a href="#">Figure 1</a>	[1]	-	100	A
$I_{DM}$	peak drain current	pulsed; $t_p \leq 10\text{ }\mu\text{s}$ ; $T_{mb} = 25\text{ °C}$ ; see <a href="#">Figure 3</a>	-	797	A	
$P_{tot}$	total power dissipation	$T_{mb} = 25\text{ °C}$ ; see <a href="#">Figure 2</a>	-	211	W	
$T_{stg}$	storage temperature		-55	175	°C	
$T_j$	junction temperature		-55	175	°C	
$T_{sld(M)}$	peak soldering temperature		-	260	°C	
<b>Source-drain diode</b>						
$I_S$	source current	$T_{mb} = 25\text{ °C}$	[1]	-	100	A
$I_{SM}$	peak source current	pulsed; $t_p \leq 10\text{ }\mu\text{s}$ ; $T_{mb} = 25\text{ °C}$	-	797	A	
<b>Avalanche ruggedness</b>						
$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	$V_{GS} = 10\text{ V}; T_{j(\text{init})} = 25\text{ °C}; I_D = 100\text{ A}; V_{sup} \leq 40\text{ V}$ ; unclamped; $R_{GS} = 50\text{ }\Omega$	-	407	mJ	

[1] Continuous current rating is limited by package.

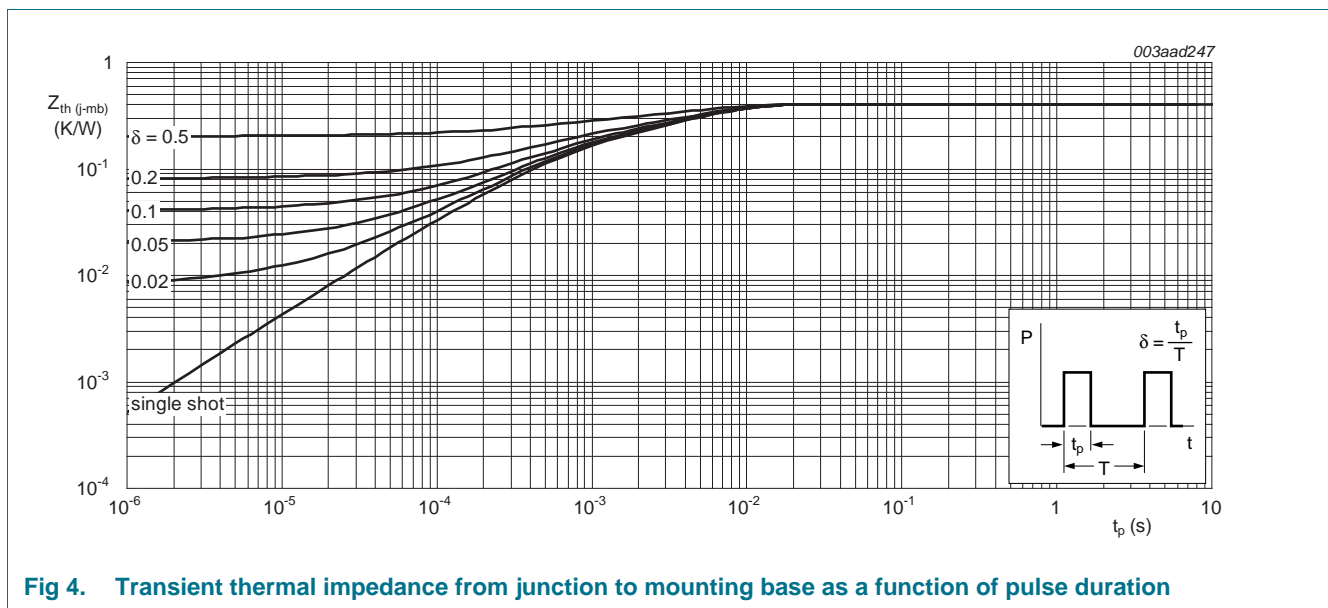




## 6. Thermal characteristics

**Table 6. Thermal characteristics**

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	see <a href="#">Figure 4</a>	-	0.4	0.7	K/W
$R_{th(j-a)}$	thermal resistance from junction to ambient	Minimum footprint; mounted on a printed circuit board	-	50	-	K/W



## 7. Characteristics

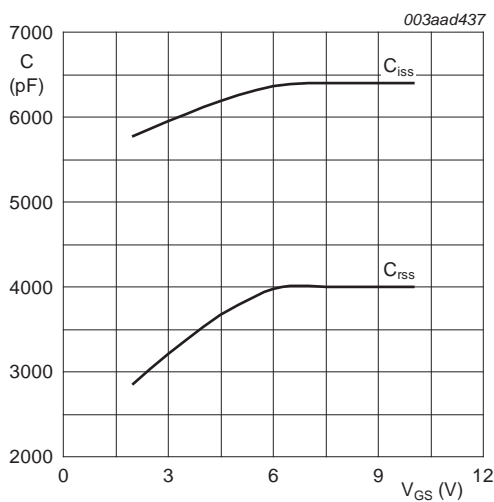
**Table 7. Characteristics**

Tested to JEDEC standards where applicable.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>Static characteristics</b>						
V <sub>(BR)DSS</sub>	drain-source breakdown voltage	I <sub>D</sub> = 250 μA; V <sub>GS</sub> = 0 V; T <sub>j</sub> = -55 °C	36	-	-	V
		I <sub>D</sub> = 250 μA; V <sub>GS</sub> = 0 V; T <sub>j</sub> = 25 °C	40	-	-	V
V <sub>GS(th)</sub>	gate-source threshold voltage	I <sub>D</sub> = 1 mA; V <sub>DS</sub> = V <sub>GS</sub> ; T <sub>j</sub> = -55 °C; see <a href="#">Figure 10</a> ; see <a href="#">Figure 11</a>	-	-	4.6	V
		I <sub>D</sub> = 1 mA; V <sub>DS</sub> = V <sub>GS</sub> ; T <sub>j</sub> = 175 °C; see <a href="#">Figure 10</a> ; see <a href="#">Figure 12</a>	1	-	-	V
		I <sub>D</sub> = 1 mA; V <sub>DS</sub> = V <sub>GS</sub> ; T <sub>j</sub> = 25 °C; see <a href="#">Figure 10</a> ; see <a href="#">Figure 11</a>	2.3	3	4	V
I <sub>DSS</sub>	drain leakage current	V <sub>DS</sub> = 40 V; V <sub>GS</sub> = 0 V; T <sub>j</sub> = 25 °C	-	0.3	10	μA
		V <sub>DS</sub> = 40 V; V <sub>GS</sub> = 0 V; T <sub>j</sub> = 125 °C	-	-	150	μA
I <sub>GSS</sub>	gate leakage current	V <sub>GS</sub> = 20 V; V <sub>DS</sub> = 0 V; T <sub>j</sub> = 25 °C	-	10	100	nA
		V <sub>GS</sub> = -20 V; V <sub>DS</sub> = 0 V; T <sub>j</sub> = 25 °C	-	10	100	nA
R <sub>DS(on)</sub>	drain-source on-state resistance	V <sub>GS</sub> = 10 V; I <sub>D</sub> = 10 A; T <sub>j</sub> = 100 °C; see <a href="#">Figure 13</a> ; see <a href="#">Figure 14</a>	-	3.58	4.2	mΩ
		V <sub>GS</sub> = 10 V; I <sub>D</sub> = 10 A; T <sub>j</sub> = 175 °C; see <a href="#">Figure 13</a> ; see <a href="#">Figure 14</a>	-	4.94	5.8	mΩ
		V <sub>GS</sub> = 10 V; I <sub>D</sub> = 10 A; T <sub>j</sub> = 25 °C; see <a href="#">Figure 14</a>	-	2.47	2.9	mΩ
R <sub>G</sub>	internal gate resistance (AC)	f = 1 MHz	-	0.7	-	Ω
<b>Dynamic characteristics</b>						
Q <sub>G(tot)</sub>	total gate charge	I <sub>D</sub> = 0 A; V <sub>DS</sub> = 0 V; V <sub>GS</sub> = 10 V	-	61	-	nC
		I <sub>D</sub> = 10 A; V <sub>DS</sub> = 20 V; V <sub>GS</sub> = 10 V; see <a href="#">Figure 15</a> ; see <a href="#">Figure 16</a>	-	71	-	nC
Q <sub>GS</sub>	gate-source charge		-	21	-	nC
Q <sub>GS(th)</sub>	pre-threshold gate-source charge		-	13	-	nC
Q <sub>GS(th-pl)</sub>	post-threshold gate-source charge		-	8.5	-	nC
Q <sub>GD</sub>	gate-drain charge		-	17	-	nC
V <sub>GS(pl)</sub>	gate-source plateau voltage	I <sub>D</sub> = 10 A; V <sub>DS</sub> = 20 V; see <a href="#">Figure 15</a> ; see <a href="#">Figure 16</a>	-	4.7	-	V
C <sub>iss</sub>	input capacitance	V <sub>DS</sub> = 20 V; V <sub>GS</sub> = 0 V; f = 1 MHz; T <sub>j</sub> = 25 °C; see <a href="#">Figure 17</a>	-	4491	-	pF
C <sub>oss</sub>	output capacitance		-	937	-	pF
C <sub>rss</sub>	reverse transfer capacitance		-	464	-	pF
t <sub>d(on)</sub>	turn-on delay time	V <sub>DS</sub> = 20 V; R <sub>L</sub> = 0.8 Ω; V <sub>GS</sub> = 10 V; R <sub>G(ext)</sub> = 4.7 Ω	-	28	-	ns
t <sub>r</sub>	rise time		-	29	-	ns
t <sub>d(off)</sub>	turn-off delay time		-	52	-	ns
t <sub>f</sub>	fall time		-	23	-	ns

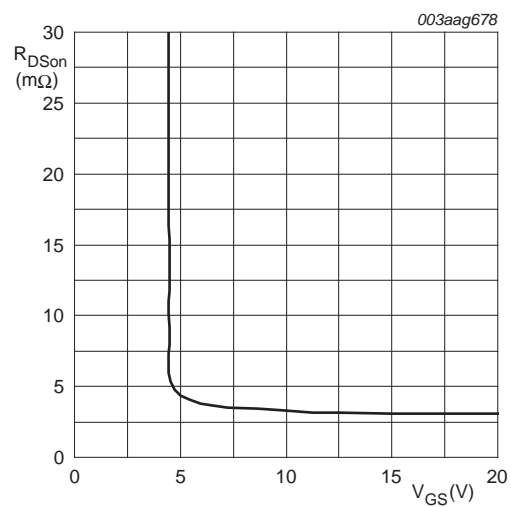
**Table 7. Characteristics ...continued**  
 Tested to JEDEC standards where applicable.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>Source-drain diode</b>						
$V_{SD}$	source-drain voltage	$I_S = 10\text{ A}$ ; $V_{GS} = 0\text{ V}$ ; $T_j = 25\text{ °C}$ ; see <a href="#">Figure 18</a>	-	0.85	1.2	V
$t_{rr}$	reverse recovery time	$I_S = 10\text{ A}$ ; $di_S/dt = -100\text{ A}/\mu\text{s}$ ; $V_{GS} = 0\text{ V}$ ; $V_{DS} = 20\text{ V}$	-	47	-	ns
$Q_r$	recovered charge	$I_S = 10\text{ A}$ ; $di_S/dt = -100\text{ A}/\mu\text{s}$ ; $V_{GS} = 0\text{ V}$ ; $V_{DS} = 20\text{ V}$ ; $T_j = 25\text{ °C}$	-	61	-	nC



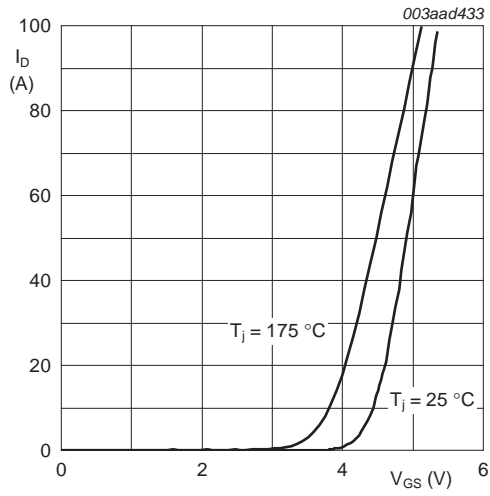
$V_{DS} = 0\text{ V}$ ;  $f = 1\text{ MHz}$

**Fig 5. Input and reverse transfer capacitances as a function of gate-source voltage; typical values**



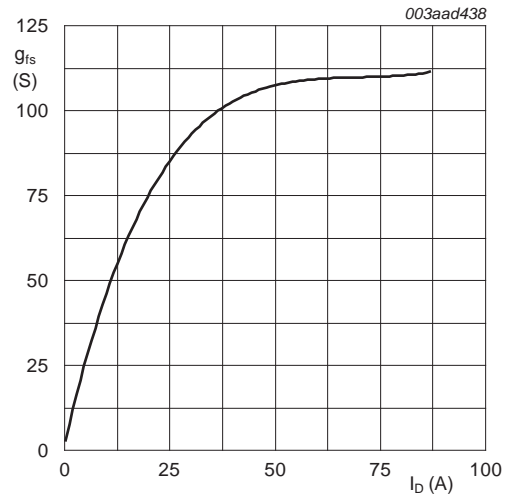
$T_j = 25\text{ °C}$ ;  $I_D = 25\text{ A}$

**Fig 6. Drain-source on-state resistance as a function of gate-source voltage; typical values**



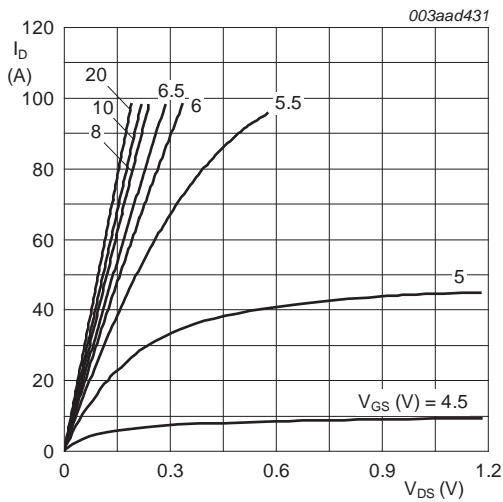
$$V_{DS} > I_D \times R_{DS(on)}$$

Fig 7. Transfer characteristics: drain current as a function of gate-source voltage; typical values



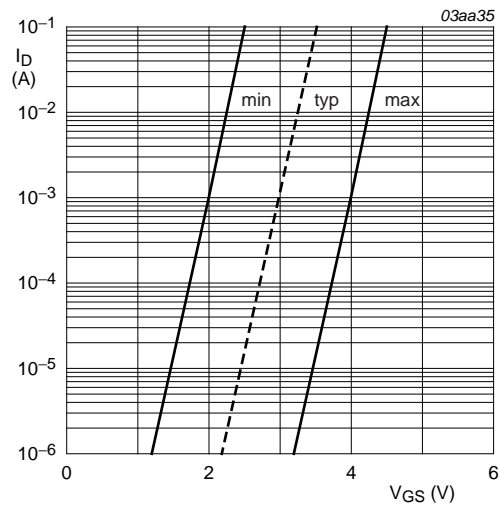
$$T_j = 25^\circ C; V_{DS} = 15V$$

Fig 8. Forward transconductance as a function of drain current; typical values



$$T_j = 25^\circ C$$

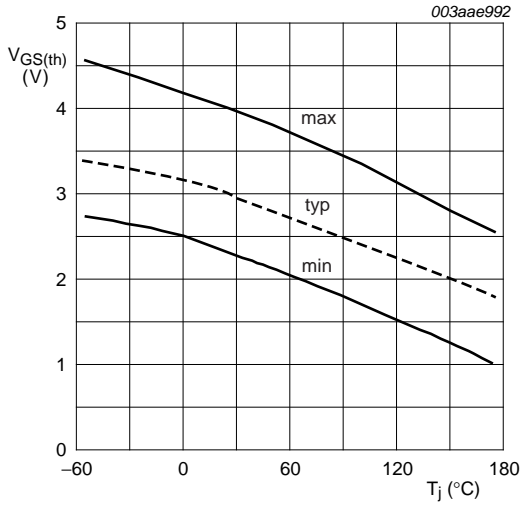
Fig 9. Output characteristics: drain current as a function of drain-source voltage; typical values



$$T_j = 25^\circ C; V_{DS} = 5V$$

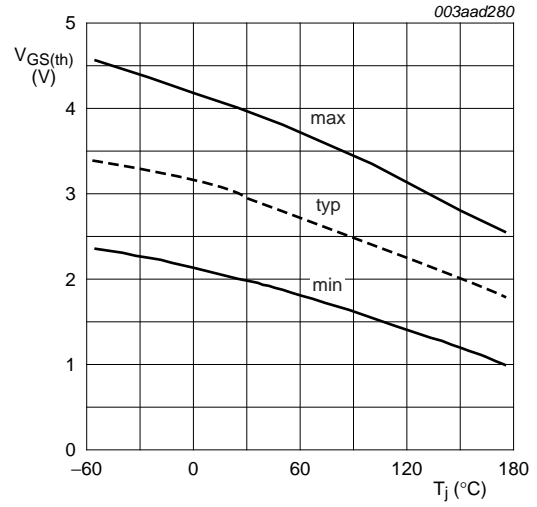
Fig 10. Sub-threshold drain current as a function of gate-source voltage





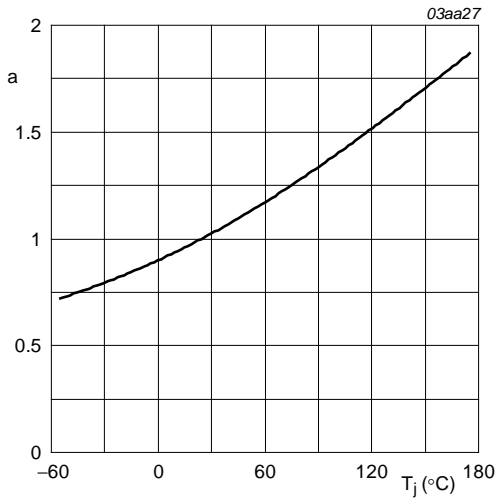
$$I_D = 1 \text{ mA}; V_{DS} = V_{GS}$$

Fig 11. Gate-source threshold voltage as a function of junction temperature



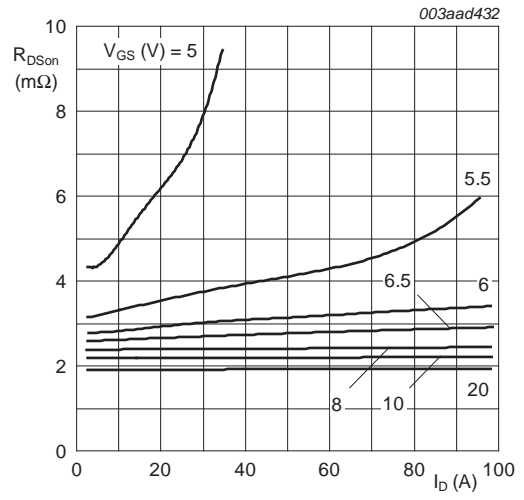
$$I_D = 1 \text{ mA}; V_{DS} = V_{GS}$$

Fig 12. Gate-source threshold voltage as a function of junction temperature



$$a = \frac{R_{DSon}}{R_{DSon(25^\circ\text{C})}}$$

Fig 13. Normalized drain-source on-state resistance factor as a function of junction temperature



$$T_j = 25^\circ\text{C}$$

Fig 14. Drain-source on-state resistance as a function of drain current; typical values

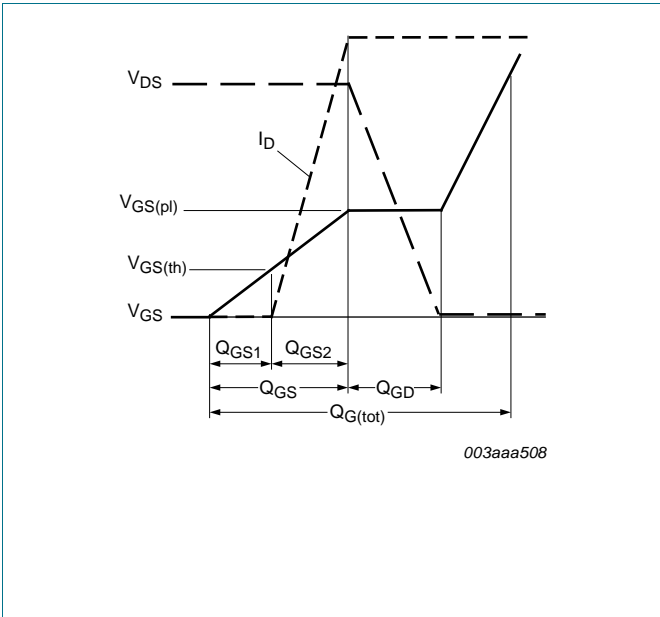


Fig 15. Gate charge waveform definitions

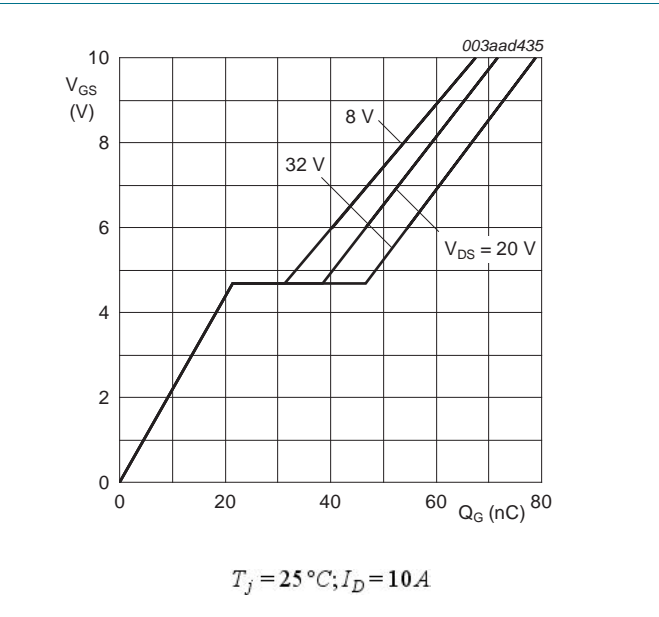


Fig 16. Gate-source voltage as a function of gate charge; typical values

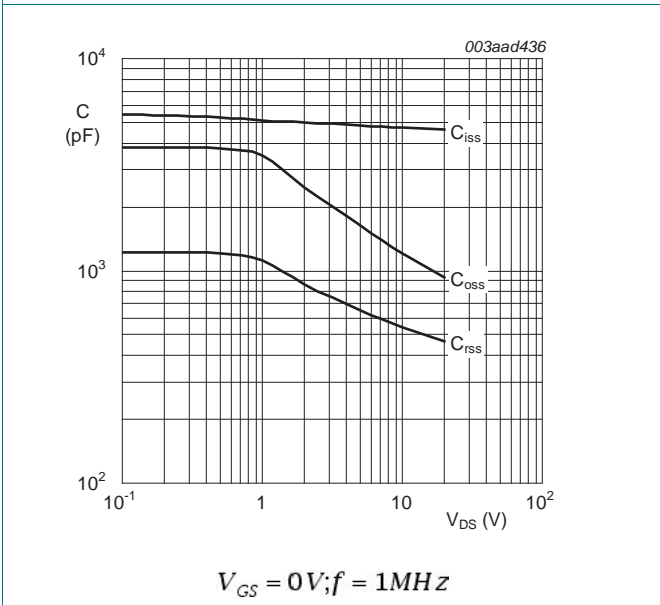


Fig 17. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values

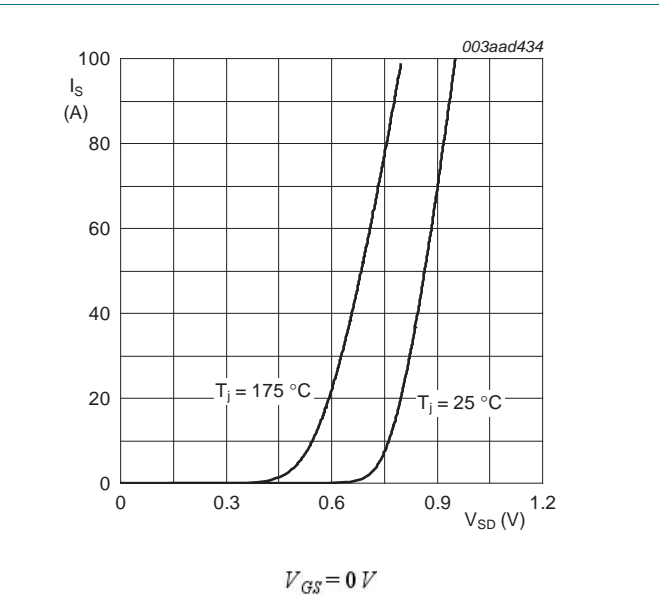


Fig 18. Source current as a function of source-drain voltage; typical values

### 8. Package outline

Plastic single-ended surface-mounted package (D2PAK); 3 leads (one lead cropped)

SOT404

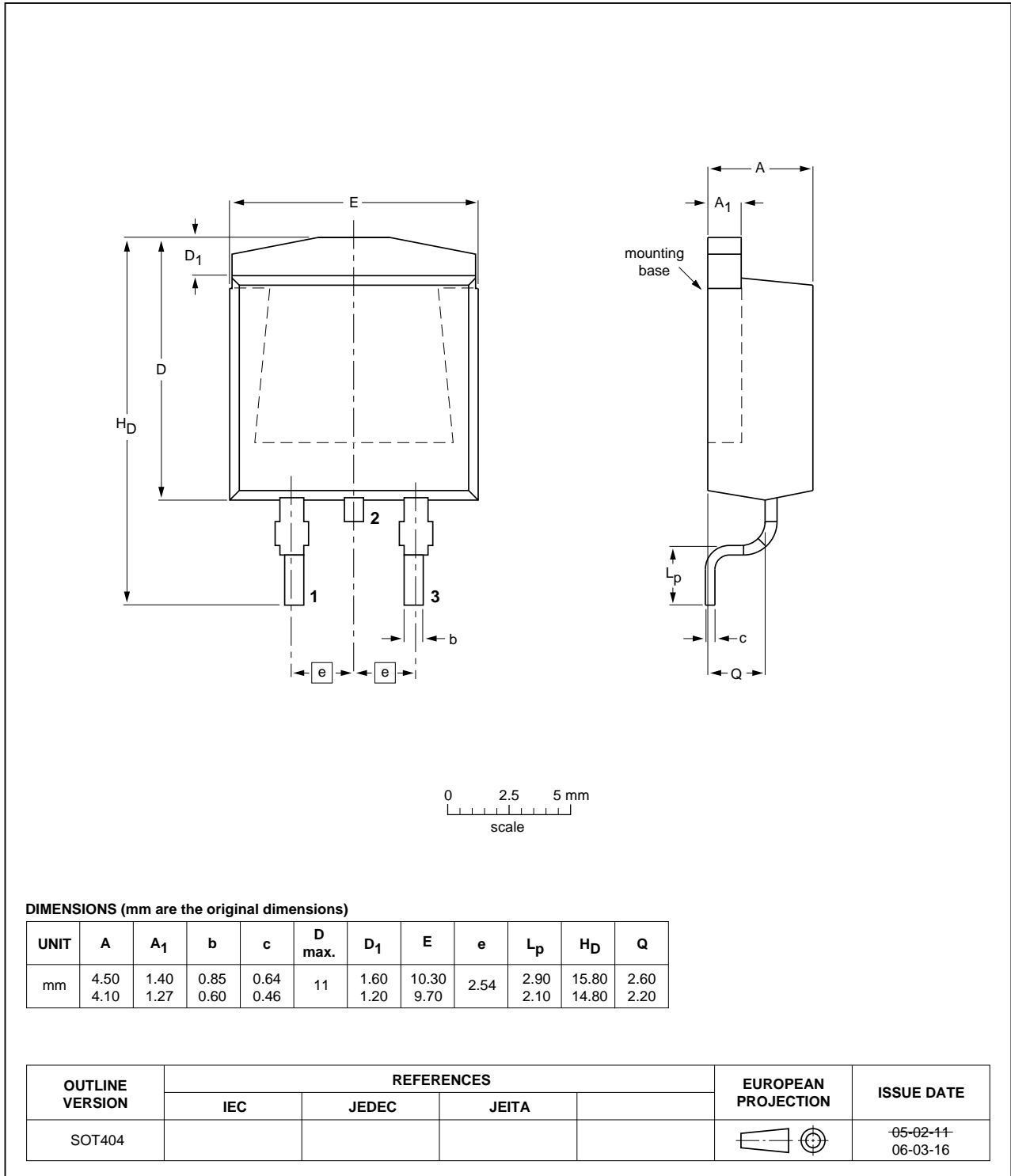


Fig 19. Package outline SOT404 (D2PAK)

## 9. Revision history

Table 8. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
PSMN2R8-40BS v.1	20120320	Product data sheet	-	-

## 10. Legal information

### 10.1 Data sheet status

Document status <sup>[1]</sup> [2]	Product status <sup>[3]</sup>	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

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## 12. Contents

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Please be aware that important notices concerning this document and the product(s) described herein, have been included in section 'Legal information'.

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