



PSMN1R7-30YL

N-channel 30 V 1.7 mΩ logic level MOSFET in LPAK

Rev. 1 — 30 May 2011

Product data sheet

1. Product profile

1.1 General description

Logic level N-channel MOSFET in LPAK package qualified to 175 °C. This product is designed and qualified for use in a wide range of industrial, communications and domestic equipment.

1.2 Features and benefits

- Advanced TrenchMOS provides low RDSon and low gate charge
- High efficiency gains in switching power convertors
- Improved mechanical and thermal characteristics
- LPAK provides maximum power density in a Power SO8 package

1.3 Applications

- DC-to-DC converters
- Lithium-ion battery protection
- Load switching
- Motor control
- Server power supplies

1.4 Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V _{DS}	drain-source voltage	T _j ≥ 25 °C; T _j ≤ 175 °C	-	-	30	V
I _D	drain current	T _{mb} = 25 °C; V _{GS} = 10 V; see Figure 1	-	-	100	A
P _{tot}	total power dissipation	T _{mb} = 25 °C; see Figure 2	-	-	109	W
T _j	junction temperature		-55	-	175	°C
Static characteristics						
R _{DSon}	drain-source on-state resistance	V _{GS} = 10 V; I _D = 15 A; T _j = 100 °C; see Figure 13	-	-	2.4	mΩ
		V _{GS} = 10 V; I _D = 15 A; T _j = 25 °C	-	1.3	1.7	mΩ
Dynamic characteristics						
Q _{GD}	gate-drain charge	V _{GS} = 4.5 V; I _D = 10 A; V _{DS} = 12 V; see Figure 14 ; see Figure 15	-	8.7	-	nC



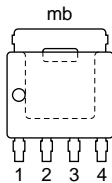
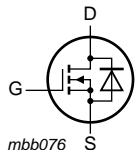
Table 1. Quick reference data ...continued

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$Q_{G(\text{tot})}$	total gate charge	$V_{GS} = 4.5 \text{ V}; I_D = 10 \text{ A};$ $V_{DS} = 12 \text{ V};$ see Figure 14	-	36.2	-	nC
Avalanche ruggedness						
$E_{DS(\text{AL})S}$	non-repetitive drain-source avalanche energy	$V_{GS} = 10 \text{ V}; T_{j(\text{init})} = 25 \text{ }^\circ\text{C};$ $I_D = 100 \text{ A}; V_{\text{sup}} \leq 30 \text{ V};$ $R_{GS} = 50 \text{ } \Omega;$ unclamped	-	-	241	mJ

[1] Continuous current is limited by package.

2. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	S	source		
2	S	source		
3	S	source		
4	G	gate		
mb	D	mounting base; connected to drain		

SOT669 (LFAK; Power-SO8)

3. Ordering information

Table 3. Ordering information

Type number	Package		Version
	Name	Description	
PSMN1R7-30YL	LFAK; Power-SO8	plastic single-ended surface-mounted package; 4 leads	SOT669

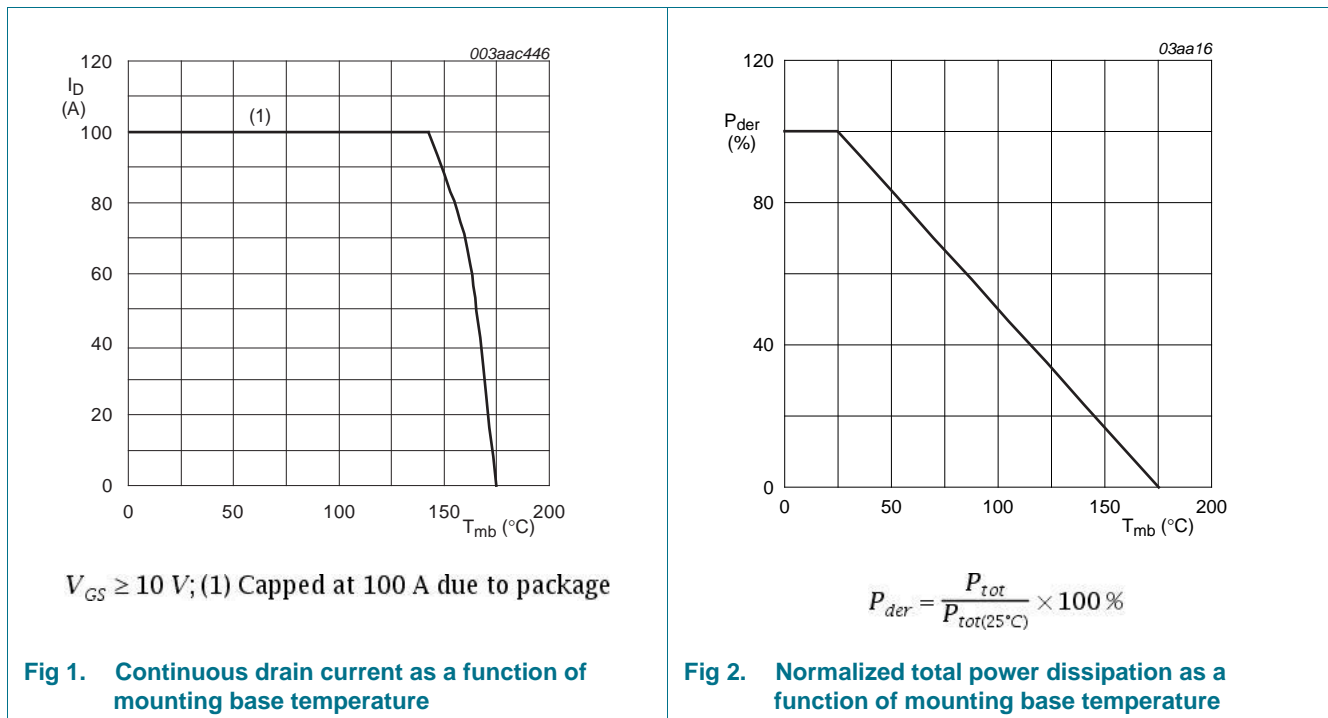
4. Limiting values

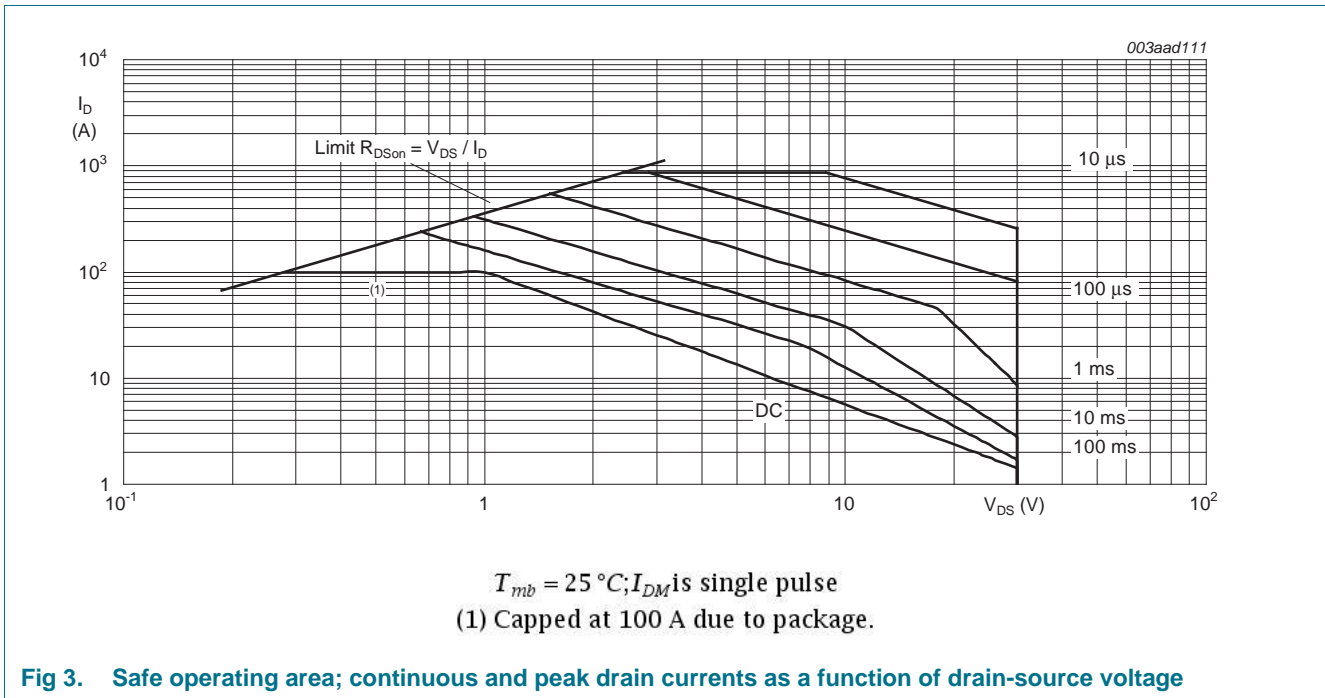
Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V _{DS}	drain-source voltage	T _j ≥ 25 °C; T _j ≤ 175 °C	-	30	V
V _{DSM}	peak drain-source voltage	t _p ≤ 25 ns; f ≤ 500 kHz; E _{DS(AL)} ≤ 360 nJ; pulsed	-	35	V
V _{DGR}	drain-gate voltage	T _j ≥ 25 °C; T _j ≤ 175 °C; R _{GS} = 20 kΩ	-	30	V
V _{GS}	gate-source voltage		-20	20	V
I _D	drain current	V _{GS} = 10 V; T _{mb} = 100 °C; see Figure 1	[1]	100	A
		V _{GS} = 10 V; T _{mb} = 25 °C; see Figure 1	[1]	100	A
I _{DM}	peak drain current	pulsed; t _p ≤ 10 μs; T _{mb} = 25 °C; see Figure 3	-	790	A
P _{tot}	total power dissipation	T _{mb} = 25 °C; see Figure 2	-	109	W
T _{stg}	storage temperature		-55	175	°C
T _j	junction temperature		-55	175	°C
Source-drain diode					
I _S	source current	T _{mb} = 25 °C	[1]	100	A
I _{SM}	peak source current	pulsed; t _p ≤ 10 μs; T _{mb} = 25 °C	-	790	A
Avalanche ruggedness					
E _{DS(AL)S}	non-repetitive drain-source avalanche energy	V _{GS} = 10 V; T _{j(init)} = 25 °C; I _D = 100 A; V _{sup} ≤ 30 V; R _{GS} = 50 Ω; unclamped	-	241	mJ

[1] Continuous current is limited by package.

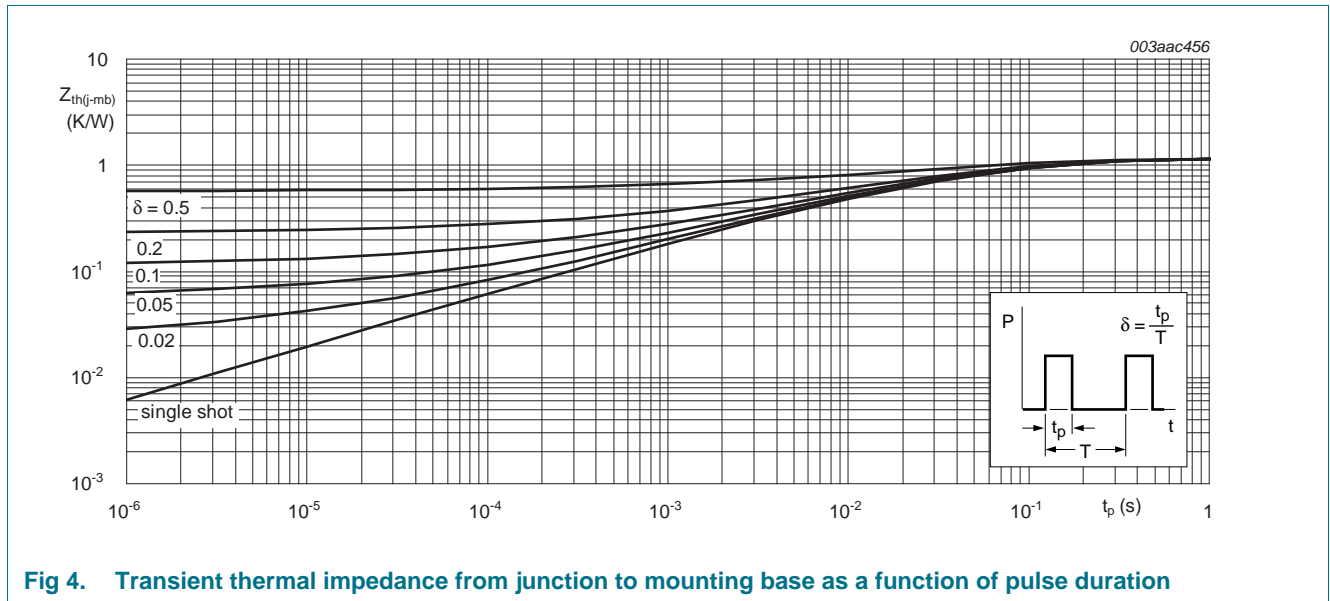




5. Thermal characteristics

Table 5. Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	see Figure 4	-	0.5	1.1	K/W



6. Characteristics

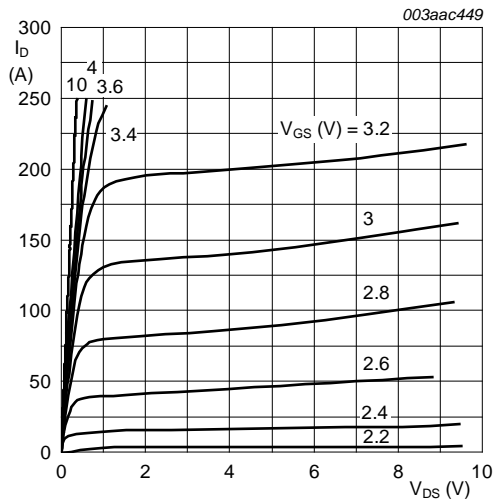
Table 6. Characteristics

Tested to JEDEC standards where applicable.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static characteristics						
$V_{(BR)DSS}$	drain-source breakdown voltage	$I_D = 250 \mu A; V_{GS} = 0 V; T_j = 25 \text{ }^\circ C$	30	-	-	V
		$I_D = 250 \mu A; V_{GS} = 0 V; T_j = -55 \text{ }^\circ C$	27	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	$I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = 25 \text{ }^\circ C$; see Figure 11 ; see Figure 12	1.3	1.7	2.15	V
		$I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = 150 \text{ }^\circ C$; see Figure 12	0.65	-	-	V
		$I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = -55 \text{ }^\circ C$; see Figure 12	-	-	2.45	V
I_{DSS}	drain leakage current	$V_{DS} = 30 V; V_{GS} = 0 V; T_j = 25 \text{ }^\circ C$	-	-	1	μA
		$V_{DS} = 30 V; V_{GS} = 0 V; T_j = 150 \text{ }^\circ C$	-	-	100	μA
I_{GSS}	gate leakage current	$V_{GS} = 16 V; V_{DS} = 0 V; T_j = 25 \text{ }^\circ C$	-	-	100	nA
		$V_{GS} = -16 V; V_{DS} = 0 V; T_j = 25 \text{ }^\circ C$	-	-	100	nA
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = 4.5 V; I_D = 15 A; T_j = 25 \text{ }^\circ C$	-	1.8	2.1	mΩ
		$V_{GS} = 10 V; I_D = 15 A; T_j = 150 \text{ }^\circ C$; see Figure 13	-	-	2.8	mΩ
		$V_{GS} = 10 V; I_D = 15 A; T_j = 100 \text{ }^\circ C$; see Figure 13	-	-	2.4	mΩ
		$V_{GS} = 10 V; I_D = 15 A; T_j = 25 \text{ }^\circ C$	-	1.3	1.7	mΩ
R_G	gate resistance	$f = 1 \text{ MHz}$	-	0.77	1.5	Ω
Dynamic characteristics						
$Q_{G(tot)}$	total gate charge	$I_D = 10 A; V_{DS} = 12 V; V_{GS} = 10 V$; see Figure 14 ; see Figure 15	-	77.9	-	nC
		$I_D = 0 A; V_{DS} = 0 V; V_{GS} = 10 V$	-	70	-	nC
		$I_D = 10 A; V_{DS} = 12 V; V_{GS} = 4.5 V$; see Figure 14	-	36.2	-	nC
Q_{GS}	gate-source charge	$I_D = 10 A; V_{DS} = 12 V; V_{GS} = 4.5 V$; see Figure 14 ; see Figure 15	-	11.6	-	nC
$Q_{GS(th)}$	pre-threshold gate-source charge		-	8	-	nC
$Q_{GS(th-pl)}$	post-threshold gate-source charge		-	3.6	-	nC
Q_{GD}	gate-drain charge		-	8.7	-	nC
$V_{GS(pl)}$	gate-source plateau voltage	$V_{DS} = 12 V$; see Figure 14 ; see Figure 15	-	2.34	-	V
C_{iss}	input capacitance	$V_{DS} = 12 V; V_{GS} = 0 V; f = 1 \text{ MHz}$;	-	5057	-	pF
C_{oss}	output capacitance	$T_j = 25 \text{ }^\circ C$; see Figure 16	-	1082	-	pF
C_{riss}	reverse transfer capacitance		-	398	-	pF
$t_{d(on)}$	turn-on delay time	$V_{DS} = 12 V; R_L = 0.5 \text{ } \Omega; V_{GS} = 4.5 V$;	-	46	-	ns
t_r	rise time	$R_{G(ext)} = 4.7 \text{ } \Omega$	-	72	-	ns
$t_{d(off)}$	turn-off delay time		-	76	-	ns
t_f	fall time		-	34	-	ns

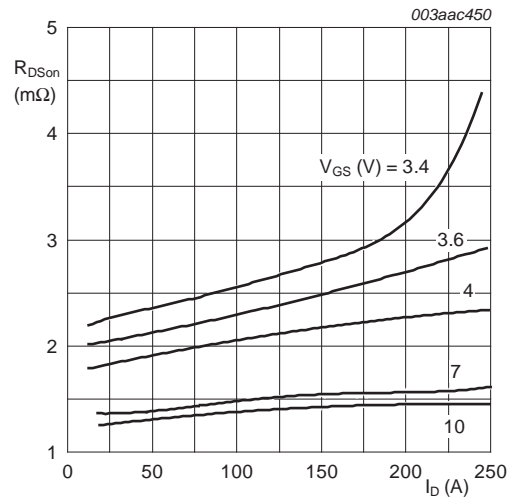
Table 6. Characteristics ...continued
Tested to JEDEC standards where applicable.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Source-drain diode						
V_{SD}	source-drain voltage	$I_S = 25\text{ A}$; $V_{GS} = 0\text{ V}$; $T_j = 25\text{ °C}$; see Figure 17	-	0.78	1.2	V
t_{rr}	reverse recovery time	$I_S = 20\text{ A}$; $dI_S/dt = -100\text{ A}/\mu\text{s}$; $V_{GS} = 0\text{ V}$; $V_{DS} = 20\text{ V}$	-	45	-	ns
Q_r	recovered charge		-	56	-	nC



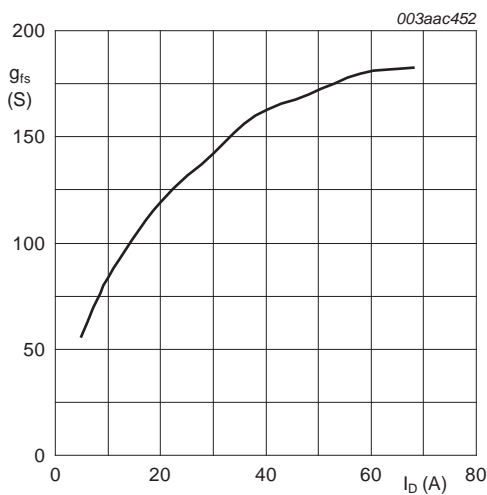
$T_j = 25\text{ °C}$; $t_p = 300\mu\text{s}$

Fig 5. Output characteristics: drain current as a function of drain-source voltage; typical values



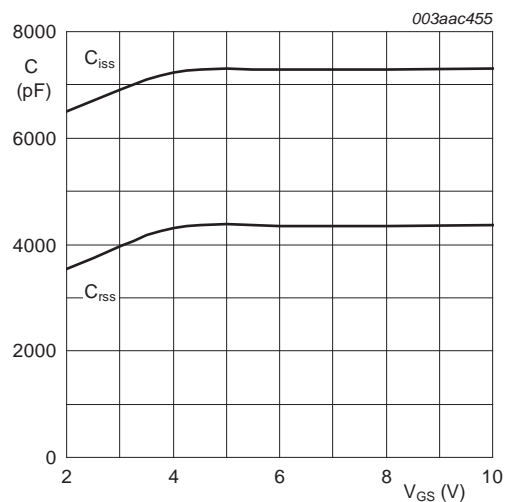
$T_j = 25\text{ °C}$; $t_p = 300\mu\text{s}$

Fig 6. Drain-source on-state resistance as a function of drain current; typical values



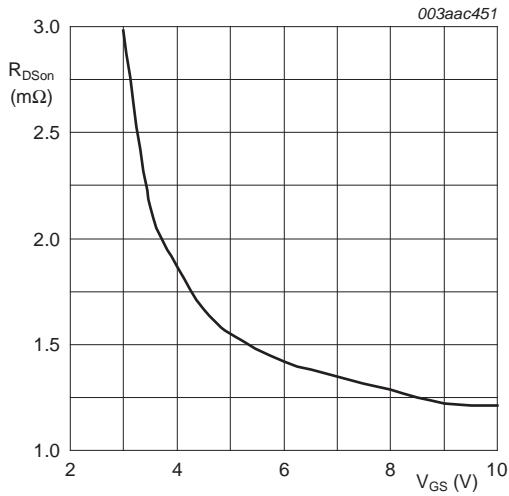
$T_j = 25\text{ °C}$; $V_{DS} = 15\text{ V}$

Fig 7. Forward transconductance as a function of drain current; typical values



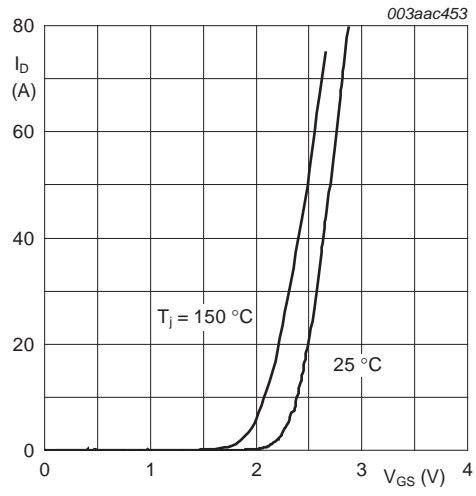
$V_{DS} = 0\text{ V}$; $f = 1\text{ MHz}$

Fig 8. Input and reverse transfer capacitances as a function of gate-source voltage; typical values



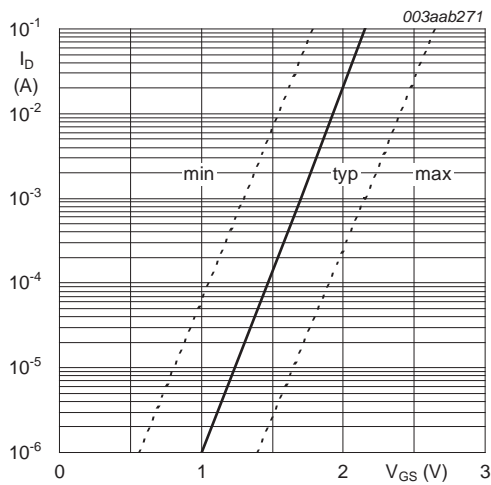
$T_j = 25\text{ }^\circ\text{C}; I_D = 15\text{ A}$

Fig 9. Drain-source on-state resistance as a function of gate-source voltage; typical values



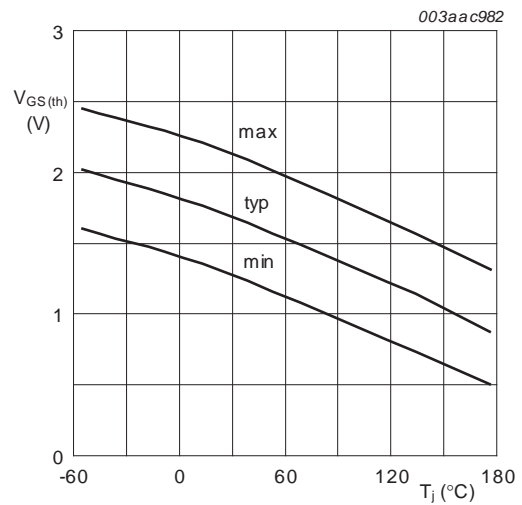
$V_{DS} = 10\text{ V}$

Fig 10. Transfer characteristics: drain current as a function of gate-source voltage; typical values



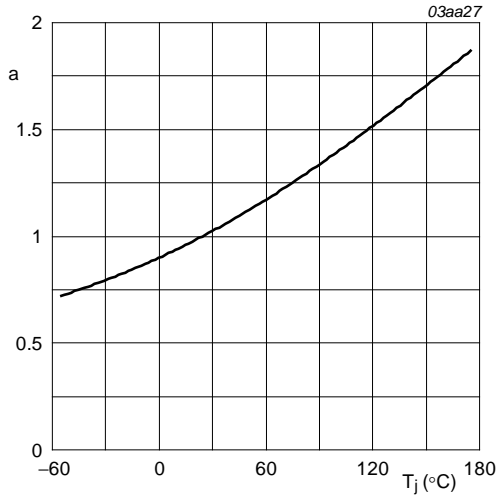
$T_j = 25\text{ }^\circ\text{C}; V_{DS} = 5\text{ V}$

Fig 11. Sub-threshold drain current as a function of gate-source voltage



$I_D = 1\text{ mA}; V_{DS} = V_{GS}$

Fig 12. Gate-source threshold voltage as a function of junction temperature



$$a = \frac{R_{DS(on)}}{R_{DS(on)25^{\circ}\text{C}}}$$

Fig 13. Normalized drain-source on-state resistance factor as a function of junction temperature

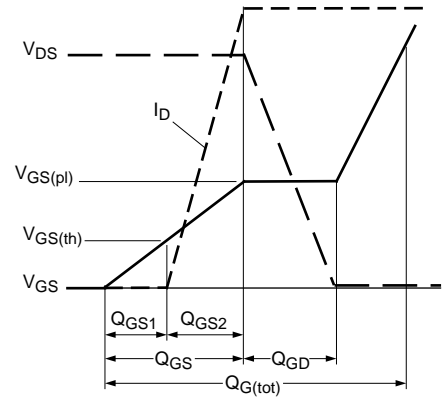
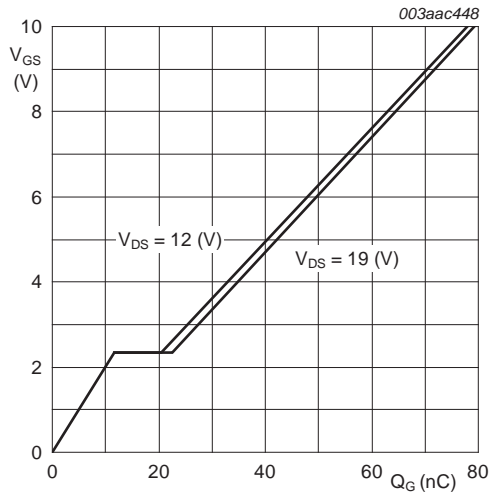
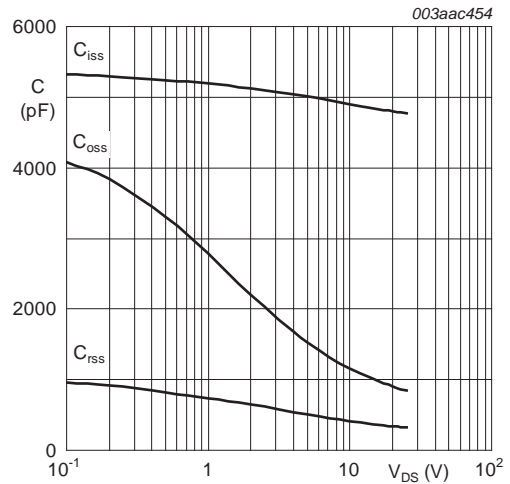


Fig 14. Gate charge waveform definitions



$T_j = 25^{\circ}\text{C}; I_D = 10\text{A}$

Fig 15. Gate-source voltage as a function of gate charge; typical values



$V_{GS} = 0\text{V}; f = 1\text{MHz}$

Fig 16. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values

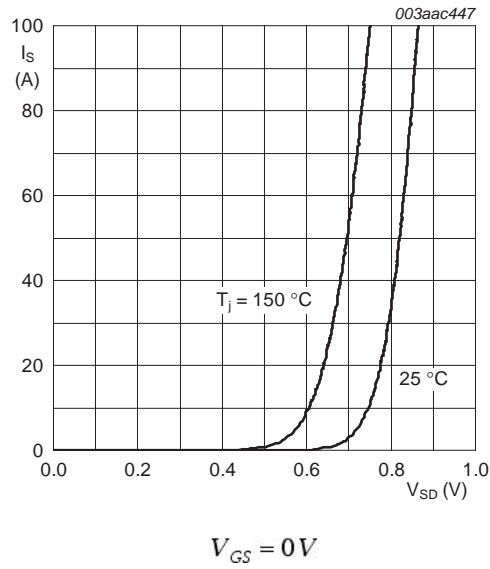


Fig 17. Source (diode forward) current as a function of source-drain (diode forward) voltage; typical values

7. Package outline

Plastic single-ended surface-mounted package (LPAK; Power-SO8); 4 leads

SOT669



Fig 18. Package outline SOT669 (LPAK; Power-SO8)

8. Revision history

Table 7. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
PSMN1R7-30YL v.5	20110530	Product data sheet	-	PSMN1R7-30YL v.4
Modifications:	• Various changes to content.			
PSMN1R7-30YL v.4	20100420	Product data sheet	-	PSMN1R7-30YL v.3

9. Legal information

9.1 Data sheet status

Document status ^[1] ^[2]	Product status ^[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

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[2] The term 'short data sheet' is explained in section "Definitions".

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