ISL78322

Dual 2A/1.7A, 2.25MHz High-Efficiency, Synchronous Buck Regulator

FN7908
Rev 3.00
November 30, 2016

The ISL78322 is a high-efficiency, dual synchronous step-down DC/DC regulator that can deliver up to 2A/1.7A continuous output current per channel. The channels are 180° out-of-phase for input RMS current and EMI reduction. The supply voltage range of 2.8V to 5.5V allows for the use of a single Li+ cell, three NiMH cells or a regulated 5V input. The current mode control architecture enables very low duty cycle operation at high frequency with fast transient response and excellent loop stability. The ISL78322 operates at 2.25MHz switching frequency, which allows for the use of small, low cost inductors and capacitors. Each channel is optimized for generating an output voltage as low as 0.6V.

The ISL78322 has a forced PWM mode that reduces noise and RF interference.

The ISL78322 offers a 1ms Power-Good (PG) signal to monitor both outputs at power-up. When shut down, ISL78322 discharges the output capacitors. Other features include internal digital soft-start, enable for power sequence, overcurrent protection, and thermal shutdown. The ISL78322 is offered in a 4mmx3mm, 12 Lead DFN package with 1mm maximum height. The complete converter occupies less than 1.8cm^2 area.

The ISL78322 is qualified to AEC-Q100 and specified for operation across the -40°C to +105°C (grade 2) ambient temperature range.

Features

- Dual 2A/1.7A high-efficiency, synchronous buck regulator with up to 97% efficiency
- 2.8V to 5.5V input supply range
- 180° out-of-phase outputs reduce ripple current and EMI
- Start-up with prebiased output prevents negative current flow in output stage
- External synchronization up to 8MHz
- Negative current detection and protection
- 100% maximum duty cycle for lowest dropout
- Internal current mode compensation
- Peak current limiting, hiccup mode short-circuit protection, and over-temperature protection
- Pb-free (RoHs compliant)
- AEC-Q100 qualified component

Applications

- DC/DC POL modules
- µC/µP, FPGA, and DSP power
- Automotive embedded processor power supply systems

Related Literature

- For a full list of related documents, visit our website
  - ISL78322 product page

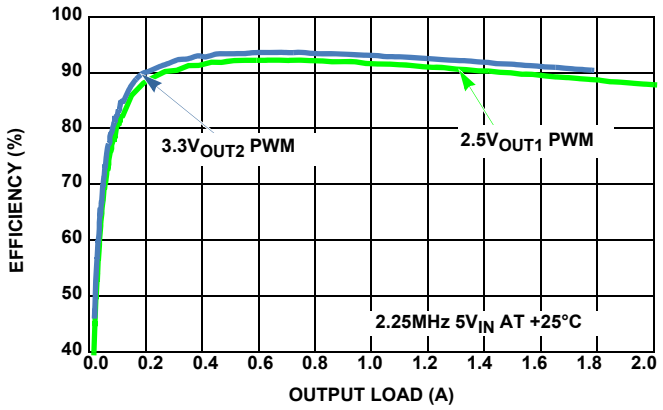


FIGURE 1. CHARACTERISTIC CURVE

Typical Applications

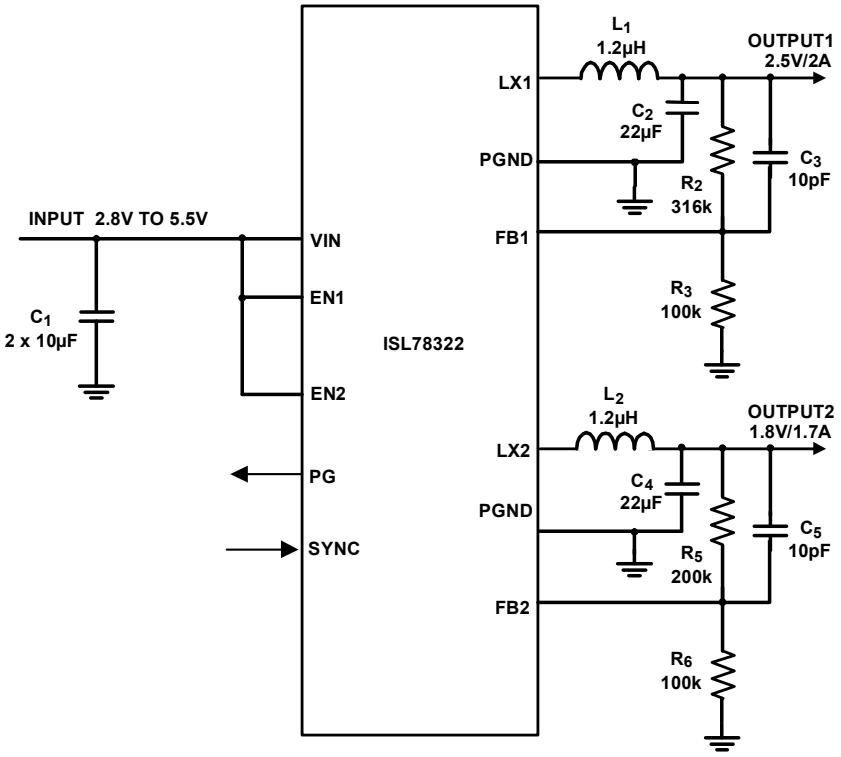


FIGURE 2. TYPICAL APPLICATION DIAGRAM - DUAL INDEPENDENT OUTPUTS

Ordering Information

PART NUMBER (Notes 1, 2, 3)	PART MARKING	TEMP. RANGE (°C)	PACKAGE (RoHS COMPLIANT)	PKG. DWG. #
ISL78322ARZ	BEKA	-40 to +105	12 Ld 4x3 DFN	L12.4x3

NOTES:

1. Add "-T" suffix for 6k unit or "-T7A" suffix for 250 unit tape and reel options. Refer to TB347 for details on reel specifications.
2. These Intersil Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.
3. For Moisture Sensitivity Level (MSL), see device information page for ISL78322. For more information on MSL, see techbrief TB363.

TABLE 1. COMPONENT VALUE SELECTION

V_{OUT}	0.8V	1.2V	1.5V	1.8V	2.5V	3.3V
C_1	2x10µF	2x10µF	2x10µF	2x10µF	2x10µF	2x10µF
C_2 (or C_4)	22µF	22µF	22µF	22µF	22µF	22µF
C_3 (or C_5)	10pF	10pF	10pF	10pF	10pF	10pF
L_1 (or L_2)	1.0~2.2µH	1.0~2.2µH	1.0~2.2µH	1.5~3.3µH	1.5~3.3µH	1.5~4.7µH
R_2 (or R_5)	33k	100k	150k	200k	316k	450k
R_3 (or R_6)	100k	100k	100k	100k	100k	100k

In Table 1, the minimum output capacitor value is given for different output voltages to make sure the whole converter system is stable. Output capacitance should increase to support faster load transient requirement.

Block Diagram

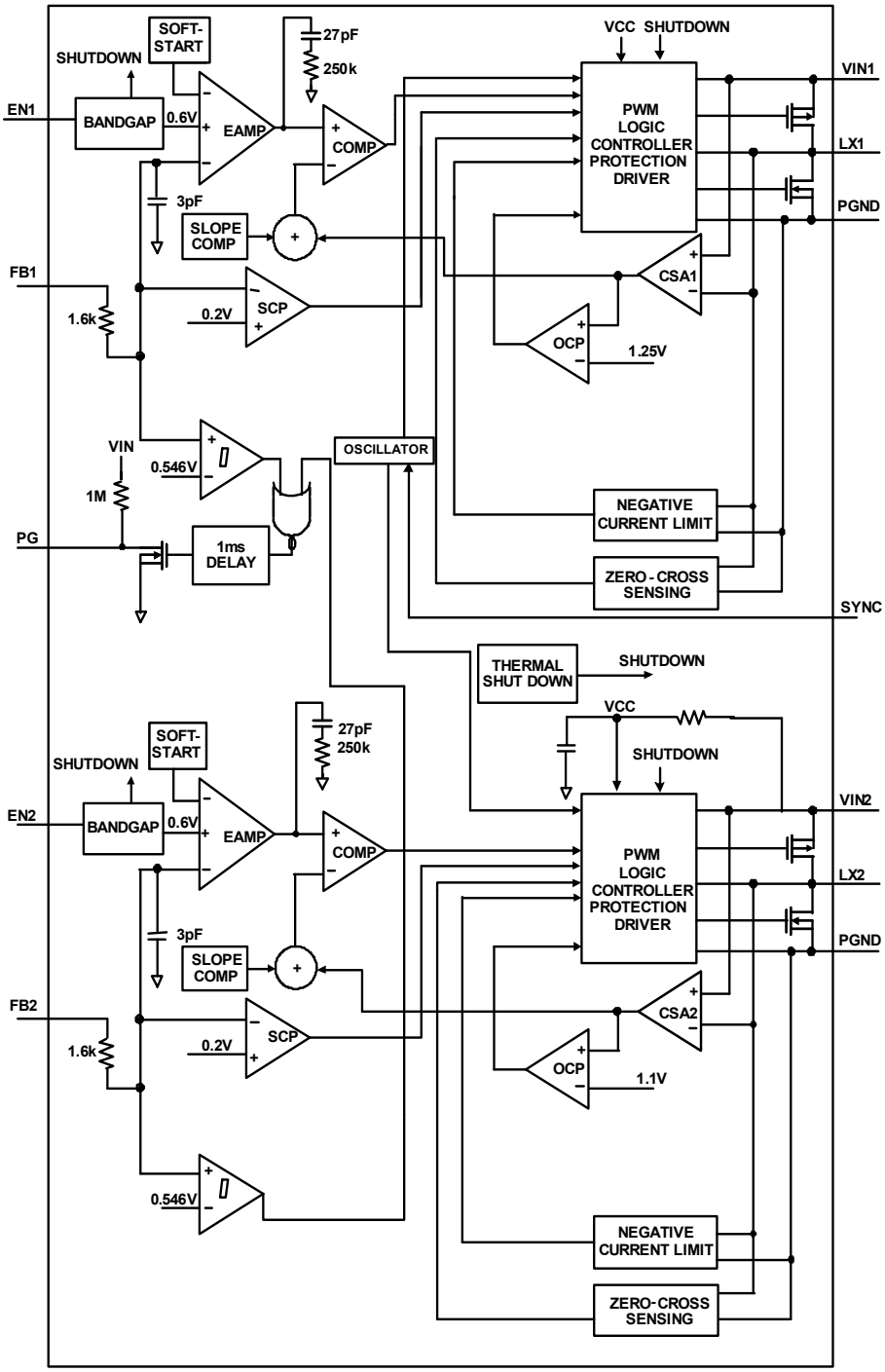
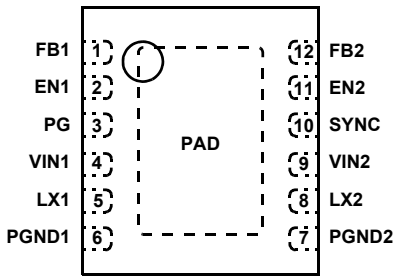


FIGURE 3. BLOCK DIAGRAM

Pin Configuration

ISL78322
(12 LD DFN)
TOP VIEW



Pin Description

PIN NUMBER	SYMBOL	DESCRIPTION
1	FB1	The feedback network of the Channel 1 regulator. FB1 is the negative input to the transconductance error amplifier. The output voltage is set by an external resistor divider connected to FB1. With a properly selected divider, the output voltage can be set to any voltage between the power rail (reduced by converter losses) and the 0.6V reference. There is an internal compensation to meet a typical application. In addition, the regulator power-good and undervoltage protection circuitry use FB1 to monitor the Channel 1 regulator output voltage.
2	EN1	Regulator Channel 1 enable pin. Enable the output, V_{OUT1}, when driven to high. Shutdown the V_{OUT1} and discharge output capacitor when driven to low. Do not leave this pin floating.
3	PG	1ms timer output. At power-up or EN_ HI, this output is a 1ms delayed power-good signal for both the V_{OUT1} and V_{OUT2} voltages. There is an internal 1MΩ pull-up resistor.
4	VIN1	Input supply voltage for Channel 1. Connect 10µF ceramic capacitor to PGND1.
5	LX1	Switching node connection for Channel 1. Connect to one terminal of inductor for V_{OUT1}.
6	PGND1	Negative supply for Power Stage 1.
7	PGND2	Negative supply for Power Stage 2 and system ground.
8	LX2	Switching node connection for Channel 2. Connect to one terminal of inductor for V_{OUT2}.
9	VIN2	Input supply voltage for Channel 2 and to provide logic bias. Make sure that VIN2 is ≥ VIN1. Connect 10µF ceramic capacitor to PGND2.
10	SYNC	Connect to logic low or ground for forced PWM mode. Connect to an external function generator for synchronization. Negative edge trigger. Do not leave this pin floating.
11	EN2	Regulator Channel 2 enable pin. Enable the output, V_{OUT2}, when driven to high. Shutdown the V_{OUT2} and discharge output capacitor when driven to low. Do not leave this pin floating.
12	FB2	The feedback network of the Channel 2 regulator. FB2 is the negative input to the transconductance error amplifier. The output voltage is set by an external resistor divider connected to FB2. With a properly selected divider, the output voltage can be set to any voltage between the power rail (reduced by converter losses) and the 0.6V reference. There is an internal compensation to meet a typical application. In addition, the regulator power-good and undervoltage protection circuitry use FB2 to monitor the Channel 2 regulator output voltage.
-	EXPOSED PAD	The exposed pad must be connected to the PGND1 and PGND2 pins for proper electrical performance. Add as many vias as possible for optimal thermal performance.

Absolute Maximum Ratings (Reference to GND)

Supply Voltage (VIN) . . . . . -0.3V to 6V (DC) or 7V (20ms)
EN1, EN2, PG, SYNC . . . . . -0.3V to V_{IN} + 0.3V
LX1, LX2. . . . . -1.5V (100ns)/-0.3V (DC) to 6.5V (DC)
. . . . . or 7V (20ms)
FB1, FB2 . . . . . -0.3V to 2.7V
ESD Rating
Human Body Model (Tested per JESD22-A114F) 3kV
Machine Model(Tested per JESD22-C101E) 250V
Charged Device Model (Tested per AEC-Q100-11) 2kV
Latch-Up (Tested per JESD-78B; Class 2, Level A) 100mA

Thermal Information

Thermal Resistance (Typical)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
4x3 DFN Package (Notes 4, 5)	41	3

Junction Temperature Range . . . . . -55°C to +150°C
Storage Temperature Range . . . . . -65°C to +150°C
Pb-Free Reflow Profile . . . . . see TB493

Recommended Operating Conditions

V_{IN} Supply Voltage Range . . . . . 2.8V to 5.5V
Load Current Range Channel 1 . . . . . 0A to 2A
Load Current Range Channel 2 . . . . . 0A to 1.7A
Ambient Temperature Range . . . . . -40°C to +105°C

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

NOTES:

4. θ_{JA} is measured in free air with the component mounted on a high-effective thermal conductivity test board with "direct attach" features. See Tech Brief TB379.
5. θ_{JC}, "case temperature" location is at the center of the exposed metal pad on the package underside.

Electrical Specifications

Unless otherwise noted, all parameter limits are established over the recommended operating conditions: T_A = -40°C to +105°C, V_{IN} = 2.8V to 5.5V, EN1 = EN2 = V_{IN}, SYNC = 0V, L = 1.2µH, C_1 = 2 x 10µF, C_2 = C_4 = 22µF, I_{OUT1} = 0A to 2A, I_{OUT2} = 0A to 1.7A. (Typical values are at T_A = +25°C, V_{IN} = 3.6V). **Boldface limits apply across the operating temperature range, -40°C to +105°C.**

PARAMETER	SYMBOL	TEST CONDITIONS	MIN (Note 6)	TYP	MAX (Note 6)	UNIT
INPUT SUPPLY						
V_{IN} Undervoltage Lock-out Threshold	V_{UVLO}	Rising		2.5	**2.8**	V
		Falling	**2.0**	2.4		V
Quiescent Supply Current	I_{VIN}	SYNC = GND, EN1 = EN2 = V_{IN}, f_{SW} = 2.25MHz, no load at the output		0.86	**1.00**	mA
Shutdown Supply Current	I_{SD}	V_{IN} = 5.5V, EN1 = EN2 = GND		6.5	**12.0**	µA
OUTPUT REGULATION						
FB1, FB2 Regulation Voltage	$V_{FB\_}$		**0.590**	0.600	**0.610**	V
FB1, FB2 Bias Current	$I_{FB\_}$	V_{FB} = 0.55V		0.1		µA
Output Voltage Accuracy		SYNC = V_{IN}, Io = 0A to 2A		±1.5		%
		SYNC = GND, Io = 0A to 2A		±1		%
Line Regulation		V_{IN} = V_O + 0.5V to 5.5V (minimal 2.8V)		0.2		%/V
Soft-Start Ramp Time Cycle				1.3		ms
OVERCURRENT PROTECTION						
Dynamic Current Limit ON-time	t_{OCON}			17		Clock pulses
Dynamic Current Limit OFF-time	t_{OCOFF}			4		SS cycle
Peak Overcurrent Limit	I_{pk1}		**2.7**	3.2	**3.6**	A
	I_{pk2}		**2.3**	2.8	**3.2**	A
Negative Current Limit	$I_{valley1}$		**-2.2**	-1.6	**-1.0**	A
	$I_{valley2}$		**-2.2**	-1.6	**-1.0**	A

Electrical Specifications Unless otherwise noted, all parameter limits are established over the recommended operating conditions: T_A = -40°C to +105°C, V_{IN} = 2.8V to 5.5V, EN1 = EN2 = V_{IN}, SYNC = 0V, L = 1.2µH, C_1 = 2 x 10µF, C_2 = C_4 = 22µF, I_{OUT1} = 0A to 2A, I_{OUT2} = 0A to 1.7A. (Typical values are at T_A = +25°C, V_{IN} = 3.6V). **Boldface limits apply across the operating temperature range, -40°C to +105°C. (Continued)**

PARAMETER	SYMBOL	TEST CONDITIONS	MIN (Note 6)	TYP	MAX (Note 6)	UNIT
LX1, LX2						
P-Channel MOSFET ON-Resistance		V_{IN} = 5.5V, I_O = 200mA Channel 1		90	**115**	mΩ
		V_{IN} = 5.5V, I_O = 200mA Channel 2		100	**125**	mΩ
N-Channel MOSFET ON-Resistance		V_{IN} = 5.5V, I_O = 200mA Channel 1		80	**103**	mΩ
		V_{IN} = 5.5V, I_O = 200mA Channel 2		90	**112**	mΩ
LX_ Maximum Duty Cycle				100		%
PWM Switching Frequency	f_{SW}		**1.80**	2.25	**2.70**	MHz
Synchronization Range		(Note 7)	**5.4**		**8.0**	MHz
Channel 1 to Channel 2 Phase Shift		Rising edge to rising edge timing		180		°
LX Minimum On Time		SYNC = High (forced PWM mode)		65		ns
Soft Discharge Resistance	$R_{DIS\_}$	EN = LOW	**80**	100	**130**	Ω
PG						
Output Low Voltage		Sinking 1mA, VFB = 0.5V			**0.4**	V
PG Pin Leakage Current		PG = V_{IN} = 3.6V		0.01	**0.10**	µA
PG Pull-Up Resistor				1		MΩ
Internal PGOOD Low Rising Threshold		Percentage of nominal regulation voltage	**85**	91	**97**	%
Internal PGOOD Low Falling Threshold		Percentage of nominal regulation voltage	**78**	85	**92**	%
Delay Time (Rising Edge)				0.76		ms
Internal PGOOD Delay Time (Falling Edge)				2	**4**	µs
EN1, EN2, SYNC						
Logic Input Low					**0.4**	V
Logic Input High			**1.4**			V
Enable Logic Input Leakage Current	$I_{EN\_}$			0.1	**1**	µA
Thermal Shutdown				150		°C
Thermal Shutdown Hysteresis				25		°C

NOTES:

6. Parameters with MIN and/or MAX limits are 100% tested at +25°C, unless otherwise specified. Temperature limits established by characterization and are not production tested.
7. The operational frequency per switching channel will be half of the SYNC frequency.

Typical Operating Performance

Unless otherwise noted, operating conditions are: T_A = +25°C, V_{VIN} = 2.8V to 5.5V, EN = V_{IN}, L_1 = L_2 = 1.2µH, C_1 = 10µF, C_2 = C_4 = 22µF, I_{OUT1} = 0A to 2A, I_{OUT2} = 0A to 1.7A.

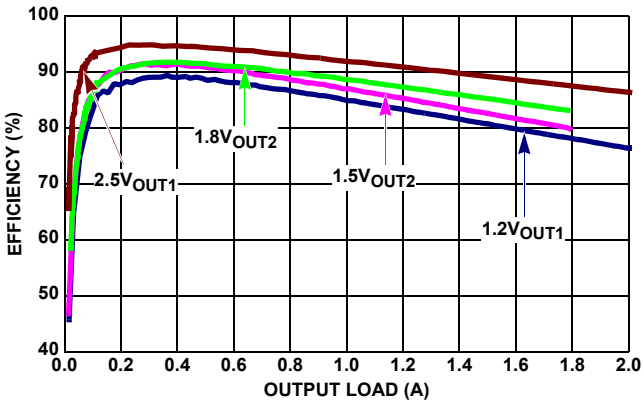


FIGURE 4. EFFICIENCY vs LOAD, 2.25MHz, 3.3V_{IN} PWM

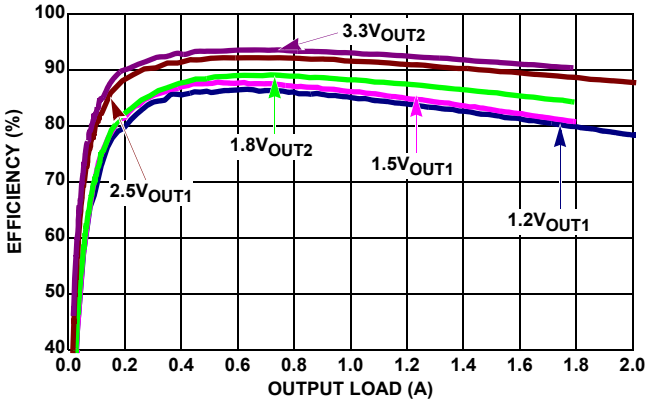


FIGURE 5. EFFICIENCY vs LOAD, 2.25MHz, 5V_{IN} PWM

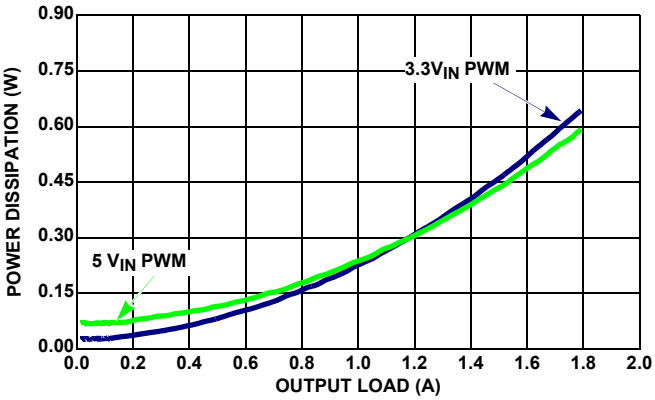


FIGURE 6. POWER DISSIPATION vs LOAD, 2.25MHz, 1.8V, CHANNEL 2

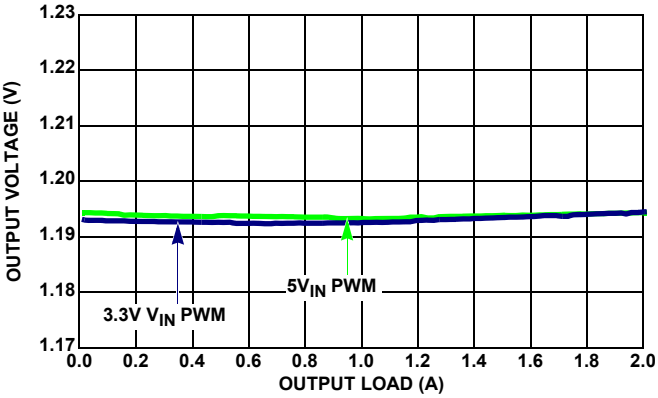


FIGURE 7. V_{OUT} REGULATION vs LOAD, 2.25MHz, 1.2V, CHANNEL 1

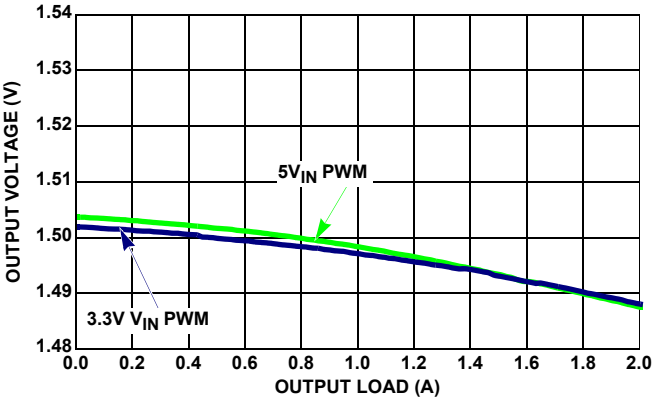


FIGURE 8. V_{OUT} REGULATION vs LOAD, 2.25MHz, 1.5V CHANNEL 2

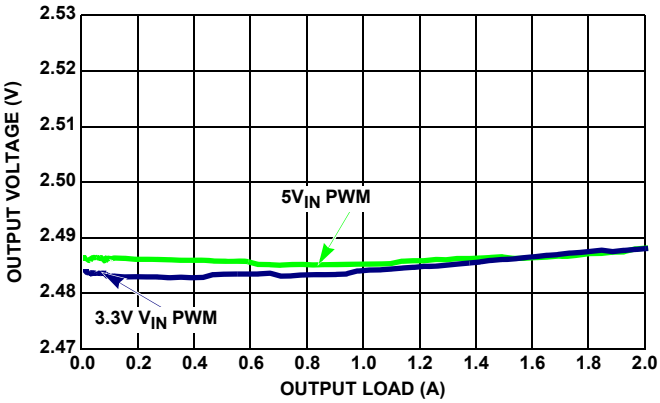


FIGURE 9. V_{OUT} REGULATION vs LOAD, 2.25MHz, 2.5V CHANNEL 1

Typical Operating Performance

Unless otherwise noted, operating conditions are: T_A = +25°C, V_{VIN} = 2.8V to 5.5V, EN = V_{IN}, L_1 = L_2 = 1.2µH, C_1 = 10µF, C_2 = C_4 = 22µF, I_{OUT1} = 0A to 2A, I_{OUT2} = 0A to 1.7A. **(Continued)**

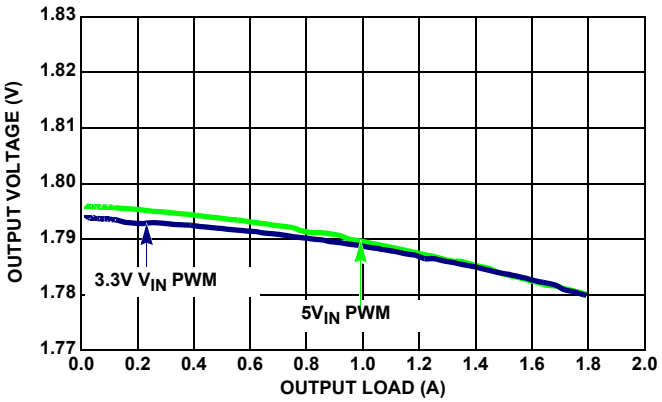


FIGURE 10. V_{OUT} REGULATION vs LOAD, 2.25MHz, 1.8V, CHANNEL 2

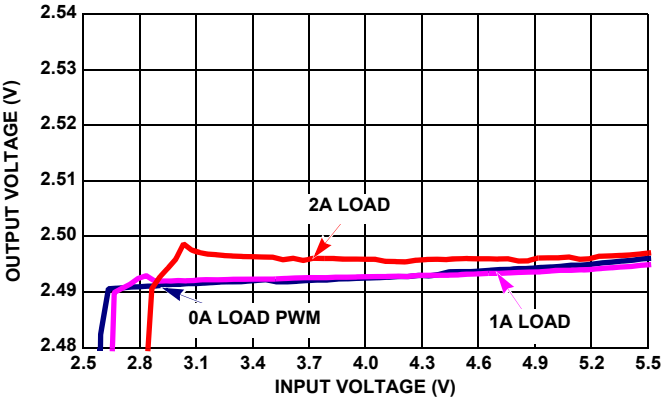


FIGURE 11. OUTPUT VOLTAGE REGULATION vs V_{IN} 2.5V CHANNEL 1

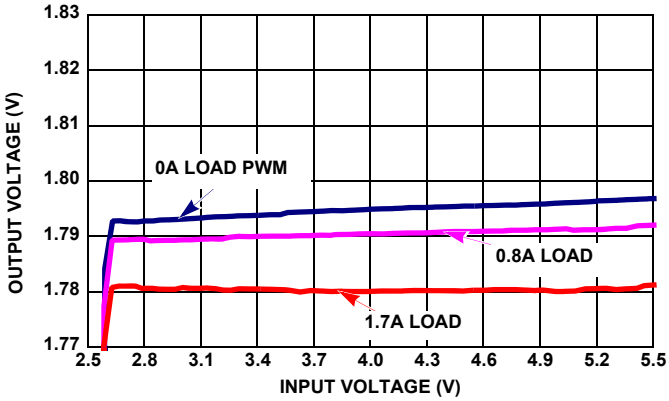


FIGURE 12. OUTPUT VOLTAGE REGULATION vs V_{IN} 1.8V CHANNEL 2

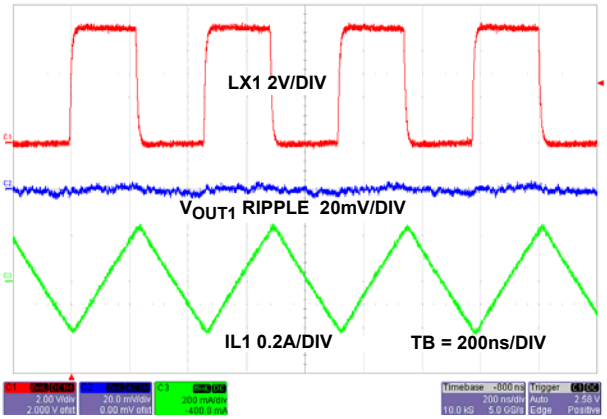


FIGURE 13. STEADY STATE OPERATION AT NO LOAD CHANNEL 1 (PWM)

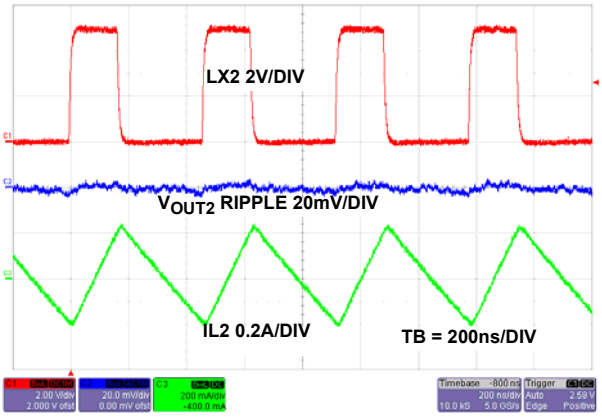


FIGURE 14. STEADY STATE OPERATION AT NO LOAD CHANNEL 2 (PWM)

Typical Operating Performance

Unless otherwise noted, operating conditions are: T_A = +25°C, V_{VIN} = 2.8V to 5.5V, EN = V_{IN}, L_1 = L_2 = 1.2µH, C_1 = 10µF, C_2 = C_4 = 22µF, I_{OUT1} = 0A to 2A, I_{OUT2} = 0A to 1.7A. **(Continued)**

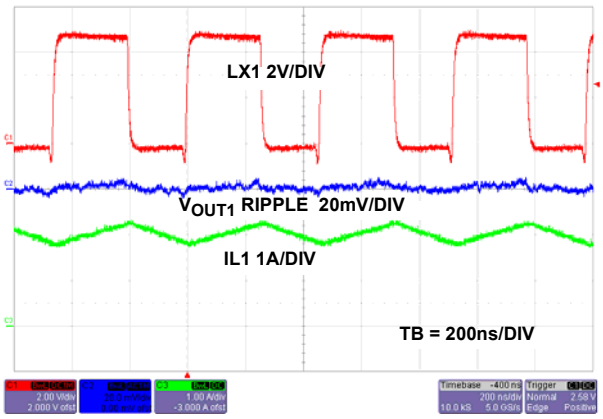


FIGURE 15. STEADY STATE OPERATION AT FULL LOAD CHANNEL 1

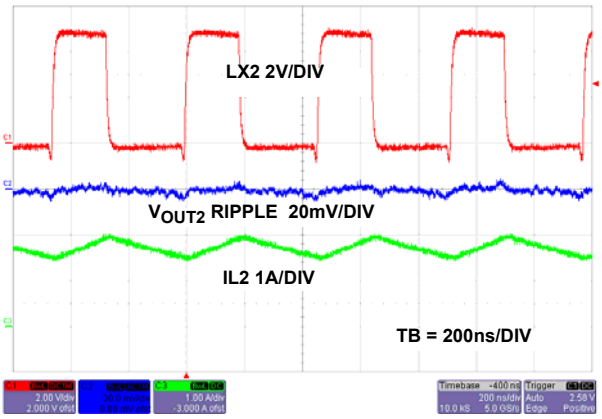


FIGURE 16. STEADY STATE OPERATION WITH FULL LOAD CHANNEL 2

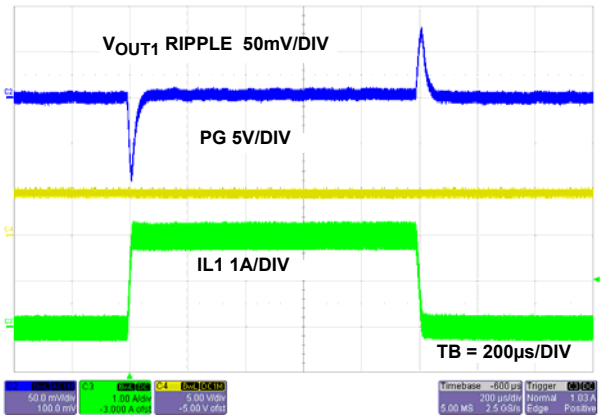


FIGURE 17. LOAD TRANSIENT CHANNEL 1 (PWM)

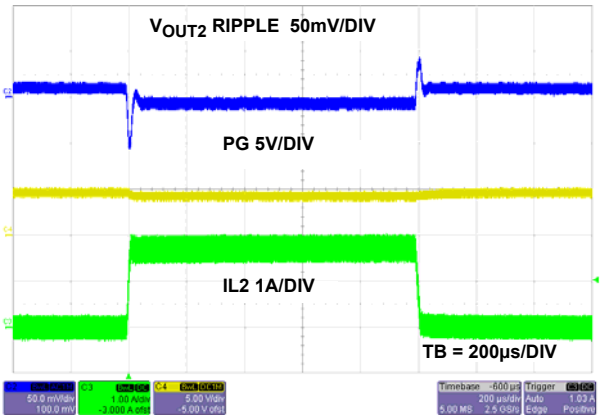


FIGURE 18. LOAD TRANSIENT CHANNEL 2 (PWM)

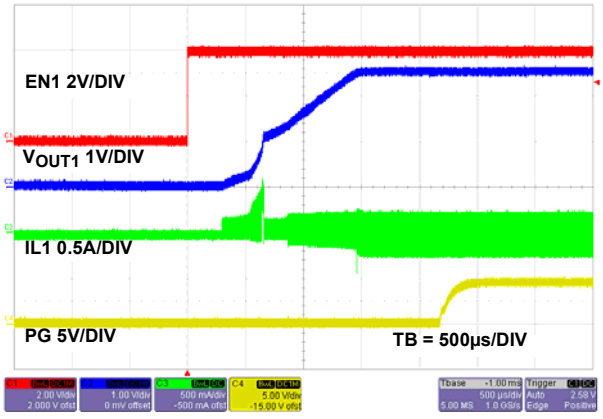


FIGURE 19. SOFT-START WITH NO LOAD CHANNEL 1 (PWM)

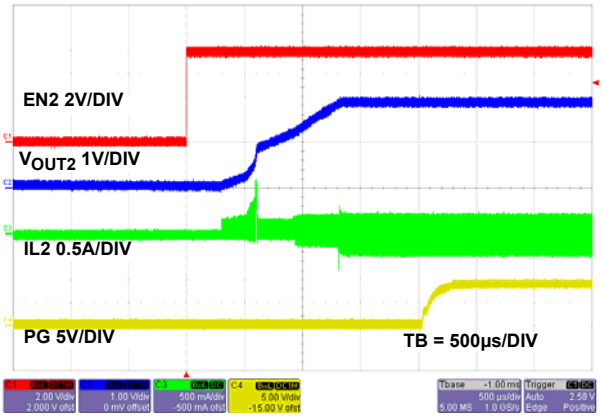


FIGURE 20. SOFT-START WITH NO LOAD CHANNEL 2 (PWM)

Typical Operating Performance

Unless otherwise noted, operating conditions are: T_A = +25°C, V_{VIN} = 2.8V to 5.5V, EN = V_{IN}, L_1 = L_2 = 1.2µH, C_1 = 10µF, C_2 = C_4 = 22µF, I_{OUT1} = 0A to 2A, I_{OUT2} = 0A to 1.7A. **(Continued)**

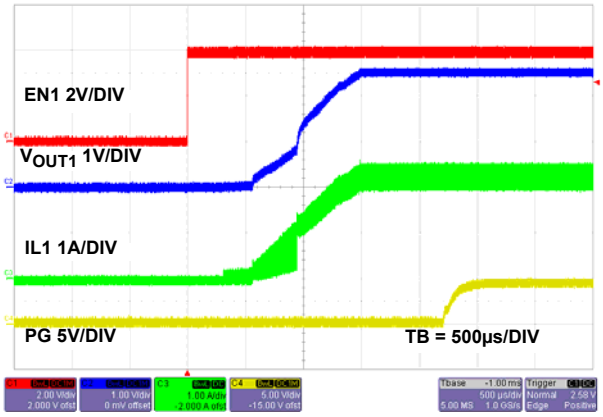


FIGURE 21. SOFT-START AT FULL LOAD CHANNEL 1

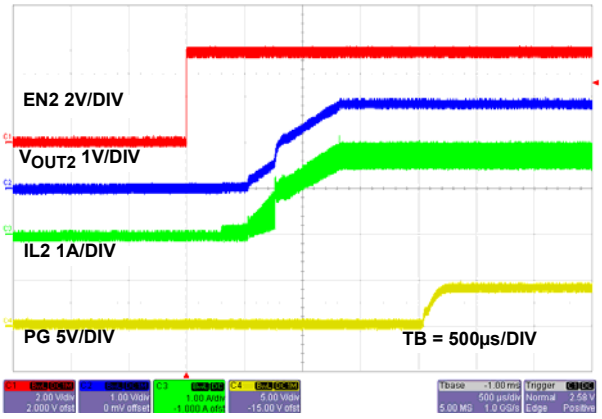


FIGURE 22. SOFT-START AT FULL LOAD CHANNEL 2

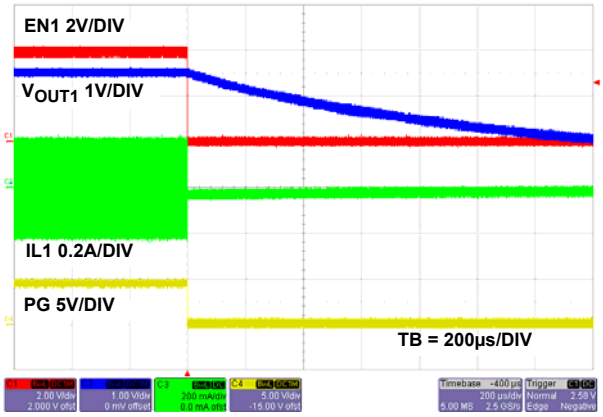


FIGURE 23. SOFT-DISCHARGE SHUTDOWN CHANNEL 1

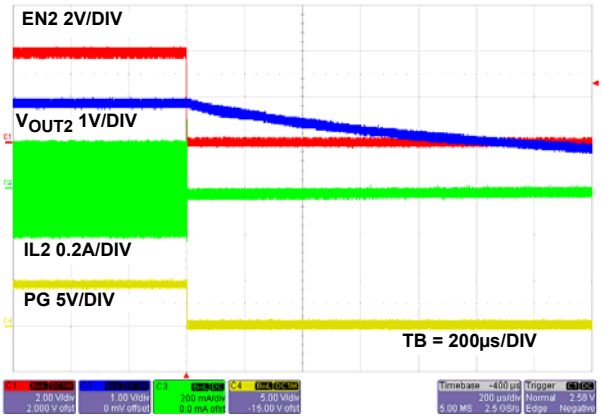


FIGURE 24. SOFT-DISCHARGE SHUTDOWN CHANNEL 2

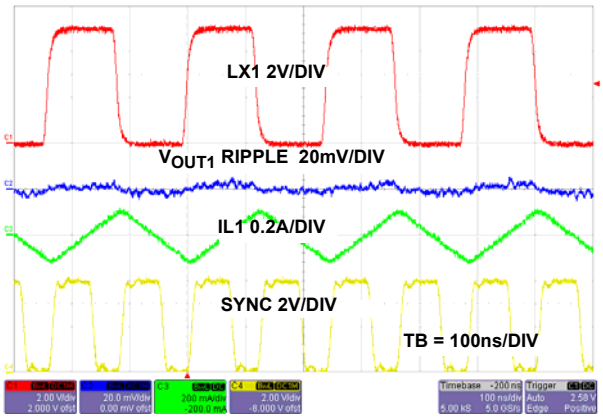


FIGURE 25. STEADY STATE OPERATION AT NO LOAD WITH FREQUENCY = 8MHz CHANNEL 1

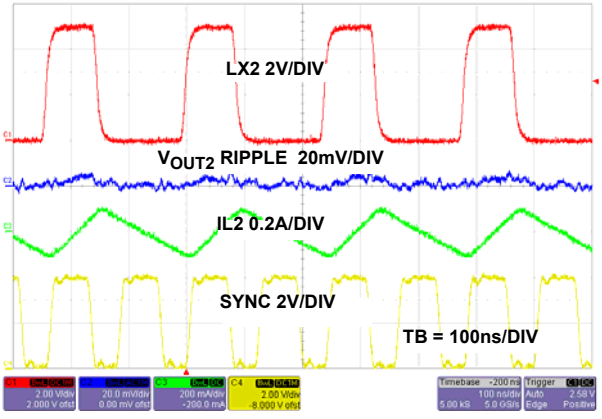


FIGURE 26. STEADY STATE OPERATION AT NO LOAD WITH FREQUENCY = 8MHz CHANNEL 2

Typical Operating Performance

Unless otherwise noted, operating conditions are: T_A = +25°C, V_{VIN} = 2.8V to 5.5V, EN = V_{IN}, L_1 = L_2 = 1.2µH, C_1 = 10µF, C_2 = C_4 = 22µF, I_{OUT1} = 0A to 2A, I_{OUT2} = 0A to 1.7A. **(Continued)**

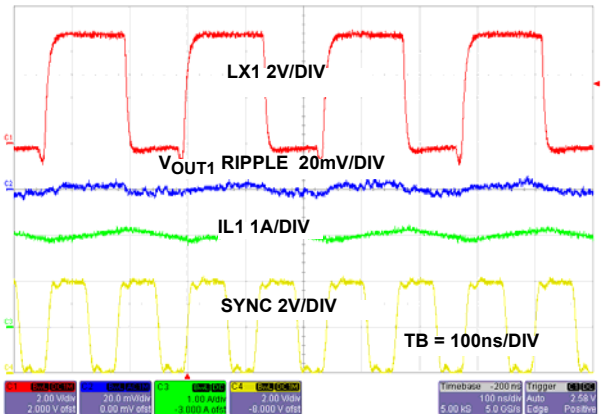


FIGURE 27. STEADY STATE OPERATION AT FULL LOAD WITH FREQUENCY = 8MHz CHANNEL 1

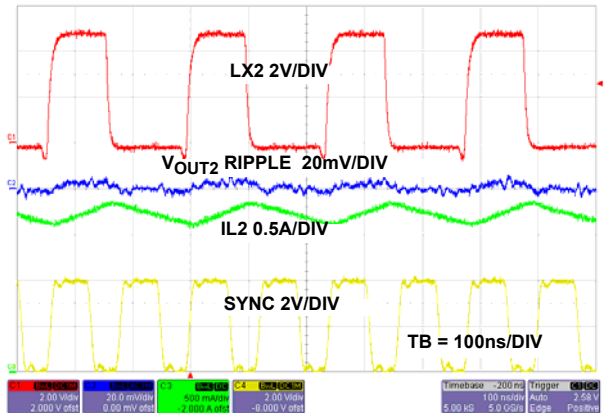


FIGURE 28. STEADY STATE OPERATION AT FULL LOAD WITH FREQUENCY = 8MHz CHANNEL 2

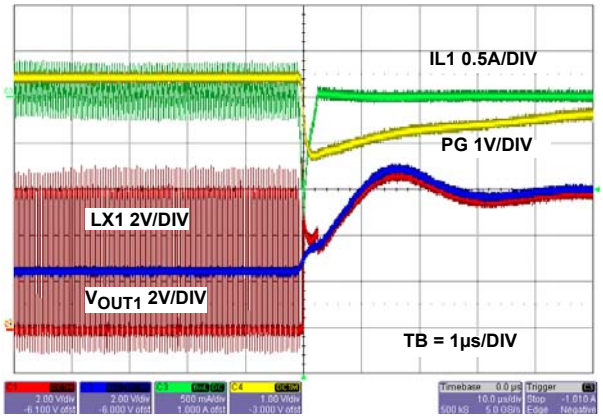


FIGURE 29. V_{OUT1} HARD SHORT TO V_{IN} NEGATIVE CURRENT WAVEFORMS AT HIGH LINE CHANNEL 1

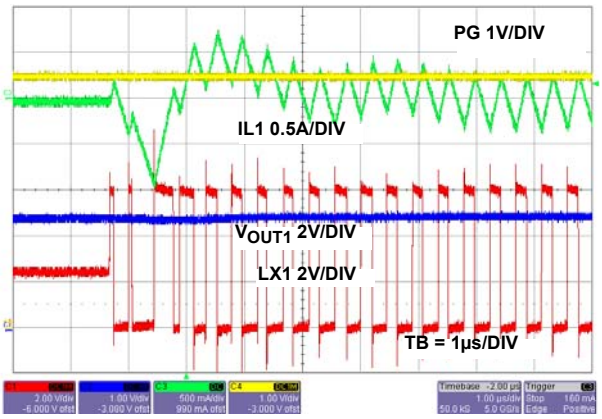


FIGURE 30. RECOVERY FROM HARD SHORT NEGATIVE CURRENT WAVEFORMS V_{OUT1} CHANNEL 1

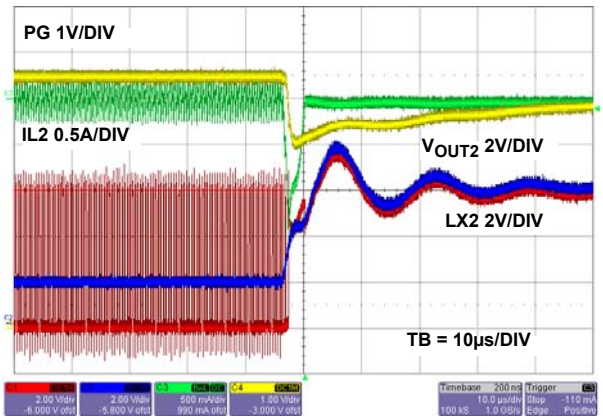


FIGURE 31. V_{OUT2} HARD SHORT TO V_{IN} NEGATIVE CURRENT WAVEFORMS AT HIGH LINE CHANNEL 2

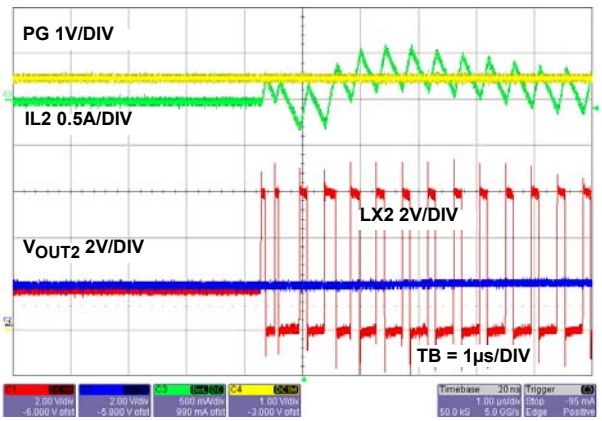


FIGURE 32. RECOVERY FROM HARD SHORT NEGATIVE CURRENT WAVEFORMS V_{OUT2} CHANNEL 2

Typical Operating Performance

Unless otherwise noted, operating conditions are: T_A = +25°C, V_{VIN} = 2.8V to 5.5V, EN = V_{IN}, L_1 = L_2 = 1.2µH, C_1 = 10µF, C_2 = C_4 = 22µF, I_{OUT1} = 0A to 2A, I_{OUT2} = 0A to 1.7A. **(Continued)**

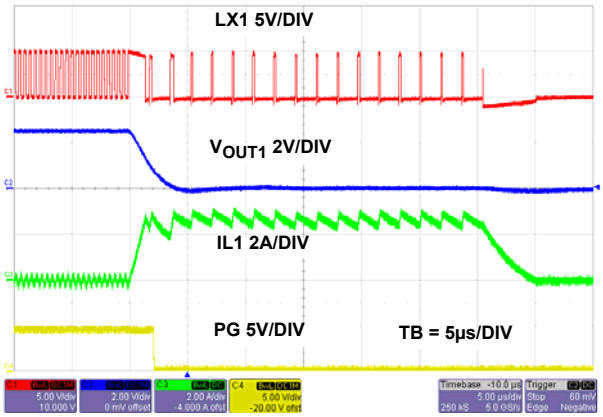


FIGURE 33. OUTPUT SHORT-CIRCUIT CHANNEL 1

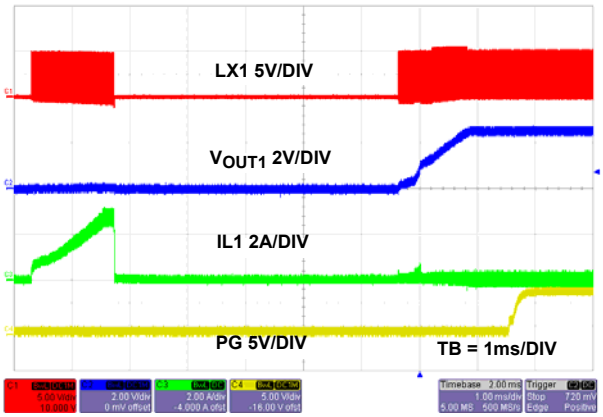


FIGURE 34. OUTPUT SHORT-CIRCUIT RECOVERY CHANNEL 1

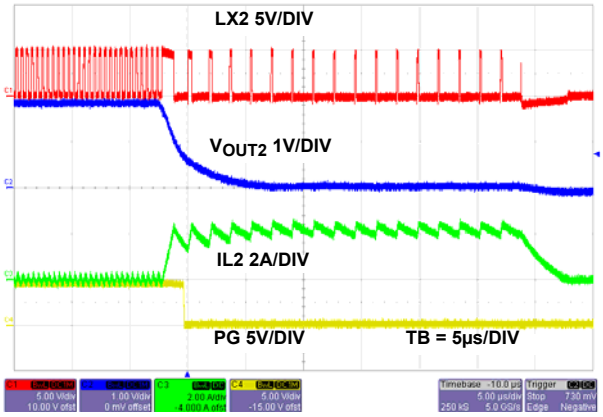


FIGURE 35. OUTPUT SHORT-CIRCUIT CHANNEL 2

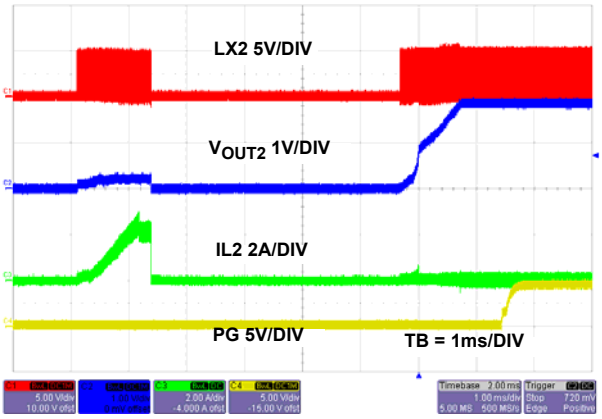


FIGURE 36. OUTPUT SHORT-CIRCUIT RECOVERY CHANNEL 2

Theory of Operation

The ISL78322 is a dual 2A/1.7A step-down switching regulator optimized for battery-powered or mobile applications. The regulator operates at 2.25MHz fixed switching frequency under heavy load condition to allow small external inductor and capacitors to be used for minimal Printed Circuit Board (PCB) area. At light load, the regulator reduces the switching frequency, unless forced to the fixed frequency, to minimize the switching loss and to maximize the battery life. The two channels are 180° out-of-phase operation. The supply current is typically only 6.5µA when the regulator is shut down.

PWM Control Scheme

Pulling the SYNC pin LOW (<0.4V) forces the converter into PWM mode in the next switching cycle regardless of output current. Each of the channels of the ISL78322 employ the current-mode Pulse-Width Modulation (PWM) control scheme for fast transient response and pulse-by-pulse current limiting shown in the "Block Diagram" on page 3. The current loop consists of the oscillator, the PWM comparator COMP, current sensing circuit, and the slope compensation for the current loop stability. The current sensing circuit consists of the resistance of the P-channel MOSFET when it is turned on and the current sense amplifier CSA1 (or CSA2 on Channel 2). The gain for the current sensing circuit is typically 0.32V/A. The control reference for the current loops comes from the error amplifier EAMP of the voltage loop.

The PWM operation is initialized by the clock from the oscillator. The P-channel MOSFET is turned on at the beginning of a PWM cycle and the current in the MOSFET starts to ramp up. When the sum of the current amplifier CSA1 (or CSA2) and the compensation slope (0.9V/µs) reaches the control reference of the current loop, the PWM comparator COMP sends a signal to the PWM logic to turn off the P-MOSFET and to turn on the N-channel MOSFET. The N-MOSFET stays on until the end of the PWM cycle. Figure 37 shows the typical operating waveforms during the PWM operation. The dotted lines illustrate the sum of the compensation ramp and the current-sense amplifier CSA_ output.

The output voltage is regulated by controlling the reference voltage to the current loop. The bandgap circuit outputs a 0.6V reference voltage to the voltage control loop. The feedback signal comes from the V_{FB} pin. The soft-start block only affects the operation during the start-up and will be discussed separately shortly. The error amplifier is a transconductance amplifier that converts the voltage error signal to a current output. The voltage loop is internally compensated with the 27pF and 250kΩ RC network. The maximum EAMP voltage output is precisely clamped to 1.8V.

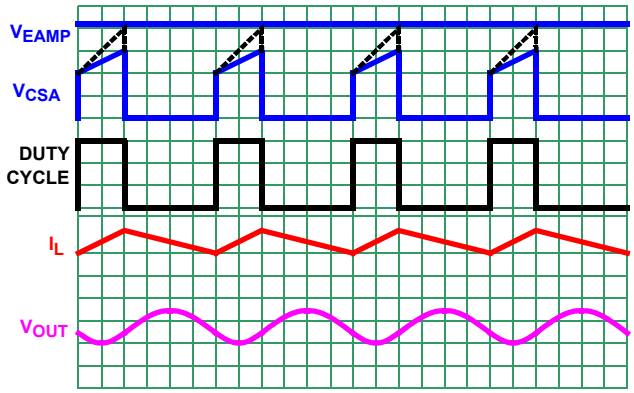


FIGURE 37. PWM OPERATION WAVEFORMS

Synchronization Control

The frequency of operation can be synchronized up to 8MHz by an external signal applied to the SYNC pin. The 1st falling edge on the SYNC triggered the rising edge of the PWM ON pulse of Channel 1. The 2nd falling edge of the SYNC triggers the rising edge of the PWM ON pulse of the Channel 2. This process alternates indefinitely allowing 180° output phase operation between the two channels. The internal frequency will take control when the divided external sync is lower than 2.25MHz. The falling edge on the SYNC triggers the rising edge of the PWM ON pulse.

Positive and Negative Overcurrent Protection

CSA1 and CSA2 are used to monitor Output 1 and Output 2 channels respectively. The overcurrent protection is realized by monitoring the CSA_ output with the OCP threshold logic, as shown in the "Block Diagram" on page 3. The current sensing circuit has a gain of 0.32V/A, from the P-MOSFET current to the CSA_ output. When the CSA_ output reaches the threshold of 1.25V for Channel 1 and 1.1V for Channel 2, the OCP comparator is tripped to turn off the P-MOSFET immediately. The overcurrent function protects the switching converter from a shorted output by monitoring the current flowing through the upper MOSFETs.

Upon detection of an overcurrent condition, the upper MOSFET will be immediately turned off and will not be turned on again until the next switching cycle. Upon detection of the initial overcurrent condition, the Overcurrent Fault Counter is set to 1 and the Overcurrent Condition Flag is set from LOW to HIGH. If, on the subsequent cycle, another overcurrent condition is detected, the OC Fault Counter will be incremented. If there are 17 sequential OC fault detections, the regulator will be shut down under an Overcurrent Fault Condition. An Overcurrent Fault Condition will result with the regulator attempting to restart in a hiccup mode with the delay between restarts being four soft-start periods. At the end of the fourth soft-start wait period, the fault counters are reset and soft-start is attempted again. If the overcurrent condition goes away prior to the OC Fault Counter reaching a count of four, the Overcurrent Condition Flag will set back to LOW.

In the event that the inductor current reaches -1.6A, the part enters Negative Overcurrent Protection. At this point, all switching stops and the part enters tri-state mode while the

pull-down FET is discharging the output until it reaches normal regulation voltage, then the IC restarts switching.

PG

The power-good signal (PG), monitors both of the output channels. When powering up, the open-collector power-on reset output holds low for about 1ms after V_{O1} and V_{O2} reaches the preset voltages. The PG output also serves as a 1ms delayed power-good signal. If one of the outputs is disabled, then PG only monitors the active channels. There is an internal 1MΩ pull-up resistor.

UVLO

When the input voltage is below the Undervoltage Lockout (UVLO) threshold, the regulator is disabled.

Enable

The enable (EN1, EN2) input allows the user to control the turning on or off of the regulator for purposes such as power-up sequencing. The regulator is enabled, there is typically a 600µs delay for waking up the bandgap reference and the soft start-up begins.

Soft Start-Up

The soft start-up eliminates the inrush current during start-up. The soft-start block outputs a ramp reference to both the voltage loop and the current loop. The two ramps limit the inductor current rising speed as well as the output voltage speed so that the output voltage rises in a controlled fashion.

At the very beginning of the start-up, the feedback voltage is less than 0.2V; hence the PWM operating frequency is 1/3 of the normal frequency. In forced PWM mode, the IC will start-up in pulse frequency mode to support prebiased load applications. During soft-start period, the device will operate in tri-state mode, with both high-side and low-side drivers off to prevent negative inductor current flow in output stage. Once soft-start is completed, the drivers will allow negative inductor current. By this time, the output should reach regulation.

Discharge Mode (Soft-Stop)

When a transition to shutdown mode occurs, or the output undervoltage fault latch is set, the outputs discharge to GND through an internal 100Ω switch.

Power MOSFETs

The power MOSFETs are optimized for best efficiency. The ON-resistance for the P-MOSFET is typically 100mΩ and the ON-resistance for the N-MOSFET is typical 90mΩ.

100% Duty Cycle

The ISL78322 features 100% duty cycle operation to maximize the battery life. When the battery voltage drops to a level that the ISL78322 can no longer maintain the regulation at the output, the regulator completely turns on the P-MOSFET. The maximum dropout voltage under the 100% duty-cycle operation is the product of the load current and the ON-resistance of the P-MOSFET.

Thermal Shutdown

The ISL78322 has built-in thermal protection. When the internal temperature reaches +150°C, the regulator is completely shut down. As the temperature drops to +130°C, the ISL78322 resumes operation by stepping through a soft start-up.

Applications Information

Output Inductor and Capacitor Selection

To consider steady state and transient operation, ISL78322 typically uses a 1.2µH output inductor. Higher or lower inductor values can be used to optimize the total converter system performance. For example, for higher output voltage 3.3V applications, in order to decrease the inductor current ripple and output voltage ripple, the output inductor value can be increased. The inductor ripple current can be expressed as in Equation 1:

$$\Delta I = \frac{V_O \bullet \left(1 - \frac{V_O}{V_{IN}}\right)}{L \bullet f_S} \quad \text{(EQ. 1)}$$

The inductor's saturation current rating needs to be at least larger than the peak current. The ISL78322 protects the typical peak current 3.2A/2.8A. The saturation current needs to be over 3.6A for maximum output current application.

ISL78322 uses internal compensation network and the output capacitor value is dependent on the output voltage. The ceramic capacitor is recommended to be X5R or X7R. The recommended minimum output capacitor values for the ISL78322 are shown in Table 1 on page 2.

Output Voltage Selection

The output voltage of the regulator can be programmed via an external resistor divider that is used to scale the output voltage relative to the internal reference voltage and feed it back to the inverting input of the error amplifier. Refer to "Typical Applications" on page 2.

The output voltage programming resistor, R_2 (or R_5 in Channel 2), will depend on the desired output voltage of the regulator. The value for the feedback resistor is typically between 0Ω and 750kΩ.

Let R_3 = 100kΩ, then R_2 will be as shown in Equation 2:

$$R_2 = R_3\left(\frac{V_{OUT}}{V_{FB}} - 1\right) \quad \text{(EQ. 2)}$$

If the output voltage desired is 0.6V, then R_3 is left unpopulated and short R_2. For better performance, add 10pF in parallel to R_2.

Input Capacitor Selection

The main functions for the input capacitor is to provide decoupling of the parasitic inductance and to provide a filtering function, which prevents the switching current from flowing back to the battery rail. One 10µF X5R or X7R ceramic capacitor is a good starting point for the input capacitor selection per channel. An optional input inductor can be used before the ceramic capacitor to limit switching noise. It is recommended to limit the inductance less than 0.15µH.

PCB Layout Recommendation

The PCB layout is a very important converter design step to make sure the designed converter works well. For ISL78322, the power loop is composed of the output inductor L's, the output capacitor C_{OUT1} and C_{OUT2}, the LX pins, and the GND pin. It is necessary to make the power loop as small as possible and the connecting traces among them should be direct, short and wide. The switching node of the converter, the LX_ pins, and the traces connected to the node are very noisy, so keep the voltage feedback trace away from these noisy traces. The input capacitor should be placed as close as possible to the VIN pin and the ground of input and output capacitors should be connected as close as possible. The heat of the IC is mainly dissipated through the thermal pad. Maximizing the copper area connected to the thermal pad is preferable. In addition, a solid ground plane is helpful for better EMI performance. It is recommended to add at least five vias ground connection within the pad for the best thermal relief.

Revision History

The revision history provided is for informational purposes only and is believed to be accurate, but not warranted. Please visit our website to make sure you have the latest Rev.

DATE	REVISION	CHANGE
November 30, 2016	FN7908.3	Updated title Updated Features bullet 1 and added bullet 2. Added Related Literature section. Removed PFM information from document including text and figures. Updated Note 1. Updated Exposed Pad pin description on page 4. Removed Quiescent Supply Current (top row only) from EC table Removed Peak Skip Limit from EC table Removed SYNC Logic Input Leakage Current from EC table Removed Skip Mode section. Updated Figures 1, 3, and 6 through 12. Updated POD L12.4x3 to the latest revision. Changes are as follows: -Tiebar Note 5 updated From: Tiebar shown (if present) is a non-functional feature. To: Tiebar shown (if present) is a non-functional feature and may be located on any of the 4 sides (or ends)
August 26, 2014	FN7908.2	Updated the “ESD Rating” on page 5, added the test method used for HBM and MM, changed CDM test method from “JESD22-C101E” to “AEC-Q100-11”. Updated “About Intersil” on page 16 to new verbiage.
January 14, 2014	FN7908.1	Page 17 - 2nd line of the disclaimer changed from: "Intersil products are manufactured, assembled and tested utilizing ISO9001 quality systems as noted" to: "Intersil Automotive Qualified products are manufactured, assembled and tested utilizing TS16949 quality systems as noted" - Updated "Products" verbiage to "About Intersil" verbiage
February 24, 2012	FN7908.0	Initial release.

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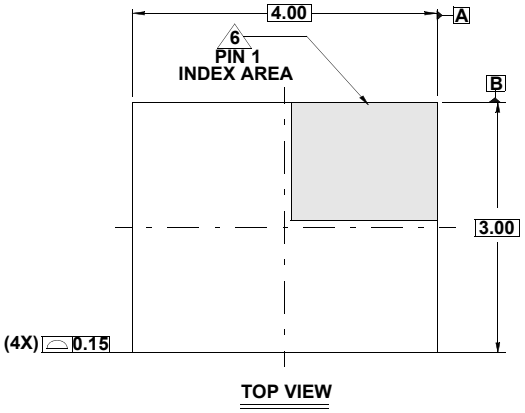
Package Outline Drawing

For the most recent package outline drawing, see L12.4x3.

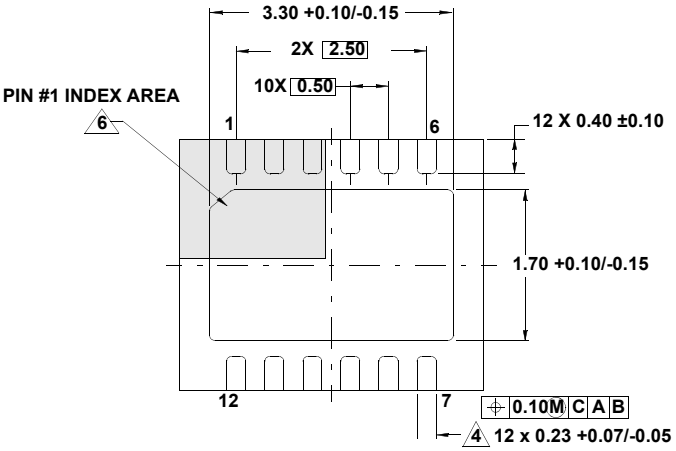
L12.4x3

12 LEAD DUAL FLAT NO-LEAD PLASTIC PACKAGE

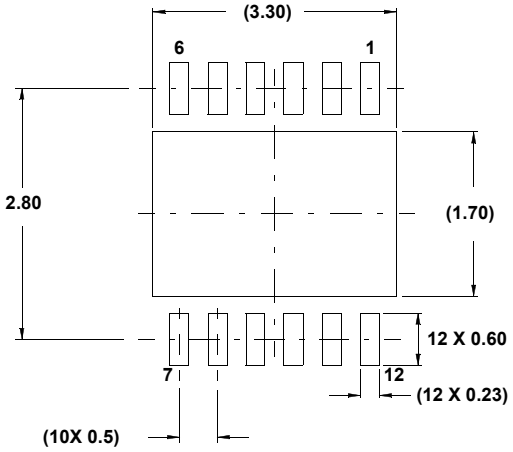
Rev 3, 3/15



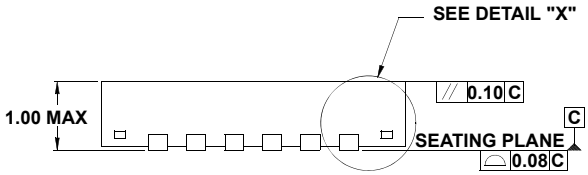
TOP VIEW



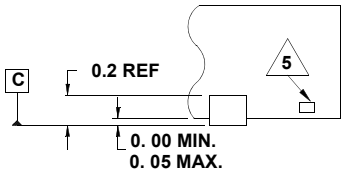
BOTTOM VIEW



TYPICAL RECOMMENDED LAND PATTERN



SIDE VIEW



DETAIL "X"

NOTES:

1. Dimensions are in millimeters.
   Dimensions in ( ) for Reference Only.
2. Dimensioning and tolerancing conform to AMSE Y14.5m-1994.
3. Unless otherwise specified, tolerance: Decimal ± 0.05
4. Dimension applies to the metallized terminal and is measured between 0.15mm and 0.30mm from the terminal tip.
5. Tiebar shown (if present) is a non-functional feature and may be located on any of the 4 sides (or ends).
6. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 identifier may be either a mold or mark feature.
7. Compliant to JEDEC MO-229 V4030D-4 issue E.

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