

# PMPB33XN

30 V single N-channel Trench MOSFET

6 July 2012

Product data sheet

## 1. Product profile

### 1.1 General description

N-channel enhancement mode Field-Effect Transistor (FET) in a leadless medium power DFN2020MD-6 (SOT1220) Surface-Mounted Device (SMD) plastic package using Trench MOSFET technology.

### 1.2 Features and benefits

- Trench MOSFET technology
- Very fast switching
- Small and leadless ultra thin SMD plastic package: 2 x 2 x 0.65 mm
- Exposed drain pad for excellent thermal conduction
- Tin-plated 100 % solderable side pads for optical solder inspection

### 1.3 Applications

- Charging switch for portable devices
- DC-to-DC converters
- Power management in battery-driven portables
- Hard disk and computing power management

### 1.4 Quick reference data

Table 1. Quick reference data

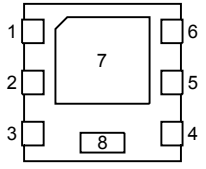
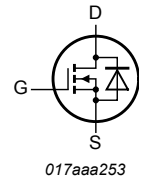
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{DS}$	drain-source voltage	$T_j = 25\text{ }^\circ\text{C}$	-	-	30	V
$V_{GS}$	gate-source voltage		-12	-	12	V
$I_D$	drain current	$V_{GS} = 4.5\text{ V}; T_{amb} = 25\text{ }^\circ\text{C}; t \leq 5\text{ s}$	[1]	-	5.5	A
<b>Static characteristics</b>						
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = 4.5\text{ V}; I_D = 4.3\text{ A}; T_j = 25\text{ }^\circ\text{C}$	-	37	47	m $\Omega$

[1] Device mounted on an FR4 Printed-Circuit Board (PCB), single-sided copper, tin-plated, mounting pad for drain 6 cm<sup>2</sup>.



## 2. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	D	drain	 <p>Transparent top view DFN2020MD-6 (SOT1220)</p>	 <p>017aaa253</p>
2	D	drain		
3	G	gate		
4	S	source		
5	D	drain		
6	D	drain		
7	D	drain		
8	S	source		

## 3. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
PMPB33XN	DFN2020MD-6	plastic thermal enhanced ultra thin small outline package; no leads; 6 terminals	SOT1220

## 4. Marking

Table 4. Marking codes

Type number	Marking code
PMPB33XN	1P

## 5. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit	
$V_{DS}$	drain-source voltage	$T_j = 25\text{ }^\circ\text{C}$	-	30	V	
$V_{GS}$	gate-source voltage		-12	12	V	
$I_D$	drain current	$V_{GS} = 4.5\text{ V}; T_{amb} = 25\text{ }^\circ\text{C}; t \leq 5\text{ s}$	[1]	-	5.5	A
		$V_{GS} = 4.5\text{ V}; T_{amb} = 25\text{ }^\circ\text{C}$	[1]	-	4.3	A
		$V_{GS} = 4.5\text{ V}; T_{amb} = 100\text{ }^\circ\text{C}$	[1]	-	2.7	A
$I_{DM}$	peak drain current	$T_{amb} = 25\text{ }^\circ\text{C}; \text{single pulse}; t_p \leq 10\text{ }\mu\text{s}$	-	17	A	
$P_{tot}$	total power dissipation	$T_{amb} = 25\text{ }^\circ\text{C}$	[1]	-	1.5	W

Symbol	Parameter	Conditions		Min	Max	Unit
		$T_{amb} = 25\text{ °C}; t \leq 5\text{ s}$	[1]	-	2.4	W
		$T_{sp} = 25\text{ °C}$		-	8.3	W
$T_j$	junction temperature			-55	150	°C
$T_{amb}$	ambient temperature			-55	150	°C
$T_{stg}$	storage temperature			-65	150	°C
<b>Source-drain diode</b>						
$I_S$	source current	$T_{amb} = 25\text{ °C}$	[1]	-	1.7	A

[1] Device mounted on an FR4 Printed-Circuit Board (PCB), single-sided copper, tin-plated, mounting pad for drain 6 cm<sup>2</sup>.

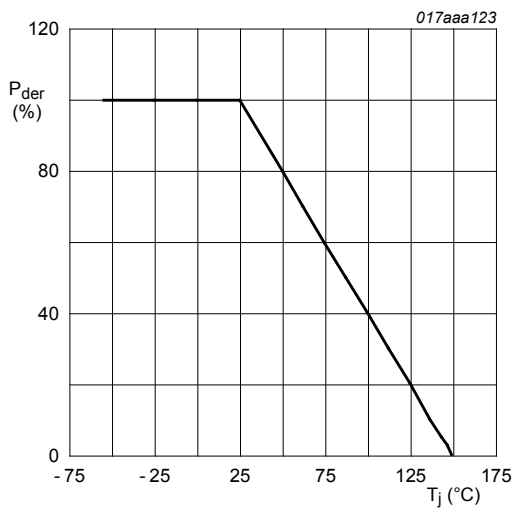


Fig. 1. Normalized total power dissipation as a function of junction temperature

$$P_{der} = \frac{P_{tot}}{P_{tot(25^\circ\text{C})}} \times 100\%$$

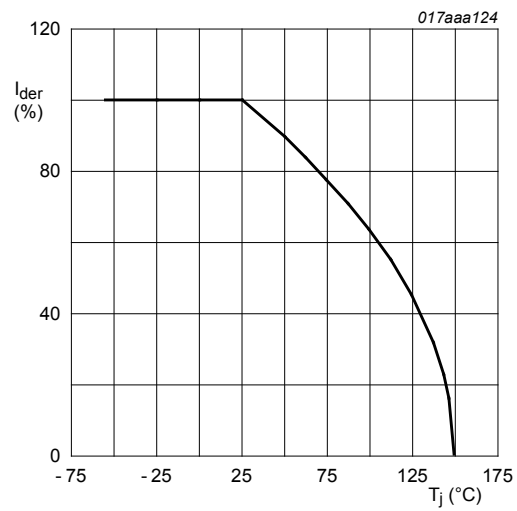
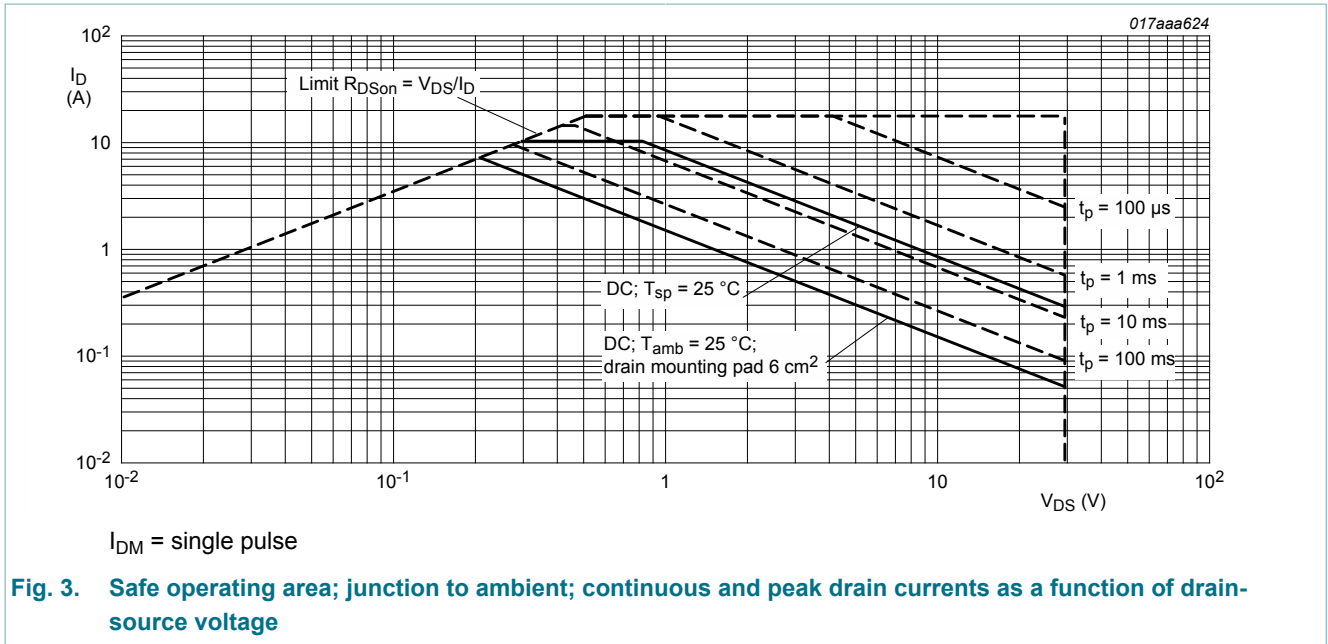


Fig. 2. Normalized continuous drain current as a function of junction temperature

$$I_{der} = \frac{I_D}{I_{D(25^\circ\text{C})}} \times 100\%$$



## 6. Thermal characteristics

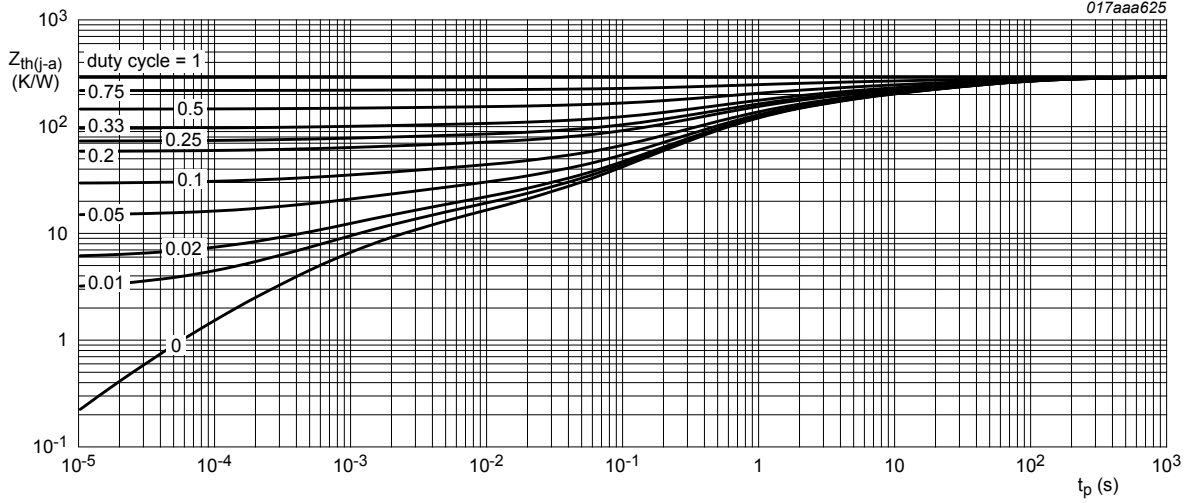
Table 6. Thermal characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air	[1]	-	245	280	K/W
			[2]	-	74	85	K/W
			[3]	-	45	52	K/W
$R_{th(j-sp)}$	thermal resistance from junction to solder point		-	10	15	K/W	

[1] Device mounted on an FR4 PCB, single-sided copper, tin-plated and standard footprint.

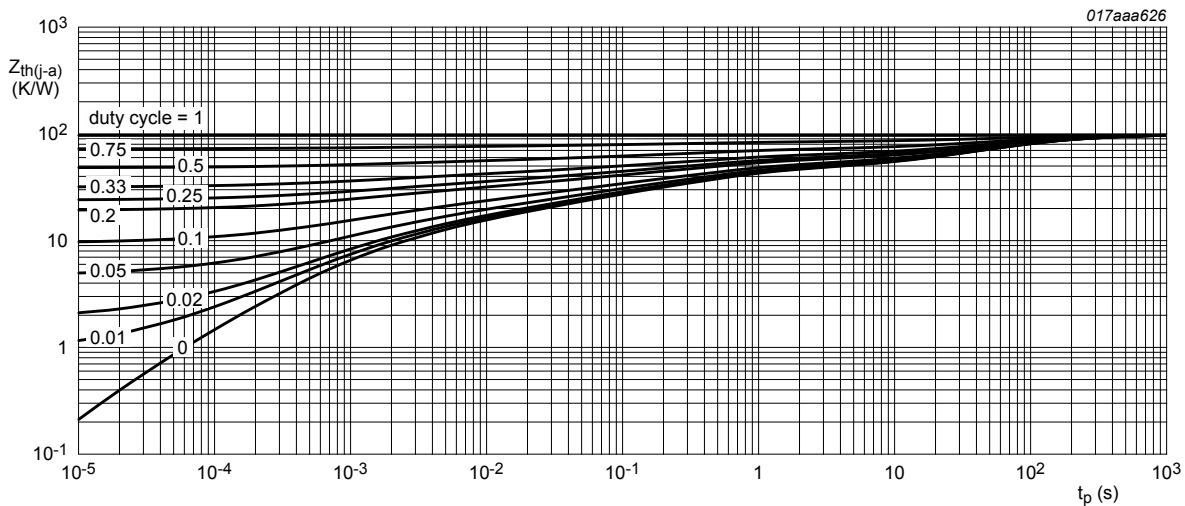
[2] Device mounted on an FR4 PCB, single-sided copper, tin-plated, mounting pad for drain  $6\text{ cm}^2$ .

[3] Device mounted on an FR4 PCB, single-sided copper, tin-plated, mounting pad for drain  $6\text{ cm}^2$ ,  $t \leq 5\text{ s}$



FR4 PCB, standard footprint

Fig. 4. Transient thermal impedance from junction to ambient as a function of pulse duration; typical values



FR4 PCB, mounting pad for drain 6 cm<sup>2</sup>

Fig. 5. Transient thermal impedance from junction to ambient as a function of pulse duration; typical values

## 7. Characteristics

Table 7. Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>Static characteristics</b>						
$V_{(BR)DSS}$	drain-source breakdown voltage	$I_D = 250 \mu A; V_{GS} = 0 V; T_j = 25 \text{ }^\circ C$	30	-	-	V
$V_{GSth}$	gate-source threshold voltage	$I_D = 250 \mu A; V_{DS} = V_{GS}; T_j = 25 \text{ }^\circ C$	0.45	0.8	1.2	V
$I_{DSS}$	drain leakage current	$V_{DS} = 30 V; V_{GS} = 0 V; T_j = 25 \text{ }^\circ C$	-	-	1	$\mu A$
		$V_{DS} = 30 V; V_{GS} = 0 V; T_j = 150 \text{ }^\circ C$	-	-	100	$\mu A$

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I <sub>GSS</sub>	gate leakage current	V <sub>GS</sub> = 12 V; V <sub>DS</sub> = 0 V; T <sub>j</sub> = 25 °C	-	-	100	nA
		V <sub>GS</sub> = -12 V; V <sub>DS</sub> = 0 V; T <sub>j</sub> = 25 °C	-	-	100	nA
R <sub>DSon</sub>	drain-source on-state resistance	V <sub>GS</sub> = 4.5 V; I <sub>D</sub> = 4.3 A; T <sub>j</sub> = 25 °C	-	37	47	mΩ
		V <sub>GS</sub> = 4.5 V; I <sub>D</sub> = 4.3 A; T <sub>j</sub> = 150 °C	-	63	80	mΩ
		V <sub>GS</sub> = 2.5 V; I <sub>D</sub> = 1 A; T <sub>j</sub> = 25 °C	-	55	76	mΩ
g <sub>fs</sub>	forward transconductance	V <sub>DS</sub> = 10 V; I <sub>D</sub> = 4.3 A; T <sub>j</sub> = 25 °C	-	20	-	S
R <sub>G</sub>	gate resistance	f = 1 MHz	-	9.8	-	Ω
<b>Dynamic characteristics</b>						
Q <sub>G(tot)</sub>	total gate charge	V <sub>DS</sub> = 15 V; I <sub>D</sub> = 4.3 A; V <sub>GS</sub> = 4.5 V; T <sub>j</sub> = 25 °C	-	5.1	7.6	nC
Q <sub>GS</sub>	gate-source charge		-	1	-	nC
Q <sub>GD</sub>	gate-drain charge		-	1.3	-	nC
C <sub>iss</sub>	input capacitance	V <sub>DS</sub> = 15 V; f = 1 MHz; V <sub>GS</sub> = 0 V; T <sub>j</sub> = 25 °C	-	505	-	pF
C <sub>oss</sub>	output capacitance		-	57	-	pF
C <sub>rss</sub>	reverse transfer capacitance		-	48	-	pF
t <sub>d(on)</sub>	turn-on delay time	V <sub>DS</sub> = 15 V; I <sub>D</sub> = 4.3 A; V <sub>GS</sub> = 4.5 V; R <sub>G(ext)</sub> = 6 Ω; T <sub>j</sub> = 25 °C	-	6	-	ns
t <sub>r</sub>	rise time		-	17	-	ns
t <sub>d(off)</sub>	turn-off delay time		-	21	-	ns
t <sub>f</sub>	fall time		-	20	-	ns
<b>Source-drain diode</b>						
V <sub>SD</sub>	source-drain voltage	I <sub>S</sub> = 1.7 A; V <sub>GS</sub> = 0 V; T <sub>j</sub> = 25 °C	-	0.8	1.2	V

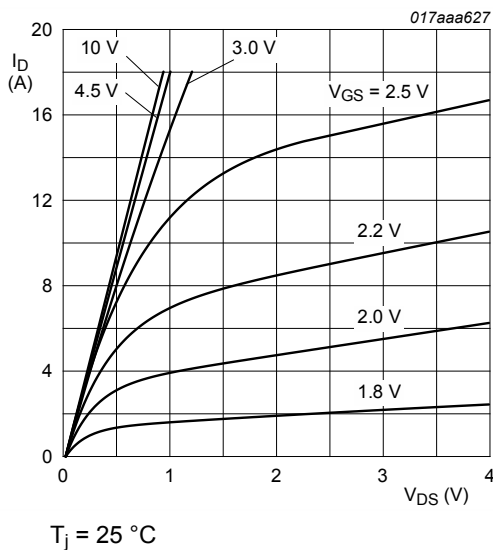


Fig. 6. Output characteristics: drain current as a function of drain-source voltage; typical values

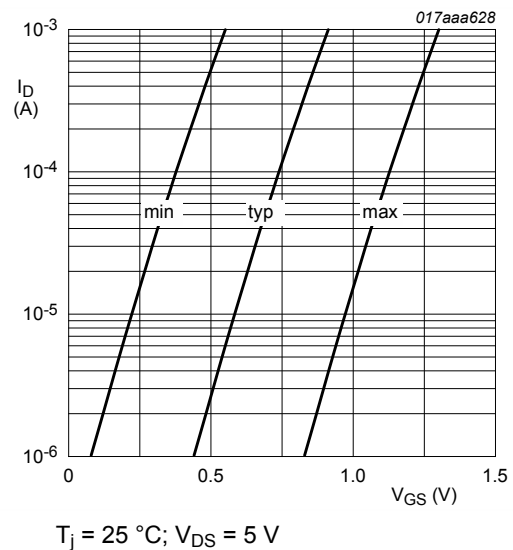


Fig. 7. Sub-threshold drain current as a function of gate-source voltage

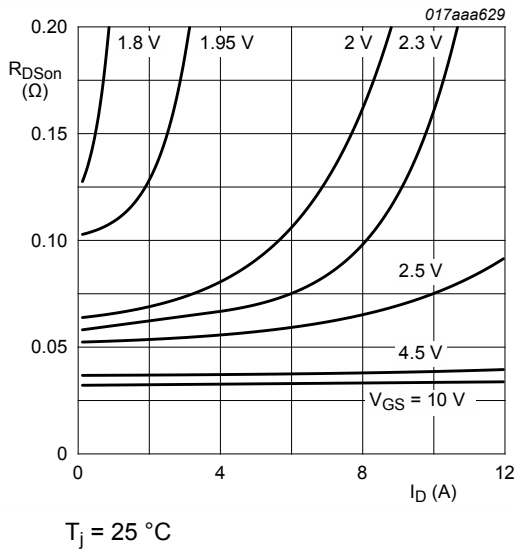


Fig. 8. Drain-source on-state resistance as a function of drain current; typical values

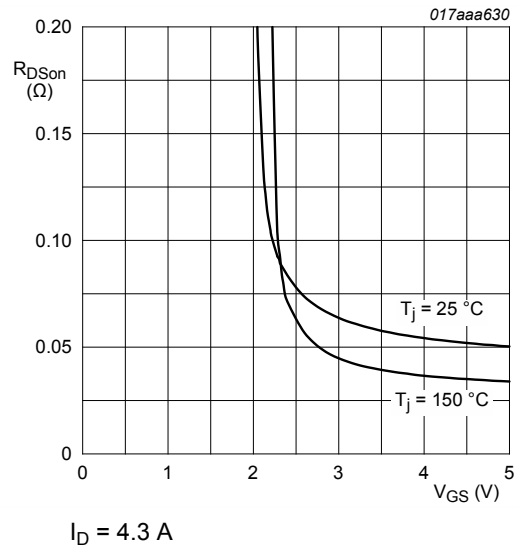


Fig. 9. Drain-source on-state resistance as a function of gate-source voltage; typical values

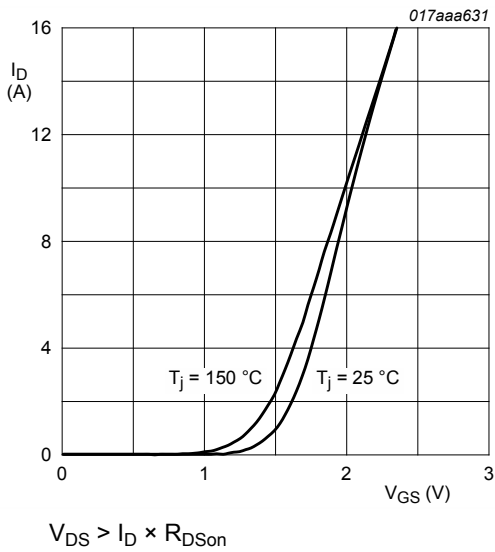


Fig. 10. Transfer characteristics: drain current as a function of gate-source voltage; typical values

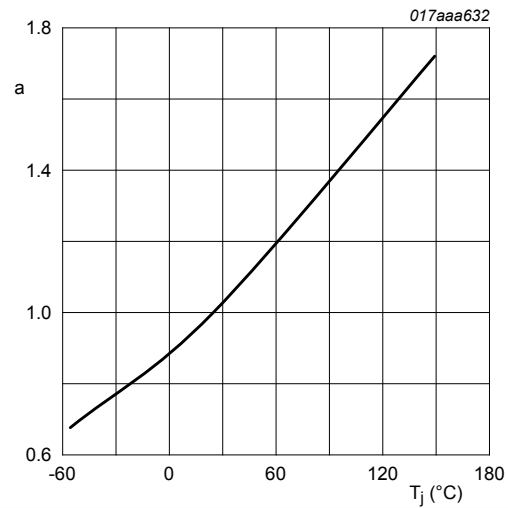
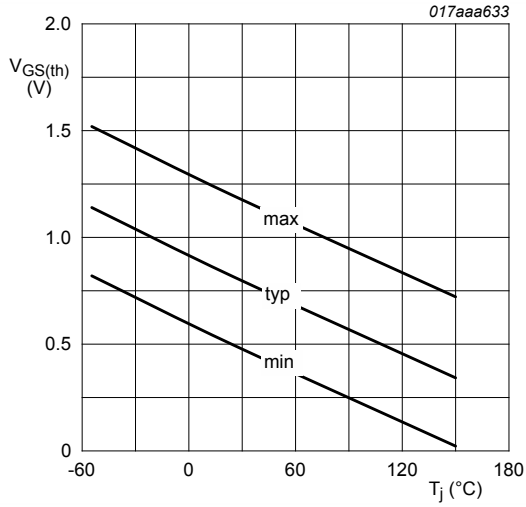


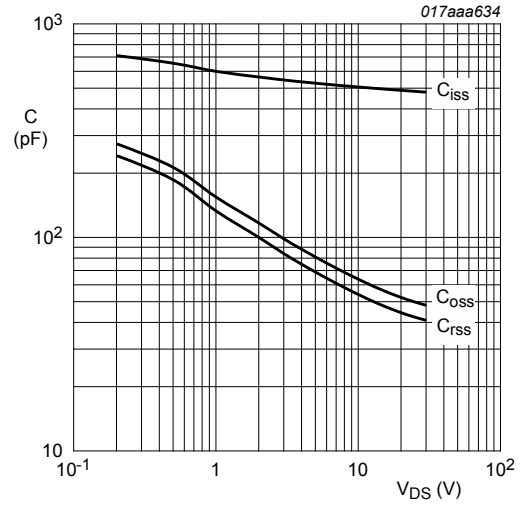
Fig. 11. Normalized drain-source on-state resistance as a function of junction temperature; typical values

$$a = \frac{R_{DSon}}{R_{DSon}(25^\circ\text{C})}$$



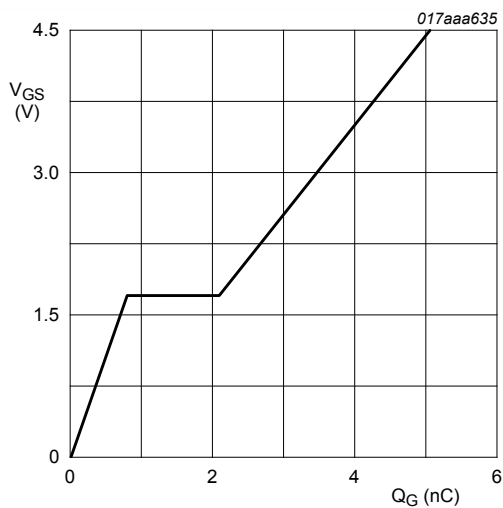
$I_D = 0.25$  mA;  $V_{DS} = V_{GS}$

Fig. 12. Gate-source threshold voltage as a function of junction temperature



$f = 1$  MHz;  $V_{GS} = 0$  V

Fig. 13. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values



$I_D = 4.3$  A;  $V_{DS} = 15$  V;  $T_{amb} = 25$  °C

Fig. 14. Gate-source voltage as a function of gate charge; typical values

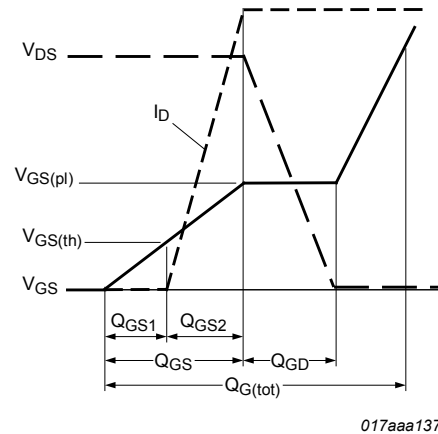
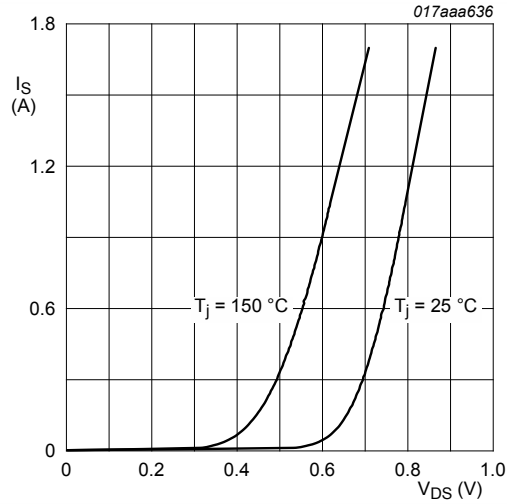


Fig. 15. Gate charge waveform definitions





$V_{GS} = 0\text{ V}$

Fig. 16. Source current as a function of source-drain voltage; typical values

### 8. Test information

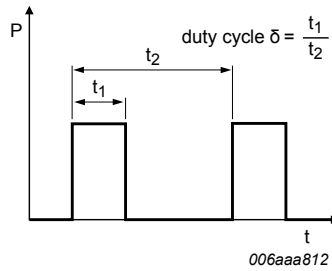


Fig. 17. Duty cycle definition

### 9. Package outline

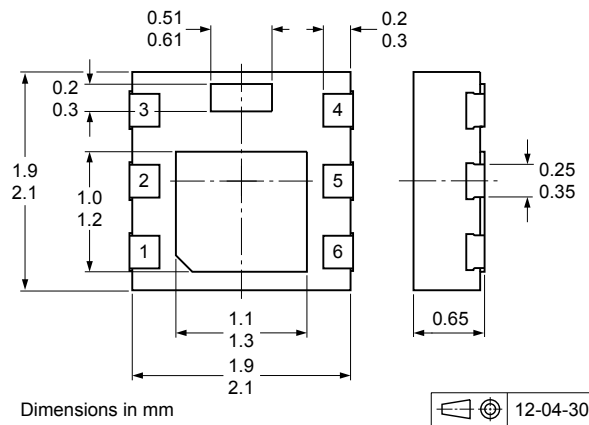


Fig. 18. DFN2020MD-6 (SOT1220)

### 10. Soldering

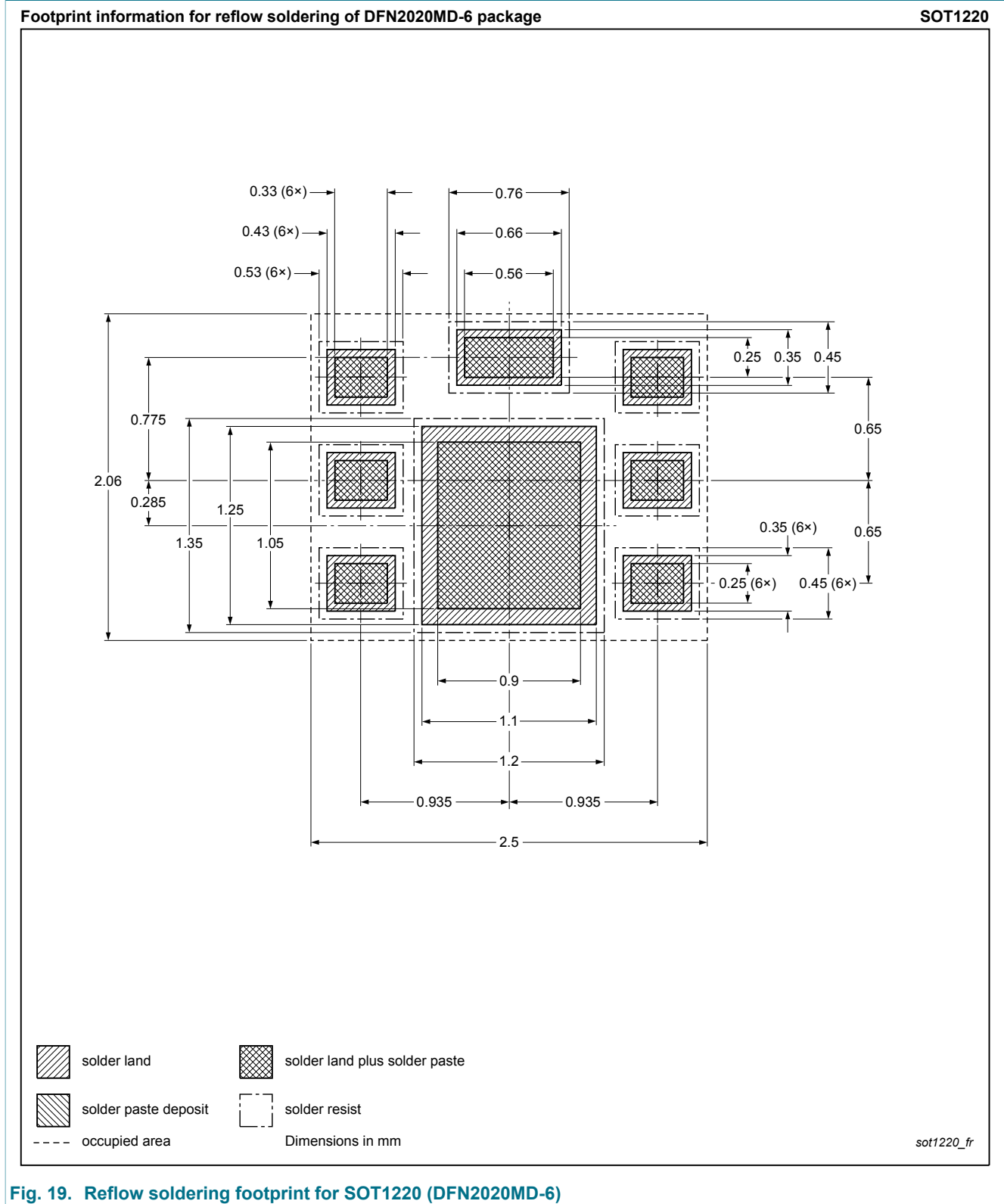


Fig. 19. Reflow soldering footprint for SOT1220 (DFN2020MD-6)

## 11. Revision history

Table 8. Revision history

Data sheet ID	Release date	Data sheet status	Change notice	Supersedes
PMPB33XN v.1	20120706	Product data sheet	-	-

## 12. Legal information

### 12.1 Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
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[MCIMX6Q-SDB](#) [MCIMX6SX-SDB](#) [74ALVC125BQ,115](#) [74HC4050N](#) [74HC4514N](#) [MK21FN1M0AVLQ12](#) [MKV30F128VFM10](#) [FRDM-K66F](#) [FRDM-KW40Z](#) [FRDM-MC-LVBLDC](#) [PESD18VF1BSFYL](#) [PMF63UNEX](#) [PSMN4R0-60YS,115](#) [HEF4028BPN](#) [RAPPID-567XFSW](#)  
[MPC565MVR56](#) [MPC574XG-176DS](#) [MPC860PCVR66D4](#) [BT137-600E](#) [BT139X-600.127](#) [BUK7628-100A118](#) [BUK765R0-100E.118](#)  
[BZT52H-B9V1.115](#) [BZV85-C3V9.113](#) [BZX79-C47.113](#) [P5020NSE7VNB](#) [S12ZVML12EVBLIN](#) [SCC2692AC1N40](#) [LPC1785FBD208K](#)  
[LPC2124FBD64/01](#) [LS1020ASN7KQB](#) [LS1020AXN7HNB](#) [LS1020AXN7KQB](#) [LS1043ASE7PQA](#) [T1023RDB-PC](#)