

## 17-27GHz Down-Converter

### GaAs Monolithic Microwave IC in SMD leadless package

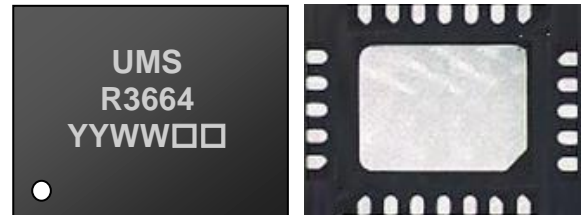
#### Description

The CHR3664-QEG is a multifunction monolithic circuit, which integrates a balanced cold FET mixer, a multiplier by two, and a RF LNA including gain control.

It is designed for a wide range of applications, typically ISM and commercial communication systems.

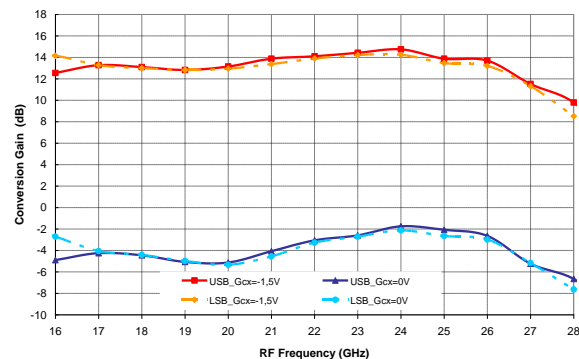
The circuit is manufactured with a pHEMT process, 0.25µm gate length, via holes through the substrate, air bridges and electron beam gate lithography.

It is supplied in RoHS compliant SMD package.



#### Main Features

- Broadband RF performance 17-27GHz
- 12dB conversion gain
- 3dBm Input IP3
- 16dB Gain Control
- 15dBc Image Rejection
- DC bias: Vd=4.0Volt @ Id=320mA
- 24L-QFN4x5
- MSL1



#### Main Characteristics

Tamb.= +25°C, Vd = 4.0V

Symbol	Parameter	Min	Typ	Max	Unit
F <sub>RF</sub>	RF frequency range	17		26.5	GHz
F <sub>OL</sub>	LO frequency range	7		15	GHz
F <sub>IF</sub>	IF frequency range	DC		3.5	GHz
G <sub>C</sub>	Conversion Gain		12		dB

## Main Characteristics

Tamb = +25°C, VD = VDL = 4.0V

Symbol	Parameter	Min	Typ	Max	Unit
F <sub>RF</sub>	RF frequency range	17		26.5	GHz
F <sub>OL</sub>	LO frequency range	7		15	GHz
F <sub>IF</sub>	IF frequency range	DC		3.5	GHz
G <sub>C</sub>	Conversion Gain @ min. attenuation	8	12		dB
ΔG	Gain control range		16		dB
NF	Noise Figure @ min. att. from 17 to 24GHz, for IF>0.1GHz		3.3	3.8	dB
	Noise Figure @ min. att. from 24 to 26.5GHz, for IF>0.1GHz		4.1	4.6	dB
Im_rej	Image rejection <sup>(1)</sup>		15		dBc
P <sub>LO</sub>	LO Input power		0	5	dBm
IIP3	Input IP3 @ min. attenuation	1	3		dBm
	Input IP3 @ all gain range (ΔG)	-4	-2		dBm
2LO/RF	2LO leakage at RF port @ max. gain		-40		dBc
VD, VDL	DC drain voltage		4.0		V
ID	Drain current on VD		245		mA
IDL	Drain current on VDL		75		mA
VGL	LNA DC gate voltage <sup>(2)</sup>		-0.6		V
GC2,3	Gain control DC voltage	-2	-1.5	+0.6	V
VGM	Mixer DC gate voltage		-0.7		V

These values are representative of onboard measurements as defined on the drawing in paragraph "Evaluation mother board".

<sup>(1)</sup> An external combiner 90° is required on I / Q.

<sup>(2)</sup> Typical VGL value for IDL = 75mA

See in paragraph " biasing option" other possibility to optimise differently the performances

Note: Id is not affected by gain control (GC2, GC3).

**Absolute Maximum Ratings** <sup>(1)</sup>T<sub>amb.</sub> = +25°C

Symbol	Parameter	Values	Unit
V <sub>d</sub>	Drain bias voltage	5	V
ID+IDL	Drain bias current	450	mA
VGL	LNA DC gate voltage	-2 to +0.4	V
VGM	Mixer DC gate voltage	-2 to +0.4	V
GC2,3	Gain control voltage	-2 to +0.8	V
P <sub>RF</sub>	Maximum peak input power overdrive	10	dBm
P <sub>LO</sub>	Maximum LO input power	10	dBm
T <sub>j</sub>	Junction temperature <sup>(2)</sup>	175	°C
T <sub>a</sub>	Operating temperature range	-40 to +85	°C
T <sub>stg</sub>	Storage temperature range	-55 to +150	°C

<sup>(1)</sup> Operation of this device above anyone of these parameters may cause permanent damage.

<sup>(2)</sup> See "Device thermal performances"

**Typical Bias Conditions**T<sub>amb.</sub> = +25°C

Symbol	Pad N°	Parameter	Values	Unit
V <sub>DL</sub> , V <sub>D</sub>	10, 12	DC drain voltages	4.0	V
ID+IDL	10, 12	Total drain current	320	mA
VGL	9	DC gate voltage	-0.6	V
VGM	11	DC gate voltage	-0.7	V
GC2, GC3	7, 8	Gain control DC voltage	-2 to +0.6	V

## Device thermal performances

All the figures given in this section are obtained assuming that the QFN device is cooled down only by conduction through the package thermal pad (no convection mode considered). The temperature is monitored at the package back-side interface (Tcase) as shown below. The system maximum temperature must be adjusted in order to guarantee that Tcase remains below than the maximum value specified in the next table. So, the system PCB must be designed to comply with this requirement.

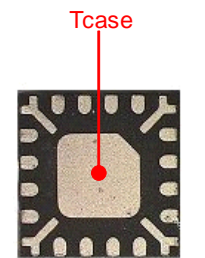
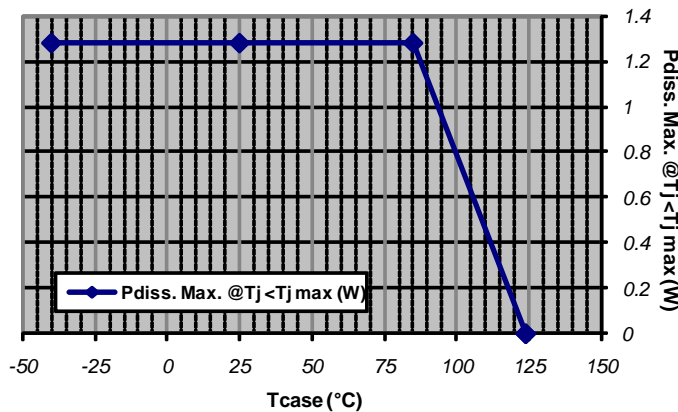
A derating must be applied on the dissipated power if the Tcase temperature cannot be maintained below than the maximum temperature specified (see the curve Pdiss. Max) in order to guarantee the nominal device life time (MTTF).

DEVICE THERMAL SPECIFICATION : CHR3664-QEG		
Recommended max. junction temperature (Tj max)	:	124 °C
Junction temperature absolute maximum rating	:	175 °C
Max. continuous dissipated power (Pdiss. Max.)	:	1.3 W
=> Pdiss. Max. derating above Tcase <sup>(1)</sup> = 85 °C	:	33 mW/°C
Junction-Case thermal resistance (Rth J-C) <sup>(2)</sup>	:	<30 °C/W
Minimum Tcase operating temperature <sup>(3)</sup>	:	-40 °C
Maximum Tcase operating temperature <sup>(3)</sup>	:	85 °C
Minimum storage temperature	:	-55 °C
Maximum storage temperature	:	150 °C

(1) Derating at junction temperature constant = Tj max.

(2) Rth J-C is calculated for a worst case considering the **hottest junction** of the MMIC and all the devices biased.

(3) Tcase=Package back side temperature measured under the die-attach-pad (see the drawing below).



Example: QFN 16L 3x3  
Location of temperature reference point (Tcase) on package's bottom side

6.0

Typical Board Measurements

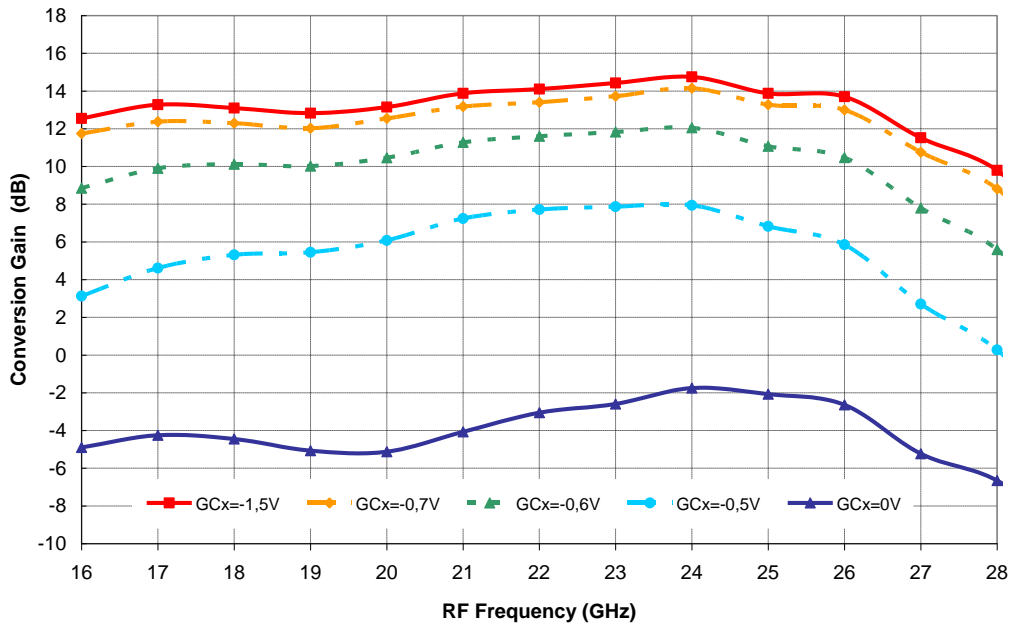
Tamb = +25°C, VD = VDL = 4.0V, VGL = -0.6V, VGM = -0.7V, P\_LO = 0dBm

If no specific mention, the following values are representative of onboard measurements (on connector access planes) as defined on the drawing at paragraph "Evaluation mother board". The board losses are estimated from 1.5 to 2dB in the frequency range.

Conversion Gain in Supradyne Mode versus RF Frequency & GCx

$$F_{RF} = 2 \times F_{LO} + F_{IF}, F_{IF} = 2.0\text{GHz}$$

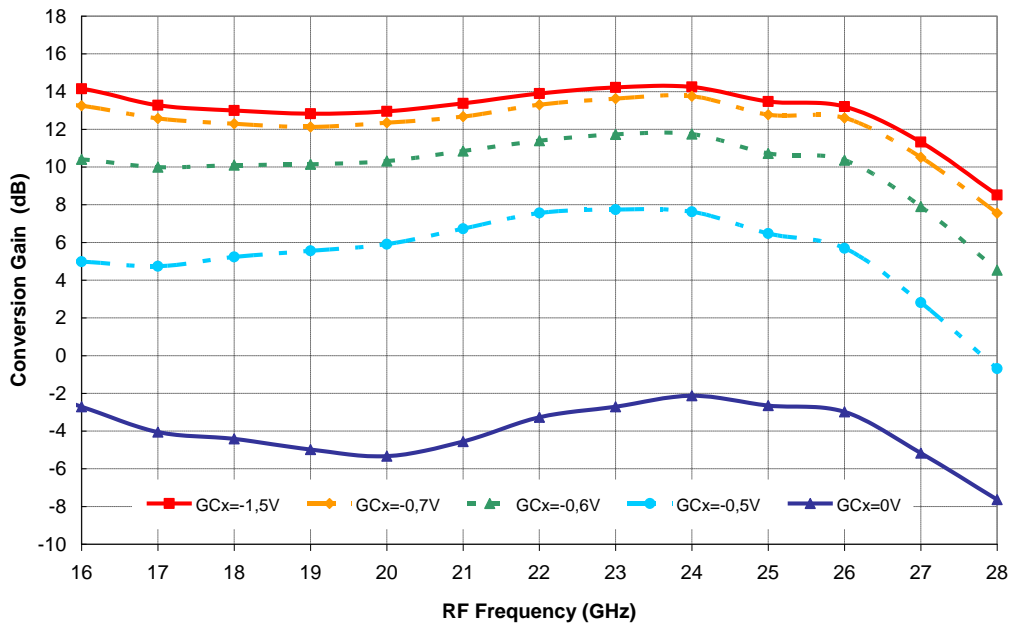
Board losses de-embedded (result given on package access planes)



Conversion Gain in Infradyne Mode versus RF Frequency & GCx

$$RF = 2 \times F_{LO} - F_{IF}, F_{IF} = 2.0\text{GHz}$$

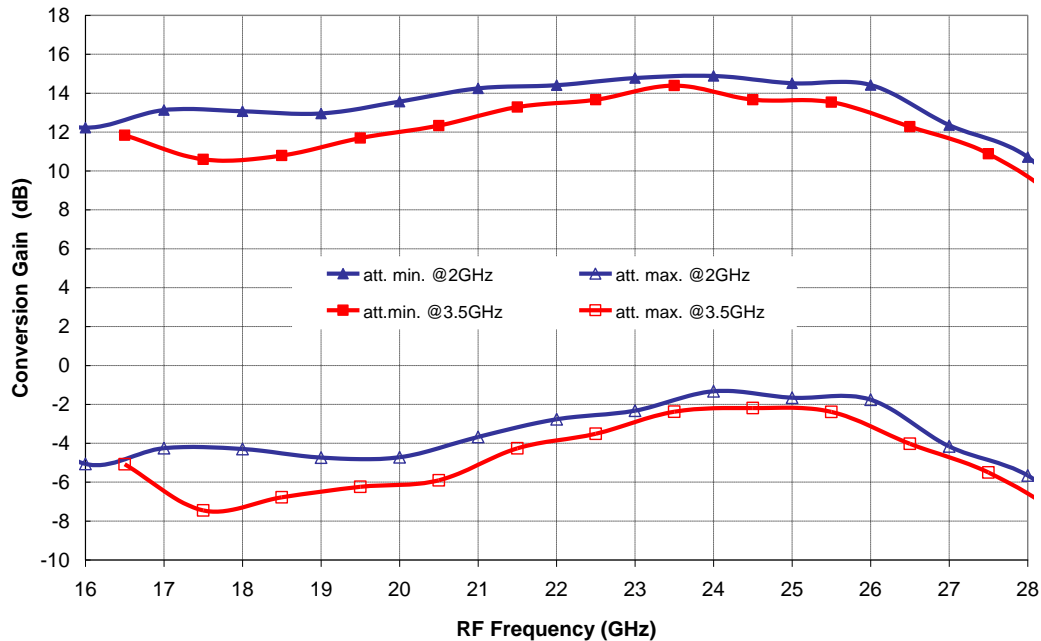
Board losses de-embedded (result given on package access planes)



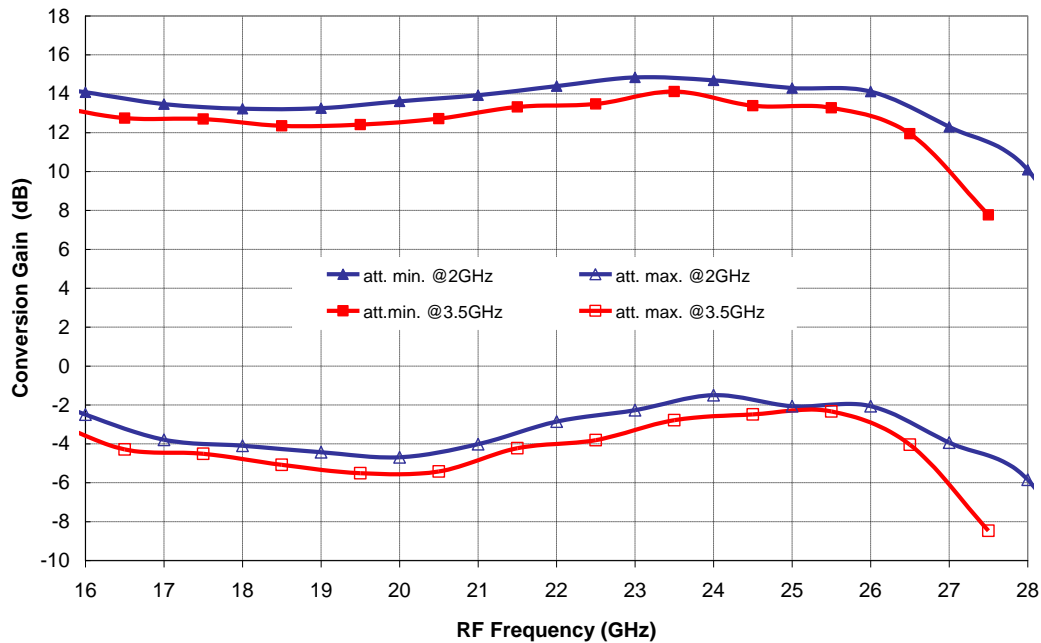
## Typical Board Measurements

Tamb = +25°C, VD = VDL = 4.0V, VGL = -0.6V, VGM = -0.7V, P\_LO = 0dBm

**Conversion Gain in Supradyn Mode versus RF Frequency & IF**  
 $F_{RF} = 2 \times F_{LO} + F_{IF}$ , GCx = -1.5V & 0V  
 Board losses de-embedded (result given on package access planes)

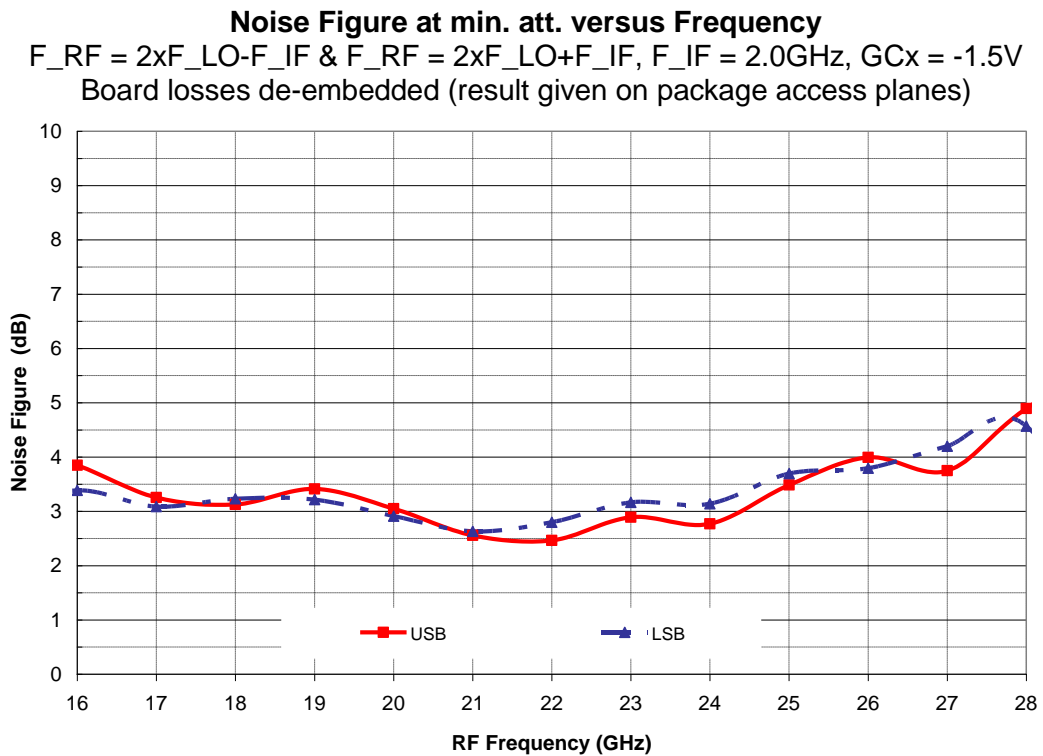
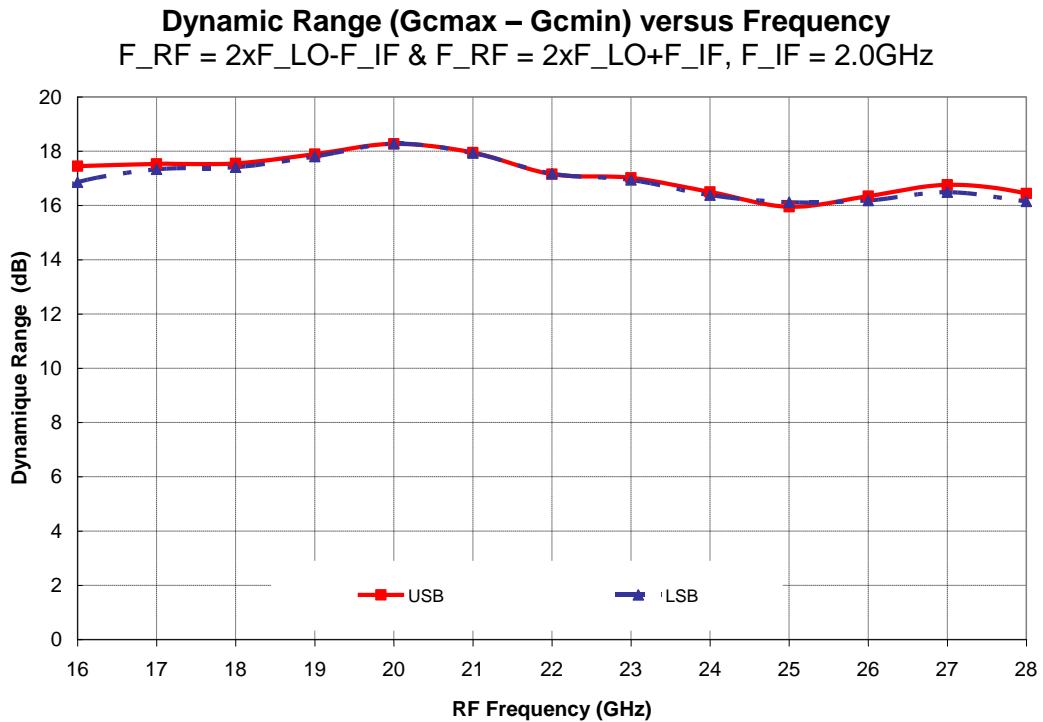


**Conversion Gain in Infradyne Mode versus RF Frequency & IF**  
 $RF = 2 \times F_{LO} - F_{IF}$ , GCx = -1.5 & 0V  
 Board losses de-embedded (result given on package access planes)



Typical Board Measurements

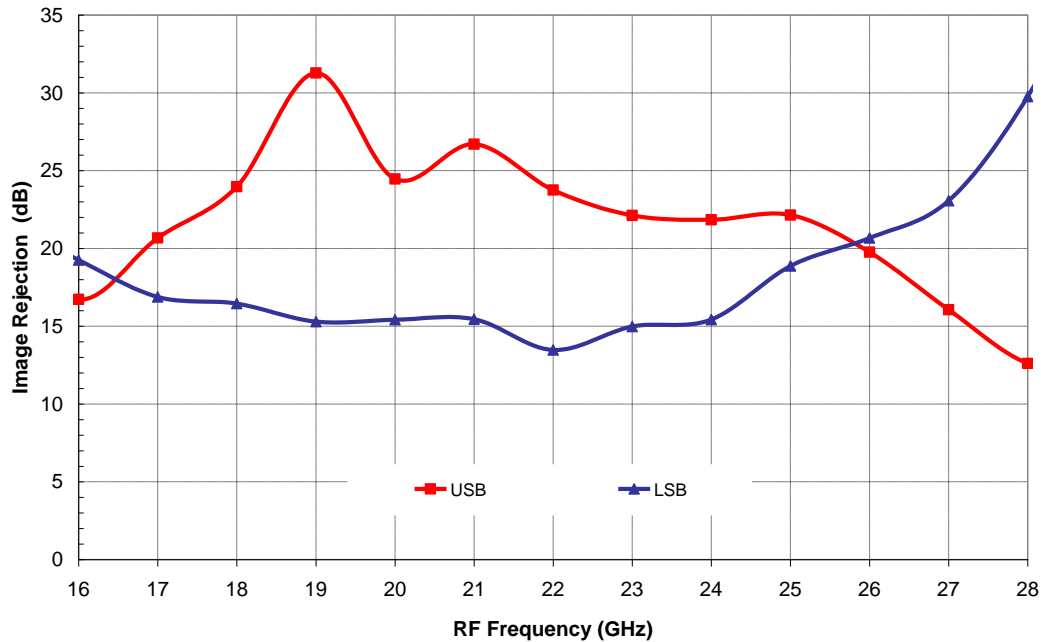
Tamb = +25°C, VD = VDL = 4.0V, VGL = -0.6V, VGM = -0.7V, P\_LO = 0dBm



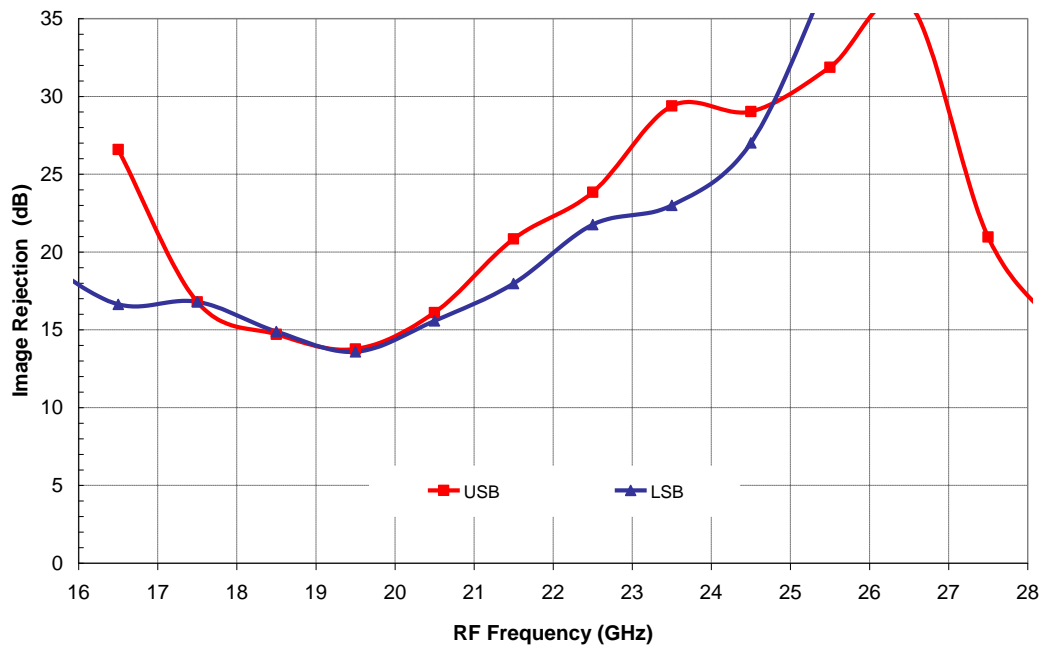
## Typical Board Measurements

Tamb = +25°C, VD = VDL = 4.0V, VGL = -0.6V, VGM = -0.7V, P\_LO = 0dBm

**Image Rejection on Supradyne & Infradyne Mode versus Frequency**  
 F\_IF = 2.0GHz, GCx = -1.5V



**Image Rejection on Supradyne & Infradyne Mode versus Frequency**  
 F\_IF = 3.5GHz, GCx = -1.5V

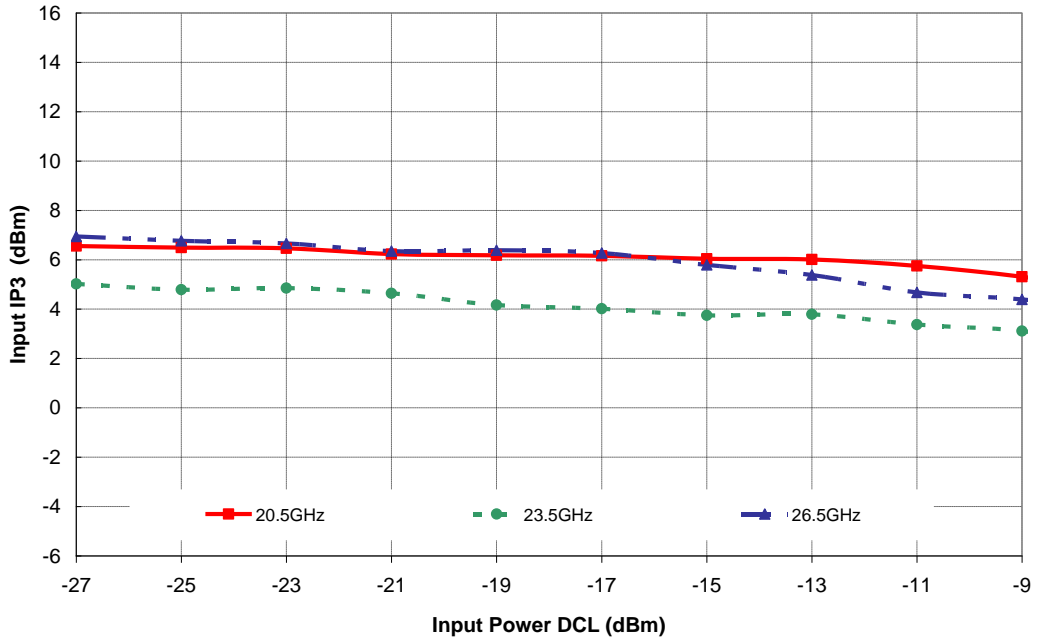




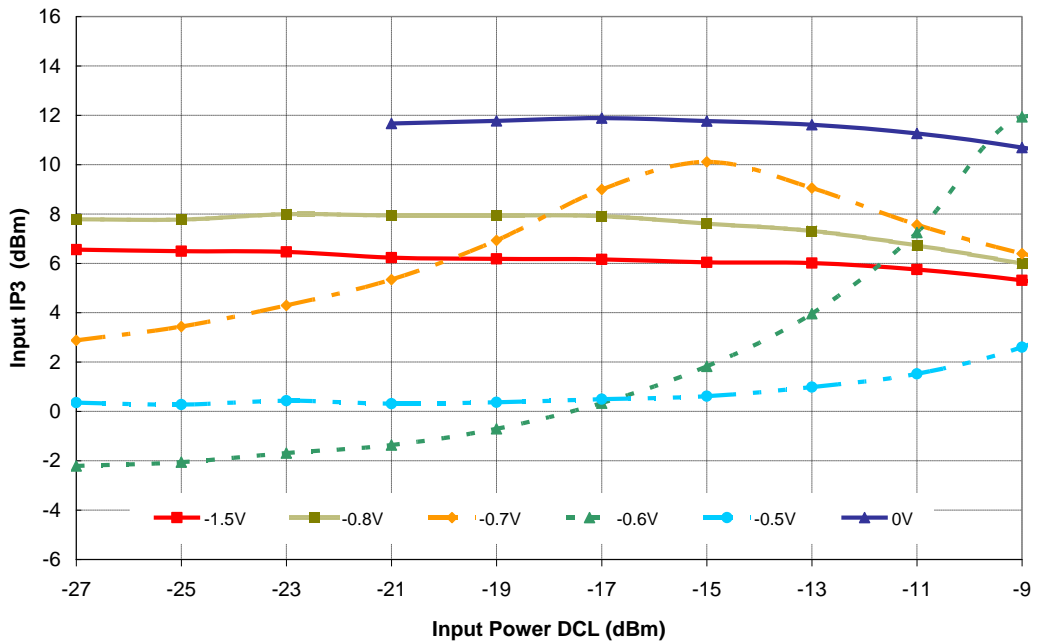
Typical Board Measurements

Tamb = +25°C, VD = VDL = 4.0V, VGL = -0.6V, VGM = -0.7V, P\_LO = 0dBm

Input IP3 versus Frequency at GCx = -1.5V  
 F\_RF = 2xF\_LO+F\_IF, F\_IF = 3.5GHz



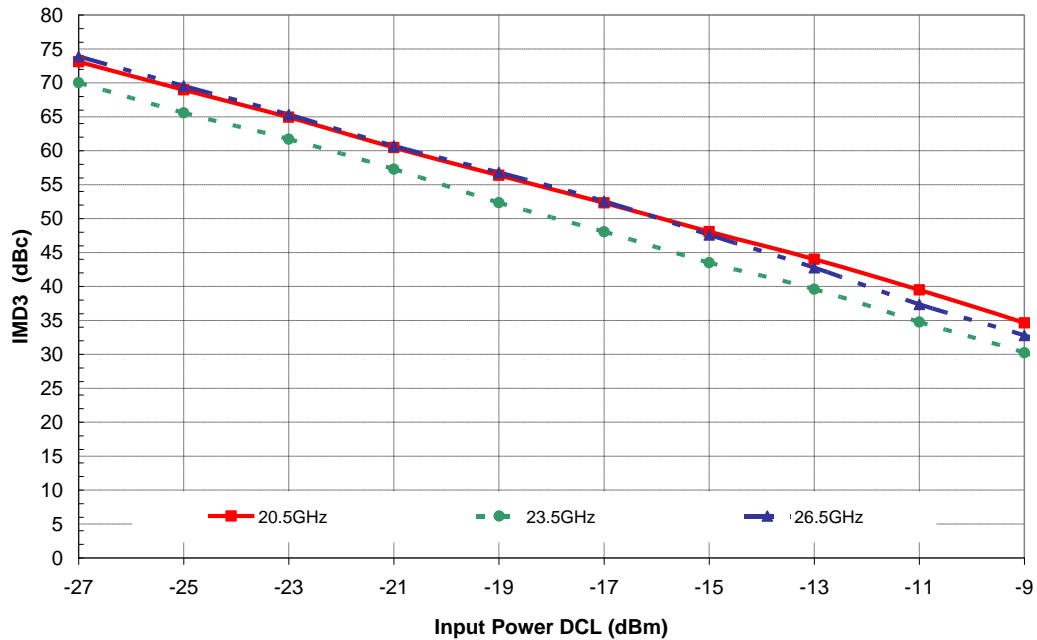
Input IP3 versus GCx  
 F\_RF = 2xF\_LO+F\_IF, F\_RF = 20.5GHz, F\_IF = 3.5GHz



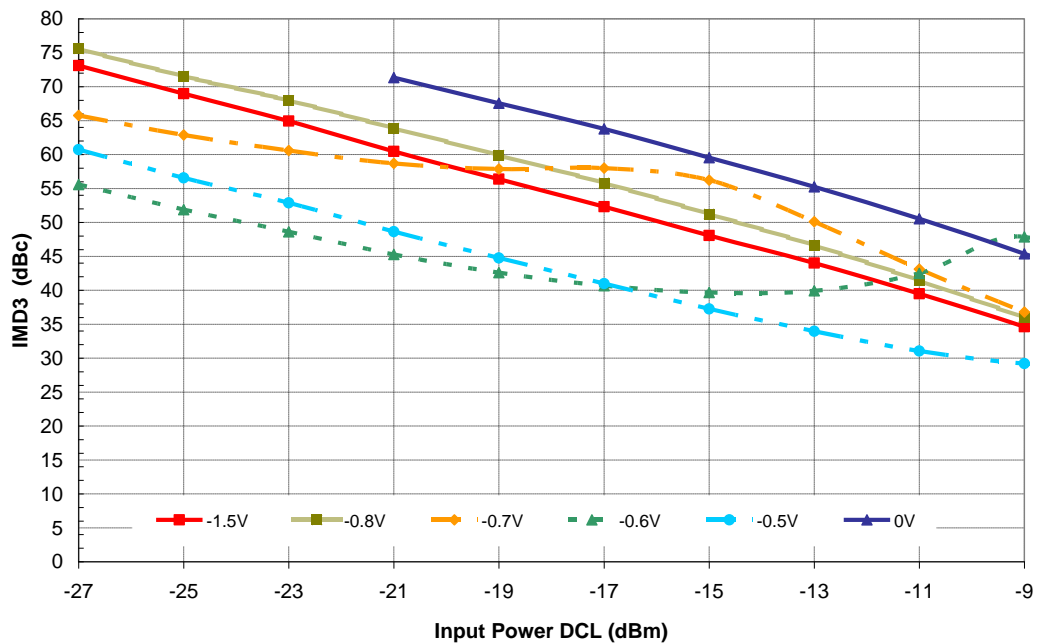
## Typical Board Measurements

Tamb = +25°C, VD = VDL = 4.0V, VGL = -0.6V, VGM = -0.7V, P\_LO = 0dBm

**IMD3 versus Frequency at GCx = -1.5V**  
 $F_{RF} = 2 \times F_{LO} + F_{IF}$ ,  $F_{IF} = 3.5\text{GHz}$



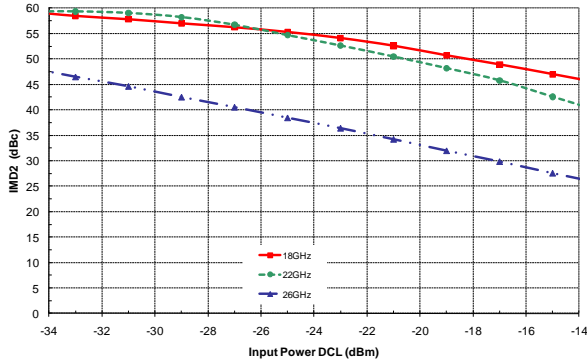
**IMD3 versus GCx**  
 $F_{RF} = 2 \times F_{LO} + F_{IF}$ ,  $F_{RF} = 20.5\text{GHz}$ ,  $F_{IF} = 3.5\text{GHz}$



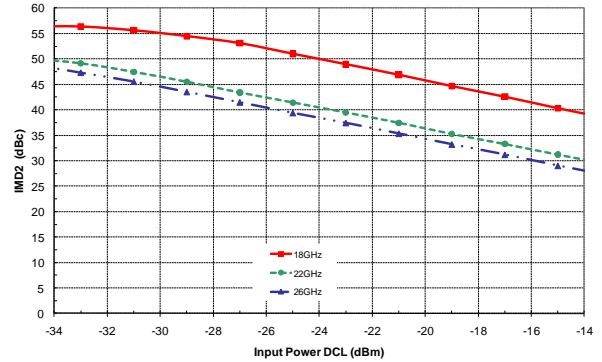
Typical Board Measurements

Tamb = +25°C, VD = VDL = 4.0V, VGL = -0.6V, VGM -0.7V, P\_LO = 0dBm

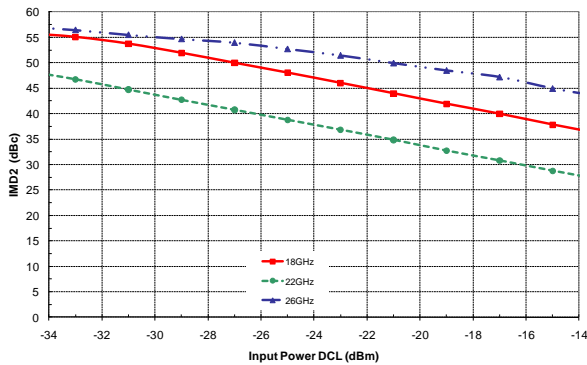
IMD2 versus Input power  
USB – lower tone  
F\_IF = 2.0GHz



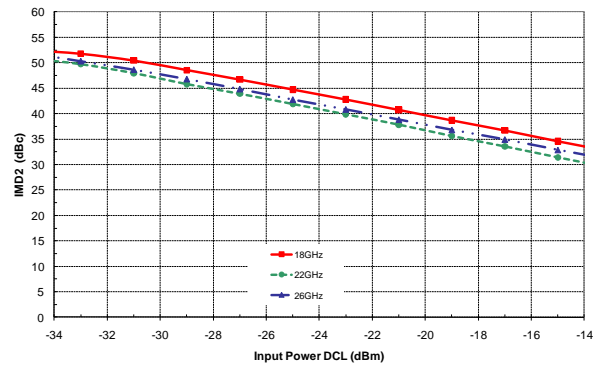
IMD2 versus Input power  
USB – higher tone  
F\_IF = 2.0GHz



IMD2 versus Input power  
LSB – lower tone  
F\_IF = 2.0GHz



IMD2 versus Input power  
LSB – higher tone  
F\_IF = 2.0GHz



Spurious on IF outputs

RF = 2LO – IF

P\_RF = -20dBm / P\_LO = 0dBm @10GHz

mRF	nLO					
	0	1	2	3	4	5
0	Xx	38	16	30	30	43
1	40	41	16	34	44	51
2	54	>75	>75	>75	30	52
3	>75	>75	>75	>75	>75	>75
4	>75	>75	>75	>75	>75	>75

All values in dBc below IF power level (IF = 1GHz).  
Data measured without external hybrid coupler.

## Temperature Board Measurements

T = [-40, +25, 85] °C, VD = VDL = 4.0V, VGL = -0.6V, VGM = -0.7V, P\_LO = 0 dBm

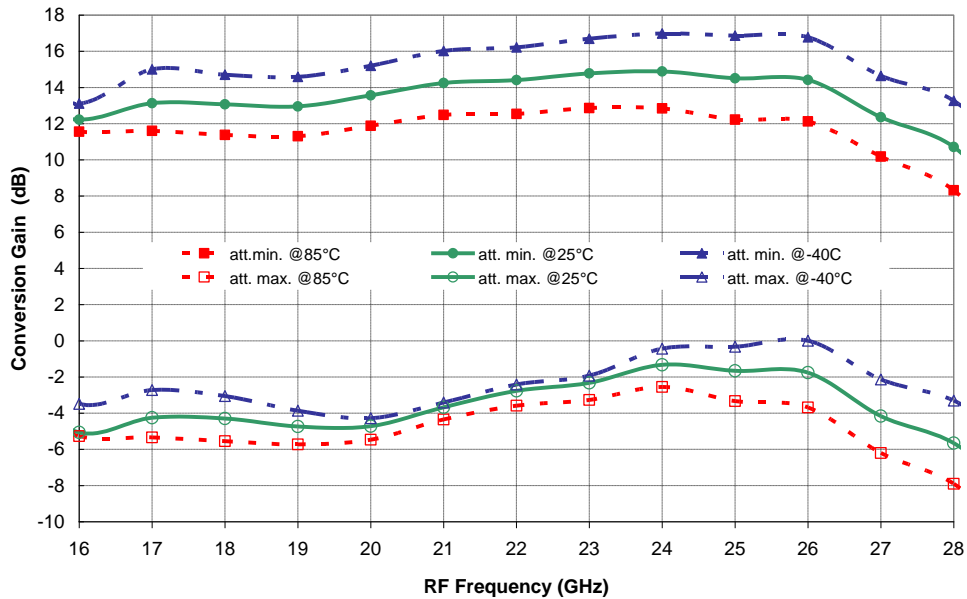
If no specific mention, the following values are representative of on board measurements (on connector access planes) as defined on the drawing at paragraph "Evaluation mother board".

The board losses are estimated from 1.5 to 2dB in the frequency range.

### Conversion Gain in Supradyne Mode versus Frequency

$F_{RF} = 2 \times F_{LO} + F_{IF}$ ,  $F_{IF} = 2.0\text{GHz}$ ,  $GCx = -1.5\text{V} \ \& \ 0\text{V}$

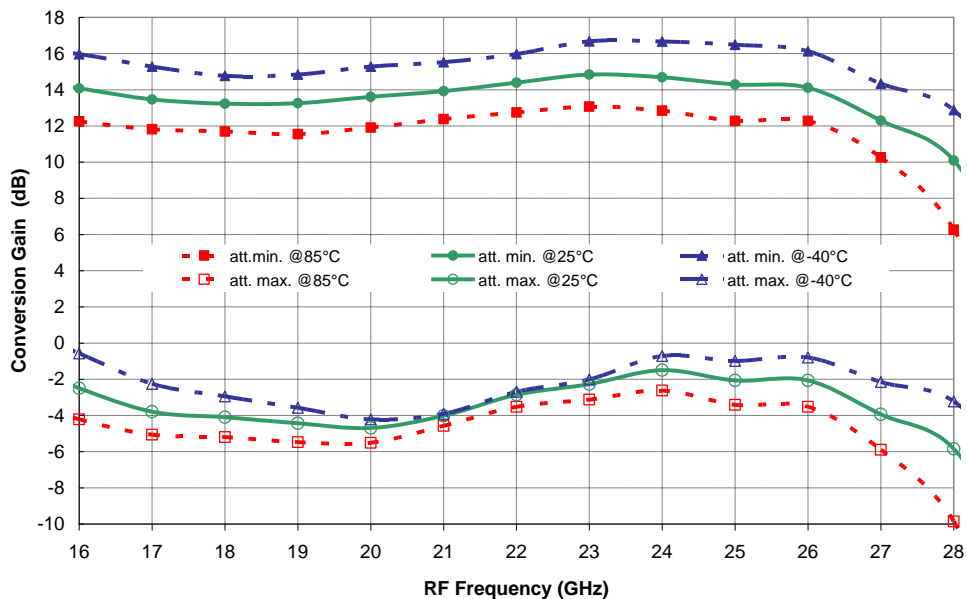
Board losses de-embedded (result given on package access planes)



### Conversion Gain in Infradyne Mode versus Frequency

$RF = 2 \times F_{LO} - F_{IF}$ ,  $F_{IF} = 2.0\text{GHz}$ ,  $GCx = -1.5\text{V} \ \& \ 0\text{V}$

Board losses de-embedded (result given on package access planes)



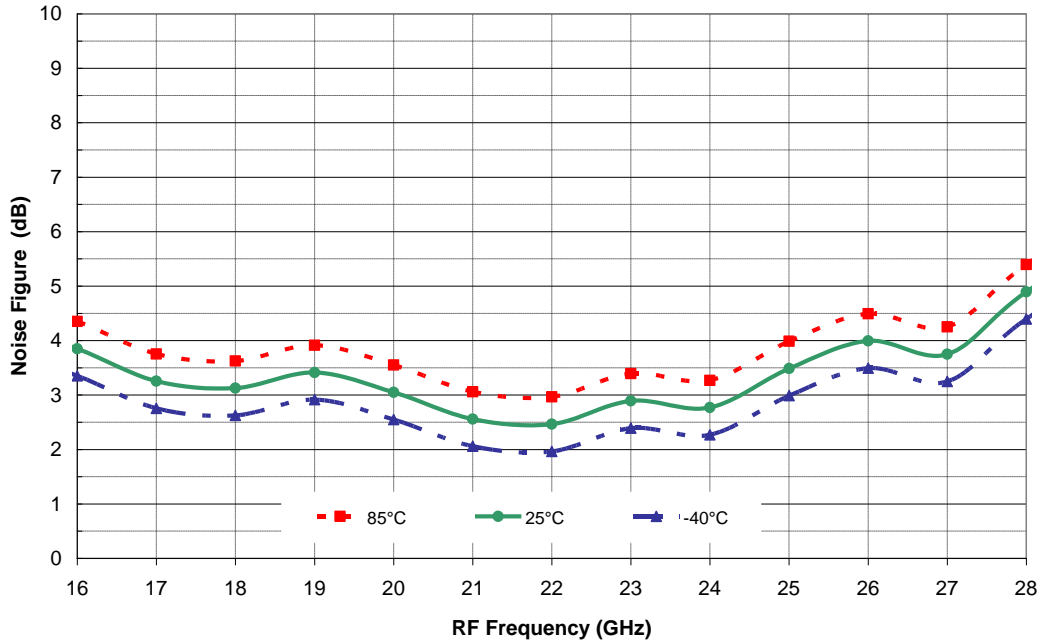
Temperature Board Measurements

T = [-40, +25, 85] °C, VD = VDL = 4.0V, VGL = -0.6V, VGM = -0.7V, P\_LO = 0 dBm

Noise Figure in Supradyn Mode at min. att. versus Frequency

$F_{RF} = 2 \times F_{LO} + F_{IF}$ ,  $F_{IF} = 2.0\text{GHz}$ ,  $GCx = -1.5\text{V}$

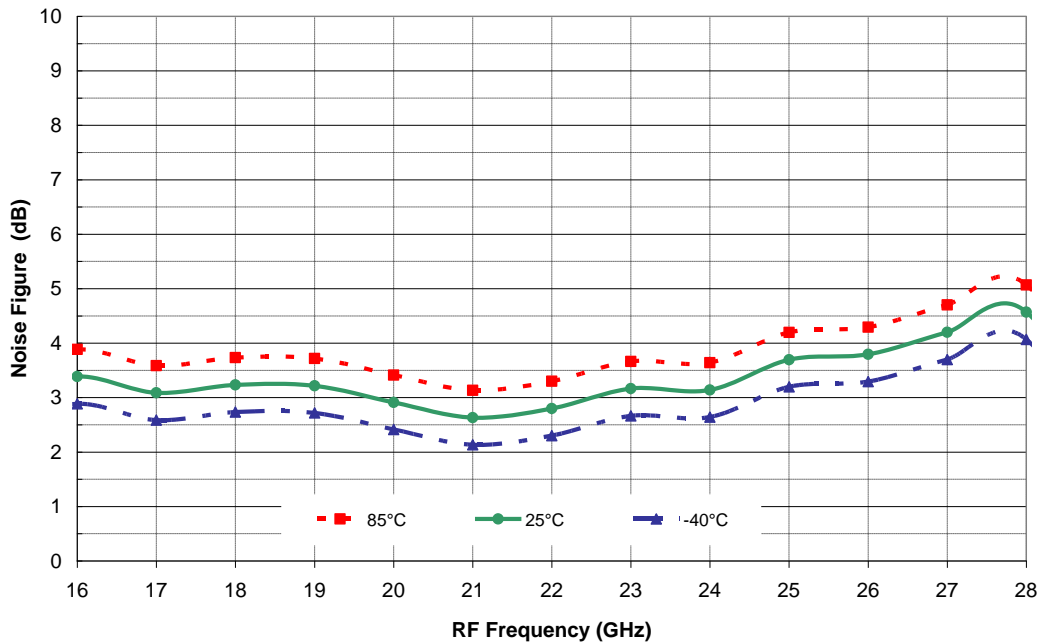
Board losses de-embedded (result given on package access planes)



Noise Figure in Infradyne Mode at min. att. versus Frequency

$F_{RF} = 2 \times F_{LO} - F_{IF}$ ,  $F_{IF} = 2.0\text{GHz}$ ,  $GCx = -1.5\text{V}$

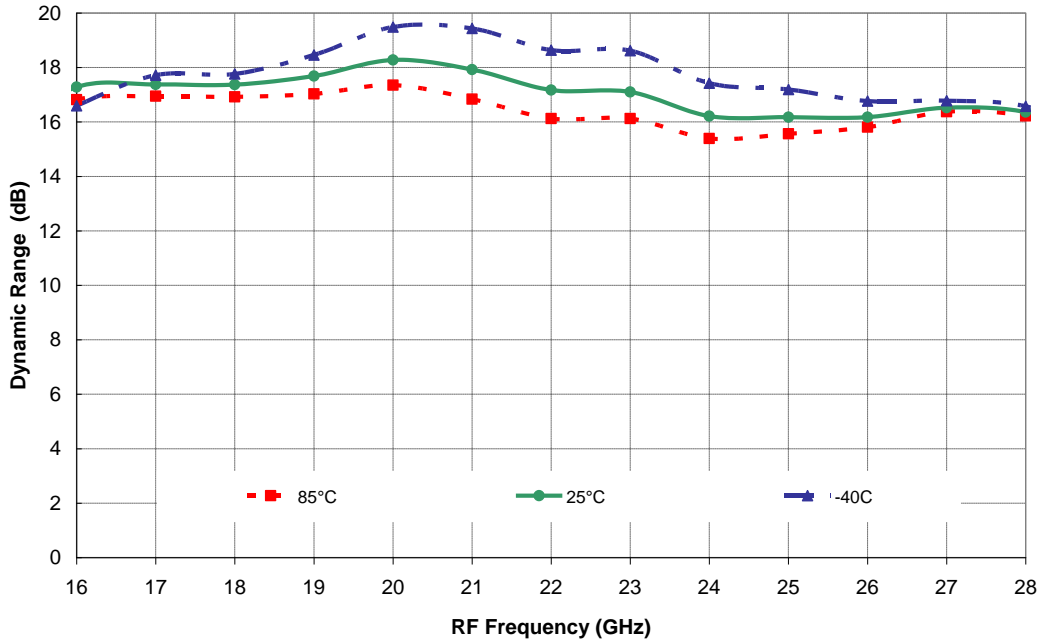
Board losses de-embedded (result given on package access planes)



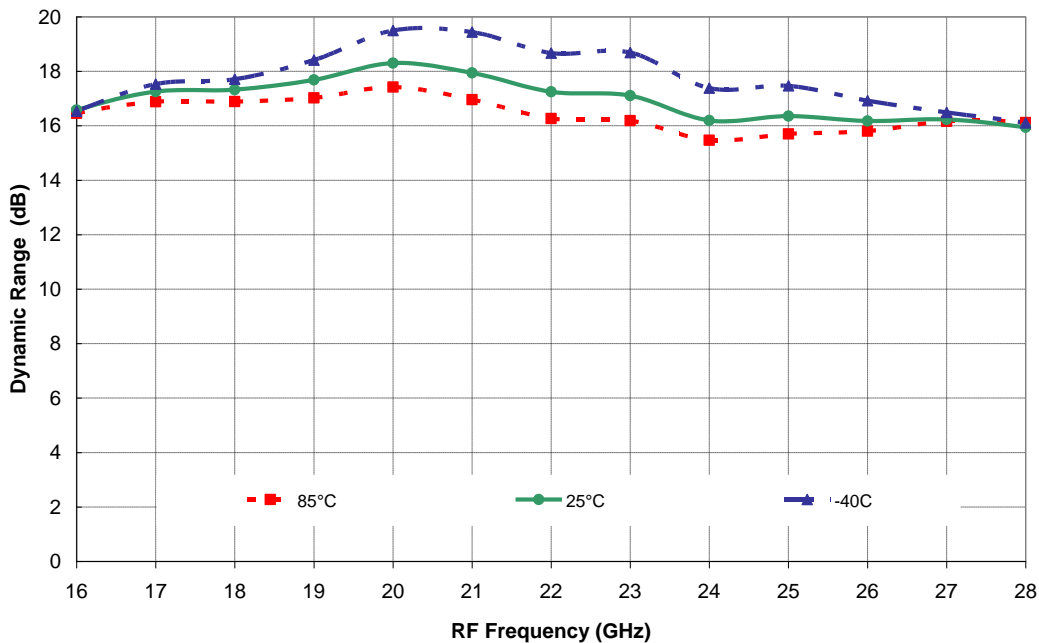
## Temperature Board Measurements

T = [-40, +25, 85] °C, VD = VDL = 4.0V, VGL = -0.6V, VGM = -0.7V, P\_LO = 0 dBm

**Dynamic Range (G<sub>cmax</sub> – G<sub>cmin</sub>) in Supradyn Mode versus Frequency**  
 $F_{RF} = 2 \times F_{LO} + F_{IF}$ ,  $F_{IF} = 2.0\text{GHz}$



**Dynamic Range (G<sub>cmax</sub> – G<sub>cmin</sub>) in Infradyne Mode versus Frequency**  
 $F_{RF} = 2 \times F_{LO} - F_{IF}$ ,  $F_{IF} = 2.0\text{GHz}$



Temperature Board Measurements

T = [-40, +25, 85] °C, VD = VDL = 4.0V, VGL = -0.6V, VGM = -0.7V, P\_LO = 0 dBm

Image Rejection on Supradyne Mode versus Frequency  
F\_IF = 2.0GHz, GCx = -1.5V

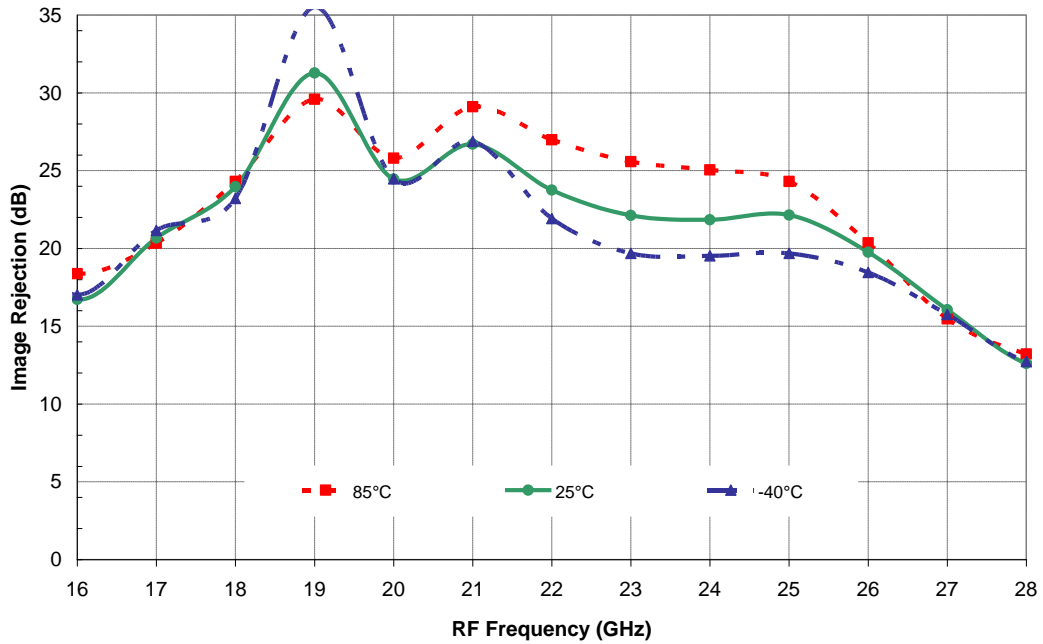
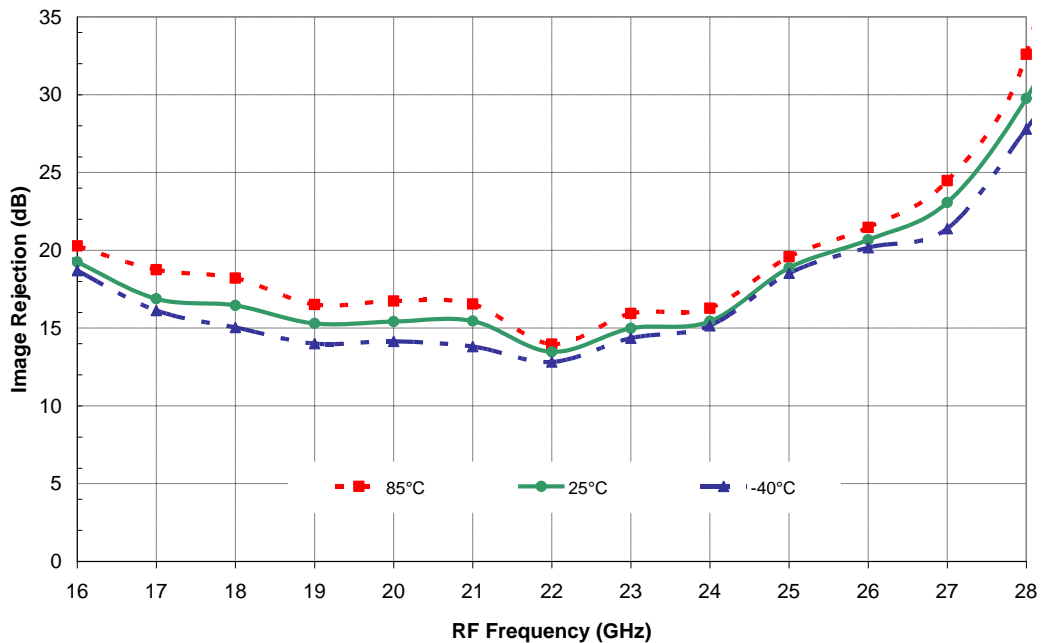


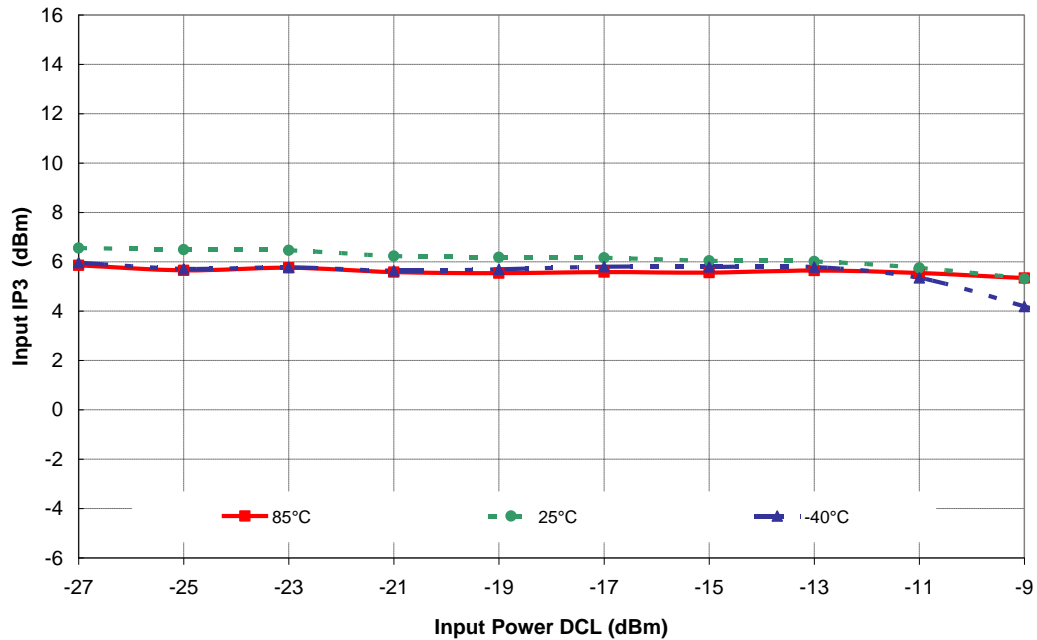
Image Rejection on Infradyne Mode versus Frequency  
F\_IF = 2.0GHz, GCx = -1.5V



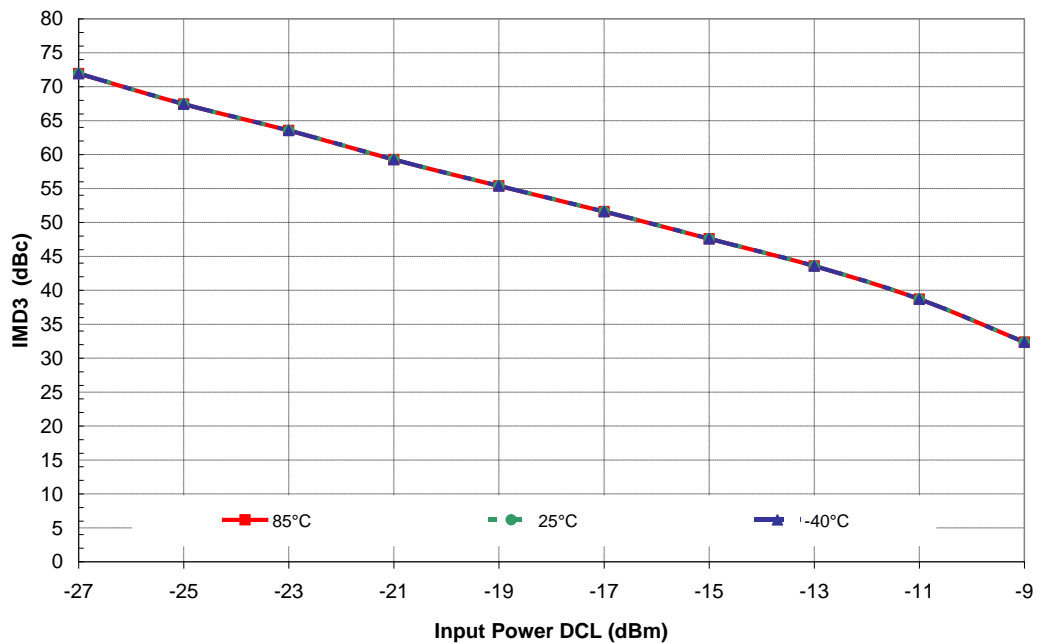
## Temperature Board Measurements

T = [-40, +25, 85] °C, VD = VDL = 4.0V, VGL = -0.6V, VGM = -0.7V, P\_LO = 0 dBm

**Input IP3 versus Temperature at GCx = -1.5V**  
 F\_RF = 2xF\_LO+F\_IF, F\_RF = 20.5GHz, F\_IF = 3.5GHz

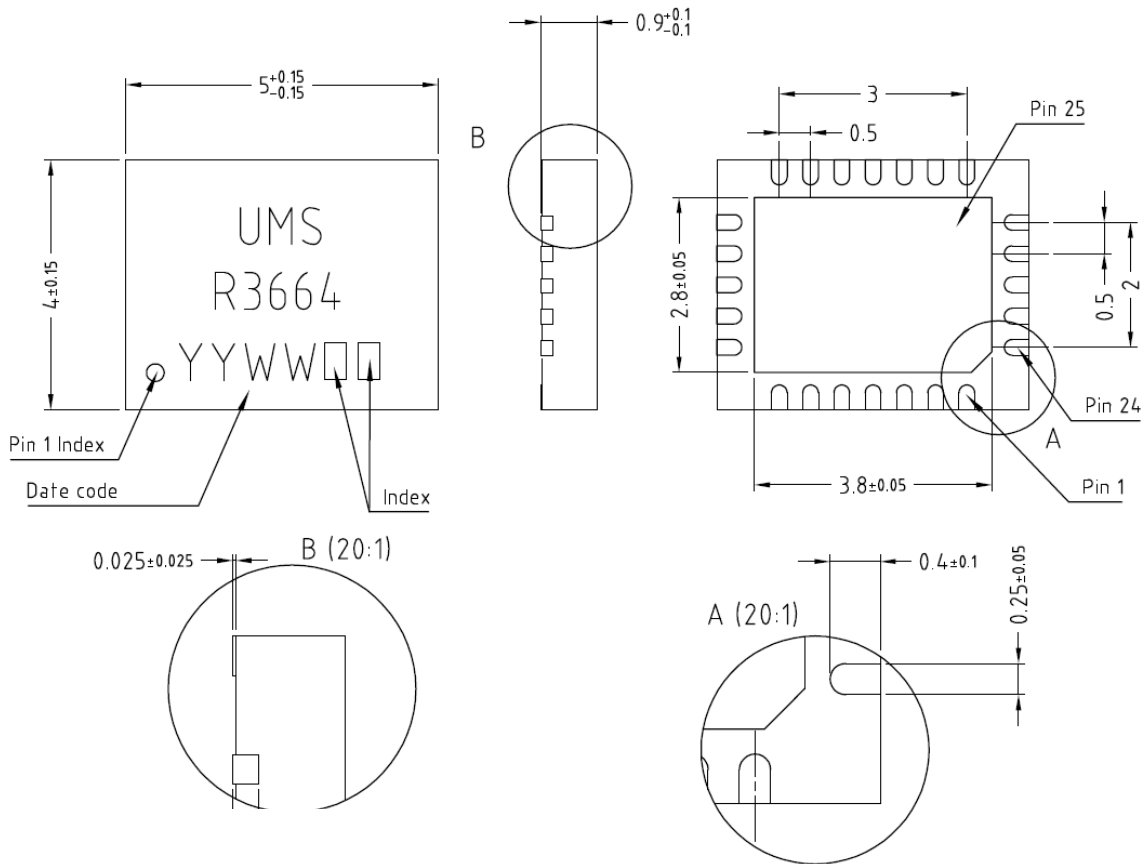


**IMD3 versus Temperature at GCx = -1.5V**  
 F\_RF = 2xF\_LO+F\_IF, F\_RF = 20.5GHz, F\_IF = 3.5GHz





Package outline <sup>(1)</sup>



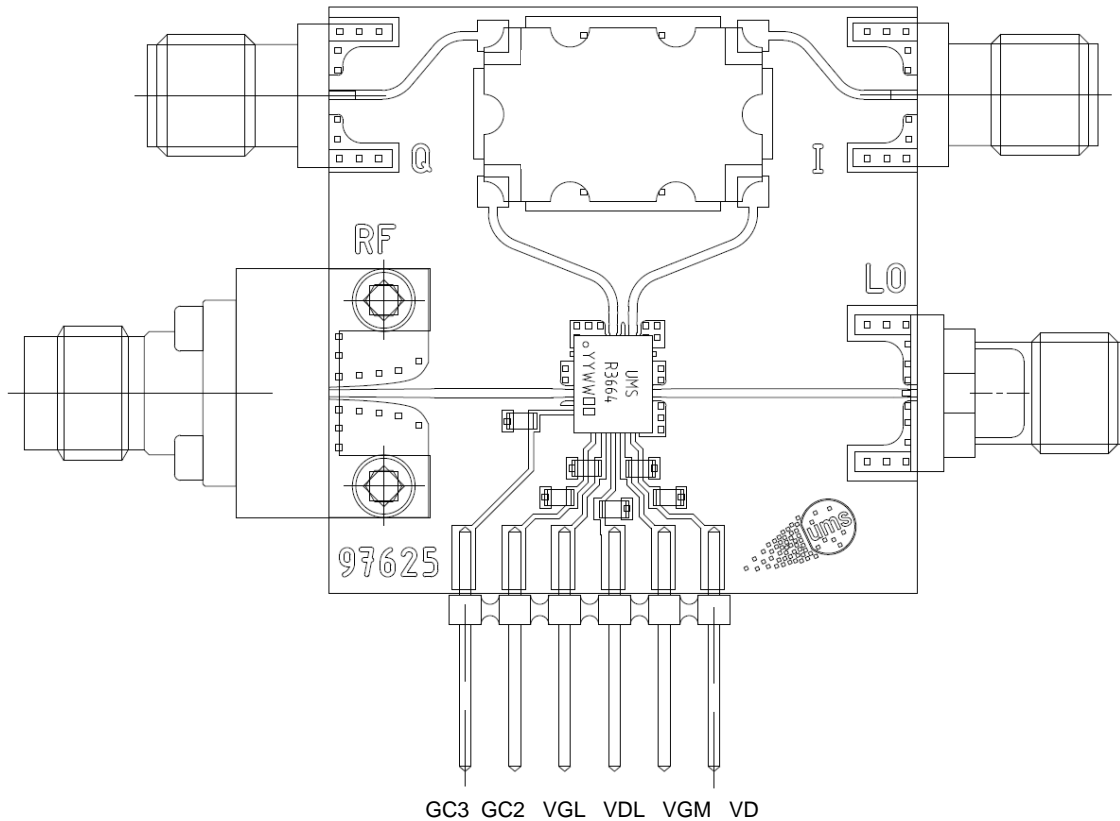
Matt tin, Lead Free	(Green)	1- Nc	9- VGL	17- Nc
Units :	mm	2- Nc	10- VDL	18- Nc
From the standard :	JEDEC MO-220 (VGGD)	3- Nc	11- VGM	19- Nc
		4- GND <sup>(2)</sup>	12- VD	20- IF_I out
	25- GND	5- RF in	13- Nc	21- GND <sup>(2)</sup>
		6- GND <sup>(2)</sup>	14- GND <sup>(2)</sup>	22- IF_Q out
		7- GC3	15- LO in	23- Nc
		8- GC2	16- GND <sup>(2)</sup>	24- Nc

<sup>(1)</sup> The package outline drawing included to this data-sheet is given for indication. Refer to the application note AN0017 (<http://www.ums-gaas.com>) for exact package dimensions.

<sup>(2)</sup> It is strongly recommended to ground all pins marked “Gnd” through the PCB board. Ensure that the PCB board is designed to provide the best possible ground to the package.

## Evaluation mother board

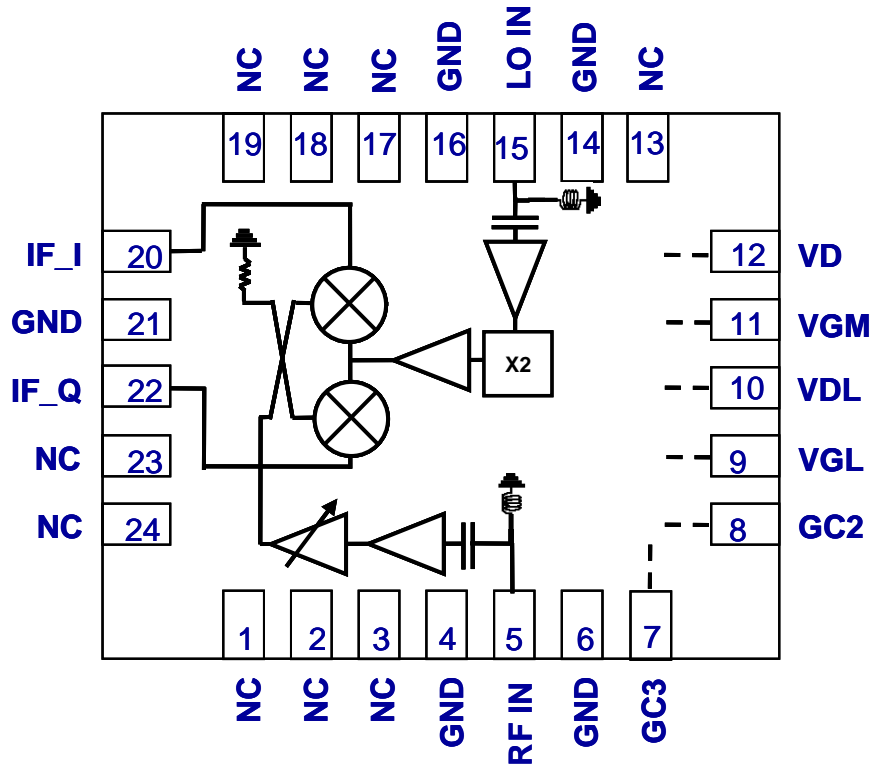
- Compatible with the proposed footprint.
- Based on typically Ro4003 / 8mils or equivalent.
- Using a micro-strip to coplanar transition to access the package.
- Recommended for the implementation of this product on a module board.
- Decoupling capacitors of 10nF  $\pm$ 10% are recommended for all DC accesses.
- See application note AN0017 for details.



Decoupling Capacitors = 10nF  
Hybrid coupler 90° 2-4GHz

**Notes**

Due to ESD protection circuits on RF and LO inputs, an external capacitance might be requested to isolate the product from external voltage that could be present on these accesses in the application.

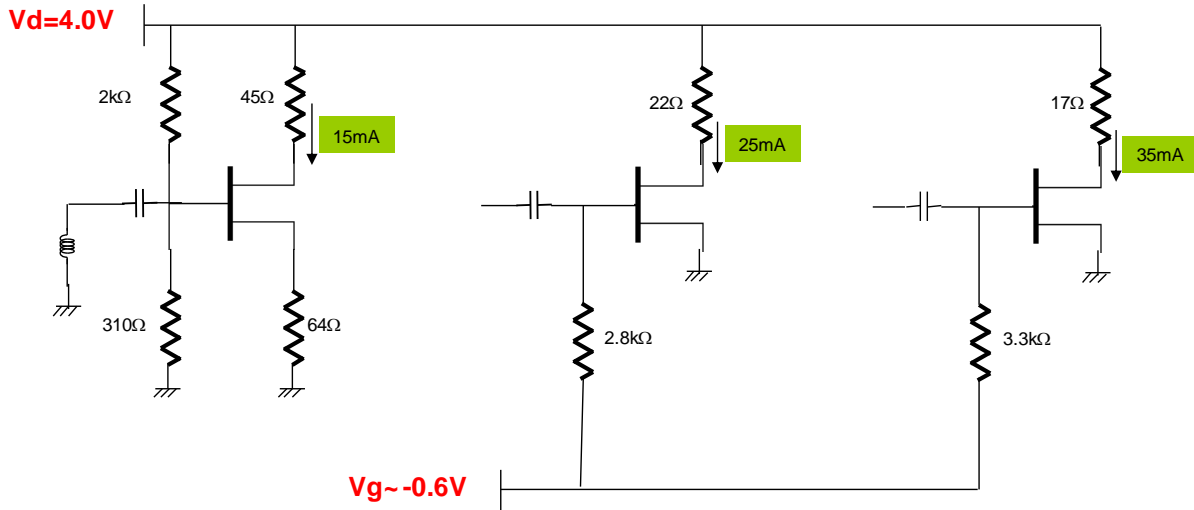


ESD protections are implemented on gate accesses.

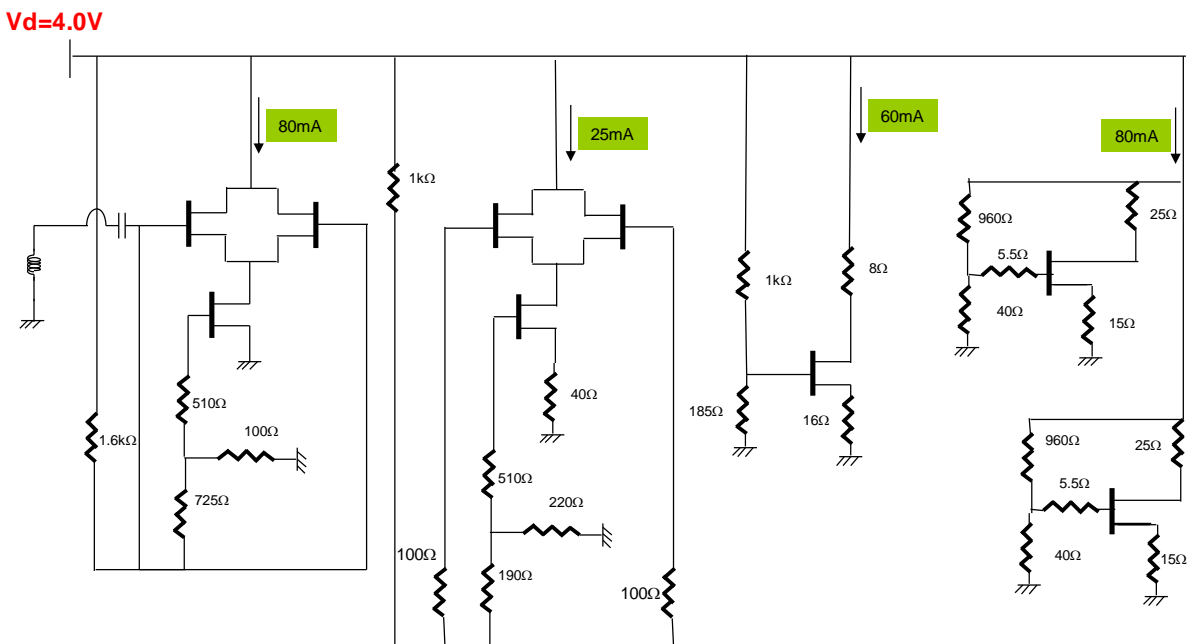
The DC connections do not include any decoupling capacitor in package, therefore it is mandatory to provide a good external DC decoupling on the PC board, as close as possible to the package.

## DC Schematic

### LNA (4.0V, 75mA)



### LO Buffer (4.0V, 245mA)



## Biasing Options

In order to improve the conversion gain and the noise figure, the biasing could be tuned. VGL voltage allows controlling IDL current.

Table below gives the typical value for main characteristics

	<b>VD=VDL= 4.0V IDL= 75mA</b>	<b>VD=VDL= 4.5V IDL= 110mA</b>
Conversion Gain@min. att. (dB)	12	13
Noise Figure@ min. att. from 17 to 24GHz (dB)	3.3	3.2
Input IP3@min. att. (dBm)	+3	+2
VGL (V)	-0.6	-0.4
ID (mA)	245	250
ID + IDL (mA)	320	360
Total DC power consumption (mW)	1280	1620

## Recommended package footprint

Refer to the application note AN0017 available at <http://www.ums-gaas.com> for package footprint recommendations.

## SMD mounting procedure

For the mounting process standard techniques involving solder paste and a suitable reflow process can be used. For further details, see application note AN0017.

## Recommended environmental management

Refer to the application note AN0019 available at <http://www.ums-gaas.com> for environmental data on UMS package products.

## Recommended ESD management

Refer to the application note AN0020 available at <http://www.ums-gaas.com> for ESD sensitivity and handling recommendations for the UMS package products.

## Ordering Information

QFN 4x5 RoHS compliant package:

CHR3664-QEG/XY

Stick: XY = 20

Tape & reel: XY = 21

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