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GreenChip TEA1731(L)TS fixed frequency flyback controller

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Document information

Info	Content
Keywords	GreenChip, TEA1731(L)TS, SMPS, flyback, adapter, notebook, LCD monitor
Abstract	The TEA1731(L)TS is a low-cost member of the GreenChip family in a very small package. It is a fixed-frequency flyback controller intended for power supplies up to 75 W for applications such as notebooks, printers and LCD monitors.

Revision history

Rev	Date	Description
v.1	20120412	first issue

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1. General description

The TEA1731(L)TS is a fixed-frequency flyback controller that can be used for Discontinuous Conduction Mode (DCM) and Continuous Conduction Mode (CCM). Despite the very small TSOP6 package it almost has the full functionality of the TEA1738 series.

1.1 Scope

This application note describes the functionality of the TEA1731(L)TS series. Fixed-frequency flyback fundamentals and calculation of transformer and other large signal parts are not dealt with in this document.

1.2 Features

- SMPS controller IC enabling low-cost applications
- Small low-cost TSOP6 package
- Large input voltage range (12 V to 30 V, 35 V peak allowed for 100 ms)
- Very low supply current during start and restart (10 μA typical)
- Low supply current during normal operation (580 μA typical at no load)
- Overpower compensation (high/low line compensation)
- 60 ms overpower time-out
- Overpower restart timer for low average input power at overload
- Fixed frequency with frequency jitter to reduce ElectroMagnetic Interference (EMI)
- Frequency reduction with fixed minimum peak current at low-power operation to maintain high efficiency at low output power levels
- Frequency increase during peak power (for more output power from same core)
- Slope compensation for CCM operation
- Low and adjustable OverCurrent Protection (OCP) trip level
- Adjustable soft start
- Two independent general-purpose protection inputs combined on a single pin; for example, for OverTemperature Protection (OTP) and output OverVoltage Protection (OVP)
- Internal overvoltage protection; triggers latched protection mode if pin VCC exceeds 30 V
- Internal OverTemperature Protection (OTP)

1.3 Applications

The TEA1731(L)TS is intended for applications that require an efficient and cost-effective power supply solution up to 75 W:

- Notebook
- LCD monitors
- Printers

1.4 Differences between the TEA1731 and the TEA1738 series

- Smaller package (TSOP6):
- Pin VINSENSE has been removed. The functionality has been partly integrated:
  - Maximum duty cycle protection serves as brownout protection
  - Overpower protection obtains its input voltage information by measuring dV/dt on pin ISENSE (NXP patent: 81421271EP01
- Pin OPTIMER has been removed. The functionality has been integrated:
  - Internal 60 ms overpower time-out; external timing components no longer required
  - Internal restart timer; extra external components for time constant no longer required
- Increased rating of the VCC clamp (1 mA instead of 730 μA)
- Extra filtering on latched protections:
  - Latched protection can only be triggered if a fault condition lasts at least four consecutive switching cycles
  - Low-pass filtering provides immunity against high-frequency signals, for example, from mobile phones
- Improved power control curves (switching frequency and peak current as functions of CTRL voltage) for high efficiency at low load as in TEA1738 series. But lower gain variation over the control range improving the stability
- Maximum duty cycle protection modified:

  In the TEA1738 series, the maximum on-time protection is only active during peak power conditions (V_{ISENSE} > 400 mV). This restriction has been removed because of the new frequency control implementation

1.5 Differences between the TEA1731 and the TEA1733 series

- Smaller package (TSOP6):
- Pin VINSENSE has been removed. The functionality has been partly integrated:
  - Maximum duty cycle protection serves as brownout protection
  - Overpower protection obtains its input voltage information by measuring dV/dt on pin ISENSE
  - The mains OVP function does not exist anymore in the TEA1731(L)TS
- Pin OPTIMER has been removed. The functionality has been integrated:
  - Internal 60 ms overpower time-out; external timing components no longer required
  - Internal restart timer; extra external components for time constant no longer required
- Internal OverVoltage Protection (OVP) added; triggers latched protection mode if pin VCC exceeds 30 V
- Increased rating of the VCC clamp (1 mA instead of 240 μA)
- Extra filtering on latched protections:
  - Latched protection can only be triggered if a fault condition lasts at least four consecutive switching cycles

  - Low-pass filtering provides immunity against high-frequency signals; for example, from mobile phones
- Maximum duty cycle protection added, ensuring a well-defined restart at mains dip and serving as brownout protection
- Improved power control curves. Switching frequency and peak current as functions of CTRL voltage for high efficiency at low load as in TEA1738 series. But lower gain variation over the control range improving the stability
- Increased switching frequency during peak load allowing more output power with the same core
- Latch version (TEA1731LTS) only:

  UnderVoltage LockOut (UVLO) has changed to latched protection. This ensures that a shorted output always triggers the latched protection when V_{CC} drops below $V_{th(UVLO)}$ before the overpower protection has a chance to respond.

1.6 Latch and safe restart version

The TEA1731(L)TS is available in a restart version and a latch version. The only difference between the two versions is how the OverPower Protection (OPP) and UnderVoltage LockOut (UVLO) events are handled:

- TEA1731TS: OPP or UVLO event initiates safe restart
- TEA1731LTS: OPP or UVLO event sets the IC to latched off-state

See Section 3.4 for more detailed information about these protection features.

1.7 Application diagram

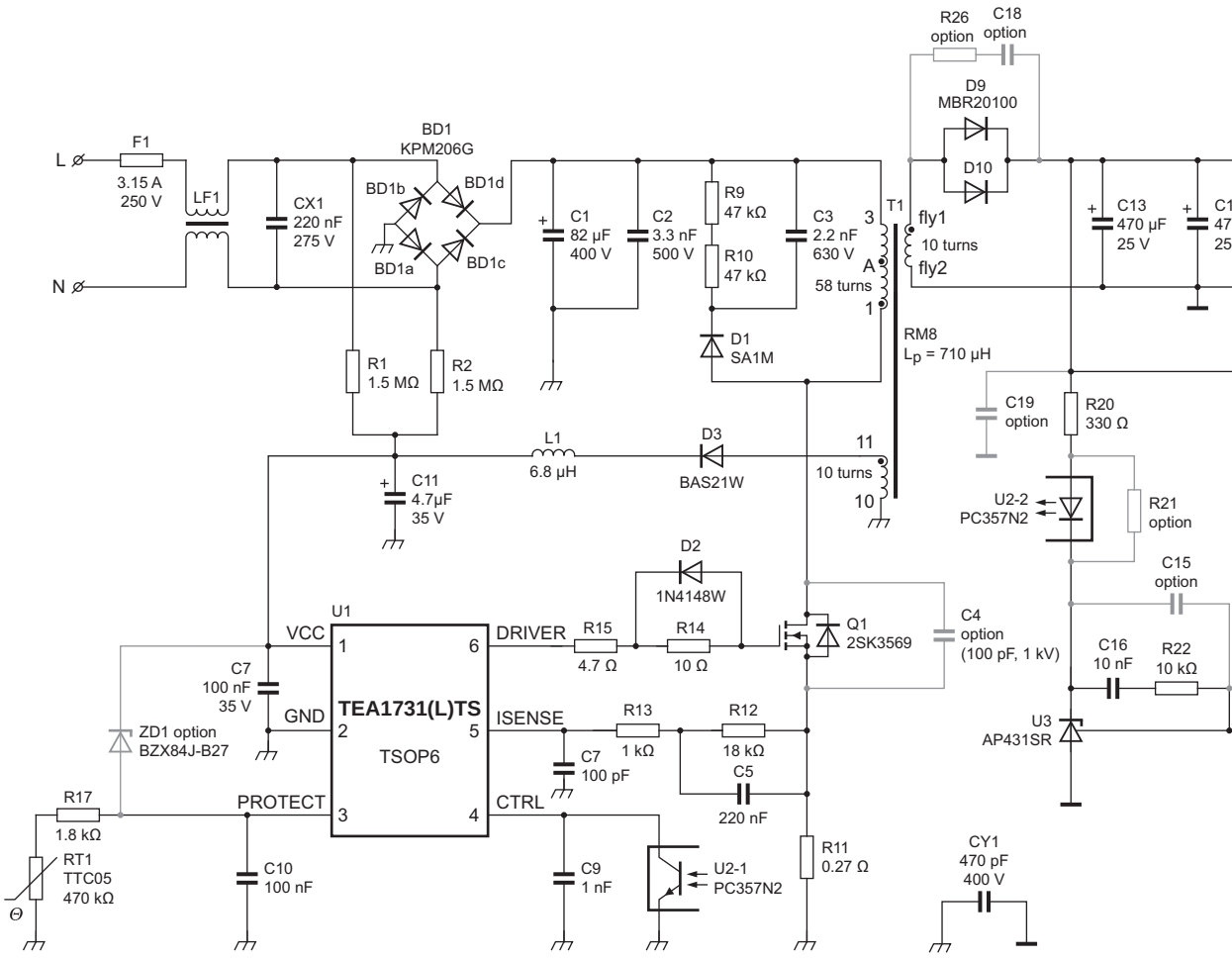


Fig 1. TEA1731(L)TS application diagram

2. Pinning

2.1 Pinning diagram

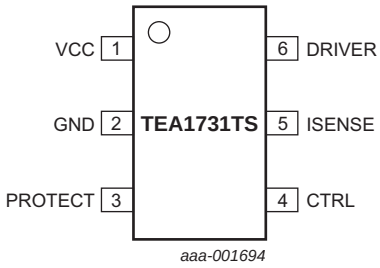


Fig 2. Pinning diagram

2.2 Pin description

Table 1. Pin description

Pin number	Pin name	Description
1	VCC	**Supply voltage** **Start-up:** At mains switch-on, an external start-up circuit (usually a passive resistor network) charges the capacitor connected to this pin. When V_{CC} exceeds $V_{startup}$ (= 21.3 V typical), the IC wakes up from Power-down mode and checks if all other conditions are met to start switching. **Undervoltage lockout:** When the voltage on the pin drops below the 12.5 V (typical; the stop voltage ($V_{th(UVLO)}$)), the IC stops switching and restarts (TEA1731TS) or latches (TEA1731LTS). **Latch reset and clamp:** During latched protection this pin is internally clamped to just above the 4.5 V latch reset voltage ($V_{rst(latch)}$). This enables fast latch reset after unplugging the mains. **Internal overvoltage protection:** An internal OVP sets the IC to latched off-state when the voltage on pin VCC exceeds 30 V (typical) for four consecutive switching cycles. **Absolute maximum rating:** V_{CC} = 30 V (35 V for 100 ms)
2	GND	**Ground**
3	PROTECT	**General-purpose protection input** Two independent protection features can be connected to this pin. An internal current source attempts to keep the pin at 0.65 V. This current source can sink 107 μA and source 32 μA. If more current is required to keep the voltage at 0.65 V, the voltage rises above 0.8 V or drops below 0.5 V for at least four switching cycles, the IC enters the Latched protection mode.

Table 1. Pin description

Pin number	Pin name	Description
4	CTRL	**Power control input** **General:** The voltage on pin CTRL controls both the switching frequency and the peak current. **Input configuration:** The input is internally connected to 5.4 V via a 7 kΩ resistor. **Range:** The active range of pin CTRL is from 1.2 V (no load) to 3.9 V (maximum peak load).
5	ISENSE	**Current sense input** **General:** This pin senses the primary coil current across an external resistor. It compares this coil current to an internal control voltage which is proportional to the voltage on pin CTRL. **Overpower protection:** When the internal control voltage exceeds 400 mV, the overpower timer is started. When this condition lasts longer than 60 ms, the IC triggers a long restart (TEA1731TS) or enters the Latched protection mode (TEA1731LTS). **Overcurrent protection:** The internal control voltage is limited to 500 mV, which limits the primary peak current and thus the input power. **Leading-edge blanking:** The first 325 ns of each switching cycle, the ISENSE input is internally blanked to prevent that spikes, due to parasitic capacitance, prematurely trigger the peak current comparator. **Propagation delay:** The delay time from detecting the level to actually switching off the driver is approximately 146 ns. **Overpower compensation (high/low line compensation):** Integrated overpower compensation senses the dV/dt on pin ISENSE. It compensates the OPP and OCP levels to keep the maximum power equal for high and low mains. **Soft start:** An adjustable soft start function slowly enables the primary peak current to grow. **Slope compensation:** Amount of slope compensation (related to pin ISENSE): 20 mV/μs. The slope compensation is only active at duty cycles higher than 45 %.
6	DRIVER	**Gate driver output for MOSFET** **Driver capability:** The driver can source and sink 0.3 A at 2 V. It can sink 0.75 A at 10 V. **Frequency modulation:** The switching frequency is modulated over a range of ±4 kHz at a rate of 280 Hz to improve EMI behavior.

3. Functional description

3.1 General

The TEA1731(L)TS has been designed for fixed-frequency flyback power supplies.

The TEA1731(L)TS uses peak current control. The output voltage is measured and transferred back via an optocoupler to pin CTRL.

This chapter describes how the controller works. See Section 4 for specific application issues.

3.2 Start-up

3.2.1 Charging the VCC capacitor

A resistor charges capacitor C11 (see Figure 1) on pin VCC to provide the start-up power. When V_{CC} is below $V_{startup}$ (21.3 V typical), the IC current consumption is low (10 μA typical). When the capacitor is charged above $V_{startup}$ (21.3 V typical) and all other conditions have been met, the controller starts to switch. When the supply has started, the TEA1731(L)TS is supplied by the auxiliary winding.

Connect the resistor in front of the bridge rectifier for fast latch reset[1].

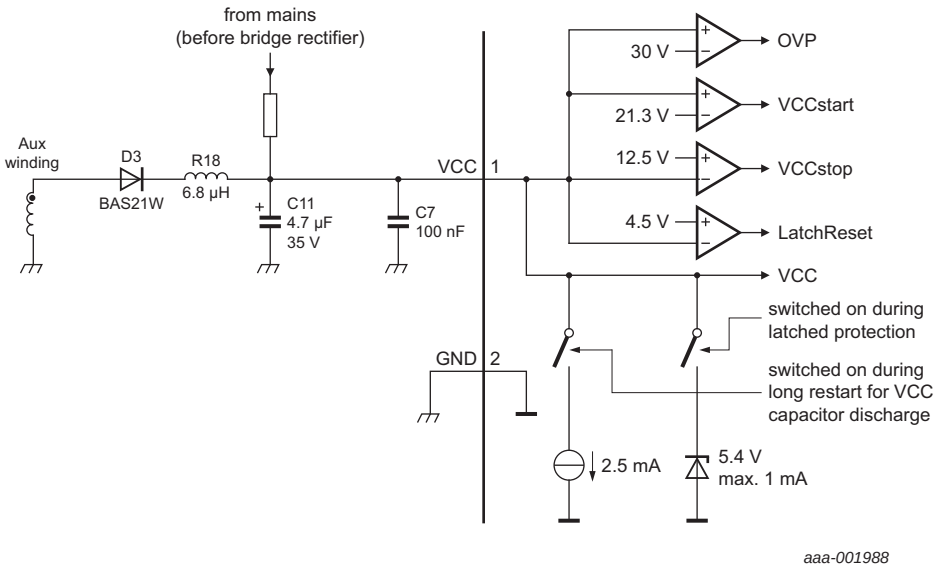


Fig 3. Pin VCC

A low-cost and efficient implementation for the start-up circuit is using two resistors to L and N. This also discharges the X-cap (CX1) after unplugging the mains (see Figure 1). See Section 5 for more information about start-up circuits.

1. The only way to reset the latched protection is to bring pin VCC below 5 V. During latched protection, the supply current is only 10 μA. If the start-up resistor is connected after the bridge rectifier, the bulk capacitor continues to feed it for a long time after unplugging the mains.

3.2.2 Start-up conditions

When pin VCC reaches $V_{startup}$ (21.3 V typical), the controller wakes up from Power-down mode and checks if the PROTECT voltage exceeds 0.5 V. If not, the controller does not switch. Due to the increased power consumption when the IC is switched on, the voltage on pin VCC eventually drops to below $V_{th(UVLO)}$ and the IC enters Power-down mode. The start-up circuit charges the VCC capacitor and the cycle repeats itself.

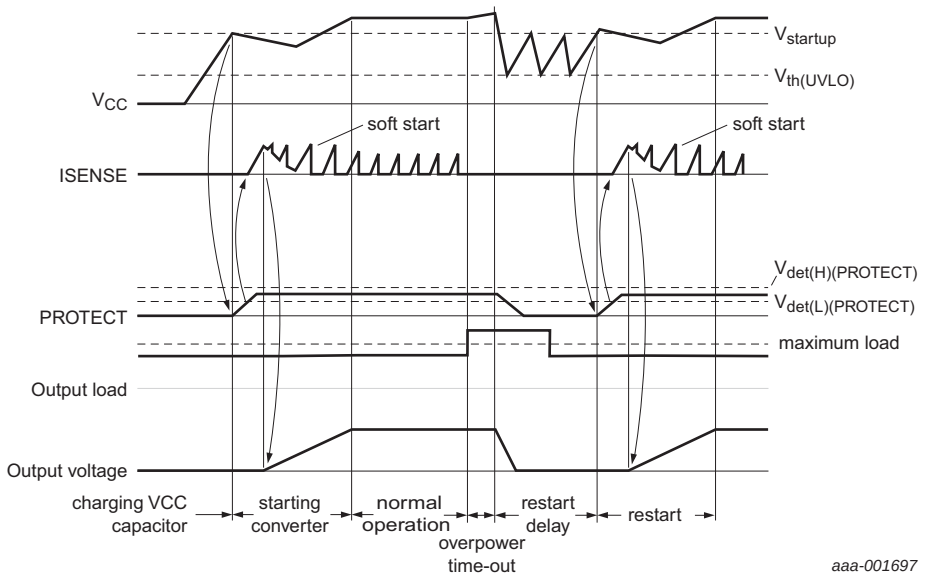


Fig 4. Start-up sequence, normal operation and restart sequence

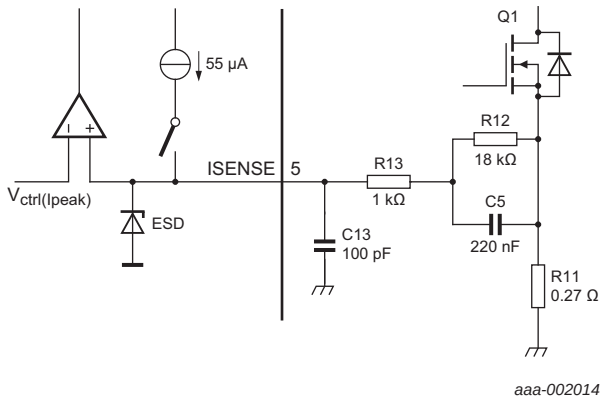
3.2.3 Soft start

When all start-up conditions have been met, the IC charges the soft start capacitor by switching on a 55 μA current source on pin ISENSE. When pin ISENSE reaches the internal control voltage (0.5 V when the output is still low), the current source is switched off and the controller starts to switch.

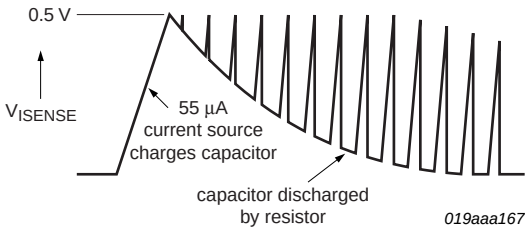
At start-up the output capacitors are still empty and the control input asks for the maximum peak current, increasing the primary duty cycle until V_{ISENSE} reaches 0.5 V[2]. But because of the charged soft start capacitor, the voltage on V_{ISENSE} is already 0.5 V. As the soft start resistor discharges the soft start capacitor, the peak current slowly increases.

The purpose of the soft start feature is to avoid audible noise at start-up. Increasing the peak current instantly from 0 A to maximum is audible. A soft start period of 4 ms is a good value for most applications.

2. The voltage to which the soft start capacitor is charged is not fixed to 0.5 V but depends on the voltage on pin CTRL. See Figure 8 for the relationship between V_{CTRL} and V_{ISENSE}. For standard applications the CTRL voltage clips to 5.4 V during start-up. The soft start capacitor is then charged to 0.5 V. Check if the CTRL voltage is always high during start-up when using non-standard applications.



a. Soft start circuit



b. Soft start waveform

Fig 5. Soft start circuit and waveform

The purpose of the extra series resistor R13 and capacitor C13 is to filter out negative spikes. Otherwise, the internal ElectroStatic Discharge (ESD) protection diode must rectify these spikes, which charge capacitor C5 and cause a positive offset voltage on pin ISENSE.

At high input voltages, the peak current can show a short peak at start-up. The empty output capacitors behave like a short circuit. The supply immediately enters Continuous conduction mode. During this peak, the minimum on-time limits the power.

3.2.4 Clamp

The 5.4 V clamp on pin VCC is only active during the latched off-state. The purpose of this clamp is to keep pin VCC just above the 4.5 V latch reset level. This ensures a fast latch reset after unplugging the mains.

3.3 Power control

3.3.1 General

Pin CTRL controls the amount of output power. This is done by changing both the peak current and the switching frequency (see Figure 6).

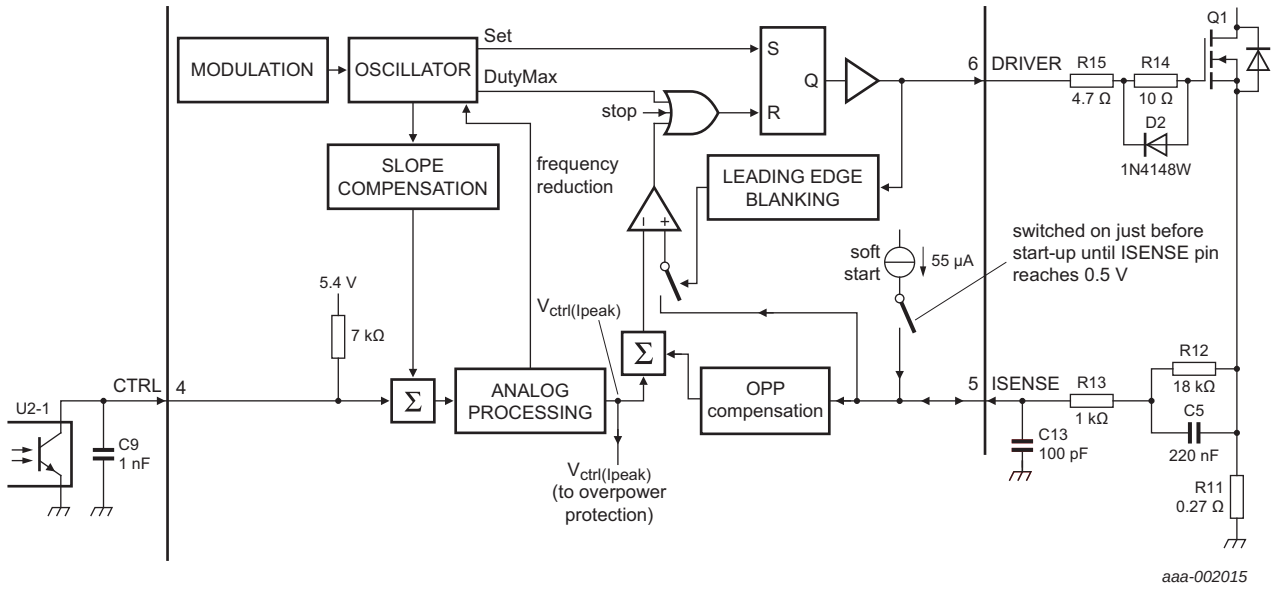


Fig 6. Pin CTRL, pin ISENSE and pin DRIVER

3.3.2 Input biasing

An internal 7 kΩ resistor connected to 5.4 V enables direct connection of an optocoupler transistor. External components to convert the output current of the optocoupler to the control voltage are not required. The relationship between the current and the voltage on pin CTRL can be calculated with Equation 1 (see Figure 7).

$$V_{CTRL} = 5.4\ V - 7 \times 10^{3} \times I_{O(CTRL)} \quad (1)$$

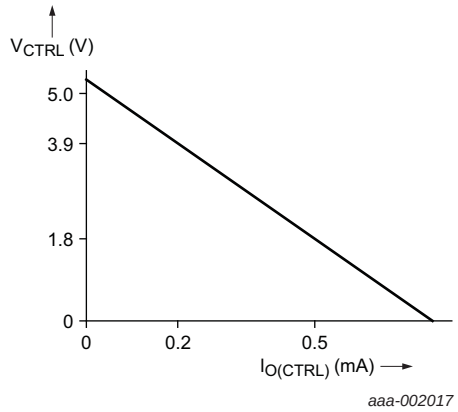


Fig 7. V_{CTRL} as a function of $I_{O(CTRL)}$

3.3.3 Peak current control

Pin CTRL controls the primary peak current. Figure 8 shows the relationship between the voltage and the peak current on pin CTRL.

The DRIVER output is switched on by each oscillator pulse. The voltage on pin CTRL controls the oscillator frequency. It is switched off when the primary peak current measured on pin ISENSE exceeds the peak current set by pin CTRL or if the duty cycle exceeds 80 %.

3.3.4 Frequency control

The voltage on pin CTRL controls the switching frequency. The frequency curve (see Figure 8) can be split into four areas:

- **Peak power**

  At peak power, the switching frequency is increased to 80 kHz to enable a higher output power from the same core. This also increases the switching losses but is irrelevant during temporary peak loads. For the maximum benefit of the frequency increase, the supply must operate (mainly) in DCM (in CCM, the frequency increase does not have much influence).

  Peak power can only be delivered during the 60 ms overpower time-out.

- **High power**

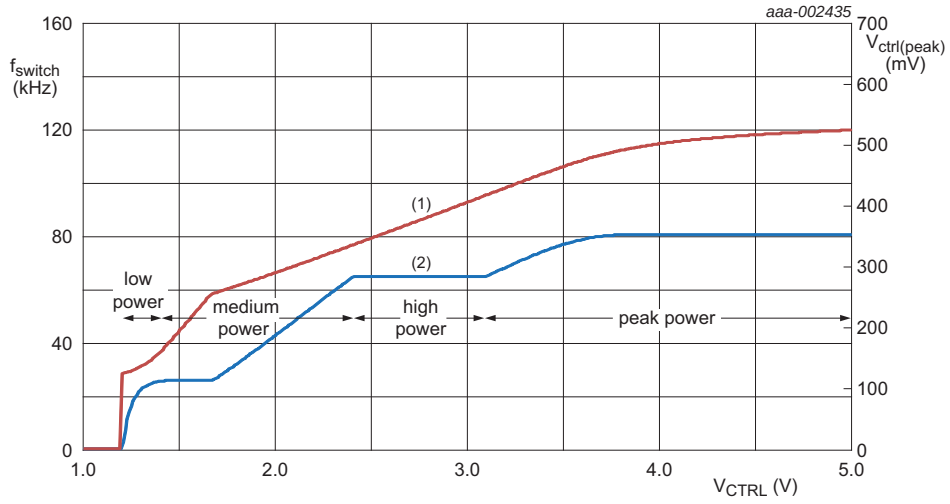
  At high power, the switching frequency is fixed to 65 kHz. Only the peak current is controlled.

- **Medium power**

  At medium power, the switching frequency is first reduced to decrease the switching losses. It is not reduced below 26.5 kHz to prevent audible noise.

- **Low power**

  The peak current is not reduced below 25 % of its maximum value to ensure efficient operation at low output power. Instead, to reduce the output power, the switching frequency is reduced. The frequency now enters the audible spectrum but does not become audible because of the low peak current. This part of the frequency curve is also referred to as Voltage Controlled Oscillator (VCO) mode.



(1) $V_{ctrl(Ipeak)}$

(2) f_{sw}

Fig 8. $V_{ctrl(Ipeak)}$ and f_{sw} as a function of V_{CTRL}

It is important to use the entire pin CTRL input range. If the chosen current sense resistor value is too low, only the lower part of the control curve is used. This means that frequency reduction already starts at a relatively high peak current which can result in audible noise.

3.3.5 Switch-off delay

The primary peak current does not immediately stop when it passes the threshold level because there is some internal and external delay. During this delay, the primary current still continues to grow. The exact increase depends on the delay, the primary inductance and the bulk voltage. The OPP compensation largely compensates this dependency on the bulk voltage.

The switch-off delay can be split into three delays:

- **External filter delay**

  The filter on pin ISENSE (resistor R13 and capacitor C7) also causes delay. This delay approximately equals R × C.

- **Propagation delay**

  The internal delay from passing the threshold level on pin ISENSE to actually switching off pin DRIVER is approximately 146 ns.

- **MOSFET switch-off delay**

  The MOSFET does not immediately switch off when pin DRIVER switches off. The MOSFET switch-off delay is defined as the delay from the moment the voltage on pin DRIVER starts to drop until the drain of the MOSFET reaches the bulk voltage. This must be measured in the application.

3.3.6 Leading-Edge Blanking (LEB)

The ISENSE input is internally blanked for the first 325 ns of each switching cycle. This prevents that spikes caused by parasitic capacitance (gate-source capacitance of the MOSFET and the parasitic capacitance of the transformer) trigger the peak current comparator prematurely.

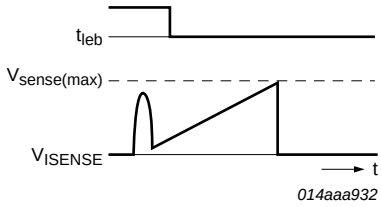


Fig 9. Leading edge blanking

3.4 Overview protections

3.4.1 General

Depending on which protection is triggered and on the version of the IC, the protection causes a safe restart or latches the converter to an off-state. Table 2 shows an overview of the protection features. See Section 3.4.2 and Section 3.4.3 for explanation of safe restart and latched off-state.

Table 2. Protection handling TEA1731(L)TS

Protection	TEA1731TS	TEA1731LTS	Comment
OPP	slow restart	latch	60 ms overpower time-out
maximum duty cycle	restart	restart	8 consecutive switching cycles
OVP (pin PROTECT = HIGH)	latch	latch	4 consecutive switching cycles
OTP (pin PROTECT = LOW)	latch	latch	4 consecutive switching cycles
internal OVP	latch	latch	4 consecutive switching cycles
internal OTP	latch	latch	4 consecutive switching cycles
UVLO	restart	latch	
OCP	cycle-by-cycle	cycle-by-cycle	

3.4.2 Restart protection

3.4.2.1 Regular restart (short)

If one of the protections triggers a restart, the TEA1731(L)TS immediately stops switching and the supply current of the IC quickly discharges the VCC capacitor. When V_{CC} drops below the undervoltage lockout level, the IC enters Power-down mode. The supply current drops to approximately 10 μA and a normal start-up sequence follows.

3.4.2.2 OPP restart (long restart, not in TEA1731LTS)

If the OPP triggers a restart, the regular restart delay is insufficient to keep the average input power below an acceptable level (usually 5 W) in a continuous overload. The TEA1731TS first carries out a regular restart sequence, but instead of starting up when

V_{CC} reaches 21.3 V, it does not wake up from Power-down mode. Instead it discharges the VCC capacitor to 12.5 V again and lets the start-up circuit charge the capacitor. It continues sawing like this between $V_{startup}$ and $V_{th(UVLO)}$ three times before starting up (see Figure 4).

The rising slope of this saw tooth depends on the mains voltage, the start-up circuit and the VCC capacitor. At low input voltage the restart time increases. An internal current source (2.5 mA) determines the falling slope of the saw tooth.

3.4.3 Latch protection

3.4.3.1 Latched off-state

When one of the protection features triggers the latched off-state, the IC immediately stops switching and enters Power-down mode. It clamps pin VCC to 5.4 V, which is just above the reset level (4.5 V).

3.4.3.2 Resetting a latched protection

The voltage on pin VCC must drop below 4.5 V to reset a latched protection. This means that a "power-cycle" of the mains must be done. Unplug the mains, wait a moment and then reconnect the mains.

If a latched protection is triggered, pin VCC is automatically clamped to a voltage just above the reset level. When the mains is unplugged, the start-up current stops and the 10 μA supply current to the TEA1731(L)TS discharges the VCC capacitor. Because the capacitor only is required to discharge from 5.4 V to 4.5 V, it resets quickly.

When capacitor C_{VCC} = 4.7 μF, the discharge time is 0.47 s. In practice, the start-up current does not always immediately stop charging the VCC capacitor after unplugging the mains because the X-cap can still be charged for about one second.

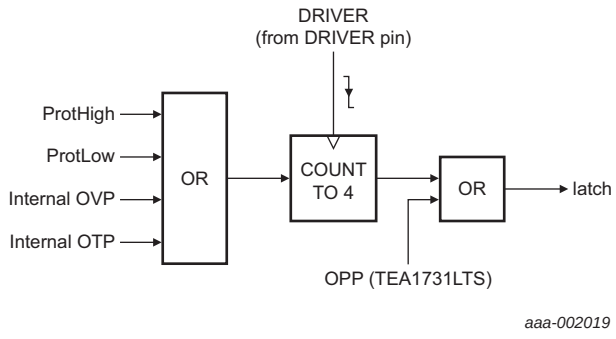


Fig 10. Latched protections

3.4.4 Maximum duty cycle limitation (cycle-by-cycle)

If the peak current measured by pin ISENSE does not reach the peak current set by pin CTRL within a duty cycle of 80 %, the maximum duty cycle limitation ends the driver pulse. In low-power mode where the switching frequency is reduced below 26 kHz, the 80 % duty cycle limitation changes into a 30 μs on-time limitation.

3.4.5 Maximum duty cycle protection (brownout protection)

3.4.5.1 Purpose

The main purpose of the maximum duty cycle protection is to ensure a well-defined response to mains supply dips. However, it can also serve as a brownout protection.

3.4.5.2 Implementation

If the peak current measured by pin ISENSE does not reach the peak current set by pin CTRL within a duty cycle of 80 %, the maximum duty cycle limitation ends the driver pulse. If this happens during eight consecutive cycles, the maximum duty cycle protection triggers a restart. In low-power mode where the switching frequency is reduced to below 26 kHz, the maximum duty cycle protection changes to a maximum on-time protection. The maximum on-time is 30 μs (typical).

3.4.5.3 Brownout

When the mains voltage is too low and at full load, the primary current increases, causing increased losses in many of the primary components. The purpose of the brownout protection is to protect the supply against overheating at input voltages that are too low.

The TEA1731(L)TS has no input voltage sensing pin, but the maximum duty cycle protection serves as a kind of brownout protection. At low input voltage (and significant load), the duty cycle becomes an indicator for the input voltage. When the duty cycle reaches 80 %, the IC triggers a restart. At very low input voltages, the start-up circuit cannot provide enough current to charge the VCC capacitor to $V_{startup}$ again.

3.4.6 Internal OverTemperature Protection (OTP)

When the temperature in the chip exceeds 140 °C, the internal OTP sets the controller to the latched off-state (in all TEA1731 versions).

3.4.7 OverPower Protection (OPP)

When the rated output power is continuously exceeded for an adjustable duration, the OPP is activated. The controller immediately stops switching and performs a safe restart (TEA1731TS) or enters the latched-off state (TEA1731LTS). See Section 3.5 for more information about overpower protection.

3.4.8 Internal output OverVoltage Protection (OVP)

An internal overvoltage protection sets the IC to latched-off state when the voltage on pin VCC exceeds 30 V for four consecutive switching cycles. The internal OVP measures on the falling edge of the DRIVER signal.

It is also possible to implement an external OVP with a lower threshold value by adding a circuit to pin PROTECT, for example, a Zener diode from pin VCC to pin PROTECT.

3.4.9 External output OverVoltage Protection (OVP)

The purpose of the overvoltage protection is to protect the devices connected to the output. It also protects the supply itself against output voltages that are too high, for example, when the voltage feedback loop is disturbed.

If an overvoltage at the output occurs, the application pulls pin PROTECT above 0.8 V and the OVP is activated. The controller immediately stops switching and enters the latched-off state (in all TEA1731 versions). See Section 4.5 for more information on applying pin PROTECT.

Connection of an external OVP application is only required if the threshold voltage must be lower than 30 V or extra filtering is required. Without external OVP application, the fixed internal OVP latches the IC when the voltage on pin VCC exceeds 30 V.

3.4.10 External OverTemperature Protection (OTP)

When the temperature in the supply exceeds the rated level, the application pulls pin PROTECT below 0.5 V and the OTP is activated. The controller immediately stops switching and enters the latched-off state (in all TEA1731 versions). See Section 4.5 for how to apply pin PROTECT.

3.4.11 UnderVoltage LockOut (UVLO)

3.4.11.1 Restart version (TEA1731TS)

When during normal operation the voltage on pin VCC drops below the undervoltage lockout threshold ($V_{th(UVLO)}$ = 12.5 V typical), the IC stops switching and enters Power-down mode. The start-up circuit charges the VCC capacitor and a normal start-up sequence follows.

3.4.11.2 Latch version (TEA1731LTS)

When during normal operation VCC drops below the undervoltage lockout threshold, the IC is set to the Latched protection mode. This ensures that a shorted output always triggers the Latched protection mode, including if V_{CC} drops below $V_{th(UVLO)}$ before the OPP has a chance to respond.

3.4.12 OverCurrent Protection (OCP)

See Section 3.5 for more information about overcurrent protection. See Section 4.4 for more information about configuring the OCP.

3.5 Overpower protection and overcurrent protection

3.5.1 Continuous and temporary output power limitation

The TEA1731(L)TS incorporates two mechanisms to protect against overload:

- **Overpower protection**

  Overpower protection performs a safe restart or enters the Latched protection mode in the latched version if the rated power is continuously exceeded. OPP is delayed by 60 ms to allow temporary overloads.

- **Cycle-by-cycle primary inductor current limitation**

  Peak current limitation prevents that the core enters saturation and as a consequence the MOSFET from currents that are too high.

3.5.2 How OPP operates

When the internal control voltage exceeds the overpower threshold (400 mV on pin ISENSE), the internal overpower timer is activated (See Figure 11 and Figure 12).

- If the overpower condition lasts long enough for the timer to reach 60 ms, the controller carries out an OPP restart (TEA1731TS) or enters Latched protection mode (TEA1731LTS).
- If the internal control voltage drops below 400 mV again before the timer reaches 60 ms, the counter is immediately reset.

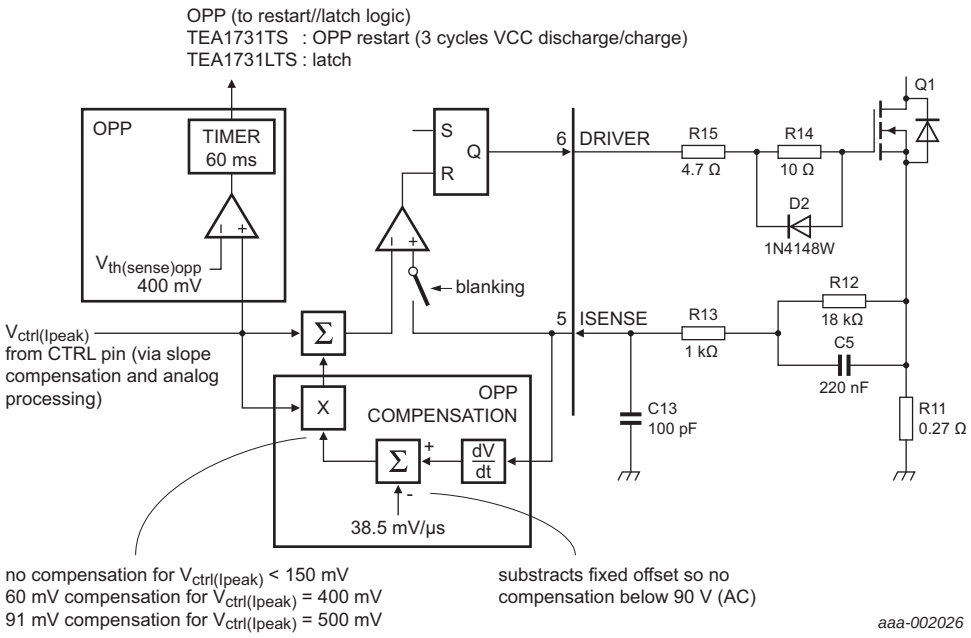


Fig 11. Overpower protection and compensation

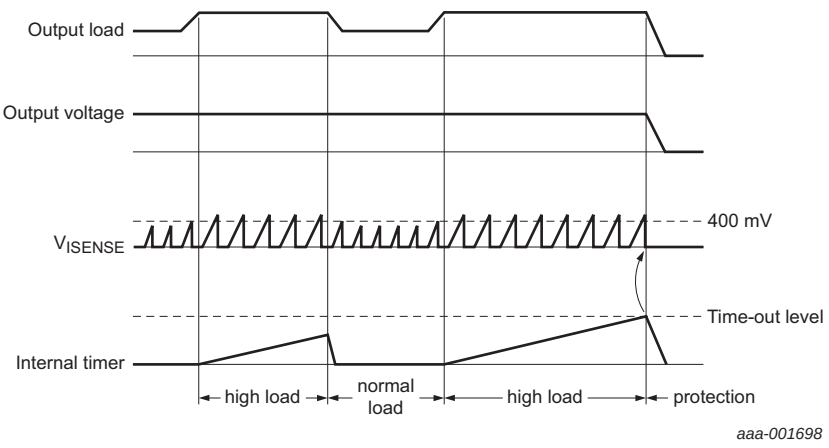


Fig 12. Overpower time-out

3.5.3 Peak current limitation (OCP)

When the voltage on pin ISENSE exceeds 500 mV, the current switching cycle is immediately ended. When the OCP limits the peak current, the output voltage can no longer be maintained. The converter continues to switch until the OPP is triggered or until V_{CC} has dropped below $V_{th(UVLO)}$.

3.5.4 Input voltage compensation

3.5.4.1 Purpose

In fixed-frequency DCM, the peak current limitation can also act as overpower protection because the maximum output power is independent of the input voltage. In fixed-frequency CCM, the maximum amount of power that can be transferred to the output not only depends on the primary peak current. It also depends on the duty cycle and therefore on the input voltage as well.

3.5.4.2 Implementation

TEA1731(L)TS has built-in input voltage compensation to ensure accurate overpower protection, independent of the input voltage.

TEA1731(L)TS has no dedicated pin for sensing the input voltage, so it has another way to sense the input voltage. The rising slope of the current through the primary winding is proportional to the input voltage. Pin ISENSE not only measures the primary current but also determines its slope (see Figure 11).

The relationship between the dV/dt slope on pin ISENSE and the resulting compensation on the internal control voltage ($V_{ctrl(Ipeak)}$) is shown in Figure 13. the internal control voltage controls the gain of the compensation.

- **Low load**

  At low load ($V_{ctrl(Ipeak)}$ below 150 mV), no compensation is done, ensuring that the low-load efficiency is not affected by decreasing the minimum $V_{ctrl(Ipeak)}$ (125 mV). Imagine a third, horizontal line at any level below 150 mV in Figure 13.

- **Maximum continuous load**

  Around the threshold of the overpower protection ($V_{ctrl(Ipeak)}$ = 400 mV), the compensation has been optimized for equal power at low and high mains. $V_{ctrl(Ipeak)}$ is reduced from 400 mV at low-bulk voltage to 340 mV at high-bulk voltage to achieve this.

- **Maximum peak load**

  During temporary peak loads, more compensation is required to make the peak power independent of the input voltage. At the highest expected bulk voltage, the maximum $V_{ctrl(Ipeak)}$ is reduced from 500 mV to 409 mV.

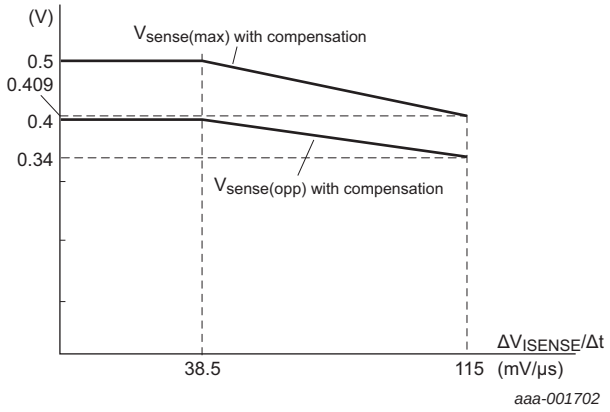


Fig 13. Overpower compensation: $V_{th(sense)opp}$ as function of dV/dt on pin ISENSE

Although the compensation is fixed, overcompensation can (within certain limits) be corrected by adding capacitance on pin ISENSE (see Section 4.4.3).

Figure 14 shows the power at which the OPP triggers as a function of the mains voltage measured in an application with 650 μH inductance, a 0.21 Ω current sense resistor and a 220 pF capacitor on ISENSE.

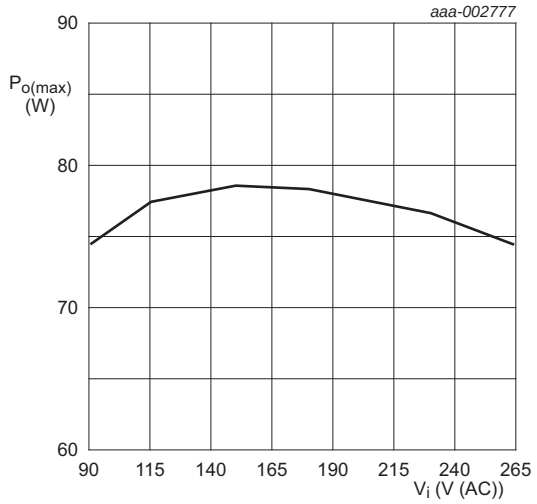


Fig 14. Maximum continuous output power as a function of mains voltage

Figure 15 shows the power at which the OCP starts to limit the peak output power as a function of the mains voltage. Measured in the same application as in Figure 14 but with continuous load of 1 A with 50 ms peaks. At each mains voltage setting, the peak load is slowly increased until the output voltage starts to drop.

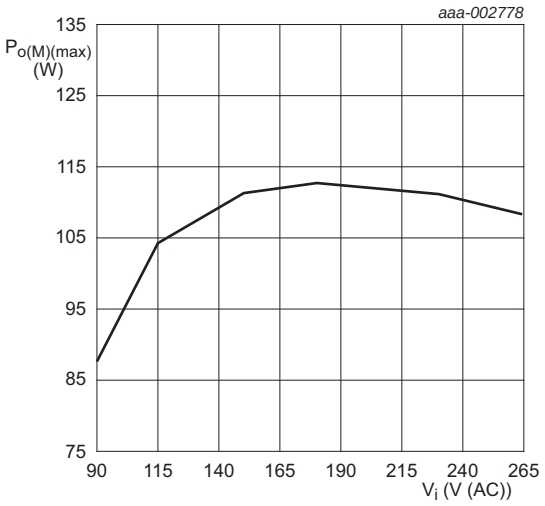


Fig 15. Maximum peak output power as a function of mains voltage

3.5.5 Overpower time-out

When the internal control voltage exceeds the overpower threshold of 400 mV, the overpower timer is activated (see Figure 12). An internal counter is started.

When the overpower condition lasts long enough for the counter to reach 60 ms, the controller carries out a safe restart procedure (or enters Latched protection mode in the latched version). If the internal control voltage drops below 400 mV before the counter reaches 60 ms, the counter is immediately reset.

3.5.6 Restart delay (TEA1731TS only)

When the OPP triggers a safe restart procedure, the TEA1731TS immediately stops switching, discharges V_{CC} to below $V_{th(UVLO)}$ and enters Power-down mode.

The start-up circuit charges the VCC capacitor to $V_{startup}$ but instead of starting up, the VCC capacitor is discharged again. This is repeated for three cycles to obtain a longer restart time.

The restart time of one restart cycle consists of two periods:

- Discharging the VCC capacitor by an internal current source (2.5 mA). The discharge time is independent of the mains voltage[3].
- Charging the capacitor from $V_{th(UVLO)}$ to $V_{startup}$ by the external start-up circuit of typically 111 μA at 230 V (AC).

The discharge current is much higher than the charge current. So the mains voltage and the start-up circuit mainly determine the restart time.

The discharge time is approximately:

$$t_{dch} = \frac{C_{VCC} \times (V_{startup} - V_{th(UVLO)})}{I_{CC(restart)}} = \frac{4.8\ \mu F \times (21.3\ V - 12.5\ V)}{2.5\ mA} = 17\ ms \quad (2)$$

Where:

- C_{VCC} is the total capacitance on pin VCC
- $I_{CC(restart)}$ is the current discharged by the internal current source

The charge time is approximately[4]:

$$t_{ch} = \frac{C_{VCC} \times (V_{startup} - V_{th(UVLO)})}{I_{ch}} = \frac{4.8\ \mu F \times (21.3\ V - 12.5\ V)}{111\ \mu A} = 0.38\ s \quad (3)$$

Where:

- I_{ch} is the charge current into the VCC capacitor (see Equation 16)

For worst case (= shortest) t_{ch}, calculate I_{ch} for high mains and for $V_{CC} = V_{th(UVLO)}$. I_{ch} = 111 μA for V_{mains} = 230 V (AC) and R1 = 1.5 MΩ.

3. The first discharge differs somewhat from the following ones. The starting voltage can be lower or higher (depending on the load) and the discharge current source is not yet switched on. The operating supply current (= 0.58 mA) discharges The VCC capacitor.
4. I_{ch} also flows during the discharge. But usually $I_{ch} << I_{dch}$ so this can be neglected.

The total restart delay for the start-up circuit with two resistors approximately equals:

$$t_{restart} = 3 \times (t_{dch} + t_{ch}) = 3 \times (0.017\ s + 0.38\ s) = 1.2\ s \quad (4)$$

3.5.7 Ratio OPP time-out/restart delay

In a continuous overload, the supply keeps switching on and off (only valid for the non-latched version). At high mains, the ratio of the on-time and off-time is approximately 1:20. This is sufficient to keep the average input power during a continuous overload below 5 W in most applications.

The average input power during a continuous overload is:

$$P_{i(AV)} = \frac{t_{to(OV)}}{t_{restart} + t_{to(OV)}} \times \frac{P_{o(M)(max)}}{\eta} = \frac{60\ ms}{1.2\ s + 60\ ms} \times \frac{90\ W}{0.9} \quad (5)$$

Where:

- $P_{i(AV)}$ is the average input power during an overload
- $t_{to(OV)}$ is the overpower protection time-out time, the time from exceeding the overpower threshold to triggering the protection. This time is fixed to 60 ms in the IC.
- $t_{restart}$ is the restart delay, the time from triggering the protection until the next start-up attempt
- $P_{o(M)(max)}$ is the maximum peak output power, the maximum power that the supply can deliver during the overpower protection time-out time.

The restart delay depends on the input voltage, the start-up circuit and the VCC capacitor. The restart delay can be changed by changing the values of the start-up circuit or the VCC capacitor, but this also influences the start-up time.

The input power at continuous overload can be decreased in the following way:

1. Increase the restart delay by increasing the start-up resistors or capacitor C_{VCC}.
2. Decrease the maximum output power by increasing the current sense resistor (if possible).

3.6 External overvoltage protection and overtemperature protection

3.6.1 General

Two protection features can be implemented on pin PROTECT using only a minimum number of components:

- Output OverVoltage Protection (OVP)
- OverTemperature Protection (OTP)

The protection features on pin PROTECT are always latched (also in the non-latched version).

3.6.2 Circuit description

An internal current source attempts to keep the voltage on pin PROTECT equal to 0.65 V. It has a range of −107 μA to +32 μA (that is, it can sink 107 μA and source 32 μA). If the internal current source is out of range, the pin can no longer be kept within the 0.5 V to 0.8 V window. Latched protection is triggered if the voltage on pin PROTECT drops below 0.5 V or exceeds 0.8 V for at least four consecutive switching cycles.

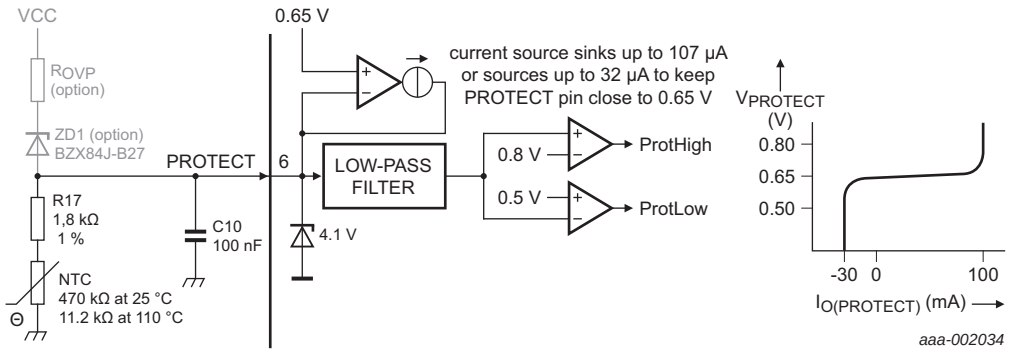


Fig 16. Pin PROTECT

3.6.3 Filtering

Due to internal filtering, pin PROTECT does not respond to HF signals.

The PROTECT pin has two kinds of internal filtering:

- Pulses shorter than 3 μs are ignored
- The fault condition has to last for at least four consecutive switching cycles

Pin PROTECT becomes immune to false triggering by disturbances from for example, GSM.

In extreme cases, such as exposure to very strong electromagnetic fields, pin PROTECT can pick up a disturbance with an amplitude of several volts. The internal ESD protection diode can rectify such high amplitude disturbances, which can unintentionally trigger the OVP. If so, a 10 Ω resistor between pin PROTECT and the external capacitor (as close as possible to the pin) can be very effective.

3.6.4 External output overvoltage protection

The output OVP is activated if the VCC voltage exceeds the Zener voltage by 0.8 V.

An external OVP application is optional. It is only required when the OVP level must be lower than the fixed 30 V level of the internal OVP protection or if extra filtering of the auxiliary winding voltage is required.

3.6.5 External overtemperature protection

The OTP is triggered when the voltage on pin PROTECT drops below 0.5 V. This happens when the resistance of the NTC with series resistor R17 has dropped below 0.5 V / 32 μA = 15.6 kΩ. VCC variations do not influence the OTP because pin PROTECT is internally biased.

3.6.6 Clamp

An internal clamp keeps the voltage on pin PROTECT at 4.1 V to prevent damage to the pin in case of spikes. The clamp voltage is specified at a 200 μA input current (the exact voltage depends on the current). In Power-down mode, the clamp voltage drops to approximately 2.0 V.

3.7 Slope compensation

The TEA1731(L)TS has built-in slope compensation to prevent subharmonic oscillation in CCM mode at duty cycles above 50 %. The slope compensation is internally added to the CTRL input signal (see Figure 17). The slope compensation is 20 mV/μs referred to pin ISENSE. The slope compensation is only active on duty cycles higher than 45 %.

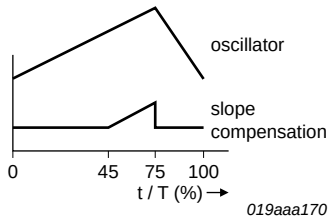


Fig 17. Slope compensation waveforms

3.8 Driver

The driver circuit has a current sourcing capability of 250 mA typical and a current sink capability of 750 mA typical. This permits fast turn-on and turn-off of the power MOSFET for efficient operation. See Figure 6 for DRIVER pin control.

3.9 Frequency modulation

The switching frequency and its harmonics are responsible for a large part of the conducted EMI problems. Modulation of the switching frequency spreads all frequency peaks that are related to the switching frequency over wider bands, significantly decreasing the so-called "average measurement". See Figure 6 for the location of oscillator and frequency modulation.

The oscillator is continuously modulated at a rate of 280 Hz and a range of ±6 % (±4 kHz at 65 kHz). For example, the third harmonic of 65 kHz is spread over a frequency band of 3 × 8 = 24 kHz.

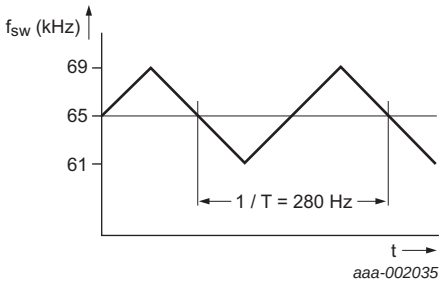


Fig 18. Frequency modulation

4. Application (pin-by-pin)

4.1 Pin VCC

4.1.1 Start-up circuits

A low-cost start-up circuit that also takes care of the X-cap discharge is the two resistor start-up circuit. See Section 5 for a full explanation of the various start-up circuits.

4.1.2 VCC capacitor

The VCC capacitor must be as small as possible to make the start-up time (and the latch reset time) as short as possible.

First of all the value of the capacitor must be sufficient to supply the TEA1731(L)TS until the auxiliary winding takes over. This depends on the configured soft start time, the load on the output and the values of the secondary capacitors.

Other factors determine the minimum value of the capacitor. Some worst case tests to determine the minimum value of the VCC capacitor are:

- **No load operation**

  The supply runs at low frequency so there is a long interval between two consecutive charge pulses from the auxiliary winding. V_{CC} must not drop to too close to $V_{th(UVLO)}$ (< 2 V) before the next cycle.

- **Transient from full load to no load**

  A transient from full load to no load can cause a small overshoot on the output voltage. It can take a long time for the output capacitor to discharge to the level at which the supply starts to switch again because of the absence of any external load.

  During this time, the auxiliary winding does not charge the VCC capacitor. This overshoot can be limited by modifying the loop. Add resistor R25 and capacitor C17 at for example, 3.9 kΩ and 1 nF respectively (see Figure 1).

- **Low ESR type**

  The VCC capacitor must be a low Equivalent Series Resistance (ESR) type. Under low load or no load conditions, the switching frequency can be very low, for example, 250 Hz. The auxiliary voltage, which can have a duty cycle of only 0.1 %, must charge the VCC capacitor. It is only present for a few μs per cycle and the time between two cycles can be a few ms. So, the VCC capacitor charge current at no load is roughly equal to the current consumption of the IC multiplied by 1000: $1000 \times 0.5\ mA = 0.5\ A$.

  Use a low ESR capacitor because the relatively high ESR of a regular electrolytic capacitor limits the charge current and can cause the VCC to drop below $V_{th(UVLO)}$. If this happens, the IC keeps restarting under no load conditions.

4.1.3 Auxiliary winding or take-over winding

The optimal voltage of the auxiliary winding is approximately 20 V:

- Not much lower because during a no load operation it has to be able to keep the V_{CC} above the $V_{th(UVLO)}$. Keep a margin of 2 V above the maximum $V_{th(UVLO)}$ value to have some margin for disturbances and component spread.
- Not much higher because at maximum load the V_{CC} must not trigger the OVP.

The purpose of the series inductor L1 is to prevent that the ringing at the start of the secondary stroke is rectified. It charges the VCC capacitor to above the OVP level.

L1 is not always required. It depends on the coupling between the windings. Sometimes a resistor of approximately 4.7 Ω is good enough.

4.1.4 Maximum start-up current

The maximum current that can be supplied by the start-up circuit must not exceed 1 mA. This means that the start-up circuit must not be able to deliver more than 1 mA at maximum mains voltage. During latched protection, VCC is clamped to 5.4 V. The clamp can sink at least 1 mA over the entire operating temperature range. Above 1 mA the clamp holding VCC below its maximum rating cannot be guaranteed[5].

If a charge current higher than 1 mA is required, a 30 V Zener diode from pin VCC to pin GND can be used to protect the IC. In that case, the internal OVP cannot work anymore because the Zener keeps the VCC below 30 V. An external OVP at a slightly lower voltage, for example 27 V, must replace the internal OVP.

If a charge pump is used (see Section 5.4), the VCC voltage can be limited by replacing one of the charge pump diodes (D_{dch}) by a 30 V Zener diode. If the Zener diode is placed at this position, it does not influence the internal OVP.

Also, during no load operation, the maximum current that can be supplied by the start-up circuit must not exceed the current into pin VCC (0.58 mA supply current + approximately 0.5 mA optocoupler transistor current ≈ 1.08 mA).

4.1.5 PCB layout

Pin VCC must not be treated as a small signal pin because the relatively high current to charge the gate of the MOSFET also passes through this pin. Keep the loop from the positive terminal of the VCC capacitor to pin VCC, via pin DRIVER, to the gate of the MOSFET, and via the source of the MOSFET back to the negative terminal of the VCC capacitor, as small as possible.

4.2 Pin CTRL

A capacitor of 1 nF on pin CTRL is a good value for most applications.

If the capacitor is much larger, it responds too slowly to load transients. Especially from full load to no load this can result in UVLO.

If the capacitor is much smaller, the control loop can become unstable and sensitive to disturbances.

4.3 Pin DRIVER

The source and sink currents on pin DRIVER can be high. The source current also rushes through pin VCC and the sink current through pin GND. This means that the PCB layout requires extra attention to avoid large loops.

5. Above a certain current, the clamp behaves like a current source. The voltage increases and the current remains constant.

4.4 Pin ISENSE

4.4.1 Configuring the current sense resistor

Calculate the maximum primary peak current before the correct value of the current sense resistor is calculated. This is done with Equation 6 or Equation 7.

In DCM mode:

$$I_{peak(max)} = \sqrt{\frac{2 \times P_{o(max)}}{\eta \times L \times f_{sw}}} \quad (6)$$

In CCM mode:

$$I_{peak(max)} = \frac{P_{o(max)}}{\eta} \times \frac{V_i + NV_o}{V_i \times NV_o} + \frac{1}{2 \times L \times f_{sw}} \times \frac{V_i \times NV_o}{V_i + NV_o} \quad (7)$$

Where:

- $I_{peak(max)}$ is the maximum continuous primary peak current, the peak current at which the OPP triggers
- $P_{o(max)}$ is the maximum continuous output power, the output power at which the OPP triggers
- η is the expected efficiency of the flyback at maximum output power
- V_i is the minimum rectified mains voltage (= $\sqrt{2} \times$ the minimum mains voltage) at which the supply must be able to deliver the maximum continuous output power[6].
- N is the winding ratio of the transformer
- V_o is the output voltage
- f_{sw} is the switching frequency, in this case 65 kHz (the "high power" area of the frequency curve, see Figure 8)

Now the (maximum) current sense resistor value can be calculated with Equation 8:

$$R_{ISENSE} = \frac{V_{th(sense)opp}}{I_{peak(max)}} = \frac{400\ mV}{I_{peak(max)}} \quad (8)$$

Where:

- $V_{th(sense)opp}$ is the overpower protection threshold voltage on pin ISENSE
- $I_{peak(max)}$ is the maximum continuous primary peak current, the peak current at which the OPP triggers

Another way to determine the correct value for the sense resistor is by trial and error:

1. Connect a load to the output and set the load to the rated maximum continuous output power of the application.

6. The peak current is larger during the valley of the mains ripple. During normal operation, the OPP threshold can already be exceeded during the valleys of the ripple on the bulk capacitor voltage. But this does not trigger the OPP. As long as the threshold is not exceeded during the tops of the bulk capacitor ripple voltage, the OPP time-out counter is reset each 8.33 ms or 10 ms. It never reaches the 60 ms OPP time-out. The OPP can only trigger if the OPP threshold is exceeded throughout the entire mains cycle.

2. Apply the minimum mains voltage at which the supply must be able to deliver the maximum continuous output power.
3. Increase the current sense resistor until the supply triggers the overpower protection. Then reduce the current sense resistor by about 5 % to keep some margin for normal operation.

The sense resistor must be accurate (1 %) and have a low inductance. Splitting the sense resistance into two or three parallel resistors not only makes it easier to implement the desired resistance and power rating but it also helps to reduce the inductance.

4.4.2 Calculating the maximum temporary peak output power

The maximum instantaneous primary peak current can now be calculated with Equation 9:

$$I_{peak(M)(max)} = \frac{V_{sense(max)}}{R_{ISENSE}} = \frac{500\ mV}{R_{ISENSE}} \quad (9)$$

Where:

- $V_{sense(max)}$ is the maximum sense voltage on pin ISENSE

Now the maximum temporary peak output power can be calculated[7].

In DCM mode:

$$P_{o(M)(max)} = \eta \times \frac{V_i \times NV_o}{V_i + NV_o} \times \frac{1}{2} \times L \times (I_{peak(M)(max)})^2 \times f_{sw} \quad (10)$$

In CCM mode:

$$P_{o(M)(max)} = \eta \times \frac{V_i \times NV_o}{V_i + NV_o} \times \left(I_{peak(M)(max)} - \frac{V_i \times NV_o}{2 \times L \times f_{sw} \times (V_i + NV_o)}\right) \quad (11)$$

Where:

- η is the expected efficiency of the flyback at maximum output power
- $I_{peak(M)(max)}$ is the maximum instantaneous primary peak current, limited by the OCP
- f_{sw} is the switching frequency, in this case 80 kHz, the "peak power" area of the frequency curve, see Figure 8
- V_i is the value of the rectified mains voltage during the valley of the ripple

This is the maximum temporary peak output power at which the output voltage remains intact.

If the temporary peak output power is not high enough, it can only be increased by decreasing the current sense resistor value. This also increases the maximum continuous output power.

7. Calculating the maximum temporary output power is complicated because it depends on the mains ripple on the bulk capacitor, which itself depends on the output power.

4.4.3 Low-pass filter (C7 and R13)

The low pass filter consisting of capacitor C7 and resistor R13 has two purposes:

- It prevents negative spikes, which cause a DC offset across capacitor C5, from reaching the pin. The internal ESD protection diode can rectify these. The inductance of the current sense resistor and the PCB tracks cause the negative spikes.
- See Section 4.4.4 for more information about trimming the OPP compensation by influencing the delay.

4.4.4 Tuning the OPP compensation (C7 and R13)

The amount of overpower compensation is fixed inside the IC. It has been optimized for a typical 65 W application with a primary inductance of 650 μH, a current sense resistor of 0.2 Ω and a 100 pF + 1 kΩ filter on pin ISENSE.

It is still possible to trim the compensation for other configurations within certain limits. The compensation depends on the current sense resistor, so the current sense resistor must be chosen first.

Steps for trimming the overpower compensation:

1. Start with a 100 pF capacitor on pin ISENSE.
2. Apply the minimum mains voltage at which the supply must be able to operate.
3. Measure the maximum output power by slowly increasing the load until the OPP is triggered.
4. Apply the maximum mains voltage at which the supply must be able to operate.
5. Measure the maximum output power by slowly increasing the load until the OPP is triggered.
6. Increase the capacitor on pin ISENSE (but not above 470 pF) if the maximum output power at high input voltage is lower than the maximum output power at low input voltage (overcompensated). Decrease the capacitor on pin ISENSE (but not below 47 pF) if the maximum output power at high input voltage is higher than the maximum output power at low input voltage (undercompensated).
7. Repeat steps 2 to 6 until the maximum output power at high and low input voltage is equal.

Remarks:

- The output power as a function of the input voltage is not a linear function (see Figure 14). When the maximum output power has been tuned to be equal for both the absolute minimum input voltage (90 V (AC)) and the absolute maximum input voltage (264 V (AC)), the actual maximum output power is slightly higher between these limits.

  Another method to configure the compensation is tuning it in such a way that the maximum output power at nominal low mains (115 V (AC)) equals the maximum output power at high mains (230 V (AC)). In that case, the maximum output power is slightly lower at the minimum and maximum input voltage and slightly higher between the high and low nominal input voltages.
- Do not reduce the capacitance below 47 pF. Some capacitance is required to prevent that negative spikes from the current sense resistor reach pin ISENSE.

- Do not increase the capacitance above 470 pF because this increases the minimum peak current which can lead to audible noise.
- Resistor R13 must not be too high because it influences the soft start behavior. It reduces the voltage to which the soft start capacitor is charged. 1 kΩ is a good value for most applications. Mount the resistor as close as possible to pin ISENSE.

4.4.5 Calculating the effect of the OPP compensation

The compensation offset on the OPP threshold can be calculated with Equation 12. The equation is valid for dV/dt > 38.5 mV/µs. In a typical application, this corresponds with an input voltage > 90 V (AC).

$$\Delta V_{ctrl(Ipeak)} = \left(\frac{V_{bulk}}{L} \times R_{ISENSE} - 38.5 \times 10^{3}\right) \times 0.6 \times 10^{-6} \quad (12)$$

The resulting peak current reduction can be calculated with Equation 13:

$$\Delta I_{peak} = \frac{\Delta V_{ctrl(Ipeak)}}{R_{ISENSE}} \quad (13)$$

Where:

- ΔI_{peak} is the peak current reduction
- $\Delta V_{ctrl(Ipeak)}$ is the offset on $V_{ctrl(Ipeak)}$ caused by the OPP compensation (see Equation 12).
- R_{ISENSE} is the value of the current sense resistor (R11 in Figure 1)

Section 4.4.1 describes how to calculate the peak current and the resulting output power without input voltage compensation. ΔI_{peak} must be subtracted from the peak current before calculating the maximum output power. This is required to calculate the output power with input voltage compensation.

4.4.6 Disabling the overpower protection

Unlike in the TEA1733 series or the TEA1738 series, the overpower protection in the TEA1731(L)TS cannot be disabled because it is fully integrated in the IC. If this is not appreciated, for example, because a secondary IC handles it, it can be shifted to a higher power by lowering the current sense resistor. It is not recommended to make it too low:

- Controlling a relatively high power using only a fraction of the CTRL range results in a very high gain and can cause instability.
- Skipping part of the peak current reduction means that it is not sufficiently reduced before entering the VCO mode. This can cause audible noise. Normally, the peak current is first reduced by a factor 3 before the frequency enters the audible spectrum.

4.4.7 Configuring the soft start resistor and capacitor

The duration of the soft start can be configured by changing the values of the soft start capacitor and resistor. The duration of the soft start roughly equals:

$$t_{start(soft)} = R_{start(soft)} \times C_{start(soft)} \quad (14)$$

A soft start time of 4 ms is recommended, for example, R12 = 18 kΩ and C5 = 220 nF.

The value of the total soft start resistance (the sum of resistors R12 and R13) must not be lower than 12 kΩ. Otherwise, the 55 μA current source cannot charge the soft start capacitor to 0.5 V and the controller does not start switching.

Remarks:

- Do not choose a soft start time that is too long. The slower the supply starts up, the longer it takes before the auxiliary winding recharges the VCC capacitor. If this takes too long, V_{CC} drops below $V_{th(UVLO)}$ before the output voltage is in regulation.
- Changing the soft start resistor value slightly also influences the maximum output power at absolute minimum input voltage. So, after configuring $R_{start(soft)}$, check if it is required to retune the current sense resistor.

4.5 Pin PROTECT

4.5.1 Specifications

Table 3. Specifications pin PROTECT

Description	Min	Typ	Max
bandwidth	-	300 kHz	-
source current	30 μA	32 μA	34 μA
sink current	87 μA	107 μA	127 μA
low detection voltage	0.47 V	0.5 V	0.53 V
high detection voltage	0.75 V	0.8 V	0.85 V

4.5.2 OverVoltage Protection (OVP)

An external OVP is only required if the voltage of the internal OVP (30 V) is too high or if it has to be more accurate than ±1 V.

Lowest cost implementation of an external OVP is a Zener diode from pin VCC to pin PROTECT. But it is also possible to implement a separate filter between the auxiliary winding and pin PROTECT.

The OVP triggers when the current through the Zener exceeds 107 μA (typical). The voltage of the Zener diode is often specified at a higher current. This means that the OVP triggers at a slightly lower voltage than the nominal Zener voltage.

The OVP can be tuned by placing a resistor (R_{OVP} in Figure 16) in series with the Zener diode. A series resistor of 10 kΩ increases the OVP voltage by approximately 1 V ($\Delta V = R_{OVP} \times 107\ \mu A$).

The accuracy of the OVP depends on the coupling between the secondary winding and the auxiliary winding. The best coupling can be obtained when these windings are wound directly on top of each other.

4.5.3 OverTemperature Protection (OTP)

The OTP can trigger if the resistance from pin PROTECT to pin GND is lower than 0.53 V / 30 μA = 17.7 kΩ.

The OTP must trigger if the resistance from pin PROTECT to pin GND is lower than 0.47 V / 34 μA = 13.8 kΩ.

Select the NTC resistance as high as possible to obtain best accuracy (see Table 4).

Table 4. Suggested NTC values

Valid for Epcos B57164 series (other manufacturers offer comparable values)

Target temperature (°C)	Suggested NTC (R at 25 °C) (kΩ)	Series resistor (kΩ)
66 to 75	100	0 to 4.7
76 to 82	150	0 to 3.0
83 to 90	220	0 to 3.5
91 to 100	330	0 to 4.3
≥ 101	470	≥ 0

If a series resistor higher than 5 kΩ is required to tune the OTP to the desired temperature, consider choosing a higher NTC value.

The NTC is often placed near the hottest component on the PCB, which is not always close to the IC. The long PCB track from NTC to pin PROTECT can act as an antenna and pick up disturbances. A filter against such disturbances can be constructed without additional components by placing the series resistor (which is required anyway) between the NTC and pin PROTECT and as close as possible to the pin.

4.5.4 What to do when pin PROTECT is not used

Connect a 10 nF capacitor from pin PROTECT to pin GND to prevent that external disturbances can trigger pin PROTECT.

Also, connect a 470 kΩ resistor from pin PROTECT to pin GND to prevent that external leakage currents before start-up can charge pin PROTECT.

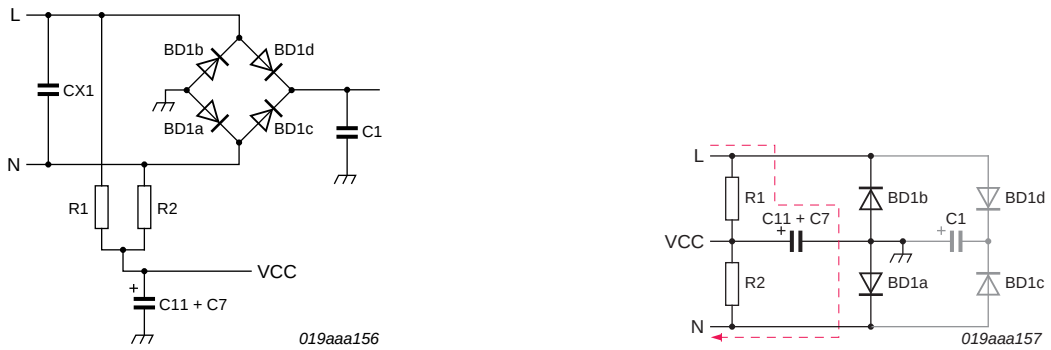
4.6 Pin GND

Do not treat pin GND as a small signal ground because the DRIVER discharge current also flows through this pin.

5. Start-up circuits

5.1 Two-resistor circuit

This is a low-cost solution that not only starts up but also takes care of X-cap discharge.



a. Start-up circuit with two resistors

b. Simplified representation

Fig 19. Start-up circuit with two resistors

Figure 19 (b) shows the circuit shown in Figure 19 (a) but drawn to show more clearly how the VCC capacitor is charged. Once the bulk capacitor C1 is fully charged, diodes BD1c and BD1d stop conducting. During the positive half mains cycle, diode BD1a conducts and the current through resistor R1 charges the VCC capacitor (C11 + C7). During this positive half cycle, part of the charge current leaks away into resistor R2. The worst case current that leaks into resistor R2 occurs when the VCC capacitor is almost charged:

$$I_{leak} = \frac{V_{startup}}{R2} = \frac{21.3\ V}{1.5\ M\Omega} = 14\ \mu A \quad (15)$$

The charge current into the VCC capacitor (leakage current already taken into account) approximately equals[8]:

$$I_{ch} = \frac{\left(2 \times \frac{\sqrt{2}}{\pi} \times V_{mains} - 2 \times V_{CC}\right)}{R1} - I_{CC(startup)} \quad (16)$$

Where:

- V_{mains} is the effective mains voltage
- $I_{CC(startup)}$ is the supply current of the IC in Power-down mode

The values of resistors R1 and R2 must be low enough to ensure the required discharge time of the X-cap (RC < 1 s) and to obtain an acceptable start-up time at low mains voltage. But it must also be as high as possible to keep the no load power consumption as low as possible.

Some examples of start-up times for different resistors are shown in Table 5.

8. Use $V_{CC} = V_{startup} = 21.3$ V for calculating the start-up time. Use $V_{CC} = V_{clamp(VCC)} = 5.4$ V for calculating the maximum current into clamp during latched protection.

Table 5. Start-up times for different start-up resistor values

VCC capacitance: 4.7 μF + 100 nF = 4.8 μF

Resistor R1 = R2	Start-up time at 90 V (AC)	Start-up time at 115 V (AC)	Power at 230 V (AC)[1]
680 kΩ	1.6 s	1.1 s	70 mW
820 kΩ	2.0 s	1.4 s	59 mW
1 MΩ	2.5 s	1.75 s	48 mW
1.2 MΩ	3.1 s	2.1 s	40 mW
1.5 MΩ	4.15 s	2.75 s	33 mW

[1] Power consumption of the combined X-cap discharge and start-up circuit at 230 V (AC).

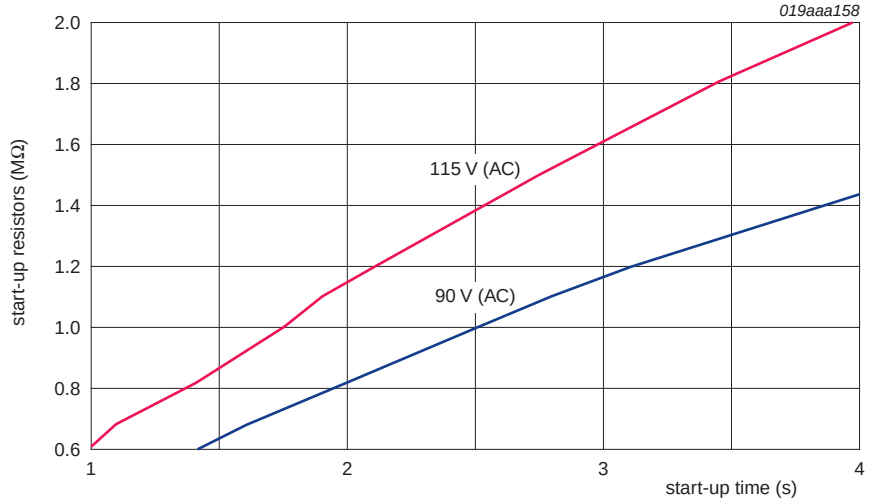


Fig 20. Start-up resistor value as a function of start-up time (VCC capacitance 4.8 μF)

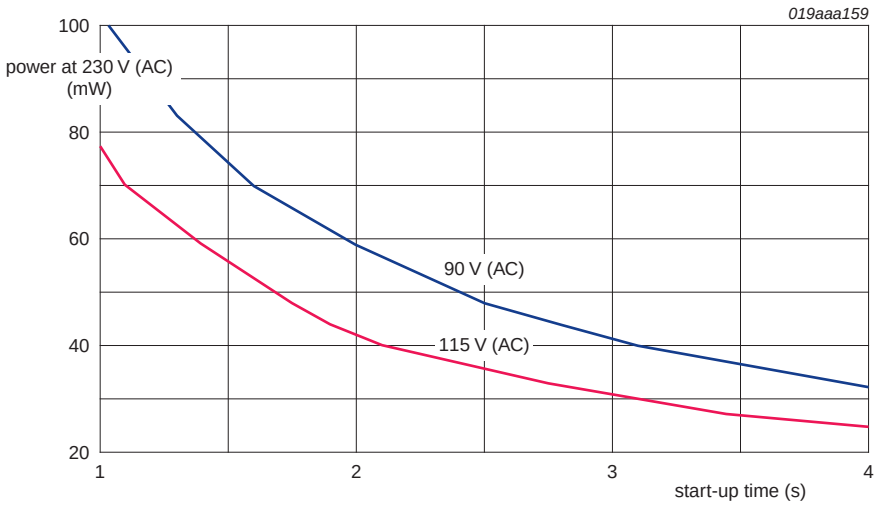


Fig 21. Power consumption of start-up circuit at 230 V (AC) as a function of start-up time (VCC capacitance 4.8 μF)

Figure 21 shows the power consumption by the combined start-up and X-cap discharge circuit as a function of the start-up time. The graph shows how to save power:

- More than 10 mW no load power can be saved by increasing the start-up time at 115 V (AC) from 2 s to 3 s.
- Approximately 17 mW no load power can be saved by specifying the start-up time at 115 V (AC) instead of 90 V (AC).

The voltage rating of most 1206 resistors is only 200 V. For 230 V (AC) applications the voltage across the start-up resistors can become nearly 400 V. This means that if SMD type resistors are used, R1 and R2 must each be split into two resistors in series.

5.2 Measuring start-up time

Capacitance across the bridge diodes changes the wave shape of the voltage before the bridge rectifier with respect to the primary ground. This can significantly decrease the start-up time. Connecting the ground clip of an oscilloscope to the primary ground of the flyback converter can add a few nF across the bridge diodes. This depends on the capacitance of the mains supply to ground.

Make sure that the board has no capacitive coupling to primary ground, so the correct worst case start-up time is measured:

- Use a current probe in the mains input cable to detect mains switch-on.
- The same current probe in the mains input cable can also be used to detect when the supply starts switching. The time, from the moment the supply starts to switch until it reaches 90 % of the output voltage, is only a few milliseconds. It can be ignored with respect to the total start-up time. If it is required to measure the output voltage with an oscilloscope, remove the Y-cap so that there is no capacitive coupling to primary ground.
- Use a resistor load instead of an electronic load. Remove the Y-cap if electronic load must be used.

Also important when measuring the start-up time:

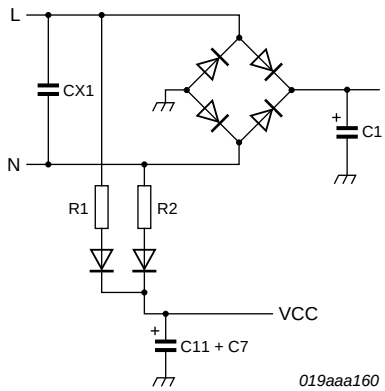
- Make sure that the VCC capacitor is entirely discharged before starting a measurement.
- Do not connect a probe or multimeter to the VCC. Even a 10 MΩ impedance influences the measurement.

5.3 Start-up circuit with diodes

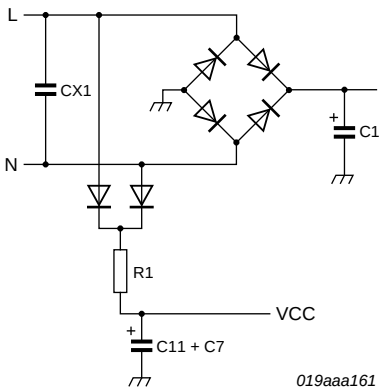
As explained in Section 3.2.1, the start-up circuit with two resistors also has a disadvantage. Some current does not flow into the VCC capacitor but is lost in one of the resistors. This can be prevented by placing diodes in series with the resistors (see Figure 22).

Figure 22 (a) requires two resistors and two low voltage diodes. Figure 22 (b) saves one resistor but requires two high-voltage diodes.

At 90 V (AC), adding the diodes reduces the start-up time by approximately 20 % without increasing the no load power consumption. The start-up time reduction is approximately 10 % at 115 V (AC).



a. Diodes at low side



b. Diodes at high side (requires high-voltage diodes but it saves one resistor

Fig 22. Start-up circuits using diodes in series

The diodes do not block the X-cap discharge path. The discharge of the X-cap takes place via resistors R1 or R2 through the series diode to pin VCC. From pin VCC, there are several paths to ground. Even when the IC is in Power-down mode a clamp on pin VCC is active. From ground, it can find its return path to the X-cap through one of the bridge diodes.

The charge current into the VCC capacitor approximately equals[9]:

$$I_{ch} = \frac{\left(2 \times \frac{\sqrt{2}}{\pi} \times V_{mains} - V_{CC}\right)}{R1} - I_{CC(startup)} \quad (17)$$

5.4 Start-up circuit with charge pump

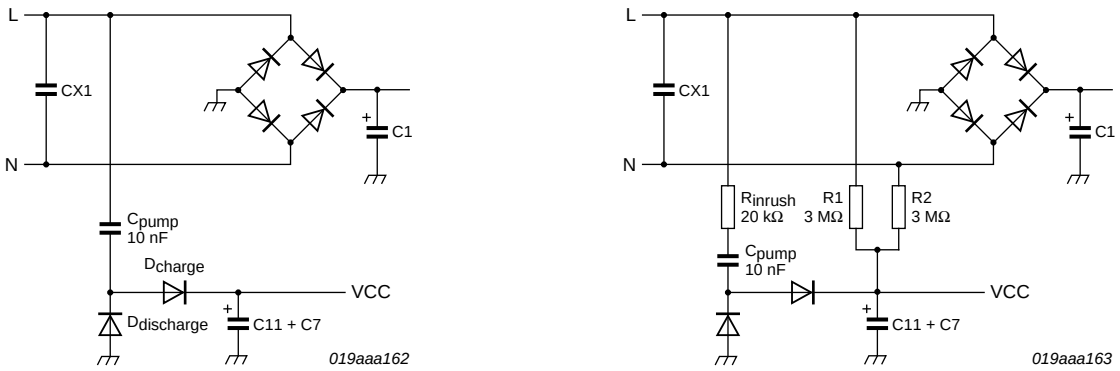
If the no load power requirements cannot be combined with the start-up time requirements, a more efficient way to decrease the start-up time is to use the charge pump circuit illustrated in Figure 23 (a).

During the positive half of each mains cycle, current flows from L via capacitor C_{pump} and diode D_{ch} to the VCC capacitor. This process stops when capacitor C_{pump} is fully charged.

During the negative half mains cycle, capacitor C_{pump} is discharged: From capacitor C_{pump} via capacitor C1 to ground and from ground via diode D_{dch} back to capacitor C_{pump}.

Unlike in the resistor start-up circuit, no significant power is lost in the circuit itself.

9. Use $V_{CC} = V_{startup} = 21.3$ V for calculating the start-up time. Use $V_{CC} = V_{clamp(VCC)} = 5.4$ V for calculating the maximum current into clamp during latched protection.



a. Basic charge pump start-up circuit

b. Practical charge pump start-up circuit with inrush current limiter and X-cap discharge

Fig 23. Start-up circuit with charge pump

The charge pump circuit does not provide a discharge path for the X-cap. An efficient way to provide the X-cap discharge path is to use the resistor start-up circuit because it not only discharges the X-cap but also helps to charge the VCC capacitor (see Figure 23 (b)).

- Choose values for resistors R1 and R2 that are as high as possible but low enough to comply with the X-cap discharge requirement: $R \times C < 1$ s:
  - For a 330 nF X-cap: R < 3 MΩ
  - For a 220 nF X-cap: R < 4.5 MΩ
- The value chosen for capacitor C_{pump} must be high enough to reach the start-up time target. Start with 10 nF and increase or decrease for a correct start-up value. It must be a high-voltage capacitor.
- The purpose of resistor R_{inrush} is to limit the inrush current when the supply is plugged in at the top of the sine wave. The value must be as low as possible to minimize losses but high enough to comply with the pulsed power rating of the resistor to survive the inrush current.
- Any low-voltage type diode with a breakdown voltage higher than 30 V can be used (breakdown voltage > 30 V).
- If the average start-up current at maximum input voltage exceeds the maximum current of the clamp on pin VCC (1 mA), a 27 V Zener diode must replace diode D_{dch}. This Zener diode must not be higher because the charge pump can trigger the internal OVP. It must not be lower because power is wasted during normal operation.

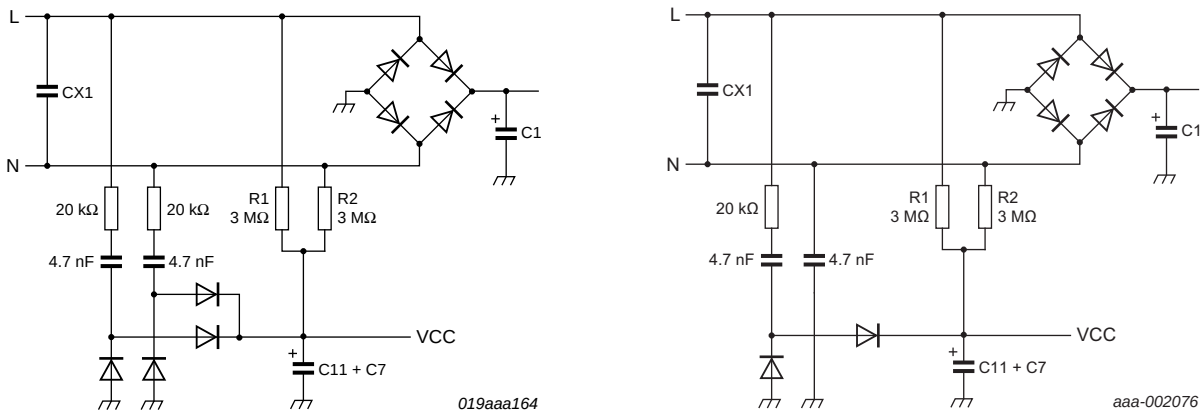
CAUTION

The rated maximum voltage of the high-voltage bulk capacitor can be exceeded if it is overcharged by the charge pump.

Remark: This can occur in the latched off-state when the power consumption is very low. In that case, the charge pump not only charges the VCC capacitor. It also very slowly charges the high-voltage bulk capacitor (C1) on the other side of the bridge rectifier.

Check at maximum input voltage that in Latched protection mode the charge pump does not charge the high-voltage bulk capacitor above its rated voltage. There are three ways to solve the problem:

- Increase the load on the rectified mains voltage. Even if some load has to be added to the rectified mains voltage to prevent that the charge pump damages the high-voltage bulk capacitor, the charge pump remains a more efficient solution than the resistor circuit.
- Another solution is to add an identical charge pump but connect its input to N instead of L (see Figure 23 (a) and Figure 24). In this case, the value of C_{pump} can be divided by two.
- Same as above but only add the capacitor to N. This saves two diodes. Now capacitor C_{pump} cannot be divided by two (see Figure 23 and Figure 24 (b)).



a. Symmetric charge pump circuit

b. Balanced charge pump circuit

Fig 24. Symmetrical charge pump circuits that prevent that capacitor C1 is charged

5.4.1 Charge pump in combination with PFC

If Power Factor Correction (PFC) is used, the voltage on the bulk capacitor can be (much) higher than the rectified mains voltage. Under these circumstances, the start-up current provided by the charge pump can be reduced or even entirely stopped. If a restart occurs during this condition, the start-up time can be very long. This can be solved by using a symmetrical charge pump.

6. Ways to reduce no load power

This section describes how the no load power can be minimized in any TEA1731-based flyback converter.

6.1 Remove power LED

Some adapters have an LED connected to the output to indicate that the power is present. An LED current of 2.5 mA supplied from a 20 V output voltage adds 50 mW to the no load power.

A high-efficiency LED in series with the LED of the optocoupler does not add to the power consumption but its brightness varies slightly with the load. Another option is to supply the LED from a separate low voltage winding.

6.2 Change the primary RDC clamp to a Zener clamp

The advantage of the Zener clamp is that it only conducts when required. It is independent of the switching frequency. Compared to a Resistor Diode Capacitor (RDC) clamp it reduces no load power but increases cost and EMI.

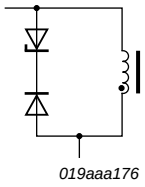


Fig 25. Zener clamp

6.3 Modify RDC clamp with a Zener diode

A Zener diode in series with the resistor of the RDC clamp prevents that the capacitor almost entirely discharges at each switching cycle when running at low frequency during no load. Adding the Zener diode increases cost and can also increase EMI (but not as much as a Zener clamp). Replacing resistor R9 (Figure 1) by a 100 V Zener diode saves 5 mW at 230 V (AC).

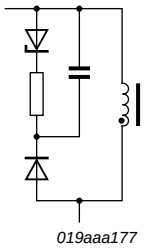


Fig 26. RDC clamp with Zener diode

6.4 Reconsider start-up time specification

Usually the maximum start-up time of a power supply is specified at a low nominal mains voltage (115 V (AC)). But occasionally the maximum start-up time is specified at the absolute minimum mains voltage (90 V (AC)). In this case, it is worth reconsidering this requirement. 90 V (AC) is probably encountered in less than 1 % of the field. However, to achieve a 2 s start-up time at 90 V (AC) requires 17 mW extra start-up power at 230 V (AC)[10].

Another 11 mW can be saved by allowing a maximum start-up time of 3 s instead of 2 s (see Figure 21).

6.5 Reduce VCC capacitor value

The efficiency of the start-up circuit can be significantly improved with a smaller VCC capacitor. Charging only half the VCC capacitor in the same time requires only half the power. A maximum start-up time of 2 s at 115 V (AC), reducing the VCC capacitance from 4.8 μF to 2.3 μF and doubling the start-up resistor values, saves approximately 20 mW.

6.6 X-cap quality

Use a good quality X-cap. A poor quality X-cap (330 nF) can dissipate as much as 25 mW at 230 V (AC)/60 Hz. A good quality X-cap dissipates less than 2 mW.

6.7 X-cap value

Reducing the value of the X-cap also decreases the X-cap losses. It is better to solve EMI problems at the source than by solving them with a very large X-cap. Reducing the X-cap value not only reduces the losses in the X-cap itself but also in the required X-cap discharge circuit.

6.8 Active X-cap discharge

Replace a passive X-cap discharge (resistor) by an active discharge circuit (requires a high-voltage transistor).

6.9 Active start-up circuit

Replace a passive start-up circuit (resistors) by an active charge circuit that is only active during start-up (requires a high-voltage transistor).

6.10 Increase the impedance of the output voltage divider

Doubling the impedance of the voltage divider on the output (resistors R23 and R24 in Figure 1) saves approximately 5 mW. In this case, also adapt capacitor C16 and resistor R22 to keep the same loop response. How much the impedance can be increased depends on the layout of the PCB and the input current of the shunt regulator.

10. If the two resistor start-up circuit is used and the VCC capacitance is 4.8 μF (4.7 μF + 100 nF).

6.11 Replacing the integrated shunt regulator (TL431) by a discrete shunt regulator

The widely available integrated TL431 shunt regulator versions usually require 1 mA for proper regulation. Some manufacturers specify 0.5 mA or 0.6 mA. It is not difficult to make a low (temperature stable) discrete alternative (see Figure 27).

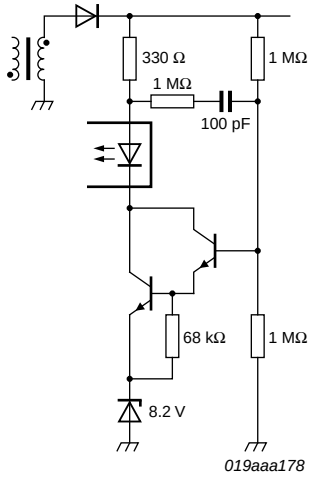


Fig 27. Discrete shunt regulator

Remark: If the power consumption on the secondary side is too low, it is possible that the controller does not switch enough to keep V_{CC} above $V_{th(UVLO)}$.

7. Layout recommendations

7.1 Input section

- Keep the mains tracks (L and N) low ohmic and close to each other to avoid loops.
- Position common-mode chokes away from the power section (MOSFET and transformer) and from each other to prevent magnetic coupling to any of the other components.
- Keep tracks from the bridge rectifier to capacitor C1 low ohmic and close to each other.

7.2 Power section

- The connection from the negative terminal of the bridge rectifier to the current sense resistor R11 must go via capacitor C1.
- The connection from the positive terminal of the bridge rectifier to the transformer must go via capacitor C1.
- Keep the cross section of the loop from capacitor C1 via the transformer, MOSFET Q1 and current sense resistor R11 back to capacitor C1 as small as possible.
- Place capacitor C2 close to capacitor C1.
- Place peak clamp circuit consisting of resistors R9 and R10, capacitor C3 and diode D1 close to the transformer and away from the TEA1731(L)TS.
- If MOSFET Q1 has a metal tab, insulate it from the heatsink. Connect the heatsink to the primary power ground.

7.3 Auxiliary winding

- Place rectifier diode D3, resistor R18 and VCC capacitor C11 close to the auxiliary winding.
- The connection of the ground of the auxiliary winding to the central signal ground point must go via capacitor C11. Use a separate track to avoid the noise in this ground causing noise in pin PROTECT, pin ISENSE, etc.
- Connect the central signal ground with a low ohmic track to the central power ground (capacitor C1).
- Keep the cross section of the loop from the auxiliary winding (via diode D3 and resistor R18) to VCC capacitor C11 and back to the auxiliary winding as small as possible.

7.4 Flyback controller

- Place the TEA1731(L)TS away from the transformer and MOSFET Q1.
- Keep the connection from current sense resistor R11 to the TEA1731(L)TS close to the ground track.
- Place VCC decoupling capacitor C7 close to pin VCC.
- The connection from pin VCC to VCC capacitor C11 must go via VCC decoupling capacitor C7.
- The connection from pin GND to the central signal ground must go via VCC decoupling capacitor C7.
- Place resistor R13 close to pin ISENSE.
- Place capacitor C10 and resistor R17 close to pin PROTECT. The other terminal of capacitor C10 must have a short connection to pin GND.
- Place capacitor C9 close to pin CTRL.

7.5 Mains insulation

- Keep at least 6 mm distance between the copper tracks of the primary and the secondary side.
- Place Y-cap CY1 close to the transformer.

7.6 Secondary side

- Heatsink secondary diodes D9 and D10:

  Connect the metal tab (which is internally connected to the cathode) directly to the heatsink. Connect the heatsink to the positive output track.
- Keep the cross section of the loop from the transformer via diodes D9 and D10 and capacitors C13 and C14 back to the transformer as small as possible. Keep output tracks close to each other.
- Use a separate signal ground for resistor R24 and shunt regulator U3. Connect the signal ground from resistor R24 and shunt regulator U3 via capacitor C19 to the power ground at capacitors C13 and C14.
- Place capacitor C19 close to resistors R20 and R23.
- The connection of resistors R20 and R23 to the positive output voltage must go via capacitor C19 to capacitors C13 and C14.
- Place the shunt regulator U3 and surrounding components away from transformer.

8. Abbreviations

Table 6. Abbreviations

Acronym	Description
CCM	Continuous Conduction Mode
DCM	Discontinuous Conduction Mode
EMI	ElectroMagnetic Interference
LEB	Leading-Edge Blanking
NTC	Negative Temperature Coefficient
OCP	OverCurrent Protection
OPP	OverPower Protection
OTP	OverTemperature Protection
OVP	OverVoltage Protection
PFC	Power Factor Corrector
SMPS	Switched Mode Power Supply
UVLO	UnderVoltage LockOut
VCO	Voltage Controlled Oscillator

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