Freescale Semiconductor
Technical Data

Document Number: A2T26H160-24S
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RF Power LDMOS Transistor

N-Channel Enhancement-Mode Lateral MOSFET

This 28 W asymmetrical Doherty RF power LDMOS transistor is designed for cellular base station applications covering the frequency range of 2496 to 2690 MHz.

2600 MHz

- Typical Doherty Single-Carrier W-CDMA Characterization Performance: V_{DD} = 28 Vdc, I_{DQA} = 350 mA, V_{GSB} = 0.6 Vdc, P_{out} = 28 W Avg., Input Signal PAR = 9.9 dB @ 0.01% Probability on CCDF.

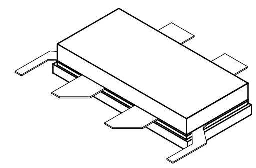
Frequency	G_{ps} (dB)	η_D (%)	Output PAR (dB)	ACPR (dBc)
2496 MHz	15.7	48.2	7.9	–31.5
2590 MHz	16.3	47.9	7.9	–34.0
2690 MHz	16.4	48.1	7.5	–34.0

Features

- Advanced High Performance In-Package Doherty
- Greater Negative Gate-Source Voltage Range for Improved Class C Operation
- Designed for Digital Predistortion Error Correction Systems
- In Tape and Reel. R3 Suffix = 250 Units, 44 mm Tape Width, 13-inch Reel.

A2T26H160-24SR3

2496–2690 MHz, 28 W AVG., 28 V AIRFAST RF POWER LDMOS TRANSISTOR



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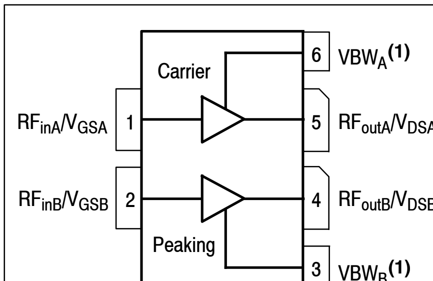


(Top View)

Figure 1. Pin Connections

1. Device cannot operate with the V_{DD} current supplied through pin 3 and pin 6.

Table 1. Maximum Ratings

Rating	Symbol	Value	Unit
Drain-Source Voltage	V_{DSS}	–0.5, +65	Vdc
Gate-Source Voltage	V_{GS}	–6.0, +10	Vdc
Operating Voltage	V_{DD}	32, +0	Vdc
Storage Temperature Range	T_{stg}	–65 to +150	°C
Case Operating Temperature Range	T_C	–40 to +150	°C
Operating Junction Temperature Range [1,2]	T_J	–40 to +225	°C

Table 2. Thermal Characteristics

Characteristic	Symbol	Value [2,3]	Unit
Thermal Resistance, Junction to Case Case Temperature 76°C, 28 W W-CDMA, 28 Vdc, I_{DQA} = 350 mA, V_{GSB} = 0.6 Vdc, 2590 MHz	$R_{\theta JC}$	0.56	°C/W

Table 3. ESD Protection Characteristics

Test Methodology	Class
Human Body Model (per JESD22-A114)	2
Machine Model (per EIA/JESD22-A115)	B
Charge Device Model (per JESD22-C101)	IV

Table 4. Electrical Characteristics (T_A = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Off Characteristics [4]					
Zero Gate Voltage Drain Leakage Current (V_{DS} = 65 Vdc, V_{GS} = 0 Vdc)	I_{DSS}	—	—	10	μAdc
Zero Gate Voltage Drain Leakage Current (V_{DS} = 32 Vdc, V_{GS} = 0 Vdc)	I_{DSS}	—	—	1	μAdc
Gate-Source Leakage Current (V_{GS} = 5 Vdc, V_{DS} = 0 Vdc)	I_{GSS}	—	—	1	μAdc
On Characteristics – Side A [4] (Carrier)					
Gate Threshold Voltage (V_{DS} = 10 Vdc, I_D = 60 μAdc)	$V_{GS(th)}$	0.8	1.2	1.6	Vdc
Gate Quiescent Voltage (V_{DD} = 28 Vdc, I_{DA} = 350 mAdc, Measured in Functional Test)	$V_{GS(Q)}$	1.4	1.8	2.2	Vdc
Drain-Source On-Voltage (V_{GS} = 10 Vdc, I_D = 0.6 Adc)	$V_{DS(on)}$	0.1	0.15	0.3	Vdc
On Characteristics – Side B [4] (Peaking)					
Gate Threshold Voltage (V_{DS} = 10 Vdc, I_D = 100 μAdc)	$V_{GS(th)}$	0.8	1.2	1.6	Vdc
Drain-Source On-Voltage (V_{GS} = 10 Vdc, I_D = 1.0 Adc)	$V_{DS(on)}$	0.1	0.15	0.3	Vdc

1. Continuous use at maximum temperature will affect MTTF.
2. MTTF calculator available at http://www.freescale.com/rf. Select Software & Tools/Development Tools/Calculators to access MTTF calculators by product.
3. Refer to AN1955, *Thermal Measurement Methodology of RF Power Amplifiers.* Go to http://www.freescale.com/rf. Select Documentation/Application Notes – AN1955.
4. Each side of device measured separately.

(continued)

Table 4. Electrical Characteristics (T_A = 25°C unless otherwise noted) **(continued)**

Characteristic	Symbol	Min	Typ	Max	Unit
Functional Tests (1,2) (In Freescale Doherty Production Test Fixture, 50 ohm system) V_{DD} = 28 Vdc, I_{DQA} = 350 mA, V_{GSB} = 0.4 Vdc, P_{out} = 28 W Avg., f = 2575 MHz, Single-Carrier W-CDMA, IQ Magnitude Clipping, Input Signal PAR = 9.9 dB @ 0.01% Probability on CCDF. ACPR measured in 3.84 MHz Channel Bandwidth @ ±5 MHz Offset.					
Power Gain	G_{ps}	14.5	15.5	17.5	dB
Drain Efficiency	η_D	43.0	47.0	—	%
Output Peak-to-Average Ratio @ 0.01% Probability on CCDF	PAR	7.0	7.7	—	dB
Adjacent Channel Power Ratio	ACPR	—	–31.0	–28.5	dBc
Load Mismatch (2) (In Freescale Doherty Characterization Test Fixture, 50 ohm system) I_{DQA} = 350 mA, V_{GSB} = 0.6 Vdc, f = 2590 MHz					
VSWR 10:1 at 32 Vdc, 178 W Pulse Output Power (3 dB Input Overdrive from 138 W Pulse Rated Power)	No Device Degradation				
Typical Performance (2) (In Freescale Doherty Characterization Test Fixture, 50 ohm system) V_{DD} = 28 Vdc, I_{DQA} = 350 mA, V_{GSB} = 0.6 Vdc, 2496–2690 MHz Bandwidth					
P_{out} @ 1 dB Compression Point, CW	P1dB	—	138	—	W
P_{out} @ 3 dB Compression Point (3)	P3dB	—	178	—	W
AM/PM (Maximum value measured at the P3dB compression point across the 2496–2690 MHz frequency range)	Φ	—	–18	—	°
VBW Resonance Point (IMD Third Order Intermodulation Inflection Point)	VBW_{res}	—	140	—	MHz
Gain Flatness in 194 MHz Bandwidth @ P_{out} = 28 W Avg.	G_F	—	0.7	—	dB
Gain Variation over Temperature (–30°C to +85°C)	ΔG	—	0.009	—	dB/°C
Output Power Variation over Temperature (–30°C to +85°C)	ΔP1dB	—	0.009	—	dB/°C

1. Part internally matched both on input and output.
2. Measurements made with device in an asymmetrical Doherty configuration.
3. P3dB = P_{avg} + 7.0 dB where P_{avg} is the average output power measured using an unclipped W-CDMA single-carrier input signal where output PAR is compressed to 7.0 dB @ 0.01% probability on CCDF.

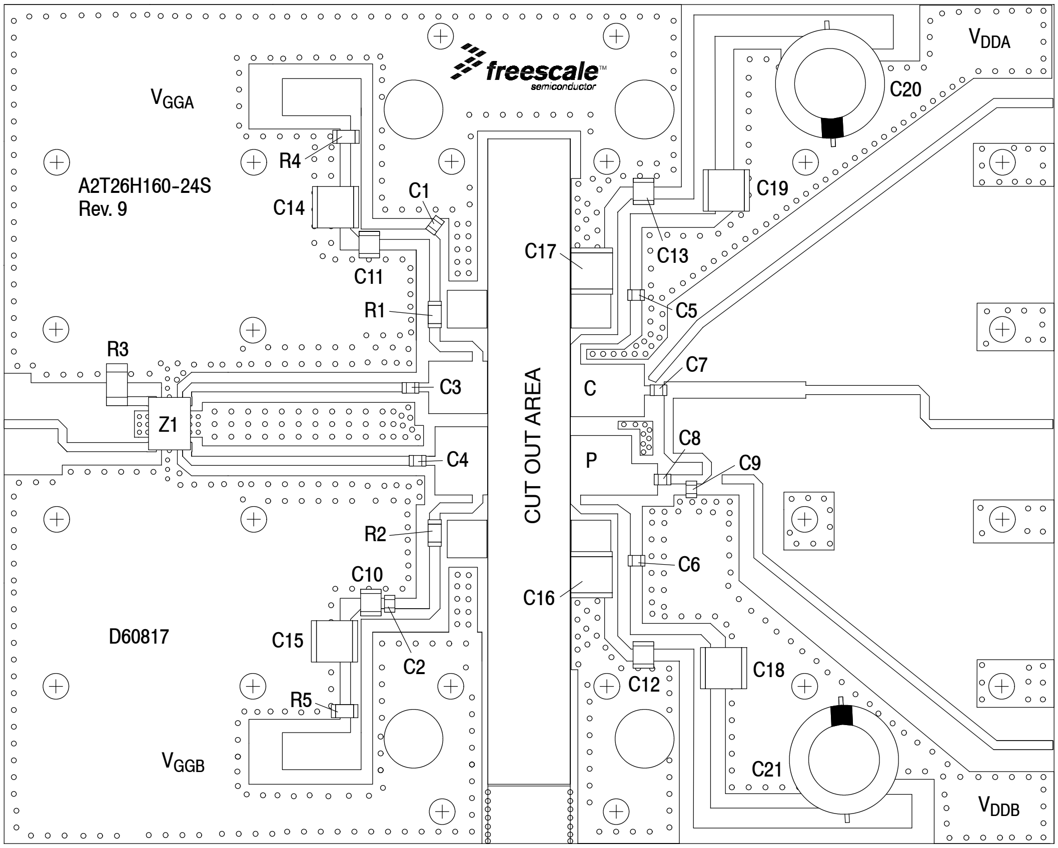


Figure 2. A2T26H160-24SR3 Production Test Circuit Component Layout

Table 5. A2T26H160-24SR3 Production Test Circuit Component Designations and Values

Part	Description	Part Number	Manufacturer
C1, C2, C3, C4, C5, C6, C8	9.1 pF Chip Capacitors	ATC600F9R1BT250XT	ATC
C7	6.8 pF Chip Capacitor	ATC600F6R8BT250XT	ATC
C9	0.2 pF Chip Capacitor	ATC600F0R2BT250XT	ATC
C10, C11, C12, C13	2.2 μF Chip Capacitors	C3225X7R2A225K230AB	TDK
C14, C15, C16, C17, C18, C19	10 μF Chip Capacitors	C5750X7S2A106K230KE	TDK
C20, C21	220 μF, 63 V Electrolytic Capacitors	SK063M0220B5S-1012	Yageo
R1, R2	2.2 Ω, 1/4 W Chip Resistors	CRCW12062R20JNEA	Vishay
R3	50 Ω, 4 W Chip Resistor	CW12010T0050GBK	ATC
R4, R5	1 KΩ, 1/4 W Chip Resistors	CRCW12061K00FKEA	Vishay
Z1	2300–2700 MHz Band, 90°, 2 dB Hybrid Coupler	X3C25P1-02S	Anaren
PCB	Rogers RO4350B, 0.020″, ε_r = 3.66	D60817	MTL

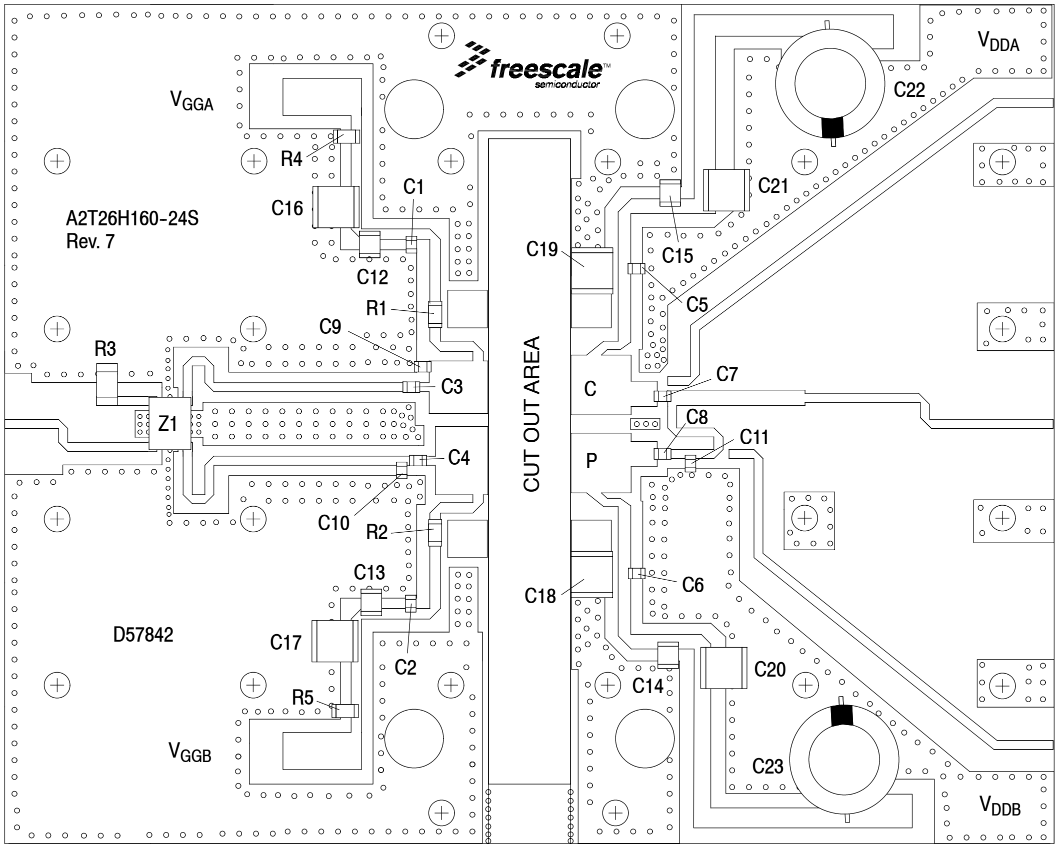


Figure 3. A2T26H160-24SR3 Characterization Test Circuit Component Layout — 2496–2690 MHz

Table 6. A2T26H160-24SR3 Characterization Test Circuit Component Designations and Values — 2496–2690 MHz

Part	Description	Part Number	Manufacturer
C1, C2, C3, C4, C5, C6, C7, C8	9.1 pF Chip Capacitors	ATC600F9R1BT250XT	ATC
C9, C10, C11	0.3 pF Chip Capacitors	ATC600F0R3BT250XT	ATC
C12, C13, C14, C15	2.2 μF Chip Capacitors	C3225X7R2A225K230AB	TDK
C16, C17, C18, C19, C20, C21	10 μF Chip Capacitors	C5750X7S2A106K230KB	TDK
C22, C23	220 μF, 63 V Electrolytic Capacitors	SK063M0220B5S-1012	Yageo
R1, R2	2.2 Ω, 1/4 W Chip Resistors	CRCW12062R20JNEA	Vishay
R3	50 Ω, 4 W Chip Resistor	CW12010T0050GBK	ATC
R4, R5	1 KΩ, 1/4 W Chip Resistors	CRCW12061K00FKEA	Vishay
Z1	2300–2700 MHz Band, 90°, 2 dB Hybrid Coupler	X3C25P1-02S	Anaren
PCB	Rogers RO4350B, 0.020″, ε_r = 3.66	D57842	MTL

TYPICAL CHARACTERISTICS

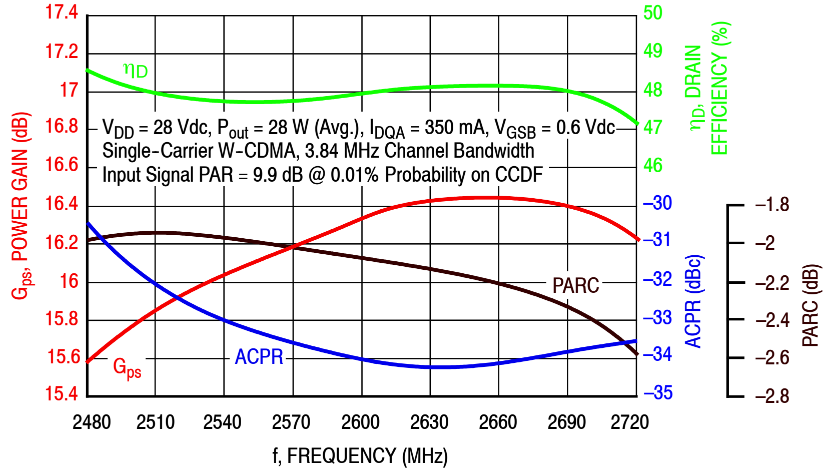


Figure 4. Single-Carrier Output Peak-to-Average Ratio Compression (PARC) Broadband Performance @ P_{out} = 28 Watts Avg.

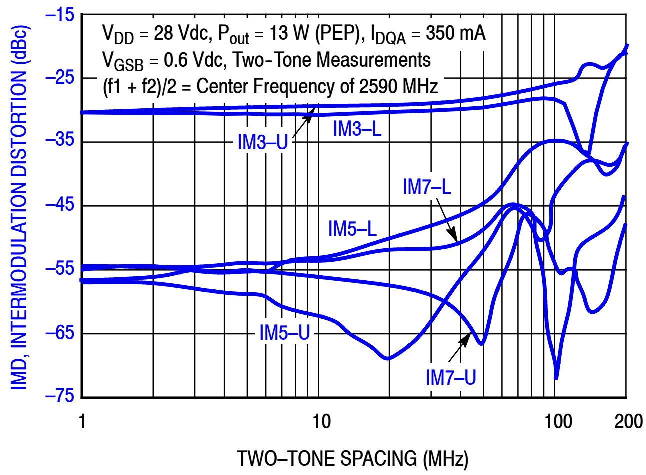


Figure 5. Intermodulation Distortion Products versus Two-Tone Spacing

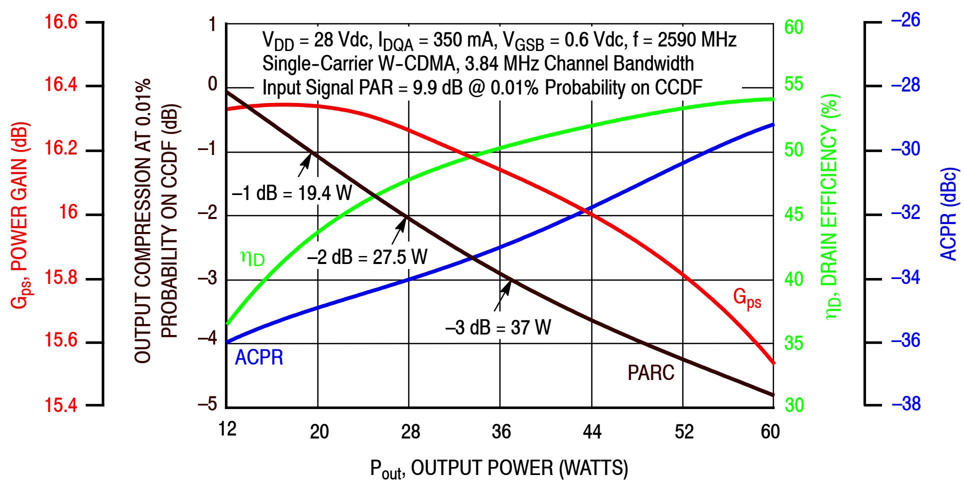


Figure 6. Output Peak–to–Average Ratio Compression (PARC) versus Output Power

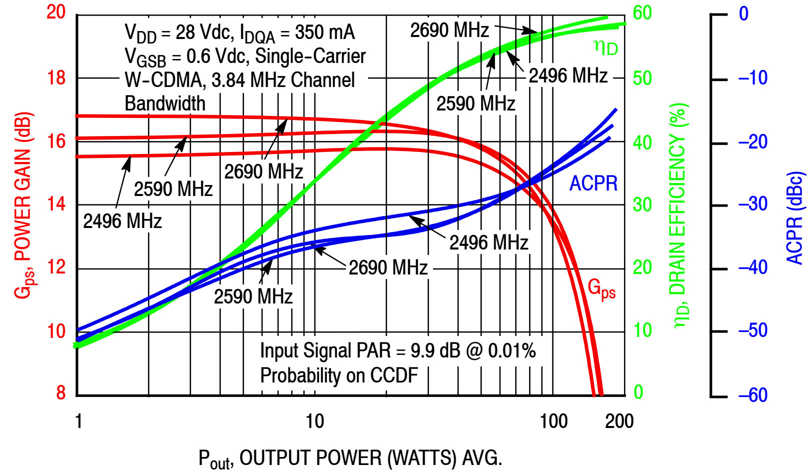


Figure 7. Single-Carrier W–CDMA Power Gain, Drain Efficiency and ACPR versus Output Power

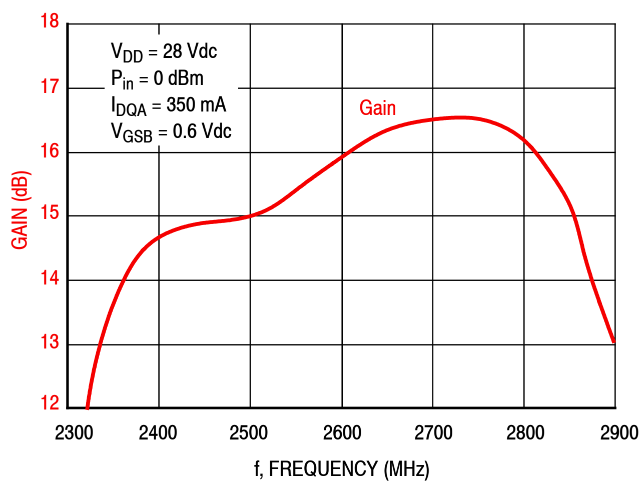


Figure 8. Broadband Frequency Response

Table 7. Carrier Side Load Pull Performance — Maximum Power Tuning

V_{DD} = 28 Vdc, I_{DQA} = 344 mA, Pulsed CW, 10 μsec(on), 10% Duty Cycle

			Max Output Power					
			P1dB					
f (MHz)	Z_{source} (Ω)	Z_{in} (Ω)	Z_{load} (1) (Ω)	Gain (dB)	(dBm)	(W)	η_D (%)	AM/PM (°)
2496	7.14 – j16.1	7.84 + j15.2	10.6 – j14.6	18.0	48.1	64	53.7	–14
2590	9.88 – j13.4	8.97 + j12.9	10.1 – j13.1	18.4	48.1	65	54.9	–15
2690	9.36 – j9.75	8.30 + j9.00	10.7 – j15.6	18.3	48.0	63	53.8	–14

			Max Output Power					
			P3dB					
f (MHz)	Z_{source} (Ω)	Z_{in} (Ω)	Z_{load} (2) (Ω)	Gain (dB)	(dBm)	(W)	η_D (%)	AM/PM (°)
2496	7.14 – j16.1	8.53 + j15.6	10.2 – j15.9	15.7	48.8	76	54.6	–18
2590	9.88 – j13.4	9.89 + j12.6	10.0 – j14.9	16.0	48.9	77	54.9	–19
2690	9.36 – j9.75	8.59 + j8.15	10.9 – j17.3	15.9	48.8	75	54.1	–19

(1) Load impedance for optimum P1dB power.
(2) Load impedance for optimum P3dB power.
Z_{source} = Measured impedance presented to the input of the device at the package reference plane.
Z_{in} = Impedance as measured from gate contact to ground.
Z_{load} = Measured impedance presented to the output of the device at the package reference plane.

Table 8. Carrier Side Load Pull Performance — Maximum Drain Efficiency Tuning

V_{DD} = 28 Vdc, I_{DQA} = 344 mA, Pulsed CW, 10 μsec(on), 10% Duty Cycle

			Max Drain Efficiency					
			P1dB					
f (MHz)	Z_{source} (Ω)	Z_{in} (Ω)	Z_{load} (1) (Ω)	Gain (dB)	(dBm)	(W)	η_D (%)	AM/PM (°)
2496	7.14 – j16.1	8.14 + j15.1	20.2 – j6.73	20.6	46.4	43	62.4	–19
2590	9.88 – j13.4	8.83 + j12.5	14.8 – j4.10	21.0	46.4	44	63.0	–21
2690	9.36 – j9.75	7.73 + j9.07	13.4 – j5.25	21.0	46.1	41	62.0	–20

			Max Drain Efficiency					
			P3dB					
f (MHz)	Z_{source} (Ω)	Z_{in} (Ω)	Z_{load} (2) (Ω)	Gain (dB)	(dBm)	(W)	η_D (%)	AM/PM (°)
2496	7.14 – j16.1	8.74 + j15.5	17.5 – j8.53	18.2	47.6	57	63.5	–26
2590	9.88 – j13.4	9.78 + j12.1	13.5 – j4.23	19.0	47.1	52	64.0	–30
2690	9.36 – j9.75	7.74 + j8.16	12.7 – j5.49	19.0	46.9	49	63.1	–30

(1) Load impedance for optimum P1dB efficiency.
(2) Load impedance for optimum P3dB efficiency.
Z_{source} = Measured impedance presented to the input of the device at the package reference plane.
Z_{in} = Impedance as measured from gate contact to ground.
Z_{load} = Measured impedance presented to the output of the device at the package reference plane.

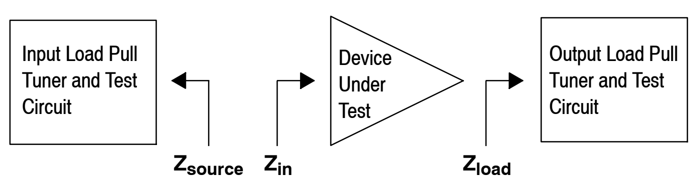


Table 9. Peaking Side Load Pull Performance — Maximum Power Tuning

V_{DD} = 28 Vdc, V_{GSB} = 0.6 Vdc, Pulsed CW, 10 μsec(on), 10% Duty Cycle

f (MHz)	Z_{source} (Ω)	Z_{in} (Ω)	Max Output Power P1dB Z_{load} (1) (Ω)	Gain (dB)	(dBm)	(W)	η_D (%)	AM/PM (°)
2496	7.60 – j18.3	7.68 + j19.7	9.04 – j14.6	13.1	50.5	113	54.8	–24
2590	10.1 – j16.7	10.5 + j17.9	8.89 – j14.2	13.4	50.5	111	54.6	–27
2690	11.6 – j11.2	12.8 + j11.3	9.69 – j16.8	13.4	50.4	110	54.0	–29

f (MHz)	Z_{source} (Ω)	Z_{in} (Ω)	Max Output Power P3dB Z_{load} (2) (Ω)	Gain (dB)	(dBm)	(W)	η_D (%)	AM/PM (°)
2496	7.60 – j18.3	8.64 + j20.2	9.31 – j15.9	10.9	51.2	131	55.3	–30
2590	10.1 – j16.7	12.1 + j17.5	9.45 – j15.3	11.3	51.1	129	54.9	–33
2690	11.6 – j11.2	13.1 + j9.46	10.7 – j17.9	11.2	51.0	127	54.4	–35

(1) Load impedance for optimum P1dB power.
(2) Load impedance for optimum P3dB power.
Z_{source} = Measured impedance presented to the input of the device at the package reference plane.
Z_{in} = Impedance as measured from gate contact to ground.
Z_{load} = Measured impedance presented to the output of the device at the package reference plane.

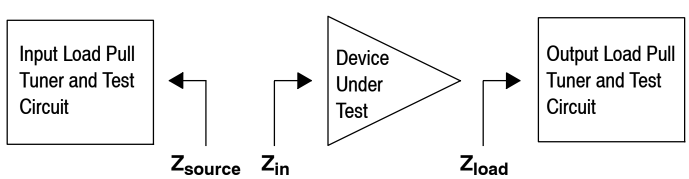
Table 10. Peaking Side Load Pull Performance — Maximum Drain Efficiency Tuning

V_{DD} = 28 Vdc, V_{GSB} = 0.6 Vdc, Pulsed CW, 10 μsec(on), 10% Duty Cycle

f (MHz)	Z_{source} (Ω)	Z_{in} (Ω)	Max Drain Efficiency P1dB Z_{load} (1) (Ω)	Gain (dB)	(dBm)	(W)	η_D (%)	AM/PM (°)
2496	7.60 – j18.3	6.75 + j20.0	15.2 – j5.96	14.3	49.0	79	66.1	–31
2590	10.1 – j16.7	9.24 + j18.8	10.7 – j4.18	14.6	48.6	72	66.6	–35
2690	11.6 – j11.2	12.7 + j13.2	9.18 – j7.22	14.6	48.6	72	65.9	–37

f (MHz)	Z_{source} (Ω)	Z_{in} (Ω)	Max Drain Efficiency P3dB Z_{load} (2) (Ω)	Gain (dB)	(dBm)	(W)	η_D (%)	AM/PM (°)
2496	7.60 – j18.3	7.82 + j20.5	15.3 – j7.51	12.2	49.7	94	66.3	–39
2590	10.1 – j16.7	11.2 + j18.4	11.4 – j6.56	12.6	49.7	93	66.7	–43
2690	11.6 – j11.2	13.4 + j10.8	9.86 – j8.35	12.6	49.5	88	65.8	–45

(1) Load impedance for optimum P1dB efficiency.
(2) Load impedance for optimum P3dB efficiency.
Z_{source} = Measured impedance presented to the input of the device at the package reference plane.
Z_{in} = Impedance as measured from gate contact to ground.
Z_{load} = Measured impedance presented to the output of the device at the package reference plane.



P1dB – TYPICAL CARRIER SIDE LOAD PULL CONTOURS — 2590 MHz

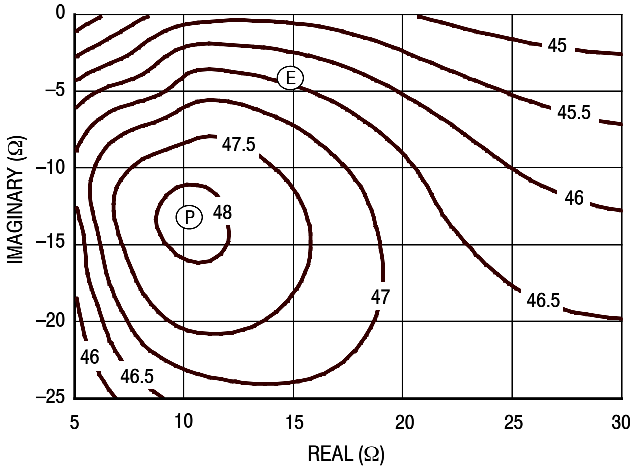


Figure 9. P1dB Load Pull Output Power Contours (dBm)

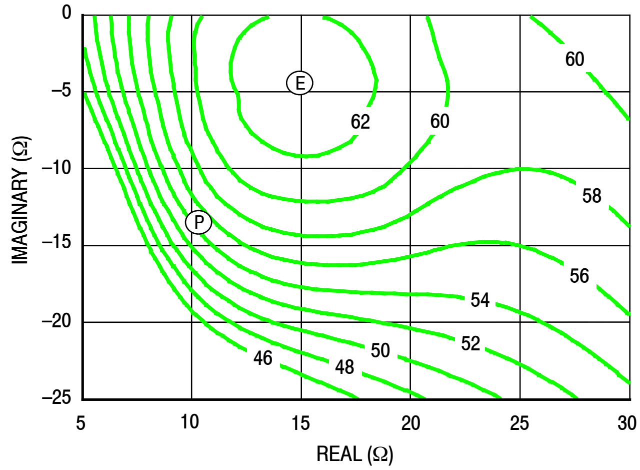


Figure 10. P1dB Load Pull Efficiency Contours (%)

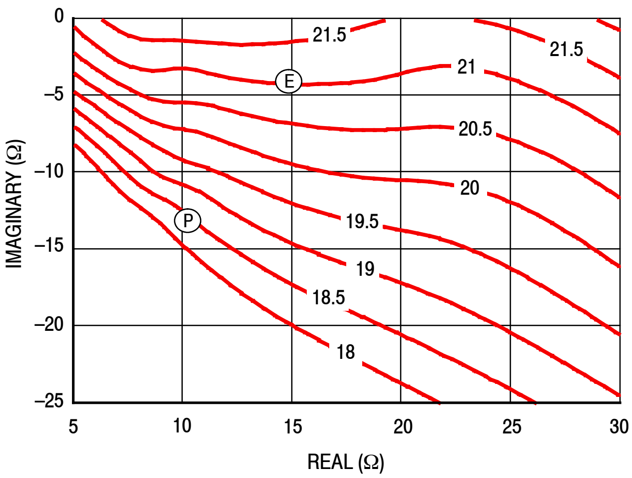


Figure 11. P1dB Load Pull Gain Contours (dB)

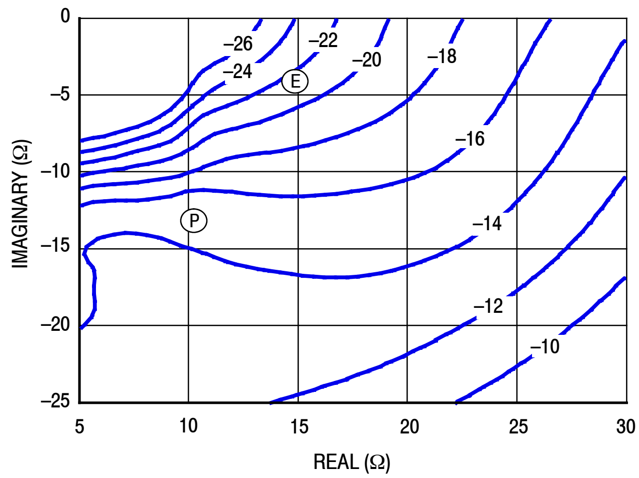


Figure 12. P1dB Load Pull AM/PM Contours (°)

NOTE: Ⓟ = Maximum Output Power

Ⓔ = Maximum Drain Efficiency

Gain

Drain Efficiency

Linearity

Output Power

P3dB – TYPICAL CARRIER SIDE LOAD PULL CONTOURS — 2590 MHz

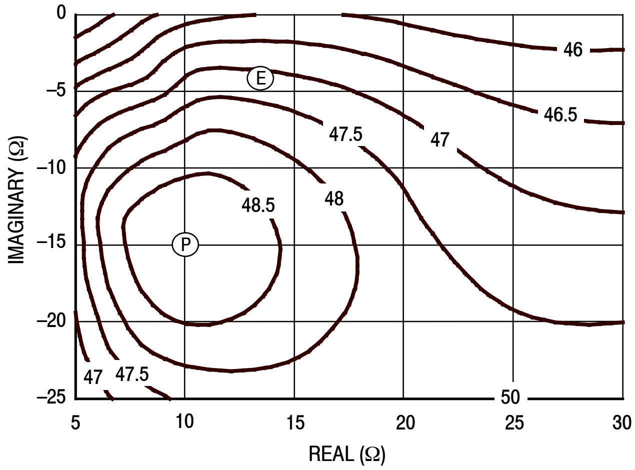


Figure 13. P3dB Load Pull Output Power Contours (dBm)

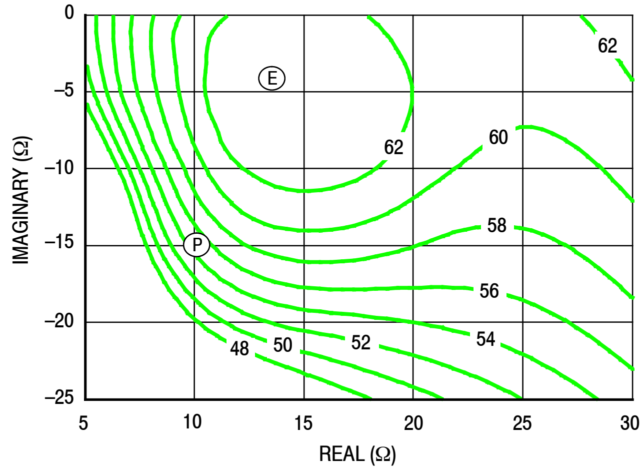


Figure 14. P3dB Load Pull Efficiency Contours (%)

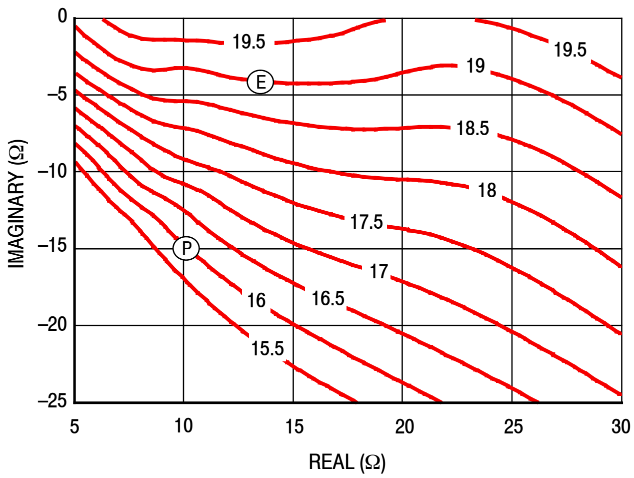


Figure 15. P3dB Load Pull Gain Contours (dB)

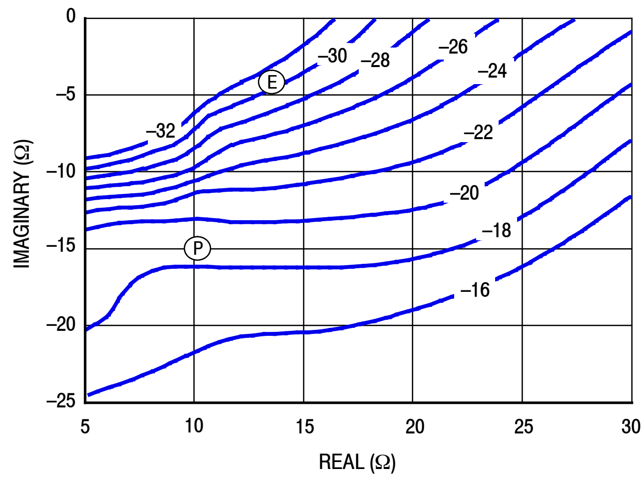


Figure 16. P3dB Load Pull AM/PM Contours (°)

NOTE: (P) = Maximum Output Power

(E) = Maximum Drain Efficiency

Gain
Drain Efficiency
Linearity
Output Power

P1dB – TYPICAL PEAKING SIDE LOAD PULL CONTOURS — 2590 MHz

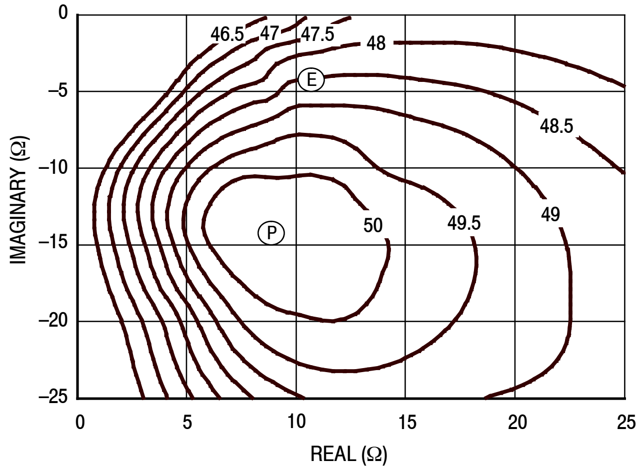


Figure 17. P1dB Load Pull Output Power Contours (dBm)

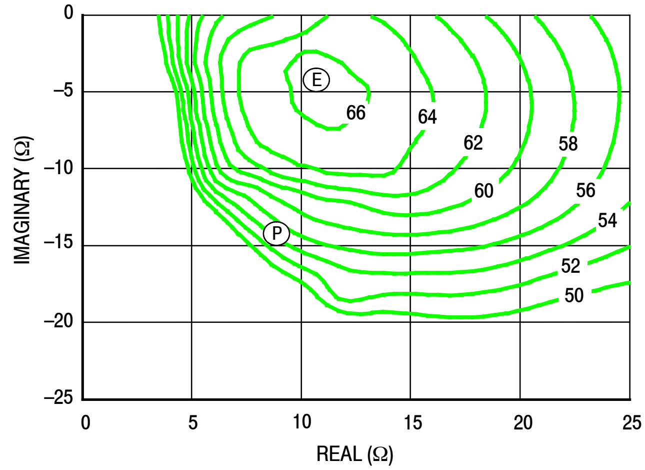


Figure 18. P1dB Load Pull Efficiency Contours (%)

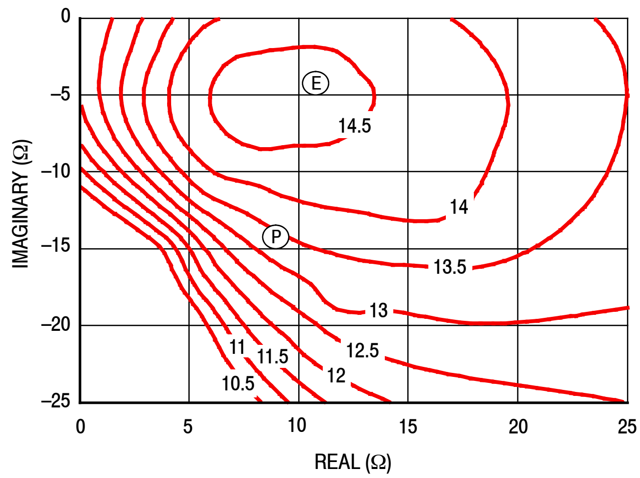


Figure 19. P1dB Load Pull Gain Contours (dB)

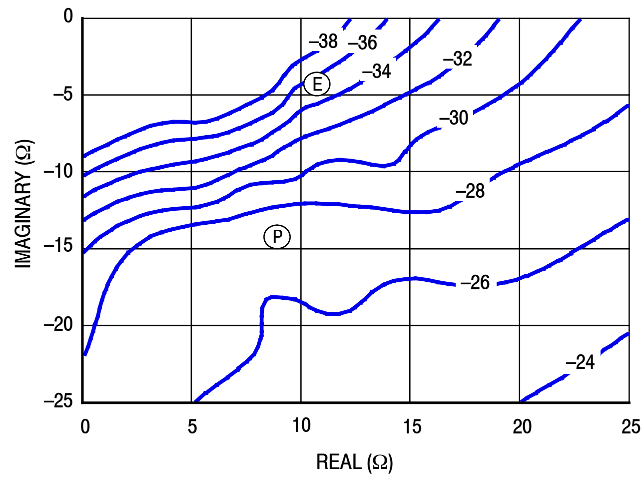


Figure 20. P1dB Load Pull AM/PM Contours (°)

NOTE: Ⓟ = Maximum Output Power

Ⓔ = Maximum Drain Efficiency

- Gain
- Drain Efficiency
- Linearity
- Output Power

P3dB – TYPICAL PEAKING SIDE LOAD PULL CONTOURS — 2590 MHz

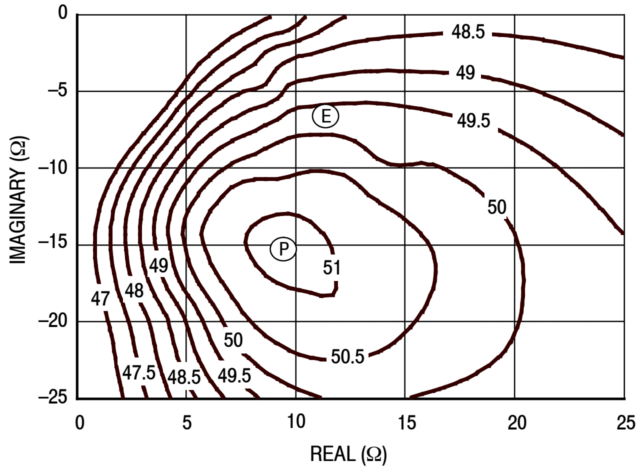


Figure 21. P3dB Load Pull Output Power Contours (dBm)

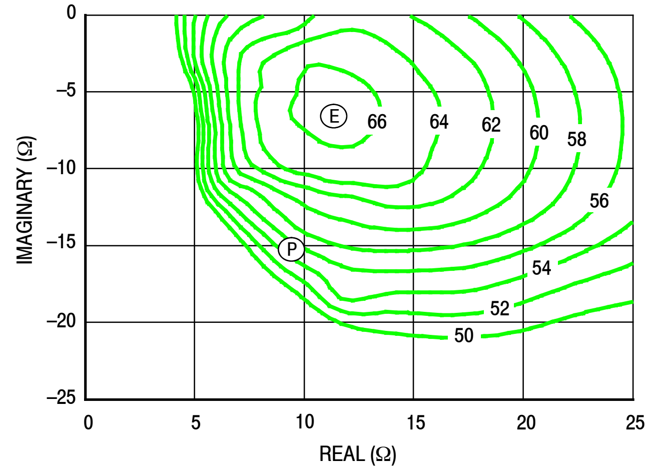


Figure 22. P3dB Load Pull Efficiency Contours (%)

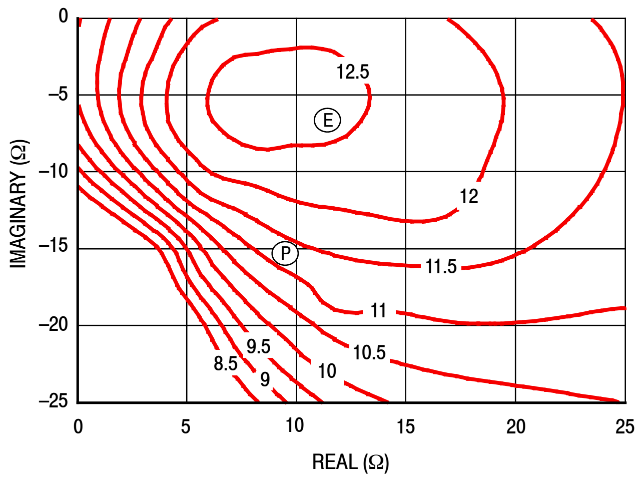


Figure 23. P3dB Load Pull Gain Contours (dB)

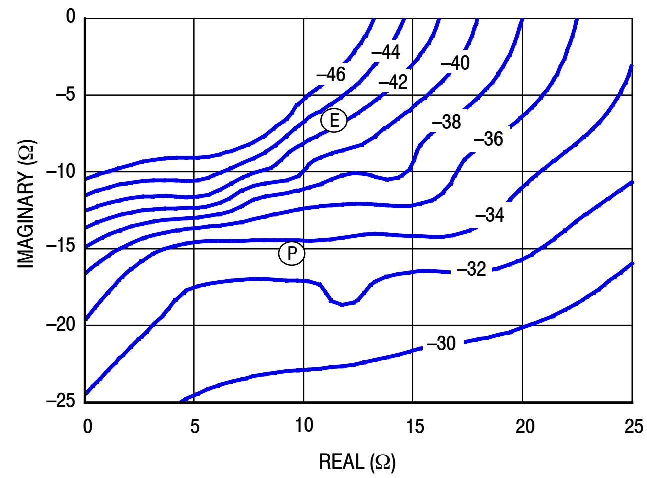


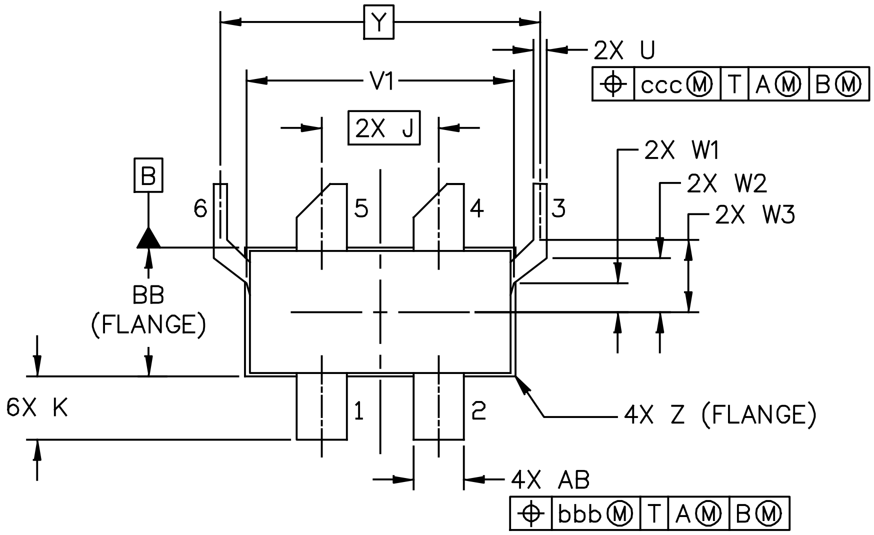
Figure 24. P3dB Load Pull AM/PM Contours (°)

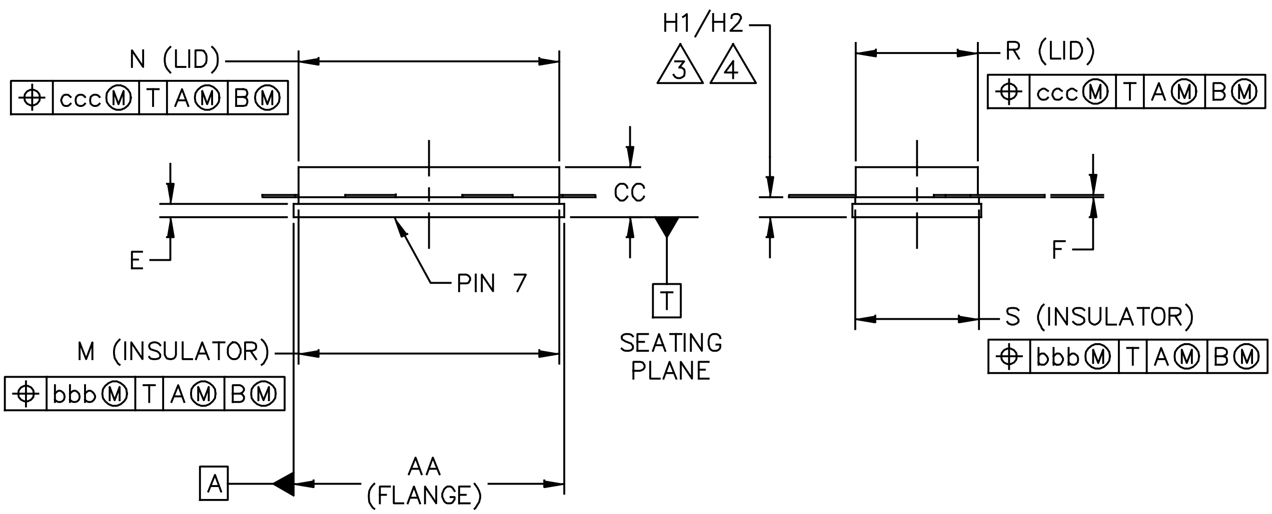
NOTE: Ⓟ = Maximum Output Power

Ⓔ = Maximum Drain Efficiency

Gain
Drain Efficiency
Linearity
Output Power

PACKAGE DIMENSIONS





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NOTES:

1. CONTROLLING DIMENSION: INCH.

2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M-1994.

3. DIMENSIONS H1 AND H2 ARE MEASURED .030 INCH (0.762 MM) AWAY FROM FLANGE PARALLEL TO DATUM B. H1 APPLIES TO PINS 1, 2, 4 & 5. H2 APPLIES TO PINS 3 & 6.

4. TOLERANCE OF DIMENSION H2 IS TENTATIVE.

DIM	INCH MIN	INCH MAX	MILLIMETER MIN	MILLIMETER MAX	DIM	INCH MIN	INCH MAX	MILLIMETER MIN	MILLIMETER MAX
AA	.805	.815	20.45	20.70	R	.365	.375	9.27	9.53
BB	.380	.390	9.65	9.91	S	.365	.375	9.27	9.53
CC	.125	.170	3.18	4.32	U	.035	.045	0.89	1.14
E	.035	.045	0.89	1.14	V1	.795	.805	20.19	20.45
F	.004	.007	0.10	0.18	W1	.080	.090	2.03	2.29
H1	.057	.067	1.45	1.70	W2	.155	.165	3.94	4.19
H2	.054	.070	1.37	1.78	W3	.210	.220	5.33	5.59
J	.350 BSC		8.89 BSC		Y	.956 BSC		24.28 BSC	
K	.170	.210	4.32	5.33	Z	R.000	R.040	R0.00	R1.02
M	.774	.786	19.66	19.96	AB	.145	.155	3.68	3.94
N	.772	.788	19.61	20.02	aaa	.005		0.13	
					bbb	.010		0.25	
					ccc	.015		0.38	

MECHANICAL OUTLINE

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16 JAN 2014

PRODUCT DOCUMENTATION, SOFTWARE AND TOOLS

Refer to the following resources to aid your design process.

Application Notes

- AN1955: Thermal Measurement Methodology of RF Power Amplifiers

Engineering Bulletins

- EB212: Using Data Sheet Impedances for RF LDMOS Devices

Software

- Electromigration MTTF Calculator
- RF High Power Model
- .s2p File

Development Tools

- Printed Circuit Boards

For Software and Tools, do a Part Number search at http://www.freescale.com, and select the “Part Number” link. Go to the Software & Tools tab on the part’s Product Summary page to download the respective tool.

REVISION HISTORY

The following table summarizes revisions to this document.

Revision	Date	Description
0	Aug. 2014	• Initial Release of Data Sheet

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