BUJ302AX

NPN power transistor

Rev. 02 — 28 March 2011 Product data sheet

1. Product profile

1.1 General description

High-voltage, high-speed planar-passivated NPN power switching transistor in a SOT186A (TO-220F) plastic package.

1.2 Features and benefits

- Fast switching
- High voltage capability
- Isolated package
- Low thermal resistance

1.3 Applications

- DC-to-DC converters
- High-frequency electronic lighting ballast applications
- Inverters
- Motor control systems

1.4 Quick reference data

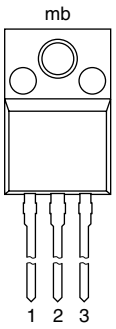
Table 1. Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I_C	collector current	see Figure 1; see Figure 2; see Figure 4	-	-	4	A
P_{tot}	total power dissipation	$T_h \leq 25$ °C; see Figure 3	-	-	26	W
V_{CESM}	collector-emitter peak voltage	$V_{BE} = 0$ V	-	-	1050	V
Static characteristics						
h_{FE}	DC current gain	$I_C = 0.1$ A; $V_{CE} = 5$ V; $T_h = 25$ °C; see Figure 11	48	66	100	
		$I_C = 0.8$ A; $V_{CE} = 3$ V; $T_h = 25$ °C; see Figure 12	25	42	50	

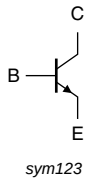
2. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	B	base		
2	C	collector		
3	E	emitter		
mb	n.c.	isolated		



SOT186A (TO-220F)



sym123

3. Ordering information

Table 3. Ordering information

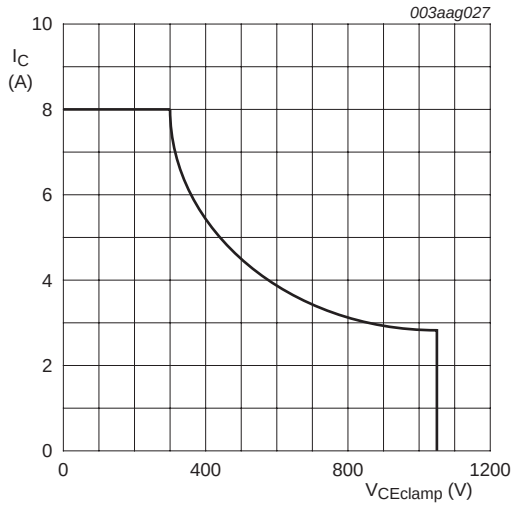
Type number	Package		
	Name	Description	Version
BUJ302AX	TO-220F	plastic single-ended package; isolated heatsink mounted; 1 mounting hole; 3-lead TO-220 "full pack"	SOT186A

4. Limiting values

Table 4. Limiting values

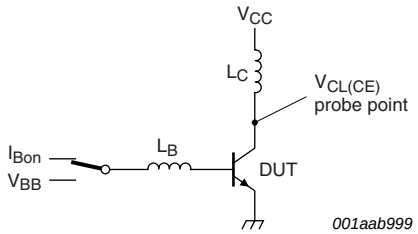
In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CESM}	collector-emitter peak voltage	V_{BE} = 0 V	-	1050	V
V_{CEO}	collector-emitter voltage	I_B = 0 A	-	400	V
I_C	collector current	see Figure 1; see Figure 2; see Figure 4	-	4	A
I_{CM}	peak collector current		-	8	A
I_B	base current	DC	-	2	A
I_{BM}	peak base current		-	4	A
P_{tot}	total power dissipation	$T_h \leq 25$ °C; see Figure 3	-	26	W
T_{stg}	storage temperature		-65	150	°C
T_j	junction temperature		-	150	°C
V_{EBO}	emitter-base voltage	I_C = 0 A; I_E = 2 A; t_p < 10 ms	-	24	V



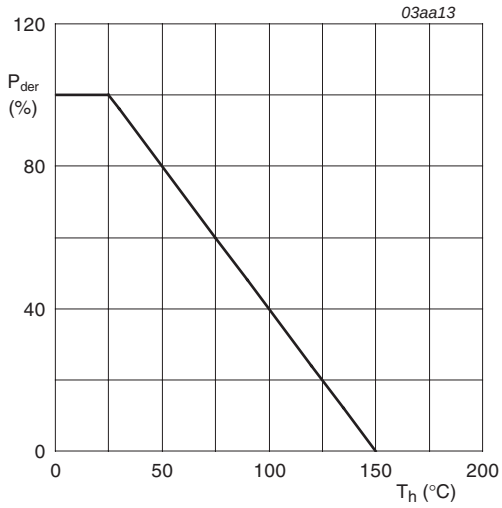
$T_j \leq T_{j(max)}$ °C

Fig 1. Reverse bias safe operating area



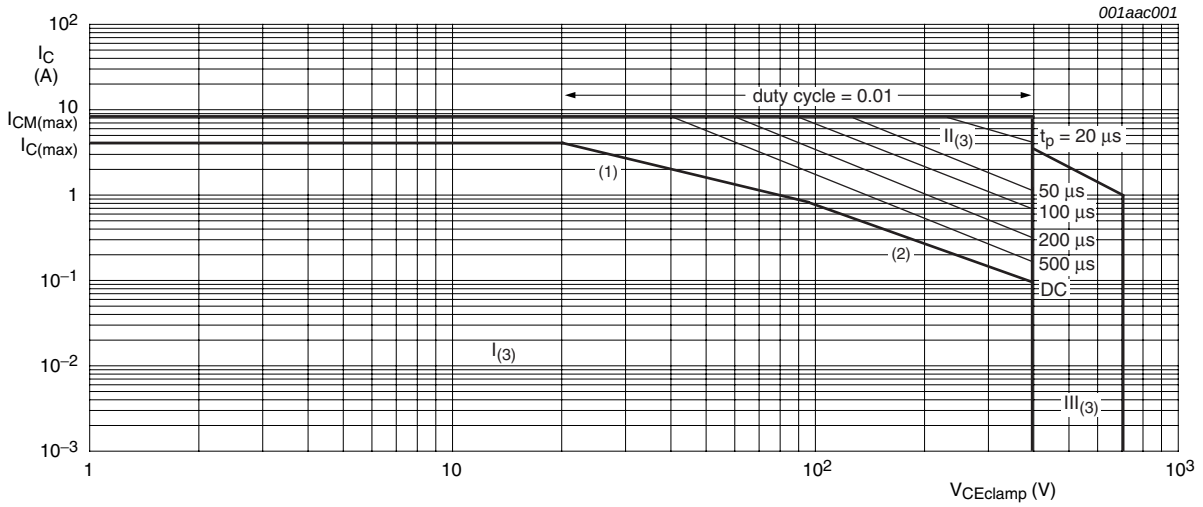
$V_{CL(CE)} \leq 1000\ V; V_{CC} = 150\ V; V_{BB} = -5\ V;$
$L_B = 1\ \mu H; L_C = 200\ \mu H$

Fig 2. Test circuit for reverse bias safe operating area



$$P_{der} = \frac{P_{tot}}{P_{tot(25°C)}} \times 100\ \%$$

Fig 3. Normalized total power dissipation as a function of heatsink temperature



1)Ptot maximum and Ptot peak maximum lines

2)Second breakdown limits

3) I = Region of permissable DC operation

II = Extension for repetitive pulse operation

III = Extension during turn-on in single transistor converters provided that RBE ≤ 100 Ω and tp ≤ 0.6 µs

Fig 4. Forward bias safe operating area for Tmb ≤ 25 °C

5. Thermal characteristics

Table 5. Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-h)}$	thermal resistance from junction to heatsink	with heatsink compound; see Figure 5	-	-	4.8	K/W
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air	-	55	-	K/W

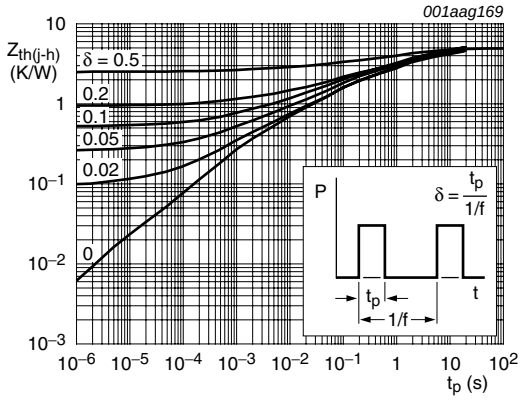


Fig 5. Transient thermal impedance from junction to heatsink as a function of pulse duration

6. Isolation characteristics

Table 6. Isolation characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{isol(RMS)}$	RMS isolation voltage	50 Hz ≤ f ≤ 60 Hz; RH ≤ 65 %; T_h = 25 °C; from all terminals to external heatsink; clean and dust free	-	-	2500	V
C_{isol}	isolation capacitance	from collector to external heatsink ; f = 1 MHz; T_h = 25 °C	-	10	-	pF

7. Characteristics

Table 7. Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static characteristics						
I_{CES}	collector-emitter cut-off current	V_{BE} = 0 V; V_{CE} = 1050 V; T_j = 25 °C	-	0.2	10	µA
I_{CEO}	collector-emitter cut-off current	V_{CE} = 400 V; I_B = 0 A; T_h = 25 °C	-	10	250	µA
$V_{(BR)EBO}$	open-collector emitter-base breakdown voltage	I_B = 1 mA; I_C = 0 A; T_h = 25 °C	15	19	-	V
V_{CEOsus}	collector-emitter sustaining voltage	I_B = 0 A; I_C = 10 mA; L_C = 25 mH; T_h = 25 °C; see Figure 6; see Figure 7	400	470	-	V
V_{CEsat}	collector-emitter saturation voltage	I_C = 1 A; I_B = 0.2 A; T_h = 25 °C; see Figure 8; see Figure 9	-	0.15	0.5	V
		I_C = 3.5 A; I_B = 1 A; T_h = 25 °C; see Figure 8; see Figure 9	-	0.6	1.5	V
V_{BEsat}	base-emitter saturation voltage	I_C = 3.5 A; I_B = 1 A; T_h = 25 °C; see Figure 10	-	1.1	1.5	V
h_{FE}	DC current gain	I_C = 0.1 A; V_{CE} = 5 V; T_h = 25 °C; see Figure 11	48	66	100	
		I_C = 0.8 A; V_{CE} = 3 V; T_h = 25 °C; see Figure 12	25	42	50	
Dynamic characteristics						
t_s	storage time	I_C = 2.5 A; I_{Bon} = 0.5 A; I_{Boff} = -0.5 A; R_L = 60 Ω; V_{BB} = -5 V; T_h = 25 °C; resistive load; t_p = 300 µs; see Figure 13; see Figure 14	-	-	3.5	µs
t_f	fall time		-	-	500	ns

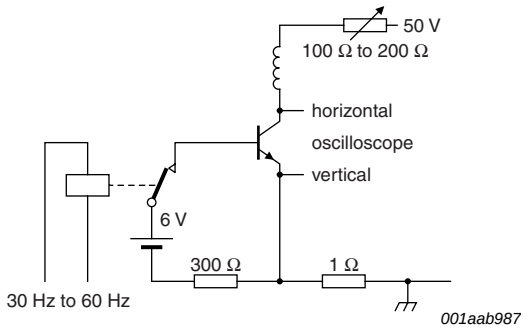


Fig 6. Test circuit for collector-emitter sustaining voltage

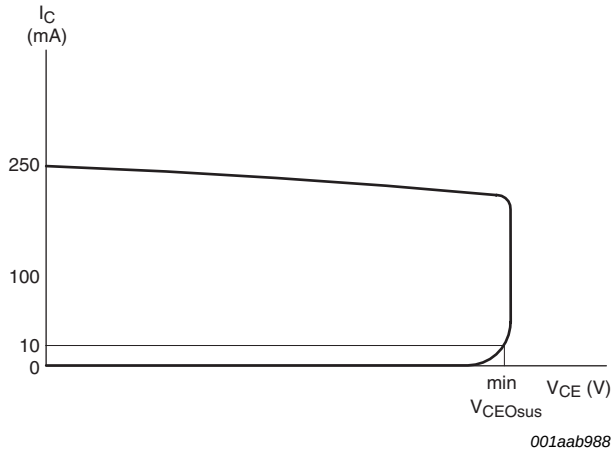


Fig 7. Oscilloscope display for collector-emitter sustaining voltage test waveform

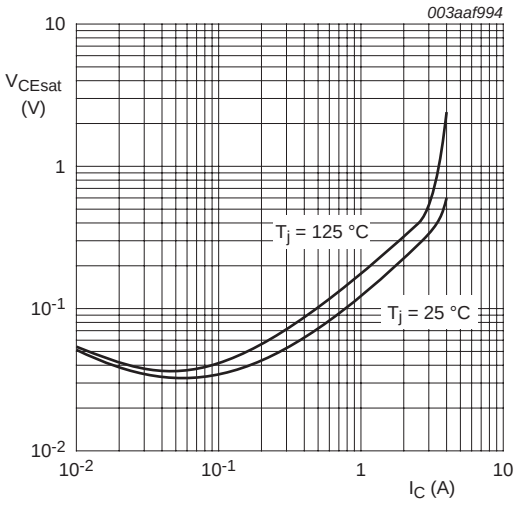


Fig 8. Collector-emitter saturation voltage as a function of collector current; typical values

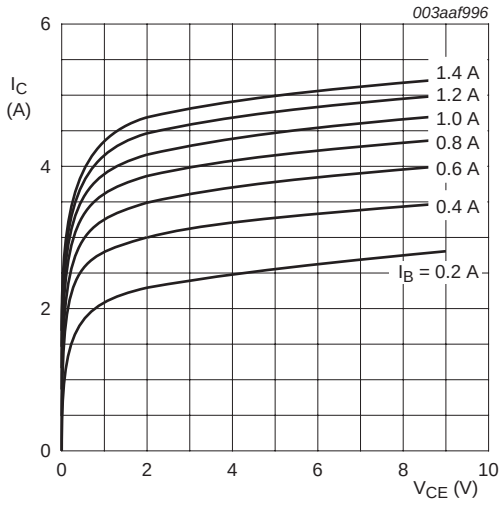


Fig 9. Collector current as a function of collector-emitter voltage; typical values

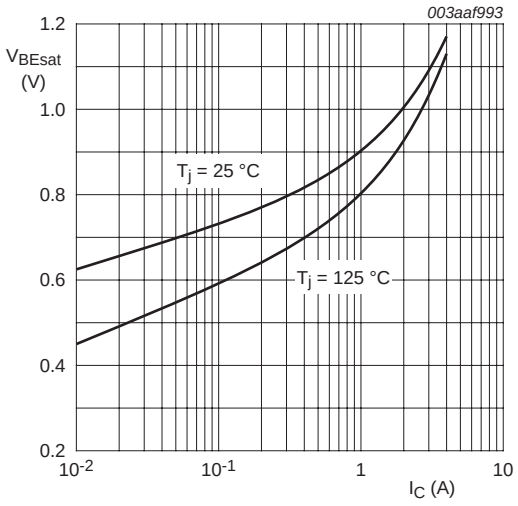


Fig 10. Base-emitter saturation voltage as a function of collector current; typical values

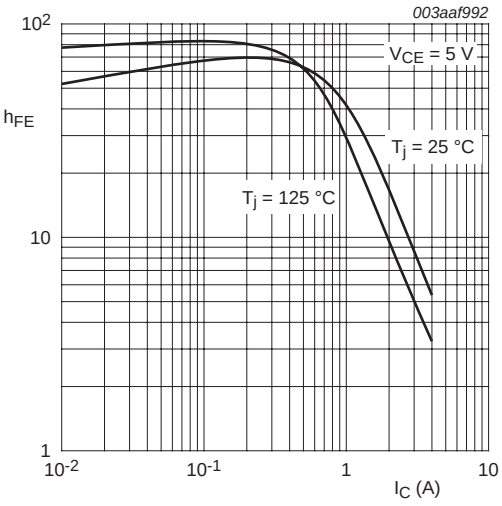


Fig 11. DC current gain as a function of collector current; typical values

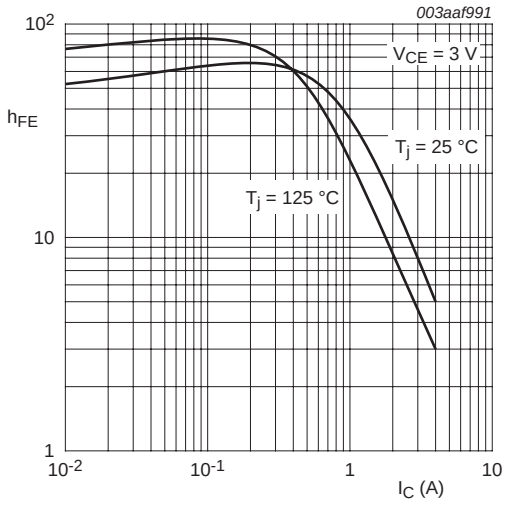
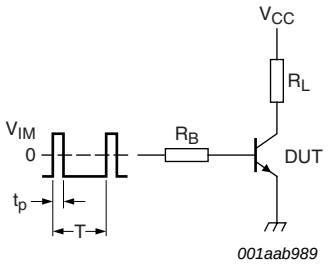


Fig 12. DC current gain as a function of collector current; typical values



$V_{IM} = -6$ to $+8\ V$; $V_{CC} = 250\ V$; $t_p = 20\ \mu s$; $\delta = \frac{t_p}{T} = 0.01$

R_B and R_L calculated from I_{Con} and I_{Bon} requirements.

Fig 13. Test circuit for resistive load switching

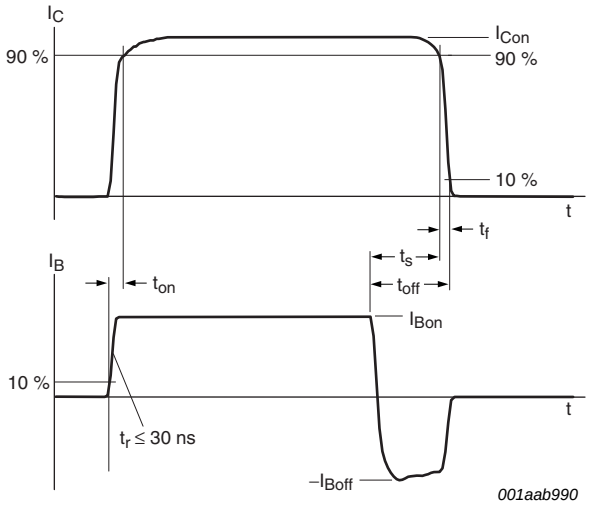
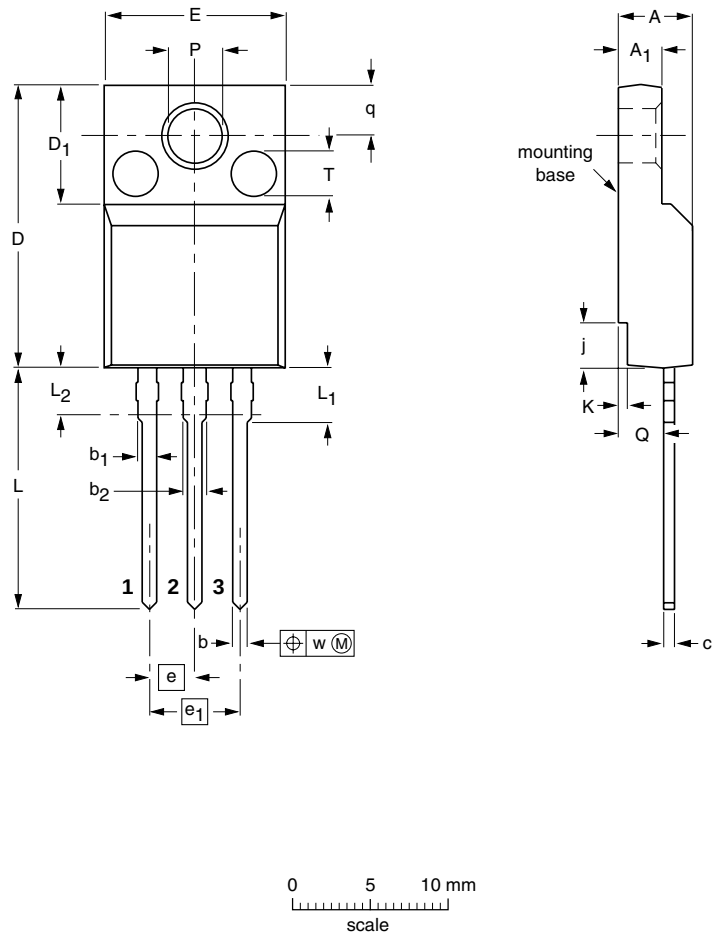


Fig 14. Switching times waveforms for resistive load

8. Package outline

Plastic single-ended package; isolated heatsink mounted;
1 mounting hole; 3-lead TO-220 'full pack'

SOT186A



DIMENSIONS (mm are the original dimensions)

UNIT	A	A_1	b	b_1	b_2	c	D	D_1	E	e	e_1	j	K	L	L_1	L_2 (1) max.	P	Q	q	T (2)	w
mm	4.6 4.0	2.9 2.5	0.9 0.7	1.1 0.9	1.4 1.0	0.7 0.4	15.8 15.2	6.5 6.3	10.3 9.7	2.54	5.08	2.7 1.7	0.6 0.4	14.4 13.5	3.30 2.79	3	3.2 3.0	2.6 2.3	3.0 2.6	2.5	0.4

Notes

1. Terminal dimensions within this zone are uncontrolled.
2. Both recesses are ∅ 2.5 × 0.8 max. depth

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT186A		3-lead TO-220F				~~02-04-09~~ 06-02-14

Fig 15. Package outline SOT186A (TO-220F)

9. Revision history

Table 8. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
BUJ302AX v.2	20110328	Product data sheet	-	BUJ302AX v.1
Modifications:	• The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors. • Legal texts have been adapted to the new company name where appropriate.			
BUJ302AX v.1	19980801	Objective specification	-	-

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10.1 Data sheet status

Document status [1] [2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

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12. Contents

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