## 1. General description

Logic level N-channel MOSFET in an LFPAK56 (Power SO8) package using TrenchMOS technology. This product has been designed and qualified to AEC Q101 standard for use in high performance automotive applications.

#### 2. Features and benefits

- Q101 compliant
- Repetitive avalanche rated
- Suitable for thermally demanding environments due to 175 °C rating
- True logic level gate with V<sub>GS(th)</sub> rating of greater than 0.5 V at 175 °C

## 3. Applications

- 12 V Automotive systems
- Motors, lamps and solenoid control
- Transmission control
- Ultra high performance power switching

### 4. Quick reference data

Table 1. Quick reference data

| Symbol                  | Parameter                        | Conditions  |  | Min | Тур  | Max | Unit |  |
|-------------------------|----------------------------------|---|--|-----|------|-----|------|--|
| V <sub>DS</sub>         | drain-source voltage             | T <sub>j</sub> ≥ 25 °C; T <sub>j</sub> ≤ 175 °C   |  | -   | -    | 40  | V    |  |
| I <sub>D</sub>          | drain current                    | V <sub>GS</sub> = 5 V; T <sub>mb</sub> = 25 °C; <u>Fig. 1</u>   |  | -   | -    | 52  | Α    |  |
| P <sub>tot</sub>        | total power dissipation          | T <sub>mb</sub> = 25 °C; <u>Fig. 2</u>  |  | -   | -    | 65  | W    |  |
| Static characte         | Static characteristics           |   |  |     |      |     |      |  |
| R <sub>DSon</sub>       | drain-source on-state resistance | $V_{GS} = 5 \text{ V}; I_D = 15 \text{ A}; T_j = 25 \text{ °C}; Fig. 11$  |  | -   | 11.2 | 12  | mΩ   |  |
| Dynamic characteristics |                                  |   |  |     |      |     |      |  |
| $Q_{GD}$                | gate-drain charge                | $V_{GS} = 5 \text{ V}; I_D = 15 \text{ A}; V_{DS} = 32 \text{ V};$<br>$T_j = 25 \text{ °C}; \underline{\text{Fig. 13}}; \underline{\text{Fig. 14}}$ |  | -   | 3.4  | -   | nC   |  |





### N-channel 40 V, 12 m $\Omega$ logic level MOSFET in LFPAK56

## 5. Pinning information

Table 2. Pinning information

| Pin | Symbol | Description                       | Simplified outline                         | Graphic symbol |
|-----|--------|-----------------------------------|--|----------------|
| 1   | S      | source                            | mb   | D<br>I         |
| 2   | S      | source                            |  |                |
| 3   | S      | source                            | [qj  | G T T          |
| 4   | G      | gate                              | <u>o o o o</u>                             | mbb076 S       |
| mb  | D      | mounting base; connected to drain | 1 2 3 4<br>LFPAK56; Power-<br>SO8 (SOT669) |                |

# 6. Ordering information

Table 3. Ordering information

| Type number | Package               |  |         |  |  |
|-------------|-----------------------|--|---------|--|--|
|             | Name                  | Description  | Version |  |  |
| BUK9Y12-40E | LFPAK56;<br>Power-SO8 | Plastic single-ended surface-mounted package (LFPAK56; Power-SO8); 4 leads | SOT669  |  |  |

# 7. Marking

Table 4. Marking codes

| Type number | Marking code |
|-------------|--------------|
| BUK9Y12-40E | 91240E       |

# 8. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

| Symbol           | Parameter               | Conditions   |        | Min | Max  | Unit |
|------------------|-------------------------|--|--------|-----|------|------|
| V <sub>DS</sub>  | drain-source voltage    | T <sub>j</sub> ≥ 25 °C; T <sub>j</sub> ≤ 175 °C                |        | -   | 40   | V    |
| $V_{DGR}$        | drain-gate voltage      | $R_{GS}$ = 20 k $\Omega$                                       |        | -   | 40   | V    |
| $V_{GS}$         | gate-source voltage     | T <sub>j</sub> ≤ 175 °C; DC                                    |        | -10 | 10   | V    |
|                  |                         | T <sub>j</sub> ≤ 175 °C; Pulsed                                | [1][2] | -15 | 15   | V    |
| I <sub>D</sub>   | drain current           | T <sub>mb</sub> = 25 °C; V <sub>GS</sub> = 5 V; <u>Fig. 1</u>  |        | -   | 52   | Α    |
|                  |                         | T <sub>mb</sub> = 100 °C; V <sub>GS</sub> = 5 V; <u>Fig. 1</u> |        | -   | 36.7 | Α    |
| I <sub>DM</sub>  | peak drain current      | $T_{mb}$ = 25 °C; pulsed; $t_p \le 10 \mu s$ ; Fig. 4          |        | -   | 208  | Α    |
| P <sub>tot</sub> | total power dissipation | T <sub>mb</sub> = 25 °C; <u>Fig. 2</u>                         |        | -   | 65   | W    |

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| Symbol               | Parameter                                    | Conditions  |        | Min | Max | Unit |
|----------------------|--|---|--------|-----|-----|------|
| T <sub>stg</sub>     | storage temperature                          |   |        | -55 | 175 | °C   |
| T <sub>j</sub>       | junction temperature                         |   |        | -55 | 175 | °C   |
| Source-drain diode   |  |   |        |     |     |      |
| I <sub>S</sub>       | source current                               | T <sub>mb</sub> = 25 °C   |        | -   | 52  | Α    |
| I <sub>SM</sub>      | peak source current                          | pulsed; $t_p \le 10 \ \mu s$ ; $T_{mb} = 25 \ ^{\circ}C$  |        | -   | 208 | Α    |
| Avalanche ruggedness |  |   |        |     |     |      |
| E <sub>DS(AL)S</sub> | non-repetitive drain-source avalanche energy | $I_D$ = 52 A; $V_{sup} \le 40$ V; $R_{GS}$ = 50 Ω; $V_{GS}$ = 5 V; $T_{j(init)}$ = 25 °C; unclamped; Fig. 3 | [3][4] | -   | 23  | mJ   |

- [1] Accumulated pulse duration up to 50 hours delivers zero defect ppm
- [2] Significantly longer life times are achieved by lowering T<sub>i</sub> and or V<sub>GS</sub>
- [3] Single-pulse avalanche rating limited by maximum junction temperature of 175 °C.
- [4] Refer to application note AN10273 for further information.

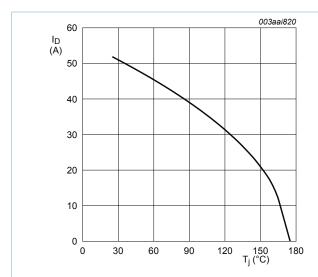


Fig. 1. Continuous drain current as a function of mounting base temperature

$$V_{GS} \ge 5V$$

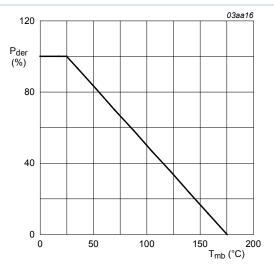


Fig. 2. Normalized total power dissipation as a function of mounting base temperature

$$P_{der} = \frac{P_{tot}}{P_{tot(25^{\circ}C)}} \times 100 \%$$

#### N-channel 40 V, 12 mΩ logic level MOSFET in LFPAK56

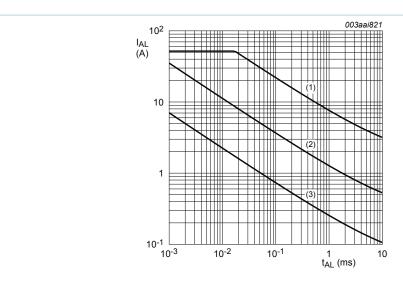
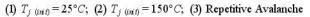


Fig. 3. Avalanche rating; avalanche current as a function of avalanche time



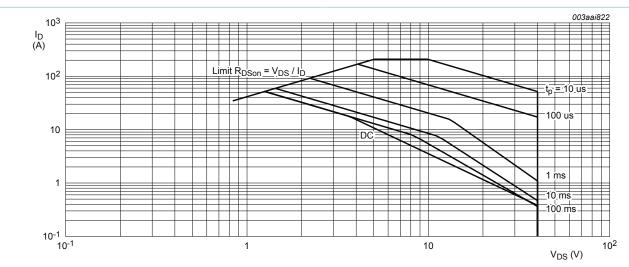


Fig. 4. Safe operating area; continuous and peak drain currents as a function of drain-source voltage

 $T_{mb} = 25^{\circ}C$ ;  $I_{DM}$  is a single pulse

### 9. Thermal characteristics

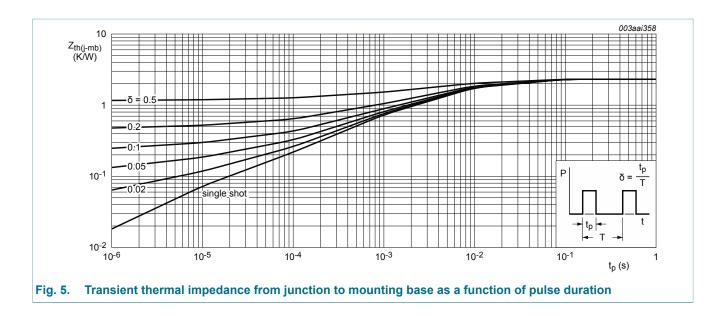
Table 6. Thermal characteristics

| Symbol                | Parameter   | Conditions | Min | Тур | Max  | Unit |
|-----------------------|---|------------|-----|-----|------|------|
| R <sub>th(j-mb)</sub> | thermal resistance<br>from junction to<br>mounting base | Fig. 5     | -   | _   | 2.31 | K/W  |

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### N-channel 40 V, 12 m $\Omega$ logic level MOSFET in LFPAK56



## 10. Characteristics

Table 7. Characteristics

| Symbol               | Parameter                     | Conditions   | Min | Тур  | Max  | Unit |
|----------------------|-------------------------------|--|-----|------|------|------|
| Static chara         | acteristics                   |  | 1   |      |      |      |
| V <sub>(BR)DSS</sub> | drain-source                  | $I_D = 250 \mu A; V_{GS} = 0 V; T_j = 25 ^{\circ}C$  | 40  | -    | -    | V    |
|                      | breakdown voltage             | $I_D = 250 \mu A; V_{GS} = 0 V; T_j = -55 °C$  | 36  | -    | -    | V    |
| $V_{GS(th)}$         | gate-source threshold voltage | $I_D$ = 1 mA; $V_{DS}$ = $V_{GS}$ ; $T_j$ = 25 °C;<br>Fig. 9; Fig. 10                      | 1.4 | 1.7  | 2.1  | V    |
|                      |                               | $I_D$ = 1 mA; $V_{DS}$ = $V_{GS}$ ; $T_j$ = -55 °C;<br>Fig. 9                              | -   | -    | 2.45 | V    |
|                      |                               | $I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = 175 \text{ °C};$<br>Fig. 9                     | 0.5 | -    | -    | V    |
| I <sub>DSS</sub>     | drain leakage current         | V <sub>DS</sub> = 40 V; V <sub>GS</sub> = 0 V; T <sub>j</sub> = 25 °C                      | -   | 0.03 | 1    | μA   |
|                      |                               | V <sub>DS</sub> = 40 V; V <sub>GS</sub> = 0 V; T <sub>j</sub> = 175 °C                     | -   | -    | 500  | μΑ   |
| I <sub>GSS</sub>     | gate leakage current          | V <sub>GS</sub> = 10 V; V <sub>DS</sub> = 0 V; T <sub>j</sub> = 25 °C                      | -   | 2    | 100  | nA   |
|                      |                               | V <sub>GS</sub> = -10 V; V <sub>DS</sub> = 0 V; T <sub>j</sub> = 25 °C                     | -   | 2    | 100  | nA   |
| R <sub>DSon</sub>    | drain-source on-state         | V <sub>GS</sub> = 5 V; I <sub>D</sub> = 15 A; T <sub>j</sub> = 25 °C; <u>Fig. 11</u>       | -   | 11.2 | 12   | mΩ   |
|                      | resistance                    | V <sub>GS</sub> = 10 V; I <sub>D</sub> = 15 A; T <sub>j</sub> = 25 °C;<br>Fig. 11          | -   | 8.8  | 10   | mΩ   |
|                      |                               | V <sub>GS</sub> = 5 V; I <sub>D</sub> = 15 A; T <sub>j</sub> = 175 °C;<br>Fig. 11; Fig. 12 | -   | -    | 24.1 | mΩ   |
| Dynamic ch           | naracteristics                |  | 1   |      |      |      |
| Q <sub>G(tot)</sub>  | total gate charge             | I <sub>D</sub> = 15 A; V <sub>DS</sub> = 32 V; V <sub>GS</sub> = 5 V;                      | -   | 9.8  | -    | nC   |
| Q <sub>GS</sub>      | gate-source charge            | T <sub>j</sub> = 25 °C; <u>Fig. 13</u> ; <u>Fig. 14</u>                                    | -   | 3.2  | -    | nC   |

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| Symbol              | Parameter                    | Conditions  | Min | Тур  | Max  | Unit |
|---------------------|------------------------------|---|-----|------|------|------|
| $Q_{GD}$            | gate-drain charge            |   | -   | 3.4  | -    | nC   |
| C <sub>iss</sub>    | input capacitance            | V <sub>GS</sub> = 0 V; V <sub>DS</sub> = 25 V; f = 1 MHz;                         | -   | 1067 | 1423 | pF   |
| C <sub>oss</sub>    | output capacitance           | T <sub>j</sub> = 25 °C; <u>Fig. 15</u>  | -   | 169  | 203  | pF   |
| C <sub>rss</sub>    | reverse transfer capacitance |   | -   | 88   | 120  | pF   |
| t <sub>d(on)</sub>  | turn-on delay time           | $V_{DS} = 30 \text{ V}; R_L = 2 \Omega; V_{GS} = 5 \text{ V};$                    | -   | 9    | -    | ns   |
| t <sub>r</sub>      | rise time                    | $R_{G(ext)} = 5 \Omega; T_j = 25 ^{\circ}C$                                       | -   | 13   | -    | ns   |
| t <sub>d(off)</sub> | turn-off delay time          |   | -   | 13   | -    | ns   |
| t <sub>f</sub>      | fall time                    |   | -   | 9    | -    | ns   |
| Source-dra          | in diode                     |   |     |      | '    |      |
| $V_{SD}$            | source-drain voltage         | $I_S = 15 \text{ A}; V_{GS} = 0 \text{ V}; T_j = 25 ^{\circ}\text{C}; Fig. 16$    | -   | 0.86 | 1.2  | V    |
| t <sub>rr</sub>     | reverse recovery time        | $I_S = 15 \text{ A}; dI_S/dt = -100 \text{ A/}\mu\text{s}; V_{GS} = 0 \text{ V};$ | -   | 15   | -    | ns   |
| Q <sub>r</sub>      | recovered charge             | $V_{DS} = 25 \text{ V}; T_j = 25 \text{ °C}$                                      | -   | 6    | -    | nC   |

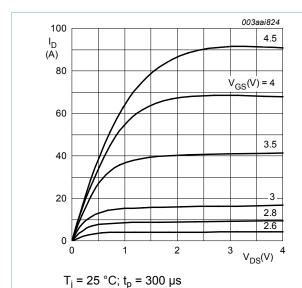


Fig. 6. Output characteristics; drain current as a function of drain-source voltage; typical values

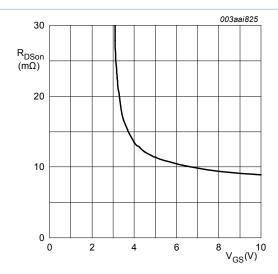


Fig. 7. Drain-source on-state resistance as a function of gate-source voltage; typical values

$$T_j = 25$$
°C;  $I_D = 15A$ 

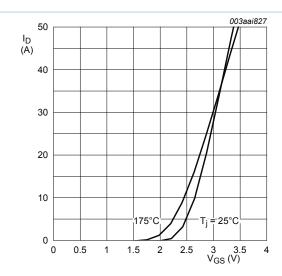


Fig. 8. Transfer characteristics; drain current as a function of gate-source voltage; typical values



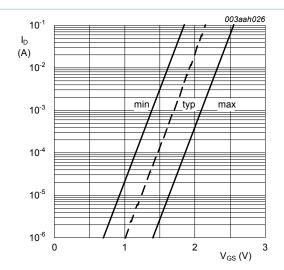


Fig. 10. Sub-threshold drain current as a function of gate-source voltage

$$T_j = 25$$
°C;  $V_{DS} = 5V$ 

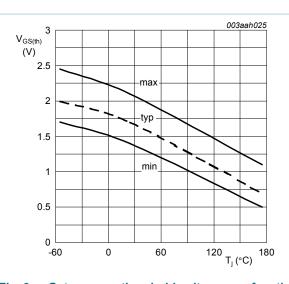
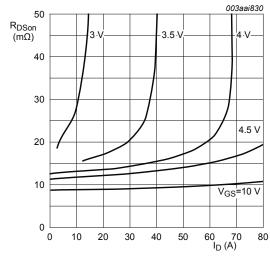


Fig. 9. Gate-source threshold voltage as a function of junction temperature

$$I_D = 1$$
 mA;  $V_{DS} = V_{GS}$ 



 $T_i = 25 \, ^{\circ}\text{C}; t_p = 300 \, \mu\text{s}$ 

Fig. 11. Drain-source on-state resistance as a function of drain current; typical values

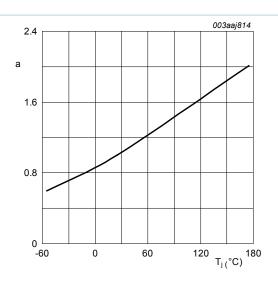


Fig. 12. Normalized drain-source on-state resistance factor as a function of junction temperature

$$a = \frac{R_{DSon}}{R_{DSon (25^{\circ}C)}}$$

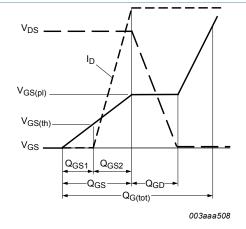


Fig. 14. Gate charge waveform definitions

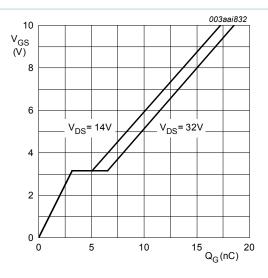


Fig. 13. Gate-source voltage as a function of gate charge; typical values

$$T_j = 25$$
°C;  $I_D = 15A$ 

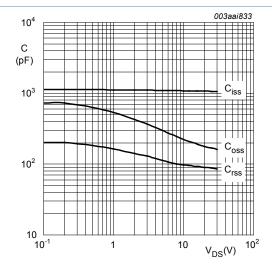


Fig. 15. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values

$$V_{GS} = \mathbf{0}V; f = \mathbf{1}MHz$$

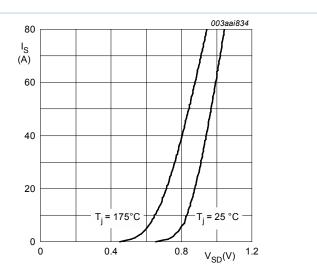
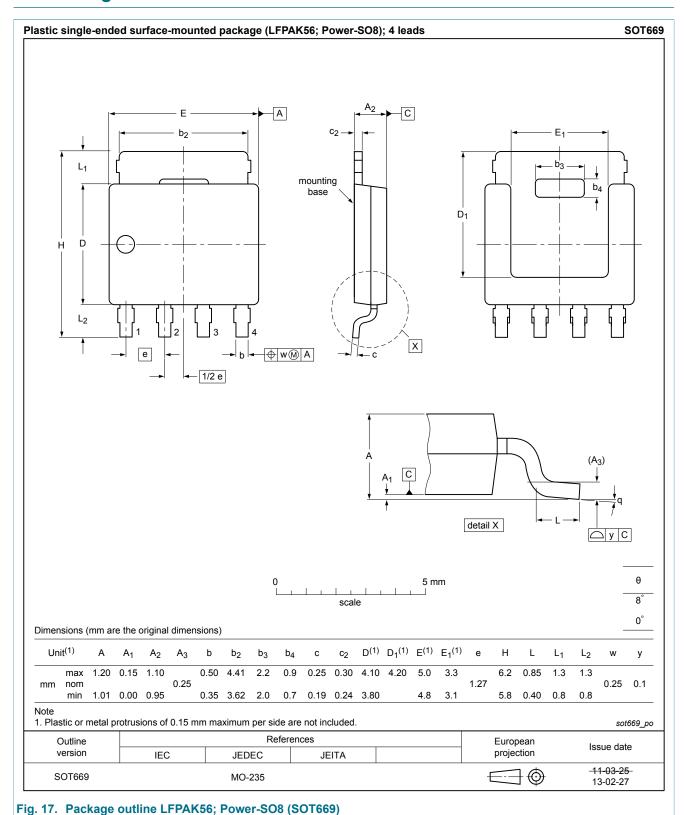


Fig. 16. Source-drain (diode forward) current as a function of source-drain (diode forward) voltage; typical values

$$V_{GS} = 0V$$

#### N-channel 40 V, 12 mΩ logic level MOSFET in LFPAK56

## 11. Package outline



### N-channel 40 V, 12 m $\Omega$ logic level MOSFET in LFPAK56

## 12. Legal information

#### 12.1 Data sheet status

| Document status [1][2]               | Product status [3] | Definition  |
|--------------------------------------|--------------------|---|
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#### N-channel 40 V, 12 m $\Omega$ logic level MOSFET in LFPAK56

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# N-channel 40 V, 12 mΩ logic level MOSFET in LFPAK56

**BUK9Y12-40E** 

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