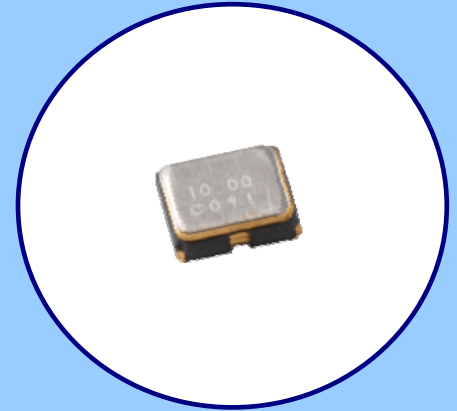




**FEATURES**

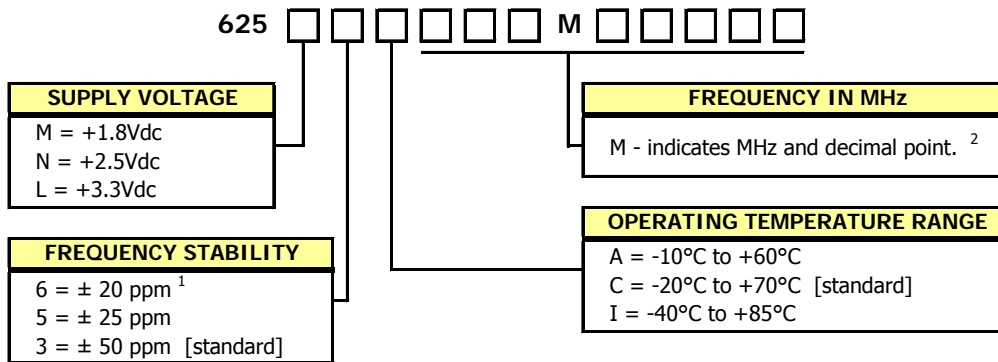
- Standard 2.5mm x 2.0mm 4-Pad Surface Mount Package
- HCMOS Output
- Fundamental and 3<sup>rd</sup> Overtone Crystal Designs
- Frequency Range 1 – 110 MHz
- Frequency Stability ±50 ppm Standard, ±25 ppm and ±20 ppm Available
- Operating Voltages +1.8Vdc, +2.5Vdc or +3.3Vdc
- Operating Temperature to -40°C to +85°C
- Output Enable Standard
- Tape & Reel Packaging Standard, EIA-418
- **RoHS/Green Compliant [6/6]**



**APPLICATIONS**

Model 625 is ideal for applications; such as broadband access, Ethernet/Gigabit Ethernet, microprocessors/DSP/FPGA, networking equipment computers and peripherals, digital video, cameras and other portable devices.

**ORDERING INFORMATION**

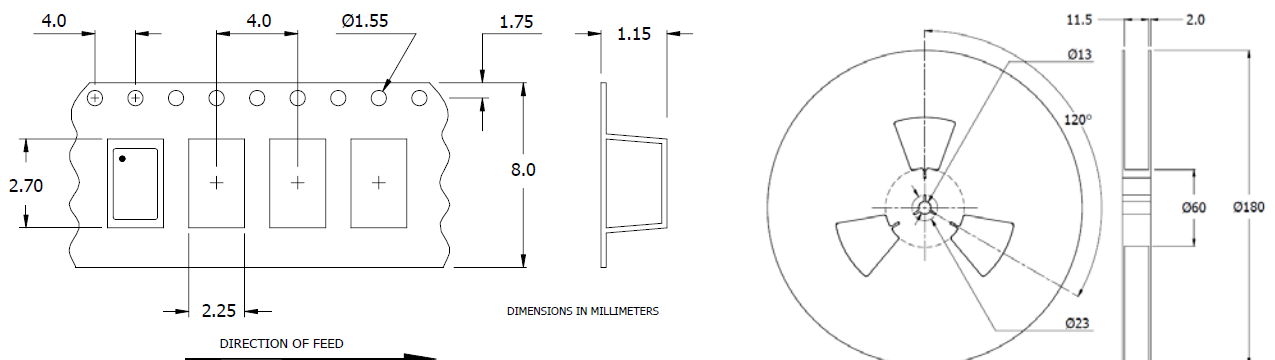


1] Consult factory for 6I Stability/Temperature availability.  
 2] Frequency is recorded with three leading significant digits before the 'M' and 5 significant digits after the 'M' (including zeros).  
 [Ex. 3.579545 MHz, code as 003M57954; 14.31818 MHz, code as 014M31818; 125 MHz, code as 125M00000]

**Not all performance combinations and frequencies may be available.  
 Contact your local CTS Representative or CTS Customer Service for availability.**

**PACKAGING INFORMATION [reference]**

Device quantity is 1k pcs. minimum and 3k pcs. maximum per 180mm reel. **8mm tape width.**



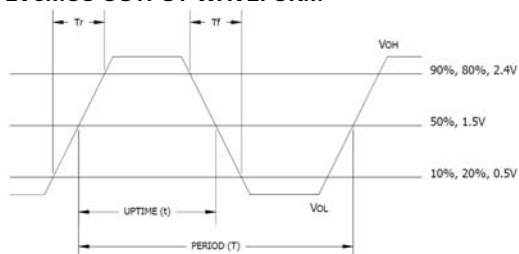
**ELECTRICAL CHARACTERISTICS**

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
Maximum Supply Voltage	$V_{CC}$	-	-0.5	-	4.0	V
Storage Temperature	$T_{STG}$	-	-40	-	+100	°C
Frequency Range	$f_o$	-	1.0	-	110	MHz
Frequency Stability [See Note 1 and Ordering Information]	$\Delta f/f_o$	-	-	-	20, 25, 50	± ppm
Aging	$\Delta f/f_o$	@+25°C, 1st year	-	-	3	± ppm
Operating Temperature						
Commercial	$T_A$	-	-10	+25	+60	°C
Industrial			-20		+70	
Supply Voltage	$V_{CC}$	±10%	1.62	1.8	1.98	V
Model 625M			2.25		2.75	
Model 625N			2.97		3.63	
Model 625L						
Supply Current	$I_{CC}$	$C_L = 15pF$				mA
Model 625M		1.0 MHz to 50 MHz	-	-	7	
[+1.8V]		50.1 MHz to 110 MHz	-	-	15	
Model 625N		1.0 MHz to 50 MHz	-	-	10	
[+2.5V]		50.1 MHz to 110 MHz	-	-	15	
Model 625L		1.0 MHz to 50 MHz	-	-	15	
[+3.3V]	50.1 MHz to 110 MHz	-	-	20		
Output Load	$C_L$		-	-	15	pF
Output Voltage Levels						
Logic '1' Level	$V_{OH}$	CMOS Load	90% $V_{CC}$	-	-	V
Logic '0' Level	$V_{OL}$	CMOS Load	-	-	10% $V_{CC}$	
Output Current						
Logic '1' Level [M,N,L]	$I_{OH}$	$V_{OH} = 90\%V_{CC}$ (1.8V, 2.5, 3.3V)	-	-	-2, -4, -8	mA
Logic '0' Level [M,N,L]	$I_{OL}$	$V_{OL} = 10\%V_{CC}$ (1.8V, 2.5, 3.3V)	-	-	+2, +4, +8	
Output Duty Cycle	SYM	@ 50% Level	45	-	55	%
Rise and Fall Time		@ 10% - 90% Levels, $C_L = 15pF$				
Model 625M	$T_R, T_F$	1.0 MHz to 20 MHz	-	-	5	ns
[+1.8V]		20.1 MHz to 110 MHz	-	-	4	
Model 625N		1.0 MHz to 20 MHz	-	-	4	
[+2.5V]		20.1 MHz to 110 MHz	-	-	3	
Model 625L		1.0 MHz to 20 MHz	-	-	3	
[+3.3V]		20.1 MHz to 110 MHz	-	-	2	
Start Up Time	$T_S$	Application of $V_{CC}$	-	2	5	ms
Enable Function						
Enable Input Voltage	$V_{IH}$	Pin 1 Logic '1', Output Enabled	0.7* $V_{CC}$	-	-	V
Disable Input Voltage	$V_{IL}$	Pin 1 Logic '0', Output Disabled	-	-	0.3* $V_{CC}$	
Enable Time [M,N,L]	$T_{PLZ}$	Pin 1 Logic '1'	-	-	5	ms
Standby Current	$I_{ST}$	Pin 1 Logic '0', Output Disabled	-	-	15	µA
Period Jitter, pk-pk	pjpk-pk	-	-	-	40	ps
Period Jitter, RMS	pjrms	-	-	-	25	
Phase Jitter, RMS	tjrms	Bandwidth 12 kHz - 20 MHz	-	-	1	

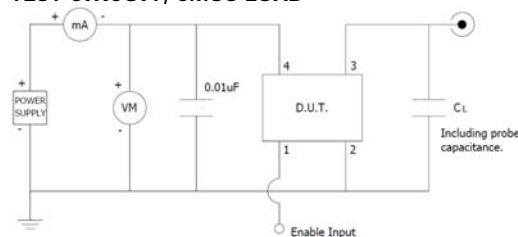
Notes:

- Inclusive of initial tolerance at time of shipment, changes in supply voltage, load, temperature and aging.

**LVC MOS OUTPUT WAVEFORM**



**TEST CIRCUIT, CMOS LOAD**

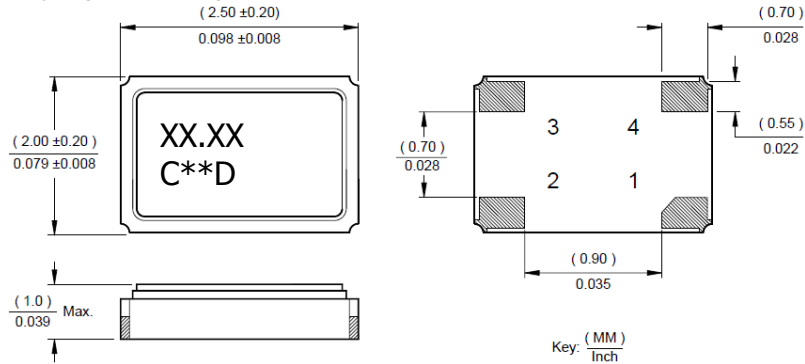


**ENABLE TRUTH TABLE**

PIN 1	PIN 3
Logic '1'	Output
Open	Output
Logic '0'	High Imp.

**MECHANICAL SPECIFICATIONS**

**PACKAGE DRAWING**



**MARKING INFORMATION**

1. XX.XX – Frequency in MHz.
2. C – CTS and Pin 1 identifier.
3. \*\* - Manufacturing Site Code.
4. D – Manufacturing Date Code.  
[See Table 1 for codes.]
5. Complete CTS part number, frequency value and date code information must appear on reel and carton labels.

**NOTES**

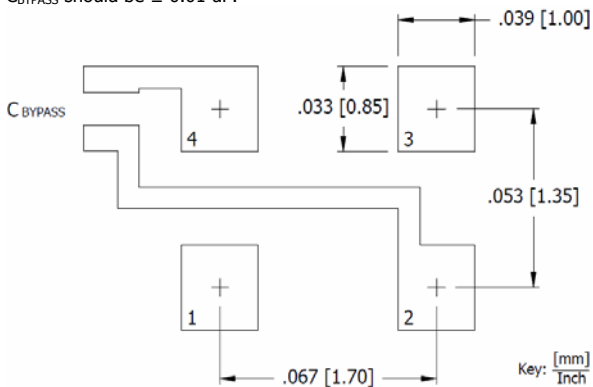
1. Termination pads [e4]. Barrier-plating is nickel [Ni] with gold [Au] flash plate.
2. Reflow conditions per JEDEC J-STD-020; 260°C maximum, 20 seconds.
3. MSL = 1.

**TABLE I**

YEAR \ MONTH					JAN	FEB	MAR	APR	MAY	JUN	JUL	AUG	SEP	OCT	NOV	DEC
					A	B	C	D	E	F	G	H	J	K	L	M
2001	2005	2009	2013	2017	A	B	C	D	E	F	G	H	J	K	L	M
2002	2006	2010	2014	2018	N	P	Q	R	S	T	U	V	W	X	Y	Z
2003	2007	2011	2015	2019	a	b	c	d	e	f	g	h	j	k	l	m
2004	2008	2012	2016	2020	n	p	q	r	s	t	u	v	w	x	y	z

**SUGGESTED SOLDER PAD GEOMETRY**

C<sub>BYPASS</sub> should be ≥ 0.01 uF.



**D.U.T. PIN ASSIGNMENTS**

PIN	SYMBOL	DESCRIPTION
1	EOH	Enable
2	GND	Circuit & Package Ground
3	Output	RF Output
4	V <sub>CC</sub>	Supply Voltage

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