Data Sheet

SCC1300-D02 COMBINED GYROSCOPE AND 3-AXIS ACCELEROMETER WITH DIGITAL SPI INTERFACES

Features

- ±100 °/s angular rate measurement range
- ±2 g 3-axis acceleration measurement range
- Angular rate measurement around X axis
- Angular rate sensor exceptionally insensitive to mechanical vibrations and shocks
- Superior bias stability for MEMS gyroscopes (<1°/h)
- Digital SPI interfacing
- Enhanced self diagnostics features
- Small size 8.5 x 18.7 x 4.5 mm (w x l x h)
- RoHS compliant robust packaging suitable for lead free soldering process and SMD mounting
- Proven capacitive 3D-MEMS technology
- Temperature range -40 °C...+125 °C

Applications

SCC1300-D02 is targeted to applications with high stability and tough environmental requirements. Typical applications are:

- Inertial Measurement Units (IMUs) for highly demanding environments
- Platform stabilization and control
- Motion analysis and control
- Roll over detection
- Robotic control systems
- Guidance systems
- Navigation systems

General Description

SCC1300-D02 is a combined high performance gyroscope and accelerometer component. The sensor is based on Murata's proven capacitive 3D-MEMS technology. The component integrates angular rate and acceleration sensing together with flexible separate digital SPI interfaces. Small robust packaging guarantees reliable operation over product lifetime. The housing is suitable for SMD mounting and the component is compatible with RoHS and ELV directives.

SCC1300-D02 is designed, manufactured and tested against high stability, reliability and quality requirements. The angular rate and acceleration sensors provide highly stable output over wide ranges of temperature and mechanical noise. The angular rate sensor bias stability is in the elite of MEMS gyros and it is also exceptionally insensitive to all mechanical vibrations and shocks. Component has several advanced self diagnostics features.

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1 General Description

1.1 Introduction

This document contains essential technical information for SCC1300 sensor. Specifications, SPI interface descriptions, user accessible register details, electrical properties and application information etc. This document should be used as a reference when designing in SCC1300 component.

1.2 General Product Description

The SCC1300 sensor consists of independent acceleration and angular rate sensing elements, and separate independent Application Specific Integrated Circuits (ASICs) used to sense and control those elements. Figure 1 represents an upper level block diagram of the component. Both ASICs have their own independent digital SPI interfaces used to control and read the accelerometer and the gyroscope.

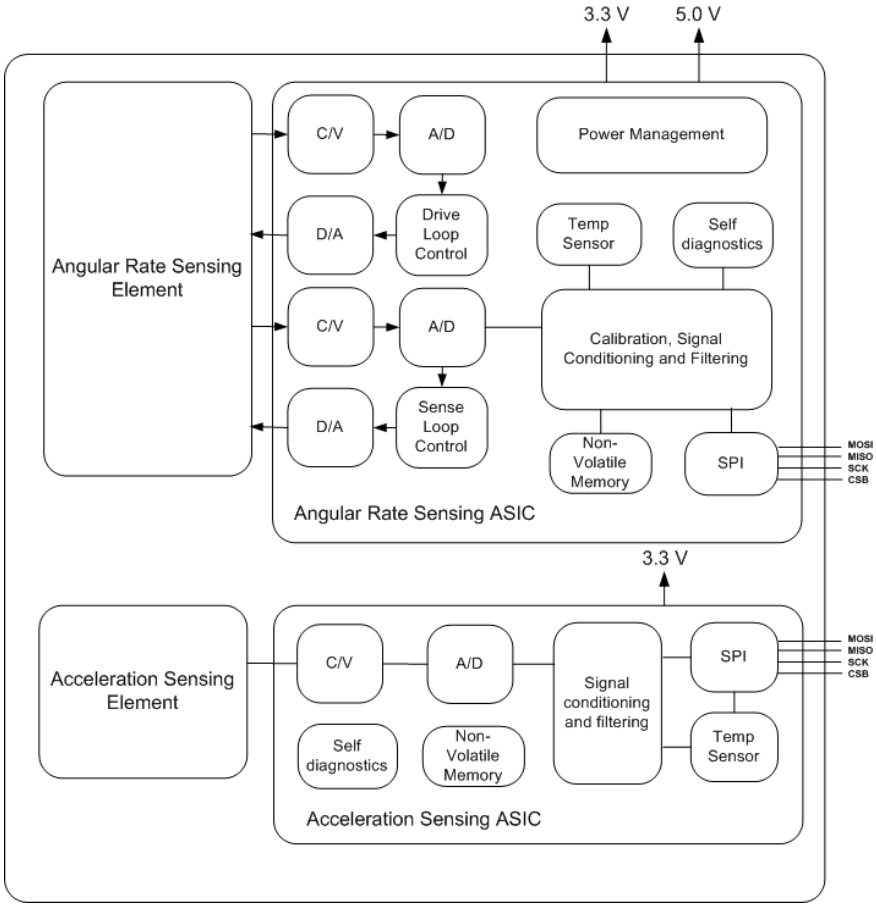

Figure 1. SCC1300 component block diagram.

The angular rate and acceleration sensing elements are manufactured using Murata proprietary High Aspect Ratio (HAR) 3D-MEMS process, which enables making robust, extremely stable and low noise capacitive sensors.

The acceleration sensing element consists of four acceleration sensitive masses. Acceleration causes capacitance change that is converted into a voltage change in the signal conditioning ASIC.

The angular rate sensing element consists of moving masses that are purposely exited to in-plane drive motion. Rotation in sensitive direction causes out-of-plane movement that can be measured as capacitance change with the signal conditioning ASIC.

1.2.1 Factory Calibration

SCC1300 sensors are factory calibrated. No separate calibration is required in the application. Trimmed parameters during production include sensitivities, offsets and frequency responses. Calibration parameters are stored during manufacturing inside non-volatile memory. The parameters are read automatically from the internal non-volatile memory during the start-up.

It should be noted that assembly can cause minor offset/bias errors to the sensor output. If best possible offset/bias accuracy is required, system level offset/bias calibration (zeroing) after assembly is recommended.

1.3 Abbreviations

ASIC	Application Specific Integrated Circuit
SPI	Serial Peripheral Interface
RT	Room Temperature
STC	Self Test Continuous (continuous self testing of accelerometer element)
STS	Self Test Static (gravitational based self test of accelerometer element)

2 Specifications

2.1 Performance Specifications for Gyroscope

Table 1. Gyroscope performance specifications (Avdd = 5 V, Dvdd = 3.3 V and ambient temperature unless otherwise specified).

Parameter	Condition	Min [A]	Typ	Max [A]	Units
Analog supply voltage		4.75	5	5.25	V
Analog supply current	Temperature range -40 ... +125 °C	24	26	29.5	mA
Digital supply voltage		3.0	3.3	3.6	V
Digital supply current	Temperature range -40 ... +125 °C	16	20	24	mA
Operating range	Measurement axis X	-100		100	°/s
Offset error [B]		-1		1	°/s
Offset over temperature	Temperature range -40 ... +125 °C	-0.6		0.6	°/s
	Temperature range -10 … +60 °C	-0.3		0.3	°/s
Offset drift velocity	Temperature gradient ≤ 2.5 K/min	-0.3		0.3	(°/s)/min
Offset short term instability [C]			<1		°/h
Angular random walk (ARW) [C]			0.45		°/√h
Sensitivity			50		LSB/(°/s)
Sensitivity over temperature	Temperature range -40 ... +125 °C	-1		1	%
Total sensitivity error [B]		-2		2	%
Nonlinearity	Temperature range -40 ... +125 °C	-0.5		0.5	°/s
Noise (RMS)			0.06	0.1	°/s
Noise Density			0.0085		(°/s)/√Hz
Cross-axis sensitivity [D]				1.7	%
G-sensitivity		-0.1		0.1	(°/s)/g
Shock sensitivity	50g, 6ms			2.0	°/s
Shock recovery time				50.0	ms
Amplitude response	-3dB frequency		50		Hz
Power on setup time				0.8	s
Output data rate			2		kHz
Output load				200	pF
SPI clock rate		0.1		8	MHz

A) MIN/MAX values are ±3 sigma variation limits from validation test population.

B) Including calibration error and drift over lifetime.

C) Typical, constant temperature, Allan Variance curve Figure 2 b).

D) Cross-axis sensitivity is the maximum sensitivity in the plane perpendicular to the measuring direction relative to the sensitivity in the measuring direction. The specified limit must not be exceeded by either axis.

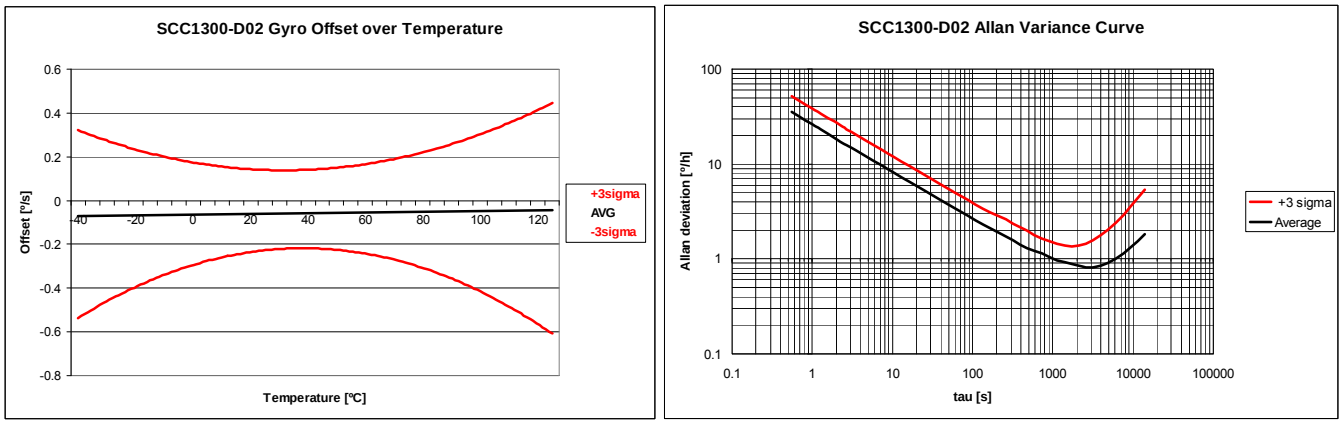

Figure 2 a) SCC1300-D02 Gyroscope offset over full temperature range, b) Allan variance curve

2.2 Performance Specifications for Accelerometer

Table 2. Acclerometer performance specifications (Vdd=3.3 V and ambient temperature unless otherwise specified).

Parameter	Condition	Min [A]	Typ	Max [A]	Units
Analog and digital supply voltage		3.0	3.3	3.6	V
Current consumption	Active mode		3	5	mA
	Power down mode		0.12		mA
Measurement range	Measurement axes X, Y & Z	-2		2	g
Offset error [B]	@25 °C ±5°C	-16		16	mg
Offset temperature drift [C]	Temperature range -40 ... +125 °C	-18		18	mg
Sensitivity	13 bit output		1800		LSB/g
	Between ±3°		0.032		°/LSB
Total sensitivity error	Temperature range -40 ... +125 °C	-4		4	% FS
Sensitivity calibration error	@25 °C ±5°C	-0.5		0.5	% FS
Sensitivity temperature drift	Temperature range -40 ... +125 °C	-0.8		0.8	% FS
Linearity error	+1g ... -1g range	-20		20	mg
Cross-Axis sensitivity		-2.5		2.5	%
Zero acceleration output	2-complement		0		LSB
Amplitude response [D]	-3dB frequency	30		55	Hz
Noise			3	5	mg RMS
Power on setup time				0.1	s
Output data rate			2000		Hz
Output load				50	pF
SPI clock rate				8	MHz
ID register value	Customer readable ID register (27hex)		8f		

A) MIN/MAX values are ±3 sigma variation limits from validation test population.

B) Includes offset deviation from 0g value, including calibration error and drift over lifetime.

C) Biggest change of output from RT value due temperature.

D) Cross-axis sensitivity is the maximum sensitivity in the plane perpendicular to the measuring direction relative to the sensitivity in the measuring direction. It is calculated as the geometric sum of the sensitivities in two perpendicular directions (Sx and Sy) in this plane

E) See Figure 3

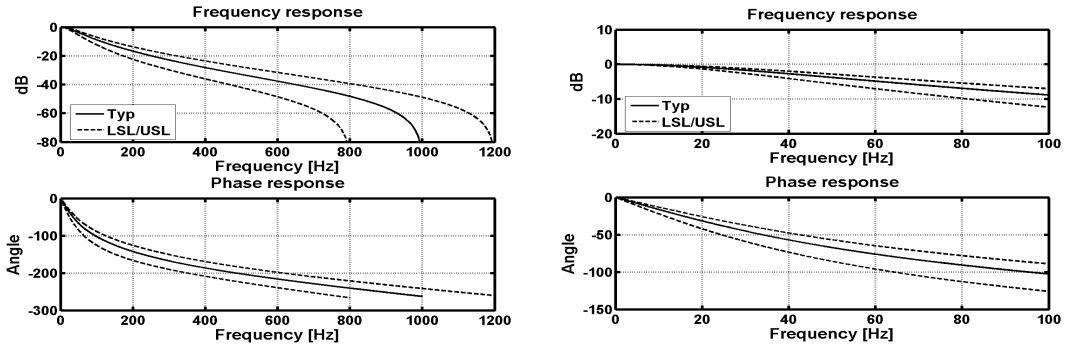

Figure 3. SCC1300-D02 Accelerometer frequency response curves

2.3 Absolute Maximum Ratings

Table 3. Absolute maximum ratings of the SCC1300 sensor.

Parameter	Condition	Min	Typ	Max	Units
Gyroscope supply voltages					
Analog supply voltage, AVDD_G		-0.5		7	V
Digital supply voltage, DVDD_G		-0.3		3.6	V
Maximum voltage at analog input/output pins		-0.3		AVDD_G + 0.3V	
Maximum voltage at digital input/output pins		-0.3		DVDD_G + 0.3	V
Accelerometer supply voltages					
Digital supply voltage, DVDD_A		-0.3		3.6	V
Analog supply voltage, AVDD_A		-0.5		7.0	V
Maximum voltage at input / output pins		-0.3		DVDD_A + 0.3V	V
General Component Ratings					
Operating temperature		-40		125	°C
Storage temperature		-40		125	°C
	Max 96h	-40		150	°C
Maximum junction temperature during lifetime. Note: device has to be functional, but not in full spec.				155	°C
Mechanical Shock			3000		g
ESD	HBM			2	kV
	CDM			500	V
Ultrasonic Cleaning	Prohibited				

2.4 Digital I/O Specification

Table 4 (gyroscope interface) and (accelerometer interface) below describe the DC characteristics of SCC1300 sensor digital I/O pins. Supply voltage is 3.3 V unless otherwise noted. Current flowing into the circuit has positive values.

Table 4. Absolute maximum ratings of the SCC1300 gyroscope SPI interface.

Parameter	Conditions	Symbol	Min	Typ	Max	Unit
Input terminal CSN_G						
Pull up current	V_{IN} = 0 V	I_{PU}	10		50	µA
Input high voltage	DVDD_G = 3.3 V	V_{IH}	2		DVDD_G	V
Input low voltage	DVDD_G = 3.3 V	V_{IL}			0.8	V
Hysteresis	DVDD_G = 3.3 V	V_{HYST}	0.3			V
V_{IN}	Open circuit	V_{IN}	2			V
Input terminal SCK_G						
Input high voltage	DVDD_G = 3.3 V	V_{IH}	2		DVDD_G	V
Input low voltage	DVDD_G = 3.3 V	V_{IL}			0.8	V
Hysteresis	DVDD_G = 3.3 V	V_{HYST}	0.3			V
Input leakage current	0 < V_{MISO} < 3.3 V	I_{LEAK}	-1		1	uA
Output terminal MOSI_G						
Input high voltage	DVDD_G = 3.3 V	V_{IH}	2		DVDD_G	V
Input low voltage	DVDD_G = 3.3 V	V_{IL}			0.8	V
Hysteresis	DVDD_G = 3.3 V	V_{HYST}	0.3			V
Input current source (pull-down)	V_{IN} = V_{DVDD_G}	I_{LEAK}	10		50	uA
V_{IN}	Open circuit	V_{IN}			0.3	V
Output terminal MISO_G (Tri-state)						
Output high voltage	I_{OUT} = -1mA	V_{OH}	DVDD_G -0.5V			V
	I_{OUT} = -50µA		DVDD_G -0.2V			V
Output low voltage	0 ≤ V_{MISO} ≤ 3.3 V	V_{OL}			0.5	V
Capacitive load					200	pF

Table 5. Absolute maximum ratings of the SCC1300 accelerometer SPI interface.

Parameter	Conditions	Symbol	Min	Typ	Max	Unit
Input terminal CSB_A						
Pull up current	V_{IN} = 0 V	I_{PU}	10		50	µA
Input high voltage	DVDD_A = 3.3 V	V_{IH}	2		DVDD_A	V
Input low voltage	DVDD_A = 3.3 V	V_{IL}			0.8	V
Hysteresis	DVDD_A = 3.3 V	V_{HYST}	0.18			V
Input terminal MOSI_A, SCK_A						
Pull down current	V_{IN} = 3.3 V	I_{PD}	10		50	µA
Input high voltage	DVDD_A = 3.3 V	V_{IH}	2		DVDD_A	V
Input low voltage	DVDD_A = 3.3 V	V_L			0.8	V
Hysteresis	DVDD_A = 3.3 V	V_{HYST}	0.18			V
Output terminal MISO_A						
Output high voltage	I > -1mA DVDD_A = 3.3 V	V_{OH}	DVDD_A - 0.5V			V
Output low voltage	I < 1 mA	V_{OL}			0.5	V
Tri-state leakage	0 < V_{MISO} < 3.3 V	I_{LEAK}	-3		3	uA

2.5 SPI AC Characteristics

The AC characteristics of SCC1300 are defined in Figure 4 and Table 6.

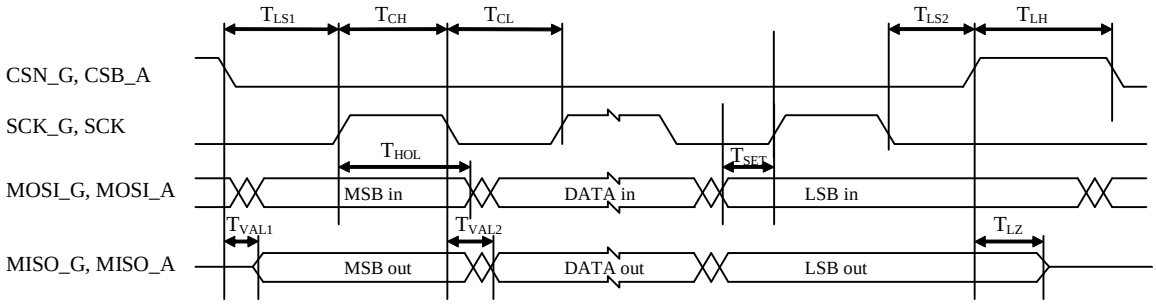

Figure 4. Timing diagram of SPI communication

Table 6. Timing Characteristics of SPI Communication.

Parameter	Condition	Min	Typ	Max	Units
F_{SPI}				8	MHz
T_{SPI}			1/ F_{SPI}		
T_{CH}	SCK_G, SCK_A high time	T_{SPI} /2			ns
T_{CL}	SCK_G, SCK_A low time	T_{SPI} /2			ns
T_{LS1}	CSN_G, CSB_A setup time	T_{SPI} /2			ns
T_{VAL1}	Delay CSN_G -> MISO_G Delay CSB_A -> MISO_A			T_{SPI} /4	ns
T_{SET}	MOSI_G, MOSI_A setup time	T_{SPI} /4			ns
T_{HOL}	MOSI_G, MOSI_A data hold time	T_{SPI} /4			ns
T_{VAL2}	Delay SCK_G -> MISO_G Delay SCK_A -> MISO_A			1.3 * T_{SPI} /4	ns
T_{LS2}	CSN_G, CSB_A hold time	T_{SPI} /2			ns
T_{LZ}	Tri-state delay time			T_{SPI} /4	ns
T_{RISE}	Rise time of the SCK_G, SCK_A			10	ns
T_{FALL}	Fall time of the SCK_G, SCK_A			10	ns
T_{LH}	Time between SPI cycles	T_{SPI}			ns

3 Reset and Power Up

After the start-up the angular rate and acceleration data is immediately available through SPI registers. There is no need to initialize the gyroscope or accelerometer before starting to use it. If the application requires monitoring operation correctness there are several options available to monitor the status.

3.1 Power-up Sequence for Gyroscope

To ensure correct ASIC start up please connect the digital supply voltage V_{DVDD_G} (3.3V) before the analog supply voltage V_{AVDD_G} (5.0V) to the gyro ASIC. After power up please read Status register twice to clear error flags. Angular rate data is available immediately so no start up command sequence is required if error flags are not used.

Table 7. SCC1300 gyroscope power-up sequence.

Procedure	Functions	Check
Set V_{DVDD_G} V=3.0...3.6V		
Wait 10ms		
Set V_{AVDD_G} V=4.75...5.25V		
Wait 800 ms		
Read Status register (08h) two times	Acknowledge error flags after start up	

3.2 Start-up and Operation Sequence for Accelerometer

3.2.1 Recommended Start-up Sequence

For correct device operation there are no specific configuration needed for the device before starting of measuring the acceleration. However if the device diagnostic features are being used the following operations could be made after the powering on the device.

Table 8. SCC1300 accelerometer part start-up sequence.

Procedure	Functions	Check
Set Vdd=3.0...3.6V	Release part from reset	
Wait 35ms	Memory reading and self-diagnostic Settling of signal path	
Read INT_STATUS	Acknowledge for possible saturation (SAT-bit) Checksum pass detected from SPI frame	SPI fixed bits SPI ST=0
Write CTRL=00001010 (a) or CTRL=00001000 (b) or CTRL=00000000 (c)	Set PORST=0 (abc) Start STC (ab) Start STS (a)	SPI fixed bits SPI FRME=0 SPI ST=0 SPI SAT=0
Wait 10ms	STS calculation	
Read CTRL	Check that STC is on, if enabled Check that STS is over if enabled	CTRL.ST=1 CTRL.ST_CFG=0 SPI fixed bits SPI FRME=0 SPI PORST=0 SPI ST=0 SPI SAT=0 dPAR, data parity
Read Z_MSB, Z_LSB, Y_MSB, Y_LSB, X_MSB, X_LSB	Read acceleration data	SPI fixed bits SPI FRME=0 SPI PORST=0 SPI ST=0 SPI SAT=0 dPAR, data parity

3.2.2 Recommended Operation Sequence for Acceleration Data Reading

Table 9. Reading of the acceleration data

Procedure	Functions	Check
Read acceleration data	Desired x, y, or/and z-data	SPI fixed bits SPI FRME=0 SPI PORST=0 SPI ST=0 SPI SAT=0 dPAR, data parity
Repeat previous line (N-1) times	Noise averaging	
Calculate average (AVE) of N-samples	Noise averaging	
Read acceleration data	Desired x, y, or/and z-data (one read before sending AVE forward to check SPI failure bits)	SPI fixed bits SPI FRME=0 SPI PORST=0 SPI ST=0 SPI SAT=0 dPAR, data parity
Send calculated AVE forward		
Jump back to item 2		

4 Component Interfacing

4.1 SPI Interfaces

SCC1300 sensor has two individual SPI interfaces for accelerometer and angular rate sensor that need to be addressed separately. Both interfaces have their own four wire interconnection pins in the component package. SPI communication transfers data between SPI master and registers of the SCC1300 ASICs. SCC1300 ASICs always operate as slave devices in the master-slave operation mode.

SCC1300 Angular rate sensor ASIC SPI interface:

MOSI_G	master out slave in	µP → ASIC
MISO_G	master in slave out	ASIC → µP
SCK_G	serial clock	µP → ASIC
CSN_G	chip select (low active)	µP → ASIC

SCC1300 Accelerometer ASIC SPI interface:

MOSI_A	master out slave in	µP → ASIC
MISO_A	master in slave out	ASIC → µP
SCK_A	serial clock	µP → ASIC
CSB_A	chip select (low active)	µP → ASIC

PLEASE NOTICE THAT EXACTLY THE SAME SPI ROUTINES DOES NOT WORK FOR BOTH ASICS! E.g. SCC1300 accelerometer ASIC uses 8 bit addressing in SPI and SCC1300 angular rate sensor ASIC uses 16 bit addressing.

Both SPI interfaces and instructions to use them are explained separately in the following chapters.

4.2 Gyroscope Interface

This chapter describes the SCC1300 angular rate sensor ASIC interface and how to use it. The angular rate sensor ASIC SPI interface has 16 bit addressing.

4.2.1 SPI Transfer

The SPI transfer is based on a 16-bit protocol. Figure 5 shows an example of a single 16-bit data transmission. Each output data/status-bits are shifted out on the falling edge of SCK (MISO line). Each bit is sampled on the rising edge of SCK (MOSI line).

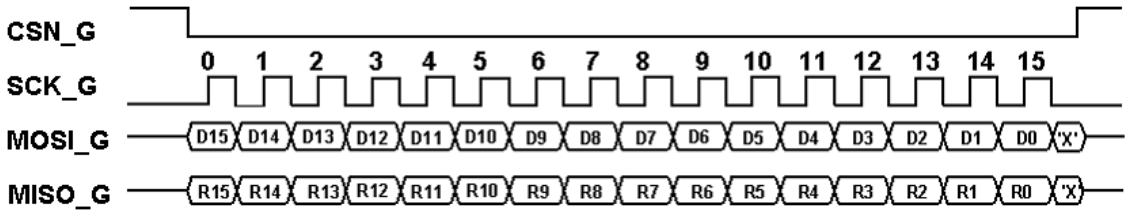

Figure 5. SCC1300 angular rate sensor 16-bit data transmission.

After the falling edge of CSN_G the device interprets the first 16-bit word is an address transfer having a bit coding scheme below.

Address Transfer:

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	0	0	ADR6	ADR5	ADR4	ADR3	ADR2	ADR1	ADR0	RW	0	Par odd

ADR[6:0] : Register address
RW : RW=1 : Write access
RW=0 : Read access
par odd : odd parity bit.
par odd = 0 : the number of ones in the data word (D15:D1) is odd.
par odd = 1 : the number of ones in the data word (D15:D1) is even.

The address selects an internal register of the device; the RW bit selects the access mode.

RW = ‘0' The master performs a read access on the selected register. During the transmission of the next word, the slave sends the requested register value to MISO_G. The slave interprets the next word at MOSI_G as an address transfer.

RW = ‘1' The master performs a write access on the selected register. The slave stores the next transmitted word in the selected device register of MOSI_G and sends the actual register value in response to MOSI_G. The transmission goes on with an address transfer to MOSI_G and the address mode flags to MISO_G.

If the device is addressed by a nonexistent address it will respond with ´0´.

The next table shows the encoding scheme of a data value for a write access.

Data Transfer:

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Dat14	Dat13	Dat12	Dat11	Dat10	Dat9	Dat8	Dat7	Dat6	Dat5	Dat4	Dat3	Dat2	Dat1	Dat0	Par odd

dat[14:0] : data value for write access (15 Bit)
par odd : see Address Transfer

It is possible to combine the two access modes (write and read access) during one communication. The communication can be finished after last transmitted word of mixed access communication frame with CSN_G='1'. CSN_G must be '0' during mixed access communication frame.

SPI result values on MISO_G

Within SPI communication SCC1300 gyro ASIC sends Status Flags (Status/Config register value) and register result values on MISO_G. The following two tables show the encoding scheme:

Status Flags:

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
														s_ok	par odd

S_OK is generated out of the monitoring flags in the status register (08h).

Register Result:

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
reg 14	reg 13	reg 12	reg11	reg 10	reg9	reg8	reg7	reg6	reg5	reg4	reg3	reg2	reg1	reg0	par odd

reg[14:0] : value of the internal register. All bits, which are not used, are set to zero.
par odd : see Address Transfer

Figure 6 shows an example of communication sequence:

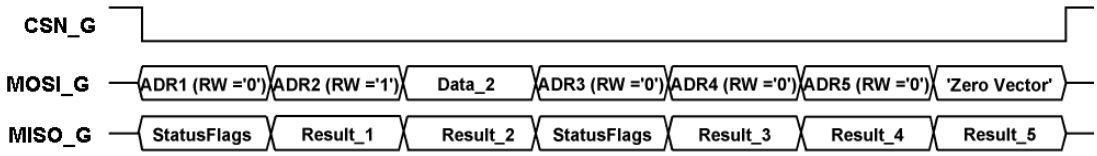

Figure 6. Communication example.

Each communication frame in the figure 6 contain 16 SCK cycles. After communication start (CSN_G falling edge) the master sends ADR1 and performs a read access. In parallel the slave sends Status Flags. During the transmission of the next data word (ADR2) the slave sends the register value of ADR1 (Result_1). On ADR2 the master performs a write access (RW='1'). The slave stores Data_2 in the register of ADR2 and sends the current register value of ADR2 to MISO_G. After the transmission of data value during a write access the slave always sends Status Flags. To receive Result_5 of the last read access the Master has to send an additional word ('Zero Vector').

Example of how to read out Rate output

The MCU begins by sending the address frame followed by a zero vector (with correct parity). The zero vector is necessary for the sensor to be able to reply to the MCU during the last 16-bit frame. The sensor replies by sending first the status bits followed by the rate data.

MOSI: 0x0001 0x0001
MISO: 0x3FFE 0x0008

4.2.2 SPI Transfer Parity Mode

SCC1300 gyro ASIC is able to support parity check during SPI Transfer. This functionality is controlled by the IC Identification Register. The internal parity status is reported in Status/Config Register.

With parity enable bit set the SCC1300 gyro ASIC is expecting an additional parity bit after the transmission of each 16 bit data word. This additional parity bit requires an additional SCK cycle, i.e. the SPI frame consists of 17 SCK cycles instead of the normal 16 SCK cycles. Detecting a wrong parity bit has the following consequences:

During read access:
The Parity Error Flag in the Status/Config Register is set. The SCC1300 reports the contents of the received register address.

During write access:
The Parity Error Flag in the Status/Config Register is set. The SPI Write Access is cancelled.
These actions are performed either if the parity failure is detected in the address word or the data word.

Due to the additional parity bit a single SPI Transfer is using now 17 Bit as shown in the Figure 7.

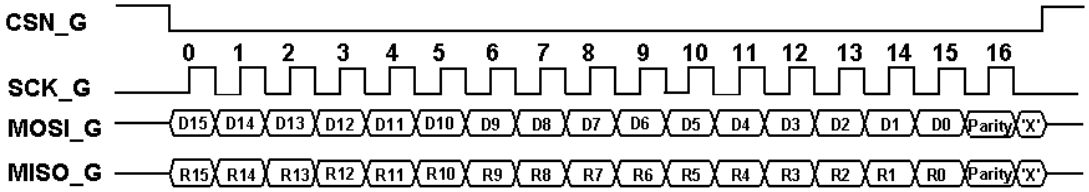

Figure 7. Communication in parity mode.

At the end of the data word the SPI master and the SPI slave have to add an additional parity bit. Both devices have to check the received parity according to the selected parity mode odd or even.

4.3 Gyroscope ASIC Addressing Space

4.3.1 Register Definition

The ASIC has multiple register and EEPROM blocks. The EEPROM blocks holding the calibration data will be programmed via SPI during manufacturing process. User only needs to access the Data Register Block at addresses 00h and 07h - 0Ah (addresses 01h-06h are reserved). The content of this register block is described below.

4.3.2 Data Register Block

Table 10. Register map of data register block.

Address Dec (hex)	Register Name [bit definition]	Number of Bits	Read/ Write/ Factory	Data Format	Description
00(00)	Rate_X[0]	1	R	-	odd Parity bit of Rate_X[14,1]
00(00)	Rate_X[1] (S_OK Flag)	1	R	-	S_OK =0 Rate_X failed S_OK =1 Rate_X valid (ok) S_OK is generated out of the monitoring flags in the status register (08h). If either one of the flags in register 08h [15:2] is 0, S_OK will be 0. Only if all flags in register 08h[15:2] are 1 S_OK is set to 1
00(00)	Rate_X[15:2]	14	R	S	Sensor output data format two's complement
07(07)	IC Identification [14, 11:1]	14	F	-	Reserved
07(07)	IC Identification[12] HWParEn	1	W		Setting this bit to '1' is enabling the Parity functionality
07(07)	IC Identification[13] HWParSel	1	W		This bit is selecting an even or an odd parity mode. Bit = 0: Even Parity mode means that the number of ones in the data word including the parity bit is even. Bit = 1: Odd Parity mode means that the number of ones in the data word including the parity bit is odd.
08(08)	Status/Config [14:10, 8:1]	14	F	-	Reserved
08(08)	Status/Config[9] (Parity_OK)	1	R	-	This bit is set as soon as the SPI logic is detecting a wrong parity bit received from the µC. This bit is automatically cleared during read access to this register. Bit = 0 : Parity error Bit = 1 : Parity check ok.
09(09)	Reserved	14	F	-	Reserved
10(0A)	Temp[0]	1	R	-	odd Parity bit of TEMP[14,1]
10(0A)	Temp[1] (S_OK Flag)	1	R	-	S_OK =0 Rate_X failed S_OK =1 Rate_X valid
10(0A)	Temp[15,2]	14	R	S	Temperature sensor output

The offset of temperature data is factory calibrated but sensitivity of the temperature data varies from part to part. Note: Registers marked with F are reserved for factory use only and not to be written to.

4.3.3 Temperature Output Register

The offset of temperature sensor is factory calibrated but sensitivity of the temperature data varies from part to part. The temperature doesn't reflect absolute ambient temperature.

Temperature data is in 2's complement format in 14 bits (15:2) of Temp register. To use the temperature sensor as an absolute temperature sensor or for additional system level compensations, the offset and sensitivity of the sensor should be measured and calibrated on system level

Temperature registers' typical output at +23 °C is -1755 counts and 1 °C change in temperature typically corresponds to 65 count change in temperature sensor output. Temperature information can be converted from decimals to [°C] as follows

$$Temp[^{o}C] = (Temp[LSB] + 3250) / 65,$$

where Temp[°C] is temperature in Celsius and Temp[LSB] is temperature from TEMP registers in decimal format,

Temperature sensor offset calibration error at 25°C: ≤ ±15 °C
Temperature sensor sensitivity calibration error : ≤ 5%

4.4 Accelerometer Interface

This chapter describes the SCC1300 accelerometer part SPI interface and how to use it. SPI frame format and transfer protocol for SCC1300 accelerometer ASIC is presented in Figure 8.

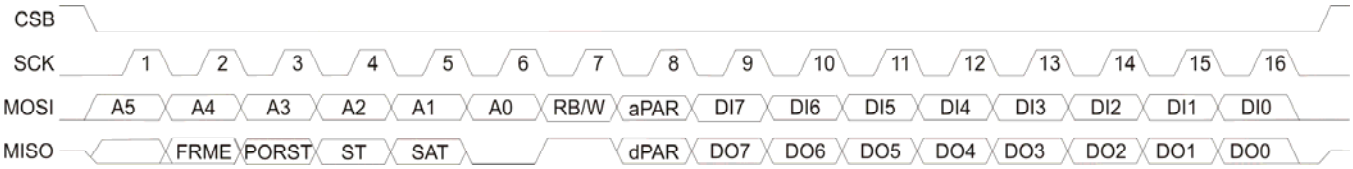

Figure 8. SPI frame format for accelerometer interface.

- MOSI_A
  - A5:A0 Register address
  - RB/W Read/Write selection, '0'=read
  - aPAR Odd parity for bits A5:A0, RB/W
  - DI7:DI0 Input data for data write
- MISO_A
  - Bit 1 not defined bit
  - FRME Frame error indication (previous frame)
  - Bit 3-5 status bits
    - PORST Power On Reset Status
    - ST Self Test error
    - SAT Output SATuration indicator
  - Bit 6 always ‘0’, fixed bit
  - Bit 7 always ‘1’, fixed bit
  - dPAR Odd parity for output data (DO7:DO0)
  - DO7:DO0 Output data

Each communication frame contains 16 bits. Each output data/status-bits are shifted out on the falling edge of SCK (MISO line). Each bit is sampled on the rising edge of SCK (MOSI line). The first 8 bits in MOSI_A line contains info about the operation (read/write) and the register address being accessed. First 6 bits define 6 bit address for selected operation, which is defined by bit 7 (‘0’ = read ‘1’ = write), which is followed by odd parity bit (aPAR) for 8 bit pattern. The later 8 bits in MOSI_A line contain data for a write operation and are ignored in case of read operation.

The first bits in MISO_A line are frame error bit (FRME, bit2) of previous frame, reset status bit (PORST, bit3), self-test status bit (ST, bit4), saturation status (SAT, bit5), fixed zero bit (bit6), fixed one bit (bit7) and odd parity bit of output data (dPAR, bit8)). Parity is calculated from data, which is currently sent. The later 8 bits contain data for a read operation. During the write operation, these data bits are previous data bits of addressed register.

For write commands, data is written into the addressed register on the rising edge of CSB_A. If the command frame is invalid, data will not be written into the register.

The output register is shifted out MSB first over MISO_A output. Attempt to read a reserved register outputs data of 00h.

When CSB is high state between data transfers, MISO_A line is in high-impedance state. If bit CTRL.SDODIS is set to ‘1’, MISO_A line is always in high-impedance state. In multi-chip SPI bus master can send data to all slave chips simultaneously.

4.4.1 Output of Acceleration Data

16-bit data is sent in 8-bit data bytes during two frames. Each frame contains odd parity bit of data bits. Number format of acceleration data is two’s complement number.

4.4.1.1 Register read operation

An example of X-axis acceleration read command is presented in Figure 9. Master gives the register address to be read via MOSI_A line: '05' in hex format and '000101' in binary format, register name is X_MSB (X-axis MSB frame). 7th bit is set to '0' to indicate the read operation and 8th bit is 1 for odd parity.
The sensor replies to asked operation by transferring the register content via MISO_A line. After transferring the asked X_MSB register content, master gives next register address to be read: '04' in hex format and '000100' in binary format, register name is X_LSB (X-axis LSB frame). The sensor replies to asked operation by transferring the register content MSB first.

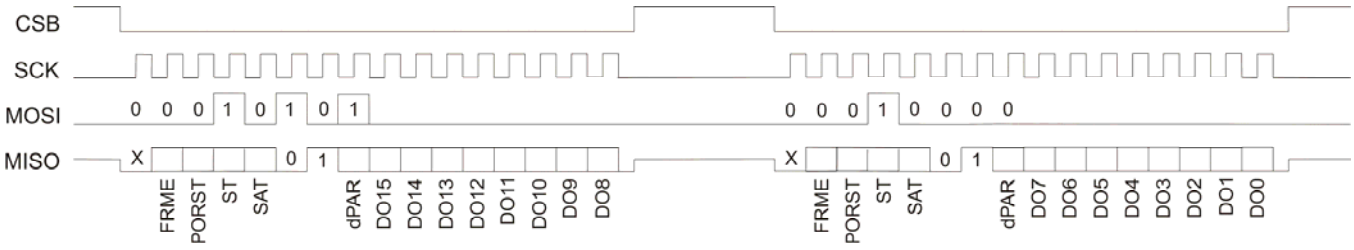

Figure 9: Example of 16 bit acceleration data transfer from registers DOUT2-1 (05h,04h).

DO15…DO0 bits are acceleration data bits (DO15=MSB) and parity (dPAR) is odd parity of register of 8 data bits. FRME is possible frame error bit of previous frame, PORST is reset bit, ST is self-test status bit and SAT is output saturation status bit.

4.4.1.2 Decremented register read operation

In Figure 10 is presented a decremented read operation where the content of four output registers is read by one SPI frame. After normal register addressing and one register content reading the µC keeps CSB_A line low and continues supplying the SCK_A pulses. After every 8 SCK pulses the output data address is decremented by one and the previous DOUT register's content is shifted out without parity bits. Parity bit is calculated and transferred only for the first data frame. From X_LSB register address the ASIC jumps to Z_MSB. Decremented reading is possible only for registers X_LSB ... Z_MSB.

Decremented read is not recommended in fail-safe critical applications because output data parity is only available for first 8bit data.

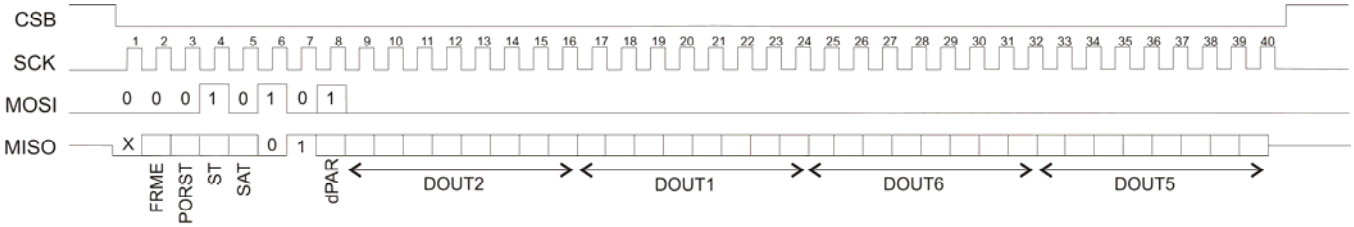

Figure 10: An example of decremented read operation.

4.4.2 MOSI data of SPI commands

Table 11. MOSI_A data during SPI read command

Register to be read	Function	MOSI (15:0) [bits]	MOSI [hex]
REVID	Read ASIC revision ID	000000 01 xxxxxxxx	01xx
CTRL	Read CTRL register	000001 00 xxxxxxxx	04xx
STATUS	Read Status register	000010 00 xxxxxxxx	08xx
X_LSB	Read acceleration on X-axis, LSB	000100 00 xxxxxxxx	10xx
X_MSB	Read acceleration on X-axis, MSB	000101 01 xxxxxxxx	15xx
Y_LSB	Read acceleration on Y-axis, LSB	000110 01 xxxxxxxx	19xx
Y_MSB	Read acceleration on Y-axis, MSB	000111 00 xxxxxxxx	1Cxx
Z_LSB	Read acceleration on Z-axis, LSB	001000 00 xxxxxxxx	20xx
Z_MSB	Read acceleration on Z-axis, MSB	001001 01 xxxxxxxx	25xx
TEMP_LSB	Read temperature, LSB	010010 01 xxxxxxxx	49xx
TEMP_MSB	Read temperature, MSB	010011 00 xxxxxxxx	4Cxx
INT_STATUS	Read INT_STATUS register	010110 00 xxxxxxxx	58xx
ID	Read product ID number	100111 01 xxxxxxxx	9Dxx

Table 12. MOSI_A data during write command

Register to be written	Function	MOSI (15:0) [bits]	MOSI [hex]
RESET	Reset component (data C'hex)	000011 10 00001100	0E0C
RESET	Reset component (data 5'hex)	000011 10 00000101	0E05
RESET	Reset component (data F'hex)	000011 10 00001111	0E0F
CTRL	Set PORST to zero	000001 11 00000000	0700
CTRL	Set chip to power down mode	000001 11 00100000	0720
CTRL	Start self-diagnostic	000001 11 00001000	0708
CTRL	Start memory self-test	000001 11 00000100	0704

4.4.3 Error Conditioning

FRME-bit

While sending a frame, if CSB is raised to 1 before sending 16 SCKs, the frame is considered invalid. The frame error is raised only if number of SCK pulses is not divisible by 8 to support decremented mode reading. When an invalid frame is received, the last command is simply ignored and the register contents are left unchanged. Status bit STATUS.FRME is set to indicate this error condition. During next SPI frame error bit send out as bit number 2. Bit STATUS.FRME will be reset, if correct frame is received.

PORST-bit

PORST length is 1bit in SPI frame. PORST bit is set if chip is reset (HW reset by POR or supply on/off) or under-voltage is detected. PORST bit is also set after power-up because chip has been in reset state. PORST can be set to zero (reseted) by writing CTRL.PORST =0. Software (SW) reset does not set PORST.
When CTRL.PORST bit is written to 0 via SPI, there is 300ns delay before register value is set to zero.

ST-bit

Self-test frame status (ST) is set if STC or STS is alarmed or checksum is not passed.

- CASE 1: Checksum fails and ST-frame bit is set 1. ST is set back to zero when (and only if) new checksum calculation is passed.

- CASE 2: ST-frame bit is set because STC or STS is alarmed. In this case ST-frame bit can be cleared by INT_STATUS register reading.

SAT-bit

Saturation status (SAT) is set if any of axis xyz is saturated and it can be cleared by INT_STATUS register reading. This bit is kept active even failure condition is over if it is not acknowledged.

aPAR-bit

aPAR is odd parity bit of input address+RB/W-bit. Master write it and slave check that bit.

- If there is parity error and RB/W='1', write command is ignored and frame error bit is set to STATUS-register and to SPI frame. Next correct SPI frame will zero this bit.

- If there is parity error and RB/W='0', read command is performed normally and frame error bit is set to STATUS-register and to SPI frame. Next correct SPI frame will zero this bit.

Table 13. Address parity.

Address								Notes
A5	A4	A3	A2	A1	A0	RB/W	aPAR	
0	0	0	0	0	0	0	**1**	correct frame
1	1	1	1	1	1	1	**0**	correct frame
1	0	1	0	1	0	1	**1**	correct frame
0	1	0	1	0	1	0	**0**	correct frame

dPAR-bit

dPAR bit is odd parity bit of 8bit data that is currently sent in the frame. Master checks this bit and compares to received data. Using dPAR at least one bit errors in data transmission can be detected.

Fixed bits

Bits 6 and 7 are always fixed in MISO line. Bit 6 should always be '0' and bit 7 always '1'

Output data

1. Reset stage: When component is in reset or under voltage state, PORST bit in SPI frame and CTRL. PORST bit is set. Furthermore, all register values are set to 00'hex.
2. Saturation: When acceleration exceeds measurement range, the output data is saturated to specified positive or negative full-scale.
3. Self-diagnostic failure: The ST bit in SPI frame is set when memory diagnostic or signal path diagnostic functions fail. Furthermore acceleration output data is forced to 7FFF'hex if memory diagnostic fails or to FFFF'hex if signal path diagnostic functions (STC/STS) fail.

4.5 Accelerometer ASIC Addressing Space

4.5.1 Register Map of Accelerometer

Table 14. Register address space

Address Dec (hex)	Register Name [bit definition]	Number of Bits	Read/ Write	Data format	Description
00(00)	REVID	8	R	-	ASIC revision identification number, each ASIC version has different REVID-number.
01(01)	CTRL	8	R/W	-	Please refer to chapter 4.5.2 for CONTROL register details.
02(02)	STATUS [7:3]	5	R	-	Reserved
02(02)	STATUS [2] (ATEST)	1	R		Analog test mode status 1 – Test mode is active 0 – Test mode is not active
02(02)	STATUS [1] (CSMERR)	1	R		EEPROM Checksum Error. ST bit of SPI frame is also set if CSMERR is set.
02(02)	STATUS [1] (FRME)	1	R		SPI frame error. Bit is reset, when next correct SPI frame is received. Bit is also visible in SPI frame.
03(03)	RESET	8	R/W		Writing 0C'hex, 05'hex, 0F'hex in this order resets component.
04(04)	X_LSB [7:1]	7	R		X-axis LSB data frame (Read always X_MSB prior to X_LSB)
04(04)	X_LSB [0]	1	R		Reserved
05(05)	X_MSB [5:0]	6	R		X-axis MSB data bits (Reading of this register latches X_LSB)
05(05)	X_MSB [7:6]	2	R		Reserved
06(06)	Y_LSB [7:1]	7	R		Y-axis LSB data frame (Read always Y_MSB prior to Y_LSB)
06(06)	Y_LSB [0]	1	R		Reserved
07(07)	Y_MSB [5:0]	6	R		Y-axis MSB data bits (Reading of this register latches Y_LSB)
07(07)	Y_MSB [7:6]	2	R		Reserved
08(08)	Z_LSB [7:1]	7	R		Z-axis LSB data frame (Read Z_MSB prior to Z_LSB)
08(08)	Z_LSB [0]	1	R		Reserved
09(09)	Z_MSB [5:0]	6	R		Z-axis MSB data bits (Reading of this register latches Z_LSB)
09(09)	Z_MSB [7:6]	2	R		Reserved
18(12)	TEMP_LSB	8		See chapter 4.5.3.	Data bits [7:0] of temperature sensor. Read always TEMP_MSB prior to TEMP_LSB.
19(13)	TEMP_MSB	8		See chapter 4.5.3.	Data bits [15:8] of temperature sensor. Reading of this register latches TEMP_LSB.
22(16)	INT_STATUS [7]	1	R		Reserved
22(16)	INT_STATUS [6] (SAT)	1	R		Saturation status of output data 1 – Over range detected, one or 2-3 of xyz axis is saturated and output data is not valid. 0 – Data in range SAT bit is also visible in SPI frame. This bit can be active after start-up or reset stage before signal path settles to final value and it has to be acknowledged in start-up sequence (see Table 8) or after SW reset or after PORST stage.
22(16)	INT_STATUS [5] (STS)		R		Status of gravitation based start-up self test 1 – Failure 0 – No failure STS sets also ST bit in SPI frame.
22(16)	INT_STATUS [4] (STC)				Status of continuous self test 1 – Failure 0 – No failure STC sets also ST bit in SPI frame.
22(16)	INT_STATUS [3:0]				Reserved
39(27)	ID	8			Component identification number (write operation by user is possible to this register but not to non-volatile memory)

Note: The acceleration data is presented in 2's complement format. At 0 g acceleration the output is ideally 0000h.
Note: INT_STATUS: The bits in this interrupt status register and corresponding SPI frame bits are cleared after register has been read. Register reading is treated as interrupt acknowledgement signal. These bits are kept active even failure condition is over if they are not acknowledged.

4.5.2 Control Register (CTRL)

Table 15. SCC1300 accelerometer ASIC control register bit level description.

Bits	Mode	Initial Value	Name	Description
7	RW	0		Reserved
6	RW	0	PORST	1 means reset state. Bit gets set to 1 when the digital gets reset by supply off control or under voltage control. Bit is set after supply off/on transition or startup. This bit can not be set by SPI but it can be reset to 0 by writing a 0 over the SPI. This bit is also sent as Bit3 of SPI output data frame on MISO.
5	RW	0	PDOW	Set chip to power down mode
4	RW	0	SLEEP	Set chip to sleep mode. This bit can not be set to 1 if PDOW is already 1 or if PDOW is being set by the current SPI command.
3	RW	0	ST	Set chip to self-test mode. Start continuous self-test calculation (STC). This bit can not be set to 1 if PDOW or SLEEP or MTST is already 1 or if PDOW or SLEEP or MTST is being set by the current SPI command. Use INT_STATUS.STC and ST bit of SPI frame for test result monitoring.
2	RW	0	MST	Memory self-test function is activated, when user sets bit to '1'. This bit is reset to 0 when test is over. During memory self test, SPI access is prevented for 85us. This bit can not be set to 1 if PDOW or SLEEP is already 1 or if PDOW or SLEEP is being set by the current SPI command. Test is done automatically during start-up. Set other bits to zero in CTRL register by previous SPI command before starting memory self-test by CTRL.MST command. Use STATUS.CSMERR for test result monitoring and ST bit in SPI frame.
1	RW	0	ST_CFG	Self-test configuration. Start gravitation based start-up self-test calculation (STS). This bit can not be set to 1 if PDOW or SLEEP or MTST is already 1 or if PDOW or SLEEP or MTST is being set by the current SPI command. STC and STS have same priority and they can be set and used simultaneously. This bit is set to 0 when test is over. Use INT_STATUS.STS and ST bit of SPI frame for test result monitoring.
0	RW	0	MISO	0 = Set MISO line to normal state (= High impedance state between SPI transfers, data out state during transfers) 1 = Set MISO like to a continuous high impedance state (same write command to multiple slaves, which share MISO line).

4.5.3 Temperature Output Registers

The offset of temperature data is factory calibrated but sensitivity of the temperature data varies from part to part. Temperature data is in unsigned format and 13 bits (13:1) of TEMP_MSB/TEMP_LSB are used for temperature. Here is presented temperature calculation using 10bit but 3-extra LSB bit can be used to improve resolution in noise sense if needed.

Table 16 Bit level description for accelerometer temperature registers

Register	TEMP_MSB							TEMP_LSB					
Bit number	B7:B6	B5	B4	B3	B2	B1	B0	B7	B6	B5	B4	B3:B1	B0
Bit in temperature register	xx	t9	t8	t7	T6	T5	t4	t3	t2	t1	t0	r r r	x

x = not used bit
r=reserved

Temperature registers' typical output at +23 °C is 512 counts and 1 °C change in temperature typically corresponds to 3.2 LSB change in temperature output. Temperature information is converted to [°C] as follows

$$Temp[°C] = (23 \pm 10)°C + \frac{Temp_{dec} - 512LSB}{k\,\frac{LSB}{°C}},$$

where Temp[°C] is temperature in Celsius and $Temp_{dec}$ is temperature from TEMP_MSB and TEMP_LSB registers in decimal format, bits(t9:0). k is temperature slope factor specified as

	Min	Typ	Max	Unit
k	2.8	3.2	3.6	LSB/°C

5 Application Information

5.1 Pin Description

The pin out for SCC1300 is presented in Figure 11 (pin descriptions can be found from Table 17).

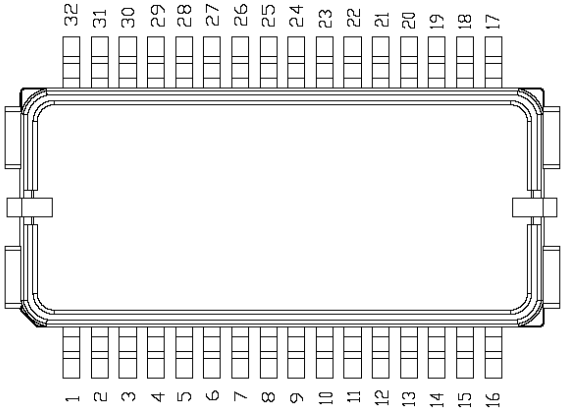

Figure 11. SCC1300 pinout diagram.

Table 17. SCA1300 pin descriptions.

pin #	Name	Type 1)	PD/PU/HV 3)	Description
1	HEAT	A1		Heatsink connection, externally connected to AVSS_G.
2	REFGND_G	AI		Analog reference ground should be connected external to AVSS_G
3	VREFP_G	AO		External C for positive reference voltage and output pin for use as supply for external load. Max load current is 5mA. Note this voltage can only be used as supply for analog circuits. Circuits that produce high current spikes due to switching circuit can not be driven by this node.
4	EXTRESN_G	DI	PU	External Reset, 3.3V level Schmitt-trigger input with internal pull-up, High low transition cause system restart
5	RESERVED	R		Factory used only, leave floating
6	AHVVDDS_G	AO	HV (~30V)	External C for high voltage analog supply, high voltage pad ≈30V
7	LHV	AI		Connection for inductor for high voltage generation, high voltage pad ≈30V
8	DVDD_G	AI		Digital Supply Voltage
9	DVSS_G	AI		Digital Supply Return, external connected to AVSS_G
10	MISO_G	DOZ		Data Out of SPI Interface, 3.3V level, Level definition see SPI-section
11	SCK_A	DI	PD	Clk Signal of SPI Interface, 3.3V level Schmitt-trigger input
12	MOSI_A	DI	PD	Data In of SPI Interface, 3.3V level Schmitt-trigger input
13	RESERVED	R		Factory used only, leave floating
14	DVIO	AI		Positive power supply (IO)
14	DVDD_A	AI		Positive power supply (digital)
15	DVSS_A	AI		Negative power supply (digital)
16	HEAT	A1		Heatsink connection, externally connected to AVSS_G.
17	HEAT	A1		Heatsink connection, externally connected to AVSS_G.
18	RESERVED	R		Factory used only, leave floating
19	SUB	AI		Substrate, wirebonded to AVSS_A
19	AVSS_A	AI		Negative power supply (analog)
20	AVDD_A	AI		Positive power supply (analog)
21	CSB_A	DI	PU	Chip Select of SPI Interface, 3.3V level Schmitt-trigger input
22	MISO_A	DOZ		Data Out of SPI Interface, 3.3V level, Level definition see SPI-section
23	MOSI_G	DI	PD	Data In of SPI Interface, 3.3V level Schmitt-trigger input
24	SCK_G	DI	PD	Clk Signal of SPI Interface, 3.3V level Schmitt-trigger input, Input Clock range 2 to 8MHz. Level definition see SPI-section
25	CSN_G	DI	PU	Chip Select of SPI Interface, 3.3V level Schmitt-trigger input, Input Clock range 2 to 8MHz. Level definition see SPI-section
26	RESERVED	R		Factory used only, leave floating
27	RESERVED	R		Factory used only, leave floating
28	AVDD_G	AI		Analog Supply voltage

pin #	Name	Type 1)	PD/PU/HV 3)	Description
29	SUB	AI		Connected external to AVSS_G
30	RESERVED	R		Factory used only, leave floating
31	RESERVED	R		Factory used only, leave floating
32	HEAT	A1		Heat sink connection, externally connected to AVSS_G.

Notes:
1) A=Analog, D=Digital, I=Input, O=Output, Z=Tristate Output, R = Reserved
3) PU=internal pullup, PD=internal pulldown, HV = high voltage

5.2 Application Circuitry and External Component Characteristics

See recommended schematics in Figure 12. Component characteristics are presented in Table 18.

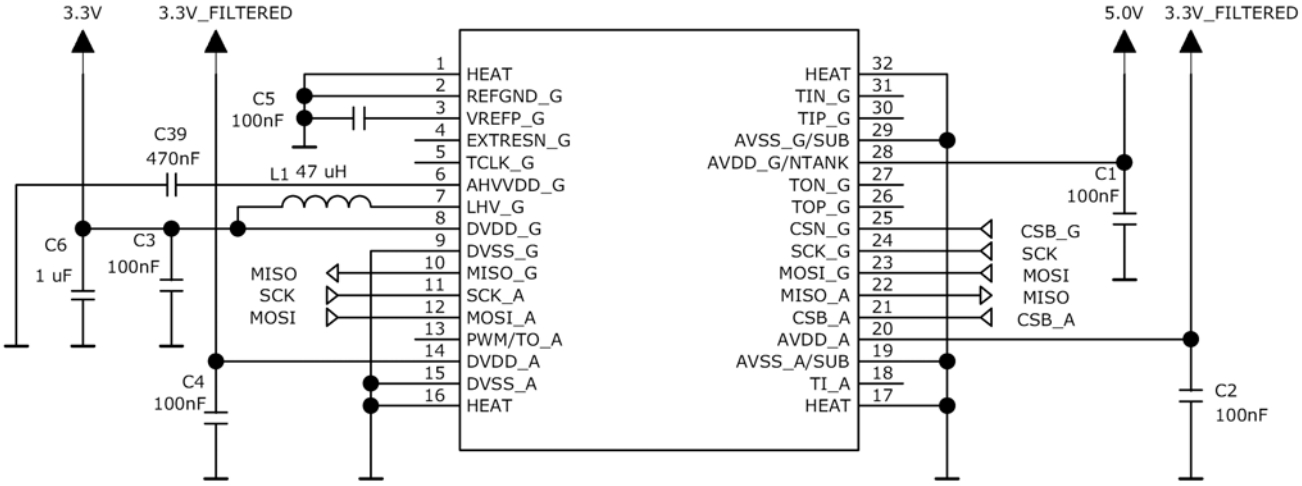

Figure 12. SCC1300 recommended circuit diagram.

Optional filtering recommendations for better PSRR (Power Supply Rejection Ratio) is presented in Figure 13. Please note that PSSR filtering is optional and not required if the 3.3V power supply is already stabile enough. RC filtering (R1 & C7 without L2) could also be sufficient for most cases.

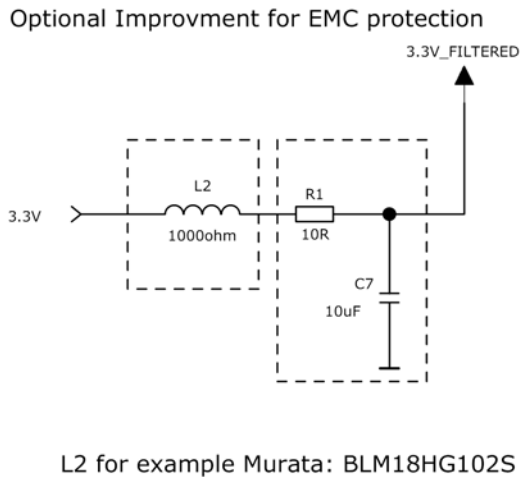

Figure 13. Optional filtering recommendation to improve PSRR if required.

5.2.1 Separate Analog and Digital Ground Layers with Long Power Supply Lines

If power supply routings/cablings are long separate ground cabling, routing and layers for analog and digital supply voltages should be used to avoid excessive power supply ripple.

In the recommended circuit diagram Figure 12 and layout Figure 15 joint ground is used as it is the simplest solution and is adequate as long as the supply voltage lines are not long (when connecting the SCC1300 directly to µC on the same PCB).

Table 18. SCC1300 external components.

Component	Parameter	Min	Typ	Max	Units
C1, C2, C3, C4, C5	Capacitance	70	100	130	nF
	ESR @ 1 MHz			100	mΩ
	Voltage rating	7			V
C39	Capacitance	376	470	564	nF
	ESR @ 1 MHz			100	mΩ
	Voltage rating	30			V
L1	Inductance	37	47	57	µH
	ESR L=47 µH			5	Ω
	Voltage rating	30			V
C6	Capacitance	0.7	1	1.3	µF
	ESR @ 1 MHz			100	mΩ
Optional for better PSRR:					
R1	Resistance		10		Ω
C7	Capacitance		4.7		µF
L2	Impedance		1k		Ω

5.3 Boost Regulator and Power Supply Decoupling in Layout

Recommended layout for DVDD_G/LHV pin decoupling is shown in Figure 14.

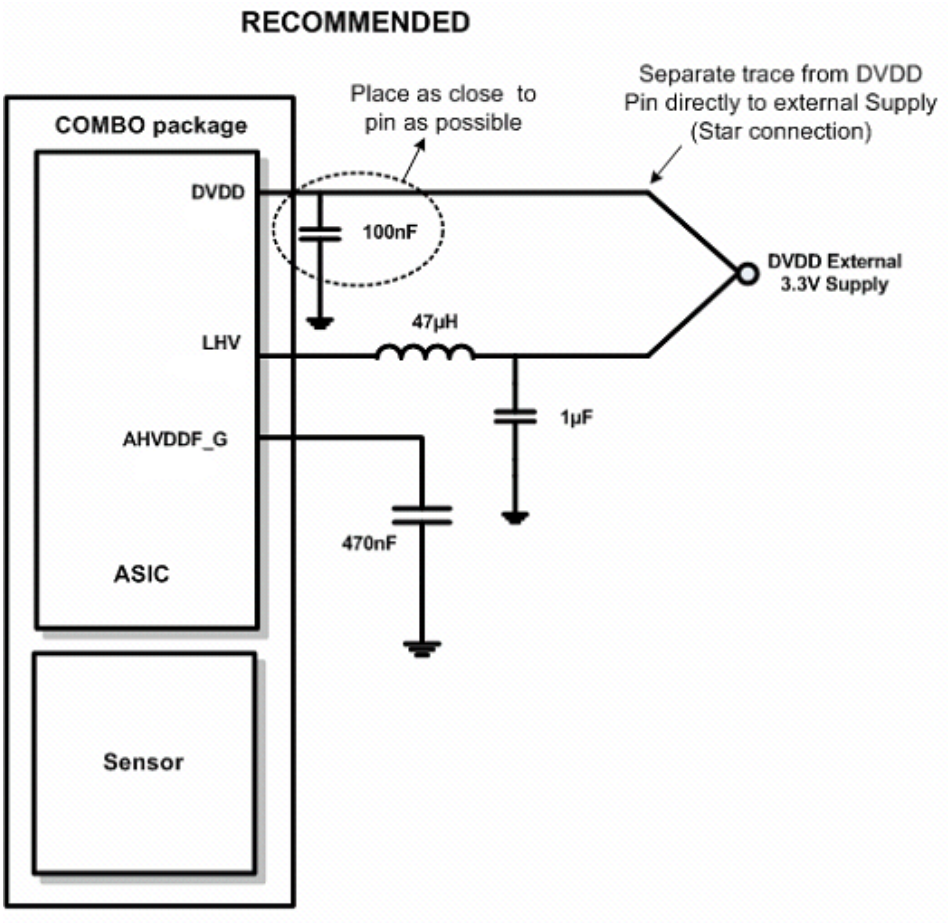

Figure 14. Layout recommendations for DVDD_G/LHV pin decoupling.

5.3.1 Layout Example

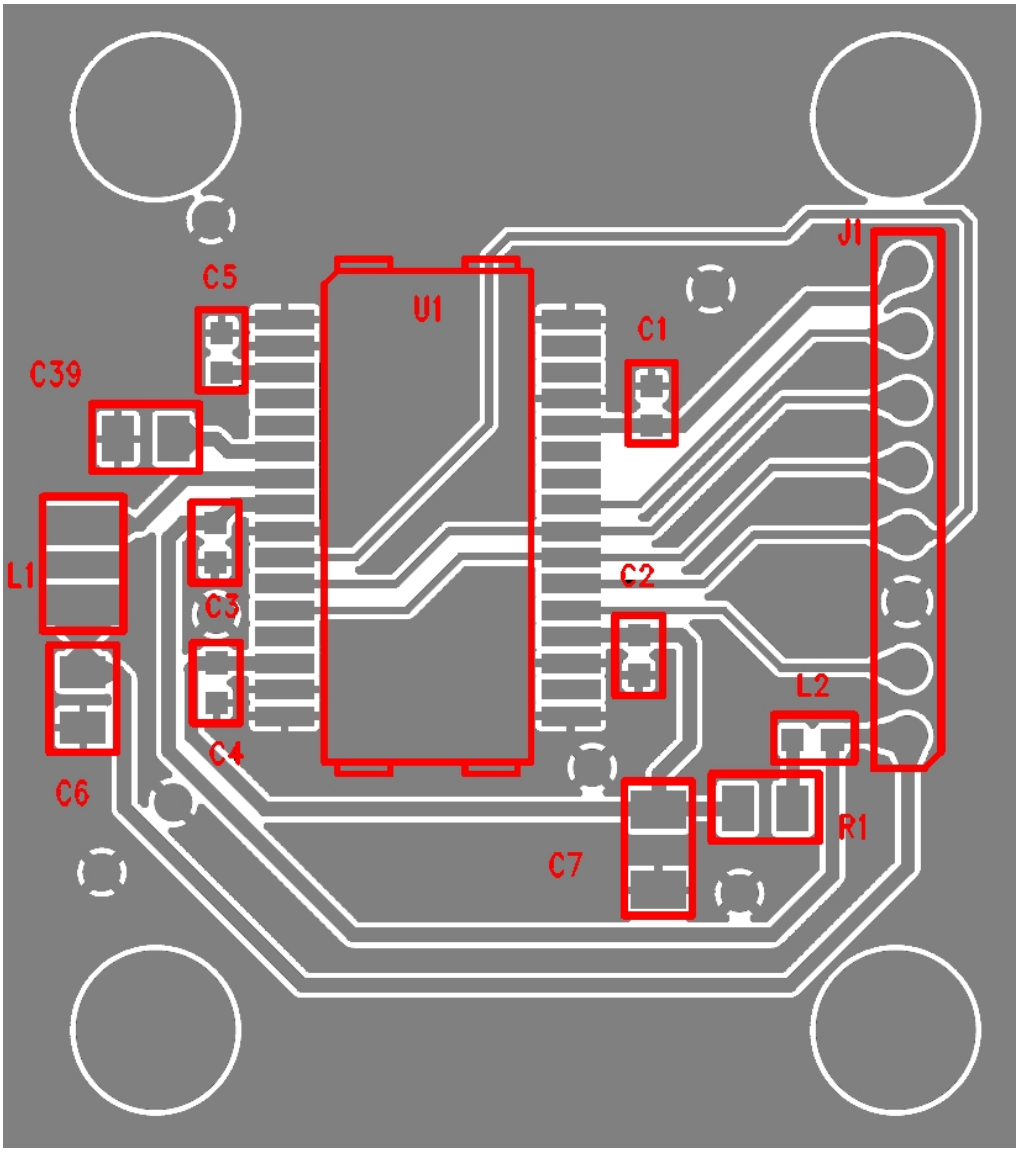

Figure 15. Example layout for SCC1300.

5.3.2 Thermal Connection

The component includes heat sink pins to transfer the internally generated heat from the package to outside. The thermal resistance to ambient should be low enough not to self heat the device. If the internal junction temperature gets too high compared to ambient, that may lead to out of specification behaviour.

Table 19. Thermal resistance.

Component	Parameter	Min	Typ	Max	Units
Thermal resistance $\Theta_{JA.}$	Total resistance from junction to ambient			50	°C/W

5.4 Measurement Axis and Directions

The SCC1300 positive/negative acceleration and angular rate measurement directions are shown below in Figure 16.

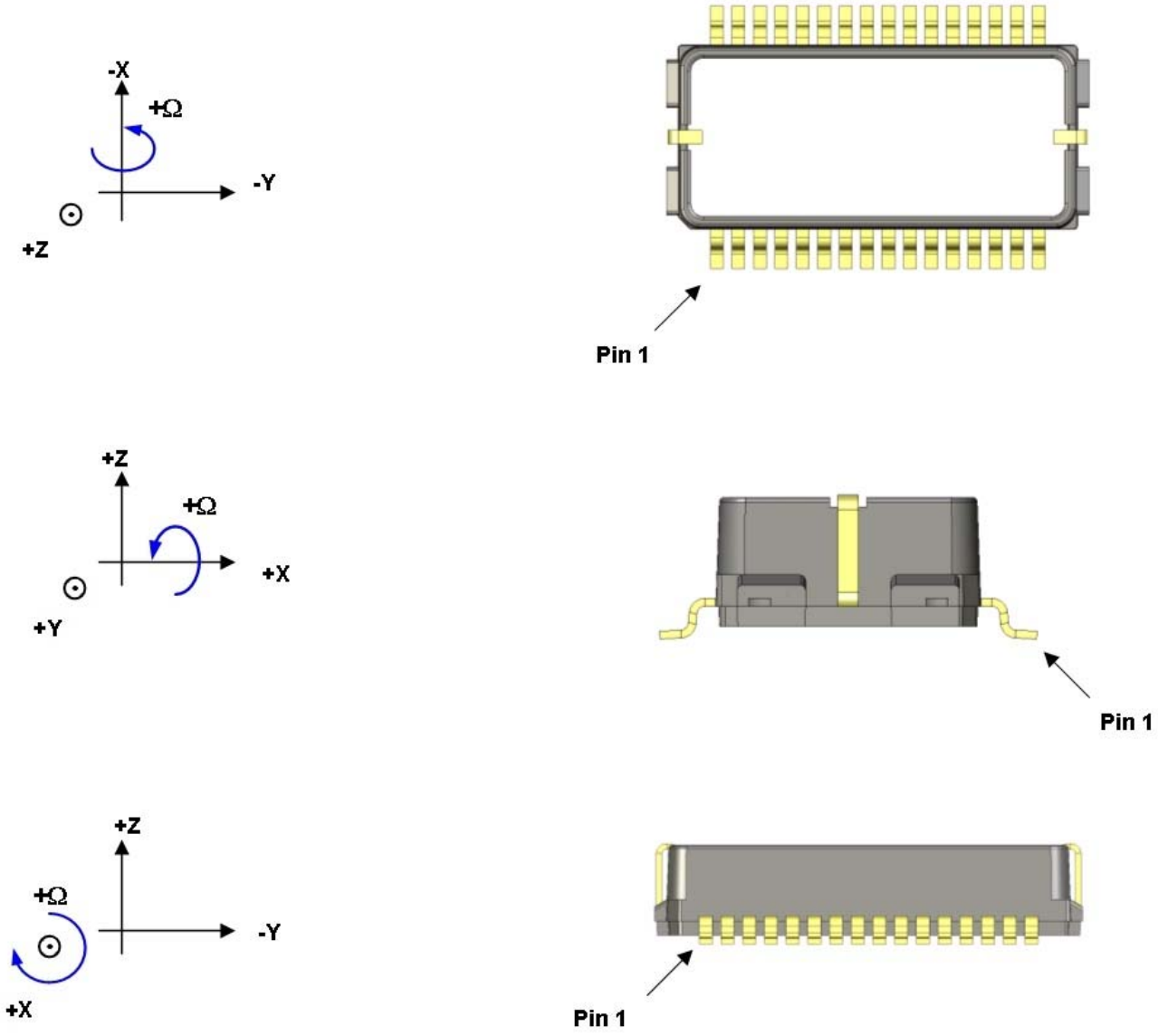

Figure 16. SCC1300 acceleration and angular rate measurement directions.

5.5 Package Characteristics

5.5.1 Package Outline Drawing

The SCC1300 package outline and dimensions are presented in Figure 17 and Table 20.

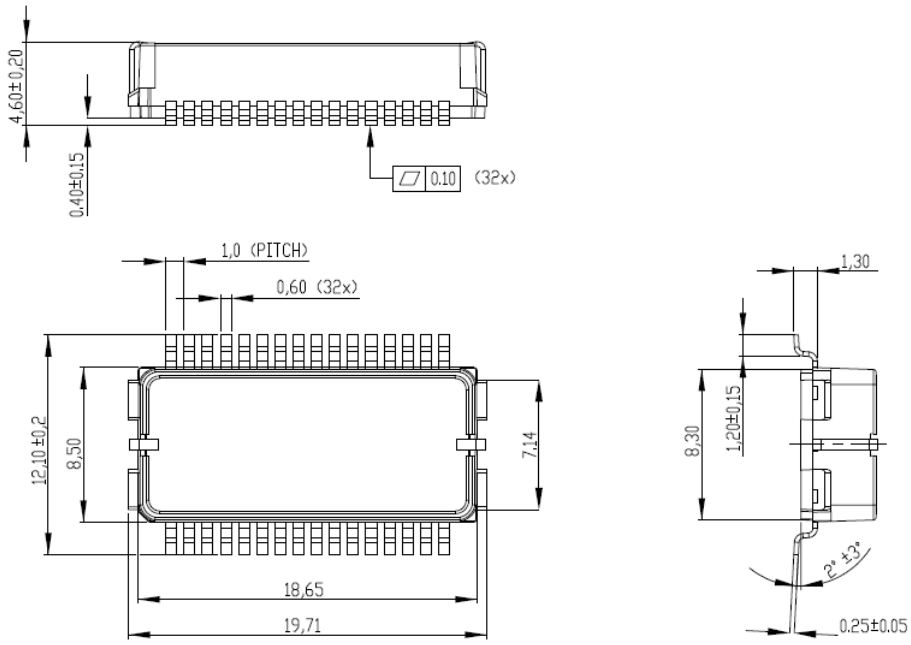

Figure 17. SCC1300 package outline and dimensions. All tolerances are according to ISO2768-f (see table in the below) unless otherwise specified.

Limits for linear measures (ISO2768-f)

Tollerance class	Limits in mm for nominal size in mm			
	0.5 to 3	Above 3 to 6	Above 6 to 30	Above 30 to 120
f (fine)	±0.05	±0.05	±0.1	±0.15

Table 20. SCC1300 package dimensions.

Component	Parameter	Min	Typ	Max	Units
Length	Without leads		19.71		mm
Width	Without leads		8.5		mm
Width	With leads		12.1		mm
Height	With leads (including stand-off and EMC lead)		4.60		mm
Lead pitch			1.0		mm

5.5.2 PCB Footprint

SCC1300 footprint dimensions are presented in Figure 18 and Table 21.

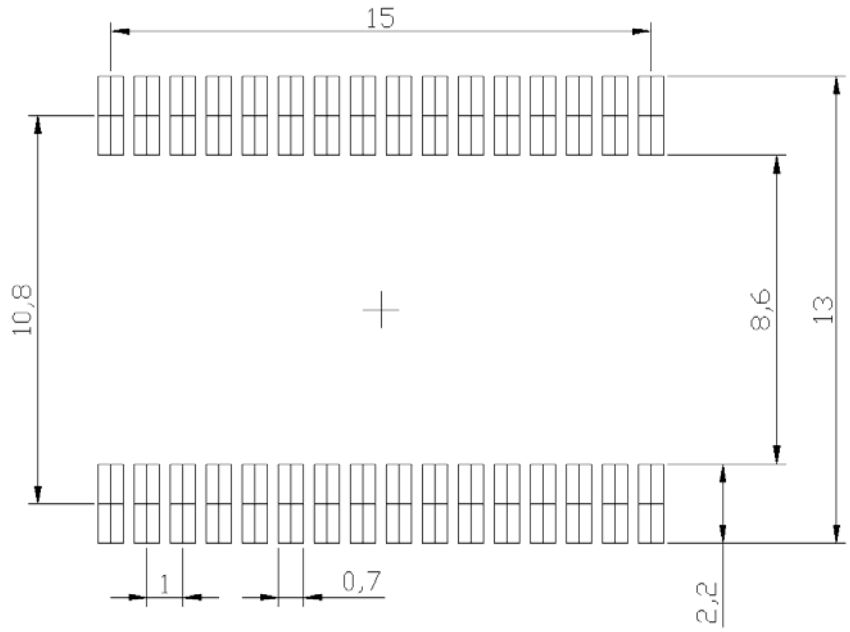

Figure 18. SCC1300 footprint.

Table 21. SCC1300 footprint dimensions.

Component	Parameter	Min	Typ	Max	Units
Footprint length	Without lead footprints		15.7		mm
Footprint width	Without lead footprints		13.0		mm
Footprint lead pitch	Long side leads		1.0		mm
Footprint lead length			2.20		mm
Footprint lead width	Long side leads		0.7		mm

5.6 Assembly instructions

Please refer to "Technical Note 82" document for assembly instructions.

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