REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Converted document to new boilerplate; corrected table I footnotes; corrected table I, analog input voltage maximum value; added footnote to clocking parameters; corrected figures 3, 6, and 7, timing diagrams; editorial changes throughout.	92-12-07	M. L. Poelking
B	Changes in accordance with NOR 5962-R064-94.	93-12-07	Monica L. Poelking
C	Update boilerplate to MIL-PRF-38535 requirements. - CFS	06-06-15	Thomas M. Hess

REV																				
SHEET																				
REV	C	C	C	C	C	C	C	C												
SHEET	15	16	17	18	19	20	21	22												

REV STATUS	REV	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C
OF SHEETS	SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14	

PMIC N/A

PREPARED
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STANDARD MICROCIRCUIT DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

CHECKED BY
Tim H. Noh

APPROVED BY
Don M. Cool

DRAWING APPROVAL DATE
91-09-11

REVISION LEVEL
C

MICROCIRCUIT, DIGITAL, CMOS, 8-BIT MICROCONTROLLER WITH A/D, PWM AND EPROM, MONOLITHIC SILICON

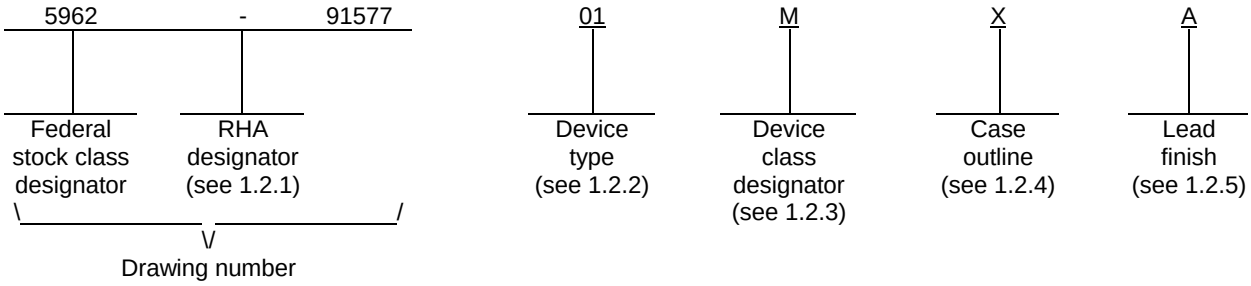
SIZE	CAGE CODE	
A	**67268**	**5962-91577**

SHEET 1 OF 22

1. SCOPE

1.1 Scope. This drawing documents two product assurance class levels consisting of high reliability (device classes Q and M) and space application (device class V). A choice of case outlines and lead finishes are available and are reflected in the Part or Identifying Number (PIN). When available, a choice of Radiation Hardness Assurance (RHA) levels is reflected in the PIN.

1.2 PIN. The PIN is as shown in the following example:



1.2.1 RHA designator. Device classes Q, and V RHA marked devices meet the MIL-PRF-38535 specified RHA levels and are marked with the appropriate RHA designator. Device class M RHA marked devices meet the MIL-PRF-38535, appendix A specified RHA levels and are marked with the appropriate RHA designator. A dash (-) indicates a non-RHA device.

1.2.2 Device type(s). The device type(s) identify the circuit function as follows:

Device type	Generic number	Circuit function
01	87C752	CMOS, 8-bit microcontroller with A/D, PWM, 2k EPROM memory (3.5 to 12 MHz)
02	87C752-16	CMOS, 8-bit microcontroller with A/D, PWM, 2k EPROM memory (3.5 to 16 MHz)
03	87C752	CMOS, 8-bit microcontroller with A/D, PWM, 2k one time programmable EPROM memory (3.5 to 12 MHz)
04	87C752-16	CMOS, 8-bit microcontroller with A/D, PWM, 2k one time programmable EPROM memory (3.5 to 16 MHz)

1.2.3 Device class designator. The device class designator is a single letter identifying the product assurance level as follows:

Device class	Device requirements documentation
M	Vendor self-certification to the requirements for MIL-STD-883 compliant, non-JAN class level B microcircuits in accordance with MIL-PRF-38535, appendix A
Q or V	Certification and qualification to MIL-PRF-38535

1.2.4 Case outline(s). The case outline(s) are as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style
X	GDIP1-T28 or CDIP2-T28	28	Dual-in-line 1/

1.2.5 Lead finish. The lead finish is as specified in MIL-PRF-38535 for device classes Q, and V or MIL-PRF-38535, appendix A for device class M.

1/ For device types 01 and 02, the lid shall be transparent to permit ultraviolet light erasure.

1.3 Absolute maximum ratings. 1/

Supply voltage V_{CC} to V_{SS} range	-0.5 V dc to +6.5 V dc
Voltage (any pin) to V_{SS} range	-0.5 V dc to V_{CC} + 0.5 V dc
Storage temperature range	-65°C to +150°C
Maximum power dissipation (P_D)	1.0 W
Lead temperature (soldering, 5 seconds)	+300°C
Thermal resistance, junction-to-case (θ_{JC})	See MIL-STD-1835

1.4 Recommended operating conditions.

Supply voltage range (V_{CC})	+4.5 V dc to +5.5 V dc
Maximum low level input voltage (except SDA, SCL)	$0.2V_{CC}$ – 0.25 V dc
Maximum low level input voltage (SDA, SCL)	$0.3V_{CC}$
Minimum high level input voltage (SDA, SCL)	$0.7V_{CC}$
Minimum high level input voltage (except X1, RST)	$0.2V_{CC}$ + 0.9 V dc
Minimum high level input voltage (X1, RST)	$0.7V_{CC}$
Case operating temperature range (T_C)	-55°C to +125°C
Oscillator frequency	3.5 MHz to 16 MHz

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATION

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-883 - Test Method Standard Microcircuits.
MIL-STD-1835 - Interface Standard Electronic Component Case Outlines.

DEPARTMENT OF DEFENSE HANDBOOKS

MIL-HDBK-103 - List of Standard Microcircuit Drawings.
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Copies of these documents are available online at http://assist.daps.dla.mil/quicksearch/ or http://assist.daps.dla.mil or from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

1/ Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements for device classes Q, and V shall be in accordance with MIL-PRF-38535 and as specified herein or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein. The individual item requirements for device class M shall be in accordance with MIL-PRF-38535, appendix A for non-JAN class level B devices and as specified herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535 and herein for device classes Q and V or MIL-PRF-38535, appendix A and herein for device class M.

3.2.1 Case outlines. The case outlines shall be in accordance with 1.2.4 herein.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.3 Block diagram. The block diagram shall be as specified on figure 2.

3.3 Electrical performance characteristics and postirradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and postirradiation parameter limits are as specified in table I and shall apply over the full case operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are defined in table I.

3.5 Marking. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked. For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device. For RHA product using this option, the RHA designator shall still be marked. Marking for device classes Q and V shall be in accordance with MIL-PRF-38535. Marking for device class M shall be in accordance with MIL-PRF-38535, appendix A.

3.5.1 Certification/compliance mark. The certification mark for device classes Q and V shall be a "QML" or "Q" as required in MIL-PRF-38535. The compliance mark for device class M shall be a "C" as required in MIL-PRF-38535, appendix A.

3.6 Certificate of compliance. For device classes Q and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see 6.6.1 herein). For device class M, a certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-HDBK-103 (see 6.6.2 herein). The certificate of compliance submitted to DSCC-VA prior to listing as an approved source of supply for this drawing shall affirm that the manufacturer's product meets, for device classes Q and V, the requirements of MIL-PRF-38535 and herein or for device class M, the requirements of MIL-PRF-38535, appendix A and herein.

3.7 Certificate of conformance. A certificate of conformance as required for device classes Q and V in MIL-PRF-38535 or for device class M in MIL-PRF-38535, appendix A shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change for device class M. For device class M, notification to DSCC-VA of change of product (see 6.2 herein) involving devices acquired to this drawing is required for any change that affects this drawing.

3.9 Verification and review for device class M. For device class M, DSCC, DSCC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

3.10 Microcircuit group assignment for device class M. Device class M devices covered by this drawing shall be in microcircuit group number 105 (see MIL-PRF-38535, appendix A).

3.11 Processing EPROM's. All testing requirements and quality assurance provisions herein shall be satisfied by the manufacturer prior to delivery.

3.11.1 Erasure of EPROM's. When specified, devices shall be erased in accordance with the procedures and characteristics specified in 4.5.

3.11.2 Programmability of EPROM's. When specified, devices shall be programmed to the specified pattern using the procedures and characteristics specified in 4.6 and table III.

3.11.3 Verification of erasure of programmability of EPROM's. When specified, devices shall be verified as either programmed to the specified pattern or erased. As a minimum, verification shall consist of performing a functional test (subgroup 7) to verify that all bits are in the proper state. Any bit that does not verify to be in the proper state shall constitute a device failure, and shall be removed from the lot.

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions 1/ $-55°C \le T_C \le +125°C$, $4.5\ V \le V_{CC} \le 5.5\ V$ unless otherwise specified		Group A subgroups	Device types	Limits		Unit
						Min	Max	
Output low voltage, Ports 1, 3, 0.3, and 0.4 (PWM disabled)	V_{OL}	I_{OL} = 1.6 mA	V_{CC} = 4.5 V, V_{IN} = V_{IL} max, V_{IH} min	1, 2, 3	All		0.45	V
Output low voltage, Port 0.2	V_{OL1}	I_{OL} = 3.2 mA					0.45	V
Ports 0.0 and 0.1 (I^2C) - Drivers output low voltage	V_{OL2}	I_{OL} = 3.2 mA					0.45	V
Output high voltage, Ports 1, 3, 0.3 and 0.4 (PWM disabled)	V_{OH}	I_{OH} = -60 µA				2.4		V
		I_{OH} = -25 µA				$0.75V_{CC}$		
		I_{OH} = -10 µA				$0.9V_{CC}$		
Output high voltage, Port 0.4 (PWM disabled)	V_{OH1}	I_{OH} = -400 µA				2.4		V
		I_{OH} = -40 µA				$0.9V_{CC}$		
Logic 0 input current, ports 1, 3, 0.3, and 0.4 (PWM disabled)	I_{IL}	V_{IN} = 0.45 V, V_{CC} = 5.5 V				0	-50	µA
Logic 1 to 0 transition current, ports 1, 3, 0.3, and 0.4	I_{TL}	V_{IN} = 2.0 V, V_{CC} = 5.5 V				0	-650	µA
Input leakage current, port 0.0, 0.1, and 0.2	I_{LI}	V_{IN} = V_{CC}	V_{CC} = 5.5 V			0	10	µA
		V_{IN} = 0.45 V				0	-10	
Reset pull-down resistor	R_{RST}					25	175	kΩ
Driver, receiver combined capacitance	C	See 4.4.1.b		4	All		10	pF
Pin capacitance	$C_{I/O}$	See 4.4.1.b					10	pF

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ $-55°C \le T_C \le +125°C$ $4.5\ V \le V_{CC} \le 5.5\ V$ unless otherwise specified	Group A subgroups	Device types	Limits		Unit
					Min	Max	
Supply current, active	I_{CC}	V_{CC} = 5.5 V, 2/ 3/ See figure 3.	1, 2, 3	01, 03		21	mA
				02, 04		24	
Supply current, idle	I_{CC1}	V_{CC} = 5.5 V, 3/ 4/ See figure 3.		01, 03		4	mA
				02, 04		5	
Power down current	I_{PD}	V_{CC} = 2 V, 5.5 V 5/	1, 2, 3	All		50	µA
V_{PP} program voltage	V_{PP}	V_{CC} = 4.5 V, 5.5 V V_{SS} = 0 V	1	All	12.5	13.0	V
Program current	I_{PP}	V_{PP} = 13.0 V				50	mA
A/D converter parameters 6/							
Analog supply voltage	AV_{CC}	$AV_{CC} = V_{CC} \pm 0.2$ V 7/	1, 2, 3	All	4.5	5.5	V
Analog input voltage	AV_{IN}	AV_{CC} = 5.12 V			AV_{SS} – 0.2	AV_{CC} + 0.2	V
Analog input capacitance	C_{IA}	See 4.4.1b	4	All		15	pF
Sampling time	T_{ADS}	8/	9, 10, 11	All		$8t_{CY}$	s
Conversion time	T_{ADS}	8/				$40t_{CY}$	s
Resolution	R		4, 5, 6	All		8	bits
Differential non-linearity	D_{NL}	8/				±1	LSB
Zero scale offset	OS_e					±1	LSB
Full scale gain error	G_e					0.4	%
Channel to channel matching	M_{CTC}	9/				±1	LSB
Crosstalk	C_T	0 – 100 kHz 7/ 8/				-60	dB

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ $-55°C \le T_C \le +125°C$ $4.5\ V \le V_{CC} \le 5.5\ V$ unless otherwise specified	Group A subgroups	Device types	Limits		Unit
					Min	Max	
Functional test		See 4.4.1c	7, 8	All			
Oscillator frequency	$1/t_{CLCL}$		9, 10, 11	01, 03	3.5	12	MHz
variable clock				02, 04	3.5	16	
External clock (See figure 4)							
High time, variable clock	t_{CHCX}	9/	9, 10, 11	All	20		ns
Low time, variable clock	t_{CLCX}	9/			20		ns
Rise time, variable clock	t_{CLCH}	9/				20	ns
Fall time, variable clock	t_{CHCL}	9/				20	ns

1/ Unless otherwise specified, parameters are valid over operating temperature range. All parameters must be tested by using the worst case forcing condition unless otherwise noted.

2/ I_{CC} is measured with all output pins disconnected; X1 driven with t_{CLCH}, t_{CHCL} = 5 ns, $V_{IL} = V_{SS} + 0.5$ V, $V_{IH} = V_{CC} - 0.5$ V; X2 = NC; RST = port 0 = V_{CC}. I_{CC} will be slightly higher if a crystal oscillator is used.

3/ The resistor ladder network is not disconnected in the power down or idle modes. Thus, to conserve power the user may remove AV_{CC}.

4/ Idle I_{CC} is measured with all output pins disconnected; X1 driven with t_{CLCH}, t_{CHCL} = 5 ns, $V_{IL} = V_{SS} + 0.5$ V, $V_{IH} = V_{CC} - 0.5$ V; X2 = NC; port 0 = V_{CC}; RST = V_{SS}.

5/ Power-down I_{CC} is measured with all output pins disconnected; port 0 = V_{CC}; X2, X1 = NC; RST = V_{SS}.

6/ Analog inputs (A/D guaranteed only with quartz window covered).

7/ If the A/D function is not required, or if the A/D function is only needed periodically, then AV_{CC} may be removed without affecting the operation of the digital circuitry. Contents of ADCON and ADAT are not guaranteed to be valid. Digital inputs on P1.0 – P1.4 will not function normally.

8/ Tested, initially and after any design changes that affect the parameters.

9/ If not tested, guaranteed to the limit specified in table I.

Device types:	All
Case outline:	X
Terminal number	Terminal symbol
1	P3.4/A4
2	P3.3/A3
3	P3.2/A2/A10
4	P3.1/A1/A9
5	P3.0/A0/A8
6	P0.2/V_{PP}
7	P0.1/SDA/OE-PGM
8	P0.0/SCL/ASEL
9	RST
10	X2
11	X1
12	V_{SS}
13	P1.0/ADC0/D0
14	P1.1/ADC1/D1
15	P1.2/ADC2/D2
16	P1.3/ADC3/D3
17	P1.4/ADC4/D4
18	AV_{SS}
19	AV_{CC}
20	P1.5/$\overline{INT0}$
21	P1.6/$\overline{INT1}$/D6
22	P1.7/T0/D7
23	P0.3
24	P0.4/PWM OUT
25	P3.7/A7
26	P3.6/A6
27	P3.5/A5
28	V_{CC}

FIGURE 1. Terminal connections.

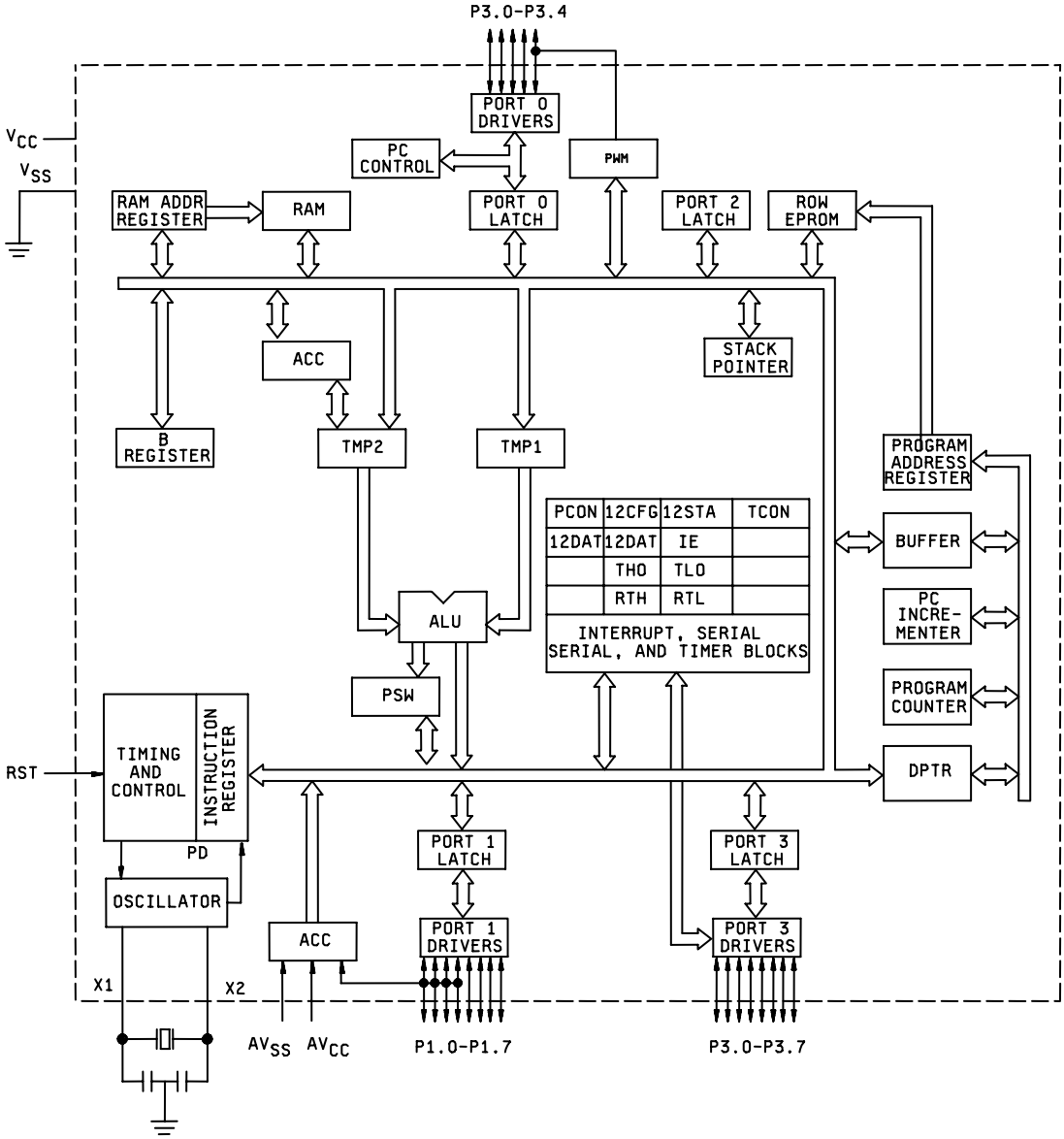
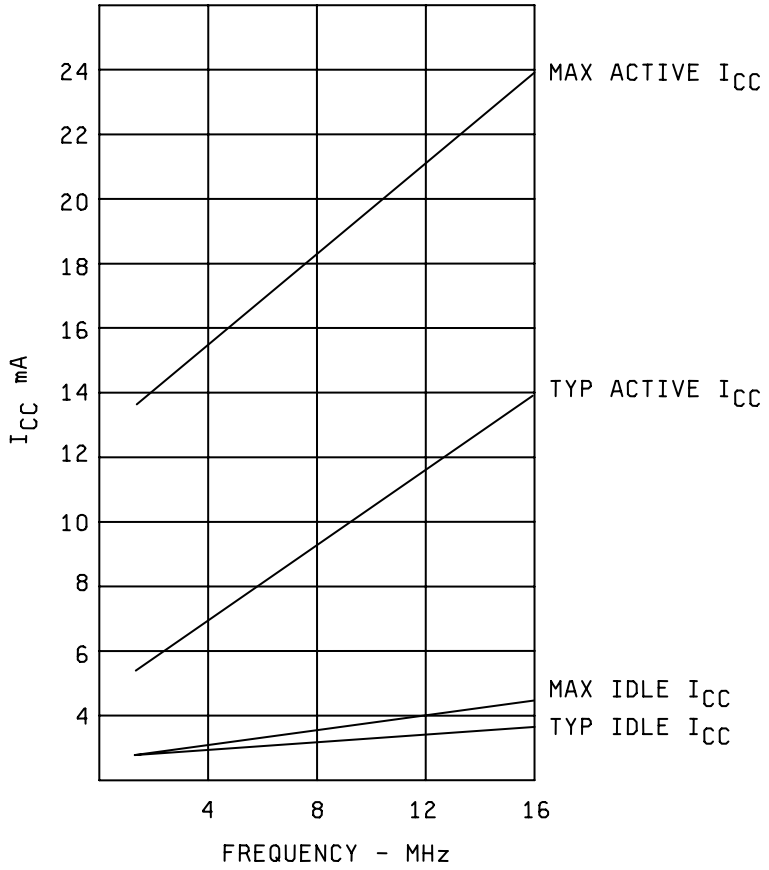


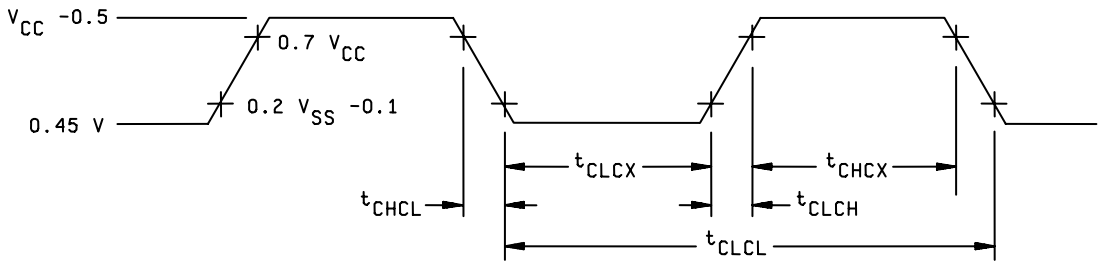
FIGURE 2. Block diagram.



Maximum I_{CC} values taken at V_{CC} = 5.5 V and worst case temperature.
Typical I_{CC} values taken at V_{CC} = 5.0 V and 20°C.

FIGURE 3. I_{CC} versus frequency.

EXTERNAL CLOCK DRIVE



AC TESTING INPUT/OUTPUT

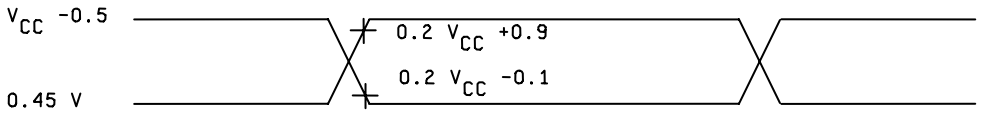


FIGURE 4. Switching waveforms.

4. VERIFICATION

4.1 Sampling and inspection. For device classes Q and V, sampling and inspection procedures shall be in accordance with MIL-PRF-38535 or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein. For device class M, sampling and inspection procedures shall be in accordance with MIL-PRF-38535, appendix A.

4.2 Screening. For device classes Q and V, screening shall be in accordance with MIL-PRF-38535, and shall be conducted on all devices prior to qualification and technology conformance inspection. For device class M, screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection.

4.2.1 Additional criteria for device class M.

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition A, B, C, or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015.

(2) T_A = +125°C, minimum.

b. Interim and final electrical test parameters shall be as specified in table II herein.

c. A data retention stress test shall be included as part of the screening procedure and shall consist of the following steps:

Margin test method A

(1) Program greater than 95 percent of the bit locations, including the slowest programming cell (see 3.11.2). The remaining cells shall provide a worst case speed pattern.

(2) Bake, unbiased for 72 hours at +140°C to screen for data retention lifetime.

(3) Perform a margin test using V_m = +5.9 V at +25°C using loose timing (i.e., $T_{ACC} > 1$ µs).

(4) Perform dynamic burn-in (see 4.2.1a).

(5) Margin at V_m = +5.9 V.

(6) Perform electrical tests (see 4.2).

(7) Erase (see 3.11.1), except devices submitted for groups A, B, C, and D testing.

(8) Verify erasure (see 3.11.3).

Margin test method B

(1) Program at 25°C, 100 percent of the bits.

(2) Bake, unbiased for 24 hours at +250°C.

(3) Perform margin test at V_m = +5.9 V.

(4) Erase (see 3.11.1).

(5) Perform interim electrical tests in accordance with table II.

(6) For device types 01 and 02, program 100 percent of the bits and verify (see 3.11.2).

(7) Perform burn-in (see 4.2.1a).

(8) One-hundred percent test at 25°C (group A, subgroups 1 and 7). V_m = 5.9 V with loose timing, apply PDA. For device types 03 and 04, the virgin state of the devices must be verified.

(9) Perform remaining final electrical subgroups and group A testing.

(10) For device types 01 and 02, erase, devices may be submitted for groups B, C, and D at this time.

(11) For device types 01 and 02, verify erasure (see 3.11.3).

(12) Steps 1 through 4 are performed at wafer level.

4.2.2 Additional criteria for device classes Q and V.

a. The burn-in test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The burn-in test circuit shall be maintained under document revision level control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015 of MIL-STD-883.

b. Interim and final electrical test parameters shall be as specified in table II herein.

c. Additional screening for device class V beyond the requirements of device class Q shall be as specified in MIL-PRF-38535, appendix B.

4.3 Qualification inspection for device classes Q and V. Qualification inspection for device classes Q and V shall be in accordance with MIL-PRF-38535. Inspections to be performed shall be those specified in MIL-PRF-38535 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4 Conformance inspection. Technology conformance inspection for classes Q and V shall be in accordance with MIL-PRF-38535 including groups A, B, C, D, and E inspections and as specified herein. Quality conformance inspection for device class M shall be in accordance with MIL-PRF-38535, appendix A and as specified herein. Inspections to be performed for device class M shall be those specified in method 5005 of MIL-STD-883 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4.1 Group A inspection.

a. Tests shall be as specified in table II herein.

b. Subgroup 4 (C, $C_{I/O}$, and C_{IA}) shall be measured only for the initial test and after process or design changes which may affect capacitance. A minimum sample size of five devices with zero rejects shall be required.

c. For device class M, subgroups 7 and 8 tests shall be sufficient to verify the truth table. For device classes Q and V, subgroups 7 and 8 shall include verifying the functionality of the device.

d. For device types 01 and 02, all devices selected for testing shall have the EPROM programmed with a checkerboard pattern or equivalent. After completion of all testing, the devices shall be erased and verified (except devices submitted for groups C and D testing).

e. For device types 03 and 04, unprogrammed devices shall be tested for programmability and functionality compliance to the requirements of group A, subgroups 7 and 8. Either of two techniques is acceptable:

(1) Testing the entire lot using additional built in test circuitry which allows the manufacturer to verify programmability and functionality without programming the user array. If this is done, the resulting test patterns shall be verified on all devices during subgroups 7 and 8, group A testing per the sampling plan specified in MIL-STD-883, method 5005.

(2) If such compliance cannot be tested on an unprogrammed device, a sample shall be selected to satisfy programmability requirements prior to performing subgroups 7 and 8. Twelve devices shall be submitted to programming. If more than 2 devices fail to program, the lot shall be rejected. At the manufacturer's option, the sample may be increased to 24 total devices with no more than 4 total device failures allowable. (Ten devices from the programmability sample shall be submitted to the requirements of group A, subgroup 7 and 8. If more than 2 total devices fail, the lot shall be rejected. At the manufacturer's option, the sample may be increased to 20 total devices with no more than 4 total device failures allowable.)

TABLE II. Electrical test requirements.

Test requirements	Subgroups (in accordance with MIL-STD-883, method 5005, table I)	Subgroups (in accordance with MIL-PRF-38535, table III)	
	Device class M	Device class Q	Device class V
Interim electrical parameters (see 4.2)	---	---	---
Final electrical parameters (see 4.2)	1, 2, 3, 5, 6, 7, 8, 9, 10, 11 1/	1, 2, 3, 5, 6, 7, 8, 9, 10, 11 1/	1, 2, 3, 5, 6, 7, 8, 9, 10, 11 2/
Group A test requirements (see 4.4)	1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11	1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11	1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11
Group C end-point electrical parameters (see 4.4)	2, 5, 8a, 10	2, 5, 8a, 10	2, 5, 8a, 10
Group D end-point electrical parameters (see 4.4)	2, 5, 8a, 10	2, 5, 8a, 10	2, 5, 8a, 10
Group E end-point electrical parameters (see 4.4)	1, 5, 7, 9	1, 5, 7, 9	1, 5, 7, 9

1/ PDA applies to subgroup 1.
2/ PDA applies to subgroups 1 and 7.

4.4.2 Group C inspection. The group C inspection end-point electrical parameters shall be as specified in table II herein.

4.4.2.1 Additional criteria for device class M. Steady-state life test conditions, method 1005 of MIL-STD-883:

a. Test condition A, B, C, or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1005 of MIL-STD-883.

b. T_A = +125°C, minimum.

c. Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

d. For device types 01 and 02, all devices selected for testing shall be programmed with a checkerboard pattern or equivalent. After completion of all testing, the devices shall be erased and verified.

e. For device types 03 and 04, the virgin state of the device must be verified.

4.4.2.2 Additional criteria for device classes Q and V. The steady-state life test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The test circuit shall be maintained under document revision level control by the device manufacturer's TRB in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1005 of MIL-STD-883.

4.4.3 Group D inspection. The group D inspection end-point electrical parameters shall be as specified in table II herein.

4.4.4 Group E inspection. Group E inspection is required only for parts intended to be marked as radiation hardness assured (see 3.5 herein).

a. End-point electrical parameters shall be as specified in table II herein.

b. For device classes Q and V, the devices or test vehicle shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535 for the RHA level being tested. For device class M, the devices shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535, appendix A for the RHA level being tested. All device classes must meet the postirradiation end-point electrical parameter limits as defined in table I at T_A = +25°C ±5°C, after exposure, to the subgroups specified in table II herein.

4.5 Erasing procedure. The recommended erasure procedure is exposure to ultraviolet light (at 2537 Angstroms) to an integrated dose of at least 15 W-s/cm^2. Exposing the EPROM to an ultraviolet lamp of 12,000 μW/cm^2 rating for 20 to 30 minutes, at a distance of about one inch, should be sufficient.

4.6 Programming procedures. The programming characteristics in table III and the following procedures shall be used for programming the device:

a. Connect the device in the electrical configuration (see figure 5) for programming. The waveforms of figure 6 and programming characteristics of table III shall apply.

b. Initially and after each erasure, all bits are in the high “H” state. Information is introduced by selectively programming “L” into the desired bit locations. A programmed “L” can be changed to an “H” by ultraviolet light erasure (see 4.5).

TABLE III. EPROM Programming and verification characteristics.

Parameter	Symbol	Conditions	Limits		Units
			Min	Max	
Oscillator frequency	$1/t_{CLCL}$	1/ See figure 7.	1.2	6	MHz
Address setup to $\overline{PROG}$ low	t_{AVGL} 2/		$10\ \mu s + 24t_{CLCL}$		ns
Address hold after $\overline{PROG}$	t_{GHAX}		$48t_{CLCL}$		ns
Data setup to $\overline{PROG}$ low	t_{DVGL}		$38t_{CLCL}$		ns
Data hold after $\overline{PROG}$	t_{GHDX}		$36t_{CLCL}$		ns
V_{PP} setup to $\overline{PROG}$ low	t_{SHGL}		10		µs
V_{PP} hold after $\overline{PROG}$	t_{GHSL}		10		µs
$\overline{PROG}$ width	t_{GLGH}		90	110	µs
V_{PP} low to data valid	t_{AVQV} 3/			$48t_{CLCL}$	ns
$\overline{PROG}$ high to $\overline{PROG}$ low	t_{GHGL}		10		µs
P0.0 (sync pulse) low	t_{SYNL}		$4t_{CLCL}$		ns
P0.0 (sync pulse) high	t_{SYNH}		$8t_{CLCL}$		ns
ASEL high time	t_{MASEL}		$13t_{CLCL}$		ns
Address hold time	t_{HAHLD}		$2t_{CLCL}$		ns
Address setup to ASEL	t_{HASET}		$13t_{CLCL}$		ns
Low address to address stable	t_{ADSTA}		$13t_{CLCL}$		ns

1/ For programming specifications, T_A = 21°C to 27°C, V_{CC} = 5 V ±10 percent, V_{SS} = 0 V.
2/ Address should be valid at least $24t_{CLCL}$ before rising edge of P0.2(V_{PP}).
3/ For a pure verify mode, i.e., no program mode in between, t_{AVQV} is $14t_{CLCL}$ maximum.

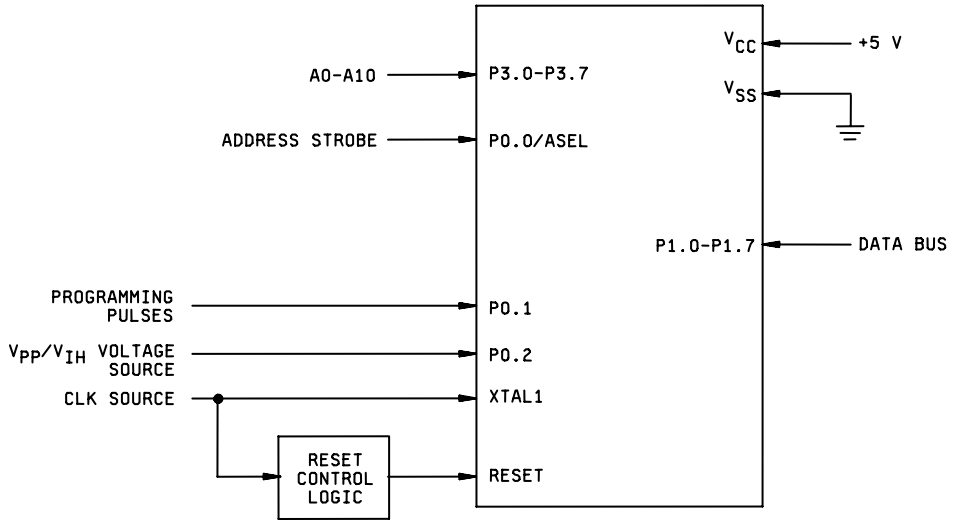


FIGURE 5. Programming configuration.

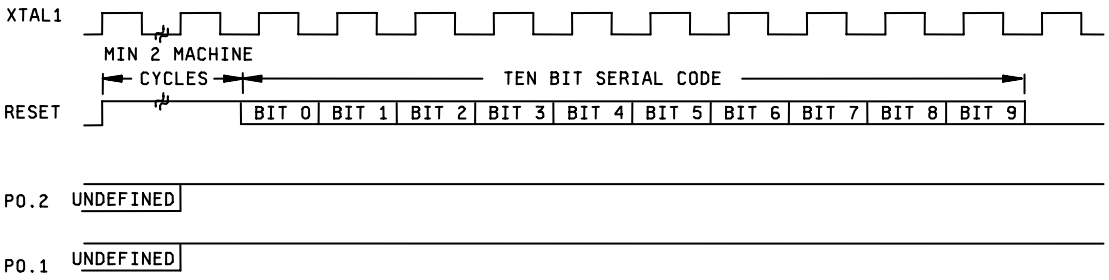


FIGURE 6. Entry into program/verify modes.

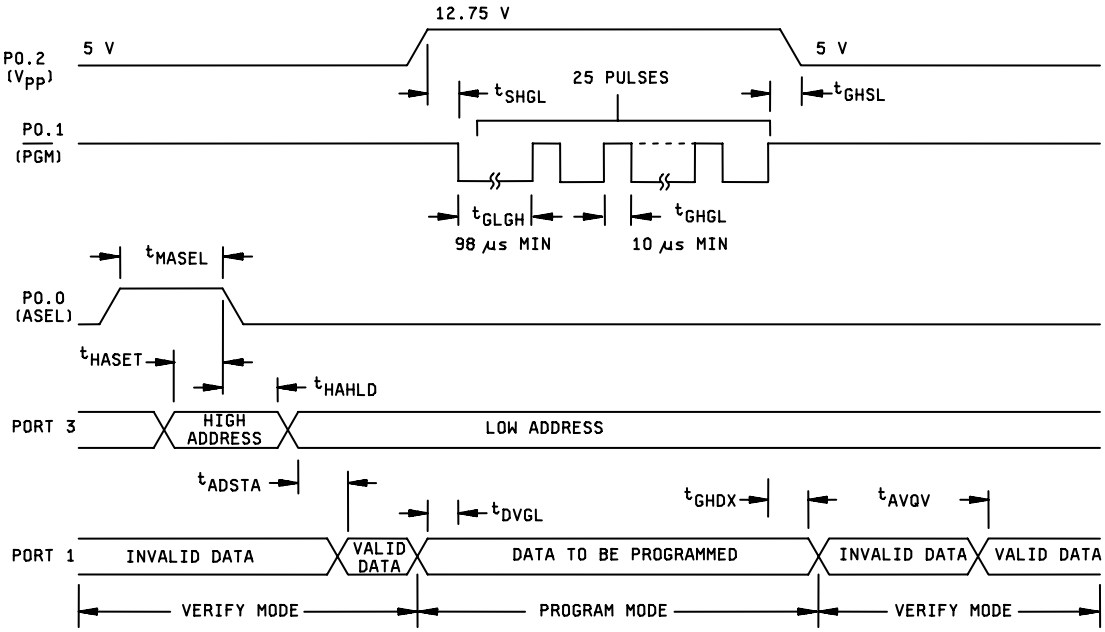


FIGURE 7. Program/verify cycle.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535 for device classes Q and V or MIL-PRF-38535, appendix A for device class M.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.1.1 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor prepared specification or drawing.

6.1.2 Substitutability. Device class Q devices will replace device class M devices.

6.2 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished using DD Form 1692, Engineering Change Proposal.

6.3 Record of users. Military and industrial users should inform Defense Supply Center Columbus (DSCC) when a system application requires configuration control and which SMD's are applicable to that system. DSCC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DSCC-VA, telephone (614) 692-0544.

6.4 Comments. Comments on this drawing should be directed to DSCC-VA, Columbus, Ohio 43218-3990, or telephone (614) 692-0547.

6.5 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-PRF-38535 and MIL-HDBK-1331 and as follows in table IV.

6.6 Sources of supply.

6.6.1 Sources of supply for device classes Q and V. Sources of supply for device classes Q and V are listed in QML-38535. The vendors listed in QML-38535 have submitted a certificate of compliance (see 3.6 herein) to DSCC-VA and have agreed to this drawing.

6.6.2 Approved sources of supply for device class M. Approved sources of supply for class M are listed in MIL-HDBK-103. The vendors listed in MIL-HDBK-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DSCC-VA.

TABLE IV. Symbols, definitions, and functional descriptions.

Mnemonic	Type	Name and function
V_{SS}		Ground: O V reference.
V_{CC}		Power Supply: Supply voltage during normal, idle, and power-down operation.
P0.0 – P0.4	I/O	Port 0: A 5-bit bidirectional port. Port P0.0 – P0.2 are open drain. Port P0.0 – P0.2 pins that have 1's written to them float, and in that state can be used as high-impedance inputs. P0.3 – P0.4 are bidirectional I/O port pins with internal pull-ups. Port 0 also serves as the serial I^2C interface. When this feature is activated by software, SCL and SDA are driven low in accordance with the I^2C protocol. These pins are driven low if the port register bit is written with a 0 or if the I^2C subsystem presents a 0. The state of the pin can always be read from the port register by the program. Ports P0.3 and P0.4 have internal pull-ups that function identically to Port 3. Pins that have 1's written to them are pulled high by the internal pull-ups and can be used as inputs. To comply with the I^2C specification, P0.0 and P0.1 are open drain bidirectional I/O pins with the electrical characteristics listed in table I. While these differ from "standard TTL" characteristics, they are close enough for the pins to still be used as general-purpose I/O in non-I^2C applications.
	I	V_{CC}(P0.2) - Programming voltage input.
	I	OE/PGM(P0.1) - Input which specifies verify mode (output enable) or the program mode. OE/PGM - 1 output enabled (verify mode). OE/PGM - Program mode.
	O	ASEL (P0.0) - Input which indicates which bits of the EPROM address are applied to Port 3. ASEL - 0 low address byte available on Port 3. ASEL - 1 high address byte available on Port 3 (only the three least significant bits are used).
P1.0 – P1.7	I/O	Port 1: Port 1 is an 8-bit bidirectional I/O port with internal pull-ups. Port 1 pins that have 1's written to them are pulled high by the internal pull-ups and can be used as inputs. P0.3 – P0.4 pins are bidirectional I/O port pins with internal pull-ups. As inputs, port 1 pins that are externally pulled low will source current because of the internal pull-ups (see DC electrical characteristics: I_{IL}). Port 1 also serves the special function features of the 80C51 family as listed below:
	I	INT0(P1.5): External interrupt.
	I	INT1(P1.6): external interrupt.
	I	T0(P1.7): Timer 0 external input.
	I	ADC0 (P1.0) – ADC4 (P1.4): Port 1 also functions as the inputs to the five channel multiplexed A/D converter. These pins can be used as outputs only if the A/D function has been disabled. These pins can be used as inputs while the A/D converter is enabled. Port 1 also serves to output the addressed EPROM contents in the verify mode and accepts as inputs the value to program into the selected address during the program mode.

TABLE IV. Symbols, definitions, and functional descriptions - Continued.

Mnemonic	Type	Name and function
P3.0 – P3.7	I/O	Port 3: Port 3 is an 8-bit bidirectional I/O port with internal pull-ups. Port 3 pins that have 1's written to them are pulled high by the internal pull-ups and can be used as inputs. As inputs, Port 3 pins that are externally being pulled low will source current because of the pull-ups (see DC characteristics: I_{IL}). Port 3 also functions as the address input for the EPROM memory location to be programmed (or verified). The 11-bit address is multiplexed into the port as specified by P0.0/ASEL.
RST	I	Reset: A high on this pin for two machine cycles while the oscillator is running resets the device. An internal diffused resistor to V_{SS} permits a power-on RESET using only an external capacitor to V_{CC}. After the device is reset, a 10-bit serial sequence, sent LSB first, applied to RESET places the device in the programming state allowing programming address, data, and V_{PP} to be applied for programming or verification purposes. The RESET serial sequence must be synchronized with the X1 input.
X1	I	Crystal 1: Input to the inverting oscillator amplifier and input to the internal clock generator circuits. X1 also serves as the clock to strobe in a serial bit stream into RESET to place the device in the programming state.
X2	O	Crystal 2: Output from the inverting oscillator amplifier.
AV_{CC}	I	Analog power supply: Analog supply voltage and reference input.
AV_{SS}	I	Analog power supply: Analog supply and reference ground.

STANDARD MICROCIRCUIT DRAWING BULLETIN

DATE: 06-06-15

Approved sources of supply for SMD 5962-91577 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 and QML-38535 during the next revision. MIL-HDBK-103 and QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DSCC-VA. This information bulletin is superseded by the next dated revision of MIL-HDBK-103 and QML-38535. DSCC maintains an online database of all current sources of supply at http://www.dscc.dla.mil/Programs/Smcr/.

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 2/
5962-9157701MXA	0C7V7	87C752/BXA
5962-9157702MXA	0C7V7	87C752-16/BXA
5962-9157703MXA	0C7V7	87C752/BXA OT
5962-9157704MXA	0C7V7	87C752-16/BXA OT

1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed contact the vendor to determine its availability.

2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

Vendor CAGE number	Vendor name and address
0C7V7	QP Semiconductor 2945 Oakmead Village Court Santa Clara, CA 95051

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